Revision History

Rev. No.	History	Issue Date	Remark
2.0	Initial issue with new naming rule	Mar. 01, 2005	
2.1	Revise 1. page 2 & 4: page address inputs 2. Add Vcc absolute max. in page 5	Nov. 23, 2005	
2.2	Modify Deep Power Down Mode & Page Mode	Jun. 15, 2006	
2.3	Revise DC/AC Char.	Oct. 29, 2007	
2.4	Change wafer process from 0.13um to 90nm	Aug. 26, 2008	
2.5	Add 48BGA-6*8mm package	Jan. 06, 2010	
2.6	Delete Die form information	Apr.12,2010	
2.7	Add the 48BGA-6*8mm package dimensions: D2 and E2	Aug.26,2010	

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■ Product Description

The CS26LV32163 is a 32M-bit PSRAM organized as 2M words by 16 bits. It provides high density, high speed and low power. The device operates single power supply. The device also features SRAM-like W/R timing whereby the device is controlled by /CE, /OE and /WE on asynchronous. The device has the page access operation. Page size is 16 words. The device also supports deep power-down mode, realizing low-power standby. The CS26LV32163 is available die form and 48-Ball BGA package.

■ Features

- Single power supply voltage of 2.6 to 3.3V
- Direct TTL compativility for all inputs and outputs.
- Deep power-down mode : Memory cell data invalid.
- Page operation mode

  Page read operation by 16 words.
- Logic compatible with SRAM R/W pin.
- Standby Current

  Standby 120 uA(Max)

  Deep power-down standby 10 uA(Max)
- Access Time

  /CE1 Access Time: 70ns

  /OE Access Time: 25ns

  Page Access Time: 20ns

■ Product Family

Product Family	Operating Temp	Vcc. Range	Speed(ns)	Standby(Max.)	Package Type
CS26LV32163	0~70°C	2.6~3.3	70	120 uA	Dice 48BGA-6*7mm 48BGA-6*8mm
	-40~85°C				

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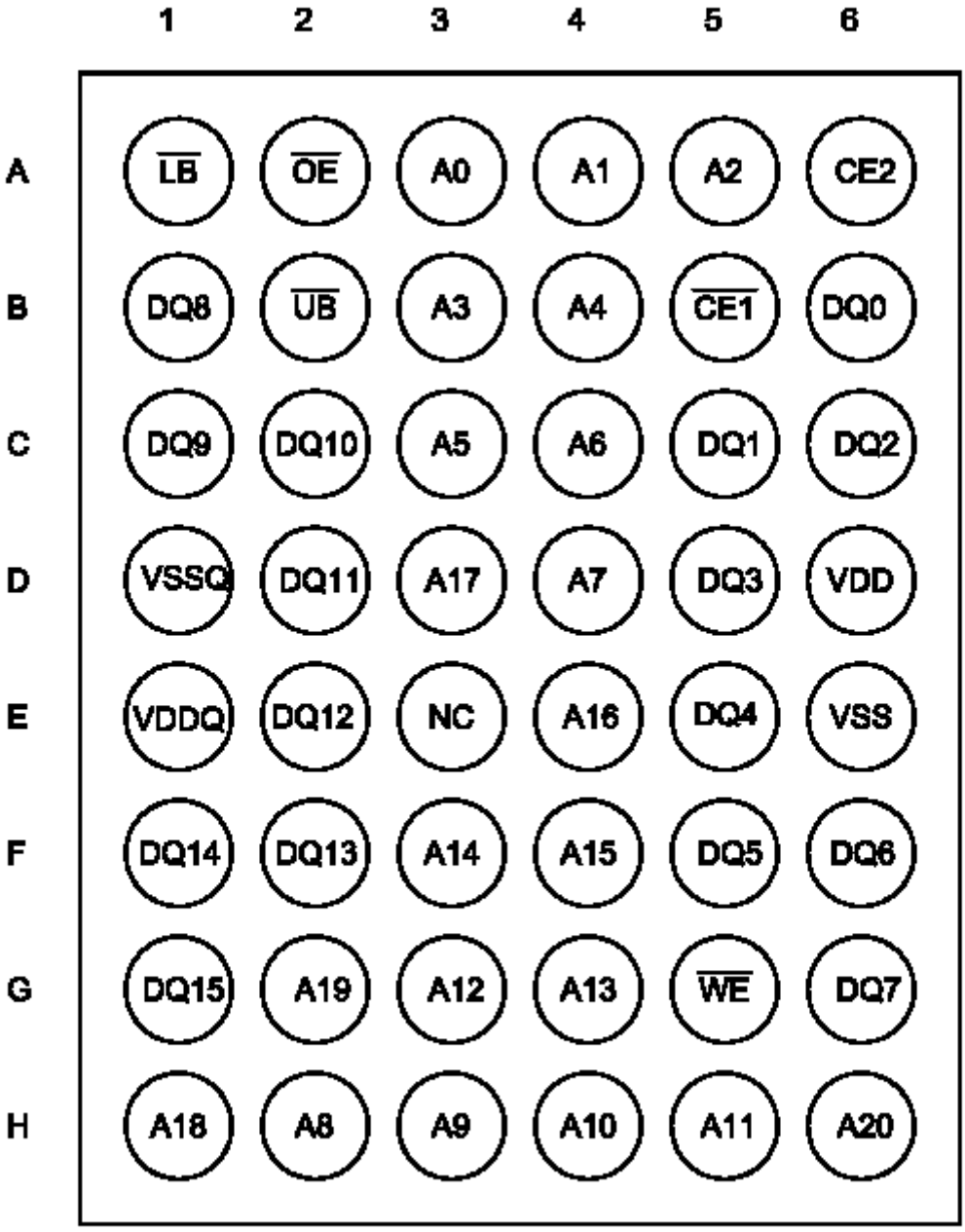
■ Pin Configuration

<48BGA>



48 BGA - Top View

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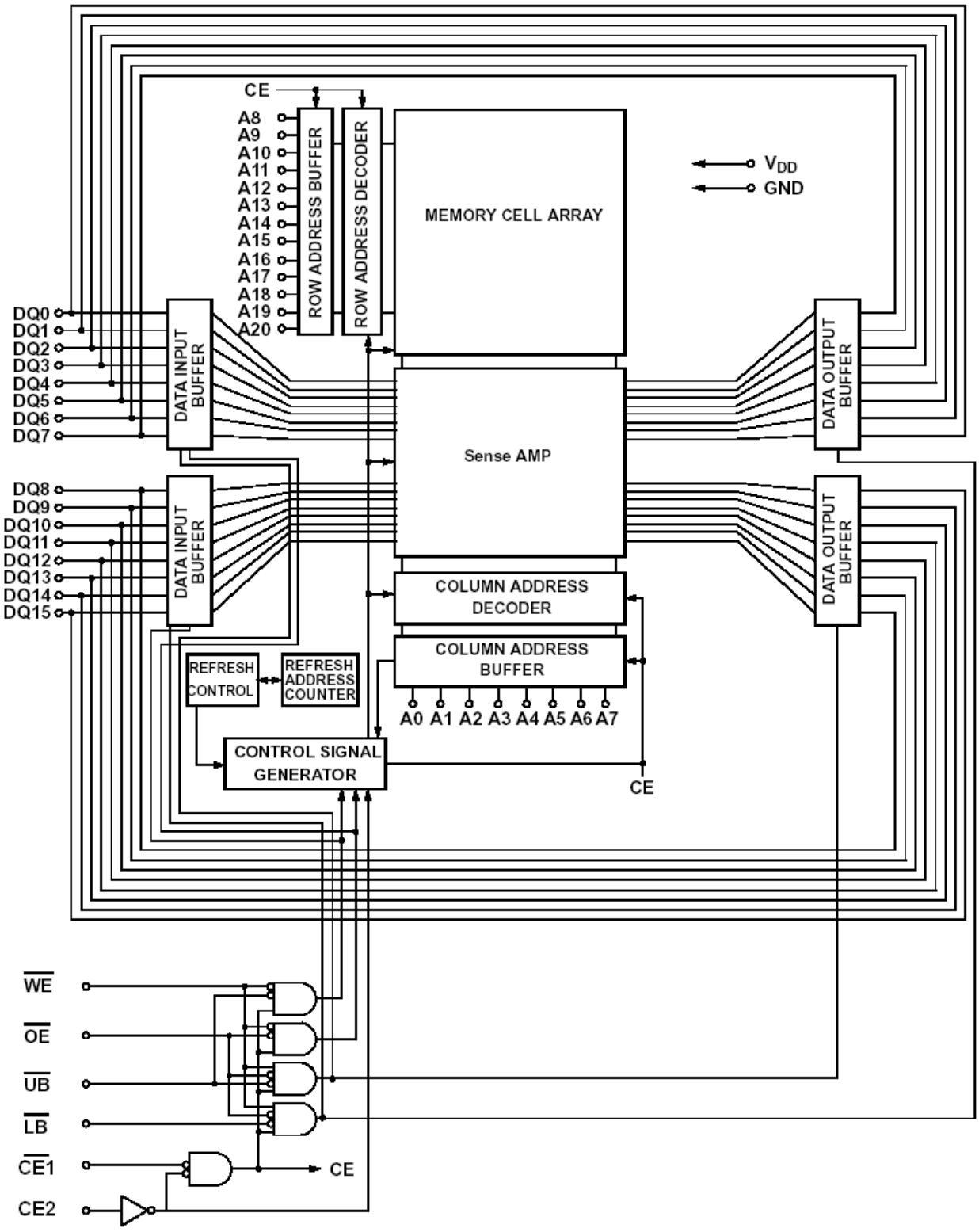
■ Functional Block Diagram



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■ Pin Descriptions

Name	Type	Function
A0~A20	input	Address input
A0~A3	input	Page Address input
/CE1	input	Chip Enable Input1, Low : Enable
CE2	input	Chip Enable Input2, High:Enable, Low:Enter Power Down mode
/WE	input	Write Enable input, Low :Enable
/OE	input	Output Enable input, Low :Enable
/LB	input	Lower byte write control
/UB	input	Upper byte write control
DQ0~DQ15	I/O	Data inputs/outputs
V_{DD}	Power	Device Power supply
V_{SS}	Power	VSS must be connected ground
V_{DDQ}	Power	I/O Power supply
V_{SSQ}	Power	VSSQ must be connected ground
NC		Not Connection

■ Truth Table

MODE	/CE1	CE2	/OE	/WE	/LB	/UB	DQ0~7	DQ8~15	V_{DD} Current
Deep power down	X	L	X	X	X	X	High Z	High Z	
Standby	H	H	X	X	X	X	High Z	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	L	H	H	H	X	X	High Z	High Z	I_{CC}
Read	L	H	L	H	L	L	D_{OUT}	D_{OUT}	I_{CC}
Upper Byte Read					L	H	D_{OUT}	High Z	I_{CC}
Lower Byte Read					H	L	High Z	D_{OUT}	I_{CC}
Write	L	H	X	L	L	L	D_{IN}	D_{IN}	I_{CC}
Upper Byte Write					L	H	D_{IN}	Invalid	I_{CC}
Lower Byte Write					H	L	Invalid	D_{IN}	I_{CC}

Note: X means don't care. (Must be low or high state)

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■ Absolute Maximum Ratings(1)

Symbol	Parameter	Rating	Unit
V_{IN}	Input Voltage	-1.0 to 3.6	V
V_{OUT}	Output Voltage	-1.0 to 3.6	V
V_{DD}	Device Power Supply Voltage	-1.0 to 3.6	V
T_{STG}	Storage Temperature	-55 to +150	^{O}C
T_A	Operating Temperature	-40 to +85	^{O}C
P_D	Power Dissipation	0.6	W

1. Stresses greater than those listed above “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ DC Electrical Characteristics (T_A = 0 to + 70^{o}C , V_{DD}= 3.0V)

Parameter Name	Parameter	Test Conduction	MIN	TYP(1)	MAX	Unit
V_{IL}	Input Low Voltage (2)		-0.3		0.6	V
V_{IH}	Input High Voltage (2)		2.4		V_{DD} + 0.3	V
I_{IL}	Input Leakage Current	V_{IN}=0 to V_{DD}	-1		1	uA
I_{OL}	Output Leakage Current	Output disable, V_{OUT}= 0V to V_{DD}	-1		1	uA
V_{OL}	Output Low Voltage	I_{OL} = 0.5mA, V_{DD}=V_{DD}min			0.6	V
V_{OH}	Output High Voltage	I_{OH} = -0.5mA	2.4			V
I_{CC1}	Operating Current	t_{RC}= Min, /CE1=V_{IL} , CE2=V_{IH} , I_{OUT}=0mA			25	mA
I_{CC2}	Page Access Operating current	t_{PC} = Min, /CE1=V_{IL}, CE2=V_{IH} , I_{OUT}=0mA, Page add. cycling.			15	mA
I_{CCSB1}	Standby Current -CMOS	/CE1≧V_{DD}-0.2V, CE2=V_{DD} -0.2V			120	uA
I_{CCSB2}	Deep Power-down Standby Current	CE2 = 0.2V			10	uA

1. Typical characteristics are at T_A = 25^{o}C.
2. V_{IH}(Max) V_{DD}+1.0V with 10ns pulse width, V_{IL}(Min)-1.0V with 10ns pulse width

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■ Capacitance (1) (TA = 25°C, f =1.0 MHz)

Symbol	Parameter	Conditions	MAX.	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT}=0V	10	pF

1. This parameter is sampled periodically and is not 100% tested

■ AC Test Conditions

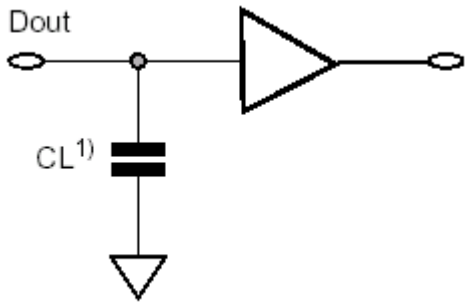
Test Conditions (Test Load and Test Input/Output Reference)

Input Pulse Level : 0.2V to V_{DDQ}-0.2V

Input Rise and Fall Time : 5ns

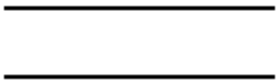
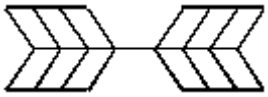
Input and Output reference Voltage : V_{DDQ} /2

Output Load (See right) : CL1) = 30pF



1. Including scope and Jig capacitance

■ Key To Switching Waveforms

Waveform	Inputs	Outputs
	Must be standby	Must be standby
	May change for H to L	Will be change from H to L
	May change for L to H	May change for L to H
	Don't care any change permitted	Change state unknown
	Does not apply	Center line is high impedance "OFF" state

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■ AC Characteristics <Read cycle & Write Cycle>

Parameter Name	Name	70		Unit
		Min	Max	
Read cycle time	t_{RC}	70	10,000	ns
Page mode cycle time	t_{MRC}	20	10,000	ns
Address access time	t_{ACC}	-	70	ns
Page Address Access Time	t_{AA}		20	ns
Chip enable access time (/CE1)	t_{CO}	-	70	ns
Output enable to output valid (/OE)	t_{OE}	-	25	ns
Byte enable access time	t_{BA}	-	25	ns
Output data hold time	t_{OH}	5	-	ns
Page mode output data hold time	t_{AOH}	5	-	ns
Chip enable to output in low Z (/CE1)	t_{COE}	10	-	ns
Output enable to output in low Z (/OE)	t_{OEE}	0	-	ns
Byte enable to output in low Z	t_{BE}	0	-	ns
Chip disable to output in High Z (/CE1)	t_{OD}	-	20	ns
Output disable to output in High Z (OE)	t_{ODO}	-	20	ns
Byte disable to output in High Z	t_{BD}	-	20	ns
Write cycle time	t_{WC}	70	10,000	ns
Byte enable to end of write	t_{BW}	60	-	ns
Address valid to end of write	t_{AW}	60	-	ns
Chip select to end of write	t_{CW}	65	-	ns
Data set up time	t_{DS}	30	-	ns
Data hold time	t_{DH}	0	-	ns
Write pulse width	t_{WP}	50	-	ns
Address set up time	t_{AS}	0	-	ns
Write recovery time(/WE)	t_{WR}	0	-	ns
/WE high to output low Z	t_{OEW}	0	-	ns
/WE low to output high Z	t_{ODW}	-	20	ns
Chip enable high pulse width	t_{CEH}	10		ns
Write enable high pulse width	t_{WEH}	6	-	ns
CE2 set –up time	t_{CS}	0	-	ns
CE2 hold time	t_{CH}	300	-	ns
CE2 pulse width	t_{DPD}	10	-	ns
CE2 hold from /CE1	t_{CHC}	0	-	ns
CE2 hold from power on	t_{CHP}	30	-	ns

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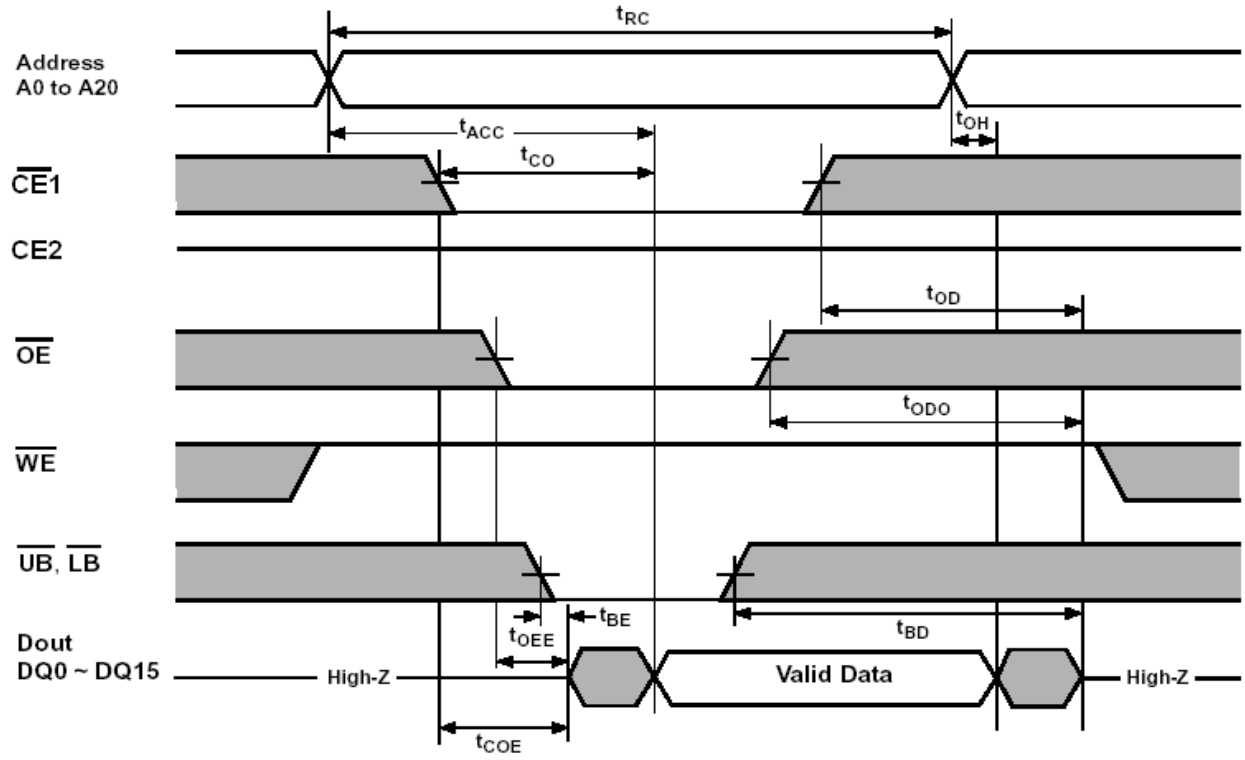
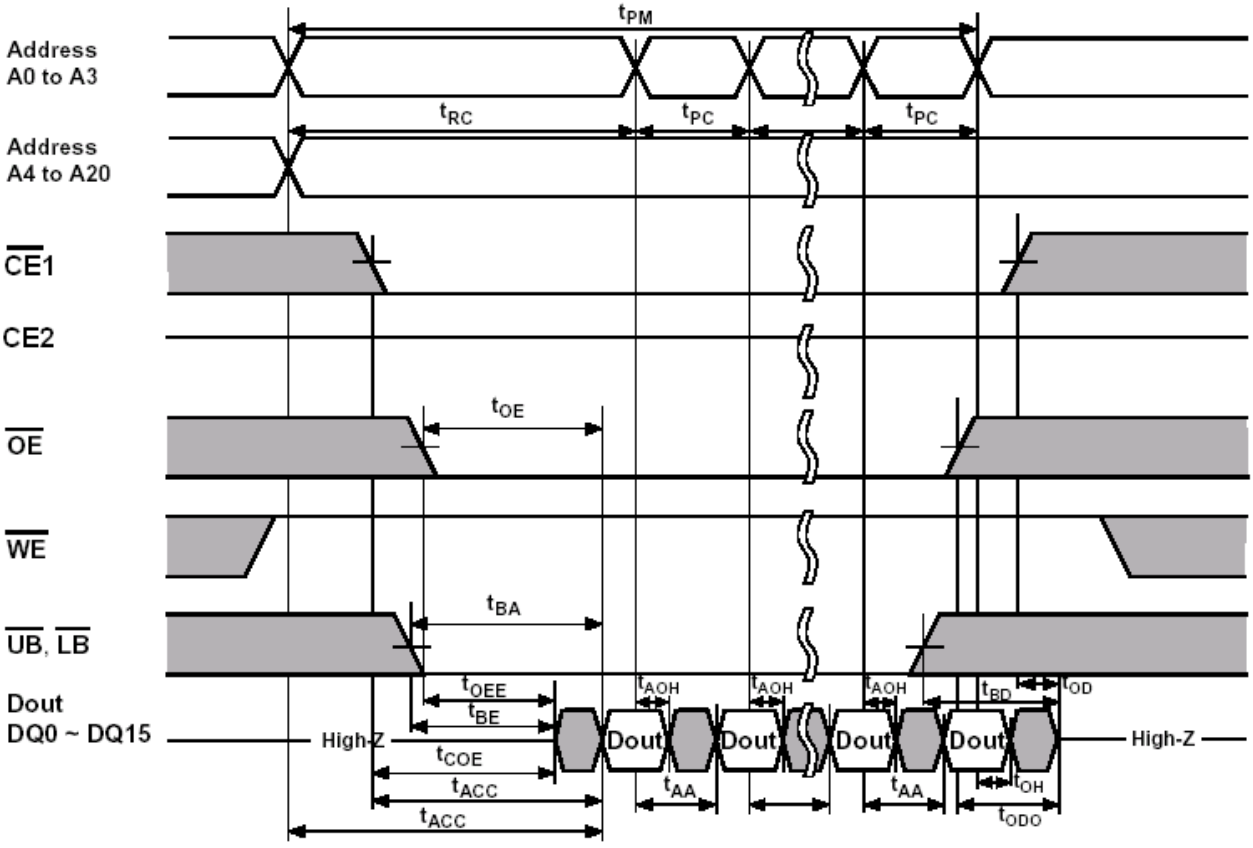
TIMING DIAGRAMS <READ CYCLE>



PAGE READ CYCLE (16 words access)



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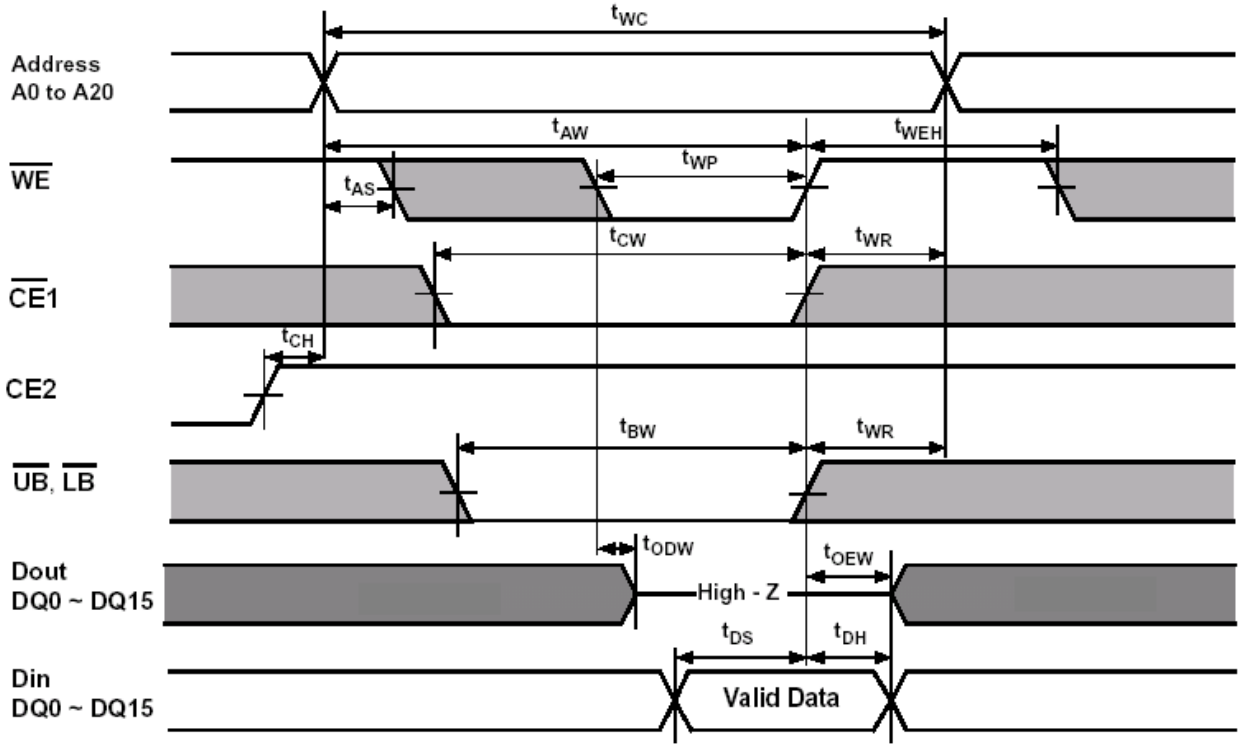
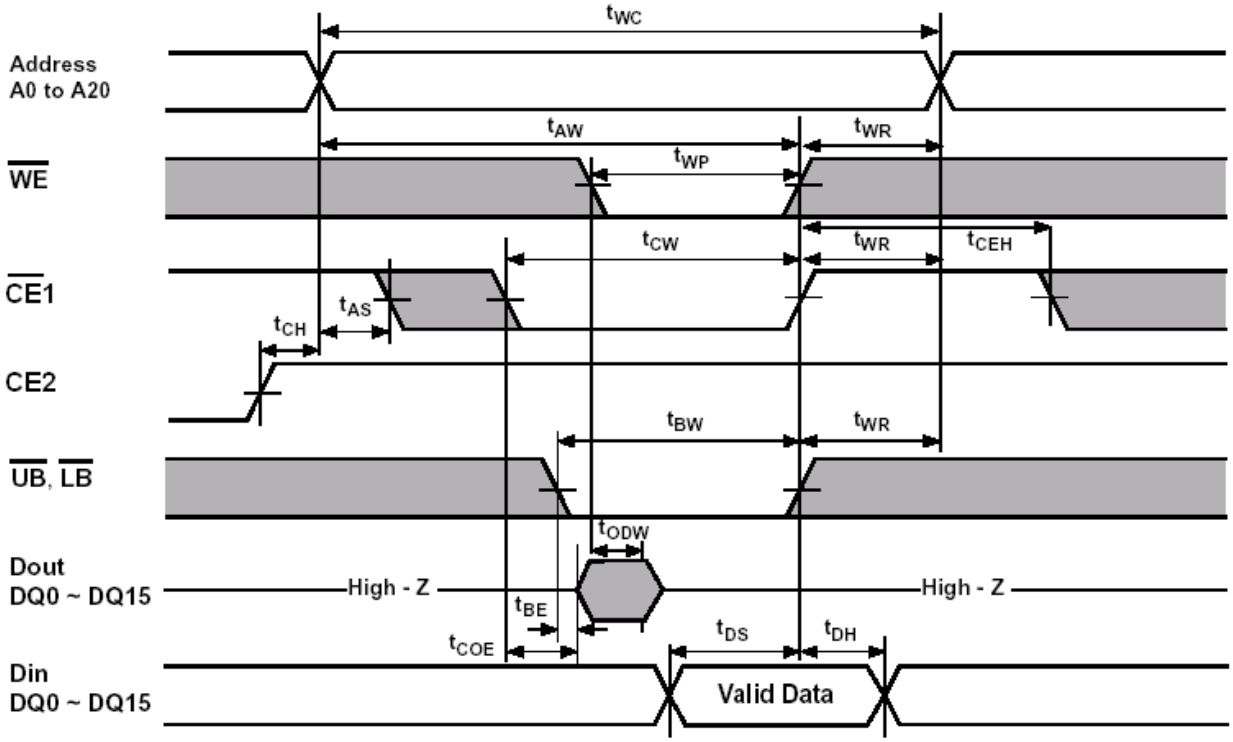
WRITE CYCLE (1) (/WE controlled)



WRITE CYCLE (2) (/CE1 controlled)



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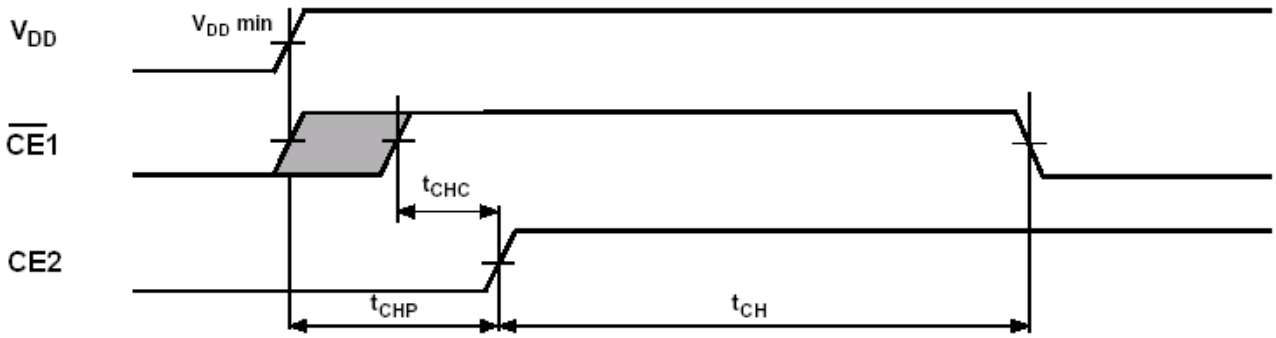
NOTES

1. AC measurement are assumed tR, tF = 5ns.
1. Parameters tOD, tODO, tBD and tODW define the time at which the output goes the open condition and are not output voltage reference levels.
2. Data cannot be retained at deep power-down stand-by mode.
3. If /OE is high during the write cycle, the outputs will remain at high impedence.
4. During the output state of DQ signals, input signals of reverse polarity must not be applied.
5. If /CE1 or /LB&/UB goes LOW coincident with or after /WE goes LOW, the outputs will remain at high impedence.
6. If /CE1 or /LB&/UB goes HIGH coincident with or before /WE goes HIGH, the outputs will remain at high impedence.

■ DEEP POWER-DOWN TIMING

■ POWER_ON TIMING



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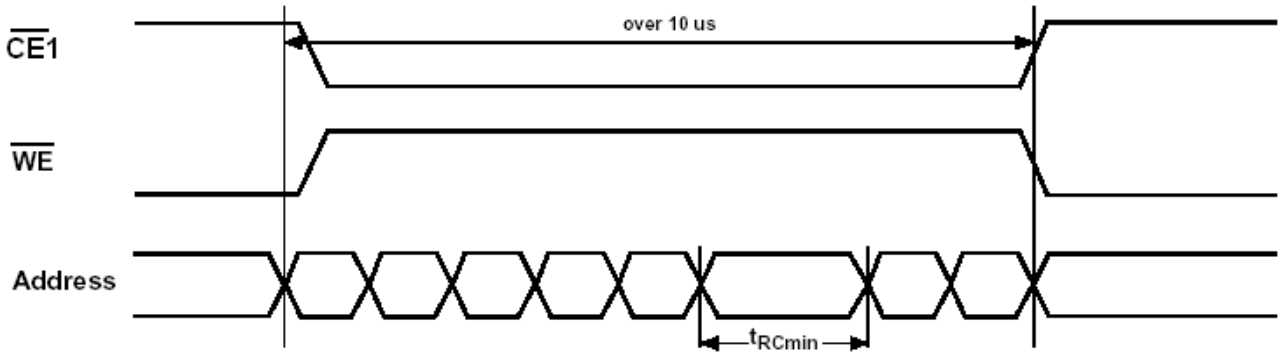
■ PROVISIONS OF ADDRESS SKEW

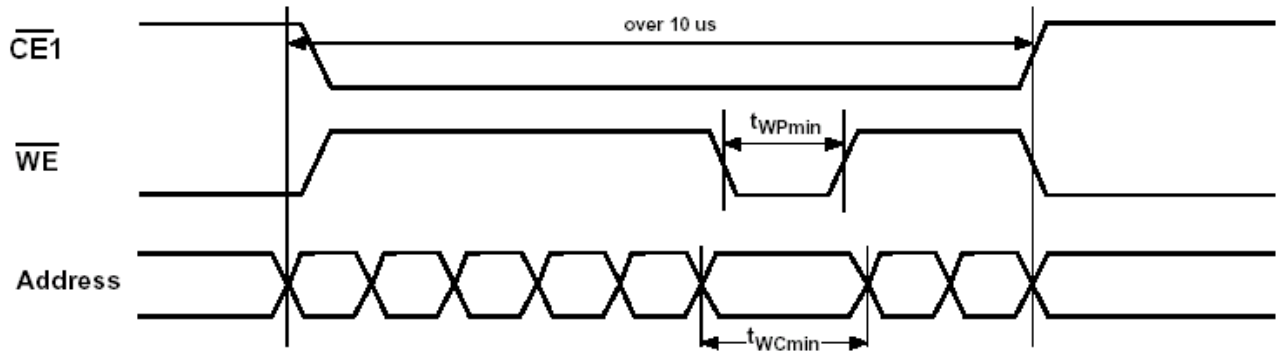
Read

In case, multiple invalid address cycles shorter than tRC_min sustain over 10us in a active status, as least one valid address cycle over tRC_min must be needed during 10us.



Write

In case, multiple invalid address cycles shorter than tWC_min sustain over 10us in a active status, as least one valid address cycle over tRC_min with tWP_min must be needed during 10us.



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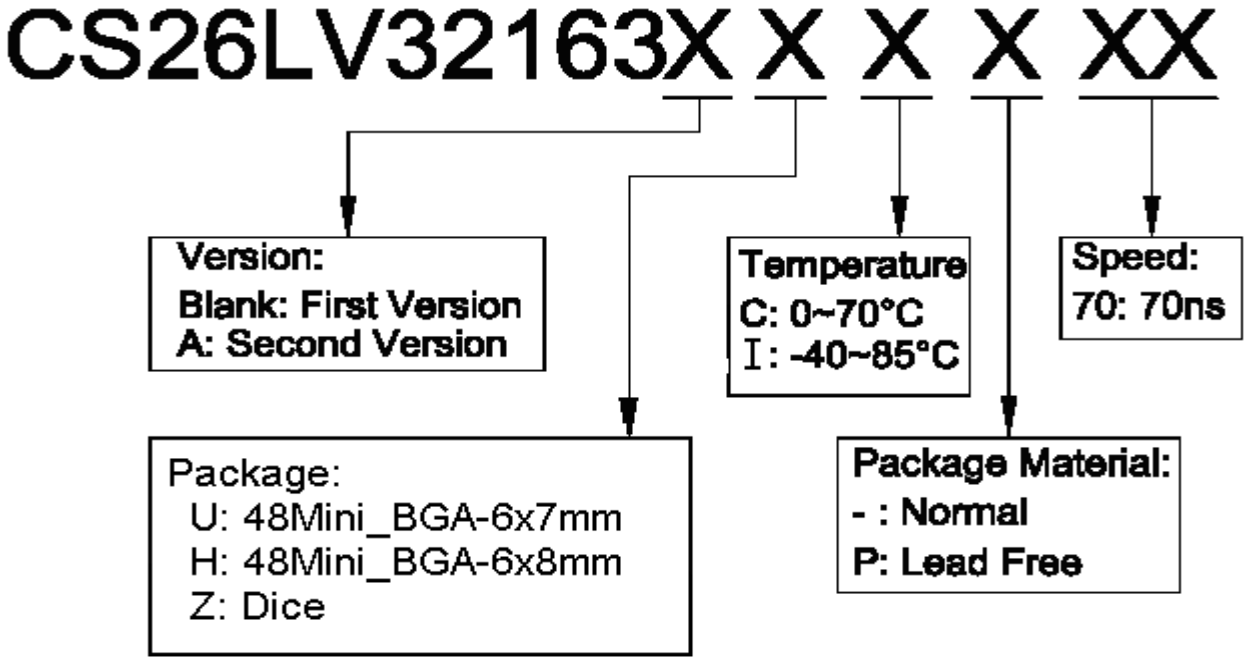
■ Order information



Note: Package material code “P” meets RoHS

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