



**Revision History**

<b><u>Rev. No.</u></b>	<b><u>History</u></b>	<b><u>Issue Date</u></b>	<b><u>Remark</u></b>
1.0	New issue (65nm process)	May. 27, 2015	



# Low Power Pseudo SRAM

1M word x 16 bit

**CS26LV16163C**

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### Product Description

The CS26LV16163C is a high performance, high speed, low power pseudo SRAM organized as 1M words by 16 bits and operates from a wide range of 2.6 to 3.6V supply voltage. Advanced DRAM technology and circuit techniques provide both high speed and maximum access time of 70ns in 3.3V operation. Easy memory expansion is provided by an active LOW chip enable (/CE) and active LOW output enable (/OE) and three-state output drivers.

The CS26LV16163C has the page access operation, page size is 16 words, and has a deep power down feature, reducing the power consumption significantly when chip is deselected. The CS26LV16163C is available 48-ball BGA package.

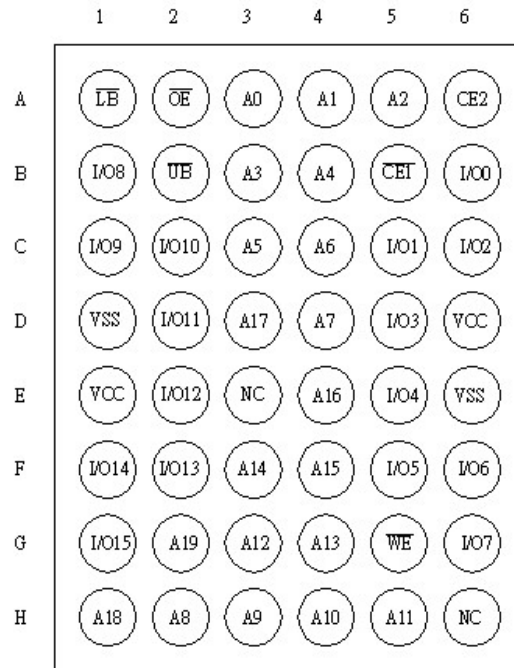
### Features

- Single power supply voltage of 2.6 to 3.6V
- Direct TTL compatibility for all inputs and outputs.
- Deep power-down mode: Memory cell data invalid.
- Page operation mode
- Page read operation by 16 words.
- Logic compatible with SRAM R/W pin.
- Standby Current
  - Standby 120 uA(Max)
  - Deep power-down standby 20 uA (Max.)
- Access Time
  - /CE1 Access Time: 70ns
  - /OE Access Time: 25ns
  - Page Access Time: 25ns

### Product Family

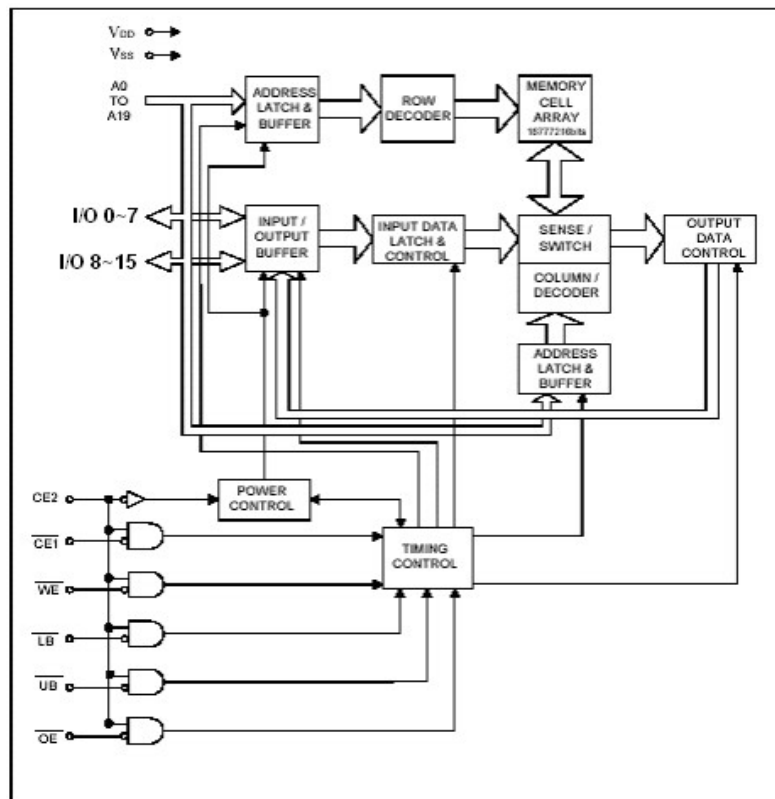
Part No.	Operating Temp	V <sub>CC</sub> Range	Speed	Standby (ISB, Max.)	Package Type
CS26LV16163C	0~70 °C	2.6~3.6V	70ns	120uA	Dice 48 BGA-6x8mm
	-40~85 °C			120uA	

### Pin Configuration



48 Ball CSP - Top View

### Functional Block Diagram





### Pin Description

Name	Type	Function
A0~A19	input	Address inputs
A0~A3	input	Page Address input
/CE1	input	Chip enables input 1. Low: enable
CE2	input	Chip enable input 2. High: enable, Low: enter power down mode
/WE	input	Write enable input
/OE	input	Output enable input
/LB	input	Lower byte data input/output control pin
/UB	input	Upper byte data input/output control pin
I/O0~I/O15	I/O	Data input/output pins
V <sub>cc</sub>	Power	Power Supply
V <sub>ss</sub>	Power	Ground
NC		No connection

### Truth Table

MODE	/CE1	CE2	/OE	/WE	/LB	/UB	DQ0~7	DQ8~15	V <sub>DD</sub> Current
Deep power down	X	L	X	X	X	X	High Z	High Z	
Standby	H	H	X	X	X	X	High Z	High Z	I <sub>CCSB</sub> , I <sub>CCSB1</sub>
Output Disabled	L	H	H	H	X	X	High Z	High Z	I <sub>CC</sub>
Read					L	L	D <sub>OUT</sub>	D <sub>OUT</sub>	I <sub>CC</sub>
Upper Byte Read	L	H	L	H	L	H	D <sub>OUT</sub>	High Z	I <sub>CC</sub>
Lower Byte Read					H	L	High Z	D <sub>OUT</sub>	I <sub>CC</sub>
Write					L	L	D <sub>IN</sub>	D <sub>IN</sub>	I <sub>CC</sub>
Upper Byte Write	L	H	X	L	L	H	D <sub>IN</sub>	Invalid	I <sub>CC</sub>
Lower Byte Write					H	L	Invalid	D <sub>IN</sub>	I <sub>CC</sub>

Note: X means don't care. (Must be low or high state)

### Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V <sub>CC</sub>	Voltage of V <sub>CC</sub> supply relative to V <sub>SS</sub>	-0.2 to V <sub>CC</sub> +0.3	V
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage at any pin relative to V <sub>SS</sub>	-0.2 to V <sub>CC</sub> +0.3	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	W

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### DC Electrical Characteristics (TA = 0 to +70°C, V<sub>CC</sub> = 2.7V to 3.6V)

Parameter Name	Parameter	Test Conduction	MIN	TYP <sup>(1)</sup>	MAX	Unit
V <sub>IL</sub>	Input Low Voltage <sup>(2)</sup>		-0.2		0.2*V <sub>CC</sub>	V
V <sub>IH</sub>	Input High Voltage <sup>(3)</sup>		0.8*V <sub>CC</sub>		V <sub>CC</sub> +0.2	V
I <sub>IL</sub>	Input Leakage Current	V <sub>CC</sub> =MAX, V <sub>IN</sub> =0 to V <sub>CC</sub>	-1		1	uA
I <sub>OL</sub>	Output Leakage Current	V <sub>CC</sub> =MAX, /CE1=V <sub>IN</sub> , or /OE=V <sub>IN</sub> , V <sub>IO</sub> =0V to V <sub>CC</sub>	-1		1	uA
V <sub>OL</sub>	Output Low Voltage	V <sub>CC</sub> =MAX, I <sub>OL</sub> = 2mA			0.2*V <sub>CC</sub>	V
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> =MIN, I <sub>OH</sub> = -1mA	0.8*V <sub>CC</sub>			V
I <sub>CC1</sub>	Operating Power Supply Current	Cycle time=1us, I <sub>IO</sub> =0mA, 100% duty, /CE1 ≤ 0.2V, CE2 ≥ V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≤ 0.2V or V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V			5	mA
I <sub>CC2</sub>		Cycle time=Min, I <sub>IO</sub> =0mA, 100% duty, /CE1=V <sub>IL</sub> , CE2=V <sub>IH</sub> , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub>			25	mA
I <sub>CCSB1</sub>	Standby Current - CMOS	/CE1 & CE2 ≥ V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤ 0.2V			120	uA
I <sub>CCSB2</sub>	Deep Power-down Standby Current	CE2 < 0.2V, Other inputs = 0 ~ VDDQ (Max. condition : VDD=3.6V @ 85oC)			20	uA

1. Typical characteristics are at TA = 25°C.

2. Undershoot: -1.0V in case of pulse width  $\leq 20ns$
3. Overshoot:  $V_{CC} + 1.0V$  in case of pulse width  $\leq 20ns$
4. Undershoot and overshoot are sampled, not 100% tested

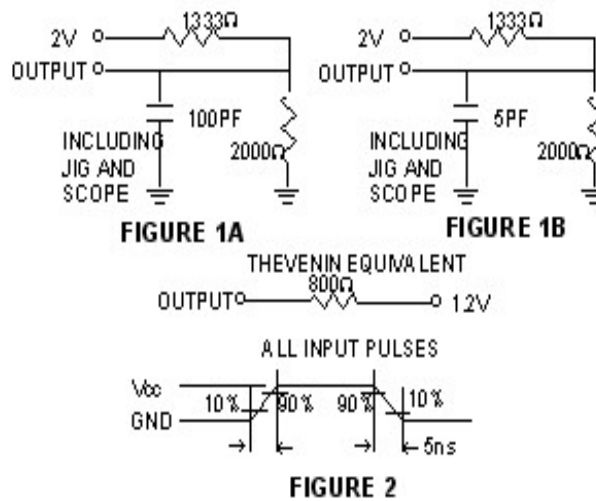
### Capacitance <sup>(1)</sup> (TA = 25°C, f = 1.0 MHz)

Symbol	Parameter	Conditions	MAX.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =0V	8	pF
C <sub>DQ</sub>	Input /Output Capacitance	V <sub>I/O</sub> =0V	10	pF

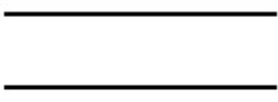



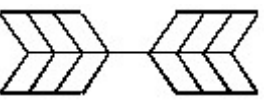
*This parameter is guaranteed and not tested.*

### AC Test Conditions

Input Pulse Levels	V <sub>CC</sub> /0V
Input Rise and Fall Times	5ns
Input and Output	
Timing Reference Level	0.5V <sub>CC</sub>



### Key to Switching Waveforms

Waveform	Inputs	Outputs
	Must be standby	Must be standby
	May change for H to L	Will be change from H to L
	May change for L to H	May change for L to H
	Don't care any change permitted	Change state unknown
	Does not apply	Center line is high impedance "OFF" state

### AC Characteristics

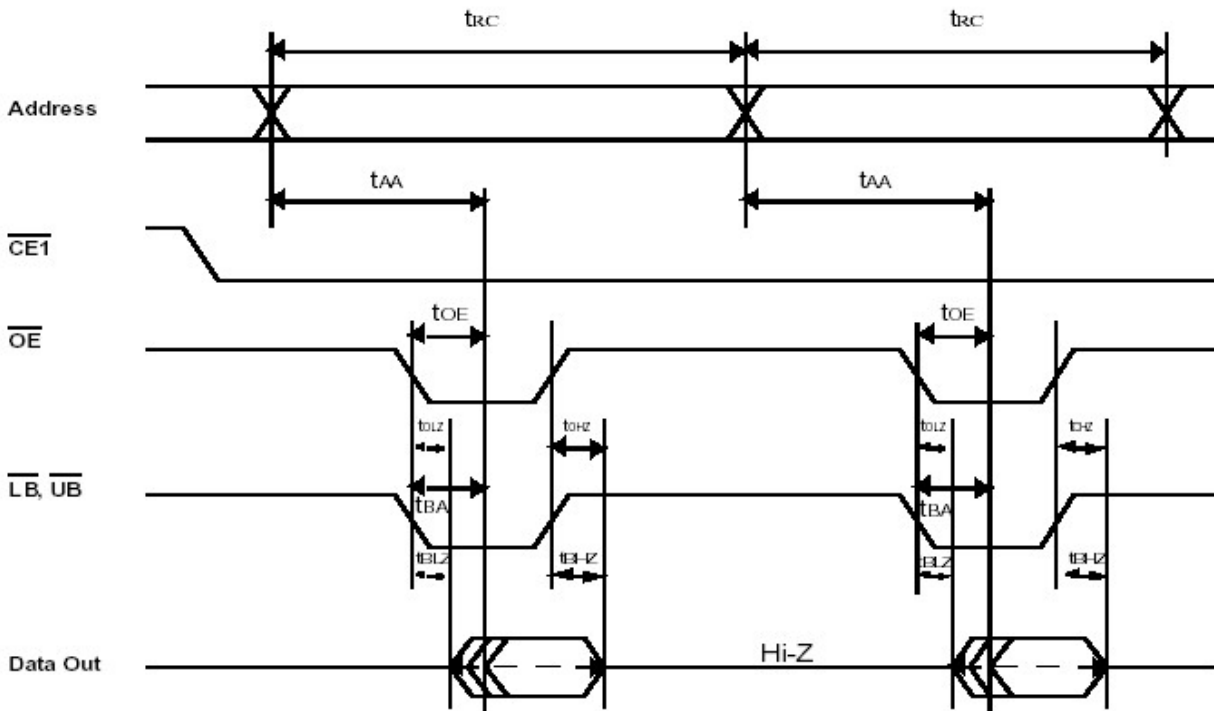
#### Read cycle

Parameter Name	Name	70		Unit
		Min	Max	
Read cycle time	t <sub>RC</sub>	70	10k	ns
Address access time	t <sub>AA</sub>	-	70	ns
Chip enable access time (/CE1)	t <sub>ACS</sub>	-	70	ns
Output enable to output valid (/OE)	t <sub>OE</sub>	-	25	ns
Byte enable access time	t <sub>BA</sub>	-	25	ns
Output hold from address change	t <sub>OH</sub>	5	-	ns
Chip enable to output in low Z (/CE1)	t <sub>LZ</sub> *	10	-	ns
Output enable to output in low Z (/OE)	t <sub>OLZ</sub> *	0	-	ns
Byte enable to output in low Z	t <sub>BLZ</sub> *	0	-	ns
Chip disable to output in High Z (/CE1)	t <sub>HZ</sub> *	0	20	ns
Output disable to output in High Z (OE)	t <sub>OHZ</sub> *	0	20	ns
Byte disable to output in High Z	t <sub>BHZ</sub> *	0	20	ns

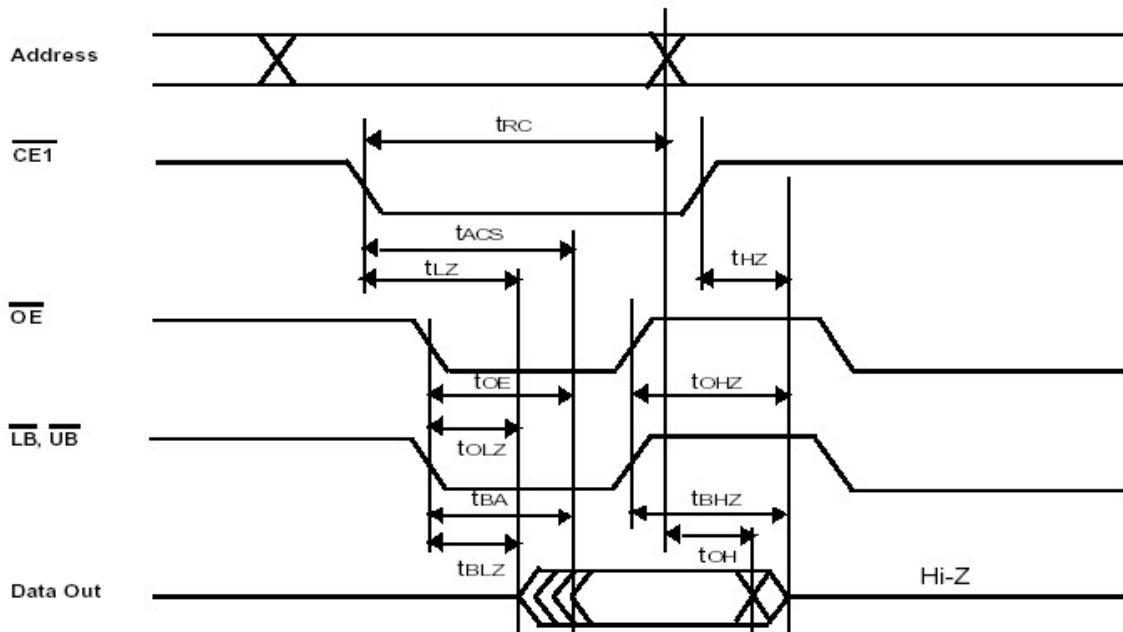
\*These parameters are sampled and are not 100% tested



### Read Cycle 1: /CE1 = VIL, /WE = VIH



### Read Cycle 2: /WE = VIH

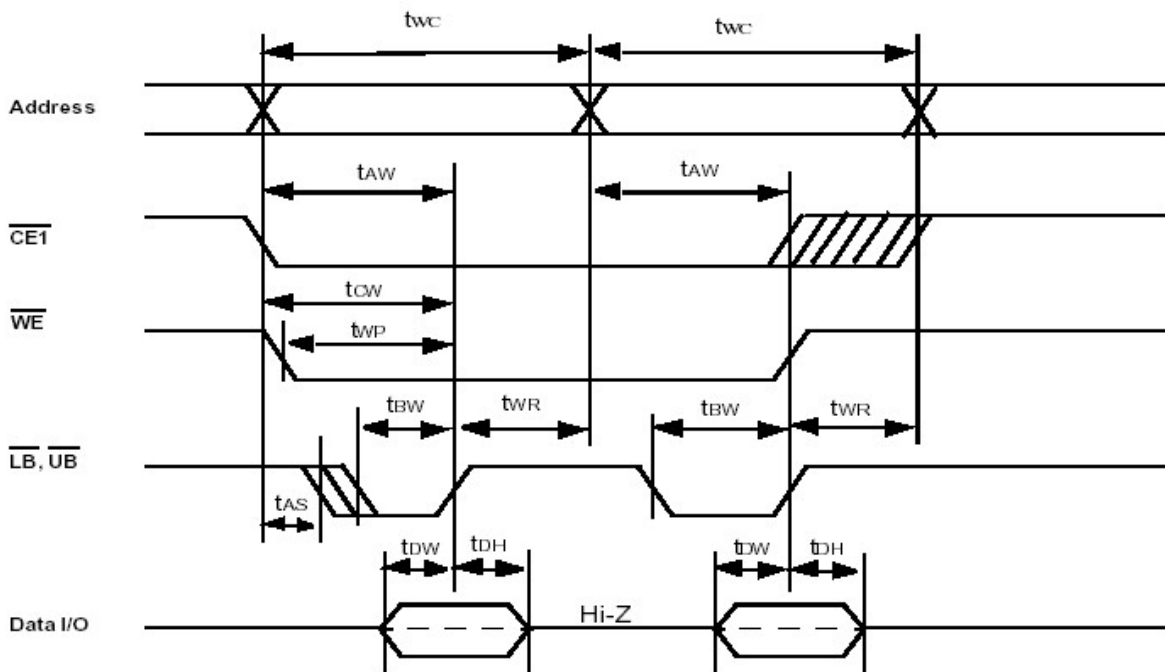


### Write Cycle

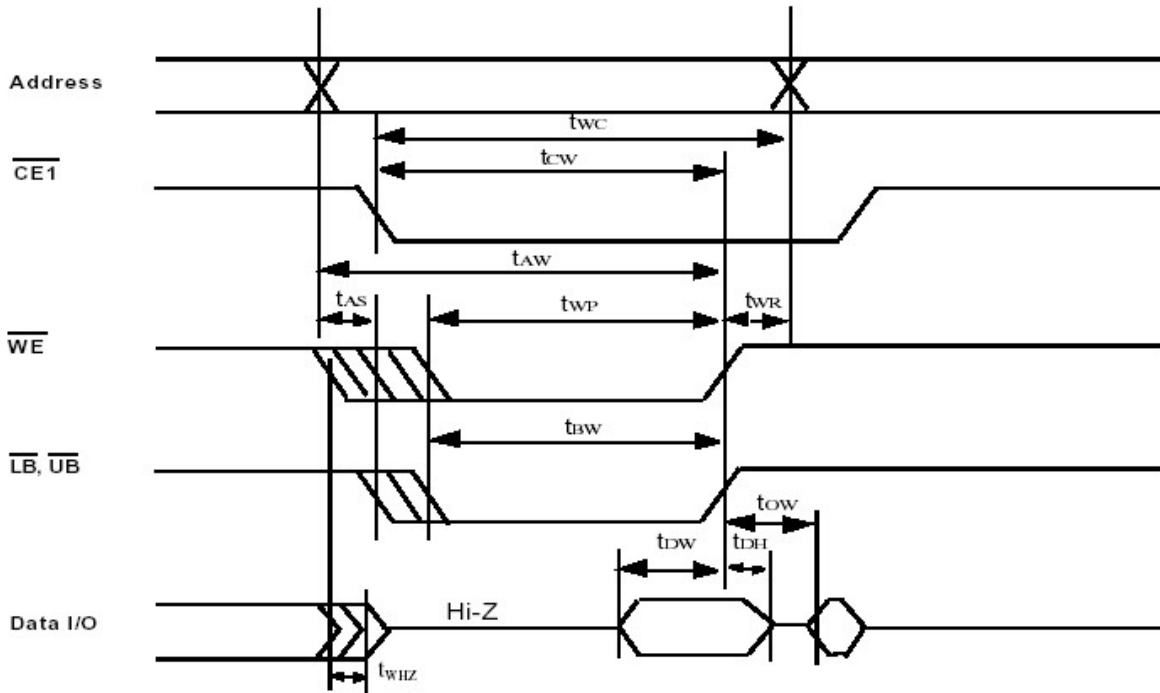
Parameter Name	Name	70		Unit
		Min	Max	
Write cycle time	$t_{WC}$	70	10k	ns
Byte enable to end of write	$t_{BW}$	60	-	ns
Address valid to end of write	$t_{AW}$	60	-	ns
Chip select to end of write	$t_{CW}$	60	-	ns
Data set up time	$t_{DW}$	20	-	ns
Data hold time	$t_{DH}$	0	-	ns
Write pulse width	$t_{WP}$	50	-	ns
Address set up time	$t_{AS}$	0	-	ns
Write recovery time(/WE)	$t_{WR}$	0	-	ns
/WE high to output low Z	$t_{OW}^*$	5	-	ns
/CE1 low to output low Z	$t_{LZ}^*$	-5	-	ns
/OE high to output high Z	$t_{OHZ}^*$	-	15	ns
Write to output high Z	$t_{WHZ}^*$	-	20	ns

\*These parameters are sampled and are not 100% tested

### Write Cycle 1: /LB & /UB control



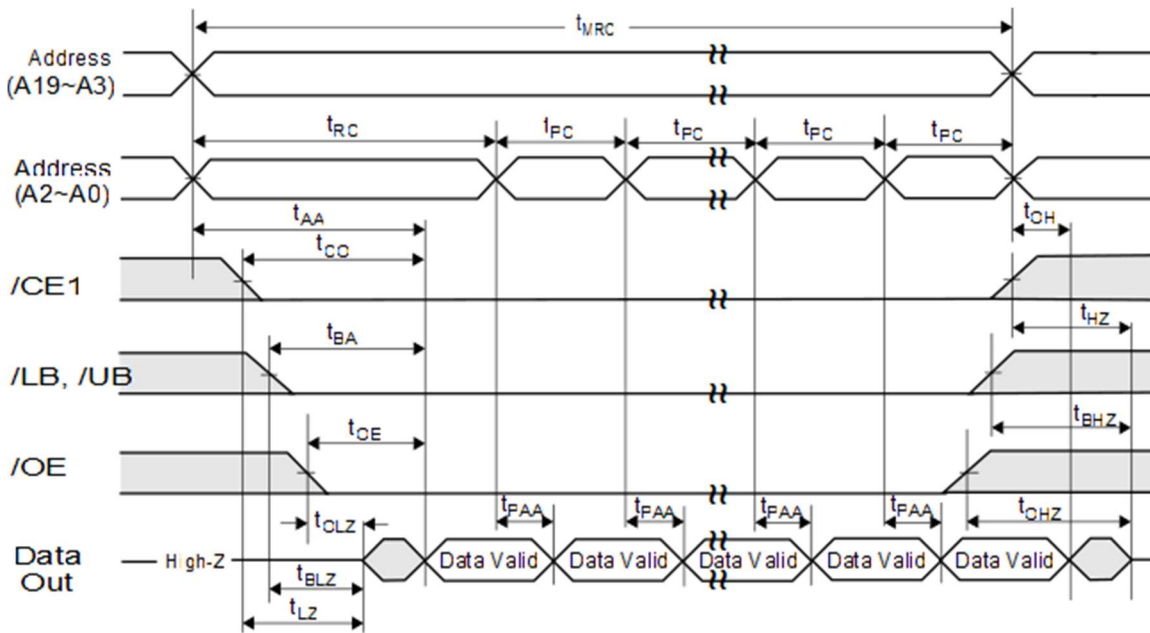
### Write Cycle 2: /WE control



### Page Cycle

Parameter Name	Name	Min.	Max.	Unit
Max. cycle time	$t_{MRC}$	-	10k	ns
Page mode cycle time	$t_{PC}$	25	-	ns
Page mode address access time	$t_{PAA}$		25	ns

### Page read cycle (1) (CE2=/we=V<sub>IH</sub>, 8 Words access)

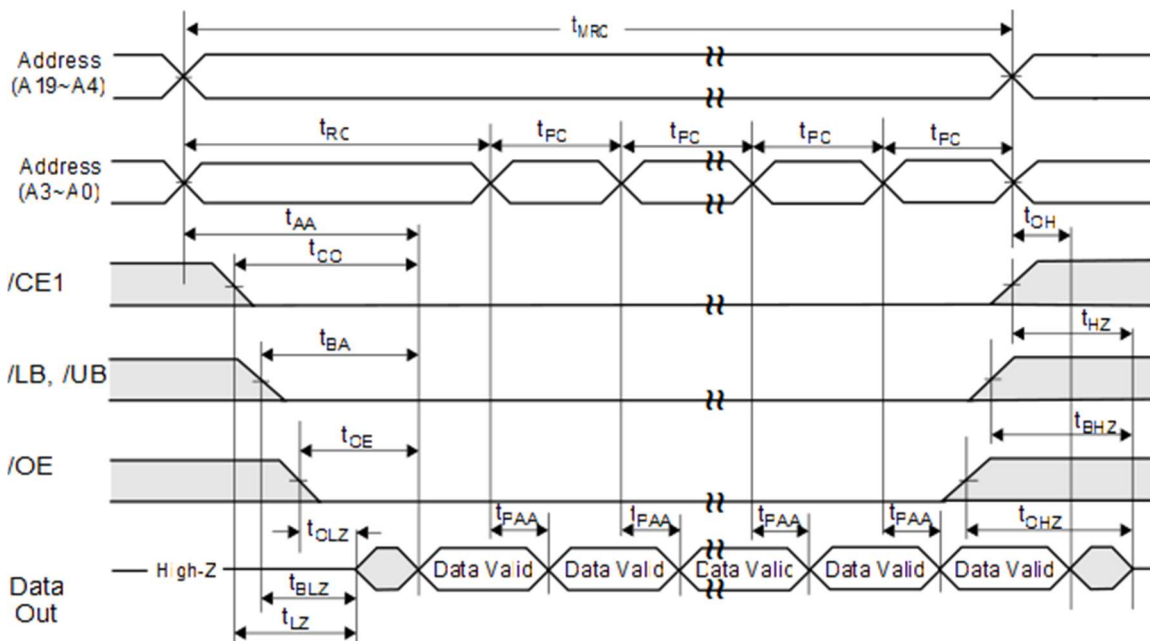


\*(read cycle)

1.  $t_{HZ}$ ,  $t_{BHZ}$ ,  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

2. Do not access device with cycle timing shorter than  $t_{RC}$  for continuous periods >10 $\mu$ s.

### Page read cycle (2) (CE2=/we=V<sub>IH</sub>, 16 Words access)



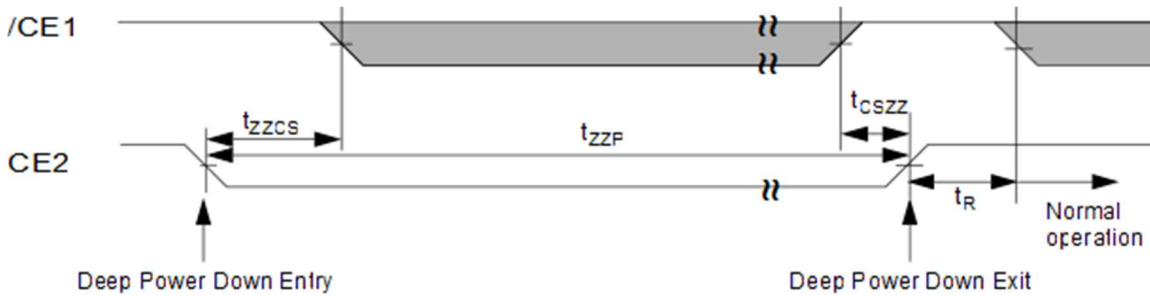
\*(read cycle)

1.  $t_{HZ}$ ,  $t_{BHZ}$ ,  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

2. Do not access device with cycle timing shorter than  $t_{RC}$  for continuous periods >10 $\mu$ s.

## Low Power Modes

### Deep power down mode entry/exit

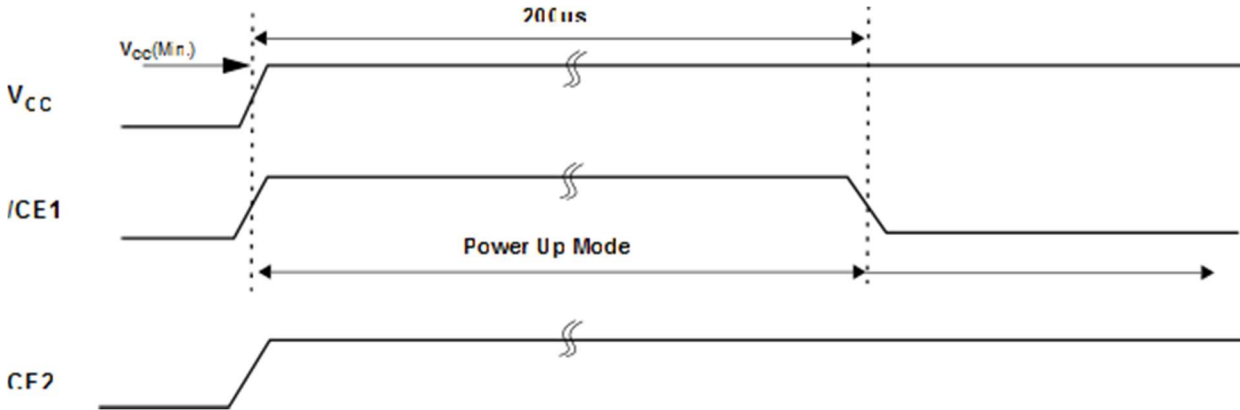


\*(Deep power down)

During deep power down mode, all refresh related activity is disabling.

Parameter Name	Name	Min.	Max.	Unit
$t_{zzcs}$	CE2 low to /CE1 low	0	-	ns
$t_{cszz}$	/CE1 high to CE2 high	0	-	ns
$t_r$	Operation recovery time	200	-	ns
$t_{zzp}$	CE2 pulse width	20	-	ns

### Timing waveform power up



\* After  $V_{CC}$  reaches  $V_{CC} (Min.)$ , wait 200us with  $/CE1$  high, then you get into the normal operation.

### Order Information

# CS26LV16163C X X X X

Package:  
 H: 48LMini\_BGA-6x8mm  
 Z: Dice

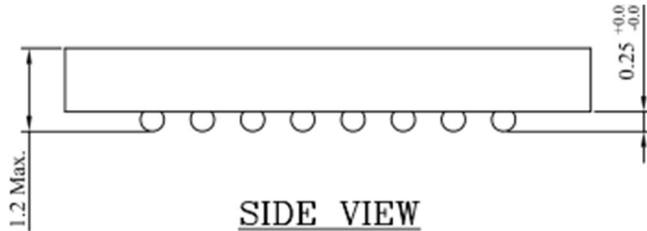
Temperature:  
 C: 0~70°C  
 I: -40~80°C

Speed:  
 70: 70ns

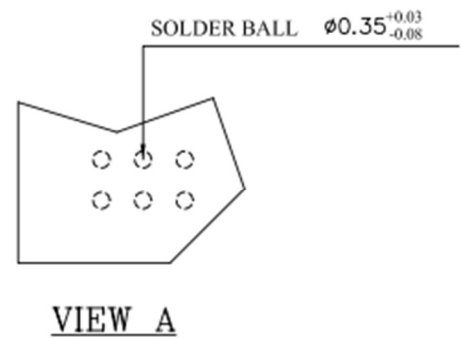
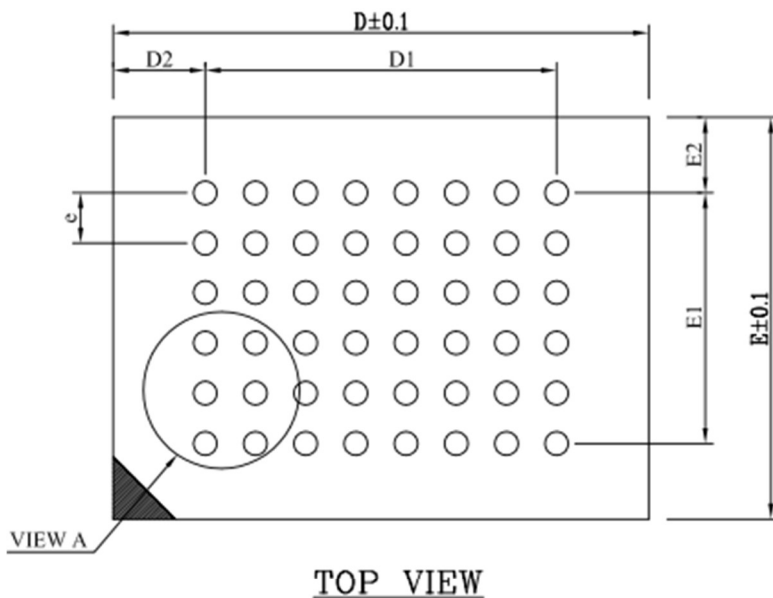
Package Material:  
 - : Normal  
 P: Lead Free

### Package Outline

48 ball Mini BGA-6x8mm



BALL PITCH $c = 0.75$						
D	E	N	D1	E1	D2	E2
8.0	6.0	48	5.25	3.75	1.375	1.125



**NOTES:**

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3. SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.
4. TOLERANCES:  
 LINEAR : X.X = ±0.1  
           X.XX = ± 0.05  
           X.XXX = ± 0.025