



L50II0 Schematics Rev:B

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25. CRT CONN WITH PR8800
26. +5V&+3V(MAX8734A)
27. +CPU CORE(MAX8771)
28. +1.5V+1.8V(OZ813) & +2.5V(RT9173B)
29. +1.05V(OZ818) & +1.2V(RT9173B) & +0.9V(RT9173B)
30. +1.0V_VGA & +1.8V_VGA(OZ813)
31. POWER ON SWITCH FUNC.
32. Charger func.(TL594) & DC IN CON & BATTERY CONN
33. Every Ver. Histor

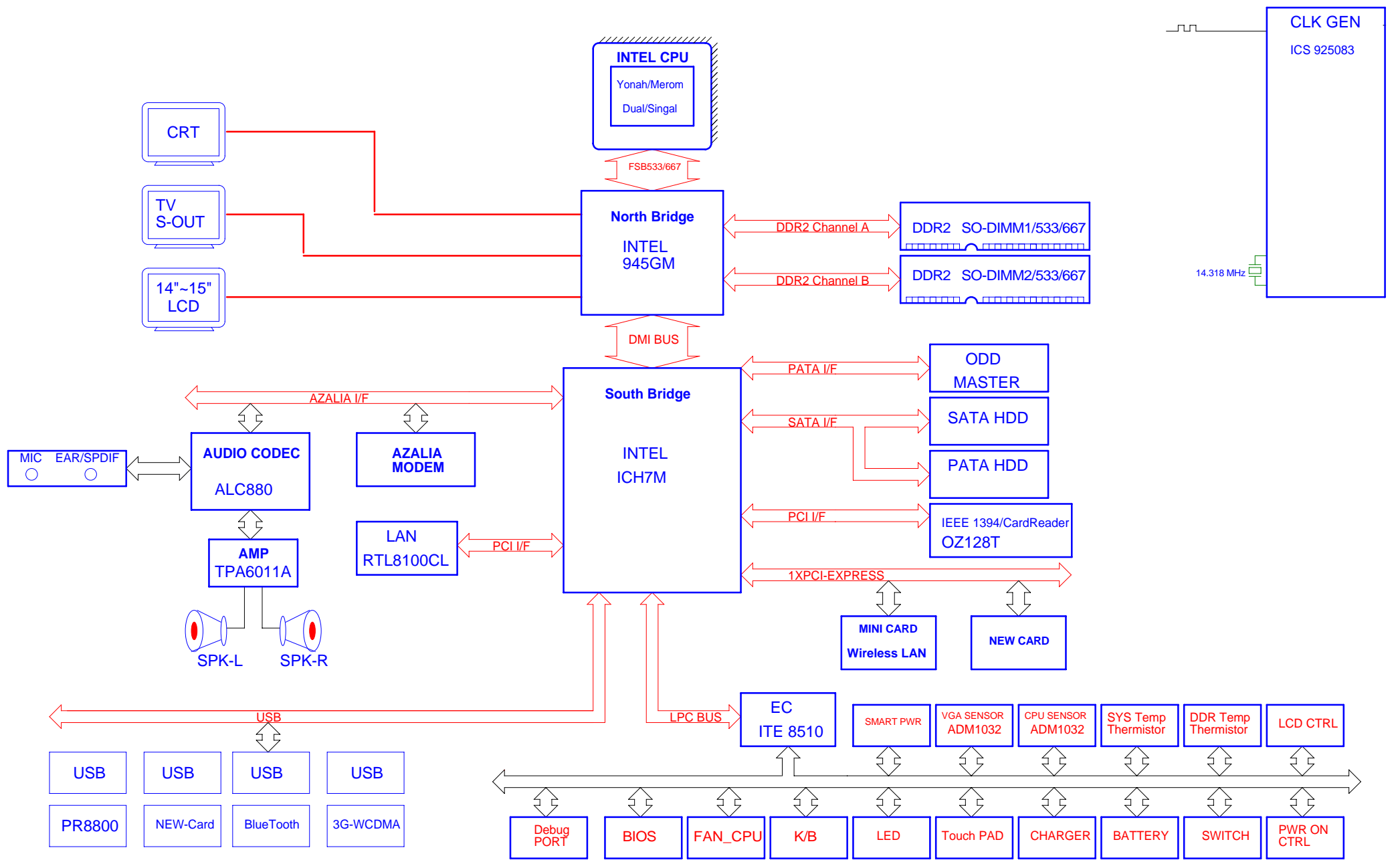
37GL50200-B0 PCB MAIN BD FOR L50II0 REV:B
82GL50200-B0 M/B ASSY FOR L50II0

L50II0 REV:A P/N LIST

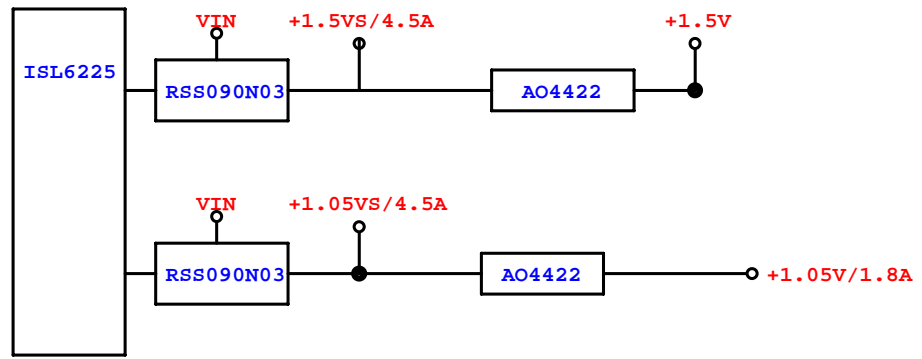
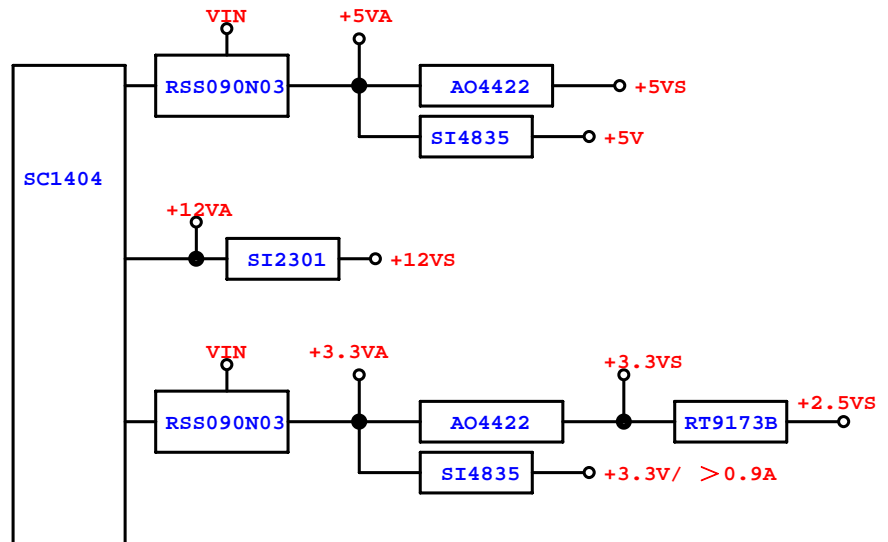
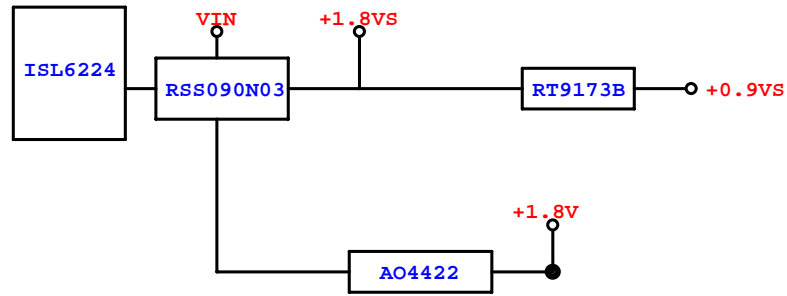
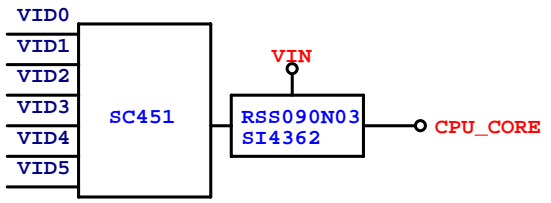
	PCB P/N	PCB ASSY P/N

Name of Part		Cover Page	
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3255 UNIWill COMPUTER CORP.			

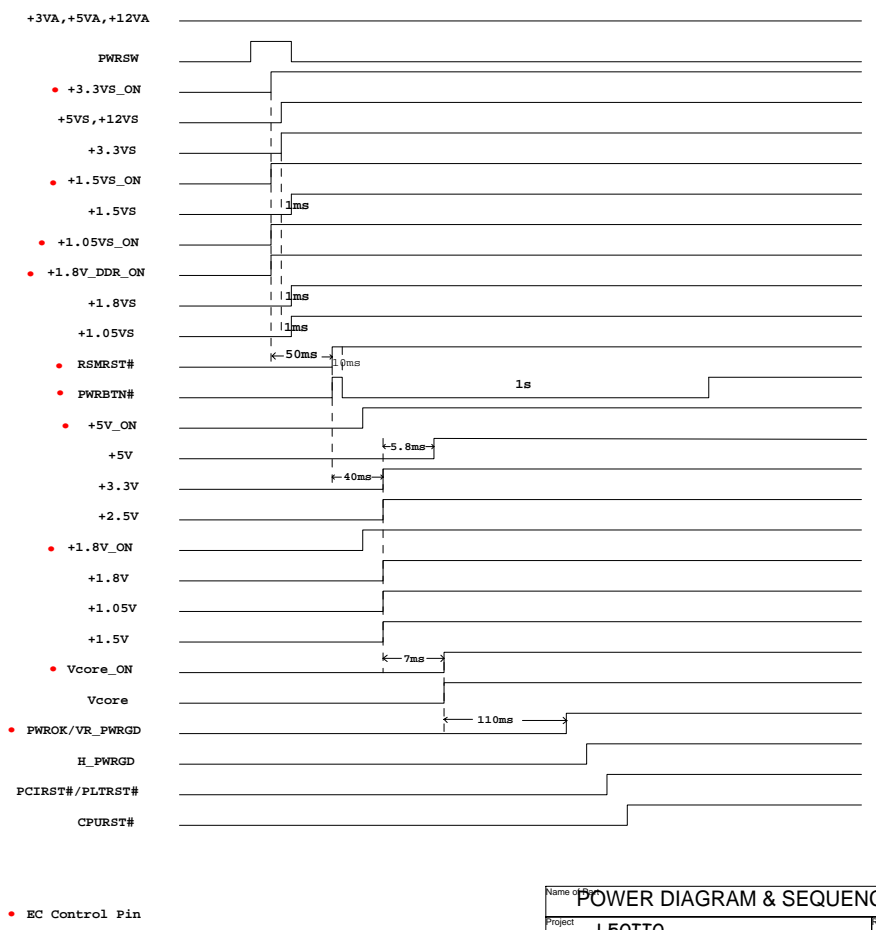
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POWER BLOCK DIAGRAM



POWER Sequence



Name of File: POWER DIAGRAM & SEQUENCE		
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3255 UNIWILL COMPUTER CORP.		

ICH6-M GPIO	
GPI0	BM_BUSY#
GP7	
GP8	EC_EXTSMI#
GPI11	SMB_ALERT#
GPI12	
GPI13	
GPI018	PM_STPPCI_ICH#
GPI019	
GPI020	PM_STPCPU_ICH#
GPI021	TPM_EN
GPI023	
GPI024	
GPI025	
GPI026	SATA0_GP
GPI027	
GPI028	
GPI029	PNLSW1
GPI030	PNLSW2
GPI031	PNLSW0
GPI032	PM_CLKRUN#
GPI033	
GPI034	

ITE8510E GPIO	
GPCF0	RF_SW#
GPCF1	SILENT# /
GPCF2	IR_PS2CLK1
GPCF3	IR_PS2DAT1
GPCF4	TP_CLK
GPCF5	TP_DATA
GPCF6	MAIL#
GPCF7	BROWSER#
GPI0	SCROLL#
GPI1	CAPS#
GPI2	NUM#
GPI3	CHG_R_LED#
GPI4	CHG_G_LED#
GPI5	SUSLED_LED#
GPI6	VOLMAX
GPH0	+1.8V_DDR_ON
GPH1	+1.8V_ON
GPH2	+1.05VS_ON
GPH3	+3.3VS_ON
GPH4	+5V_ON
GPH5	SET_V
GPH6	+1.5VS_ON
GPH7	VCORE_ON
GPG4	TP_DISABLE
GPG5	LCDSW
GPG6	MUTE#
GPG7	EXTTS#0
GPB0	CELERON_VO_DET
GPB1	CPPE#
GPB2	PM_RSMRST#
GPB3	BAT_SMBCLK
GPB4	BAT_SMBDAT
GPB5	H_A20GATE
GPB6	H_RCIN#
GPB7	RFLED_ON#
GPE0	NA
GPE1	CPU_BSEL0
GPE2	NA
GPE3	NA
GPE4	PWRSW
GPE5	LID#
GPE6	PCM#
GPE7	PM_SLP_S3#
GPD0	ADAP_IN
GPD1	REMOTE_ON#
GPD2	PCI_RST# / PLT_RST#
GPD3	EC_EXTSMI#
GPD4	PM_SLP_S4#
GPD5	PM_THROTTLING#
GPD6	FAN_SPD#
GPD7	EC_PREST#
GPA0	BTL_BEEP
GPA1	EC_VID1
GPA2	EC_VID2
GPA3	EC_VID3
GPA4	EC_VID4
GPA5	SMP1_EN#
GPA6	SMP2_EN#
GPA7	PWRBTN#

ITE8510E GPIO	
GPC0	PWR0K
GPC1	BAT2_SMBCLK
GPC2	BAT2_SMBDAT
GPC3	SB_ALERT#1
GPC4	SB_ALERT#2
GPC5	TP_LED#
GPC6	CHG_ON
GPC7	SILENT_LED#
ADC0	BAT_TEMP
ADC1	ADAPTOR_I
ADC2	DDR2_TEMP
ADC3	VGA_TEMP
DAC0	BRIGHTADJ
DAC1	CHG_I
DAC2	FAN_CTRL0
DAC3	NA

CPU				
CPU	CORE (V)	ICC (mA)	W	TEMP (°C)
2.0G	1.525	35.7	54.3	69
2.2G	1.525	37.5	57.1	70
2.26G	1.525	38.1	58.0	70
2.4G	1.525	39.3	59.8	71
2.5G	1.525	40	61.0	72
2.53G	1.525	40.4	61.5	72
2.6G	1.525	41.05	62.6	72
2.66G	1.525	43.35	66.1	74
2.8G	1.525	44.86	68.4	75
3.06G	1.525	55.9	85.2	81

MCHE			
VCC	ICC (mA)	W	TEMP (°C)
+3.3V	108.19	0.357	70
+3.3VA	501.3	1.254	
+2.5V	1390	2.502	
+1.5V	33.4	0.084	
+VCCP	10	0.018	
+VCC_SMBCLK	266	0.452	

ICH6-M			
VCC	ICC (mA)	W	TEMP (°C)
+3.3V	96	0.315	70
+3.3VA	275	0.909	
+1.5V	487	0.876	
+1.5VA	27	0.049	
+3.3VA_RTC	0.003	0.00001	

SMART POWER TABLE

VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE	+mV
0	0	0	0	0	0	0	1.5000	-0mV
0	0	0	0	0	0	1	1.4875	-2.5mV
0	0	0	0	0	1	0	1.4750	-5mV
0	0	0	0	1	0	0	1.4500	-50mV
0	0	0	1	0	0	0	1.4000	-100mV
0	0	1	0	0	0	0	1.3000	-200mV
0	1	0	0	0	0	0	1.1000	-400mV
1	0	0	0	0	0	0	0.7000	-800mV
0	0	1	1	0	1	1	1.1625	
0	0	1	0	0	0	1		
0	0	1	0	0	1	0		
0	0	1	0	1	0	0		
0	0	1	0	1	1	0		
0	0	1	1	0	0	1		
0	0	1	1	0	1	0		

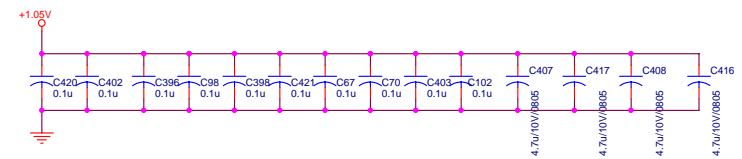
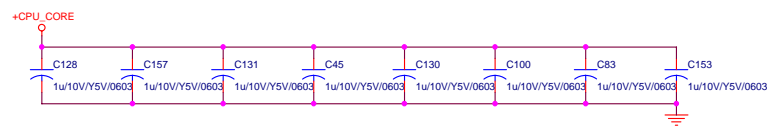
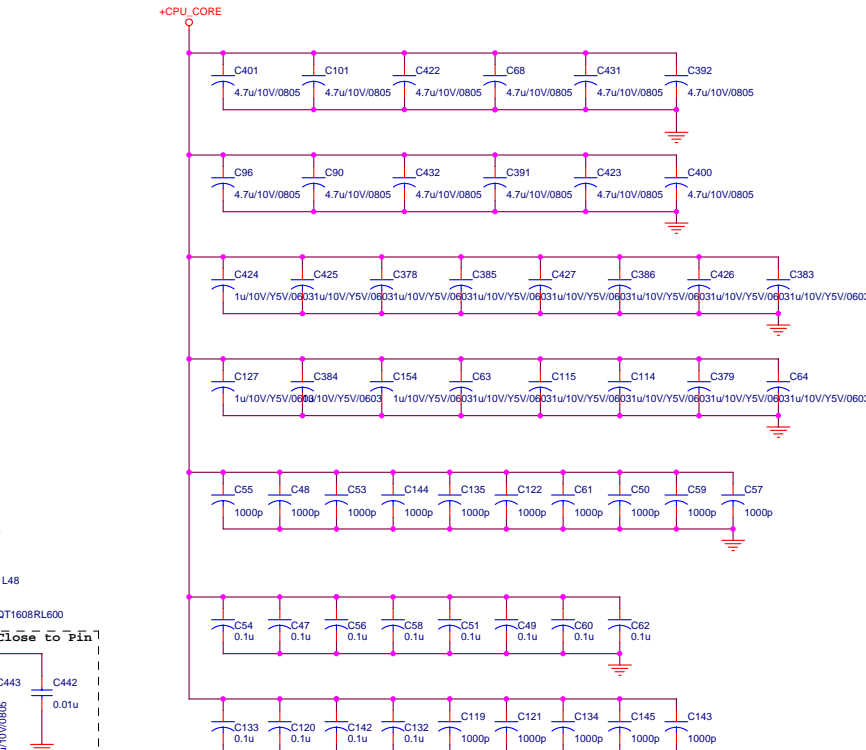
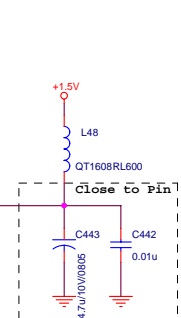
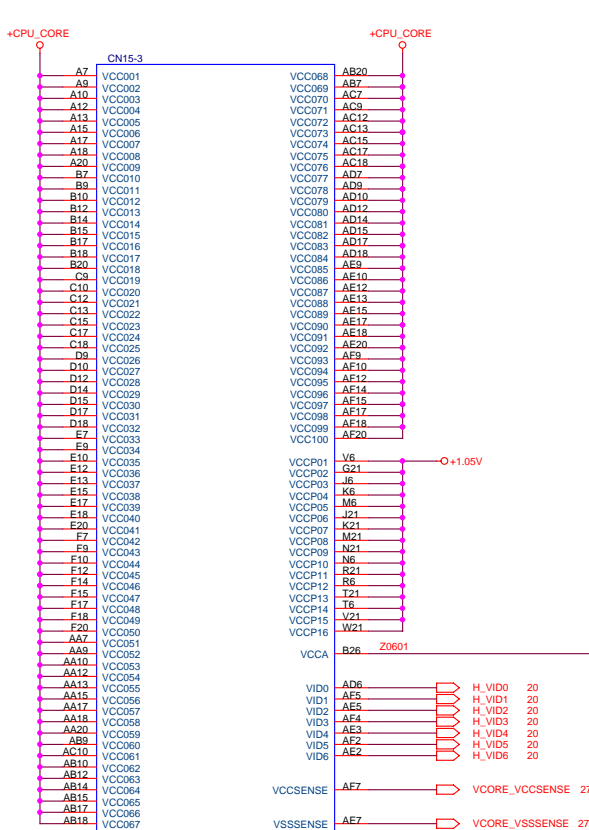
ITE8510E			
VCC	ICC (mA)	W	TEMP (°C)
+3.3V	300	1	70

CLOCK GENERATOR			
VCC	ICC (mA)	W	TEMP (°C)
+3.3V	180	0.594	70

ALC880			
VCC	ICC (mA)	W	TEMP (°C)
+3.3V(DVDD)	71	0.234	70

TPA6011A4			
VCC	ICC (mA)	W	TEMP (°C)
3.3V	30	0.099W	85

ADM1032			
VCC	ICC	W	TEMP (°C)
+3.3V	170uA	0.56mW	150



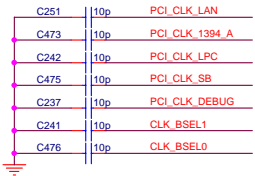
CN15-4		
A4	VSS001	VSS082
A8	VSS002	VSS083
A11	VSS003	VSS084
A14	VSS004	VSS085
A16	VSS005	VSS086
A19	VSS006	VSS087
A26	VSS007	VSS088
A33	VSS008	VSS089
B6	VSS009	VSS090
B8	VSS010	VSS091
B11	VSS011	VSS092
B13	VSS012	VSS093
B16	VSS013	VSS094
B19	VSS014	VSS095
B21	VSS015	VSS096
B24	VSS016	VSS097
C5	VSS017	VSS098
C8	VSS018	VSS099
C11	VSS019	VSS100
C14	VSS020	VSS101
C16	VSS021	VSS102
C19	VSS022	VSS103
C22	VSS023	VSS104
C25	VSS024	VSS105
C28	VSS025	VSS106
D1	VSS026	VSS107
D4	VSS027	VSS108
D8	VSS028	VSS109
D11	VSS029	VSS110
D13	VSS030	VSS111
D16	VSS031	VSS112
D19	VSS032	VSS113
D23	VSS033	VSS114
D26	VSS034	VSS115
E3	VSS035	VSS116
E6	VSS036	VSS117
E8	VSS037	VSS118
E11	VSS038	VSS119
E14	VSS039	VSS120
E16	VSS040	VSS121
E19	VSS041	VSS122
E21	VSS042	VSS123
E24	VSS043	VSS124
F5	VSS044	VSS125
F11	VSS045	VSS126
F8	VSS046	VSS127
F13	VSS047	VSS128
F16	VSS048	VSS129
F19	VSS049	VSS130
F2	VSS050	VSS131
F22	VSS051	VSS132
F25	VSS052	VSS133
G4	VSS053	VSS134
G1	VSS054	VSS135
G23	VSS055	VSS136
G36	VSS056	VSS137
H3	VSS057	VSS138
H6	VSS058	VSS139
H21	VSS059	VSS140
H24	VSS060	VSS141
J2	VSS061	VSS142
J5	VSS062	VSS143
J22	VSS063	VSS144
J25	VSS064	VSS145
K1	VSS065	VSS146
K4	VSS066	VSS147
K23	VSS067	VSS148
K26	VSS068	VSS149
L3	VSS069	VSS150
L6	VSS070	VSS151
L21	VSS071	VSS152
L24	VSS072	VSS153
M2	VSS073	VSS154
M5	VSS074	VSS155
M22	VSS075	VSS156
M25	VSS076	VSS157
N1	VSS077	VSS158
N4	VSS078	VSS159
N23	VSS079	VSS160
N26	VSS080	VSS161
P3	VSS081	VSS162

24089147

- QT1608GRL600 = 200mA
- QT1608RL120 = 200mA
- QT1608RL600 = 200mA
- QT1608RL030 = 500mA
- QT1608RL060 = 500mA

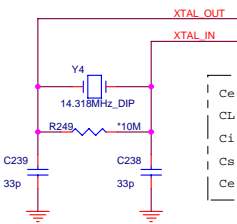
Name of Part		CPU_POWER	
Project	L50II0	Rev	B
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3255		UNIWILL COMPUTER CORP.	

Reserved FOR EMI



SELDOT , 1= Pin 14/15 DOT 96MHZ , Pin 17/18 LCDCLK
0= Pin 14/15 27MHZ Fix/SS Pin 17/18 PCIEIX

Bsel [0,2]
Vil = 0.3
Vih = 0.7



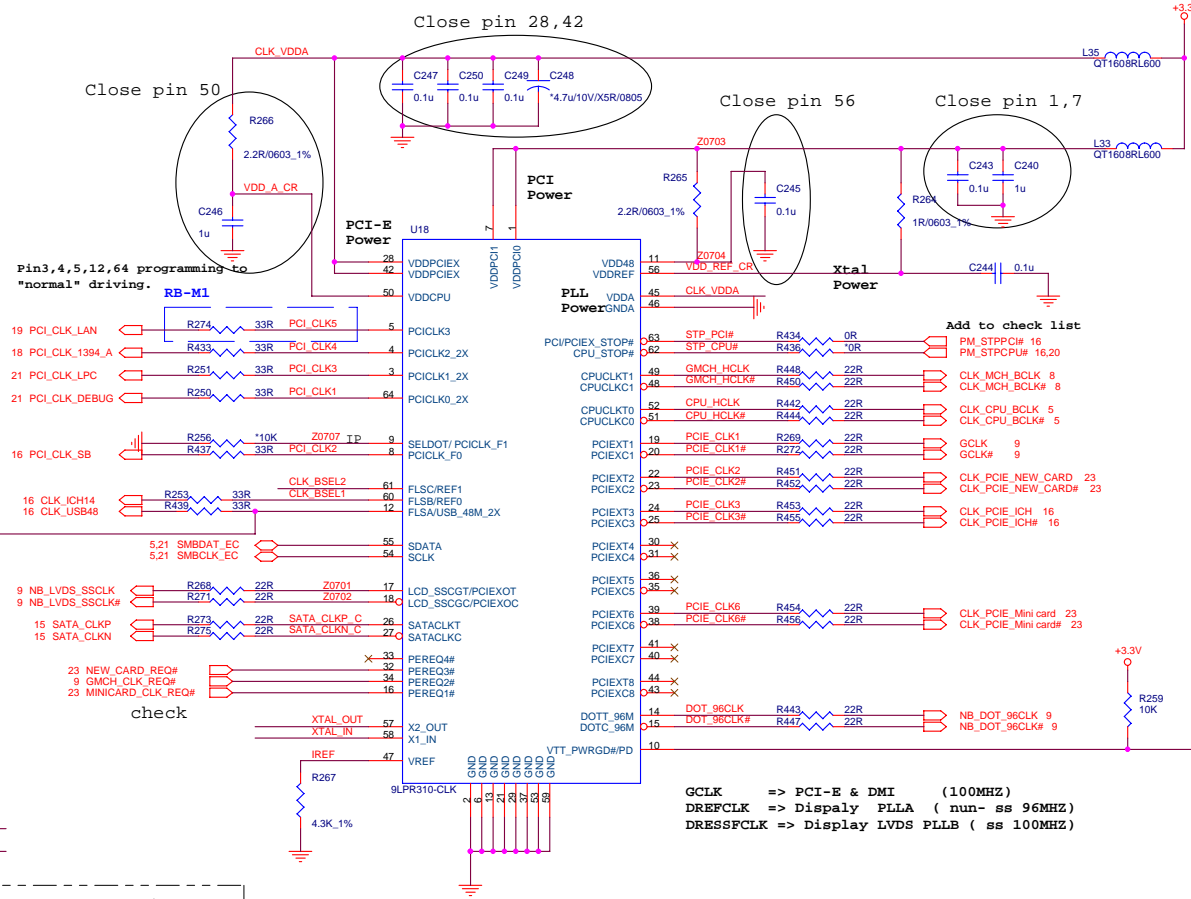
$$C_e = 2 * CL - (C_s + C_i)$$

CL = Crystal Load Cap = 20P
C_i = IC internal Cap = 5P
C_s = 2P
C_e = Crystal external Cap = 33P

- REQ1# = PCI-E 0,6
- REQ2# = PCI-E 1,8
- REQ3# = PCI-E 2,4
- REQ4# = PCI-E 3,5,7

	FS4	FS3	BSEL2 FSLC	BSEL1 FSLB	BSEL0 FSLA	CPU MHZ	PCI MHZ	PCI-E MHZ	SPREAD %
PSB533	0	0	0	0	1	133	33	100	0.5% DOWN
PSB667	0	0	0	1	1	166			
PSB533	0	1	0	0	1	133	33	100	+/- 0.25% CENTER
PSB667	0	1	0	1	1	166			

FS3 , FS 4 SEETING BY I2C BUS ???????



Pin Configuration

Pin	Signal	Pin	Signal
VDDPCI1	64	PCICLK0_2X	64
GND2	63	PCI/PCIE_X_STOP#	63
PCICLK1_2X3	62	CPU_STOP#	62
PCICLK2_2X4	61	REFI/FSLC	61
PCICLK3	60	FSLB/FSLB	60
GND6	59	GND	59
VDDPCI7	58	X1	58
PCICLK_F08	57	X2	57
*SELDOT/PCICLK_F19	56	VDDREF	56
VIT_PwrGd#/PD10	55	SDATA	55
VDD48	54	SCLK	54
FS_A/USB_48MHZ_2X12	53	GND	53
GND13	52	CPUCLKTOLP	52
27FIX/DOT96C_LP14	51	CPUCLKCOLP	51
27SS/DOT96C_LP15	50	VDDCPU	50
*PEREQ1#16	49	CPUCLKT1LP	49
PCIeTo_LP/LCDCLK_LP17	48	CPUCLKC1LP	48
PCIeCo_LP/LCDCLK_LP18	47	VREF	47
PCIeT1_LP19	46	GND4	46
PCIeC1_LP20	45	VDDA	45
GND21	44	PCIeT8_LP	44
PCIeT2_LP22	43	PCIeC8_LP	43
PCIeC2_LP23	42	VDDPCIEIX	42
PCIeT3_LP24	41	PCIeT7_LP	41
PCIeC3_LP25	40	PCIeC7_LP	40
SATACLKLP26	39	PCIeT6_LP	39
SATACLKLP27	38	PCIeC6_LP	38
VDDPCIEIX28	37	GND	37
GND29	36	PCIeT5_LP	36
PCIeT4_LP30	35	PCIeC5_LP	35
PCIeC4_LP31	34	PEREQ2#	34
*PEREQ3#32	33	PEREQ4#	33

64-TSSOP
* Internal Pull-Up Resistor
** Internal Pull-Down Resistor

GCLK => PCI-E & DMI (100MHZ)
DREFCLK => Dispaly PLLA (nun- ss 96MHZ)
DRESSFCLK => Display LVDS PLLB (ss 100MHZ)

Functionality Table

FS4	FS3	FS2	CPU MHz	PCI MHz	PCI-E MHz	Spread %
0	0	0	266.66	33.33	100.00	0.5% Down
0	0	1	133.33	33.33	100.00	0.5% Down
0	1	0	200.00	33.33	100.00	0.5% Down
0	1	1	166.66	33.33	100.00	0.5% Down
1	0	0	333.33	33.33	100.00	0.5% Down
1	0	1	100.00	33.33	100.00	0.5% Down
1	1	0	400.00	33.33	100.00	0.5% Down
1	1	1	200.00	33.33	100.00	0.5% Down

Name of Part: **CLK GEN**

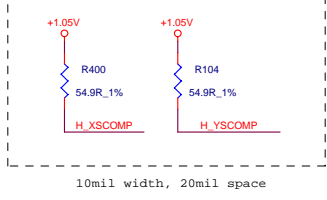
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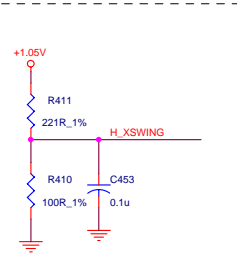
3255 **UNIWILL COMPUTER CORP.**

U14J		
AT23	VSS_180	J11
AN23	VSS_181	D11
AM23	VSS_182	B11
AC23	VSS_183	AV10
W23	VSS_185	AP10
K23	VSS_186	AL10
J23	VSS_187	AV10
F23	VSS_188	AC10
C23	VSS_189	W10
A422	VSS_190	L10
K22	VSS_191	BA9
G22	VSS_192	AW9
F22	VSS_193	AR9
E22	VSS_194	AH9
D22	VSS_195	AB9
A22	VSS_196	Y9
AV21	VSS_197	G9
AR21	VSS_199	E9
AN21	VSS_200	AG8
AL21	VSS_201	AD8
Y21	VSS_202	AA8
K21	VSS_204	UB
J21	VSS_206	K8
H21	VSS_207	C8
C21	VSS_208	BA7
AW20	VSS_209	AV7
AR20	VSS_210	AP7
AM20	VSS_211	AL7
AA20	VSS_212	AH7
K20	VSS_213	AF7
B20	VSS_214	U8
A20	VSS_215	R7
AN19	VSS_216	G7
AC19	VSS_217	D7
W19	VSS_218	AG6
K19	VSS_219	AD6
G19	VSS_220	AB6
C19	VSS_221	Y6
AV18	VSS_222	UB
AR18	VSS_223	N6
P18	VSS_224	K6
H18	VSS_225	H6
D18	VSS_226	B6
A18	VSS_227	AV5
AY17	VSS_228	AF5
AB17	VSS_229	AD5
AM17	VSS_230	AL5
AK17	VSS_231	AR4
AM16	VSS_232	AP4
AN16	VSS_233	AL4
AL16	VSS_234	Y4
J16	VSS_235	UB
F16	VSS_236	R4
C16	VSS_237	J4
AN15	VSS_238	F4
AM15	VSS_239	C4
AK15	VSS_240	AY3
N15	VSS_241	AW3
M15	VSS_242	AV3
L15	VSS_243	AL3
B15	VSS_244	AH3
A15	VSS_245	AB3
BA14	VSS_246	AD3
AT14	VSS_247	AC3
AK14	VSS_248	G3
AD14	VSS_249	AT2
AA14	VSS_250	AR2
U14	VSS_251	AP2
K14	VSS_252	AK2
H14	VSS_253	AJ2
E14	VSS_254	AD2
AV13	VSS_255	AB2
AR13	VSS_256	Y2
AM13	VSS_257	UB
AL13	VSS_258	L2
AG13	VSS_259	T2
P13	VSS_260	N2
F13	VSS_261	J2
D13	VSS_262	H2
B13	VSS_263	E2
AY12	VSS_264	F2
AC12	VSS_265	C2
K12	VSS_266	C2
H12	VSS_267	AL1
E12	VSS_268	
AD11	VSS_269	
AA11	VSS_270	
Y11	VSS_271	
	VSS_272	

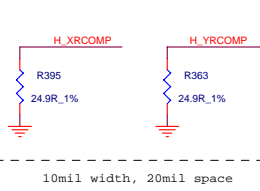
FSB I/O slew rate compensation



Reference Voltage for RCOMP



Calibration FSB I/O Buffer



5 H_D# [8:3]

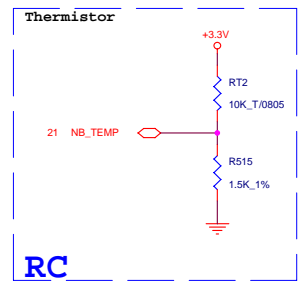
5 H_A# [31:3]

U14A		
H_D#0	F1	H_D#_0
H_D#1	J1	H_D#_1
H_D#2	H1	H_D#_2
H_D#3	JB	H_D#_3
H_D#4	KB	H_D#_4
H_D#5	K2	H_D#_5
H_D#6	G2	H_D#_6
H_D#7	G2	H_D#_7
H_D#8	K9	H_D#_8
H_D#9	K1	H_D#_9
H_D#10	J8	H_D#_10
H_D#11	K7	H_D#_11
H_D#12	H4	H_D#_12
H_D#13	JA	H_D#_13
H_D#14	K11	H_D#_14
H_D#15	G4	H_D#_15
H_D#16	T10	H_D#_16
H_D#17	W11	H_D#_17
H_D#18	T3	H_D#_18
H_D#19	U7	H_D#_19
H_D#20	U9	H_D#_20
H_D#21	U11	H_D#_21
H_D#22	T11	H_D#_22
H_D#23	W9	H_D#_23
H_D#24	T8	H_D#_24
H_D#25	T8	H_D#_25
H_D#26	T4	H_D#_26
H_D#27	W7	H_D#_27
H_D#28	U5	H_D#_28
H_D#29	T9	H_D#_29
H_D#30	W6	H_D#_30
H_D#31	T6	H_D#_31
H_D#32	AB2	H_D#_32
H_D#33	AA9	H_D#_33
H_D#34	WA	H_D#_34
H_D#35	W3	H_D#_35
H_D#36	Y3	H_D#_36
H_D#37	Y7	H_D#_37
H_D#38	W5	H_D#_38
H_D#39	V10	H_D#_39
H_D#40	ABA	H_D#_40
H_D#41	V2	H_D#_41
H_D#42	AA4	H_D#_42
H_D#43	AA7	H_D#_43
H_D#44	AA2	H_D#_44
H_D#45	AA8	H_D#_45
H_D#46	AA10	H_D#_46
H_D#47	Y8	H_D#_47
H_D#48	AA1	H_D#_48
H_D#49	AA4	H_D#_49
H_D#50	AC3	H_D#_50
H_D#51	AB11	H_D#_51
H_D#52	AC11	H_D#_52
H_D#53	AB3	H_D#_53
H_D#54	AC2	H_D#_54
H_D#55	AD1	H_D#_55
H_D#56	AD9	H_D#_56
H_D#57	AC1	H_D#_57
H_D#58	AD7	H_D#_58
H_D#59	AC8	H_D#_59
H_D#60	AB5	H_D#_60
H_D#61	AD10	H_D#_61
H_D#62	AD4	H_D#_62
H_D#63	AC8	H_D#_63

H_XRCOMP E1
H_XSCOMP E2
H_XSWING E4

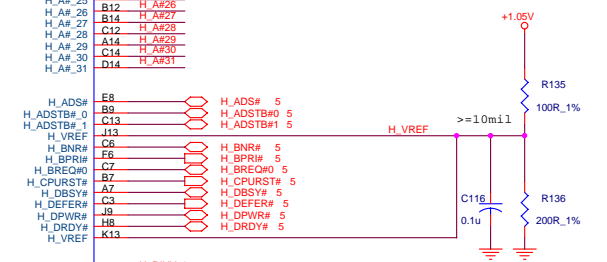
H_YRCOMP Y1
H_YSCOMP U1
H_YSWING W1

7 CLK_MCH_BCLK AG2
7 CLK_MCH_BCLK# AG1



HOSI

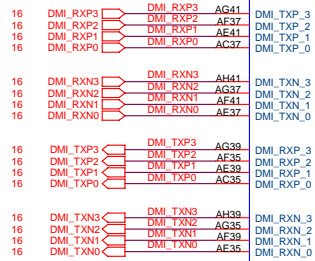
HOSI		
H_A#_3	H9	H_A#3
H_A#_4	C8	H_A#4
H_A#_5	E11	H_A#5
H_A#_6	G11	H_A#6
H_A#_7	E11	H_A#7
H_A#_8	G12	H_A#8
H_A#_9	F9	H_A#9
H_A#_10	H11	H_A#10
H_A#_11	I12	H_A#11
H_A#_12	G14	H_A#12
H_A#_13	D9	H_A#13
H_A#_14	I14	H_A#14
H_A#_15	H13	H_A#15
H_A#_16	I15	H_A#16
H_A#_17	E14	H_A#17
H_A#_18	D12	H_A#18
H_A#_19	A11	H_A#19
H_A#_20	A12	H_A#20
H_A#_21	A13	H_A#21
H_A#_22	E13	H_A#22
H_A#_23	G13	H_A#23
H_A#_24	E12	H_A#24
H_A#_25	B12	H_A#25
H_A#_26	B14	H_A#26
H_A#_27	C12	H_A#27
H_A#_28	A14	H_A#28
H_A#_29	C14	H_A#29
H_A#_30	D14	H_A#30
H_A#_31	D14	H_A#31



HOSI		
H_ADS#	E8	H_ADS# 5
H_ADSTB#_0	C13	H_ADSTB#0 5
H_ADSTB#_1	I13	H_ADSTB#1 5
H_VREF	C6	H_VREF
H_BNR#	E6	H_BNR# 5
H_BREQ#_0	C7	H_BREQ#0 5
H_CPURST#	B7	H_CPURST# 5
H_DESY#	A7	H_DESY# 5
H_DEFER#	C3	H_DEFER# 5
H_DPWR#	JB	H_DPWR# 5
H_DRDY#	HB	H_DRDY# 5
H_VREF	K13	H_VREF
H_DIN#_0	J7	H_DIN#0 5
H_DIN#_1	W8	H_DIN#1 5
H_DIN#_2	U3	H_DIN#2 5
H_DIN#_3	AB10	H_DIN#3 5
H_DSTB#0	K4	H_DSTB#0 5
H_DSTB#1	I7	H_DSTB#1 5
H_DSTB#2	Y5	H_DSTB#2 5
H_DSTB#3	AC4	H_DSTB#3 5
H_DSTB#0	K3	H_DSTB#0 5
H_DSTB#1	I6	H_DSTB#1 5
H_DSTB#2	AA5	H_DSTB#2 5
H_DSTB#3	AC5	H_DSTB#3 5
H_HIT#	D3	H_HIT# 5
H_HITM#	D4	H_HITM# 5
H_LOCK#	B3	H_LOCK# 5
H_REQ#_0	D8	H_REQ#(4:0) 5
H_REQ#_1	C8	H_REQ#1 5
H_REQ#_2	B8	H_REQ#2 5
H_REQ#_3	F8	H_REQ#3 5
H_REQ#_4	A8	H_REQ#4 5
H_RS#_0	B4	H_RS#(2:0) 5
H_RS#_1	E6	H_RS#1 5
H_RS#_2	D6	H_RS#2 5
H_SLP#_UP	E3	H_CPUSLP#_GMCH
H_TRDY#	E7	H_CPUSLP# 5.15 H_TRDY# 5

Name of Part	NB(1)_Host	
Project	L50IIO	Rev B
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3255	UNIWILL COMPUTER CORP.	

U14B



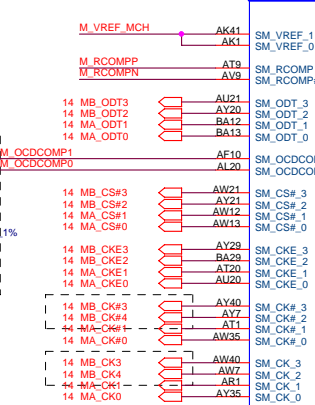
DMI

NC



CLK

PM

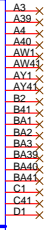


DDR

CFG

MUXING

RSVD



MISC

PM

CFG

RSVD



MISC

PM

CFG

RSVD

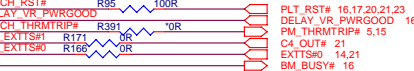
GCLK => PCI-E & DMI (100MHZ)
 DREFCLK => Display PLLA (nun-ss 96MHZ)
 DRESSFCLK => Display LVDS PLLB (ss 100MHZ)

SDVODATA has internal pull down
 0= no DVO device
 1= DVO device present
 SDVOCLK has internal pull down .

Asserted to control the raw PCI-E clock



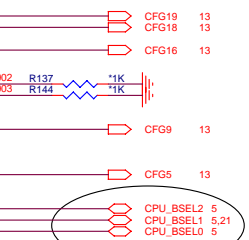
Asserted to synchronize with ICH on fault



PWROK input level
 PM_THRMTRIP# space 2:1

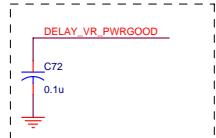
Break event in C3 state.

GHCH integrated graphics busy

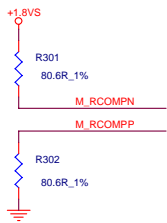
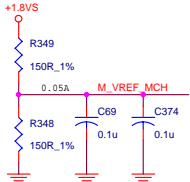
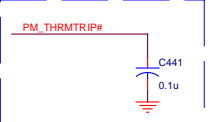


Base on PWROK

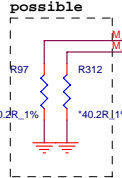
Cause to NB



RB->M2

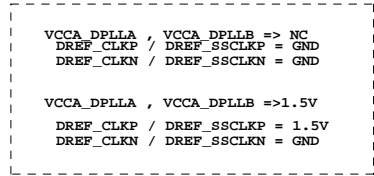


as short as possible

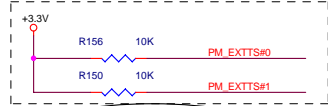


SM_CKE_2(#) connected to Dimm1 CK1(#)
 SM_CKE_3(#) connected to Dimm1 CK0(#)

Only Base on Discreted VGA



For MEN bus throttling

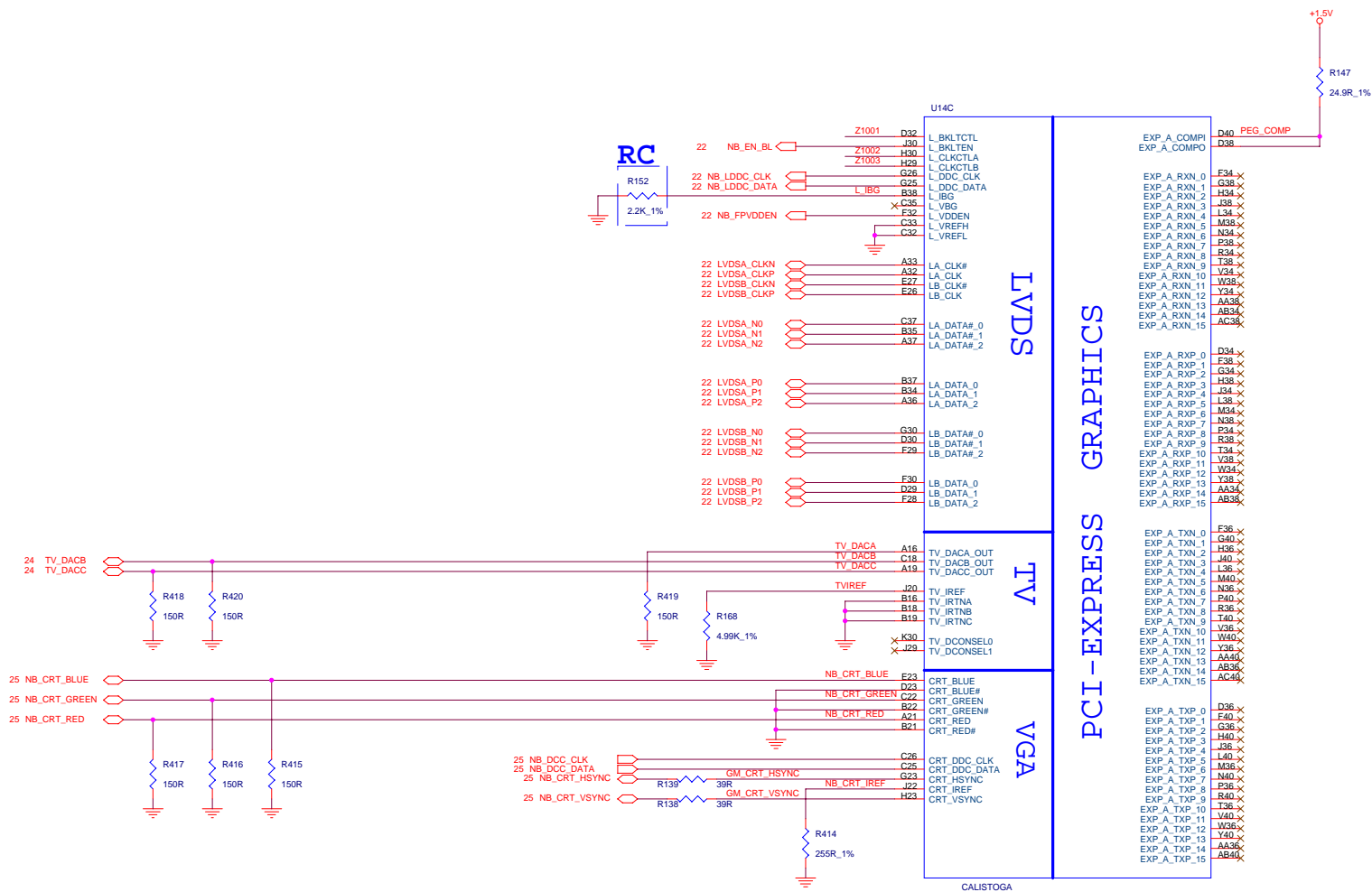


Check with S/W

CFG0	CFG1	CFG2	Host Clock frequency
1	0	0	133
1	1	0	166

CFG7 (IPU) => 1= Mobility CPU
 0 = Reverse

Name of Part	NB(2)_DMI/VGA/MICS	
Project	L50IIO	Rev B
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TC Modify 0914

Name of Part		NB(3)_VGA_TV_LVDS	
Project	L50IIO	Rev	B
Date:	Wednesday, April 19, 2006	Sheet	10 / 33
3255 UNIWILL COMPUTER CORP.			

14 MA_DQ[63:0]

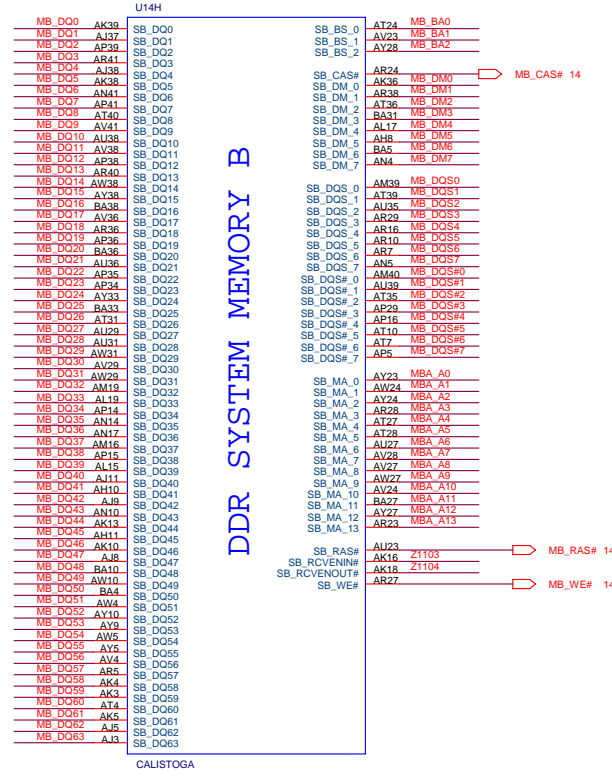
MA_BA[2:0] 14
MA_DM[7:0] 14
MA_DQS[7:0] 14
MA_DQS# [7:0] 14
MAA_A[13:0] 14

14 MB_DQ[63:0]

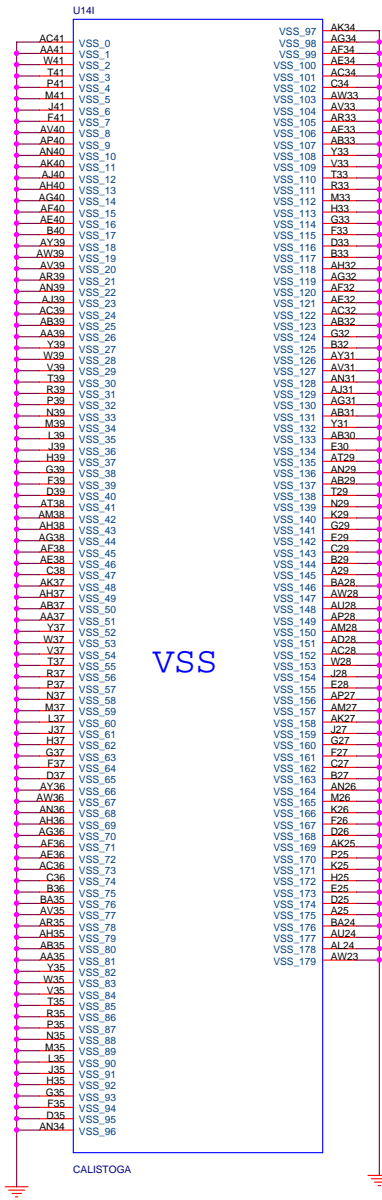
MB_BA[2:0] 14
MB_DM[7:0] 14
MB_DQS[7:0] 14
MB_DQS# [7:0] 14
MBA_A[13:0] 14



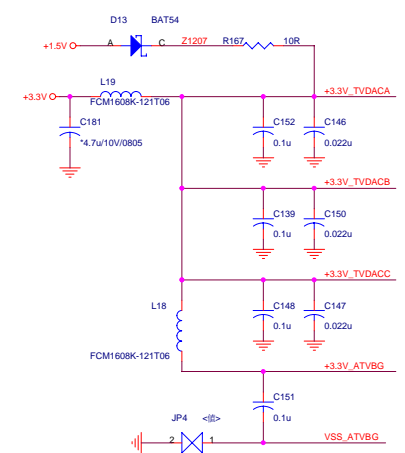
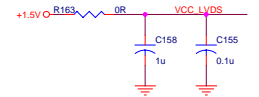
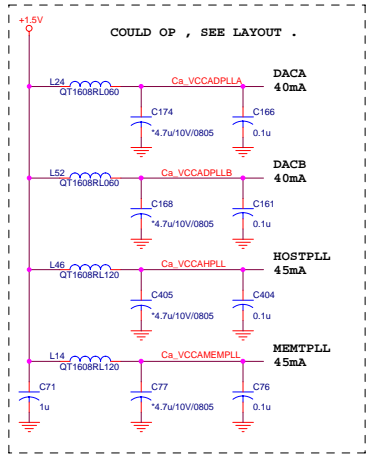
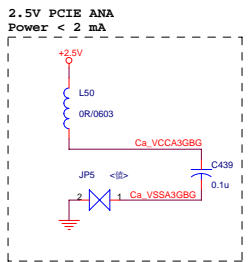
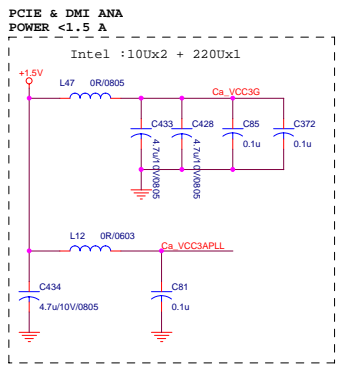
DDR SYSTEM MEMORY A



DDR SYSTEM MEMORY B

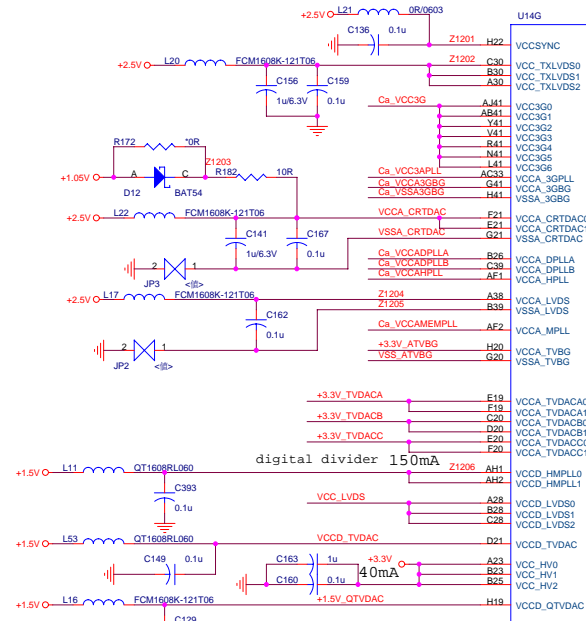
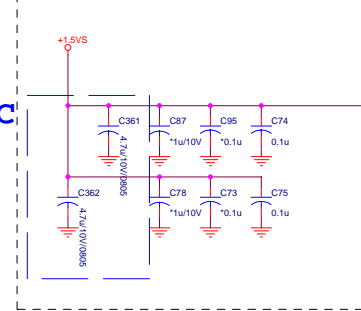


Name of Part	NB(3)_DDR2	
Project	L50II0	Rev B
Date: Wednesday, April 19, 2006	Sheet	11 / 33
3255	UNIWILL COMPUTER CORP.	

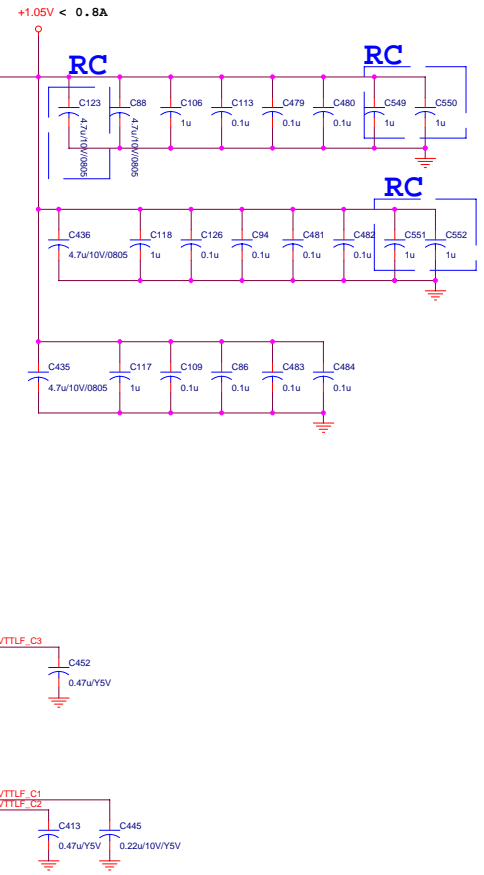


For DDR DLL , DDR IO ,
FSB IO < 1.9A

Filter component only need when GMCH
core is 1.5V for extended graphics
performance .

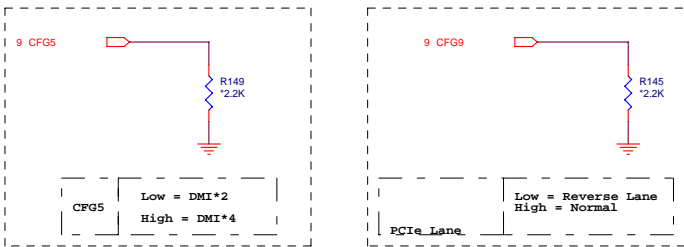
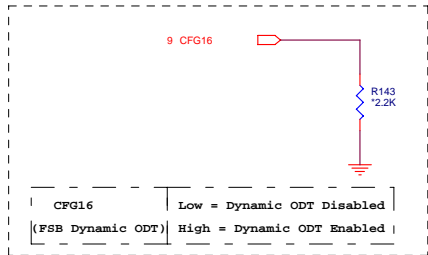


POWER

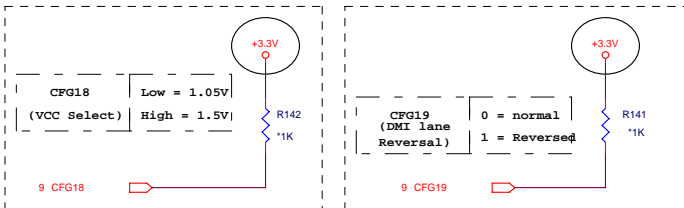


- NB 1.05V layout < 2.5A
- NB 1.5VS layout < 1.9A
- NB 1.5V layout < 1.8A
- NB 2.5V layout < 0.1A
- NB 3.3V layout < 0.1A
- NB 1.8VS layout < 3.2A

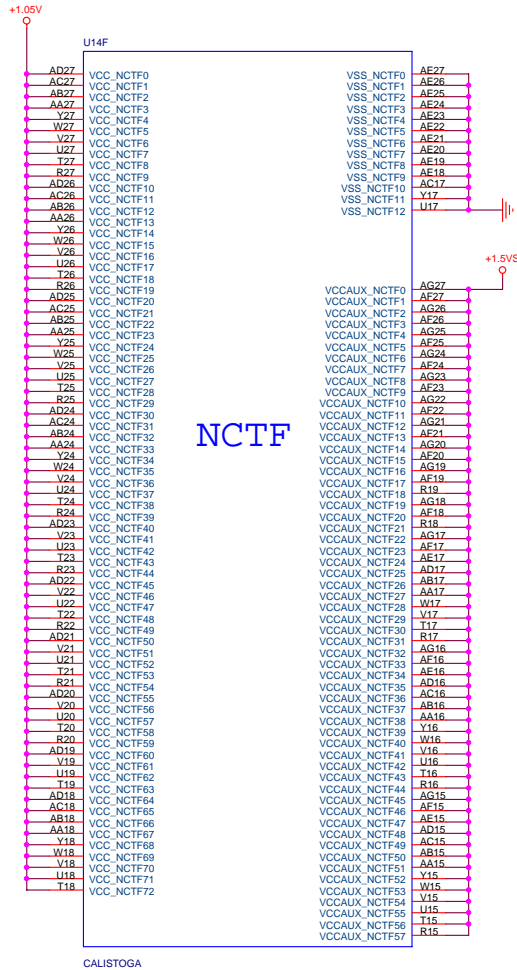
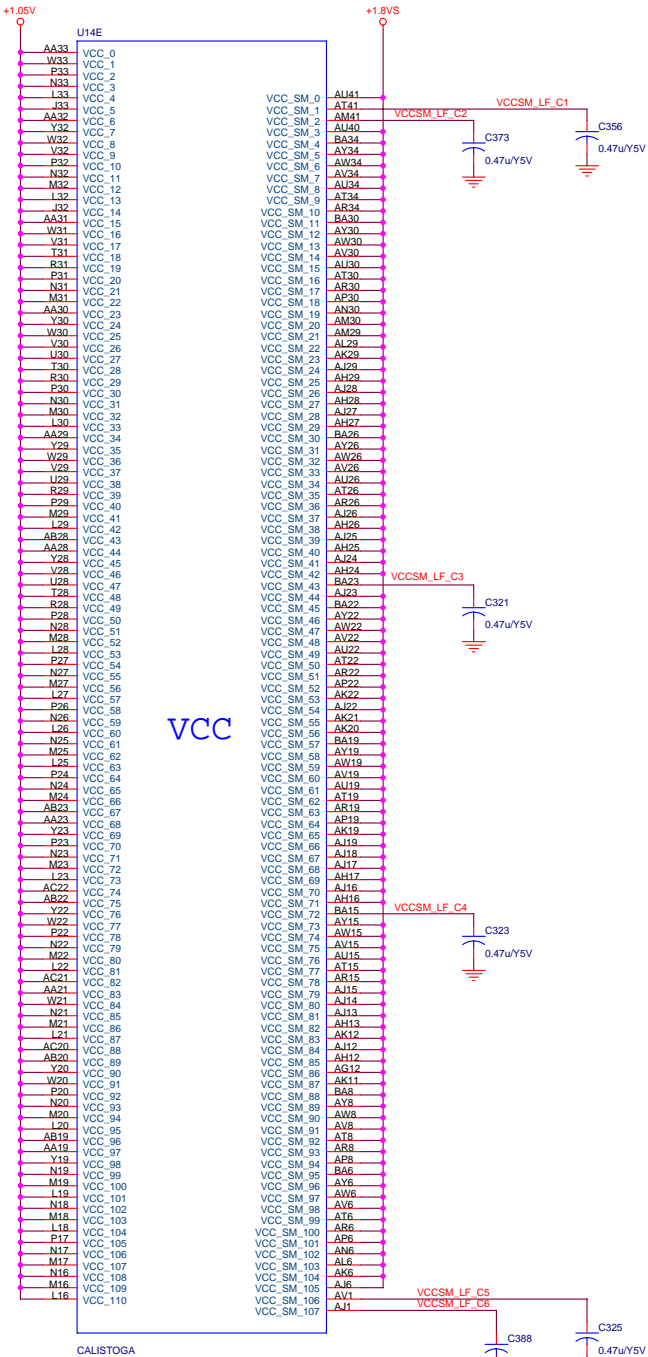
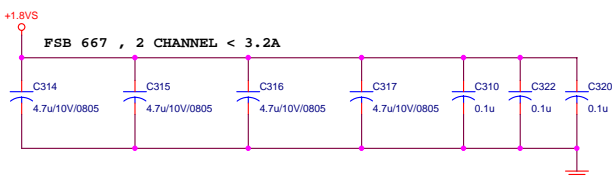
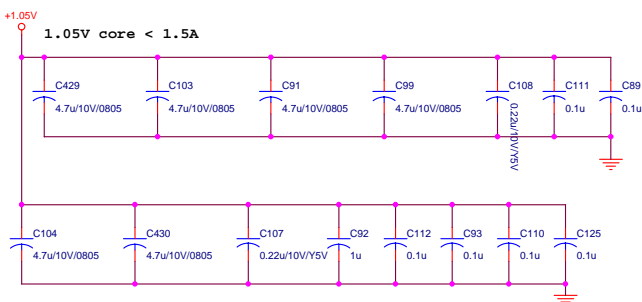
Name of Part		NB(4)_POWER	
Project	L50IIO	Rev	B
Date:	Wednesday, April 19, 2006	Sheet	12 / 33
UNWILL COMPUTER CORP.			



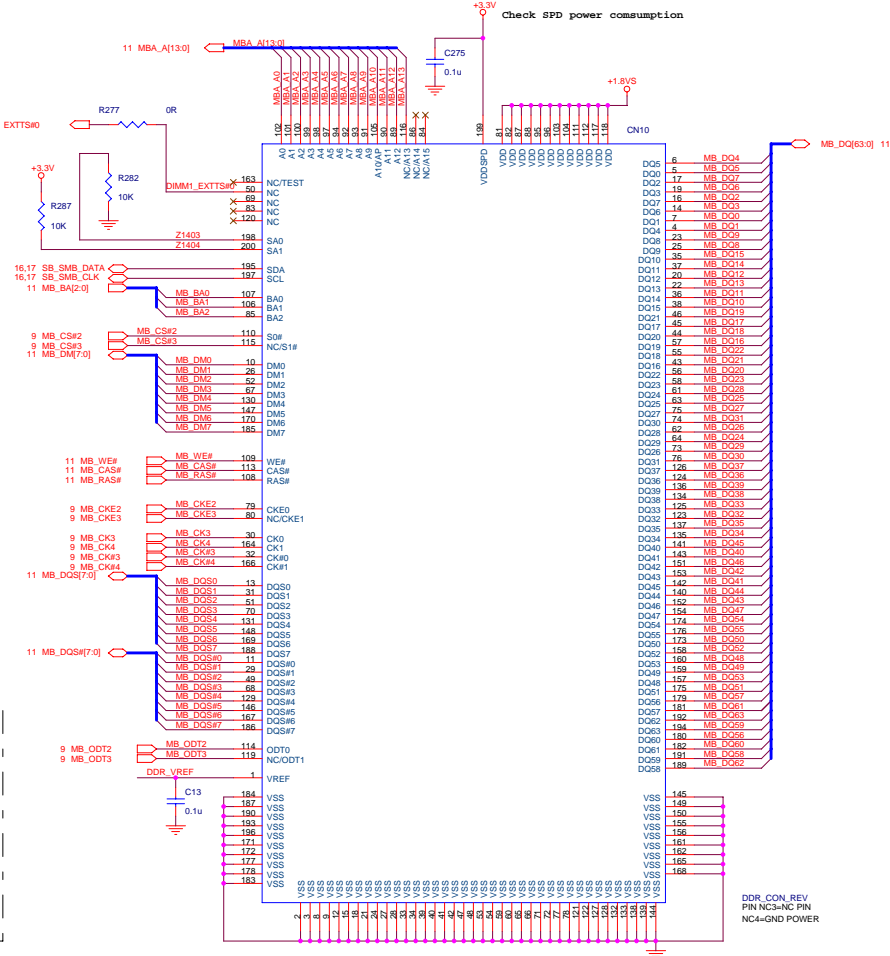
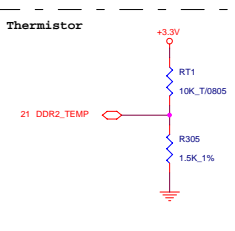
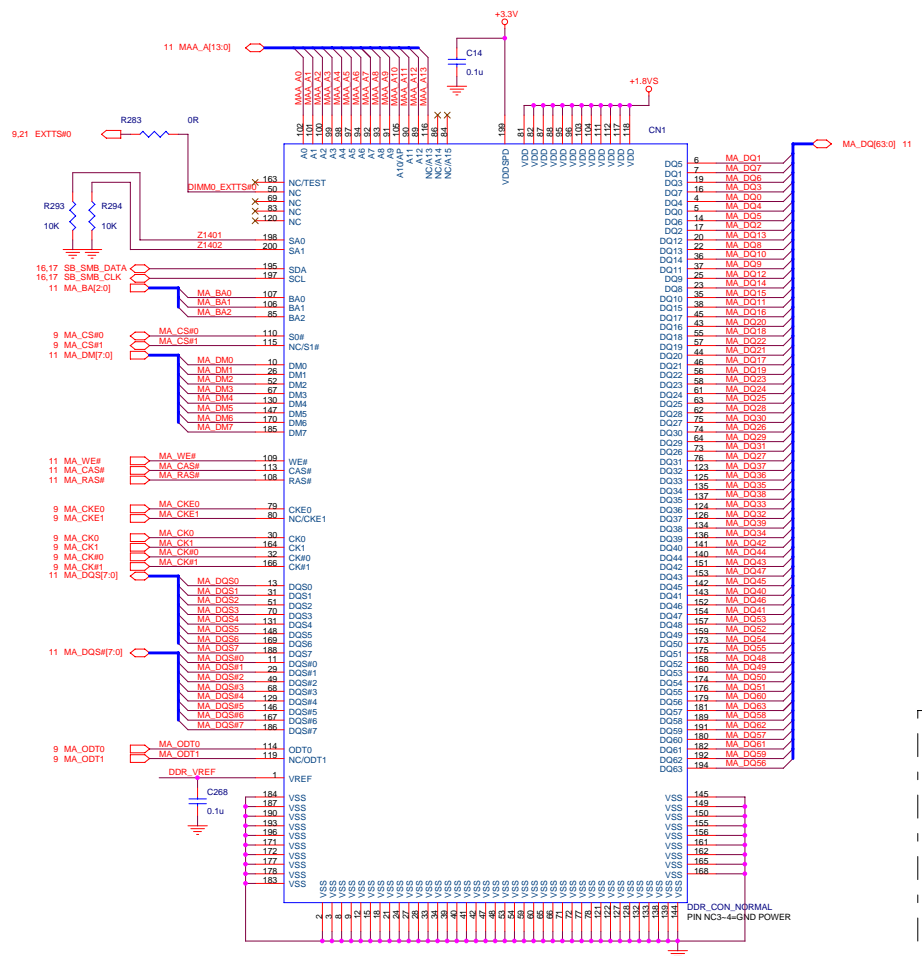
CFG[17:3] have internal pullup resistors. Design guide use 2.5V



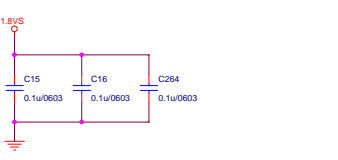
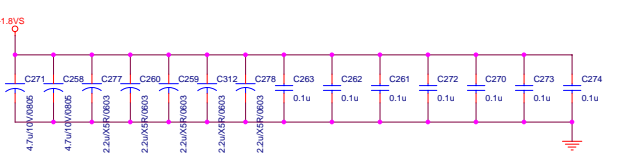
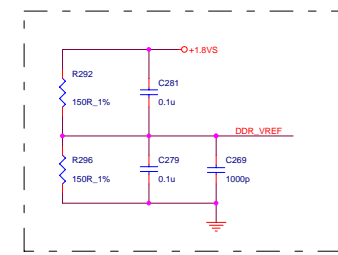
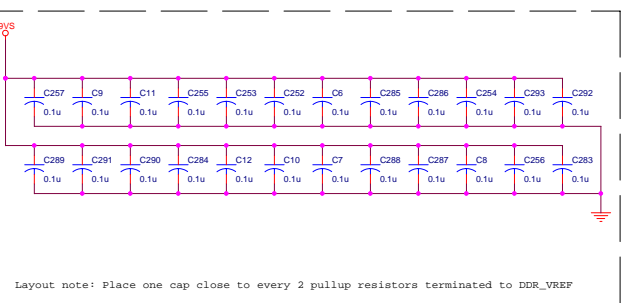
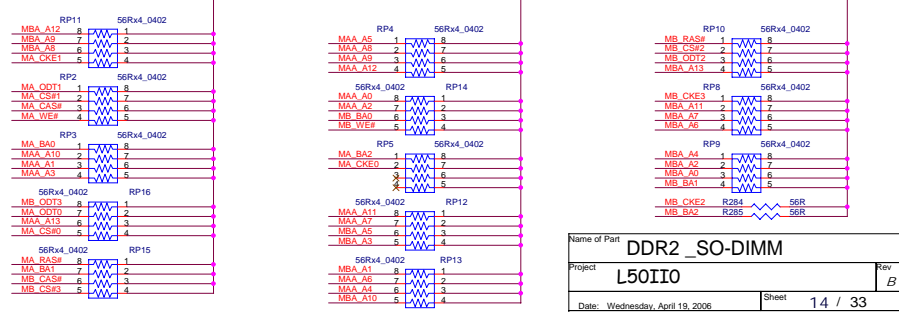
CFG[20:18] have internal pulldown resistors.

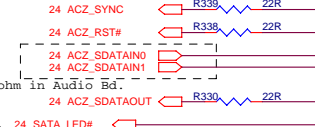
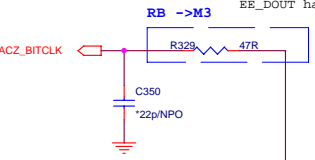
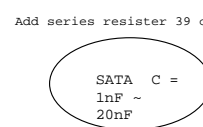
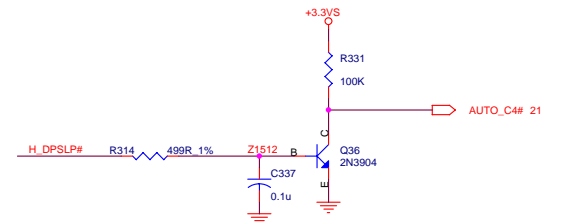
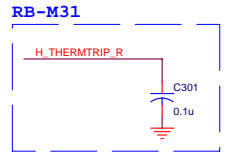
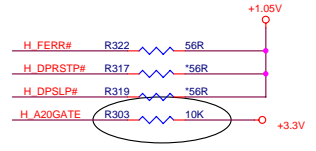
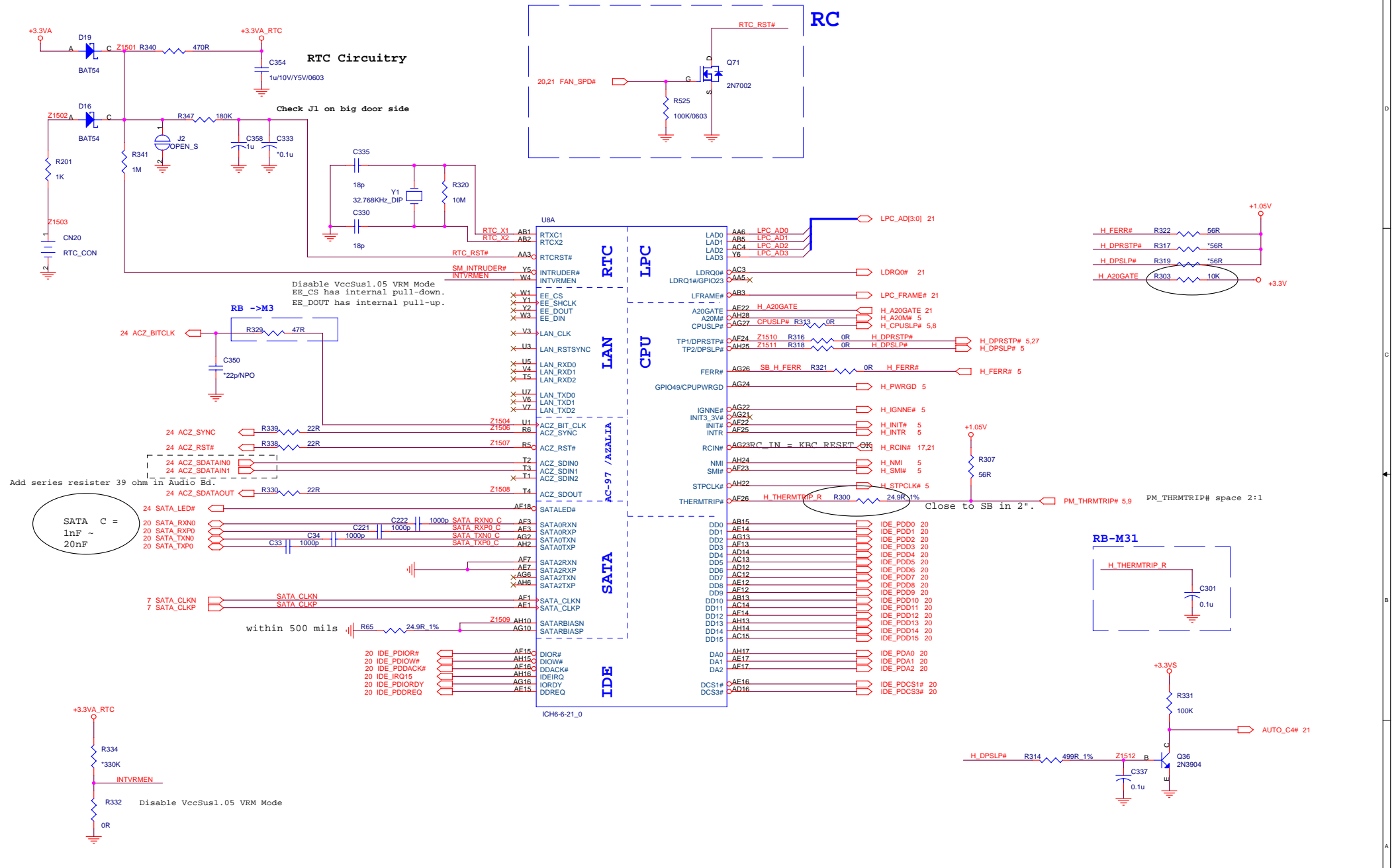


Name of Part	NB(5)_POWER	
Project	L50II0	Rev B
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3255	UNIWILL COMPUTER CORP.	



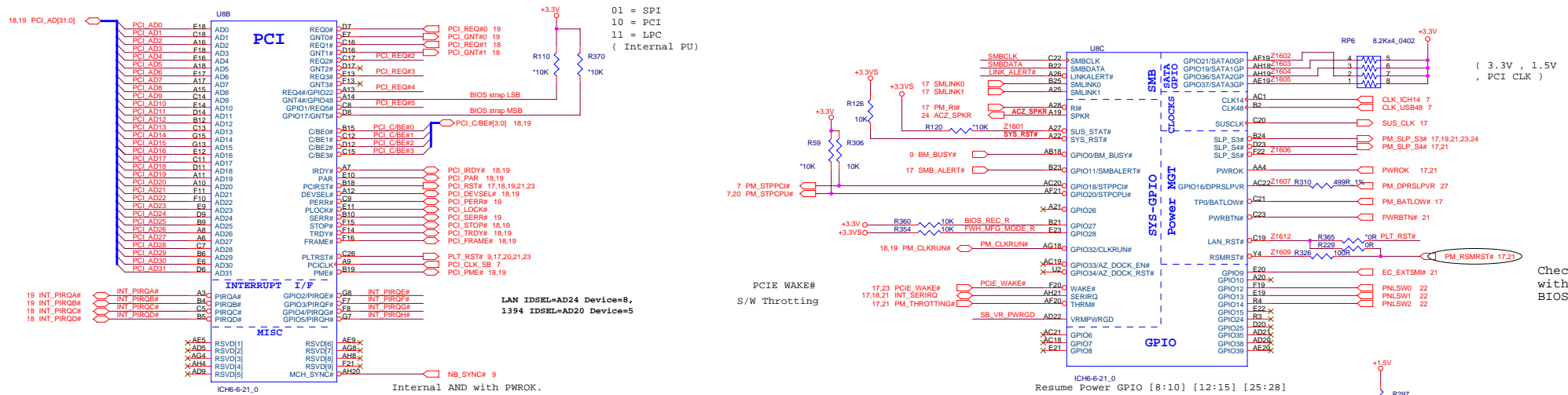
DDR2 Terminate (SWAP RP PIN when layout)



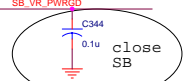


Close to SB in 2". PM_THRMTRIP# 5.9 PM_THRMTRIP# space 2:1

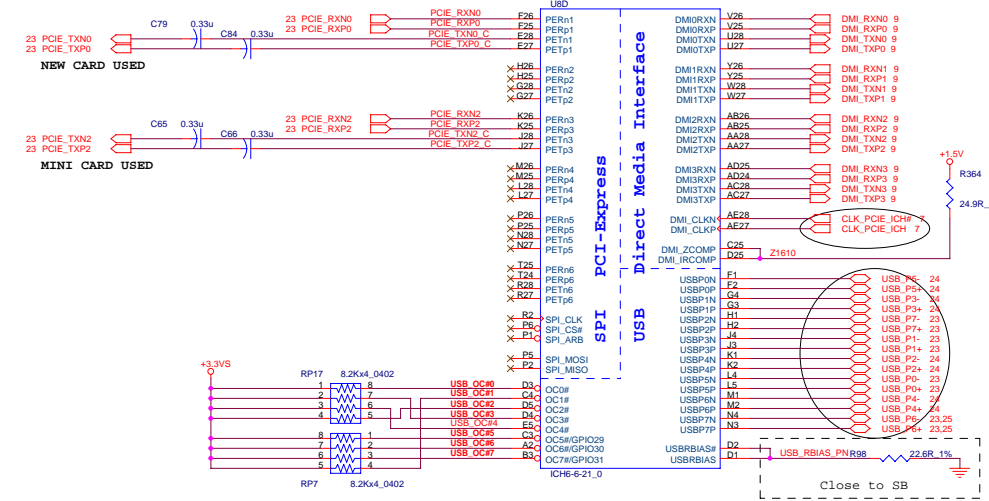
Name of Part		
SB(1)_CPU/SATA/IDE		
Project	L50IIO	Rev B
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UNIWILL COMPUTER CORP.		
3255		



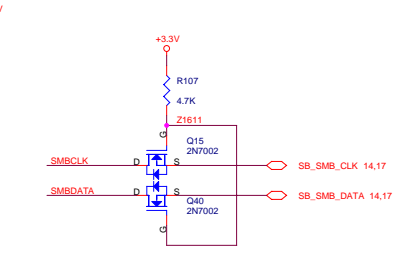
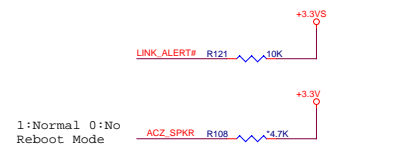
PLTRST = platform Reset
 High minimum 1ms after both PEROK & VRMPWRGD are high



ICH7M support PCI-E port1-4,
 ICH7M-DH support PCI-E port1-6.

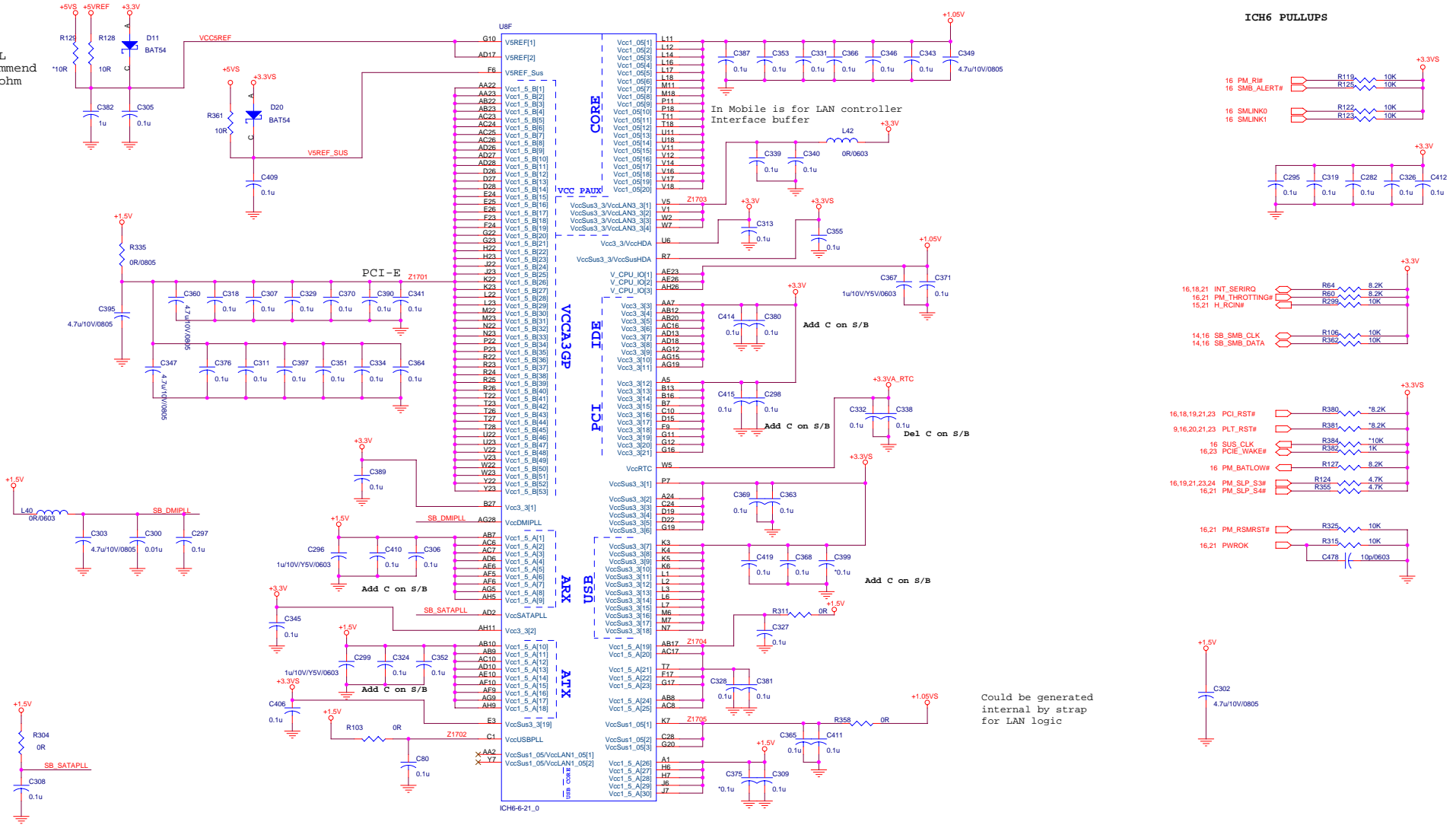


L50110	
USB0	3G MODULE
USB1	NEW CARD
USB2	AUDIO USB
USB3	AUDIO USB
USB4	MDC USB
USB5	M/B USB
USB6	FRBDD
USB7	MINI CARD

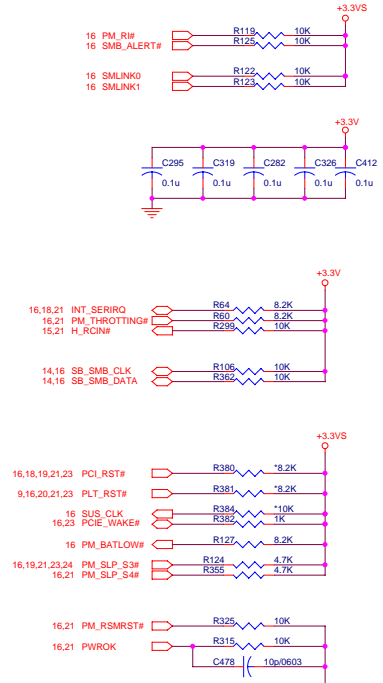


Name of Part	SB(2)_IO/GPIO/SYS	
Project	L50110	Rev
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UNWILL COMPUTER CORP.		

INTEL
recommend
100 ohm



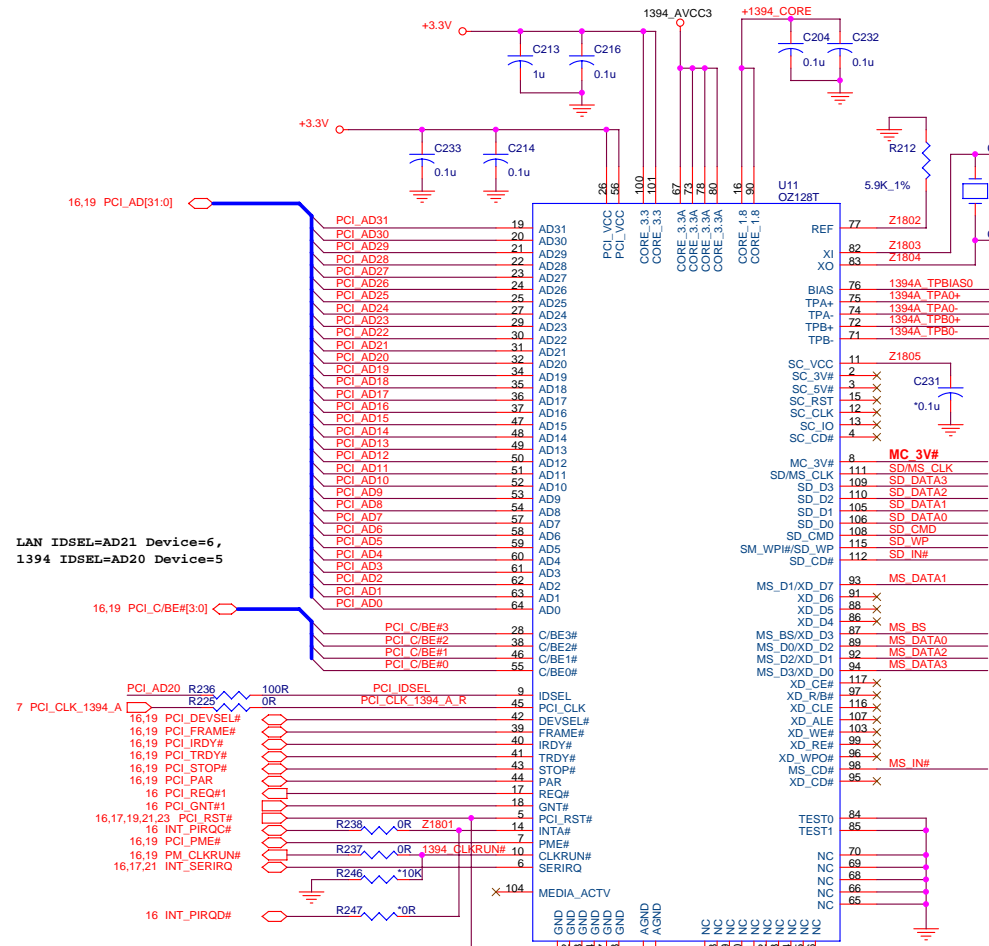
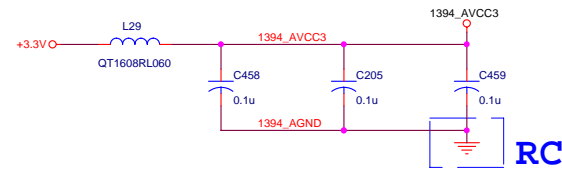
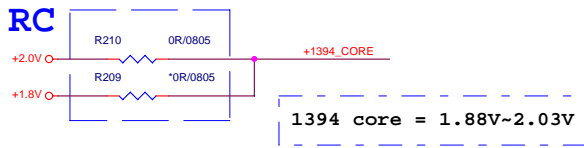
ICH6 PULLUPS



USB



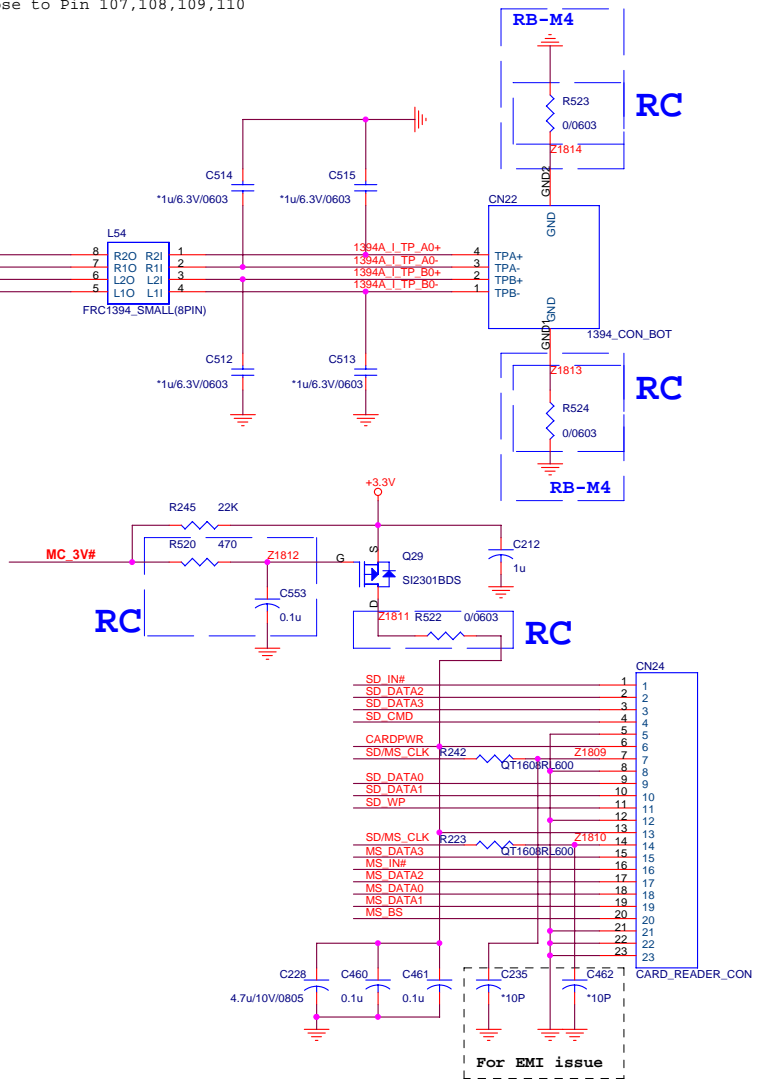
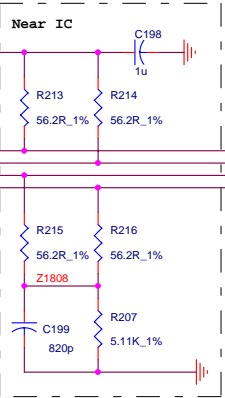
Name of Part	SB(3)_Power	
Project	L50IIO	Rev B
Date:	Wednesday, April 19, 2006	Sheet 17 / 33
UNWILL COMPUTER CORP.		



LAN IDSEL=AD21 Device=6,
1394 IDSEL=AD20 Device=5

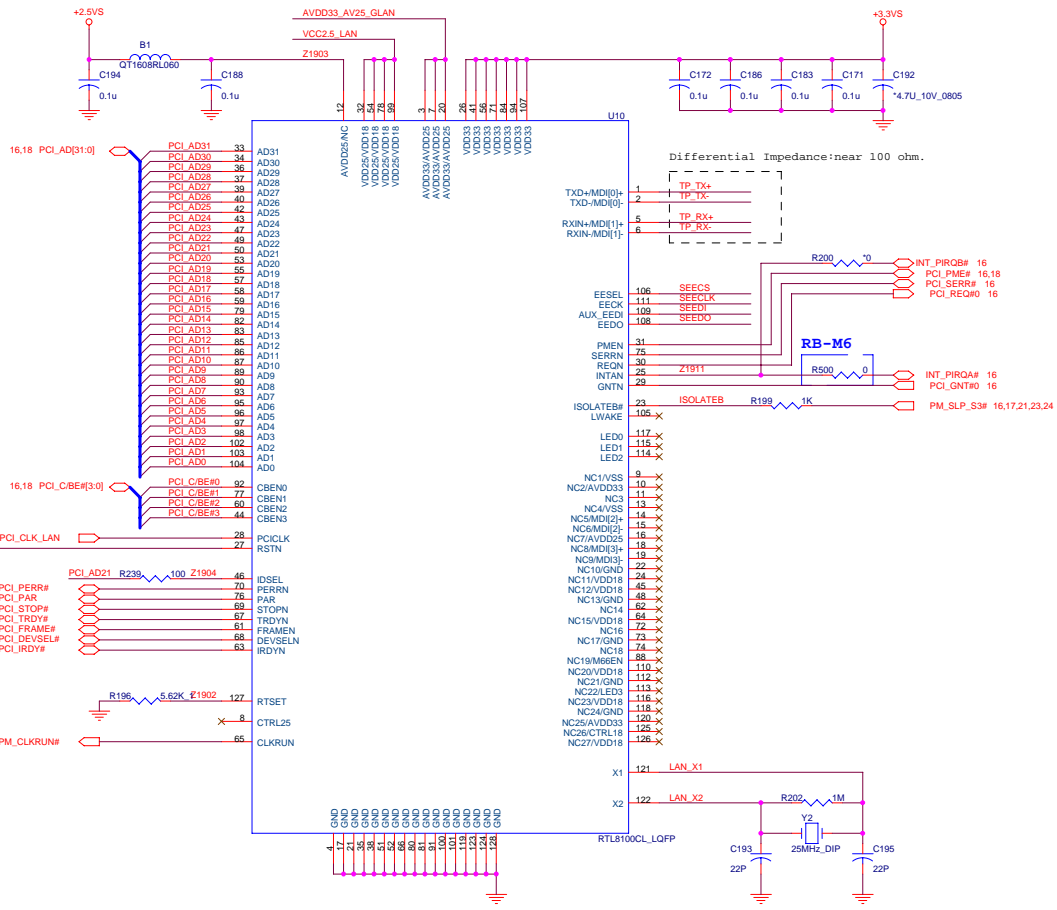
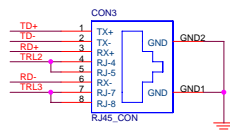
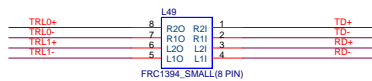
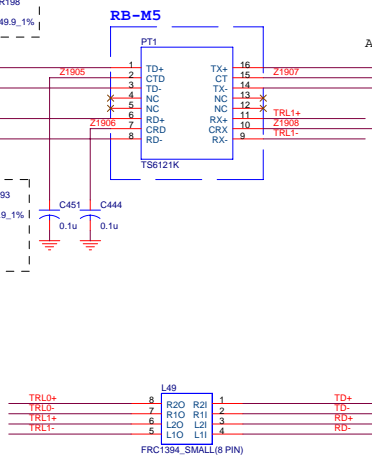
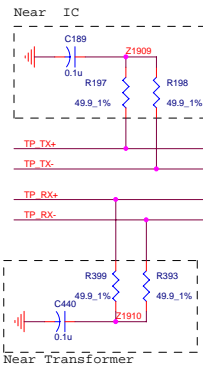
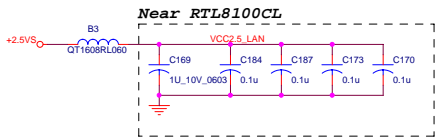
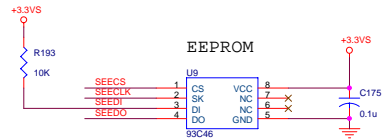
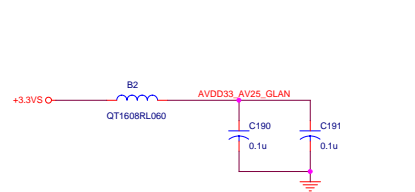
16,19 PCI_AD[31:0]
16,19 PCI_C/BE#[3:0]
7 PCI_CLK_1394_A
16,19 PCI_DEVSEL#
16,19 PCI_FRAME#
16,19 PCI_IRDY#
16,19 PCI_TRDY#
16,19 PCI_STOP#
16,19 PCI_PAR#
16,19 PCI_REQ#1
16 PCI_GNT#1
16,17,19,21,23 PCI_RST#
16 INT_PIRQC#
16,19 PCI_PME#
16,19 PM_CLKRUN#
16,17,21 INT_SERIRQ
16 INT_PIRQD#

PME#, CLKRUN, IRQSER# AND INTA#
MUST BE PULLED-UP ON THE MLB.



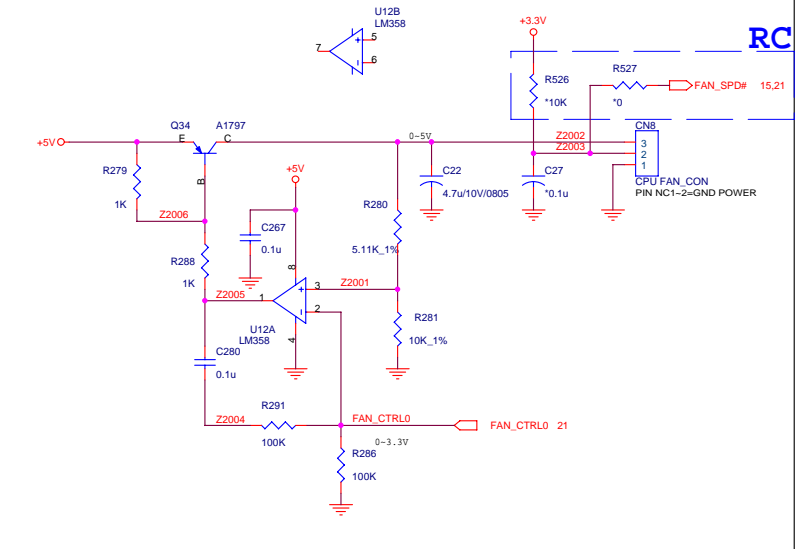
MMC(Mutimedia Card) / SD(Seure Digital Card)
MS(Memory Stick) /MS Pro

Name of Part	IEEE1394A	
Project	L50IIO	Rev B
Date: Wednesday, April 19, 2006	Sheet	18 / 33
UNIWILL COMPUTER CORP.		
3255		

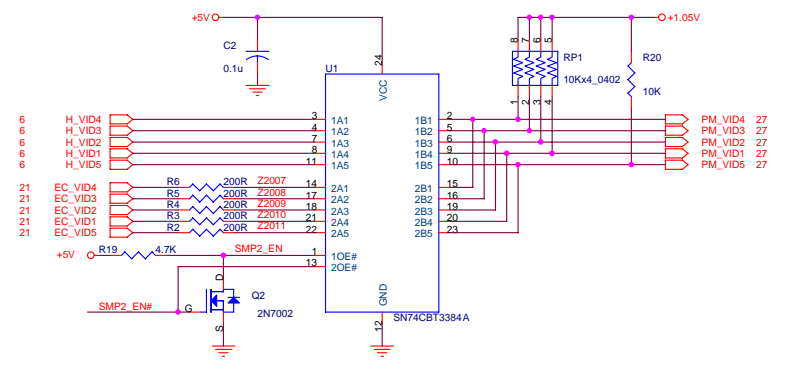


Name of Part	LAN 10/100	
Project	L50IIO	Rev B
Date:	Wednesday, April 19, 2006	Sheet 19 / 33
UNWILL COMPUTER CORP.		

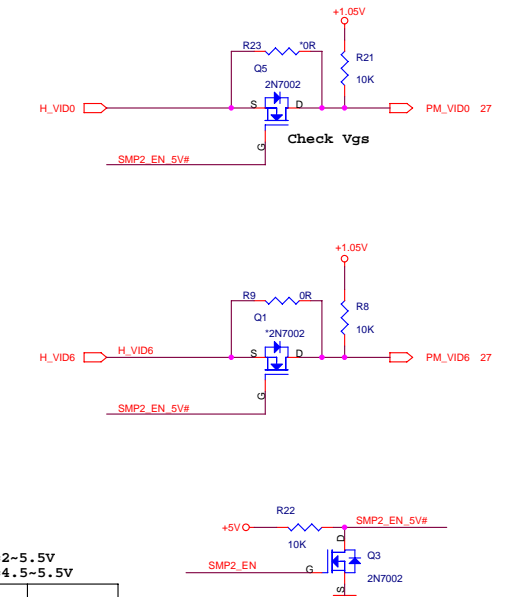
CPU FAN CONTROL



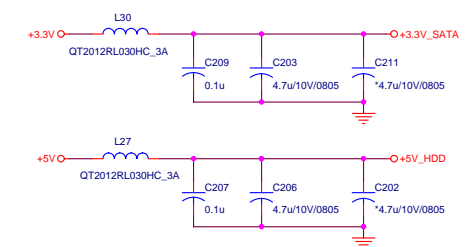
SMART POWER



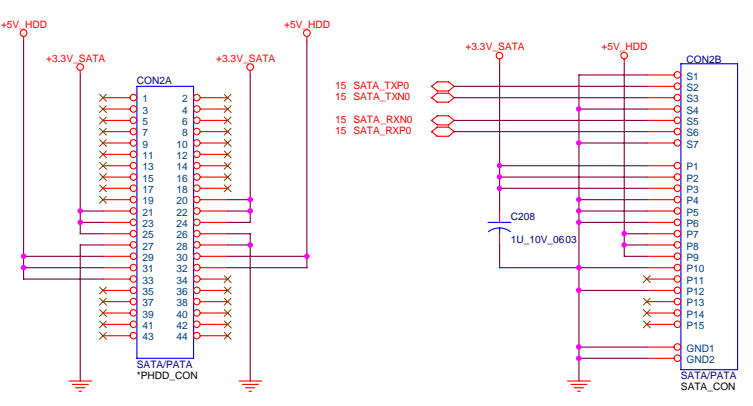
SMART POWER2



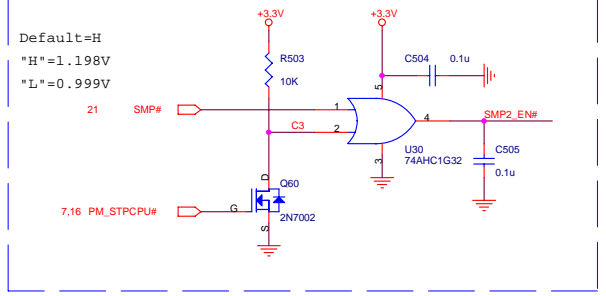
SATA HDD CONN



PATA_CONN



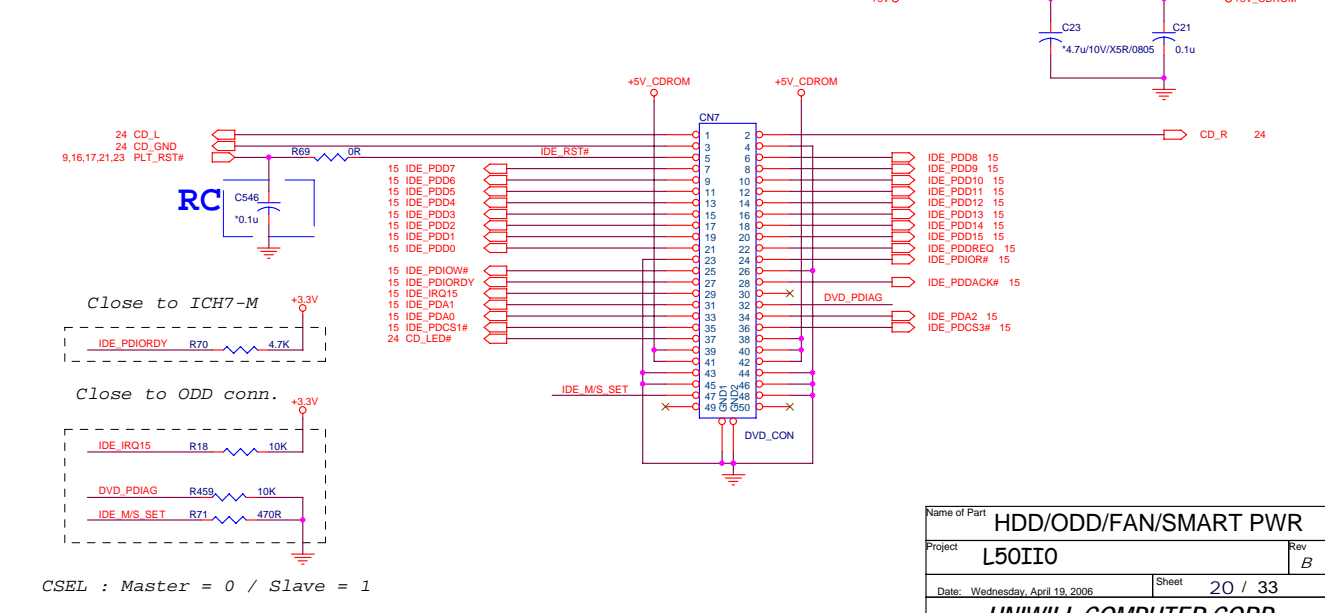
RB-M7



74AHC1G32 VCC=2-5.5V
74AHC1G32 VCC=4.5-5.5V

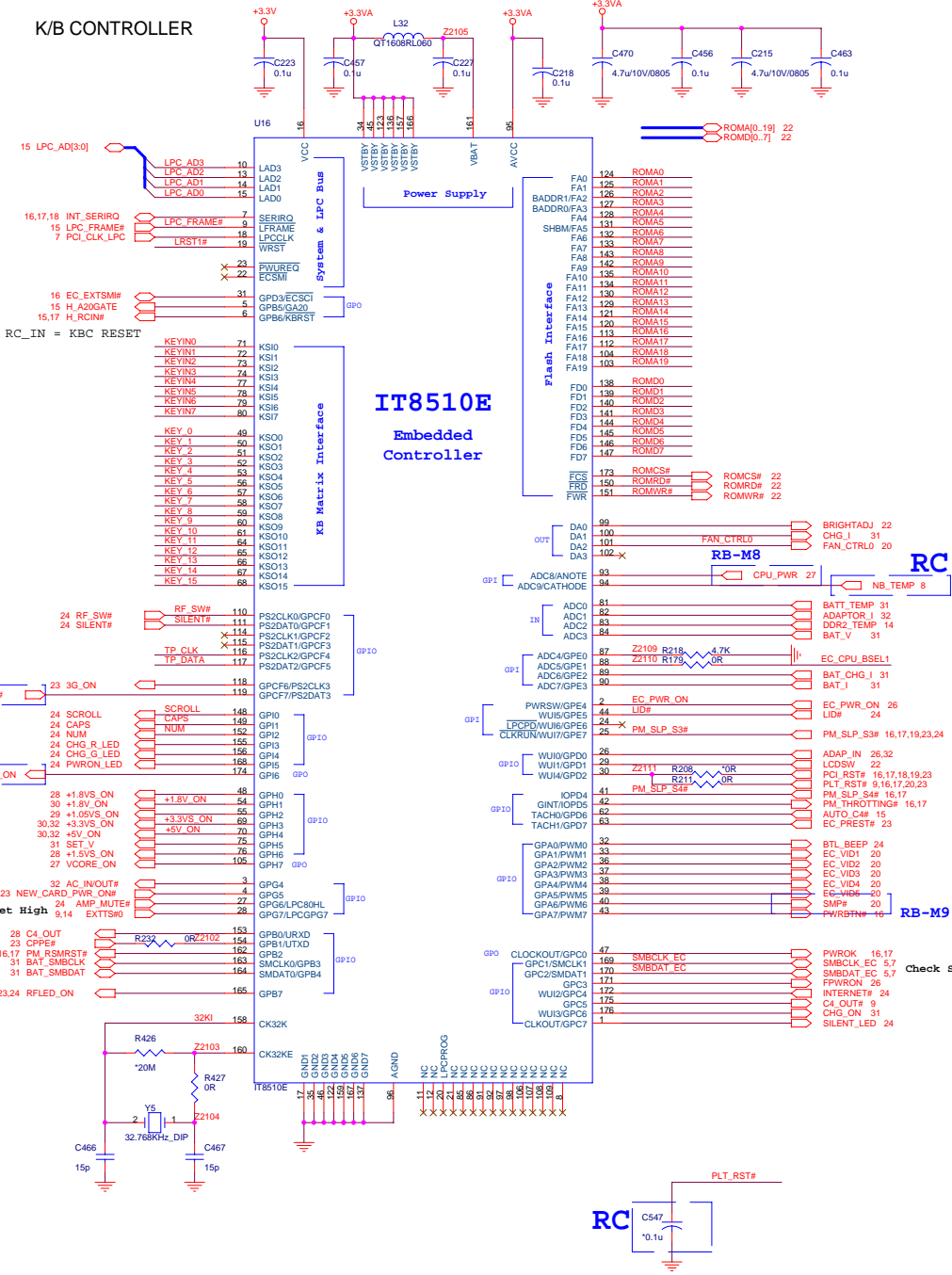
PM_STPCPU#	SMP#	SMP2_EN#
0	0	0
0	1	1
1	0	1
1	1	1

ODD CONN



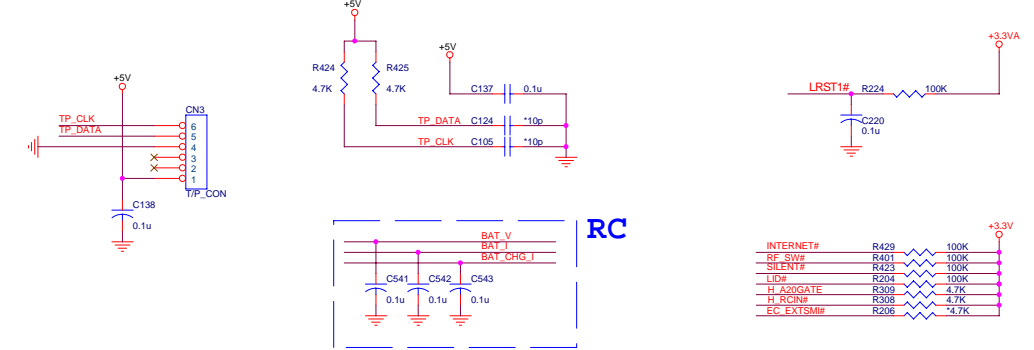
Name of Part	HDD/ODD/FAN/SMART PWR	
Project	L50IIO	Rev B
Date: Wednesday, April 19, 2006	Sheet	20 / 33
3255	UNIWILL COMPUTER CORP.	

K/B CONTROLLER



IT8510E
Embedded Controller

TOUCHPAD CONN

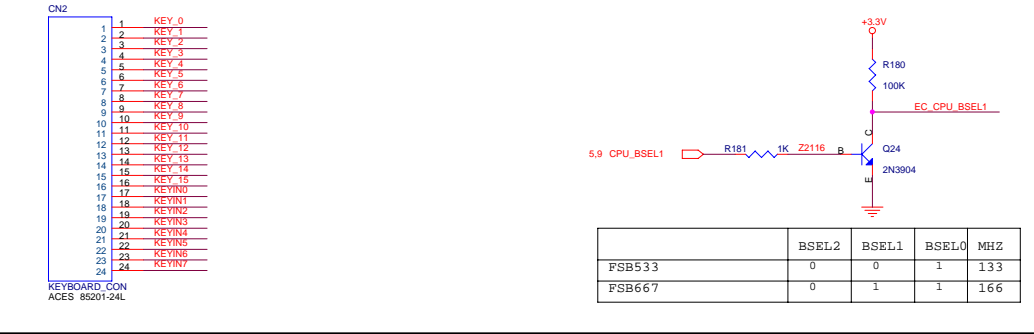


RC

EC SMBUS

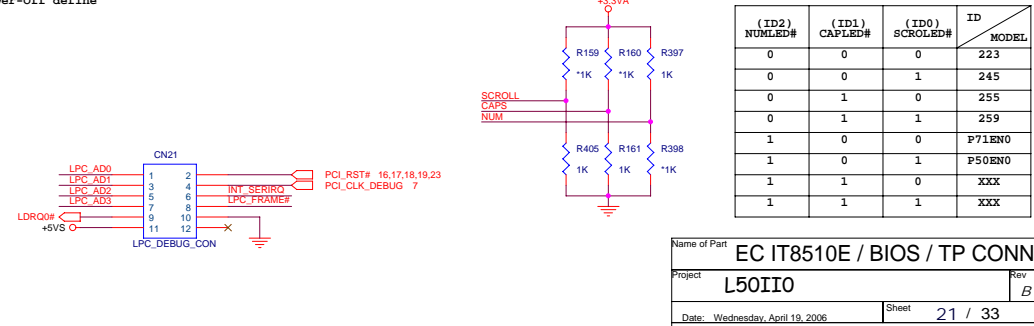


Keyboard CONN



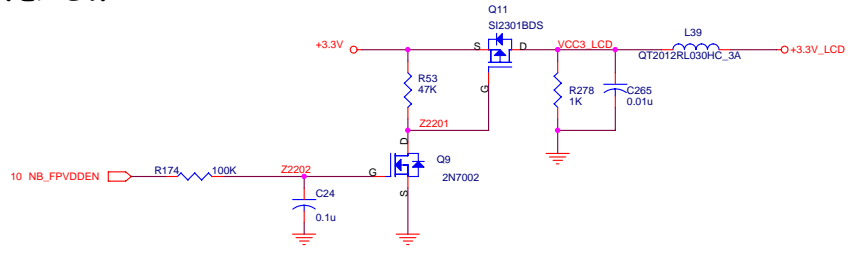
	BSEL2	BSEL1	BSEL0	MHZ
FSB533	0	0	1	1.33
FSB667	0	1	1	1.66

LPC Debug CONN



(ID2) NUMLED#	(ID1) CAPLED#	(ID0) SCROLED#	ID MODEL
0	0	0	223
0	0	1	245
0	1	0	255
0	1	1	259
1	0	0	P71EN0
1	0	1	P50EN0
1	1	0	XXX
1	1	1	XXX

LCD POWER SW

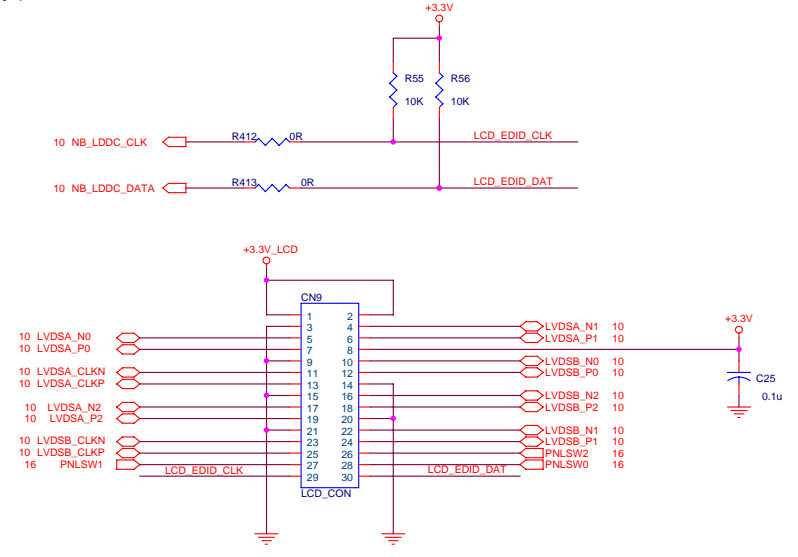


PANNEL ID SELECT

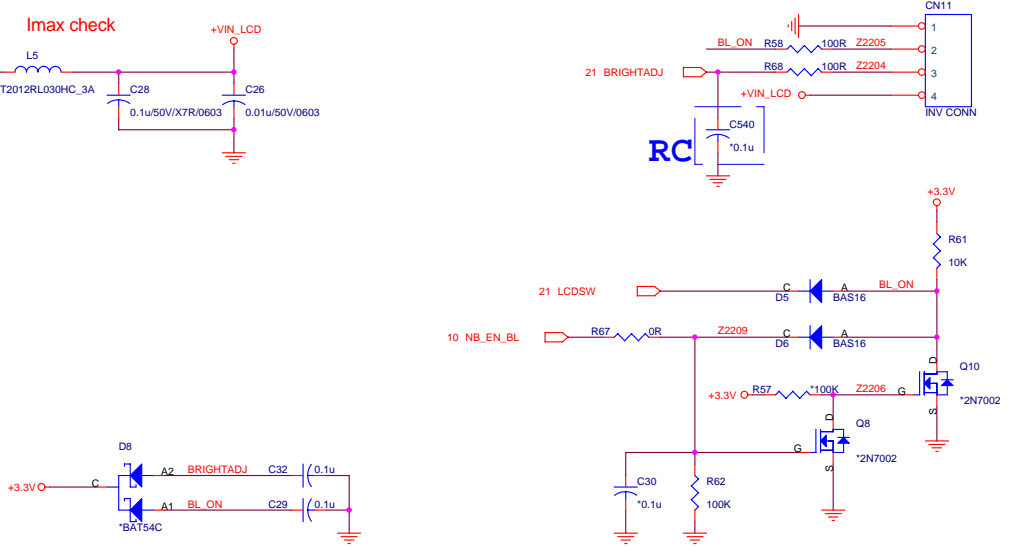


PNLSW2	PNLSW1	PNLSW0	
L	L	L	1024X768
L	L	H	1400X1050
L	H	L	1280X800
L	H	H	1280X768
H	L	L	reserved
H	L	H	1680X1050
H	H	L	1920X1200
H	H	H	1440X900

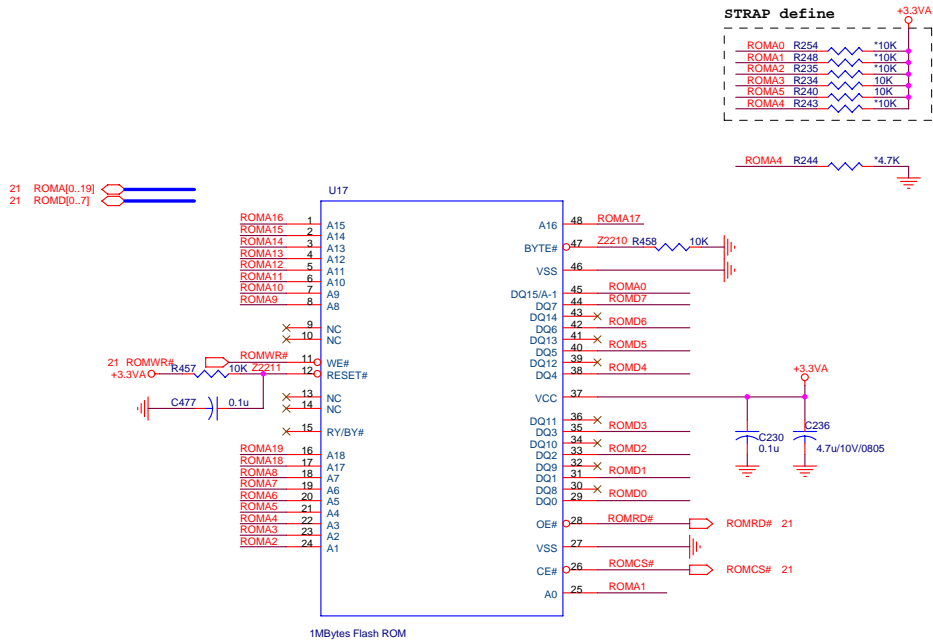
LCD CONN



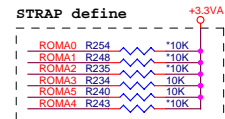
INVERTER CONN



FLASH ROM

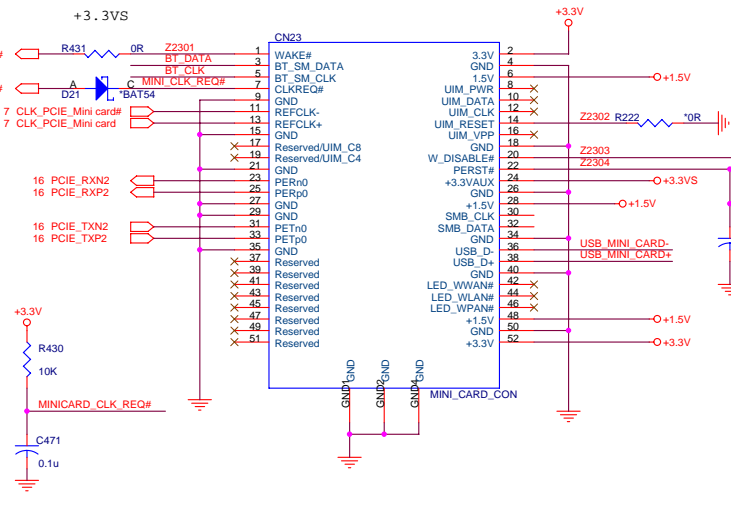
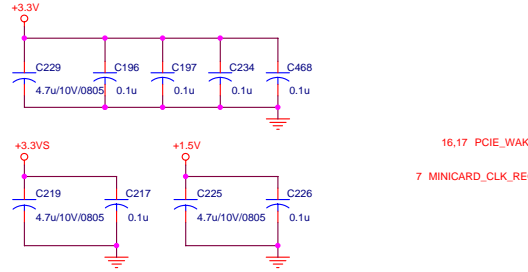


solving system power off leakage current over 2mA@10.8V issue



Name of Part ROM/INV CONN/LCD		
Project L50IIO	Rev B	
Date: Wednesday, April 19, 2006	Sheet 22 / 33	
3255 UNIWILL COMPUTER CORP.		

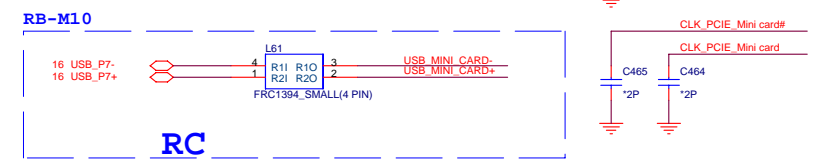
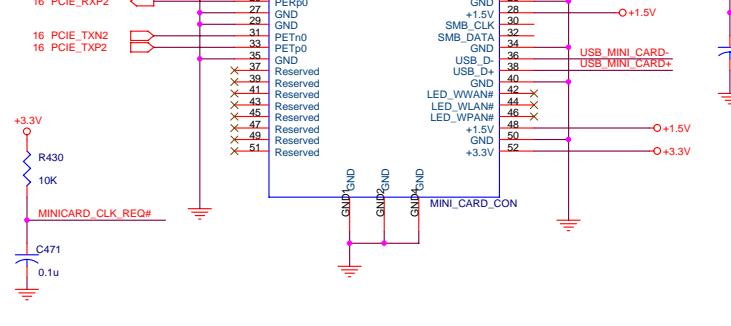
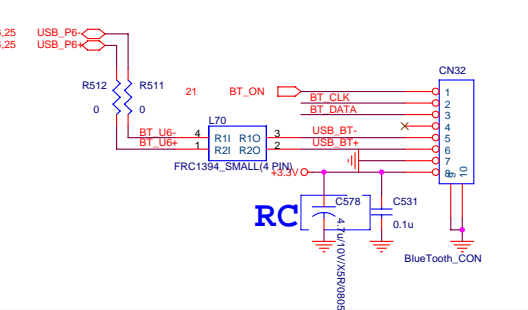
MINI CARD Socket



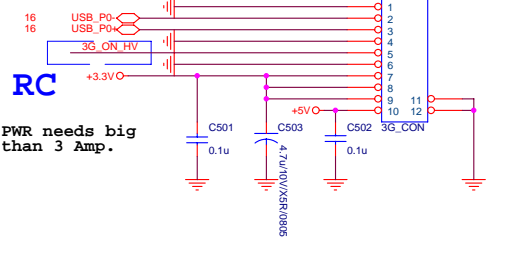
Intel PRO/Wireless 2100 LAN

PIN#	Signal	Level	Control	Associated AP
PIN11	LED_WLAN_LINK	Hi(3.3V)	Solid ON	Not Associated with an AP
		Low(0V)	LED OFF	Power OFF or RF_Kill active
PIN2	LED_WLAN_ACT	Hi(3.3V)	Rapid Blinking	Passing data traffic to AP
		Low(0V)	Slow Blinking	Beacon traffic to Ap
		Hi(3.3V)	LED OFF	Power OFF or not activity or RF_Kill active
PIN13	HW_RadioXMIT_OFF#	Hi(3.3V)	Enable	Radio transmitter is ON
		Low(0V)	Disable	Radio transmitter turn off

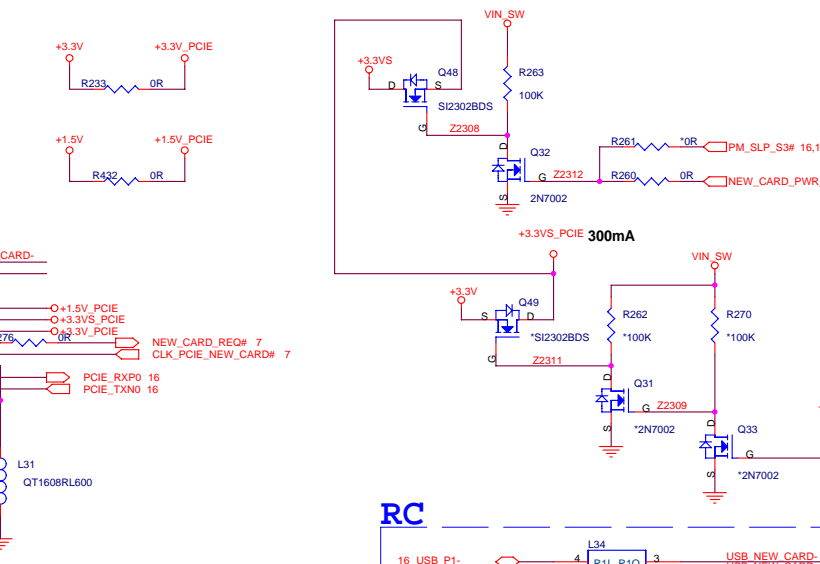
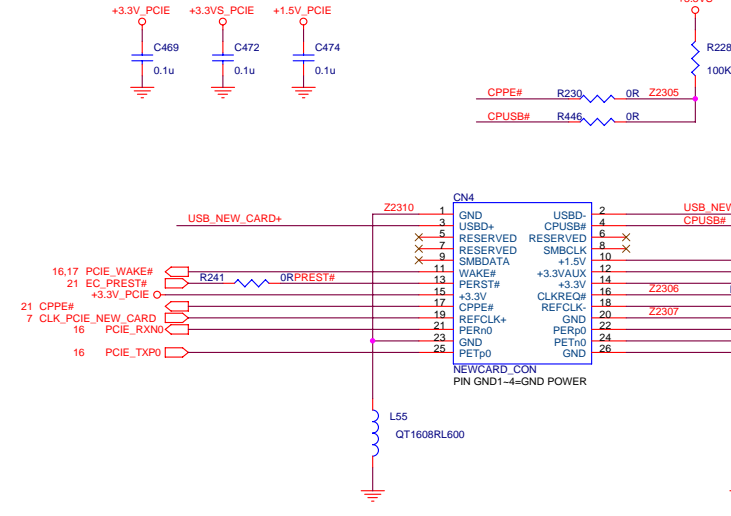
Blue Tooh



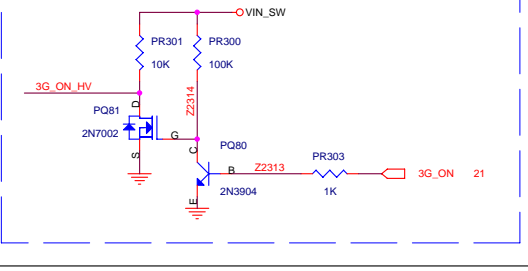
3G Module



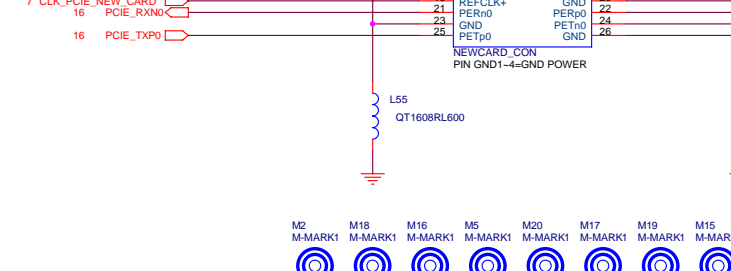
NEW CARD Socket



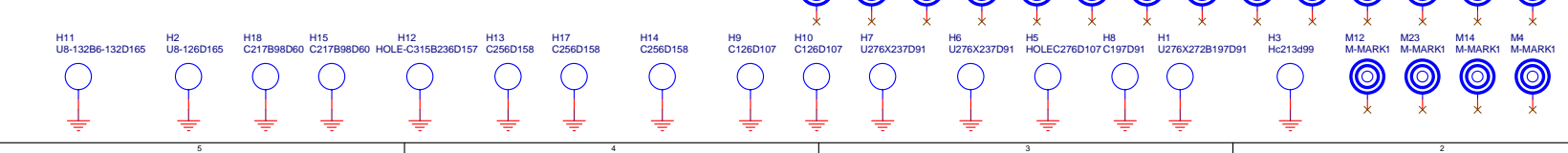
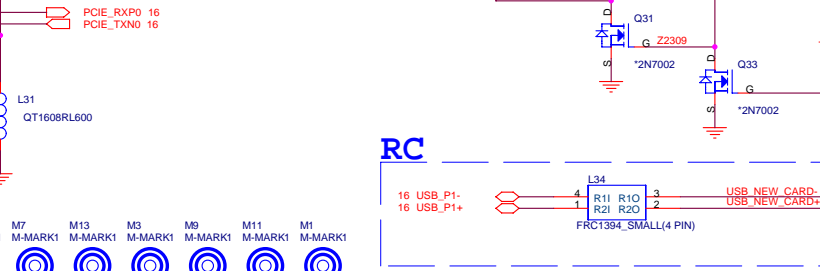
RC



RC

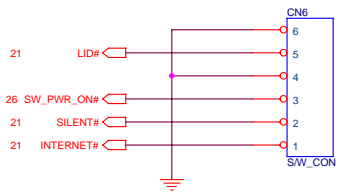


RC

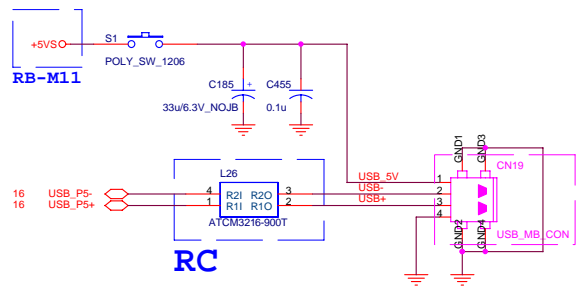


Name of Part	MINI CARD / NEW CARD / 3G / BT	
Project	L50IIO	Rev B
Date:	Wednesday, April 19, 2006	Sheet 23 / 33
UNIWILL COMPUTER CORP.		
3255		

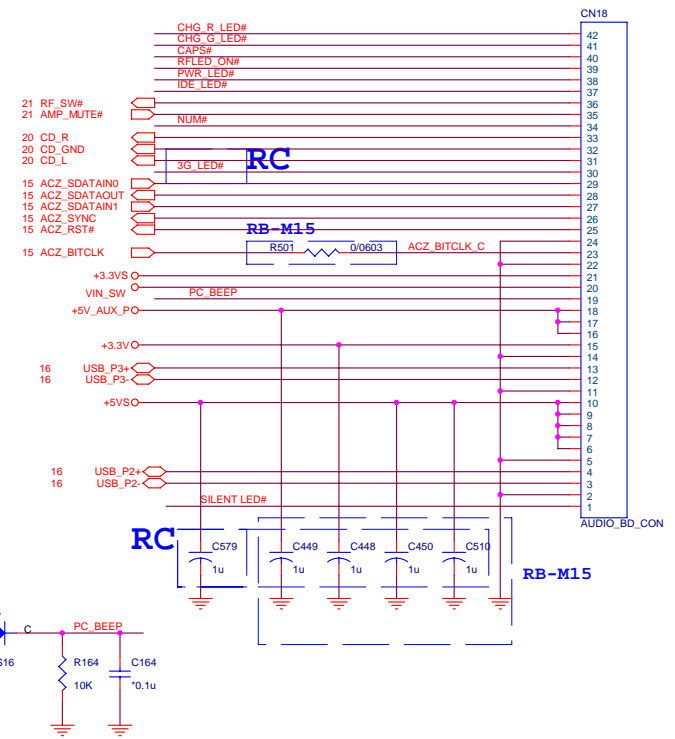
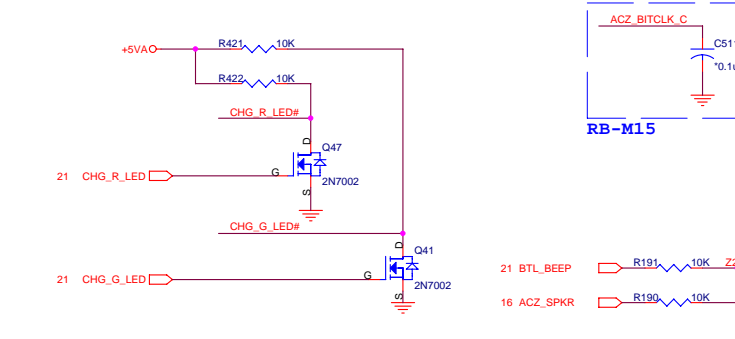
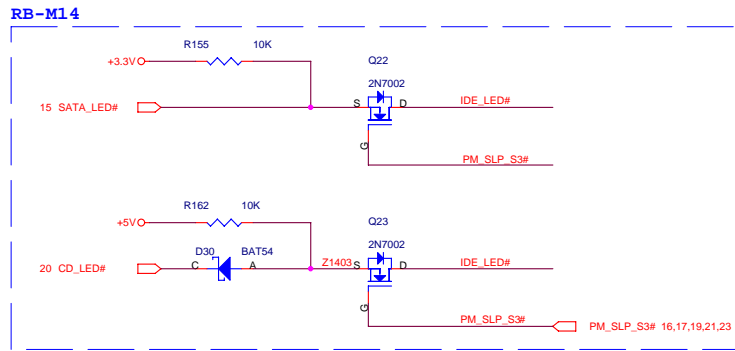
SWITCH BD CONN



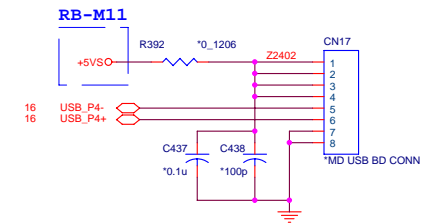
ON BOARD USB



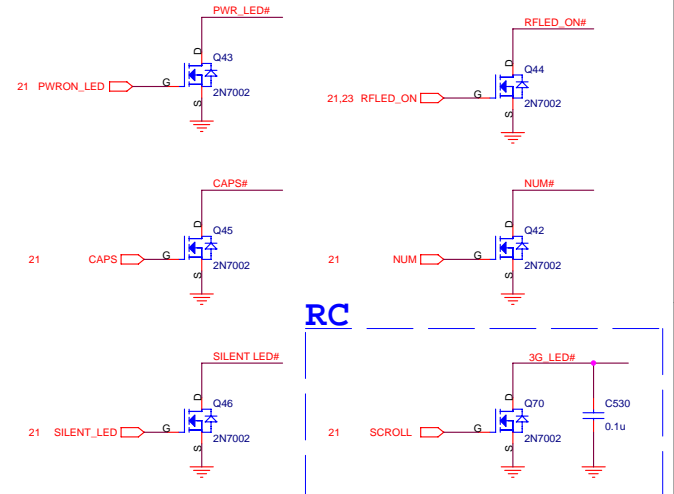
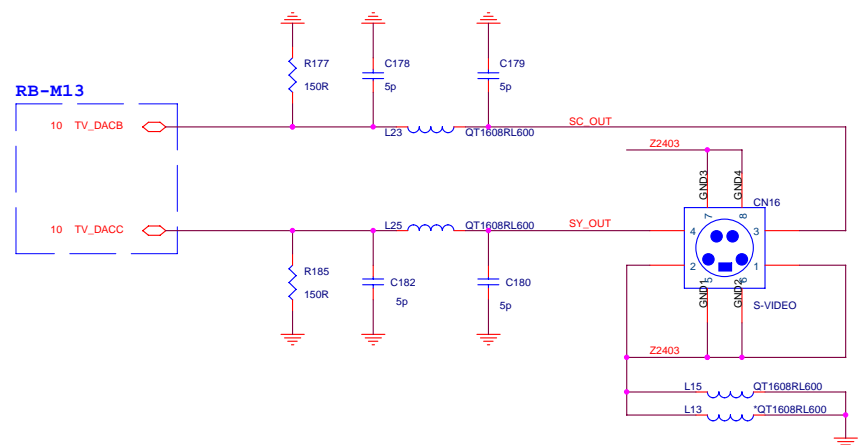
AUDIO & LED BD CONN



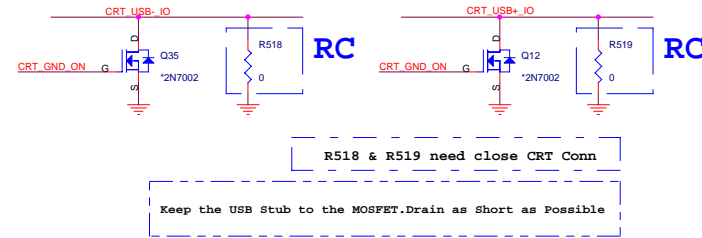
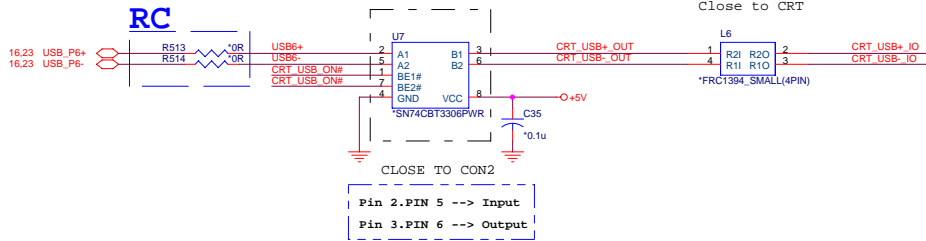
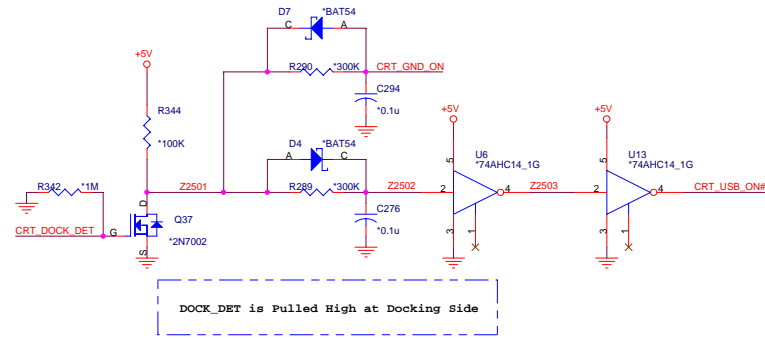
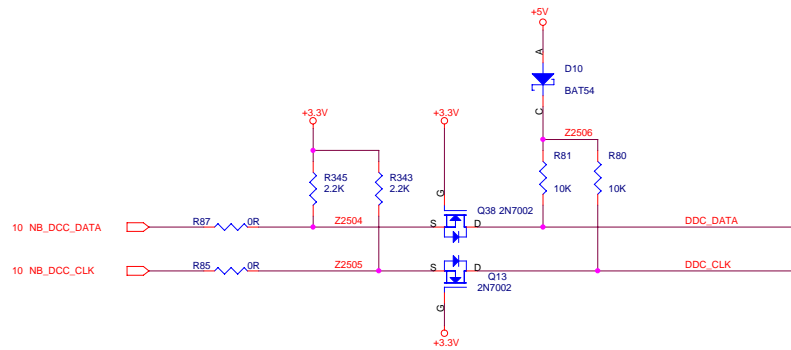
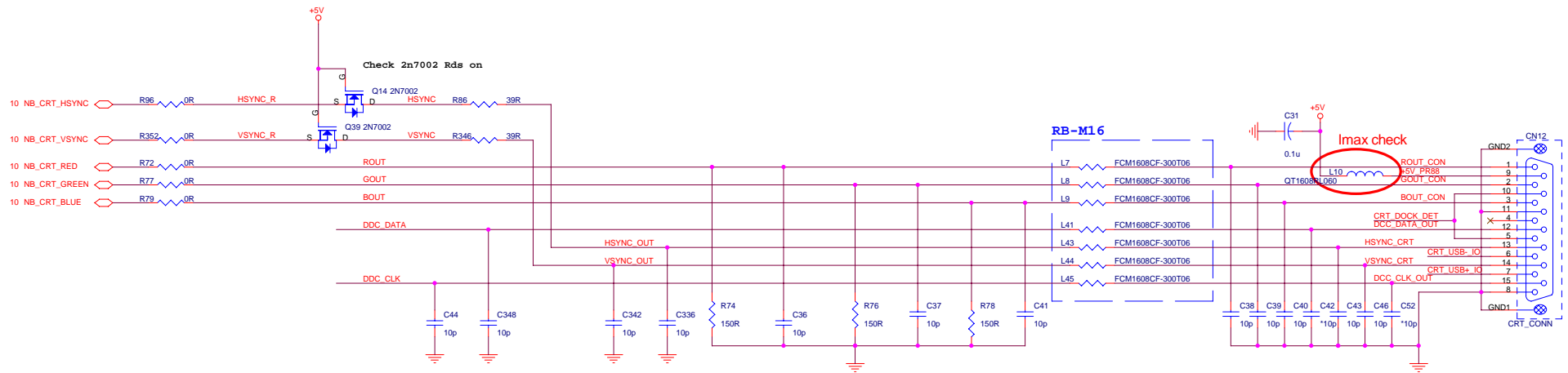
MDC BD's USB Conn



S-Vedio CONN

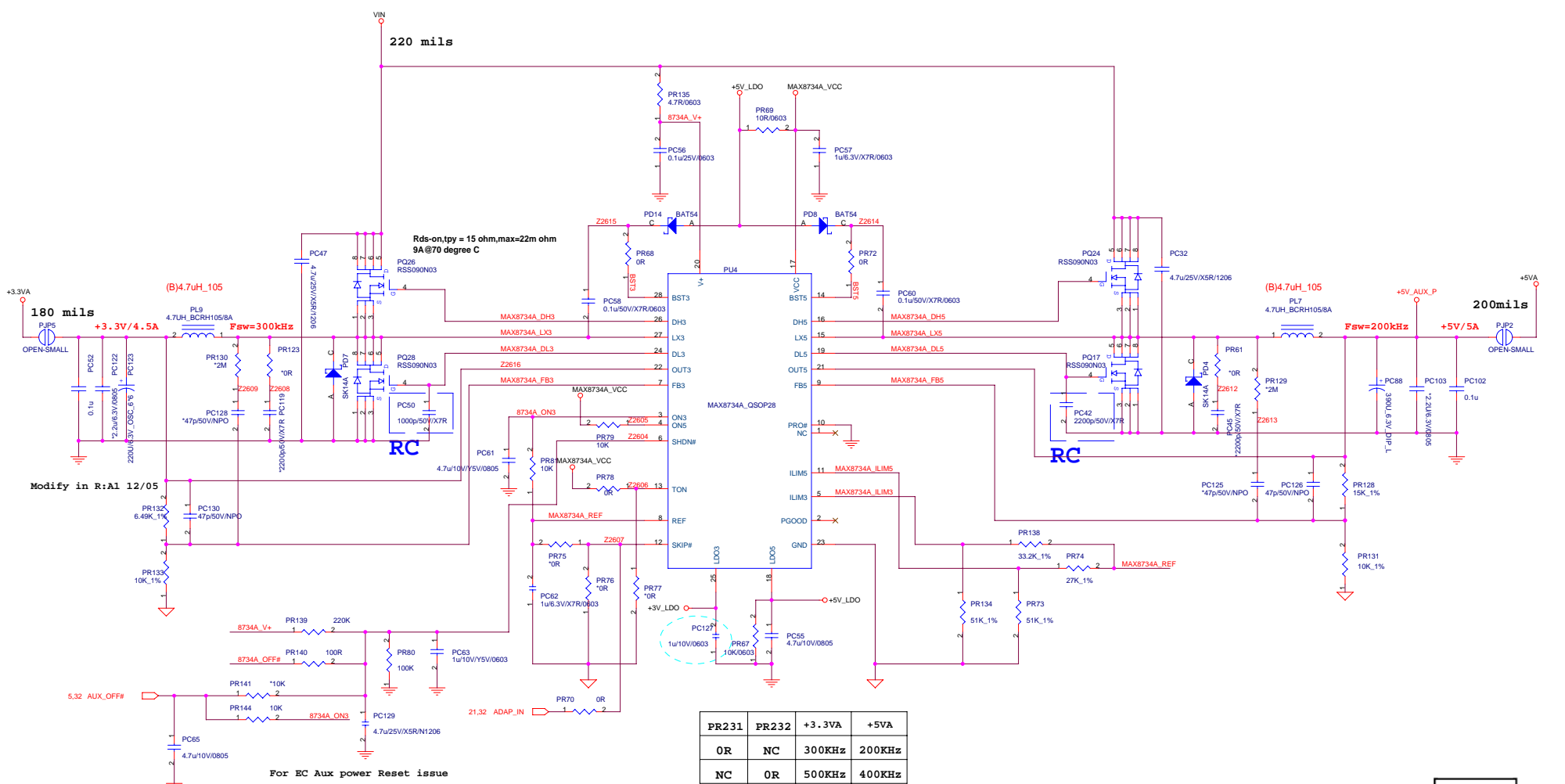


Name of Part		
Daughter BD CONN		
Project	L50II0	Rev B
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3255 UNIWILL COMPUTER CORP.		



TC Modify 0914

Name of Part		Card Reader	
Project	L50IIO	Rev	B
Date:	Thursday, April 20, 2006	Sheet	25 / 33
3255	UNIWILL COMPUTER CORP.		

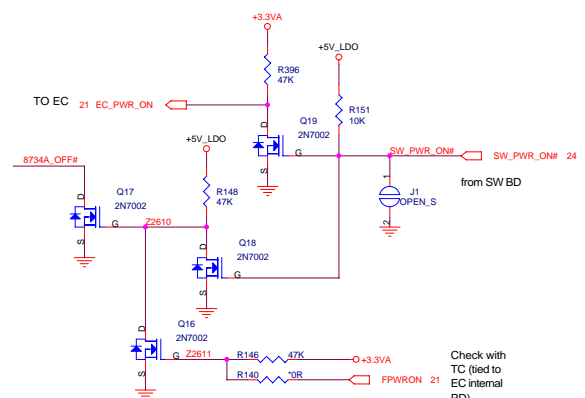


Rds-on, t_{py} = 15 ohm,max=22m ohm
9A@70 degree C

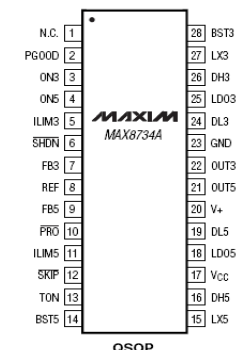
Modify in R:A1 12/05

For EC Aux power Reset issue

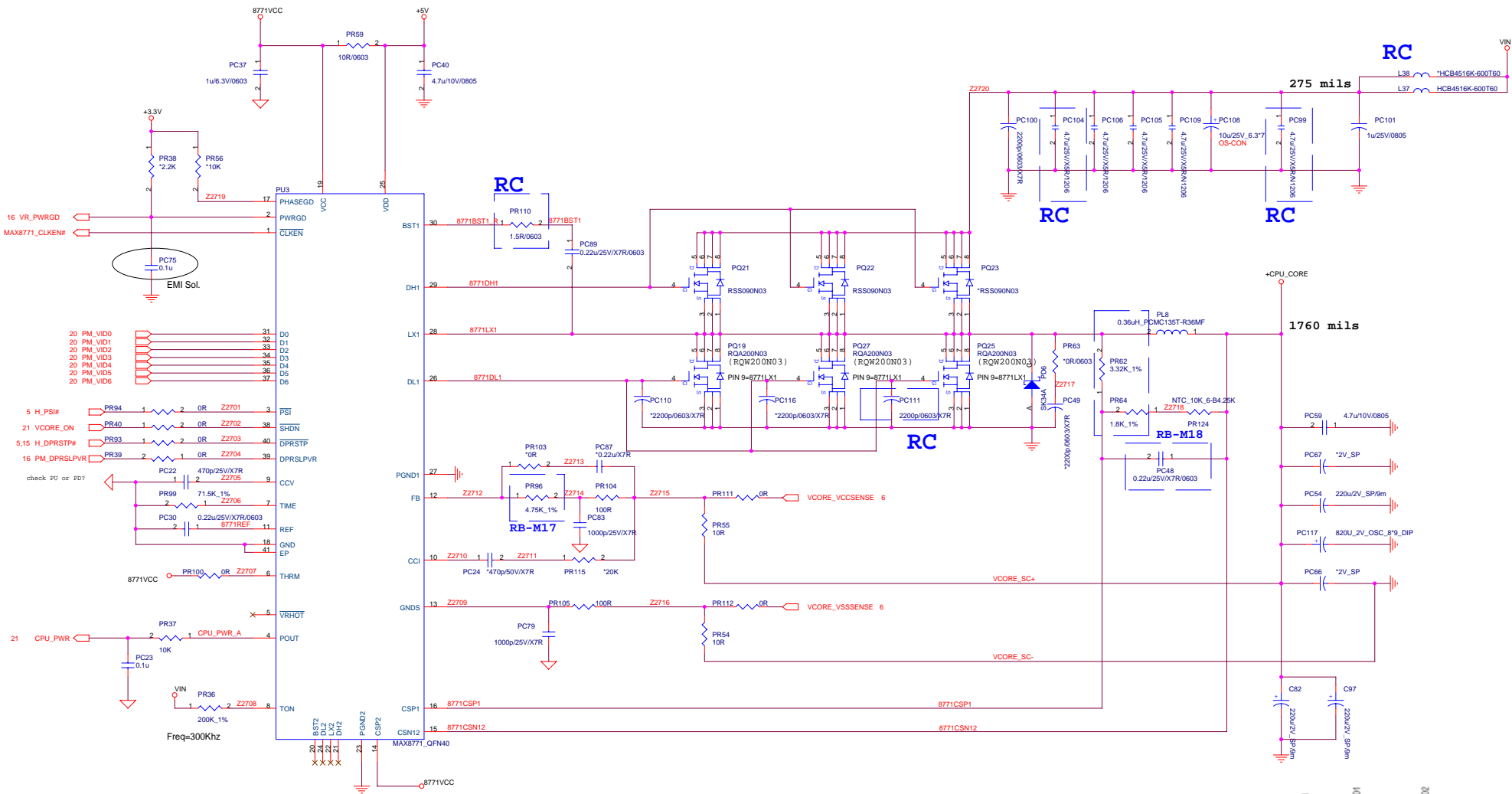
PR231	PR232	+3.3VA	+5VA
OR	NC	300KHz	200KHz
NC	OR	500KHz	400KHz



PL9, PL6--->4.7uH_105
PR163, PR165, PR55=>51K_1%
PR56=>39.2K_1%



Name of Part	+5V&+3V(MAX8734A)	
Project	L50IIO	Rev B
Date:	Thursday, April 20, 2006	Sheet 26 / 33
UNIWILL COMPUTER CORP.		

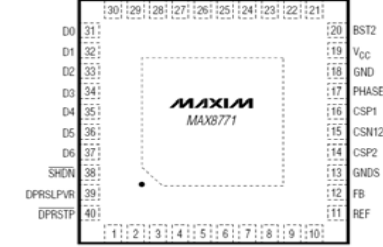


1. check PSI#&DPRSTP#&DPRSLPVR PU or PD?
2. what CAP or R need use 0603?
3. CPU vcc-sense & vss-sense?
4. Input CAP enough?
5. thermal func. disable.NC?
6. DGND and AGND problem?
7. check CHOKE footprint and hight with ME?
8. BST func.?
9. TON pull high to Vin or 5V?

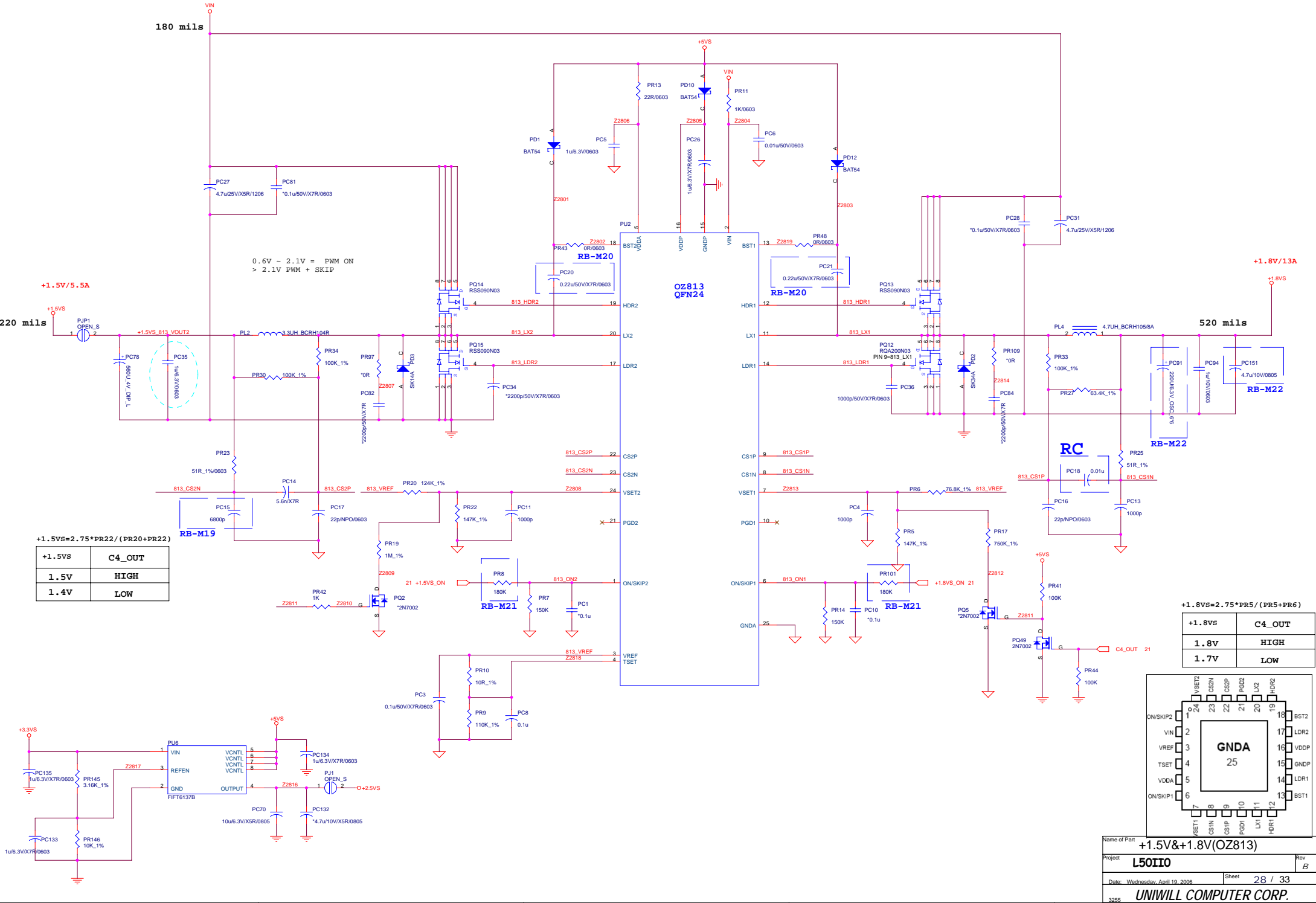
VID TABLE

6	5	4	3	2	1	0	Vcore	Status
0	0	1	0	0	0	1	1.2875	Yonah(HFM)
0	0	1	1	0	0	0	1.2000	Boot Vout
0	0	1	1	1	0	0	1.1500	Merom(HFM)
0	1	1	0	1	0	1	0.8375	Y&M(LFM)
0	1	1	1	0	1	1	0.7625	Y&M(Deeper Sleep)
1	1	1	1	1	1	1	0.0000	Shut down

TOP VIEW



Name of Part	+CPU CORE(MAX8771)	
Project	L50110	Rev B
Date:	Thursday, April 20, 2006	Sheet 27 / 33
UNWILL COMPUTER CORP.		



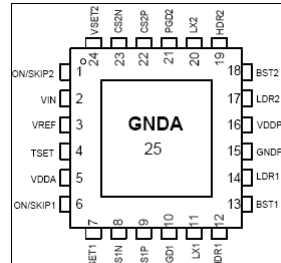
0.6V - 2.1V = PWM ON
 > 2.1V PWM + SKIP

$+1.5VS = 2.75 * PR22 / (PR20 + PR22)$

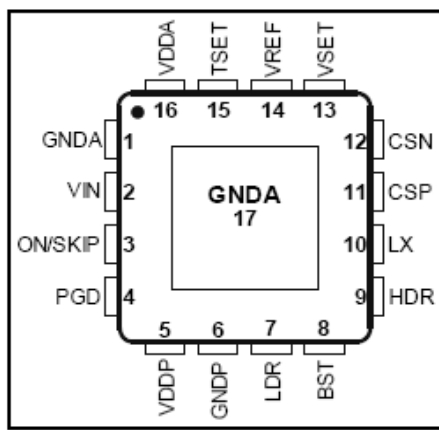
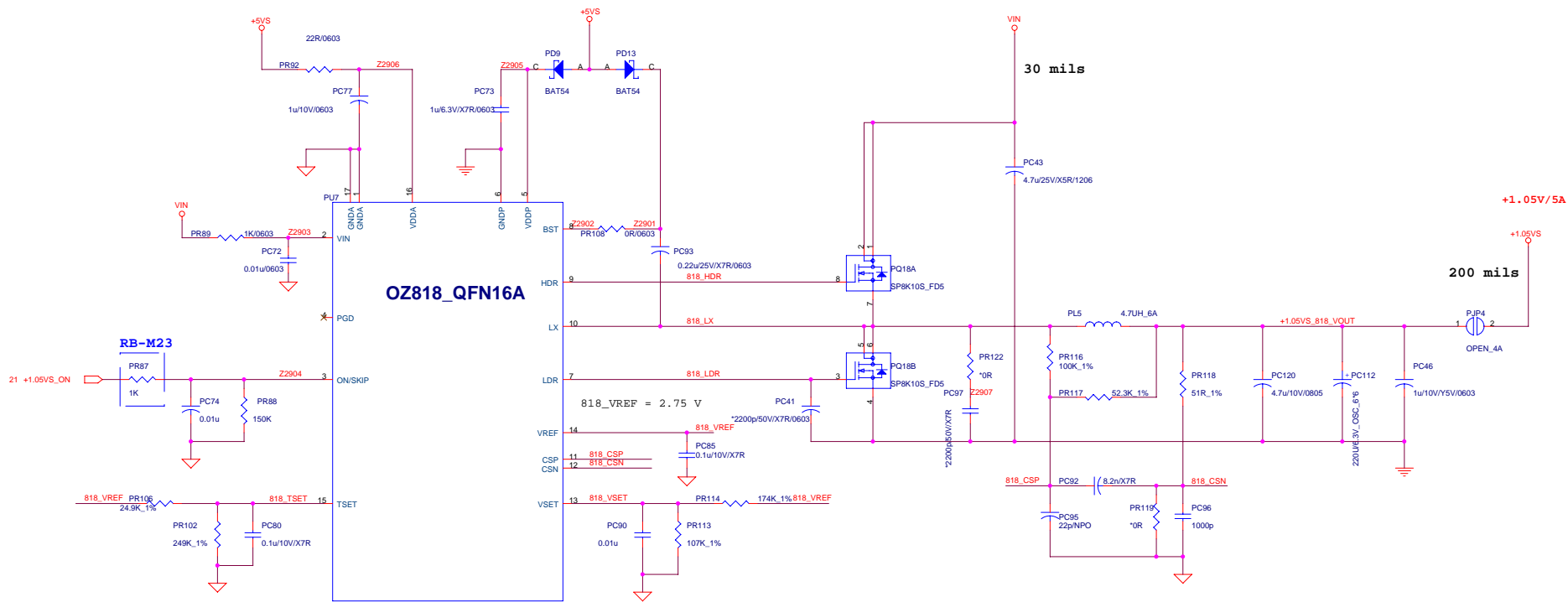
+1.5VS	C4_OUT
1.5V	HIGH
1.4V	LOW

$+1.8VS = 2.75 * PR5 / (PR5 + PR6)$

+1.8VS	C4_OUT
1.8V	HIGH
1.7V	LOW

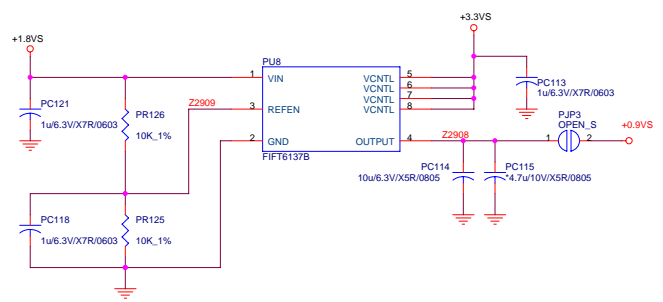


Name of Part	+1.5V/+1.8V(OZ813)	
Project	L50110	Rev B
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UNIWILL COMPUTER CORP.		



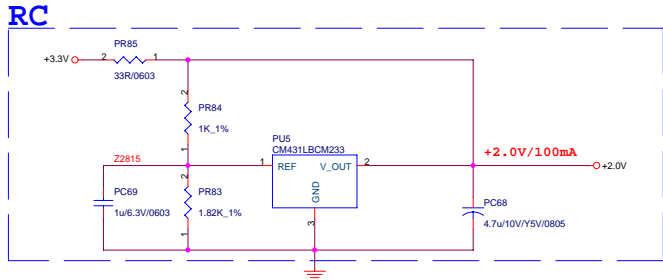
Name of Part	+0.9VS/+1.05V(OZ818)	
Project	L50110	Rev B
Date:	Thursday, April 20, 2006	Sheet 29 / 33
UNIWILL COMPUTER CORP.		

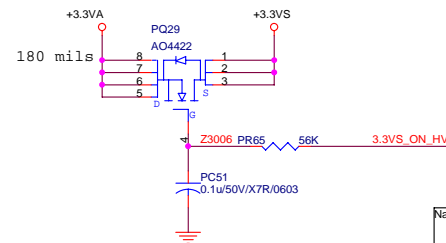
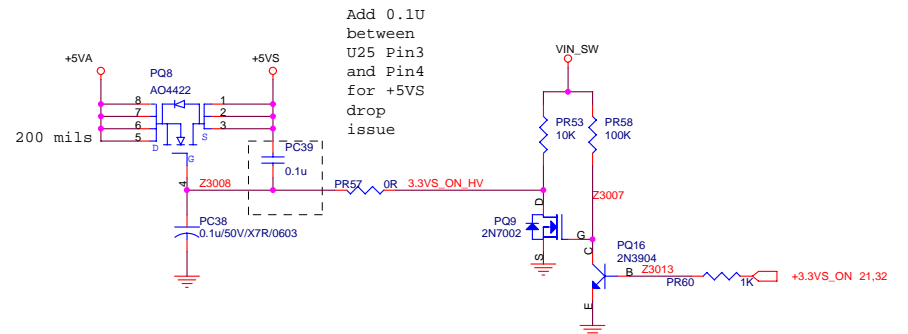
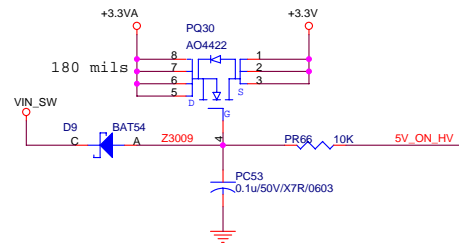
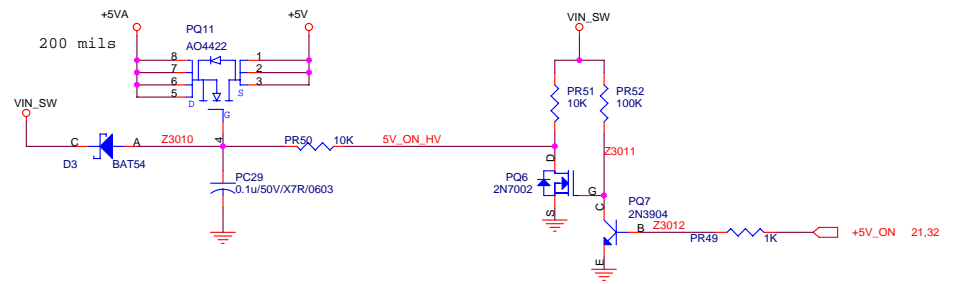
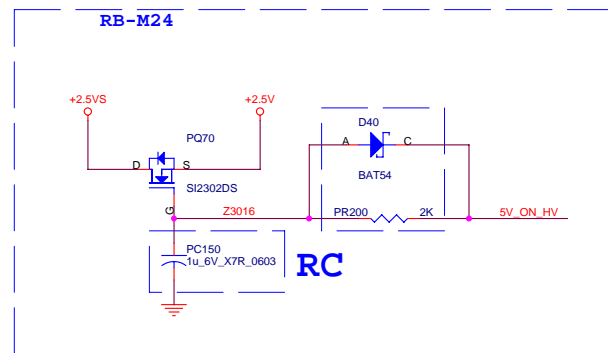
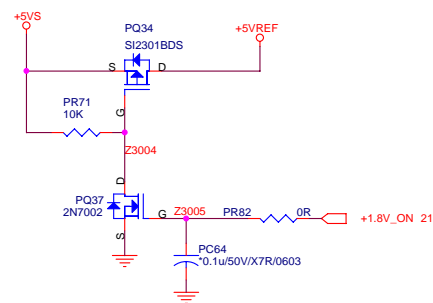
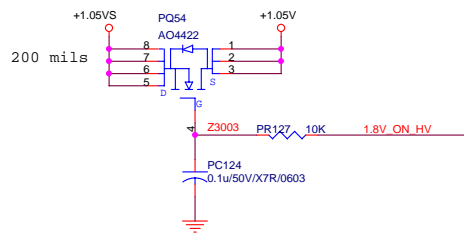
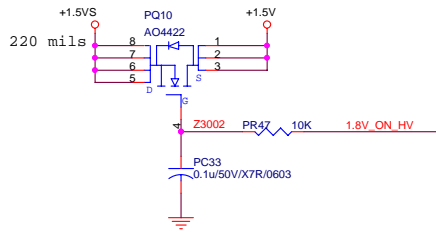
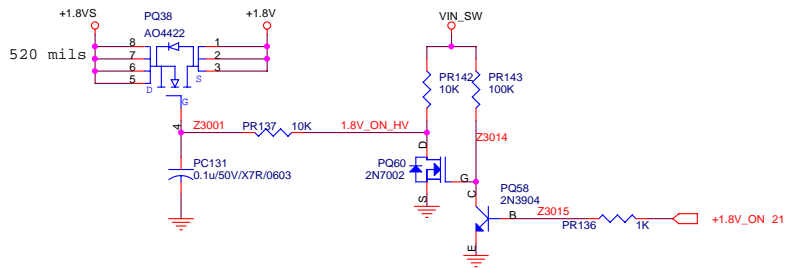
DDR2 Termination Power



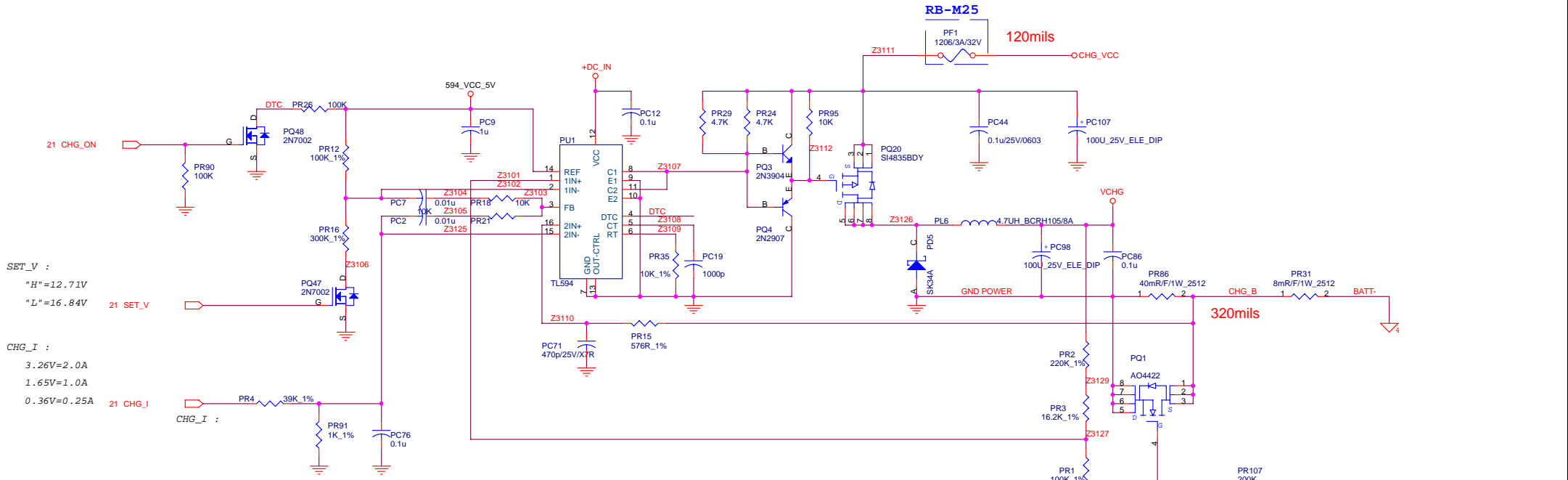
For 1394 core power

Vout	PR84	PR83
1.8V	1.2K	2.7K
1.9V	1K	1.9K
1.93V	1K	1.82K
2.0V	1K	1.6K



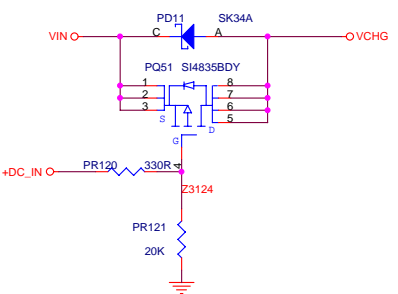


Name of Part		VCC SW/Discharger	
Project	L50IIO	Rev	B
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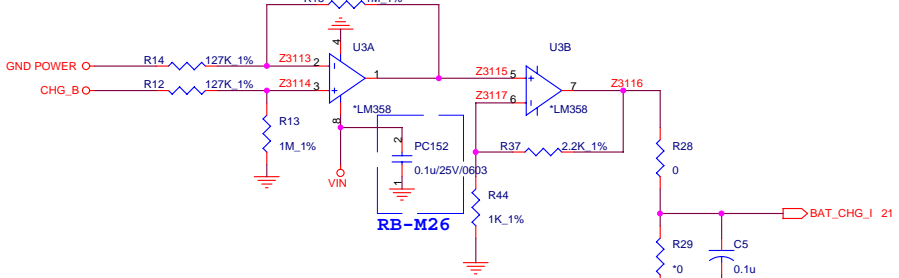


SET_V :
 "H"=12.71V
 "L"=16.84V

CHG_I :
 3.26V=2.0A
 1.65V=1.0A
 0.36V=0.25A

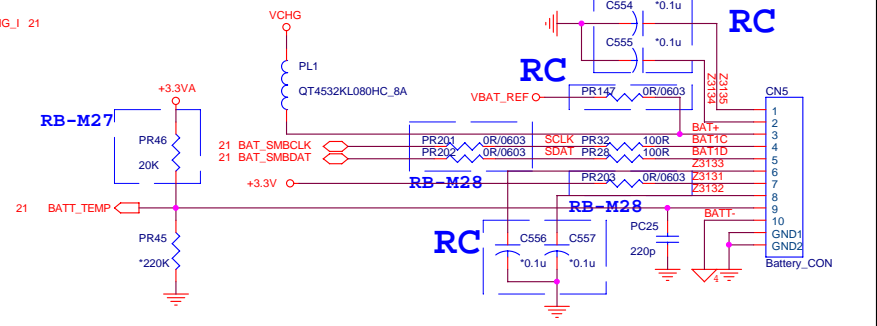
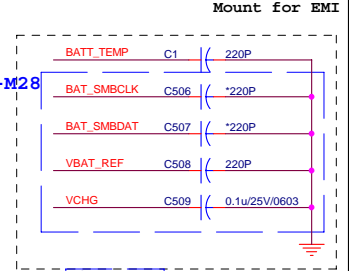
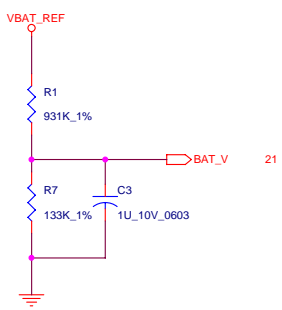


Charge Detect

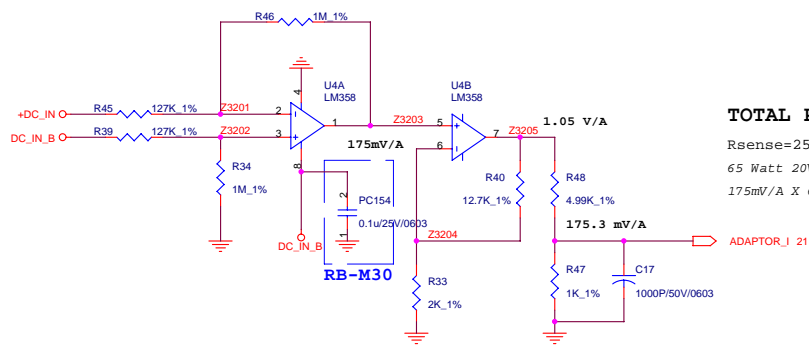
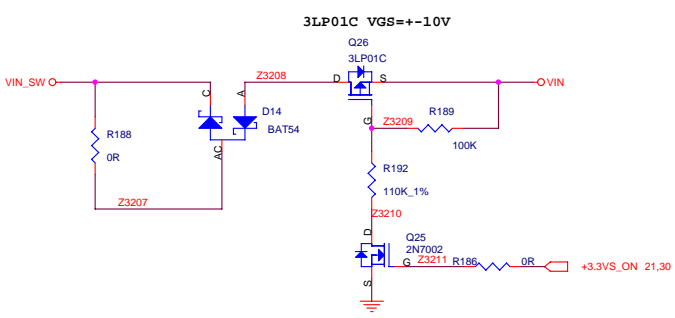
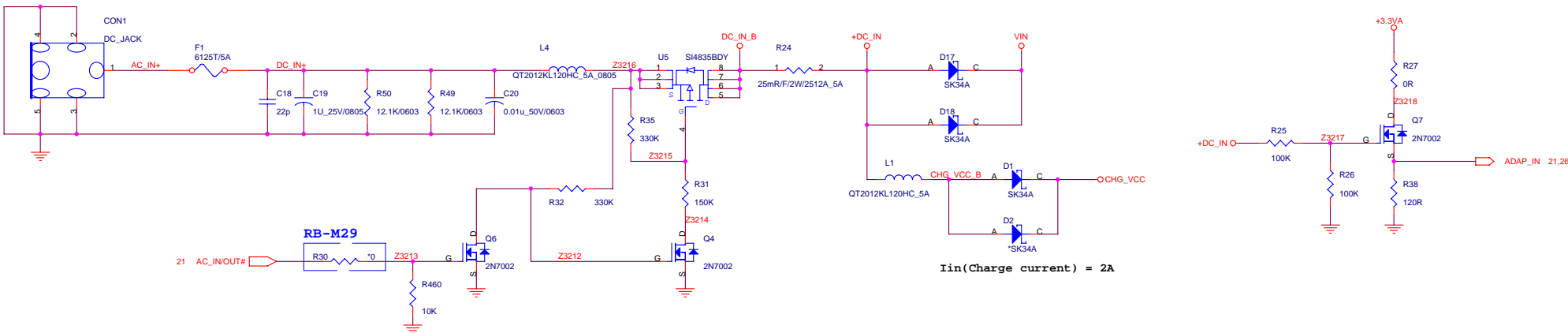
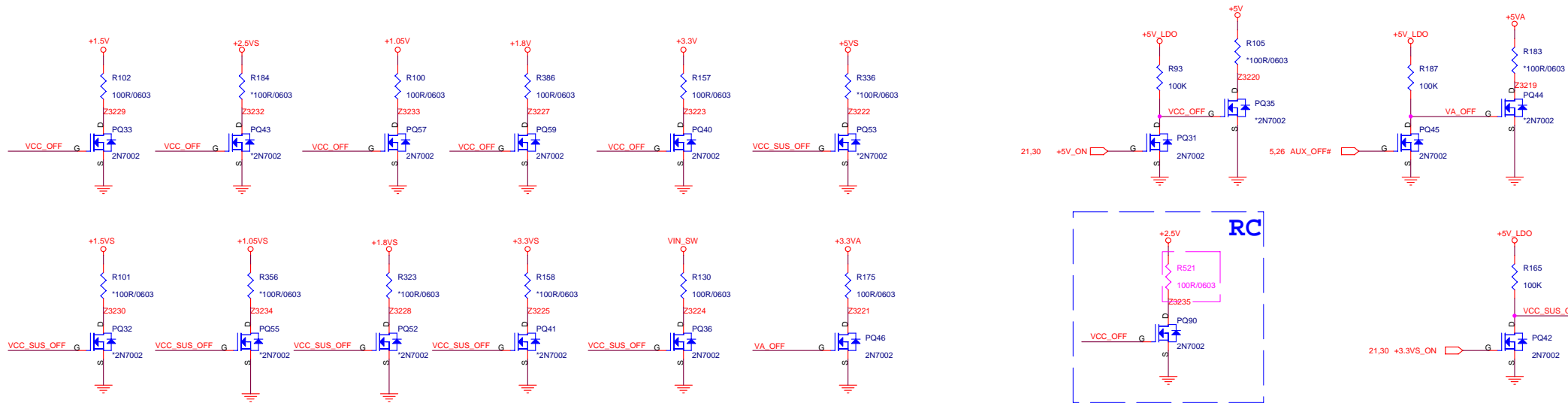


Discharge Detect

Battery Voltage Detect



Name of Part		BATT IN / Charger	
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TOTAL POWER
 Rsense=25m ohm
 65 Watt 20V/3.25A , 25mV/A X 7 = 175 mV/A ,
 175mV/A X 6 = 1.05 V/A , 1.05 V/A / 5.99 = 175.3 mV/A.

Name of Part		DC IN/DISCHARGE
Project	L50IIO	Rev B
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RA to RB change list:

- Page 7,M1->change net name for LAN clock.
- Page 9,M2->Add cap. for EMI solution.
- Page 15,M3->Change R329 to 47 ohm for EMI solution.
- Page 18,M4->Del bead to GND for ESD solution.
- Page 19,M5->Change transformer for LAN function.
- Page 19,M6->Add R500 for IRQA or IRQB selection.
- Page 20,M7->Add circuit for SMP.
- Page 21,M8->Add CPU_PWR pin to EC for CPU vlotage detection function.
- Page 21,M9->Change pin name for SMP.
- Page 23,M10->Add USB signal for mini_card.
- Page 24,M11->Change USB port power source.
- Page 24,M12->Reserve common choke for EMI test.
- Page 24,M13->Change TV signal for right design.
- Page 24,M14->Change HDD LED circuit for flash function.
- Page 24,M15->Add cap. and resister for EMI solution.
- Page 25,M16->Change CRT signal bead for signal quality.
- Page 27,M17->Addjust CPU PWR load line.
- Page 27,M18->Addjust CPU PWR OCP point.
- Page 28,M19->Change PC15 to 6800pf for vset2 ccuracy.
- Page 28,M20->Change cap. from 0.1uf to 0.22uf for LX accuracy.
- Page 28,M21->Disable skip mode.
- Page 28,M22->Add PC151 and change PC91 to solve PWR ripple over spec. issue.
- Page 29,M23->Change PR87 to 1K ohm for skip mode function.
- Page 30,M24->Add PQ70 for +2.5VS and +2.5V switch.
- Page 31,M25->Change PF1 type to 1A/32V.
- Page 31,M26->Add cap. for OP input power.
- Page 31,M27->Change PR46 to 20K ohm for bat temp.
- Page 31,M28->Add Res. for EMI solution.
- Page 32,M29->Disable AC IN / OUT function.
- Page 32,M30->Add cap. for OP input power.
- Page 15,M31->Add cap. for EMI solution.

Name of Part		Every Ver. Histor	
Project	L50II0	Rev	B
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