

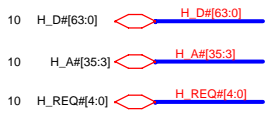
Rocky 40/50 Schematic Index

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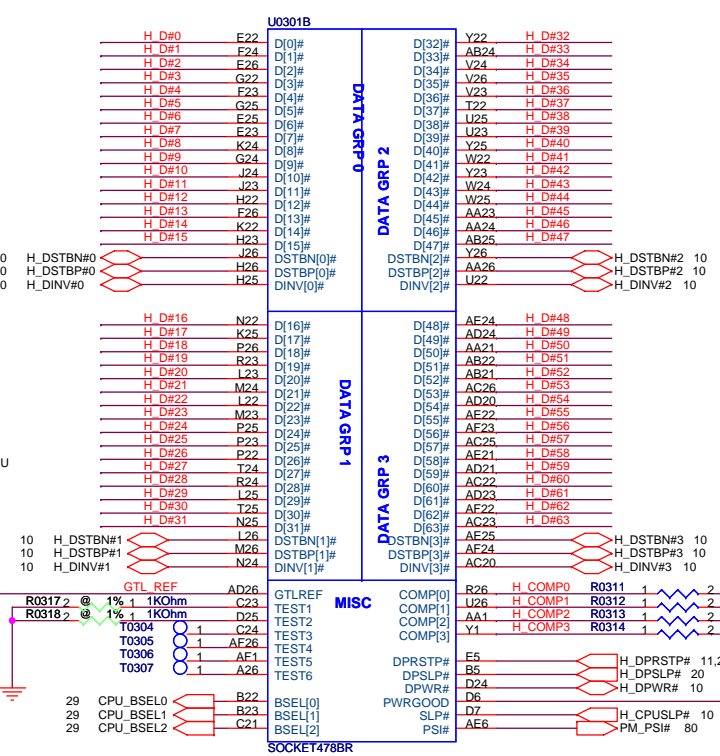
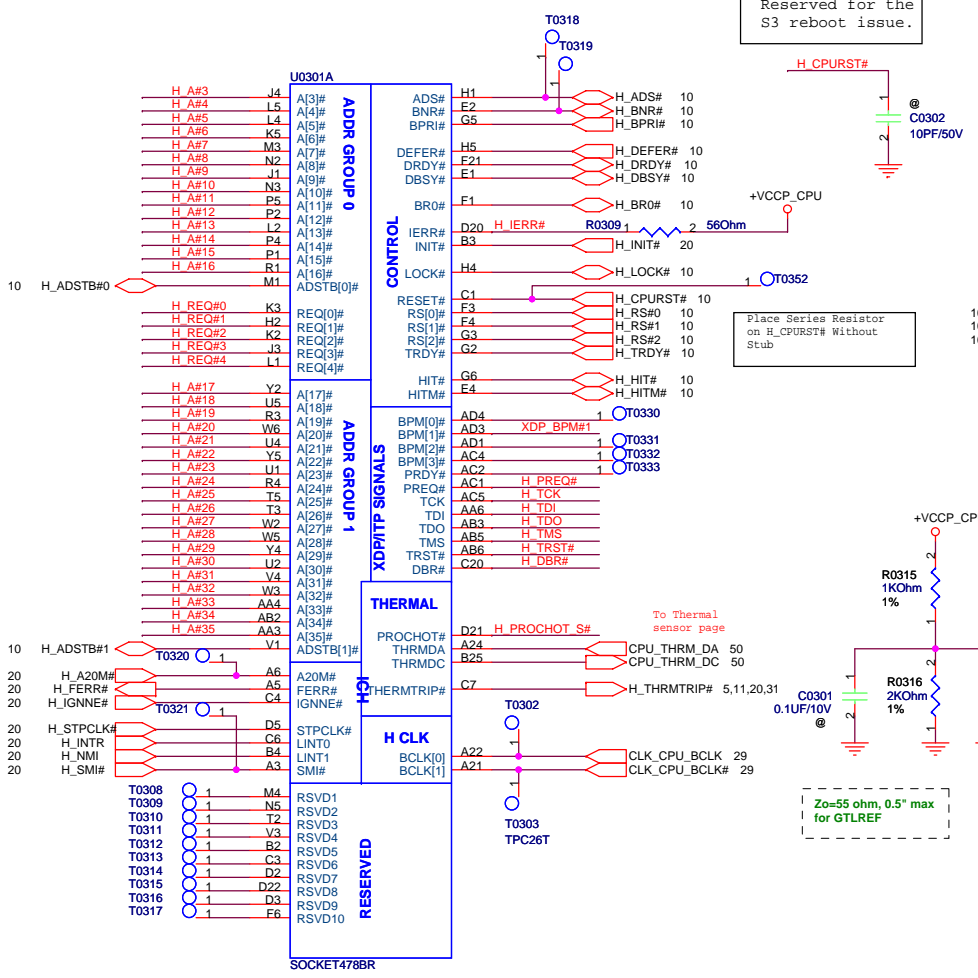
| ICH9-M GPIO | Use As | Signal Name | Power |
|-------------|--------|---------------|--------|
| GPIO 00 | GPI | PM_SYNC# | +3VS |
| GPIO 01 | GPI | - | +3VS |
| GPIO [2:5] | GPI | PCI_INT[E:H]# | +3VS |
| GPIO 06 | GPI | - | +3VS |
| GPIO 07 | GPI | - | +3VS |
| GPIO 08 | GPI | EXT_SMI# | +3VSUS |
| GPIO 09 | Native | UWB_ON | +3VSUS |
| GPIO 10 | GPI | - | +3VSUS |
| GPIO 11 | Native | EXT_SCI# | +3VSUS |
| GPIO 12 | GPO | - | +3VSUS |
| GPIO 13 | GPI | CB_SD# | +3VSUS |
| GPIO 14 | GPI | RTLAN_DSM# | +3VSUS |
| GPIO 15 | Native | - | +3VSUS |
| GPIO 16 | Native | PM DPRSLPVR | +3VS |
| GPIO 17 | GPI | WLAN_LED | +3VS |
| GPIO 18 | GPO | - | +3VS |
| GPIO 19 | GPI | - | +3VS |
| GPIO 20 | GPO | - | +3VS |
| GPIO 21 | GPI | - | +3VS |
| GPIO 22 | GPI | BT_DET# | +3VS |
| GPIO 23 | Native | - | +3VS |
| GPIO 24 | GPO | WLAN_ON | +3VSUS |
| GPIO 25 | Native | - | +3VSUS |
| GPIO 26 | Native | - | +3VSUS |
| GPIO 27 | GPO | BT_ON | +3VSUS |
| GPIO 28 | GPO | - | +3VSUS |
| GPIO 29 | Native | USB_OC5# | +3VSUS |
| GPIO 30 | Native | USB_OC6# | +3VSUS |
| GPIO 31 | Native | USB_OC7# | +3VSUS |
| GPIO 32 | GPO | - | +3VS |
| GPIO 33 | GPO | - | +3VS |
| GPIO 34 | GPO | - | +3VS |
| GPIO 35 | GPO | CLK_SATA_REQ# | +3VS |
| GPIO 36 | GPI | - | +3VS |
| GPIO 37 | GPI | PCB_ID0 | +3VS |
| GPIO 38 | GPI | PCB_ID1 | +3VS |
| GPIO 39 | GPI | PCB_ID2 | +3VS |
| GPIO 40 | Native | USB_OC1# | +3VSUS |
| GPIO 41 | Native | USB_OC2# | +3VSUS |
| GPIO 42 | Native | USB_OC3# | +3VSUS |
| GPIO 43 | Native | USB_OC4# | +3VSUS |
| GPIO 44 | Native | USB_OC8# | N/A |
| GPIO 45 | Native | USB_OC9# | N/A |
| GPIO 46 | Native | USB_OC10# | N/A |
| GPIO 47 | Native | USB_OC11# | N/A |
| GPIO 48 | GPI | - | +3VS |
| GPIO 49 | GPO | GPU_RST# | +3VS |
| GPIO 50 | Native | PCI_REQ#1 | +3VS |
| GPIO 51 | Native | - | +3VS |
| GPIO 52 | Native | PCI_REQ#2 | +3VS |
| GPIO 53 | Native | - | +3VS |
| GPIO 54 | Native | PCI_REQ#3 | +3VS |
| GPIO 55 | Native | - | +3VS |
| GPIO 56 | GPI | - | +3VSUS |
| GPIO 57 | GPI | - | +3VSUS |
| GPIO 58 | GPI | - | +3VSUS |
| GPIO 59 | Native | USB_OC0# | +3VSUS |
| GPIO 60 | Native | RTLAN_DSM_EN | +3VSUS |

| EC GPIO | Use As | Signal Name | Power |
|---------|--------|----------------|-------|
| GPA0 | GPO | PWR_LED# | |
| GPA1 | GPO | CHG_LED# | |
| GPA2 | GPO | BATSEL_3S# | |
| GPA3 | - | NOVO_CARE_LED# | |
| GPA4 | GPO | LCD_BL_PWM | |
| GPA5 | GPO | FAN_PWM | |
| GPA6 | GPO | - | |
| GPA7 | GPO | - | |
| GPB0 | GPO | CHG_EN# | |
| GPB1 | GPO | PRECHG | |
| GPB2 | GPI | - | |
| GPB3 | ALT | SMB0_CLK | |
| GPB4 | ALT | SMB0_DAT | |
| GPB5 | OD | A20GATE | |
| GPB6 | OD | RCIN# | |
| GPB7 | GPO | PM_RSMRST# | |
| GPC0 | GPI | - | |
| GPC1 | ALT | SMB1_CLK | |
| GPC2 | ALT | SMB1_DAT | |
| GPC3 | GPO | PM_PWRBTN# | |
| GPC4 | ALT | AC_IN_OC# | |
| GPC5 | GPO | OP_SD# | |
| GPC6 | ALT | BAT1_IN_OC# | |
| GPC7 | GPO | RFON_SW# | |
| GPC8 | GPI | PWRLIMIT# | |
| GPD1 | ALT | PM_SUSC# | |
| GPD2 | ALT | BUF_PLT_RST# | |
| GPD3 | OD | EXT_SCI# | |
| GPD4 | OD | EXT_SMI# | |
| GPD5 | GPO | LCD_BACKOFF# | |
| GPD6 | ALT | FAN0_TACH | |
| GPD7 | GPI | - | |
| GPE0 | GPO | VSUS_ON | |
| GPE1 | GPO | SUSC_EC# | |
| GPE2 | GPO | SUSB_EC# | |
| GPE3 | GPO | CPU_VRON | |
| GPE4 | ALT | PWR_SW# | |
| GPE5 | ALT | - | |
| GPE6 | GPI | LID_SW# | |
| GPE7 | GPO | MEDIA_KEY# | |
| GPFO | GPI | - | |
| GPF1 | GPI | NOVO_CARE# | |
| GPF2 | ALT | TP1_CLK | |
| GPF3 | ALT | TP1_DAT | |
| GPF4 | ALT | TP_CLK | |
| GPF5 | ALT | TP_DAT | |
| GPF6 | GPO | THRO_CPU | |
| GPF7 | GPO | SUSPEND_LED# | |
| GPFO | GPI | PM_THERM#_EC | |
| GPG1 | ALT | PM_SUSB# | |
| GPG2 | GPO | BAT1_CNT2# | |
| - | - | - | |
| - | - | - | |

| EC GPIO | Use As | Signal Name | Power |
|---------|--------|------------------|-------|
| - | - | - | |
| GPG6 | GPO | - | |
| - | - | - | |
| GPH0 | OD | PM_CLKRUN# | |
| GPH1 | ALT | 3G_ON# | |
| GPH2 | ALT | LOGO_LED# | |
| GPH3 | GPO | BAT_LEARN | |
| GPH4 | GPO | - | |
| GPH5 | GPO | NUM_LED# | |
| GPH6 | GPO | CAP_LED# | |
| - | - | - | |
| GPIO | GPI | NV_OVERT# | |
| GPI1 | GPI | SUS_PWRGD | |
| GPI2 | GPI | ALL_SYSTEM_PWRGD | |
| GPI3 | GPI | VRM_PWRGD | |
| GPI4 | GPI | XOUT | |
| GPI5 | GPI | YOUT | |
| GPI6 | GPI | - | |
| GPI7 | GPI | - | |
| GPJ0 | GPO | EC_CLK_EN | |
| GPJ1 | GPO | PM_PWROK | |
| GPJ2 | GPI | - | |
| GPJ3 | - | - | |
| GPJ4 | GPO | BL_DA | |
| GPJ5 | GPO | PWR_LED# | |
| GPK0 | GPI | - | |
| GPK1 | GPI | - | |
| GPK2 | GPI | - | |
| GPK3 | GPI | - | |
| GPK4 | GPI | - | |
| GPK5 | GPI | - | |
| GPL0 | GPI | APS_PWR_CNT# | |
| GPL1 | GPI | APS_ST# | |
| GPL2 | GPO | USB_PWR_EN# | |
| GPL3 | GPO | - | |
| GPL4 | GPO | - | |
| GPL5 | GPO | AC_ID | |
| GPL6 | GPO | AC_65W | |
| GPL7 | GPO | CHG_LOW_LED# | |
| GPK6 | GPO | - | |
| GPK7 | GPI | - | |
| - | - | - | |
| - | - | - | |



Reserved for the S3 reboot issue.



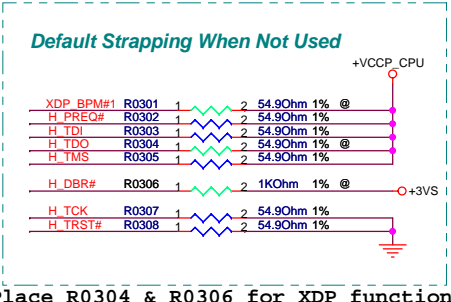
Place Series Resistor on H_CPURST# Without Stub

Comp0,2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
 Comp 1,3 connect with Zo=55 ohm, make trace length shorter than 0.5".

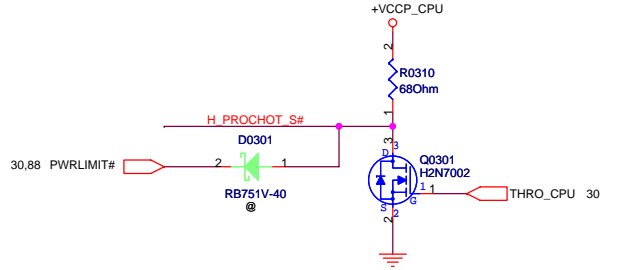
Place Series Resistor on H_PWRGD Without Stub

Zo=55 ohm, 0.5" max for GTLREF

| BCLK | FSB | BSEL2 | BSEL1 | BSEL0 |
|------|------|-------|-------|-------|
| 166 | 667 | L | H | H |
| 200 | 800 | L | H | L |
| 266 | 1067 | L | L | L |



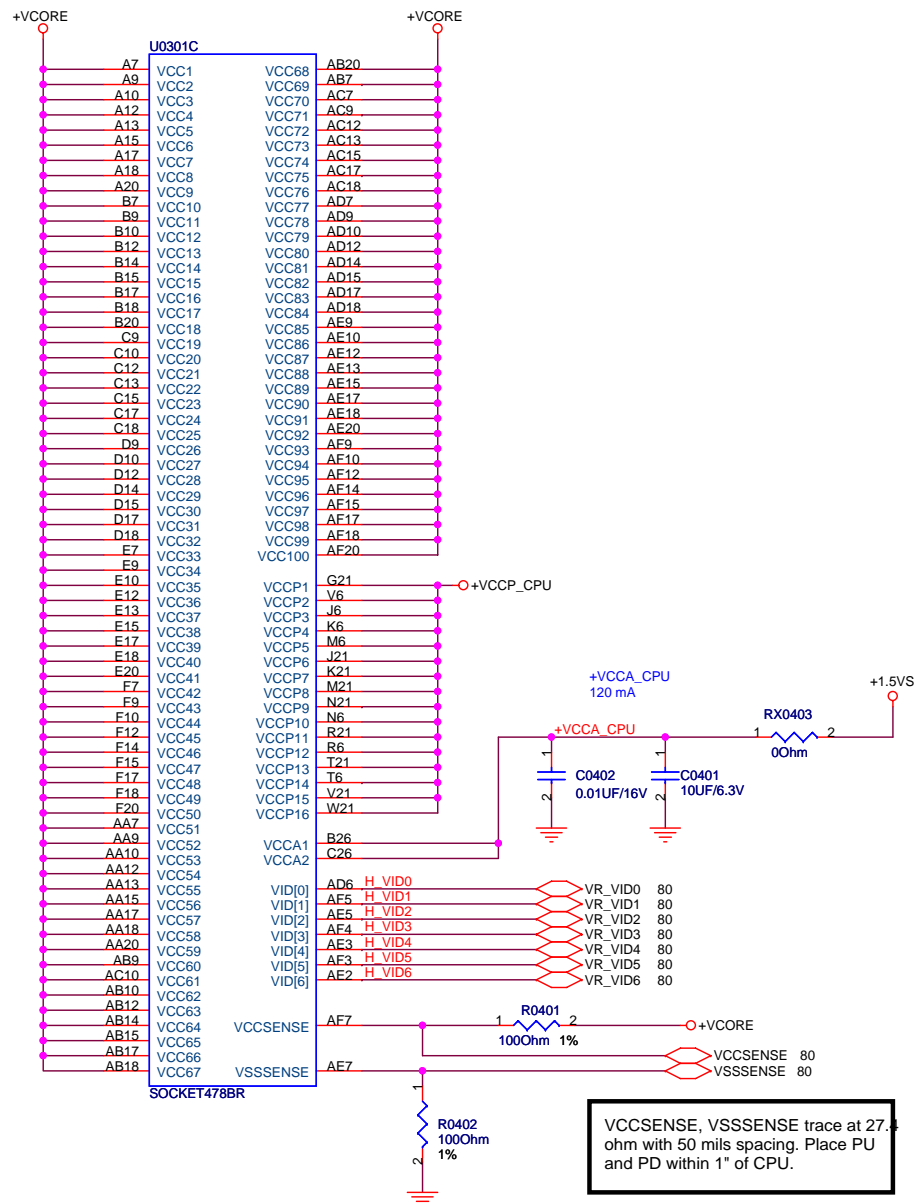
Place R0304 & R0306 for XDP function



+VCORE ○ +VCORE 5,80

+VCCP_CPU ○ +VCCP_CPU 3,5

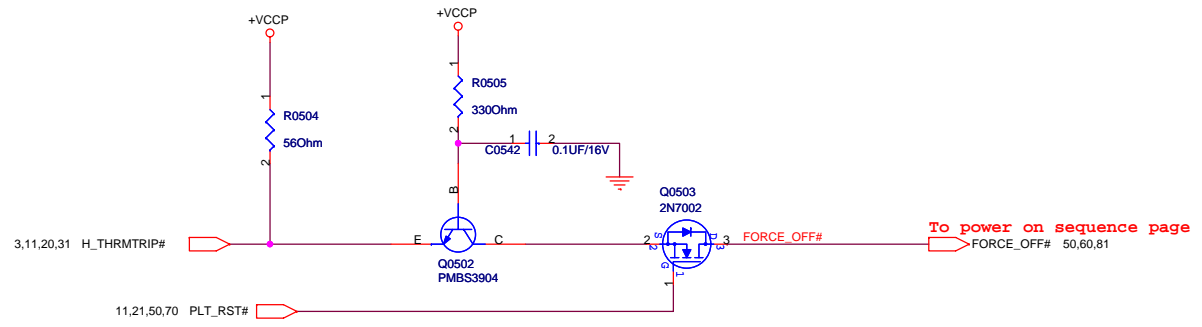
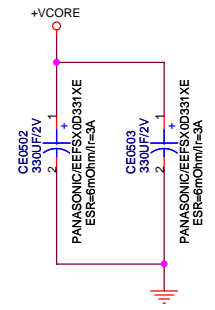
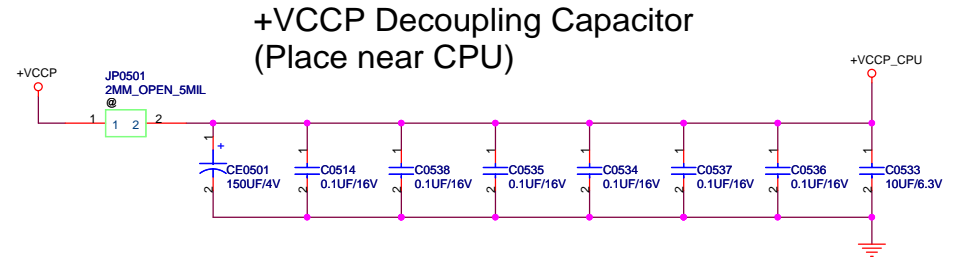
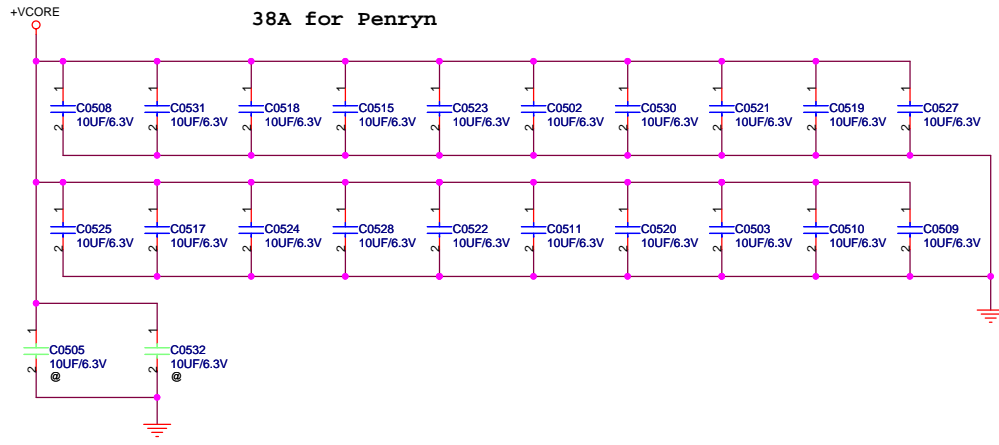
+1.5VS ○ +1.5VS 14,23,53,57,59,82



VCCSENSE, VSSSENSE trace at 27 ohm with 50 mils spacing. Place PU and PD within 1" of CPU.

| | | | |
|-----------------------------------|--------------|------------------------|----|
| | | Title : Penryn CPU (2) | |
| | | Engineer: Tina Lee | |
| Size | Project Name | Rev | |
| Custom | Rocky 40/50 | 1.0 | |
| Date: Thursday, December 20, 2007 | Sheet 4 | of | 94 |

+V CORE 4,80
 +VCCP 10,11,13,14,20,23,29,80,82
 +VCCP_CPU 3,4



Thermal Trip signal(From CPU to ICH-9M and sequence)

5

4

3

2

1

D

D

C

C

B

B

A

A



Engineer: *Tina Lee*

| | | |
|------------|------------------------------------|------------|
| Size A4 | Project Name Rocky 40/50 | Rev 1.0 |
|------------|------------------------------------|------------|

Date: **Monday, December 17, 2007** Sheet **6** of **94**

5

4

3

2

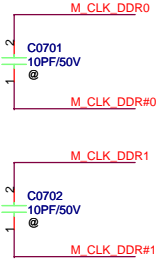
1



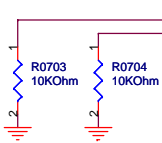
SMBus Slave Address:A0H

SMBus Slave Address: A0H

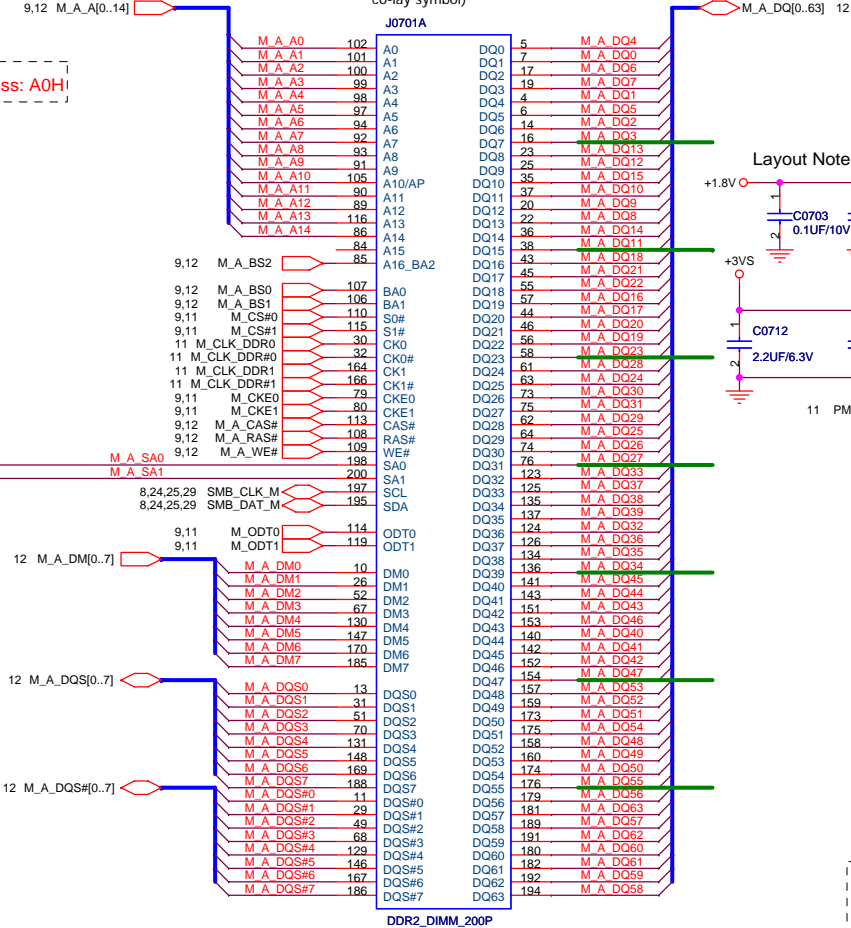
Place near SO-DIMM_0



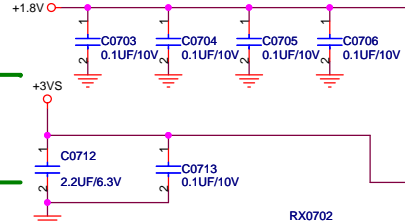
Layout Note: Place these caps near SO DIMM 0



temp_5886_t101
(12G025M22000LVwith 12G025C2200WLV
co-lay symbol)

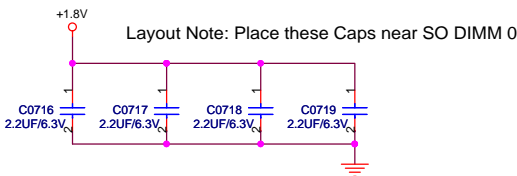
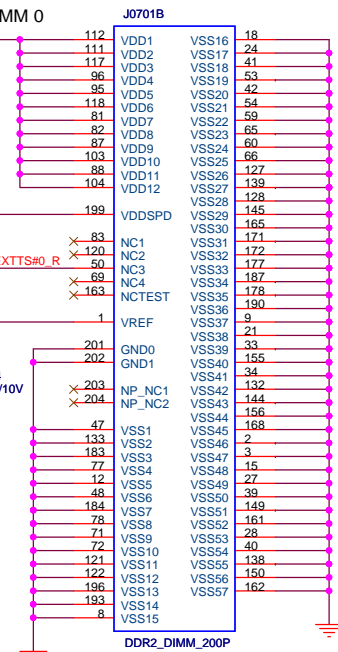


Layout Note: Place these caps near SO DIMM 0



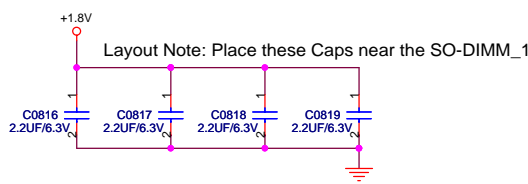
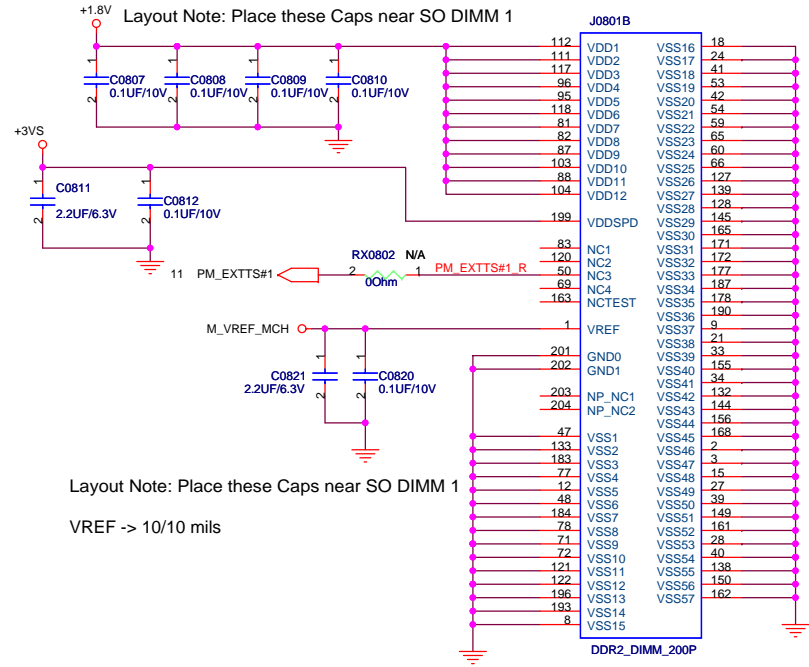
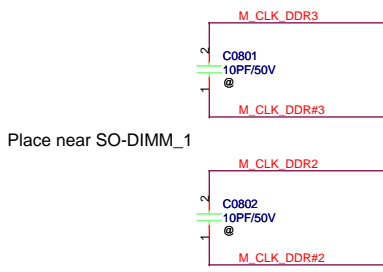
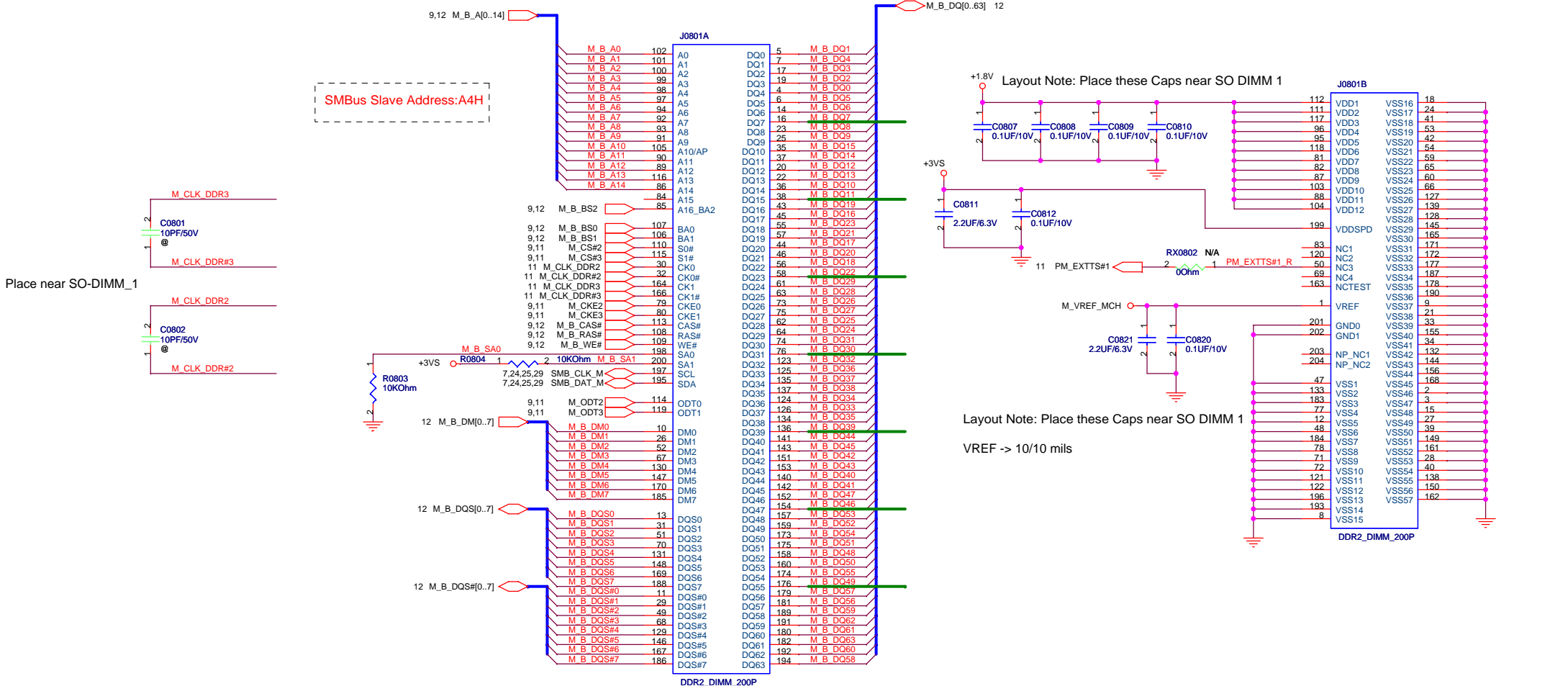
VREF -> 10/10 mils

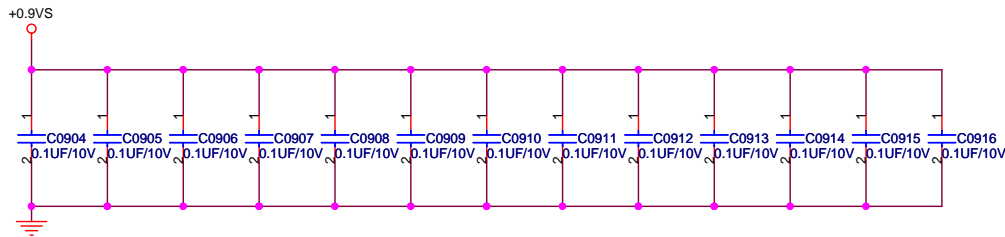
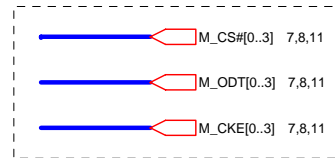
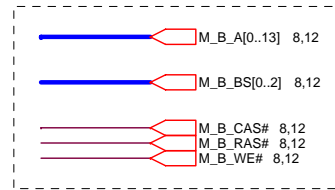
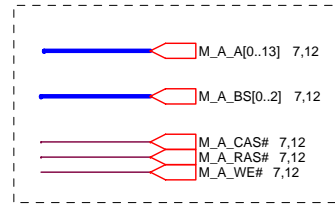
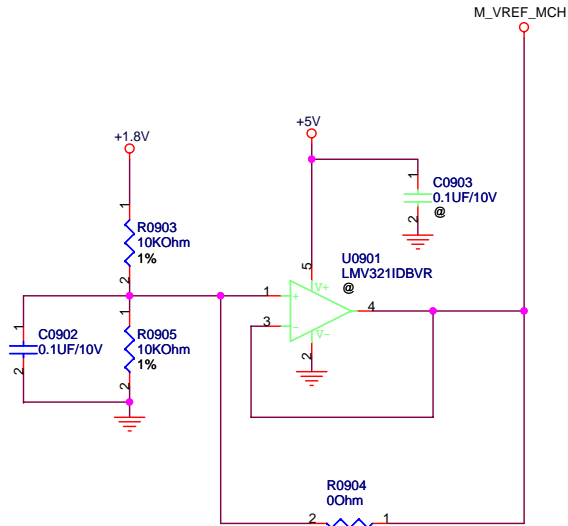
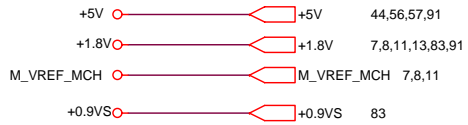
SO-DIMM 0 is placed nearer the GMCH than SO-DIMM 1



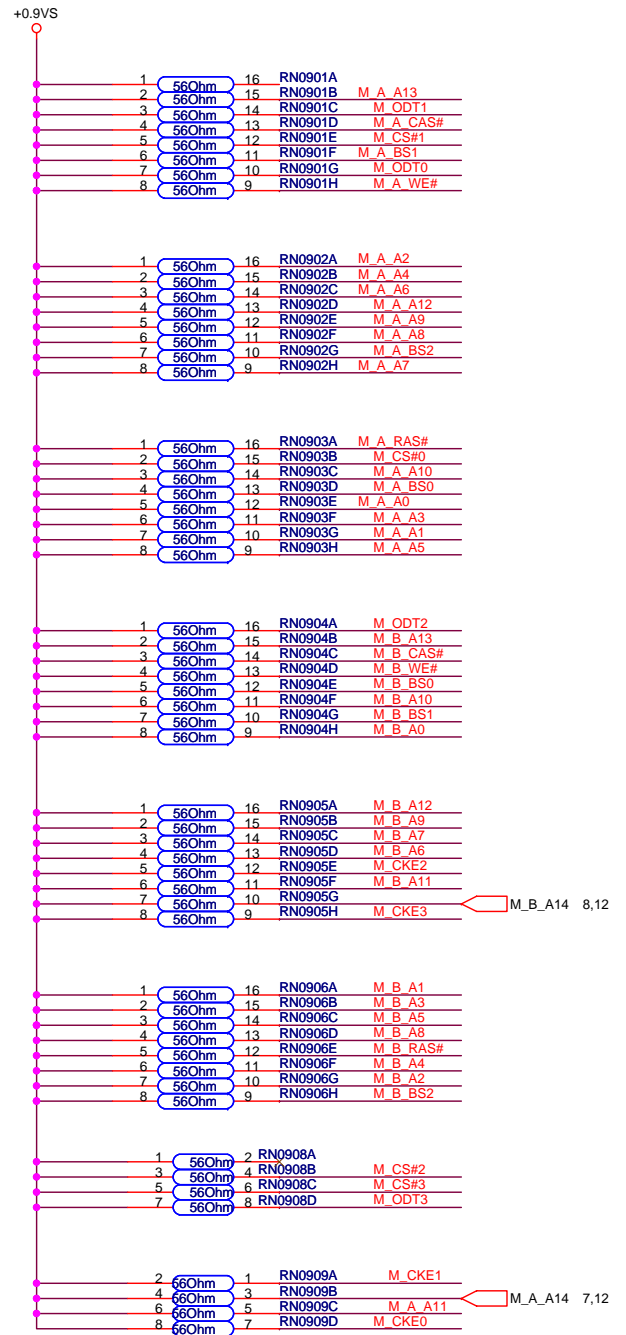
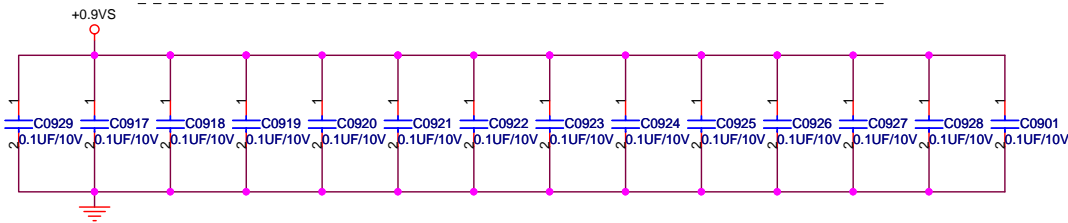


temp_5886_t102
(12G025032005LV with 12G025022004LV
CO-LAY symbol)

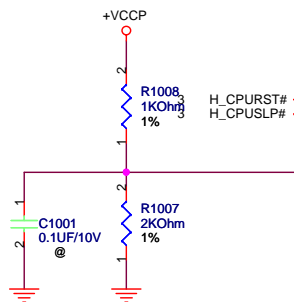
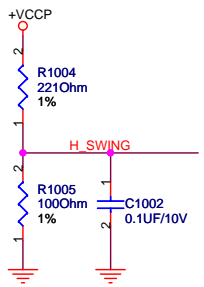
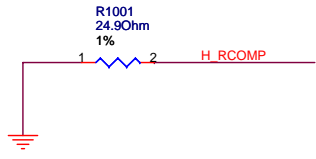




Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS



+VCCP +VCCP 5,11,13,14,20,23,29,80,82



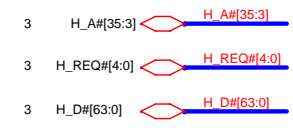
CAP 0.1U within 100 miles from GMCH

| Pin | Label | Signal |
|--------|-------|---------|
| H_D#0 | F2 | H_D#_0 |
| H_D#1 | G8 | H_D#_1 |
| H_D#2 | F8 | H_D#_2 |
| H_D#3 | E6 | H_D#_3 |
| H_D#4 | G2 | H_D#_4 |
| H_D#5 | H6 | H_D#_5 |
| H_D#6 | H2 | H_D#_6 |
| H_D#7 | F6 | H_D#_7 |
| H_D#8 | D4 | H_D#_8 |
| H_D#9 | H3 | H_D#_9 |
| H_D#10 | M9 | H_D#_10 |
| H_D#11 | M11 | H_D#_11 |
| H_D#12 | J1 | H_D#_12 |
| H_D#13 | J2 | H_D#_13 |
| H_D#14 | N12 | H_D#_14 |
| H_D#15 | J6 | H_D#_15 |
| H_D#16 | P2 | H_D#_16 |
| H_D#17 | L2 | H_D#_17 |
| H_D#18 | R2 | H_D#_18 |
| H_D#19 | N9 | H_D#_19 |
| H_D#20 | L6 | H_D#_20 |
| H_D#21 | M5 | H_D#_21 |
| H_D#22 | H3 | H_D#_22 |
| H_D#23 | N2 | H_D#_23 |
| H_D#24 | R1 | H_D#_24 |
| H_D#25 | N5 | H_D#_25 |
| H_D#26 | N6 | H_D#_26 |
| H_D#27 | P13 | H_D#_27 |
| H_D#28 | N8 | H_D#_28 |
| H_D#29 | L7 | H_D#_29 |
| H_D#30 | N10 | H_D#_30 |
| H_D#31 | M3 | H_D#_31 |
| H_D#32 | M3 | H_D#_32 |
| H_D#33 | Y3 | H_D#_33 |
| H_D#34 | AD14 | H_D#_34 |
| H_D#35 | Y6 | H_D#_35 |
| H_D#36 | Y10 | H_D#_36 |
| H_D#37 | Y12 | H_D#_37 |
| H_D#38 | Y14 | H_D#_38 |
| H_D#39 | Y7 | H_D#_39 |
| H_D#40 | W2 | H_D#_40 |
| H_D#41 | AA8 | H_D#_41 |
| H_D#42 | Y9 | H_D#_42 |
| H_D#43 | AA13 | H_D#_43 |
| H_D#44 | AA9 | H_D#_44 |
| H_D#45 | AA11 | H_D#_45 |
| H_D#46 | AD10 | H_D#_46 |
| H_D#47 | AD13 | H_D#_47 |
| H_D#48 | AE12 | H_D#_48 |
| H_D#49 | AE9 | H_D#_49 |
| H_D#50 | AA2 | H_D#_50 |
| H_D#51 | AD8 | H_D#_51 |
| H_D#52 | AA3 | H_D#_52 |
| H_D#53 | AD3 | H_D#_53 |
| H_D#54 | AD7 | H_D#_54 |
| H_D#55 | AE14 | H_D#_55 |
| H_D#56 | AF3 | H_D#_56 |
| H_D#57 | AC1 | H_D#_57 |
| H_D#58 | AE3 | H_D#_58 |
| H_D#59 | AC3 | H_D#_59 |
| H_D#60 | AE11 | H_D#_60 |
| H_D#61 | AE8 | H_D#_61 |
| H_D#62 | AG2 | H_D#_62 |
| H_D#63 | AD6 | H_D#_63 |

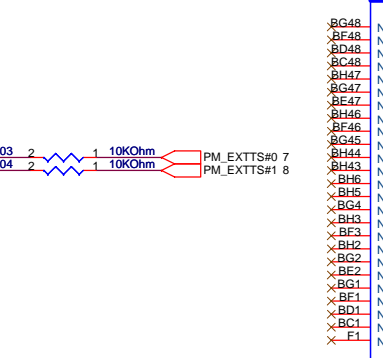
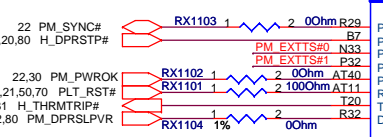
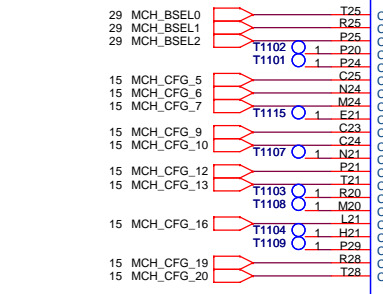
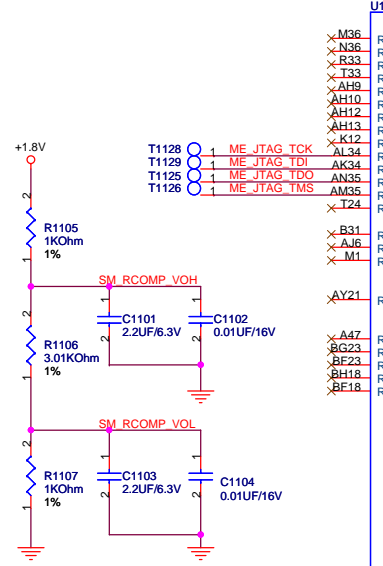
U1001A

HOST

| | | |
|------------|-----|------------------|
| H_A#_3 | A14 | H_A#3 |
| H_A#_4 | C15 | H_A#4 |
| H_A#_5 | F16 | H_A#5 |
| H_A#_6 | H13 | H_A#6 |
| H_A#_7 | C18 | H_A#7 |
| H_A#_8 | M16 | H_A#8 |
| H_A#_9 | J13 | H_A#9 |
| H_A#_10 | P16 | H_A#10 |
| H_A#_11 | R16 | H_A#11 |
| H_A#_12 | N17 | H_A#12 |
| H_A#_13 | M13 | H_A#13 |
| H_A#_14 | E17 | H_A#14 |
| H_A#_15 | P17 | H_A#15 |
| H_A#_16 | F17 | H_A#16 |
| H_A#_17 | G20 | H_A#17 |
| H_A#_18 | B19 | H_A#18 |
| H_A#_19 | J16 | H_A#19 |
| H_A#_20 | E20 | H_A#20 |
| H_A#_21 | H16 | H_A#21 |
| H_A#_22 | J20 | H_A#22 |
| H_A#_23 | L17 | H_A#23 |
| H_A#_24 | A17 | H_A#24 |
| H_A#_25 | B17 | H_A#25 |
| H_A#_26 | L16 | H_A#26 |
| H_A#_27 | C21 | H_A#27 |
| H_A#_28 | J17 | H_A#28 |
| H_A#_29 | H20 | H_A#29 |
| H_A#_30 | B18 | H_A#30 |
| H_A#_31 | K17 | H_A#31 |
| H_A#_32 | B20 | H_A#32 |
| H_A#_33 | F21 | H_A#33 |
| H_A#_34 | K21 | H_A#34 |
| H_A#_35 | L20 | H_A#35 |
| H_ADS# | H12 | H_ADS# 3 |
| H_ADSTB#_0 | B16 | H_ADSTB#0 3 |
| H_ADSTB#_1 | G17 | H_ADSTB#1 3 |
| H_BNR# | A9 | H_BNR# 3 |
| H_BPRI# | F11 | H_BPRI# 3 |
| H_BREQ# | G12 | H_BPRI# 3 |
| H_DEFER# | E9 | H_DEFER# 3 |
| H_DBSY# | B10 | H_DBSY# 3 |
| HPLL_CLK | AH7 | CLK_MCH_BCLK# 29 |
| HPLL_CLK# | AH6 | CLK_MCH_BCLK# 29 |
| H_DPWR# | J11 | H_DPWR# 3 |
| H_DRDY# | F9 | H_DRDY# 3 |
| H_HIT# | H9 | H_HIT# 3 |
| H_HITM# | E12 | H_HITM# 3 |
| H_LOCK# | H11 | H_LOCK# 3 |
| H_TRDY# | C9 | H_TRDY# 3 |
| H_DINV#_0 | J8 | H_DINV#0 3 |
| H_DINV#_1 | L3 | H_DINV#1 3 |
| H_DINV#_2 | Y13 | H_DINV#2 3 |
| H_DINV#_3 | Y1 | H_DINV#3 3 |
| H_DSTBN#_0 | L10 | H_DSTBN#0 3 |
| H_DSTBN#_1 | M7 | H_DSTBN#1 3 |
| H_DSTBN#_2 | AA5 | H_DSTBN#2 3 |
| H_DSTBN#_3 | AE6 | H_DSTBN#3 3 |
| H_DSTBP#_0 | L9 | H_DSTBP#0 3 |
| H_DSTBP#_1 | M8 | H_DSTBP#1 3 |
| H_DSTBP#_2 | AA6 | H_DSTBP#2 3 |
| H_DSTBP#_3 | AE5 | H_DSTBP#3 3 |
| H_REQ#_0 | B15 | H_REQ#0 |
| H_REQ#_1 | K13 | H_REQ#1 |
| H_REQ#_2 | E13 | H_REQ#2 |
| H_REQ#_3 | B13 | H_REQ#3 |
| H_REQ#_4 | B14 | H_REQ#4 |
| H_RS#_0 | B6 | H_RS#0 3 |
| H_RS#_1 | F12 | H_RS#1 3 |
| H_RS#_2 | C8 | H_RS#2 3 |



| | | | |
|--|--------------------|-----------------------------------|--|
| | | Title : Cantiga -- CPU (1) | |
| | | Engineer: <i>Tina Lee</i> | |
| Size | Project Name | Rev | |
| Custom | Rocky 40/50 | 1.0 | |
| Date: Thursday, December 20, 2007 | | Sheet 10 of 94 | |



U1001B

RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
RSVD8
RSVD9
RSVD10
RSVD11
RSVD12
RSVD13
RSVD14
RSVD15
RSVD16
RSVD17
RSVD20
RSVD21
RSVD22
RSVD23
RSVD24
RSVD25

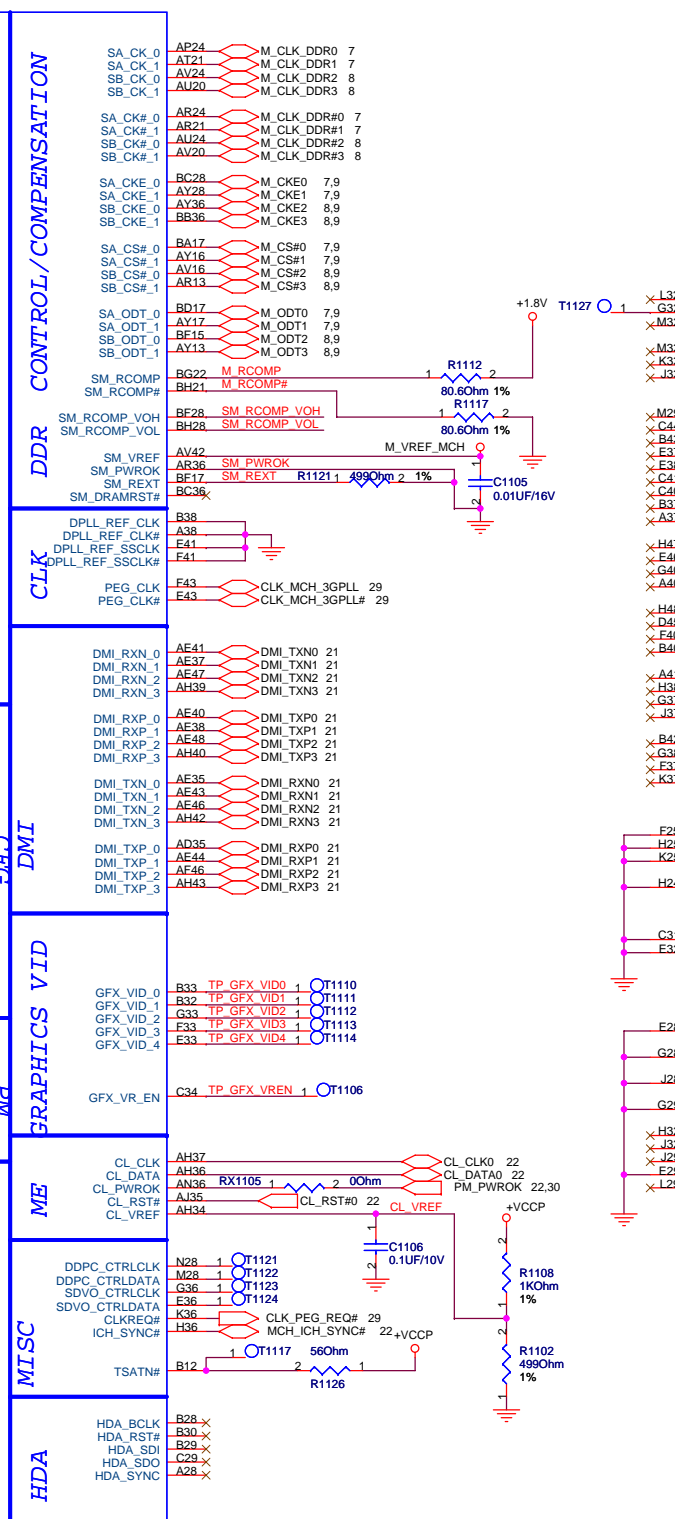
CFG_0
CFG_1
CFG_2
CFG_3
CFG_4
CFG_5
CFG_6
CFG_7
CFG_8
CFG_9
CFG_10
CFG_11
CFG_12
CFG_13
CFG_14
CFG_15
CFG_16
CFG_17
CFG_18
CFG_19
CFG_20

PM_SYNC#
PM_DPRSTP#
PM_EXT_TS#_0
PM_EXT_TS#_1
RSTIN#
THERMTRIP#
DPRSLPVR

NC.1
NC.2
NC.3
NC.4
NC.5
NC.6
NC.7
NC.8
NC.9
NC.10
NC.11
NC.12
NC.13
NC.14
NC.15
NC.16
NC.17
NC.18
NC.19
NC.20
NC.21
NC.22
NC.23
NC.24
NC.25

CL_CLK
CL_DATA
CL_PWROK
CL_RST#
CL_VREF
DDPC_CTRLCLK
SDVO_CTRLCLK
SDVO_CTRLDATA
CLKREQ#
ICH_SYNC#
TSATN#

HDA_BCLK
HDA_RST#
HDA_SDI
HDA_SDO
HDA_SYNC



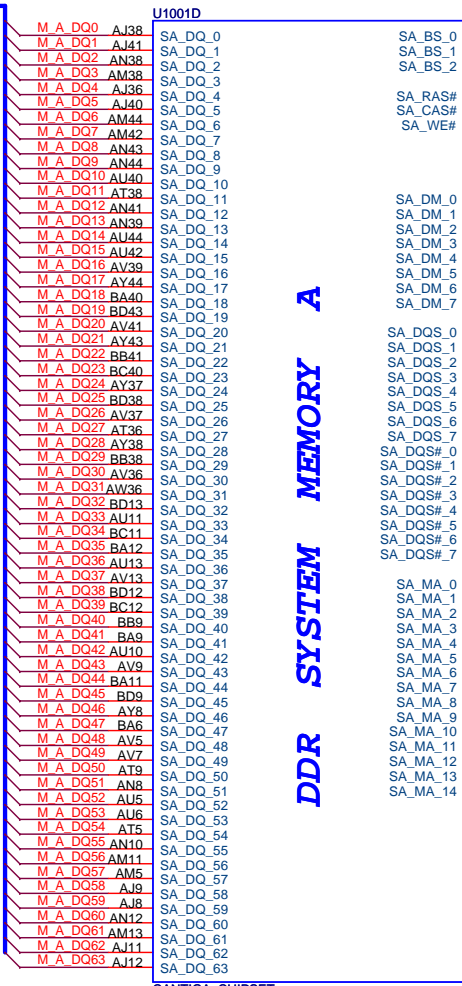
ASUS Title : Cantiga-DDR2/PEG(2)

Engineer: Tina Lee

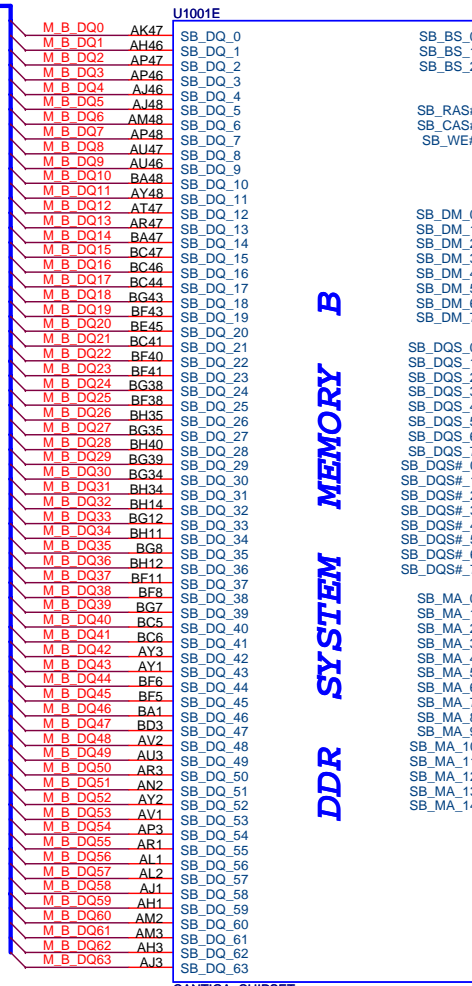
| | | |
|--------|--------------|-----|
| Size | Project Name | Rev |
| Custom | Rocky 40/50 | 1.0 |

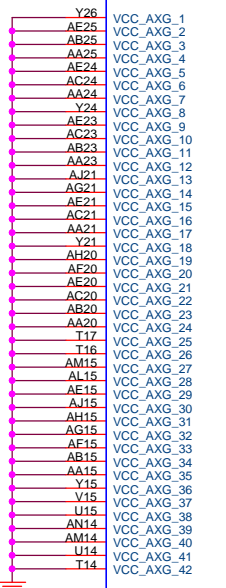
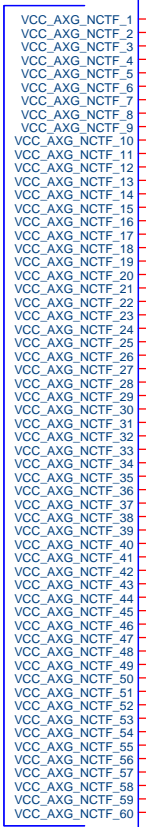
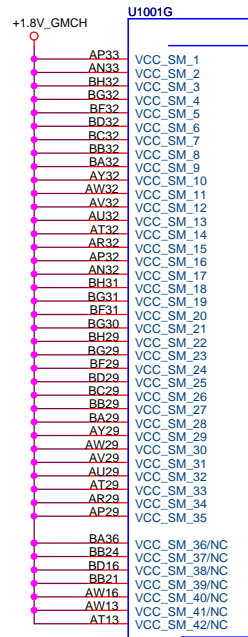
Date: Thursday, December 20, 2007 Sheet 11 of 94

7 M_A_DQ[0:63]



8 M_B_DQ[0:63]



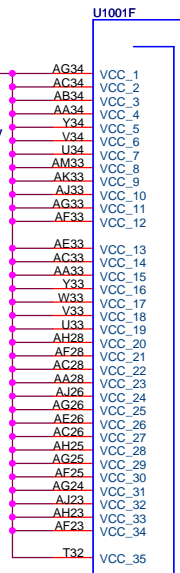
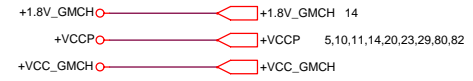
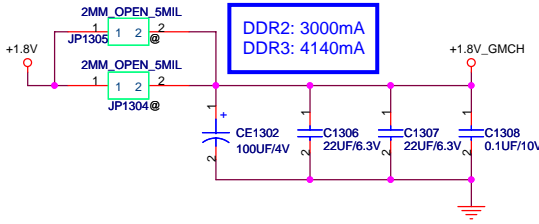
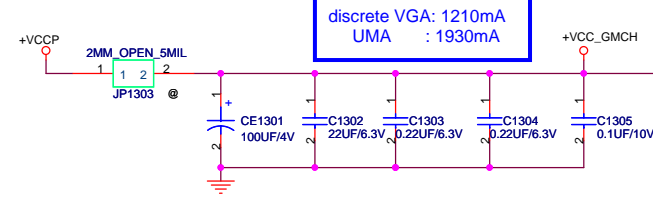
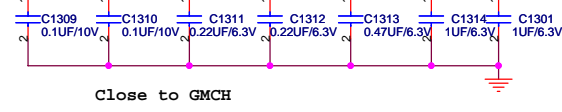
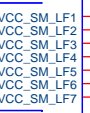


VCC SM POWER

VCC GFX NCTF

Max: 6327mA

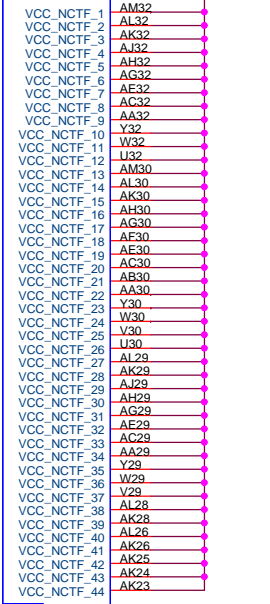
VCC SM LF



VCC CORE

POWER

VCC NCTF



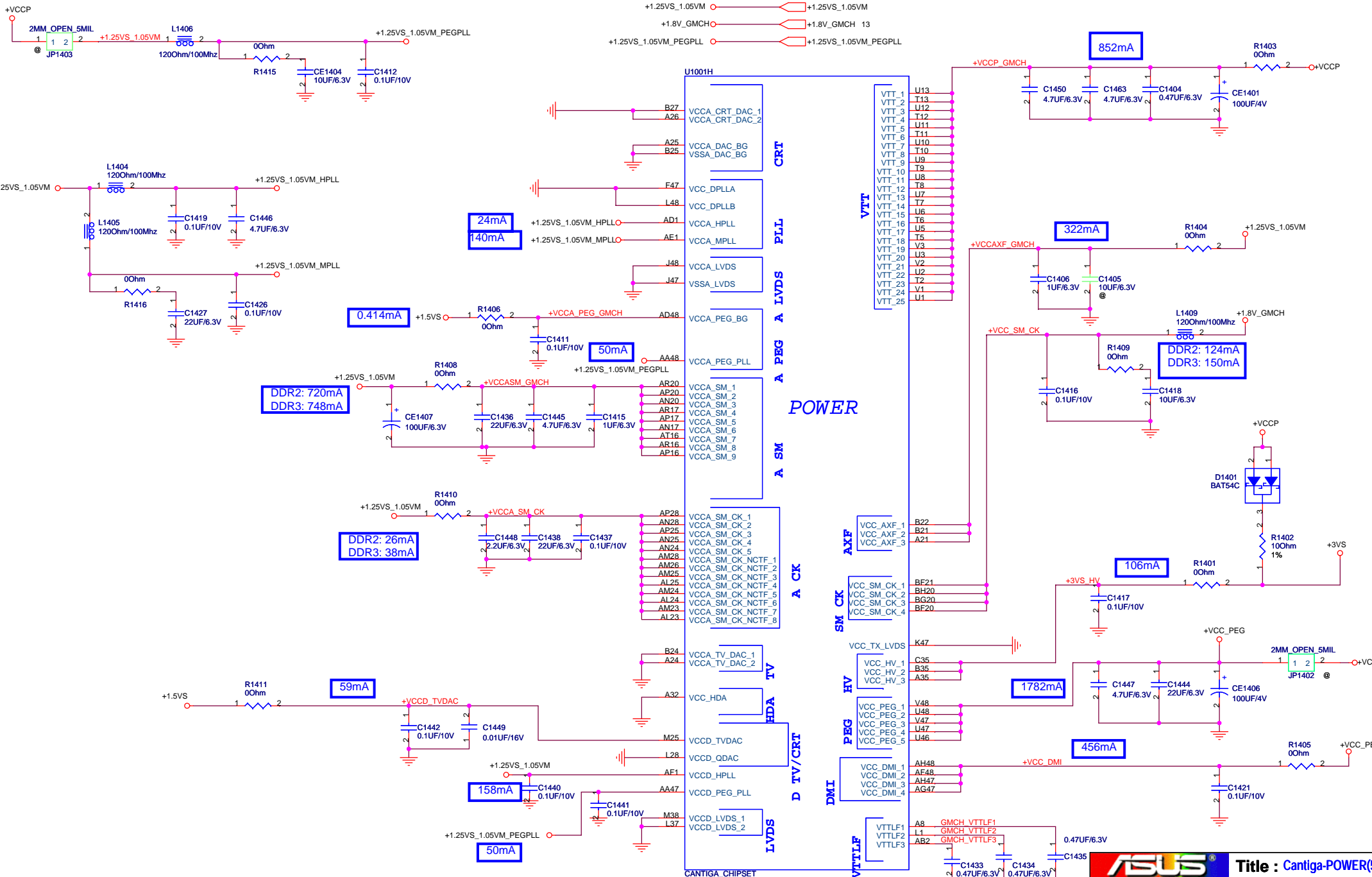
CANTIGA_CHIPSET

CANTIGA_CHIPSET

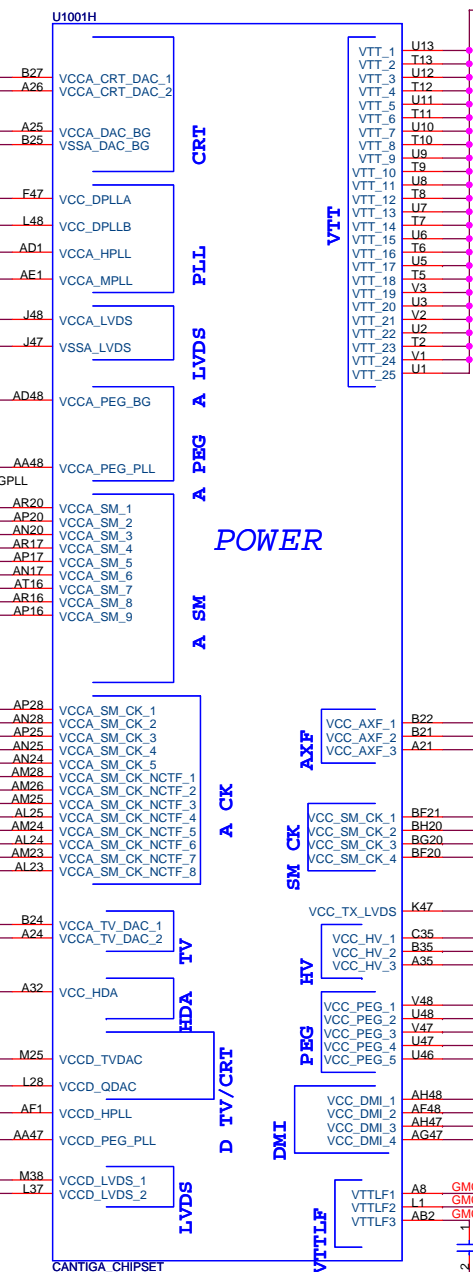
Route VCC_AGX_SENSE and VSS_AGX_SENSE differentially.

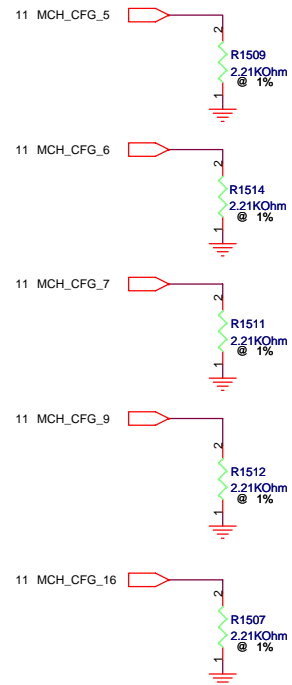
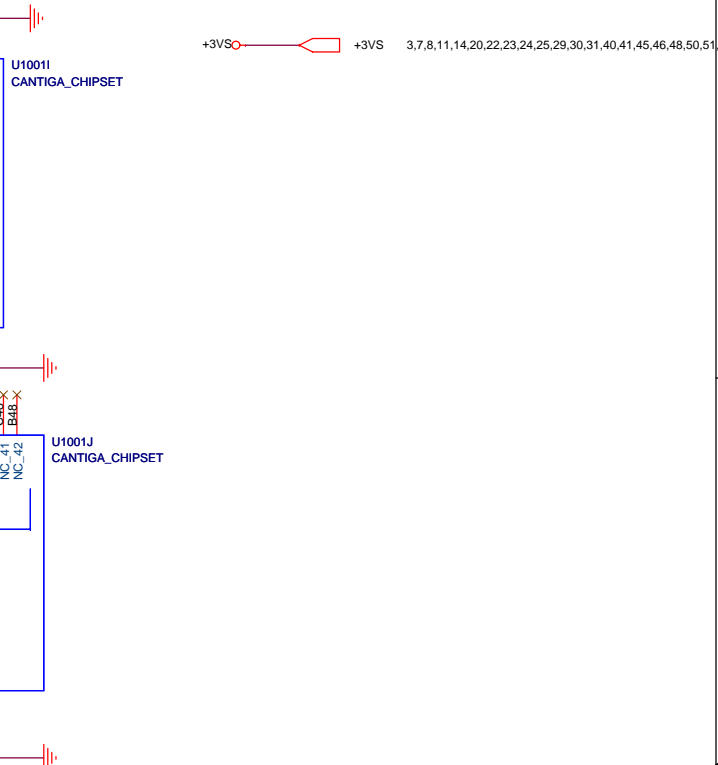
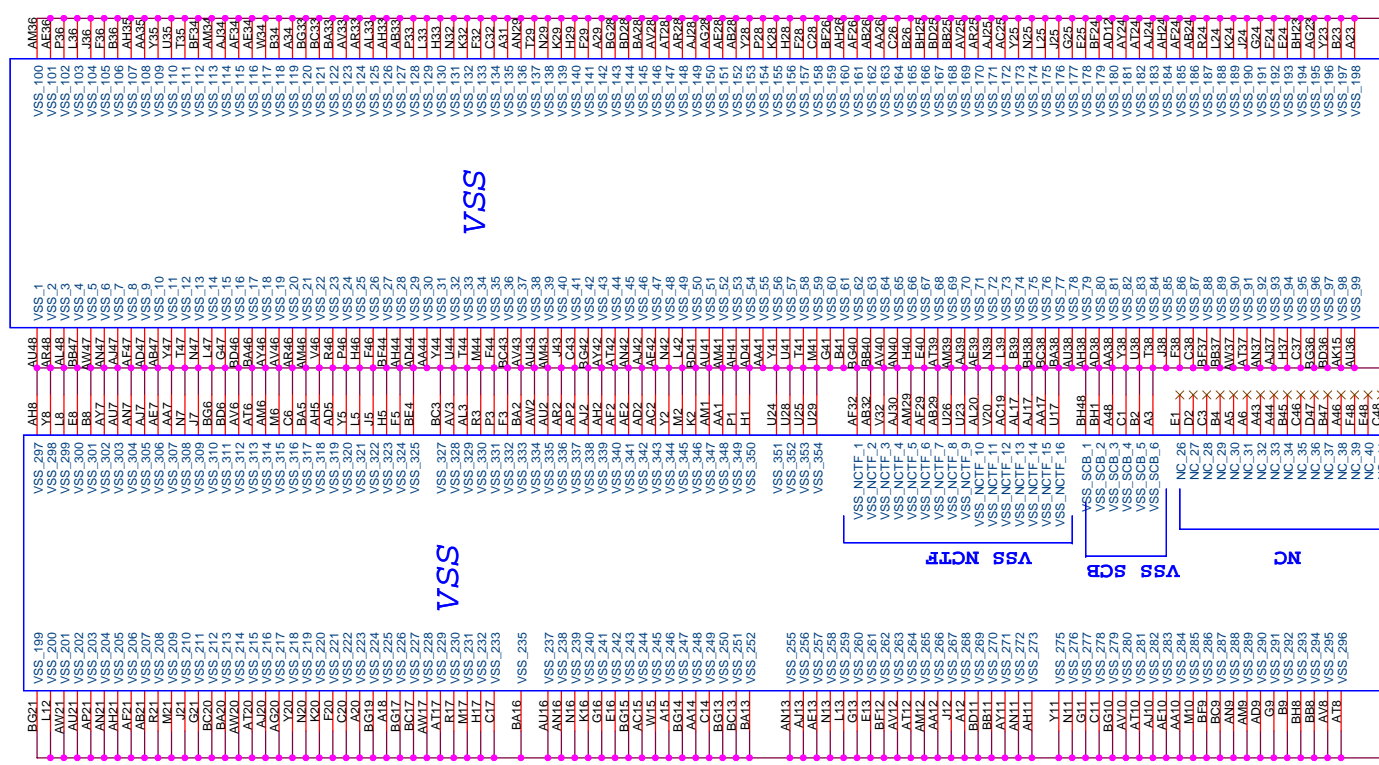
ASUS Title : Cantiga-POWER (4)
 Engineer: Tina Lee

| | | |
|-----------------------------------|----------------|-----|
| Size | Project Name | Rev |
| Custom | Rocky 40/50 | 1.0 |
| Date: Thursday, December 20, 2007 | Sheet 13 of 94 | |



| | |
|-----------------------|--|
| +3VS | 3,7,8,11,15,20,22,23,24,25,29,30,31,40,41,45,46,48,50,51,53,57,58,59,61,70,74,75,91,92 |
| +1.5VS | 4,23,53,57,59,82 |
| +VCCP | 5,10,11,13,20,23,29,80,82 |
| +1.25VS_1.05VM | +1.25VS_1.05VM |
| +1.8V_GMCH | 13 |
| +1.25VS_1.05VM_PEGPLL | +1.25VS_1.05VM_PEGPLL |





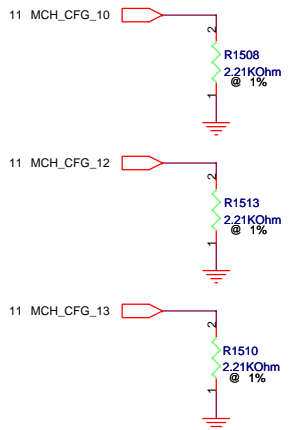
CFG5 : DMI STRAP
HIGH = DMI X 4 (Default)
LOW = DMI X 2

CFG6 : Integrated TPM Host Interface
HIGH = iTPM disable (Default)
LOW = iTPM enable

CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite
HIGH = With confidentiality (Default)
LOW = Without confidentiality

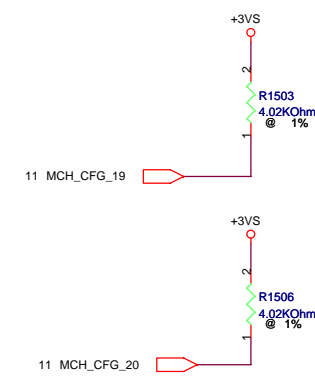
CFG9 : PCIE GRAPHIC LANE
LOW = Reverse Lanes
HIGH = Normal Operation (Default)

CFG16 : FSB Dynamic ODT
HIGH = Enable (Default)
LOW = Disable



CFG10 : PCIe Loopback
HIGH = Disable (Default)
LOW = Enable

CFG [13:12] : XOR/ALL-Z
00 = Reserved
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation (Default)



CFG19 : DMI Lane Reversal
LOW = NORMAL (default)
HIGH = Reverse Lanes

CFG20 : SDVO/PCIE CONCURRENT MODE
LOW = ONLY SDVO or PCIE is Operational (Default)
HIGH = SDVO and PCIE are operating simultaneously via the PEG port

5

4

3

2

1

D

D

C

C

B

B

A

A

| | | | |
|---|--------------------|----------------------------------|-----------------|
|  | | Title : *** | |
| | | Engineer: <i>Tina Lee</i> | |
| Size | Project Name | Rev | |
| A4 | Rocky 40/50 | 1.0 | |
| Date: Monday, December 17, 2007 | | Sheet | 16 of 94 |

5

4

3

2

1

5

4

3

2

1

D

D

C

C

B

B

A

A

| | | | |
|---|--------------------|----------------------------------|------------------------|
|  | | Title : *** | |
| | | Engineer: <i>Tina Lee</i> | |
| Size | Project Name | Rev | |
| A4 | Rocky 40/50 | 1.0 | |
| Date: Monday, December 17, 2007 | | Sheet | 17 of 94 |

5

4

3

2

1

5

4

3

2

1

D

D

C


C

B

B

A

A

| | | | |
|---|--------------------|----------------------------------|-----------------|
|  | | Title : *** | |
| | | Engineer: <i>Tina Lee</i> | |
| Size | Project Name | Rev | |
| A4 | Rocky 40/50 | 1.0 | |
| Date: Monday, December 17, 2007 | | Sheet | 18 of 94 |

5

4

3

2

1

5

4

3

2

1

D

D

C

C

B

B

A

A



Engineer: *Tina Lee*

| | | |
|------------|------------------------------------|------------|
| Size A4 | Project Name Rocky 40/50 | Rev 1.0 |
|------------|------------------------------------|------------|

Date: **Monday, December 17, 2007** Sheet **19** of **94**

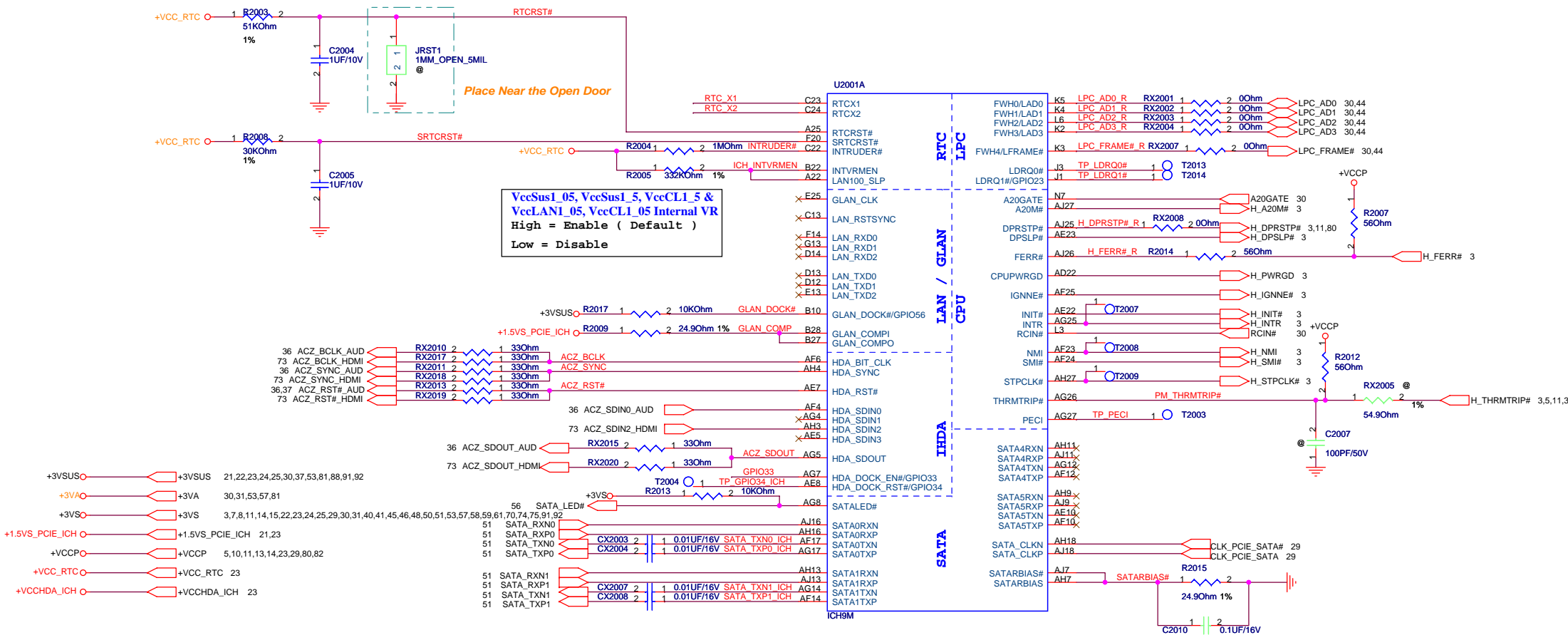
5

4

3

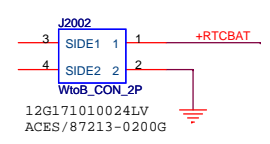
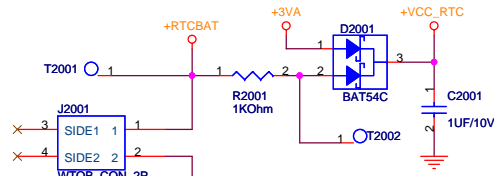
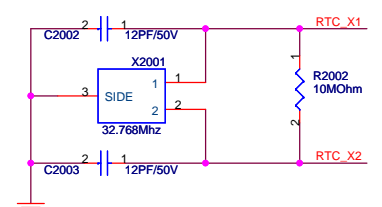
2

1

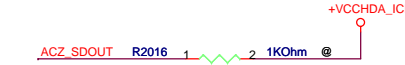


VccSus1_05, VccSus1_5, VccCLI_5 & VccLAN1_05, VccCLI_05 Internal VR
 High = Enable (Default)
 Low = Disable

- +3VSUS0 → +3VSUS 21,22,23,24,25,30,37,53,81,88,91,92
- +3VA → +3VA 30,31,53,57,81
- +3VS → +3VS 3,7,8,11,14,15,22,23,24,25,29,30,31,40,41,45,46,48,50,51,53,57,58,59,61,70,74,75,91,92
- +1.5VS_PCIE_ICH → +1.5VS_PCIE_ICH 21,23
- +VCCP → +VCCP 5,10,11,13,14,23,29,80,82
- +VCC_RTC → +VCC_RTC 23
- +VCC_HDA_ICH → +VCC_HDA_ICH 23



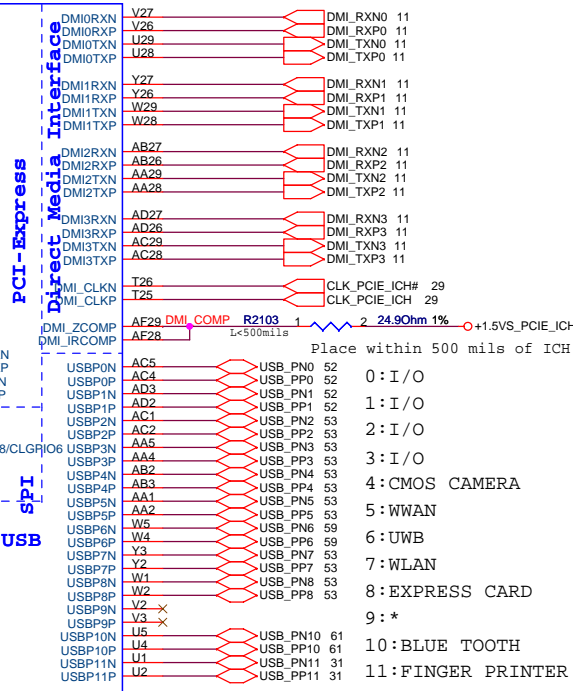
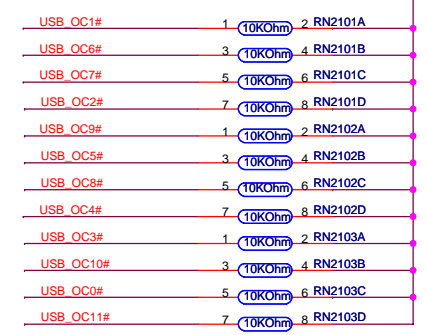
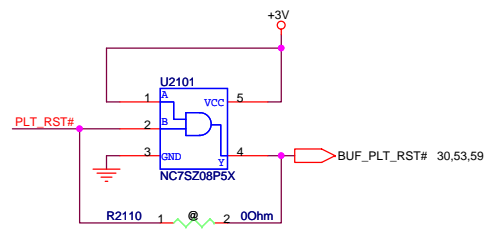
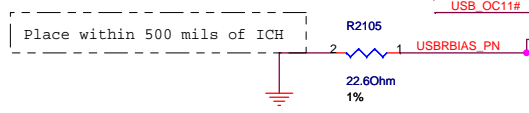
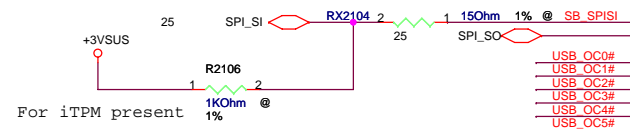
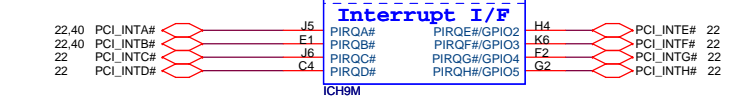
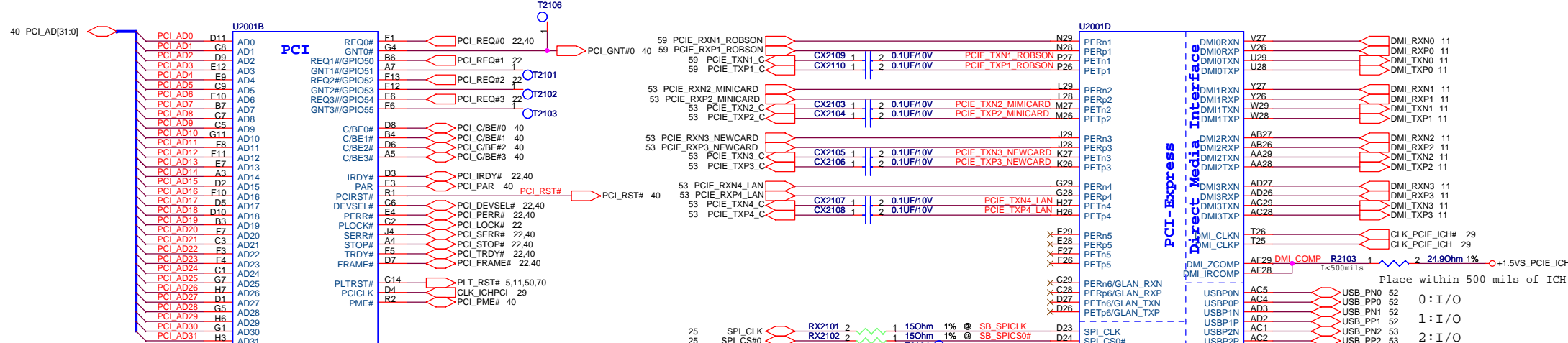
12G17100002RLV
 TYCO/3-1734261-2



[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap
 00 = Reserved
 01 = Enter XOR Chain
 10 = Normal Operation (Default)
 11 = Set PCIe Port Config Bit 1

| | | | |
|-----------------------------------|--------------------|----------------------------|----------|
| ASUS | | Title : SB-ICH9M(1) | |
| Engineer: Tina Lee | | | |
| Size | Project Name | Rev | |
| Custom | Rocky 40/50 | 1.0 | |
| Date: Thursday, December 20, 2007 | | Sheet | 20 of 94 |

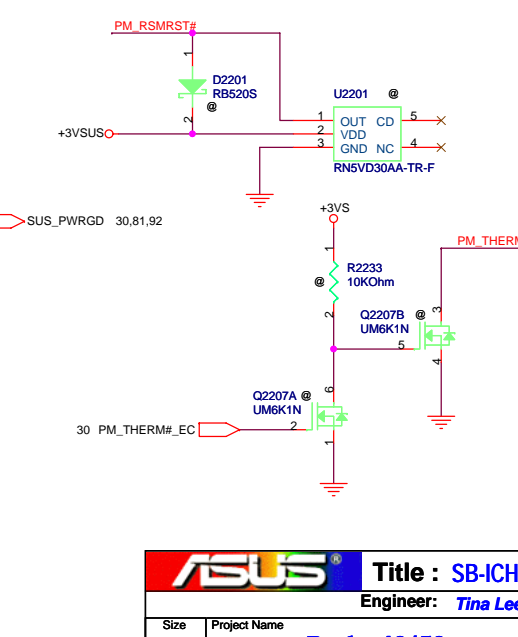
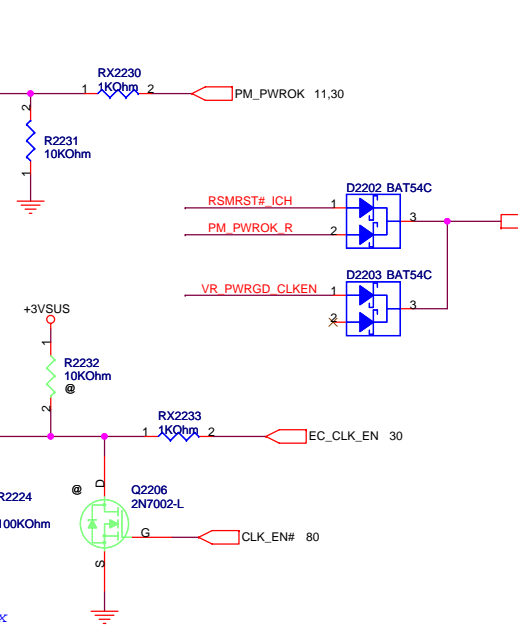
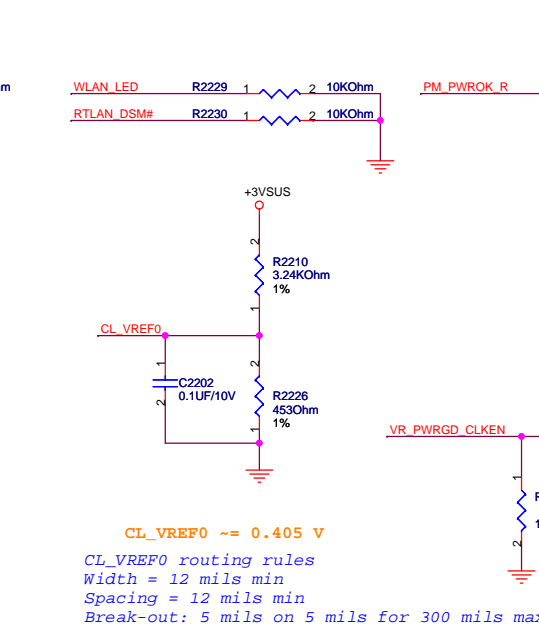
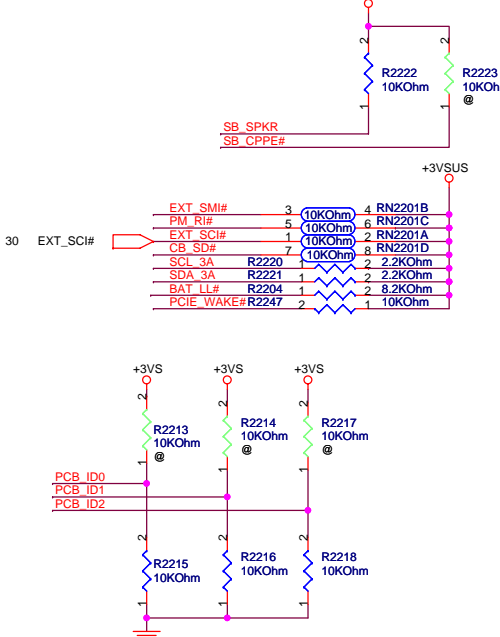
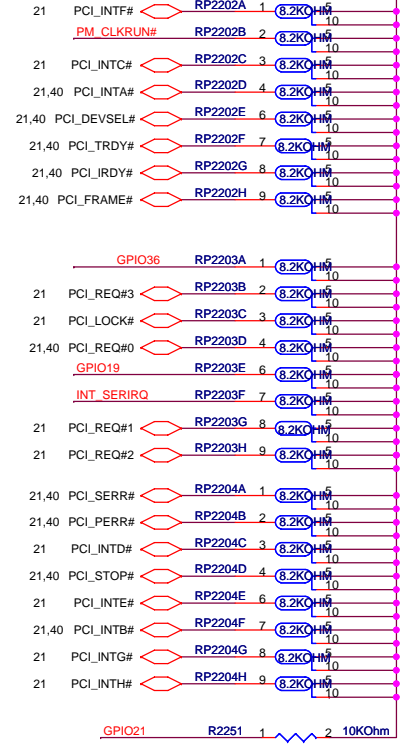
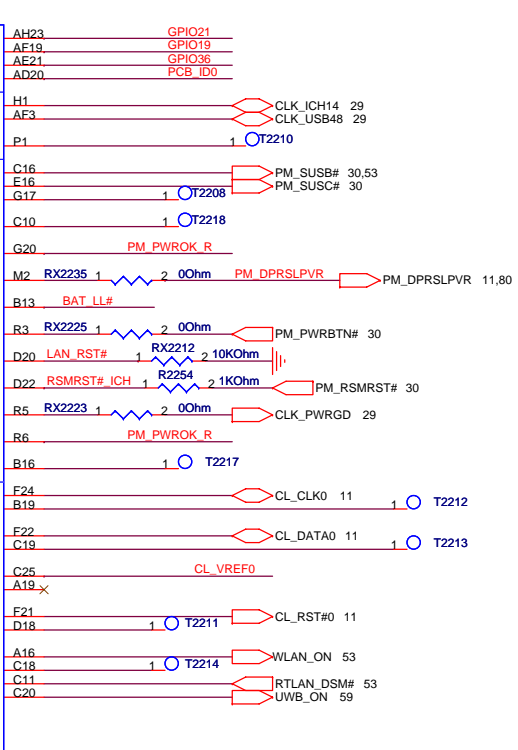
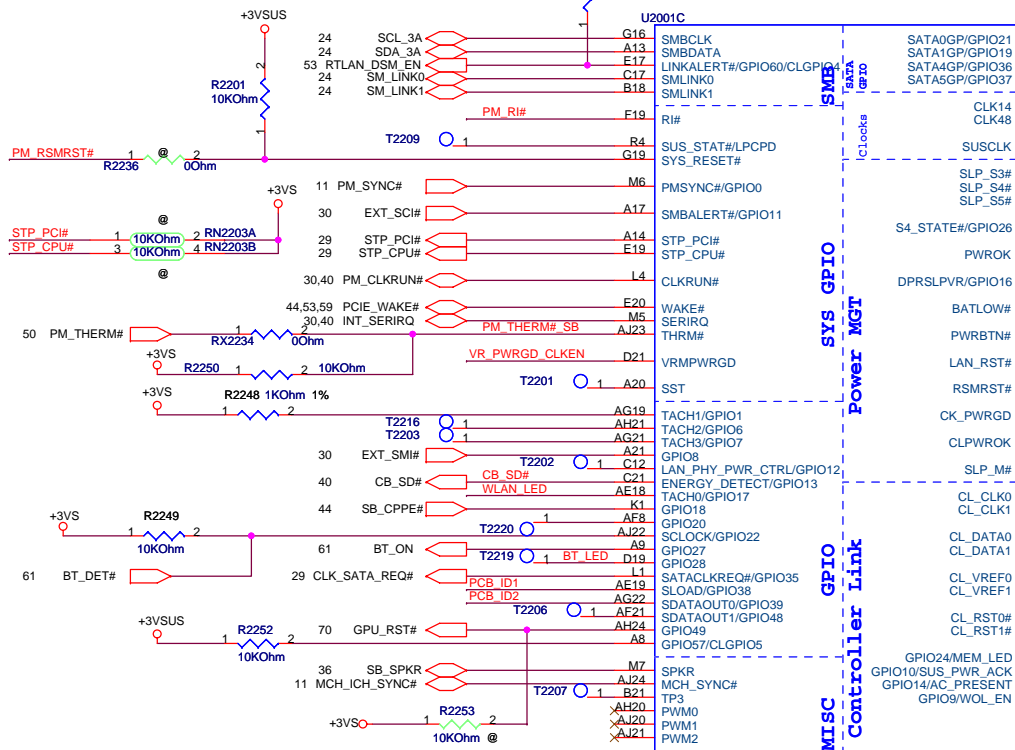
+3VSUS +3VSUS 20,22,23,24,25,30,37,53,81,88,91,92
 +3V +3V 36,42,44,53,57,59,61,91
 +1.5VS_PCIE_ICH +1.5VS_PCIE_ICH 20,23

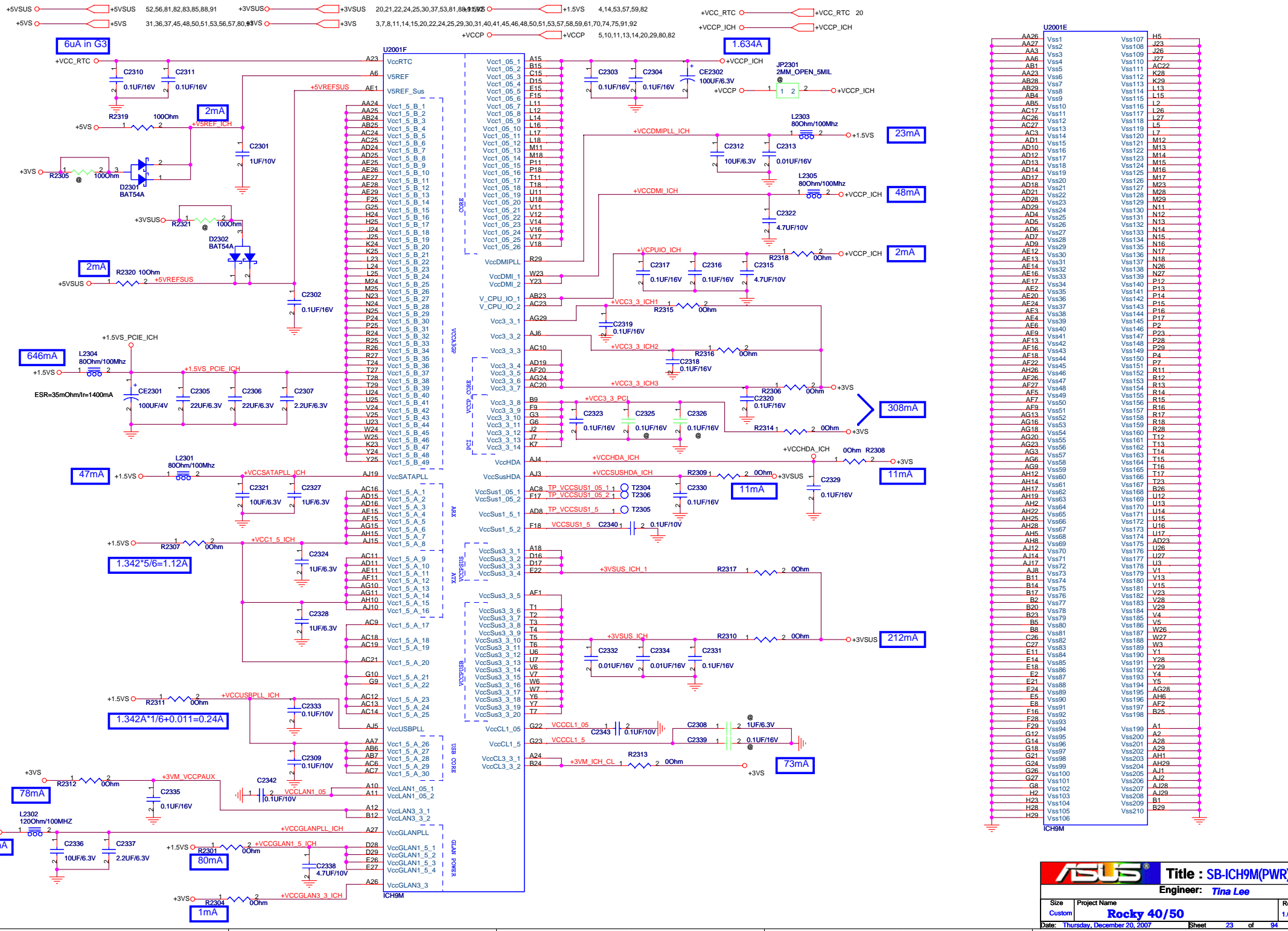


ICH9M Boot BIOS select

| | GNT#0 | CS#1 | (default) |
|-----|-------|------|-----------|
| LPC | 1 | 1 | |
| PCI | 1 | 0 | |
| SPI | 0 | 1 | |

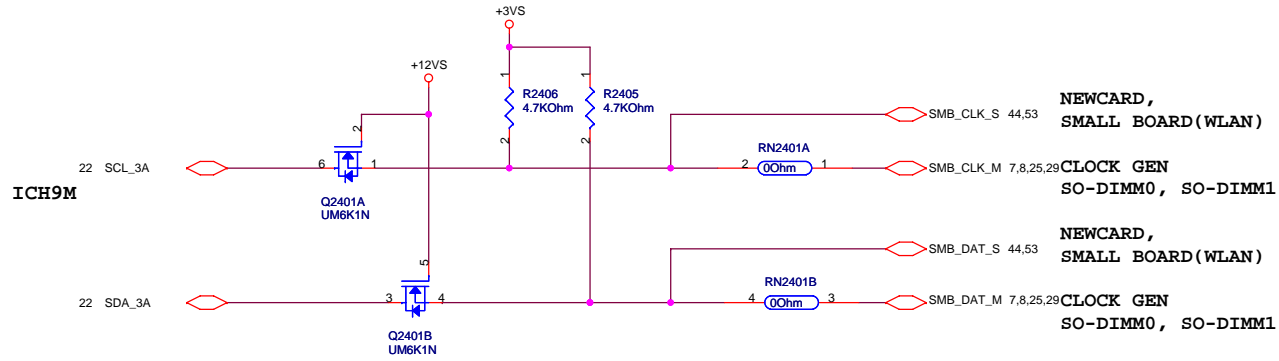
+3VSUS \rightarrow +3VSUS 20,21,23,24,25,30,37,53,81,88,91,92
 +3VS \rightarrow +3VS 3,7,8,11,14,15,20,23,24,25,29,30,31,40,41,45,46,48,50,51,53,57,58,59,61,70,74,75,91,92



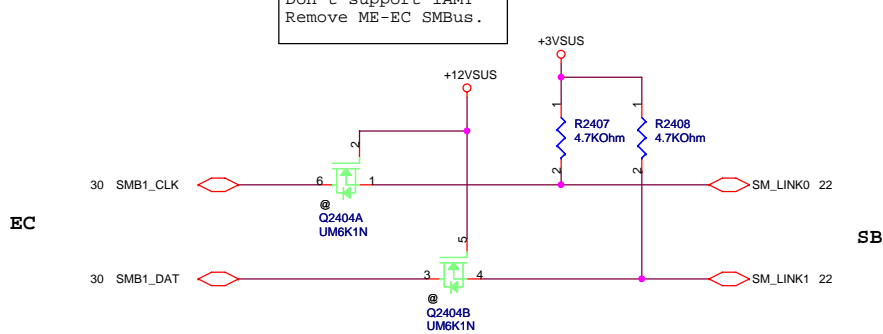


ICH9-M

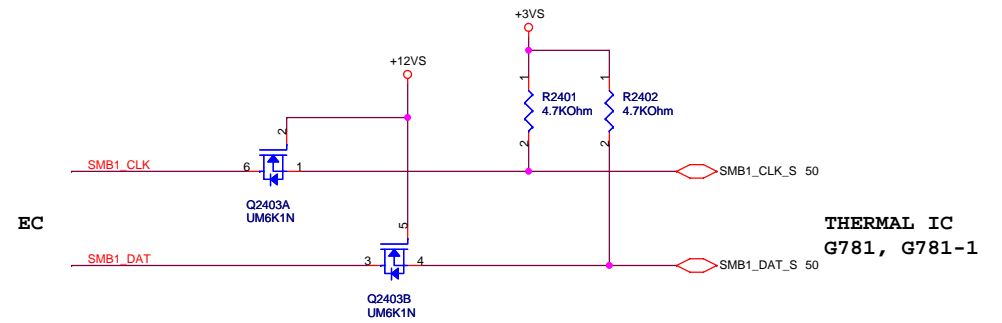
| | | |
|---------|---------|--|
| +12VSUS | +12VSUS | 52,81,91 |
| +12VS | +12VS | 45,91 |
| +3VA | +3VA | 20,30,31,53,57,81 |
| +3VSUS | +3VSUS | 20,21,22,23,25,30,37,53,81,88,91,92 |
| +3VS | +3VS | 3,7,8,11,14,15,20,22,23,25,29,30,31,40,41,45,46,48,50,51,53,57,58,59,61,70,74,75,91,92 |

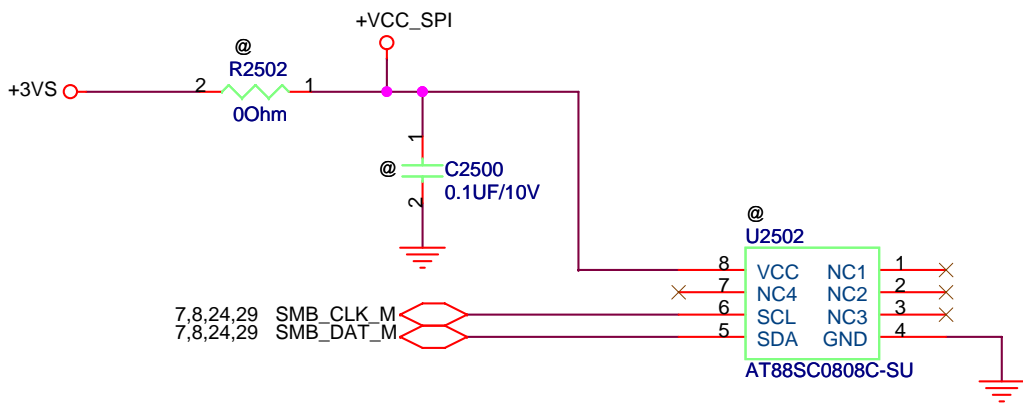
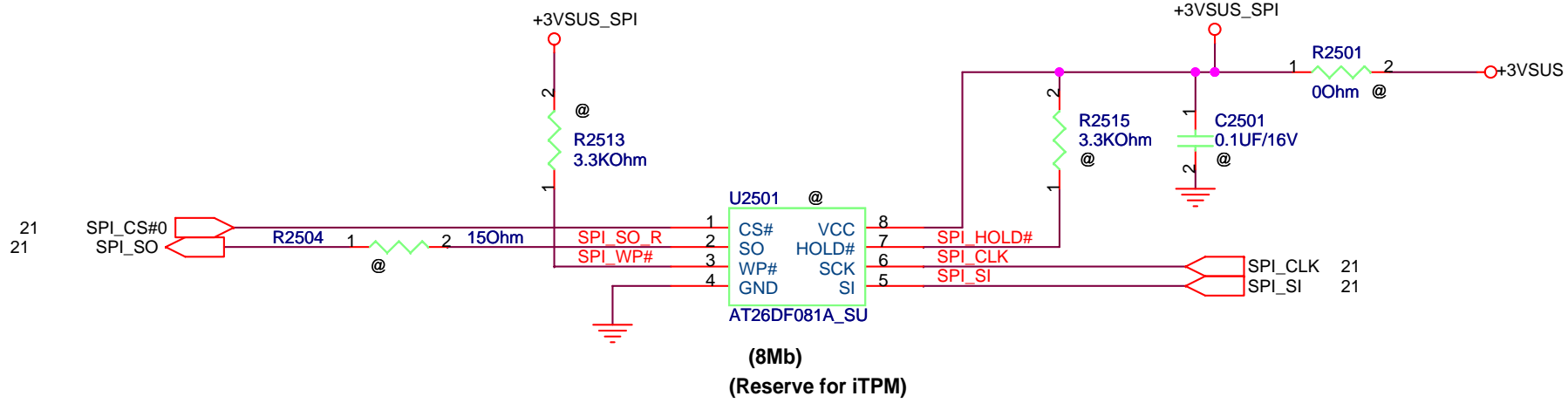


Don't support iAMT
Remove ME-EC SMBus.



EC





| | | |
|-----------------------------------|------------------------------------|---------------------------|
| | | Title : SPI ROM |
| | | Engineer: Tina Lee |
| Size Custom | Project Name Rocky 40/50 | Rev 1.0 |
| Date: Thursday, December 20, 2007 | | Sheet 25 of 94 |

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Engineer: *Tina Lee*

| | | |
|------------|------------------------------------|------------|
| Size A4 | Project Name Rocky 40/50 | Rev 1.0 |
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|  | | Title : | |
| Engineer: <i>Tina Lee</i> | | | |
| Size | Project Name | | Rev |
| A4 | Rocky 40/50 | | 1.0 |
| Date: Monday, December 17, 2007 | | Sheet | 27 of 94 |

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|---|--------------------|----------------------------------|------------------------|
|  | | Title : | |
| | | Engineer: <i>Tina Lee</i> | |
| Size | Project Name | Rev | |
| A4 | Rocky 40/50 | 1.0 | |
| Date: Monday, December 17, 2007 | | Sheet | 28 of 94 |

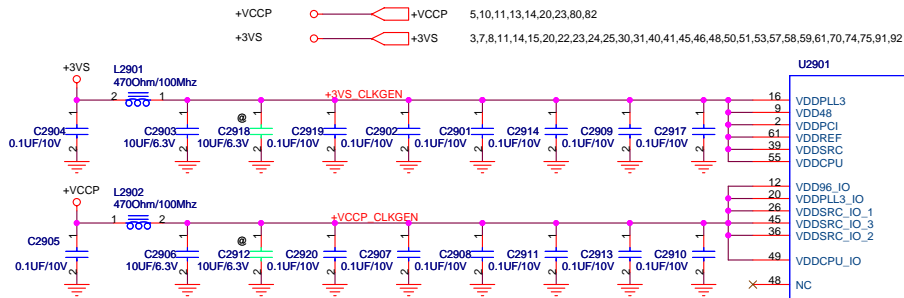
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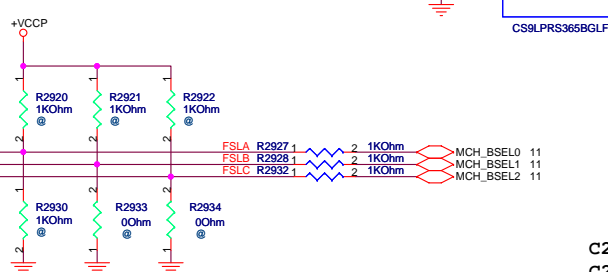
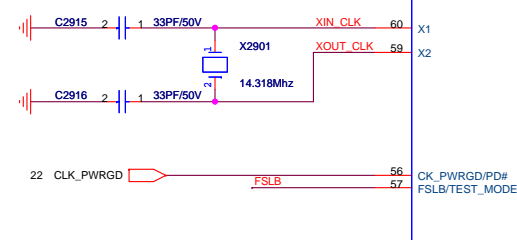
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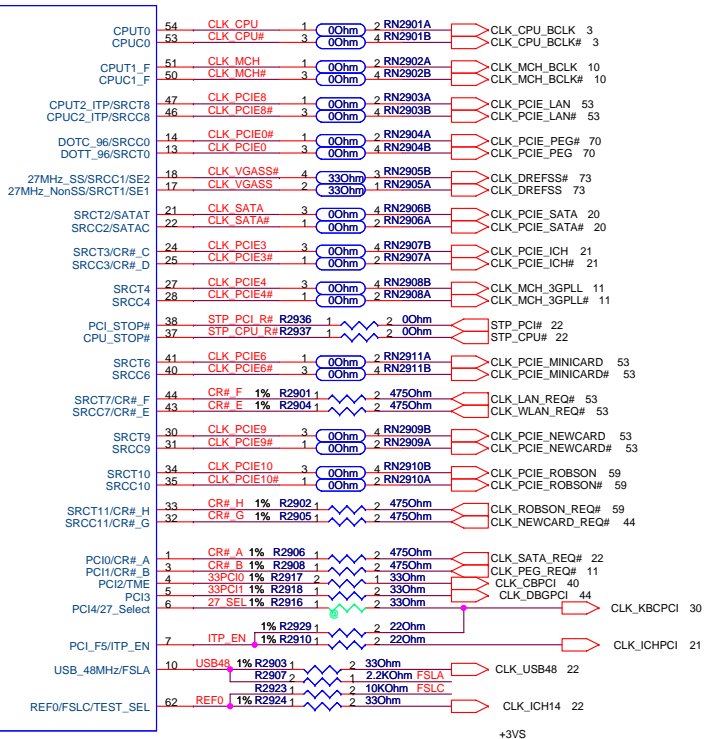
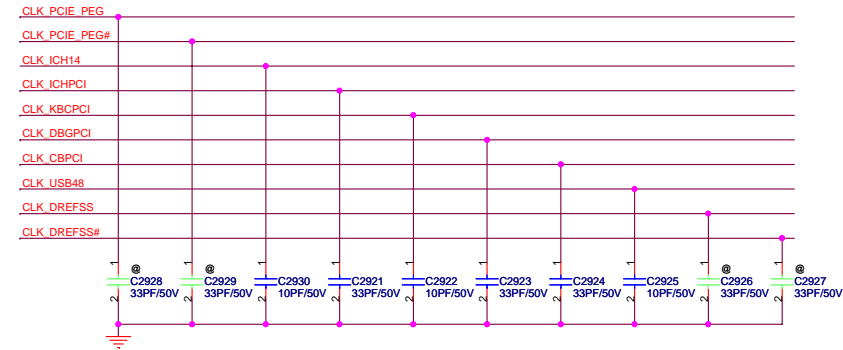


C2917, C2918, C2919 near CLK Gen.



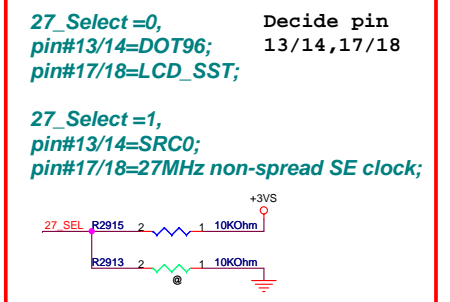
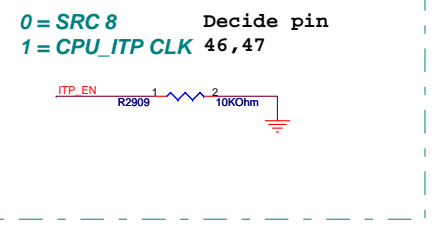
| | FSLC | FSLB | FSLA |
|-------|------|------|------|
| BCLK | 667 | 0 | 1 |
| FSB | 0 | 1 | 1 |
| BSEL2 | 0 | 1 | 0 |
| BSEL1 | 0 | 1 | 0 |
| BSEL0 | 0 | 0 | 0 |

C2921, C2922, C2923, C2924, C2925, C2926, C2927, C2928, C2929, C2930 near CLK Gen.

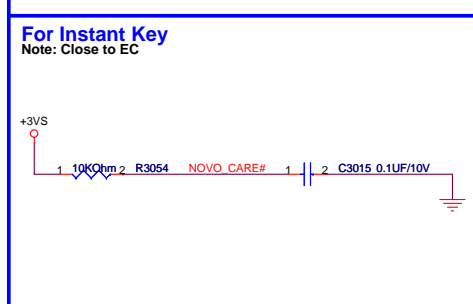
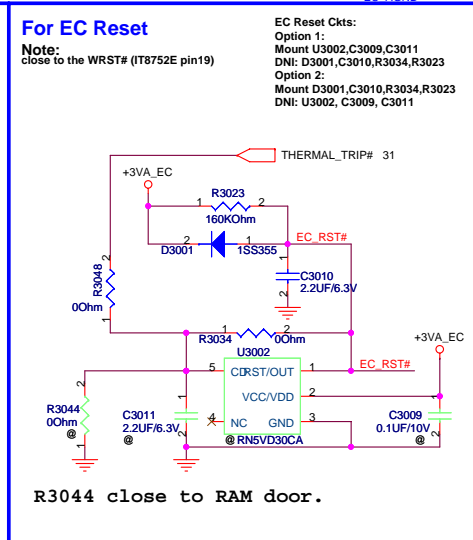
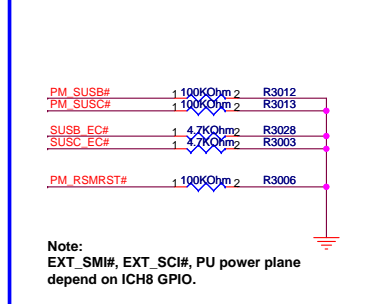
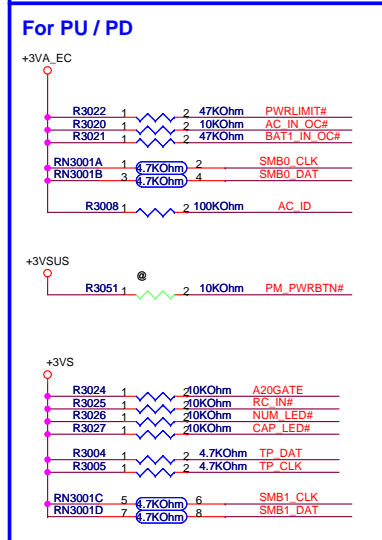
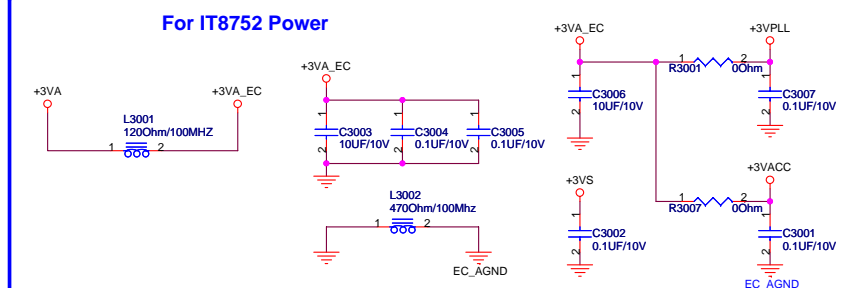
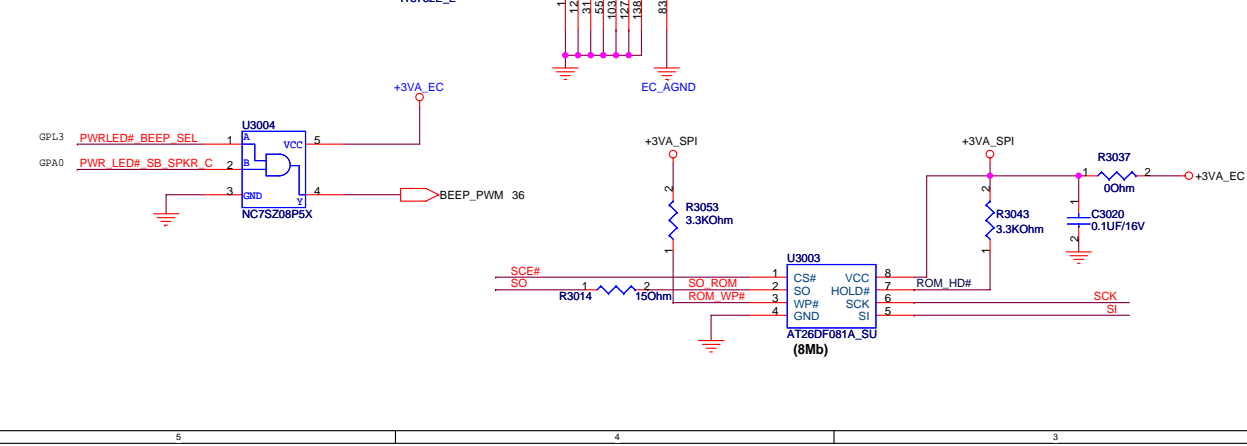
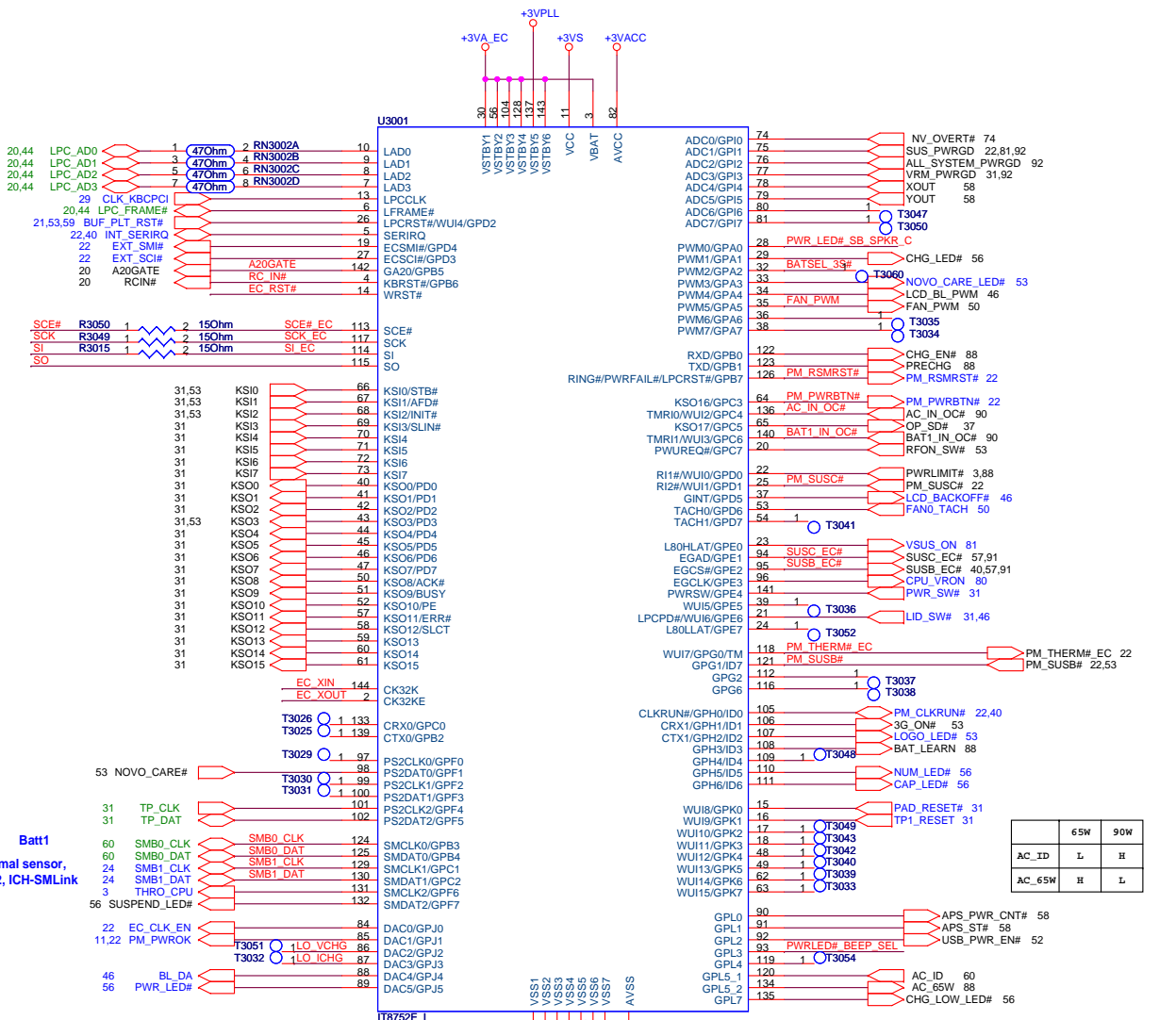


| CR# | A | B | C | D | E | F | G | H |
|-----|-----------|----------|---|---|---|---|---|---|
| | 0 = SRC 0 | | | | | | | |
| | 1 = SRC 2 | SATA | | | | | | |
| | 0 = SRC 1 | | | | | | | |
| | 1 = SRC 4 | MCH | | | | | | |
| | 0 = SRC 0 | | | | | | | |
| | 1 = SRC 2 | | | | | | | |
| | 0 = SRC 1 | | | | | | | |
| | 1 = SRC 4 | | | | | | | |
| | SRC 6 | WLAN | | | | | | |
| | SRC 8 | LAN | | | | | | |
| | SRC 9 | New Card | | | | | | |
| | SRC 10 | Robson | | | | | | |

Latched Input Select



For GM/GL, need to PD for 96MHz output.
For PM, need to PU for 27MHz output.



For EC Hardware Strap

I/O Base Address
 Note: It can be programmable by EC firmware
 Share Memory
 Note: It can be programmable by EC firmware.
 PP Enable
 Note: Default Int. Pull-Down

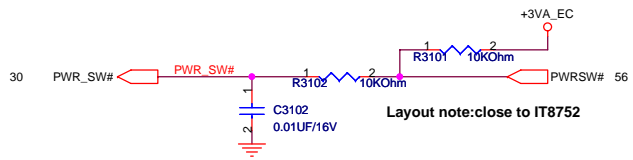
| | | |
|--------|--------------|-----|
| Size | Project Name | Rev |
| Custom | Rocky 40/50 | 1.0 |

Date: Thursday, December 20, 2007 Sheet 30 of 94

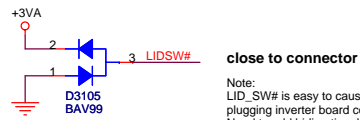
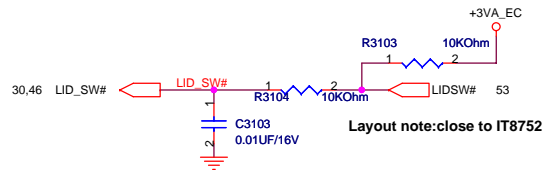
| | | | |
|--------|---|-----|-----|
| | | 65W | 90W |
| AC_ID | L | H | |
| AC_65W | H | L | |

For Switch

PWR SWITCH

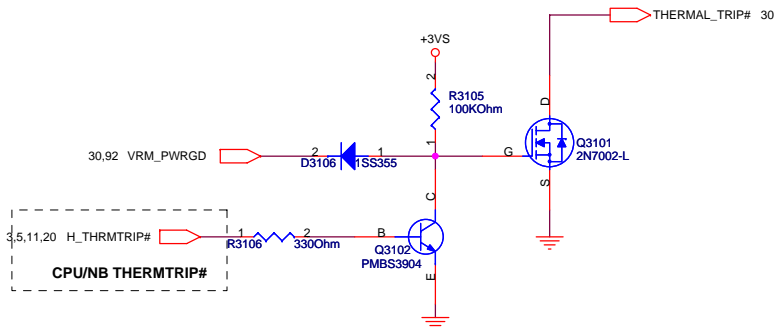


LID SWITCH

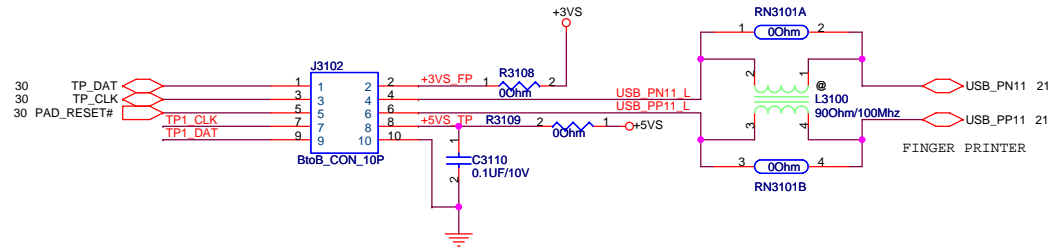


Note:
LID_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. Need to add bidirectional diode to protect this pin.

For Thermal Control Method

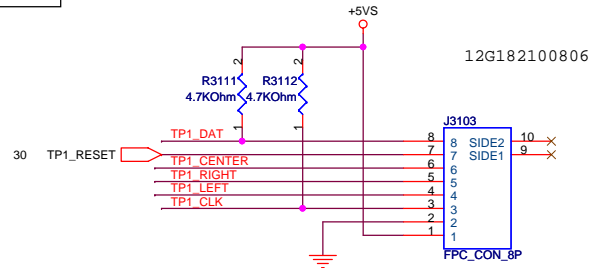


TOUCH PAD CONN

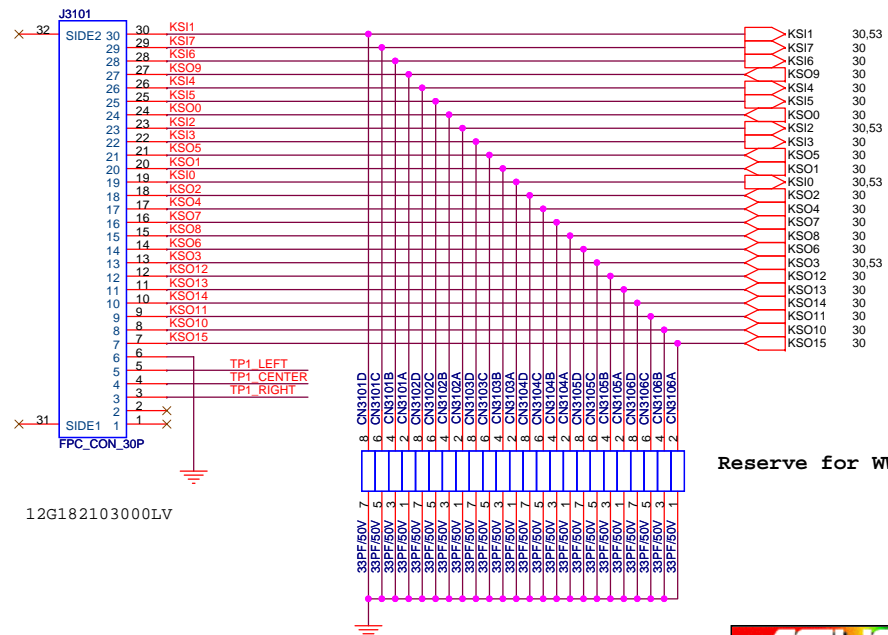


TP : Touch Pad
TP1: Track Point

TRACK POINT CONN



Keyboard Connector



Reserve for WWAN

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Engineer: *Tina Lee*

| | | |
|------------|------------------------------------|------------|
| Size A4 | Project Name Rocky 40/50 | Rev 1.0 |
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|---|---------------------------|---------------------|----------|
|  | | Title :***** | |
| Engineer: Tina Lee | | | |
| Size | Project Name | | Rev |
| A4 | Rocky 40/50 | | 1.0 |
| Date: | Monday, December 17, 2007 | Sheet | 33 of 94 |

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 **Title :** ****

Engineer: *Tina Lee*

| | | |
|------------|------------------------------------|------------|
| Size A4 | Project Name Rocky 40/50 | Rev 1.0 |
|------------|------------------------------------|------------|

Date: **Monday, December 17, 2007** Sheet **34** of **94**

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|  | | Title : MDC |
|---|--|--------------------|

Engineer: Tina Lee

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|------------|------------------------------------|------------|
| Size A4 | Project Name Rocky 40/50 | Rev 1.0 |
|------------|------------------------------------|------------|

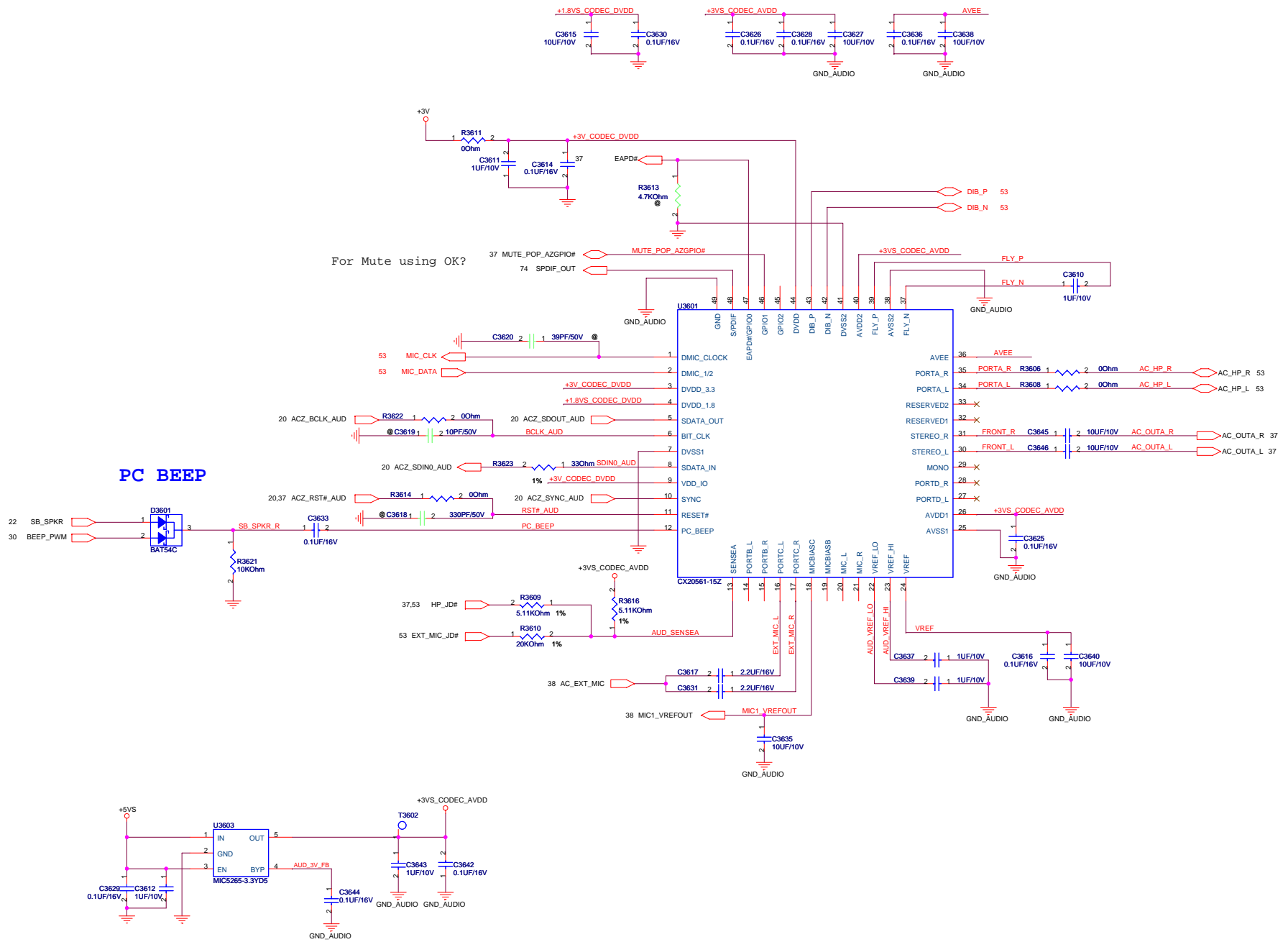
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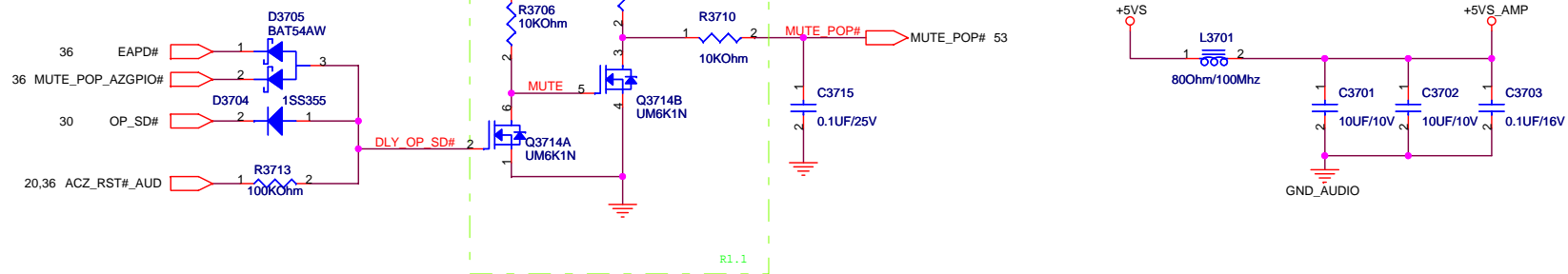
1



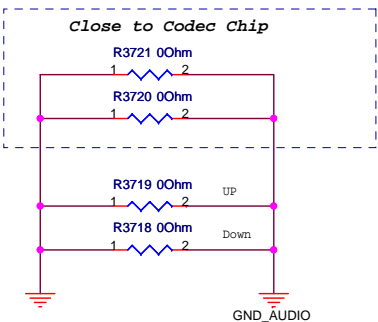
PC BEEP

For Mute using OK?

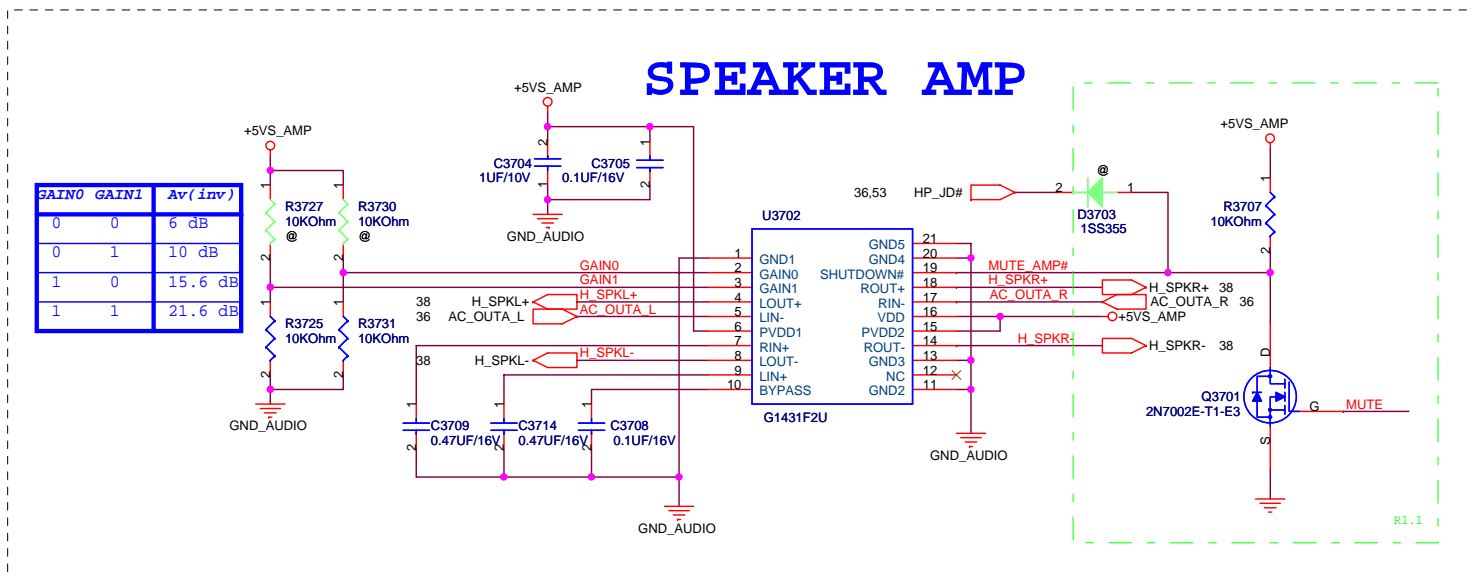
DePOP Circuit



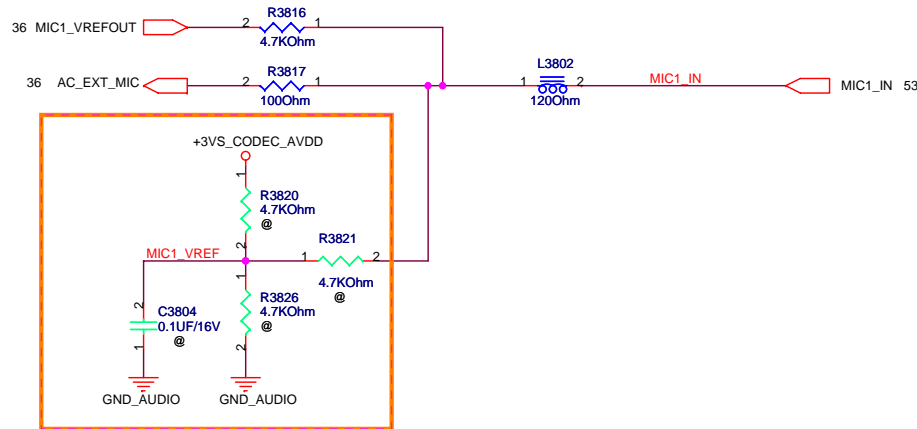
JACK GND



SPEAKER AMP

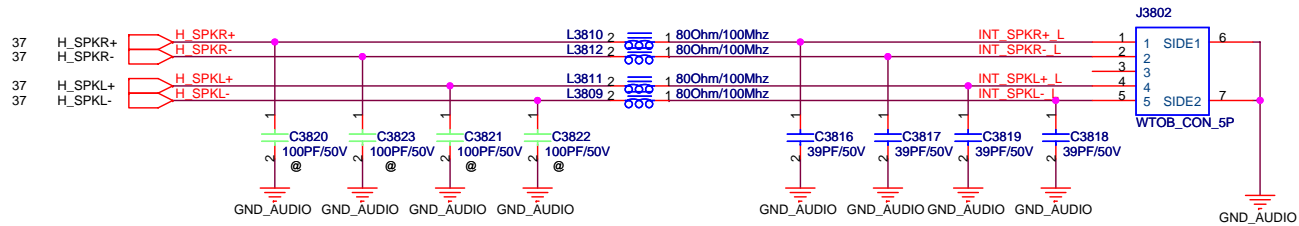


EXT MICROPHONE

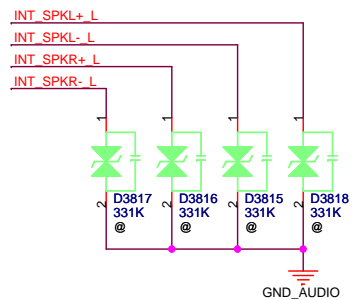


Reserved the external MIC bias(T filter).

SPEAKER CONNECTOR



12G171010050LV
ACES/87213-0500G



| | | | |
|-----------------------------------|------------------------------------|-------------------------------|----------|
| | | Title : MIC&LINEIN | |
| | | Engineer: <i>Tina Lee</i> | |
| Size Custom | Project Name Rocky 40/50 | Rev 1.0 | |
| Date: Thursday, December 20, 2007 | | Sheet | 38 of 94 |

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Engineer: Tina Lee

| | | |
|------------|------------------------------------|------------|
| Size A4 | Project Name Rocky 40/50 | Rev 1.0 |
|------------|------------------------------------|------------|

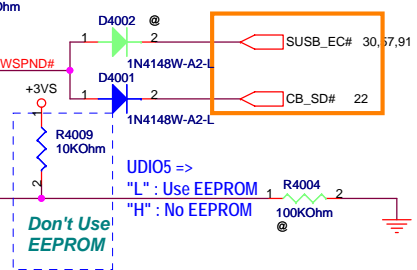
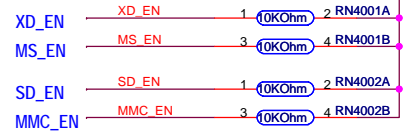
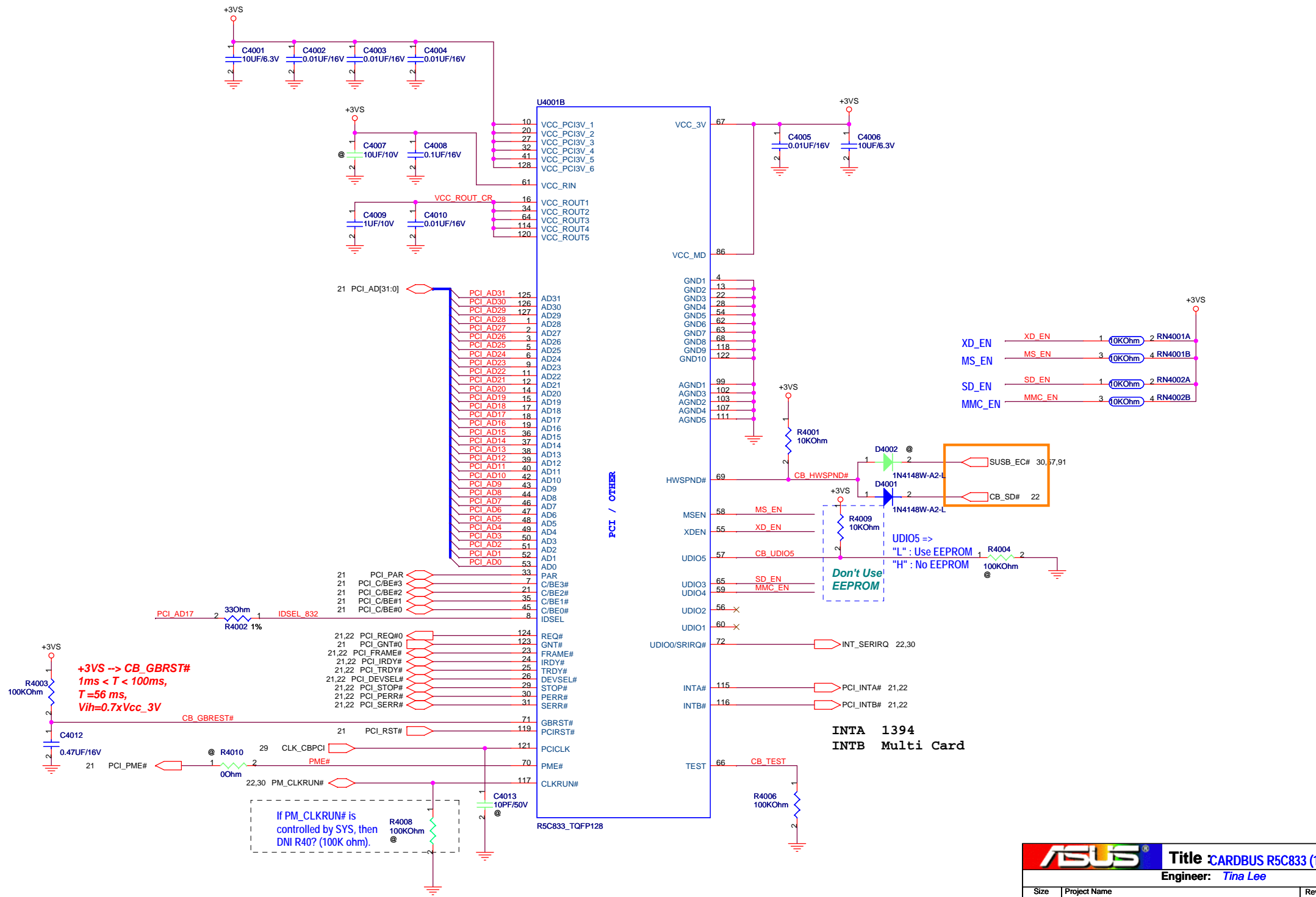
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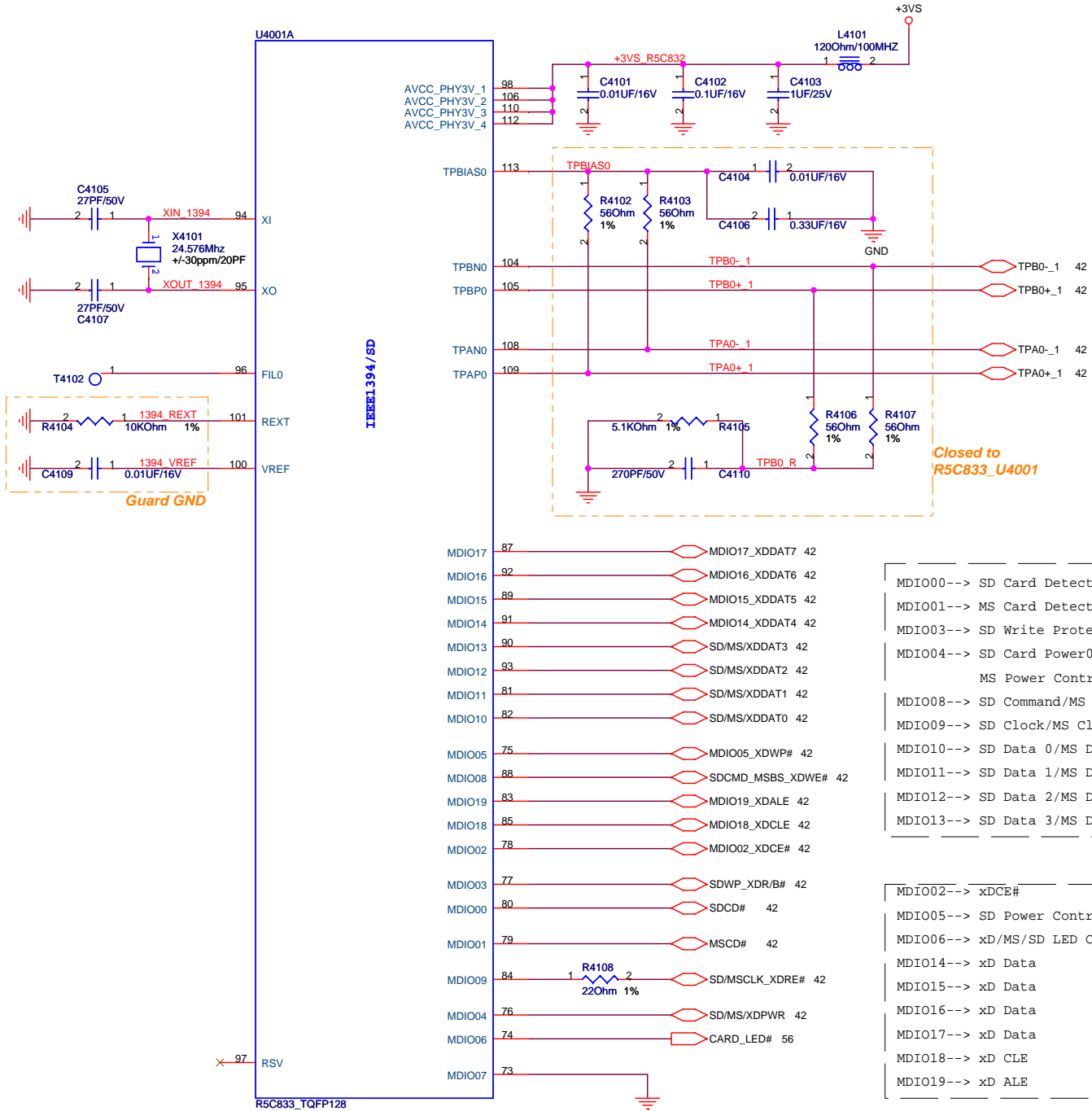


UDIO5 =>
 "L" : Use EEPROM
 "H" : No EEPROM

INTA 1394
 INTB Multi Card

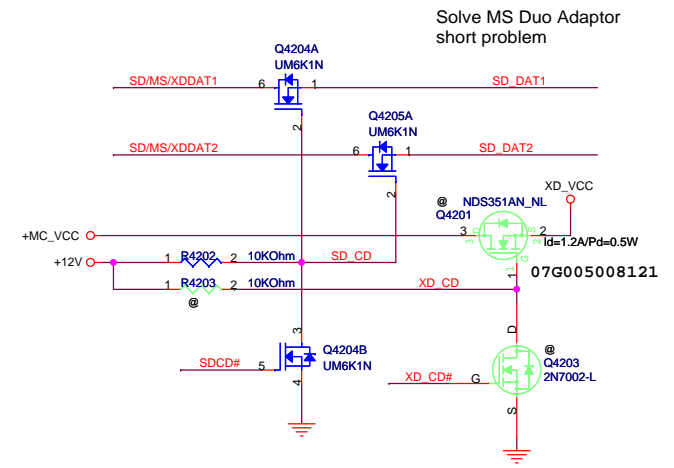
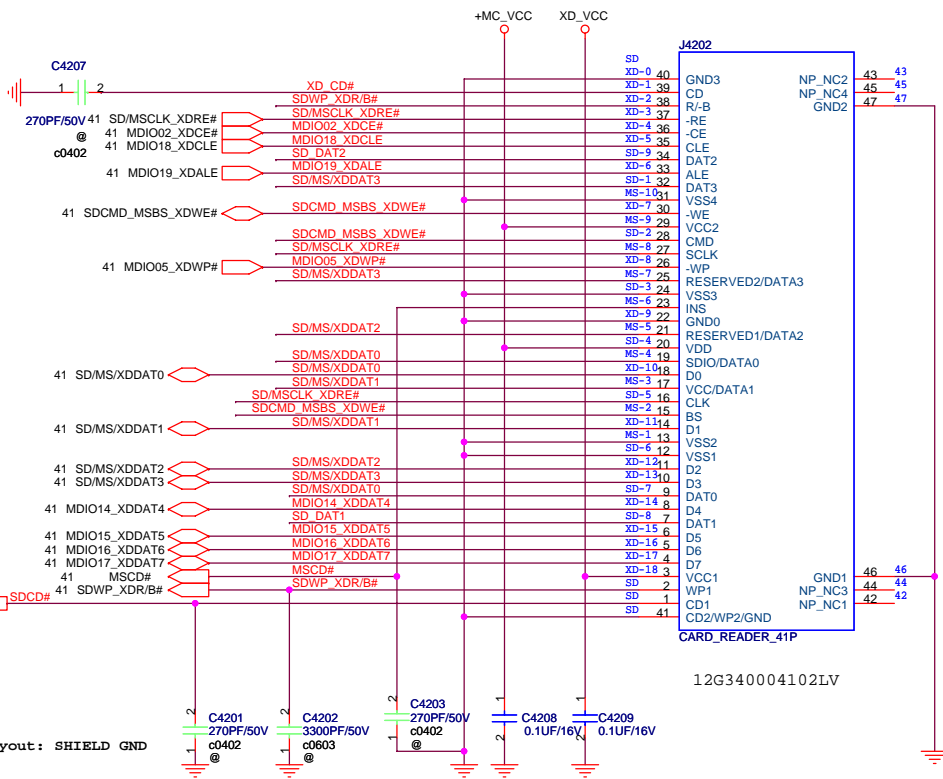
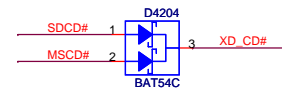
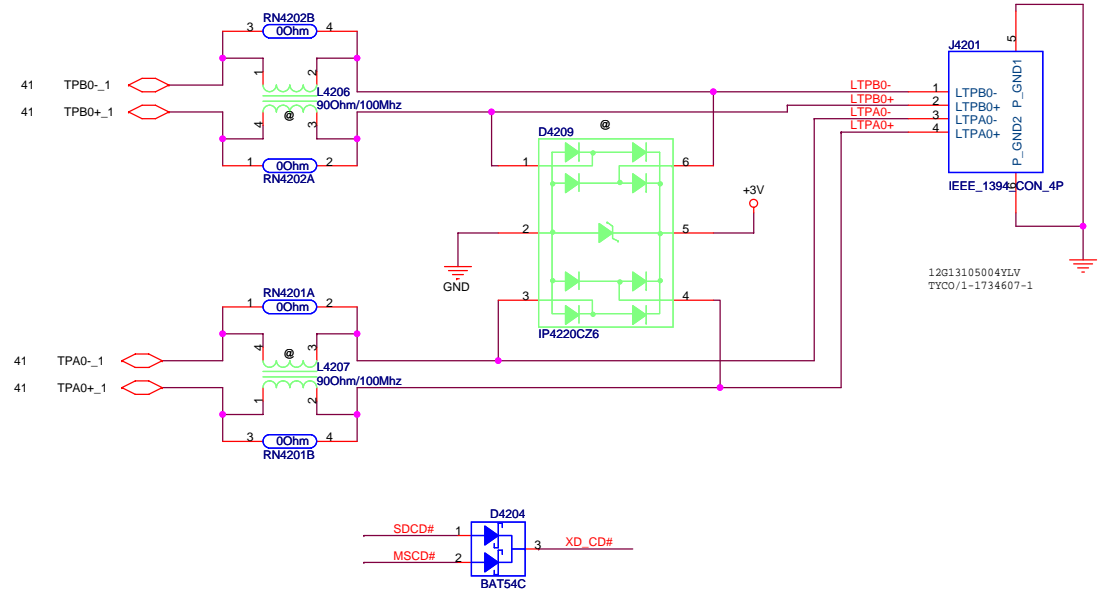
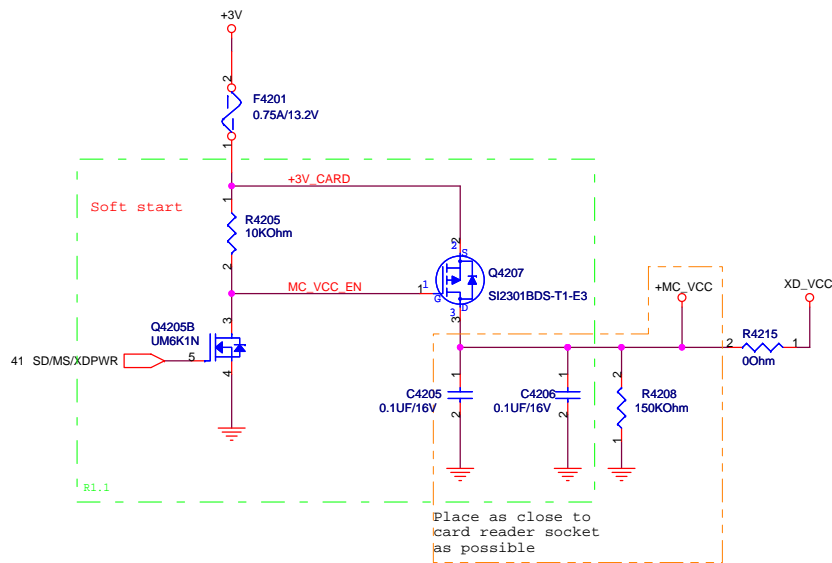
If PM_CLKRUN# is controlled by SYS, then DNI R40? (100K ohm).

+3VS --> CB_GBRST#
 1ms < T < 100ms,
 T=56 ms,
 Vih=0.7xVcc_3V



MDIO00--> SD Card Detect
 MDIO01--> MS Card Detect
 MDIO03--> SD Write Protect
 MDIO04--> SD Card Power0 Control/
 MS Power Control
 MDIO08--> SD Command/MS Bus State
 MDIO09--> SD Clock/MS Clock
 MDIO10--> SD Data 0/MS Data 0
 MDIO11--> SD Data 1/MS Data 1
 MDIO12--> SD Data 2/MS Data 2
 MDIO13--> SD Data 3/MS Data 3

MDIO02--> xDCE#
 MDIO05--> SD Power Control 1 / xDWP
 MDIO06--> xD/MS/SD LED Control
 MDIO14--> xD Data
 MDIO15--> xD Data
 MDIO16--> xD Data
 MDIO17--> xD Data
 MDIO18--> xD CLE
 MDIO19--> xD ALE



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Engineer: *Tina Lee*

| | | |
|------------|------------------------------------|------------|
| Size A4 | Project Name Rocky 40/50 | Rev 1.0 |
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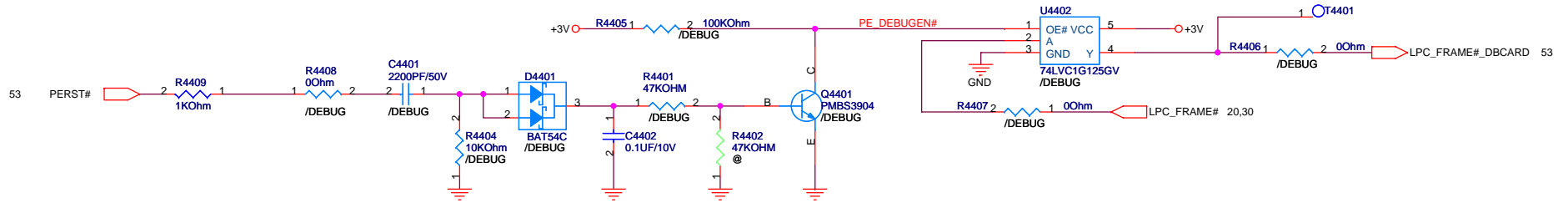
4

3

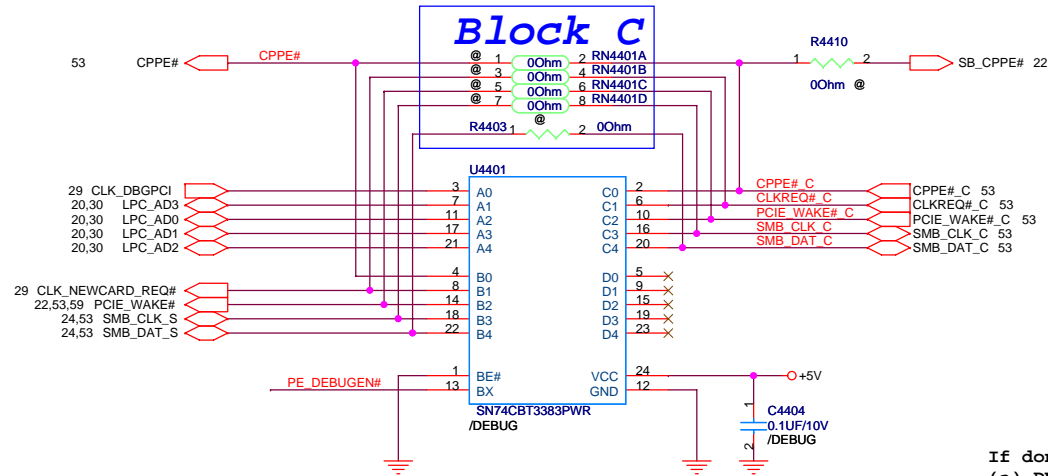
2

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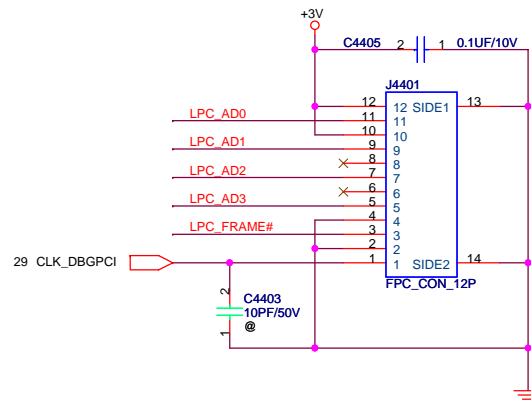
Block A

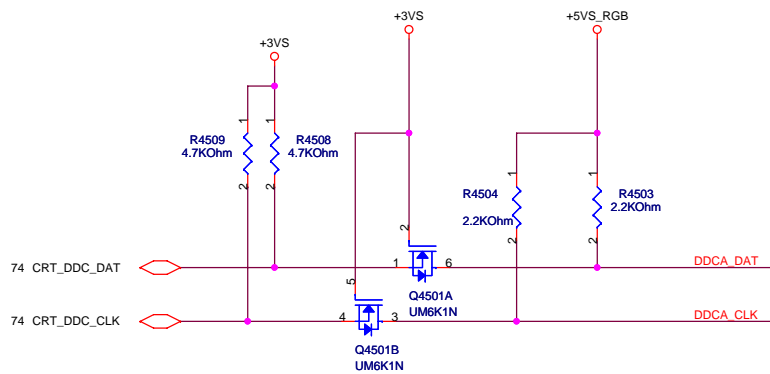
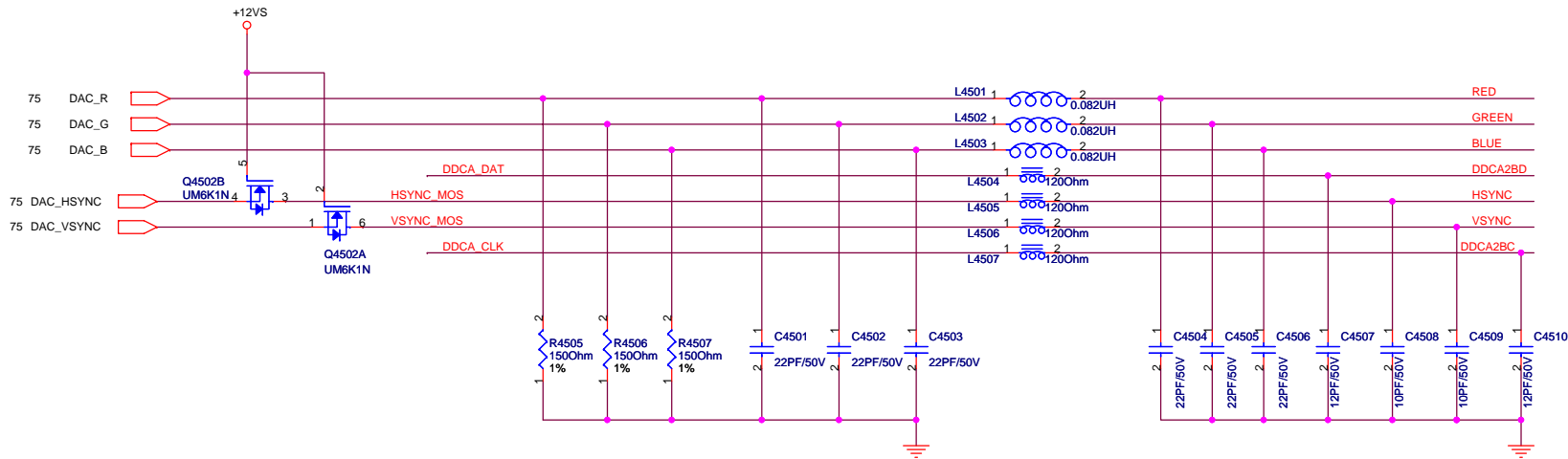


Block C

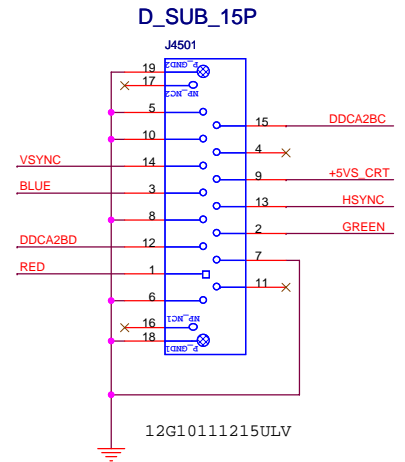
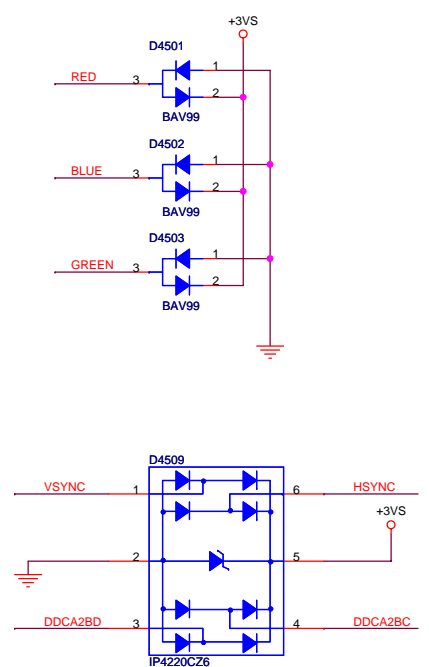


If don't support NewCard Debug Card,Pls do
 (a) DNI all components of block A
 (b) Mount Block C (RN5401,R6975)

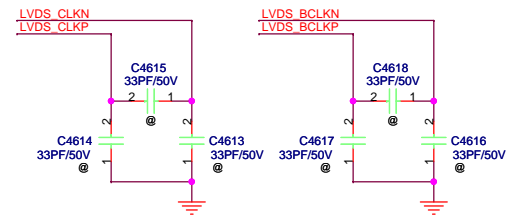
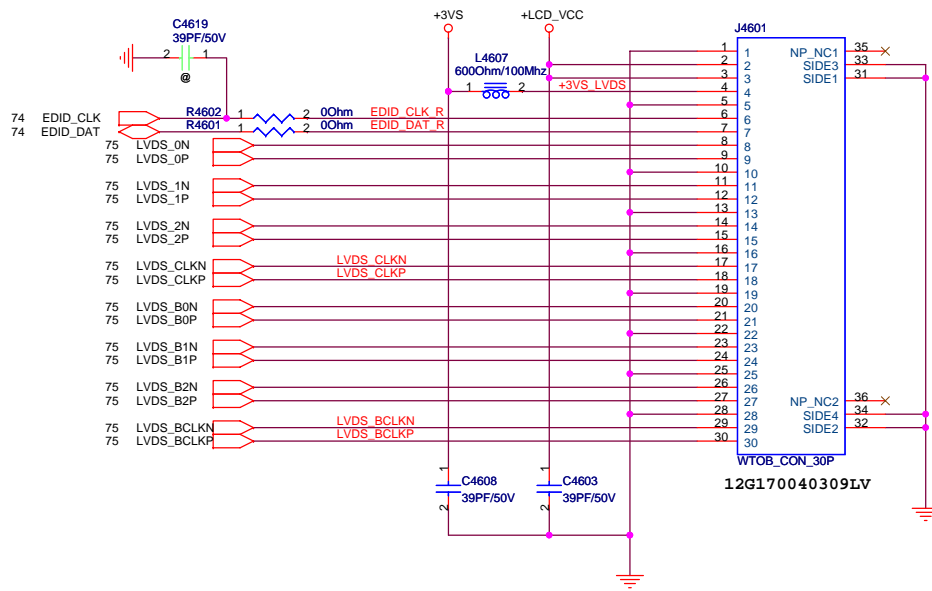




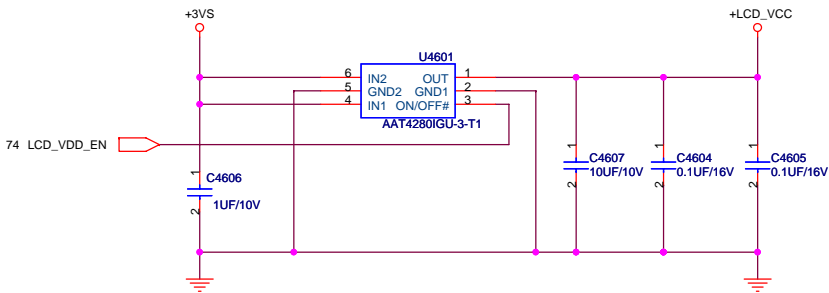
PLACE ESD Diodes near VGA port



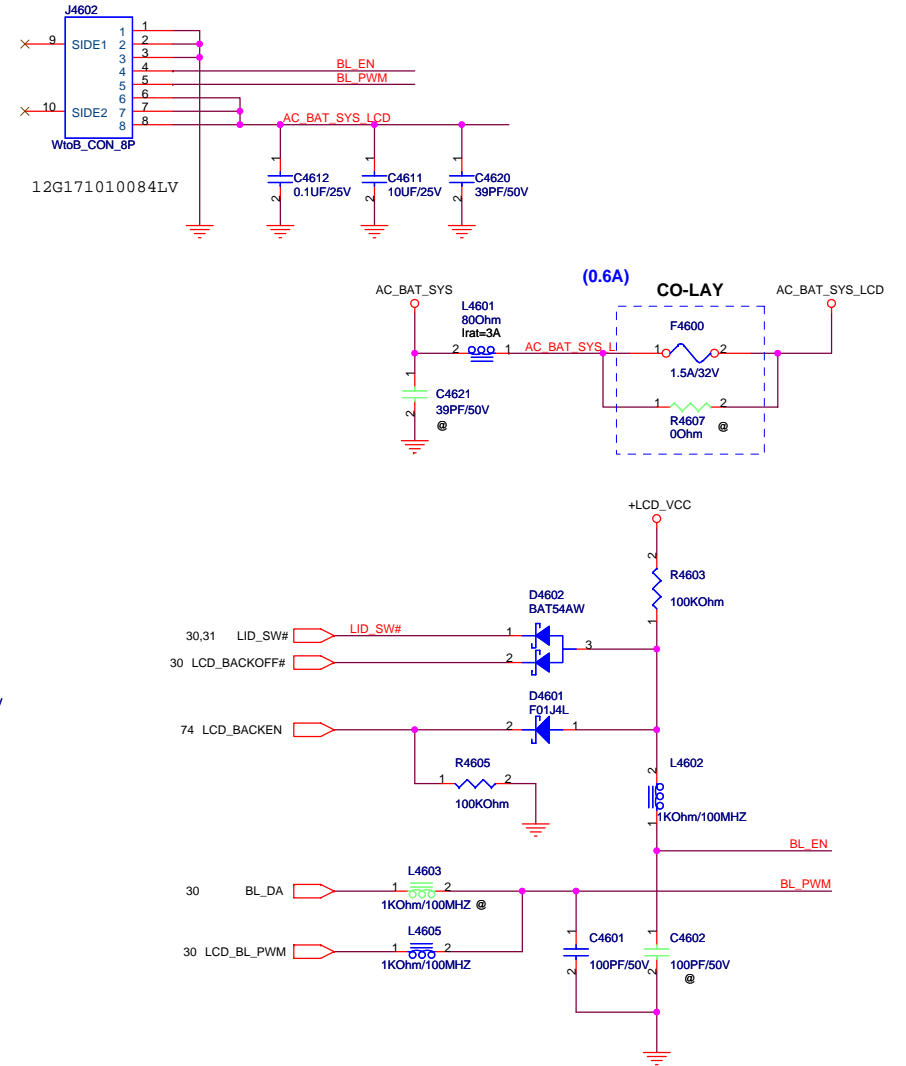
LVDS CNT



Power Switch for LCD Power



INVERTER CNT



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Engineer: *Tina Lee*

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| Size A4 | Project Name Rocky 40/50 | Rev 1.0 |
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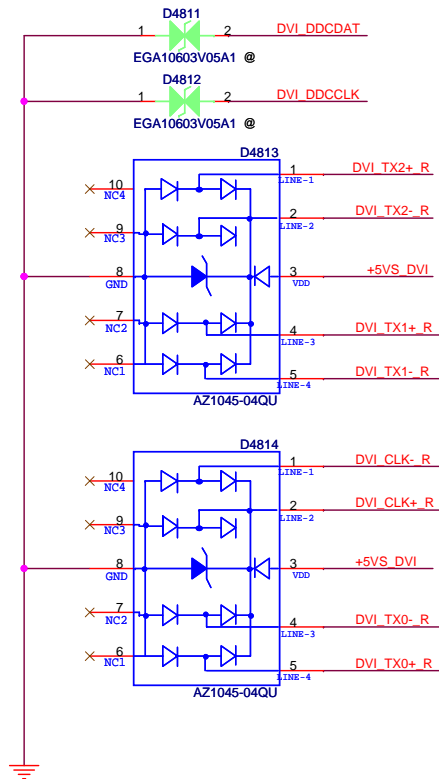
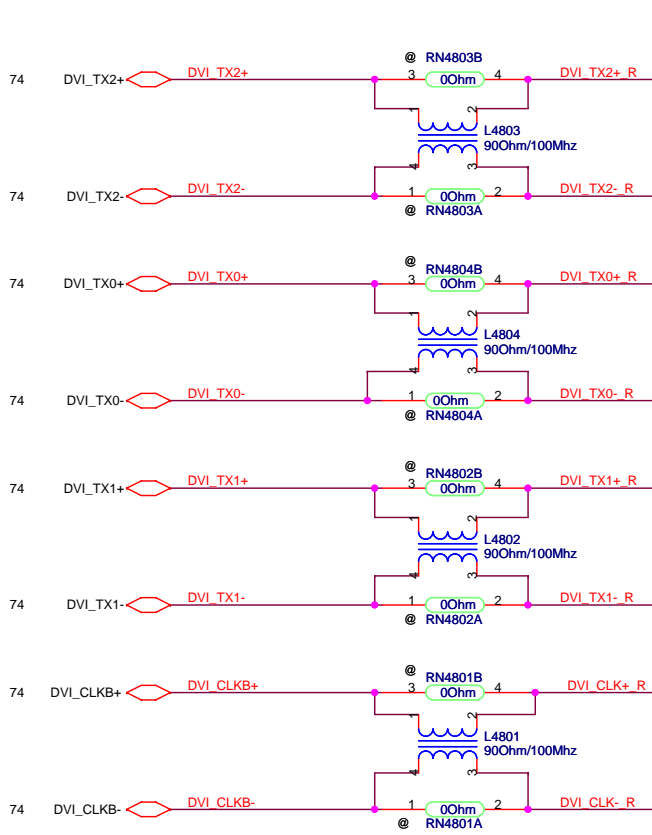
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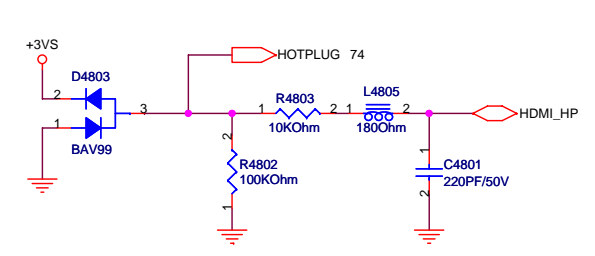
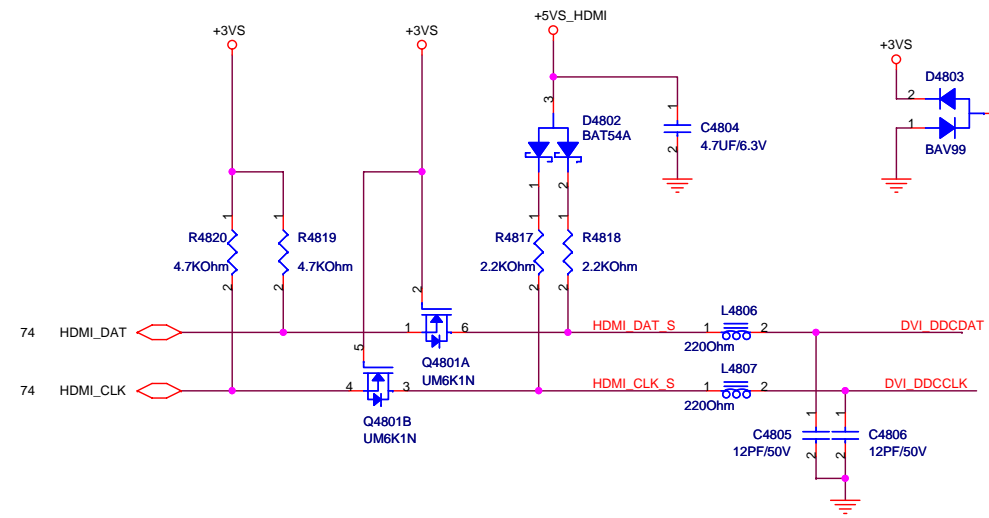
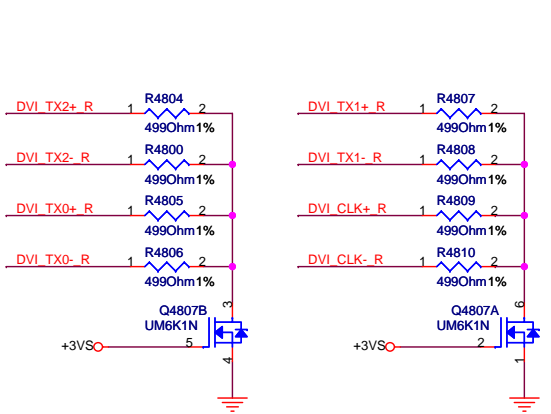
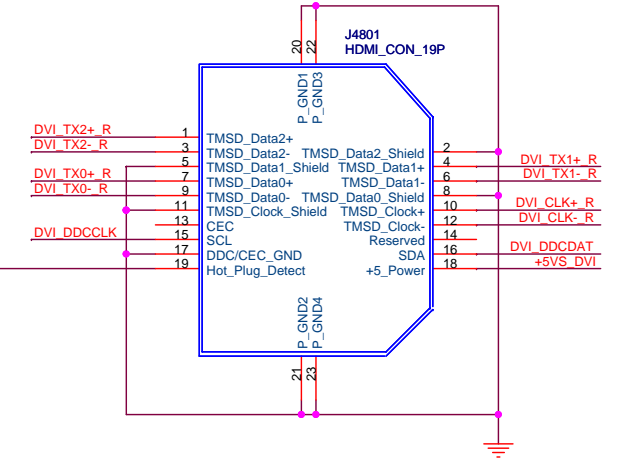
2

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HDMI CNT

12G241101935LV



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Engineer: *Tina Lee*

| | | |
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| Size A4 | Project Name Rocky 40/50 | Rev 1.0 |
|------------|------------------------------------|------------|

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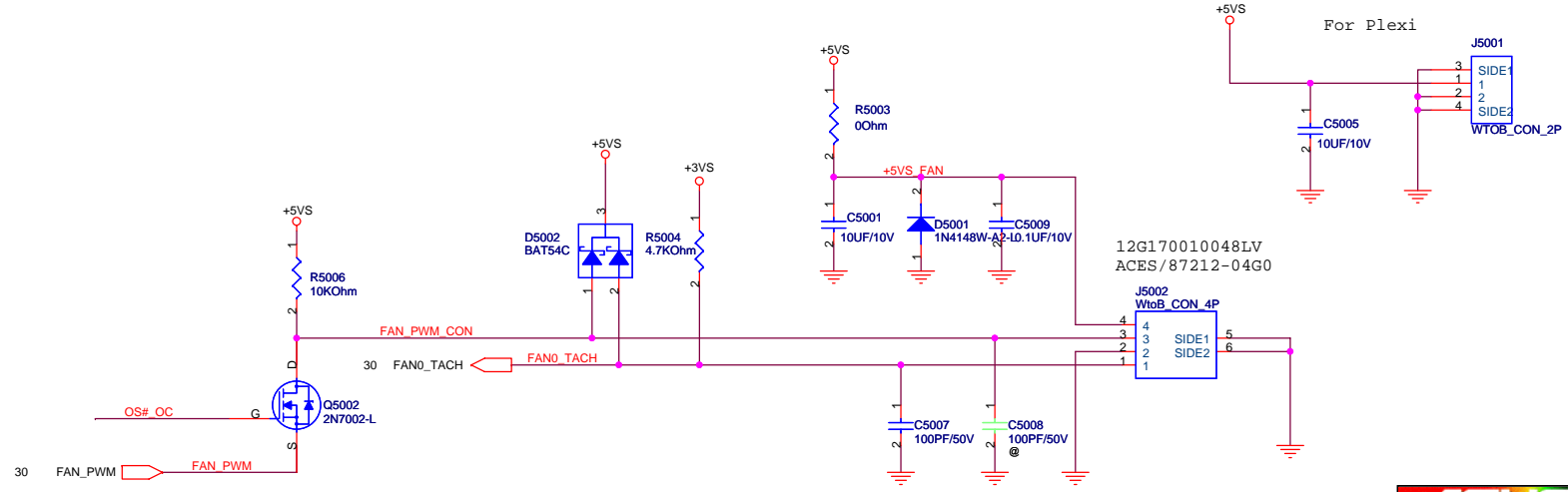
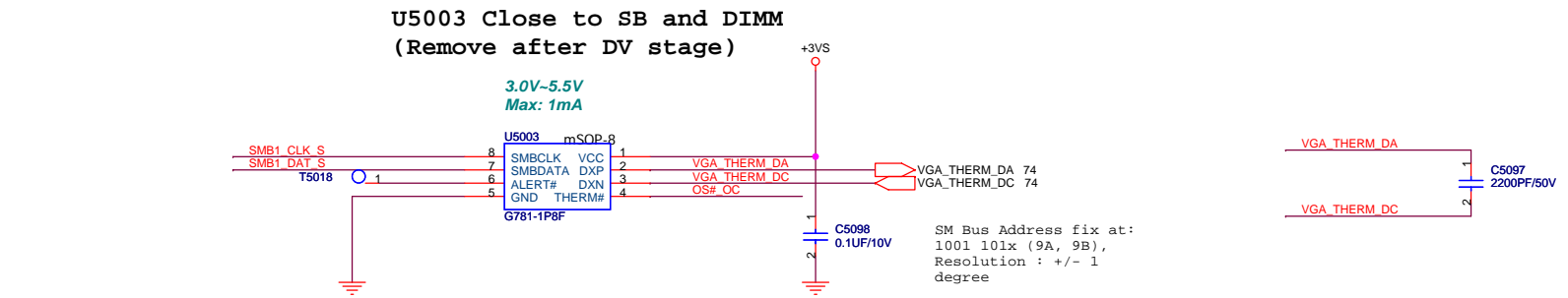
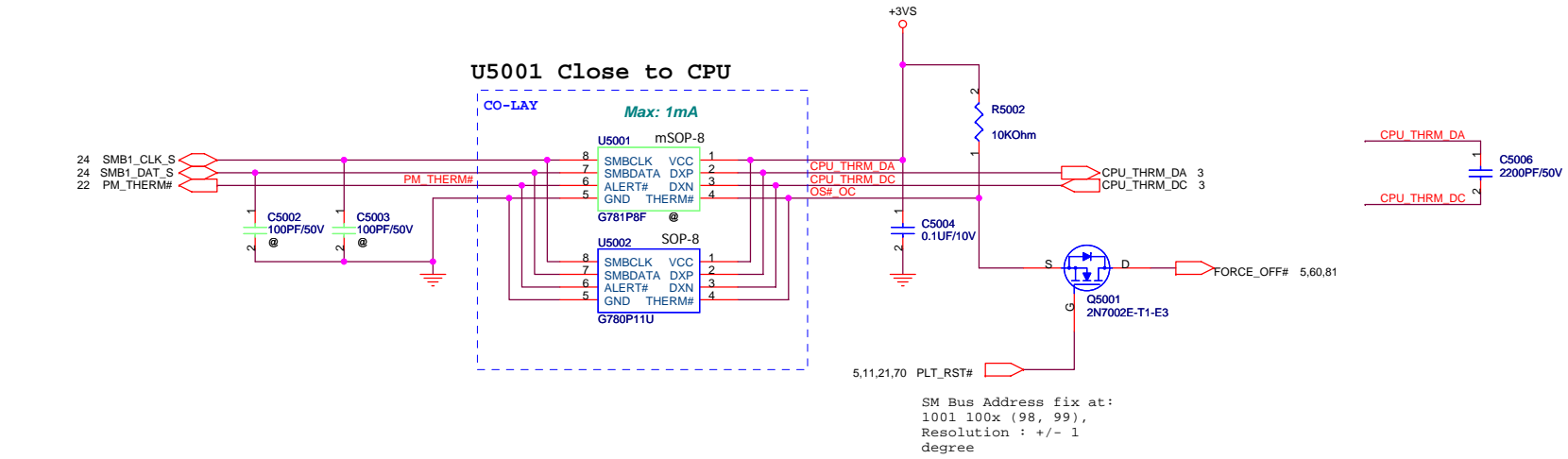
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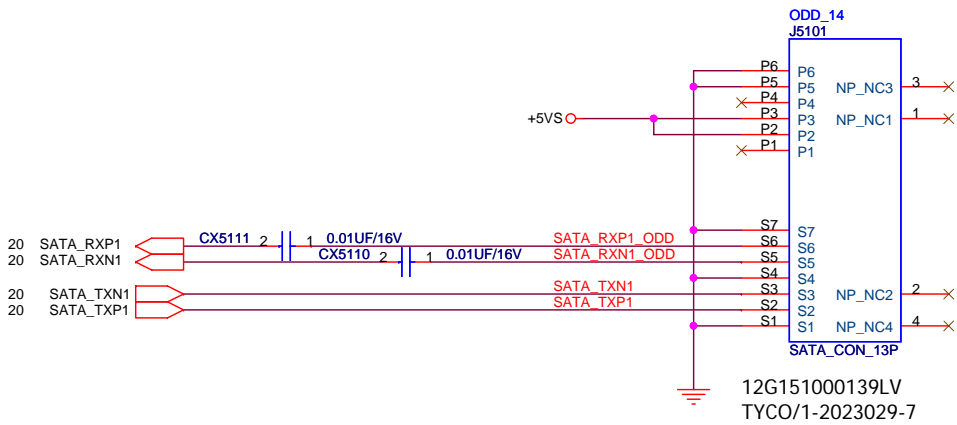
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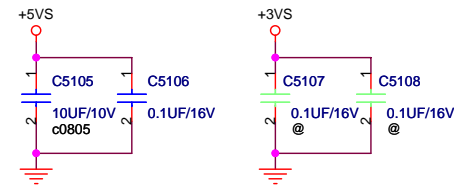
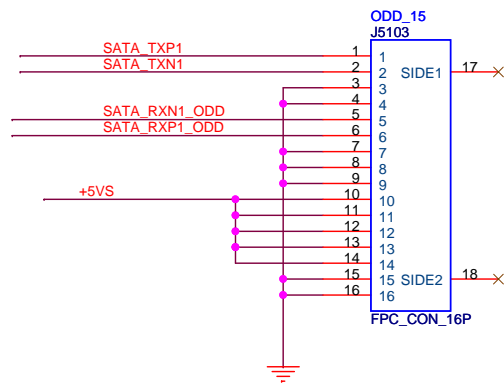
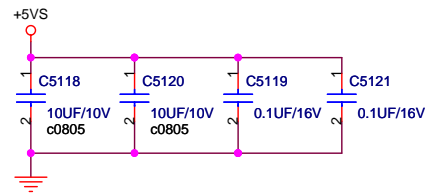
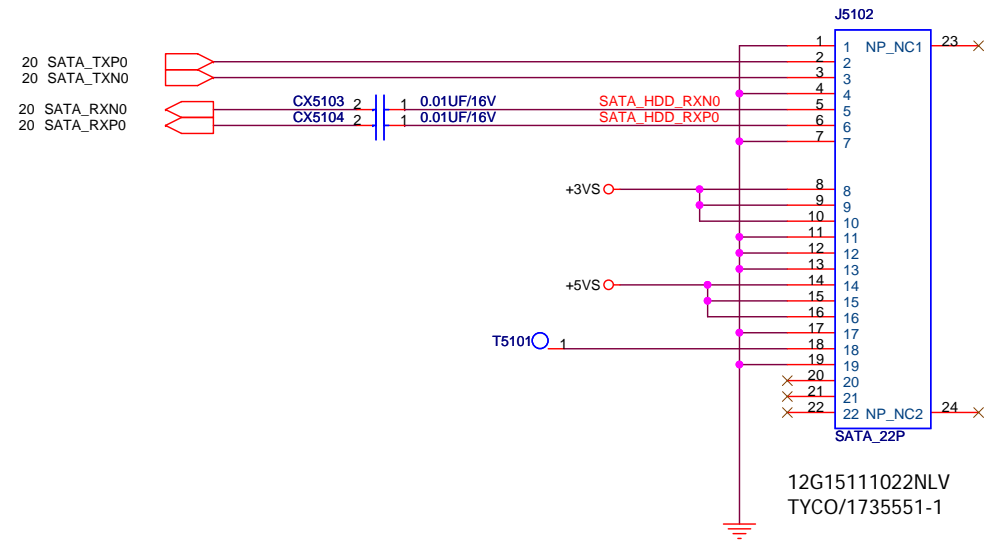
Thermal Sensor

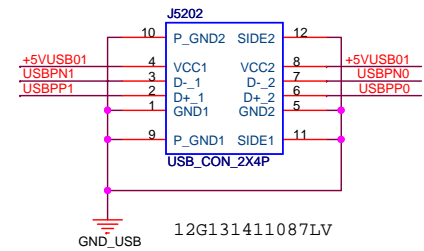
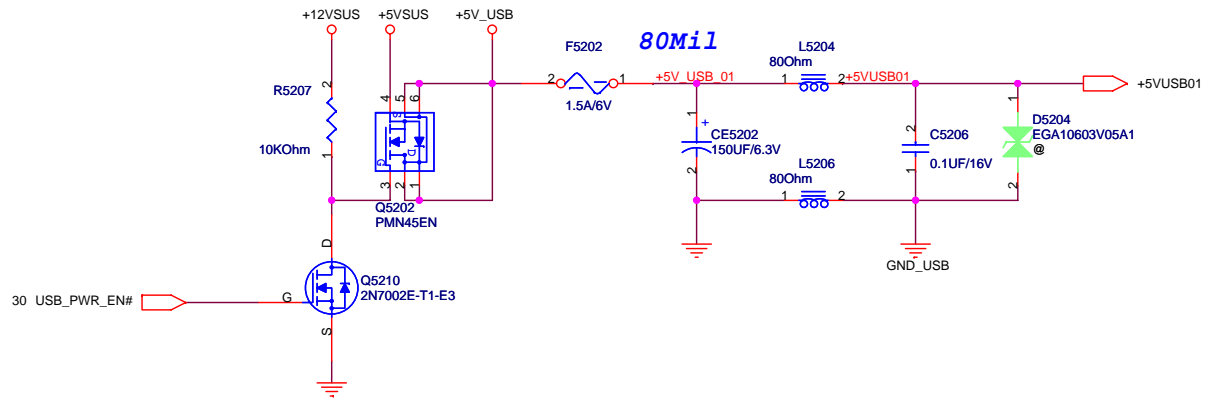
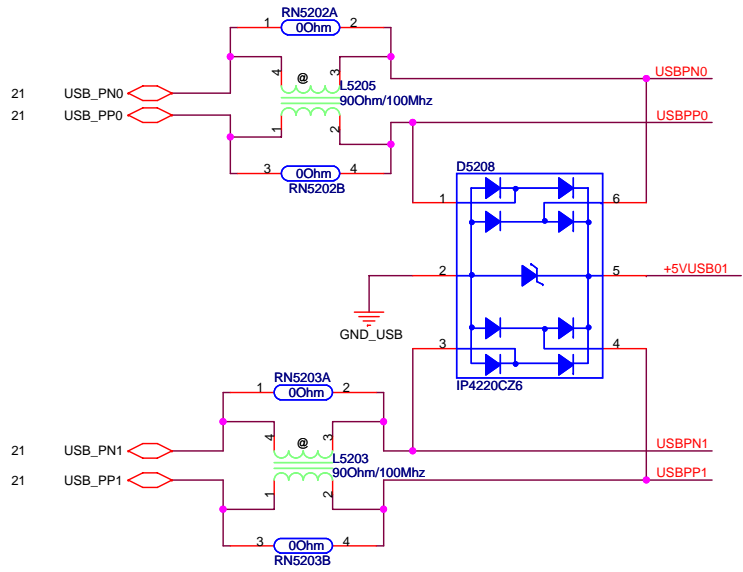


ODD CON



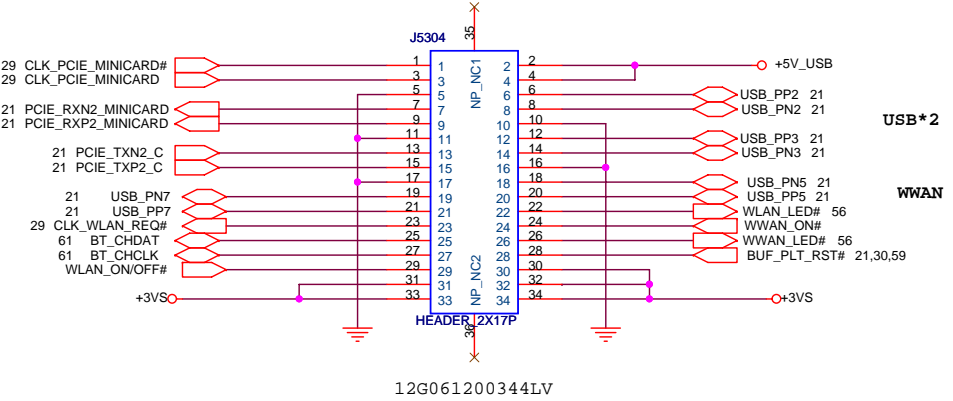
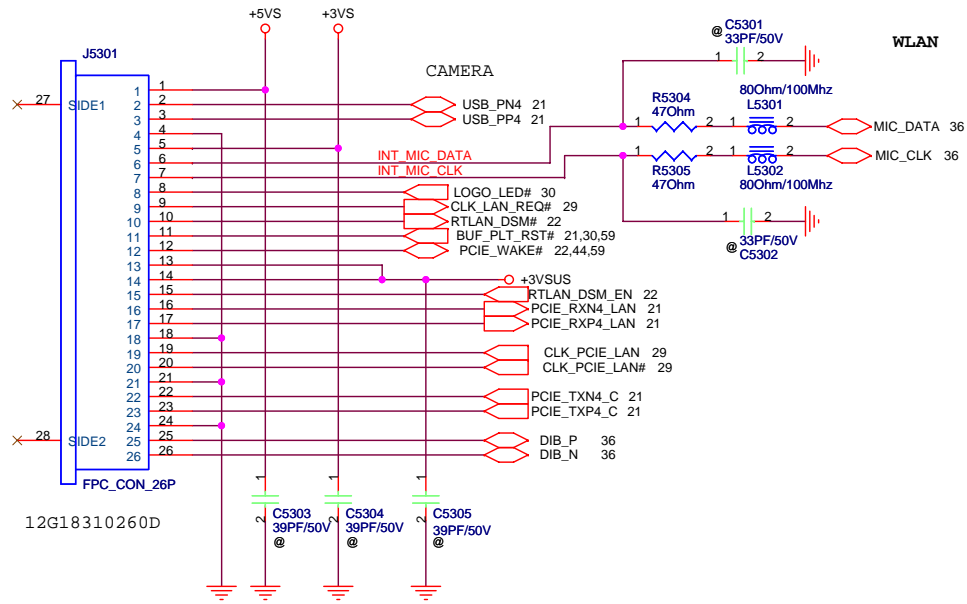
SATA HDD CON



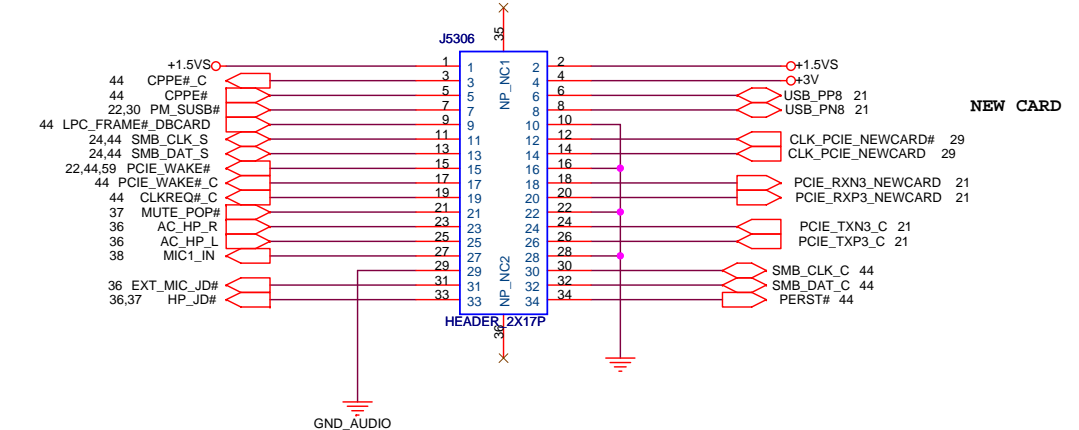
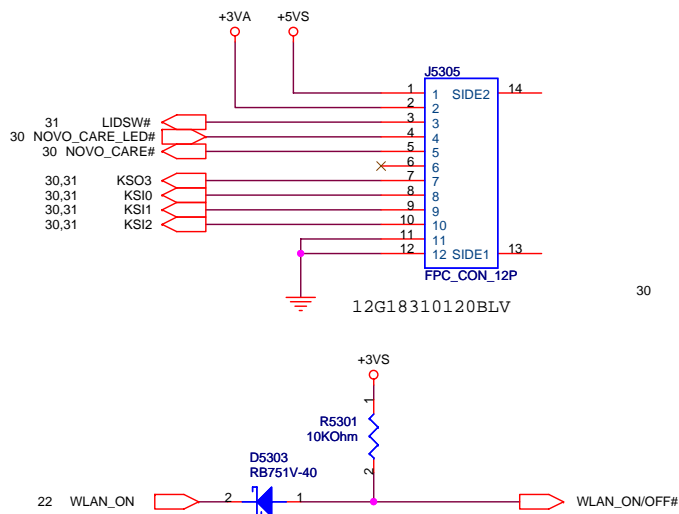


IO BOARD

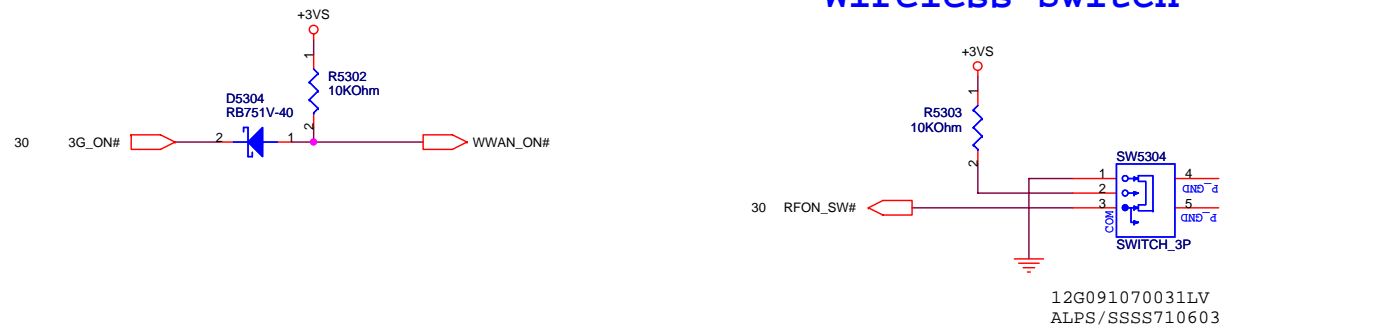
SMALL BOARD



For Media Control Board



Wireless Switch



| | | | |
|-----------------------------------|--------------------|---------------------------|--|
| ASUS | | Title : IO BOARD | |
| | | Engineer: Tina Lee | |
| Size | Project Name | Rev | |
| Custom | Rocky 40/50 | 1.0 | |
| Date: Thursday, December 20, 2007 | Sheet 53 | of 94 | |

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Engineer: *Tina Lee*

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| Size A4 | Project Name Rocky 40/50 | Rev 1.0 |
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Title : Super I/O & FIR

Engineer: Tina Lee

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| Size | Project Name | Rev |
| A4 | Rocky 40/50 | 1.0 |

A

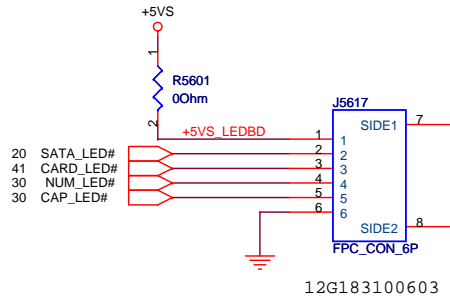
B

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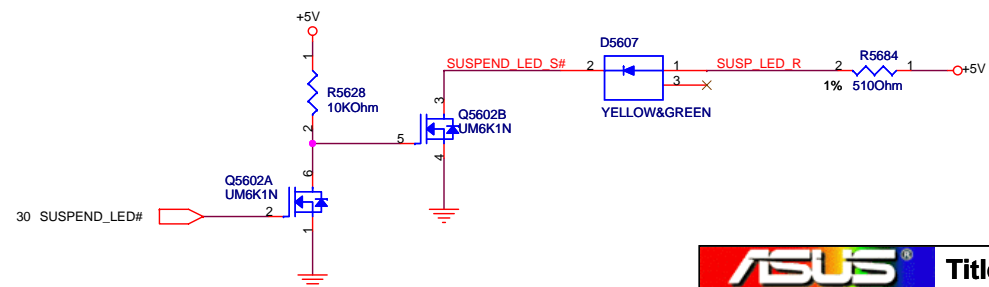
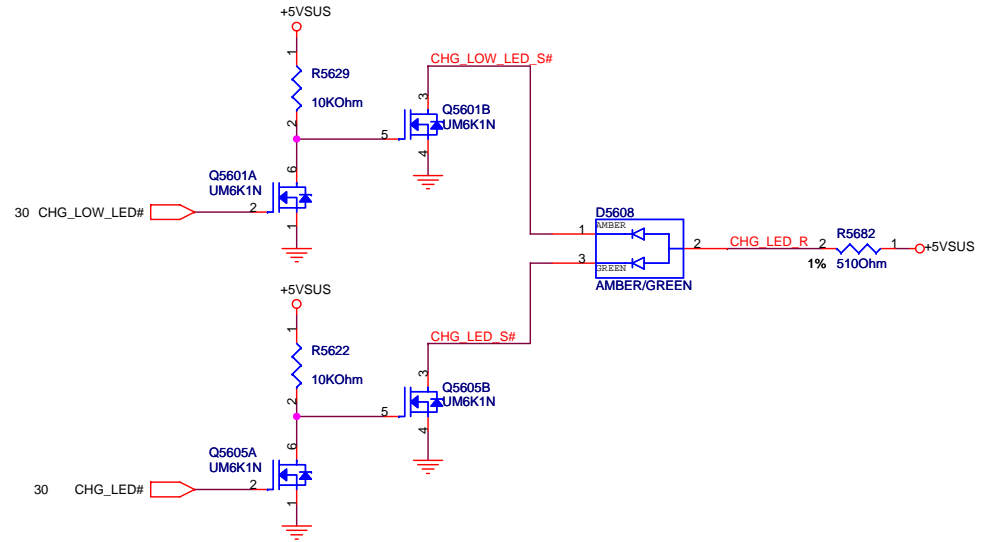
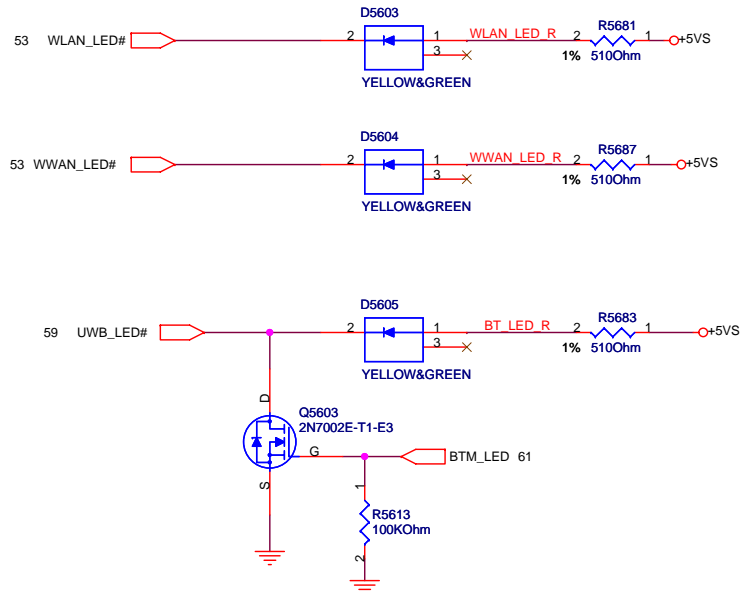
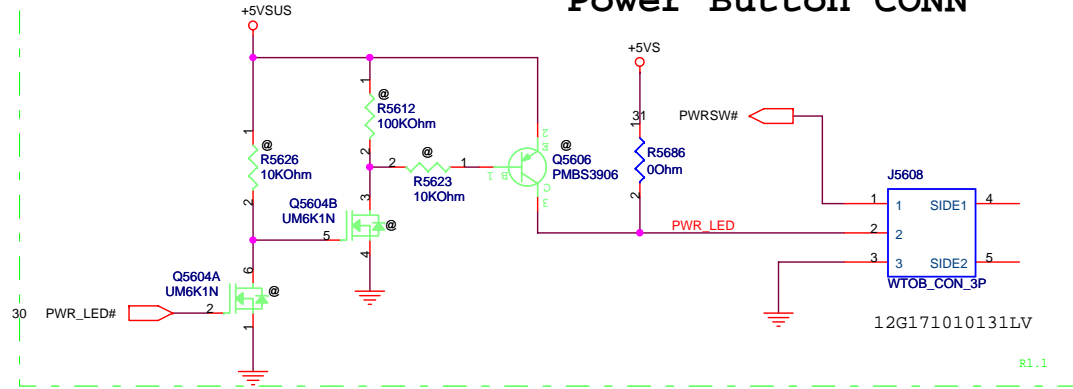
D

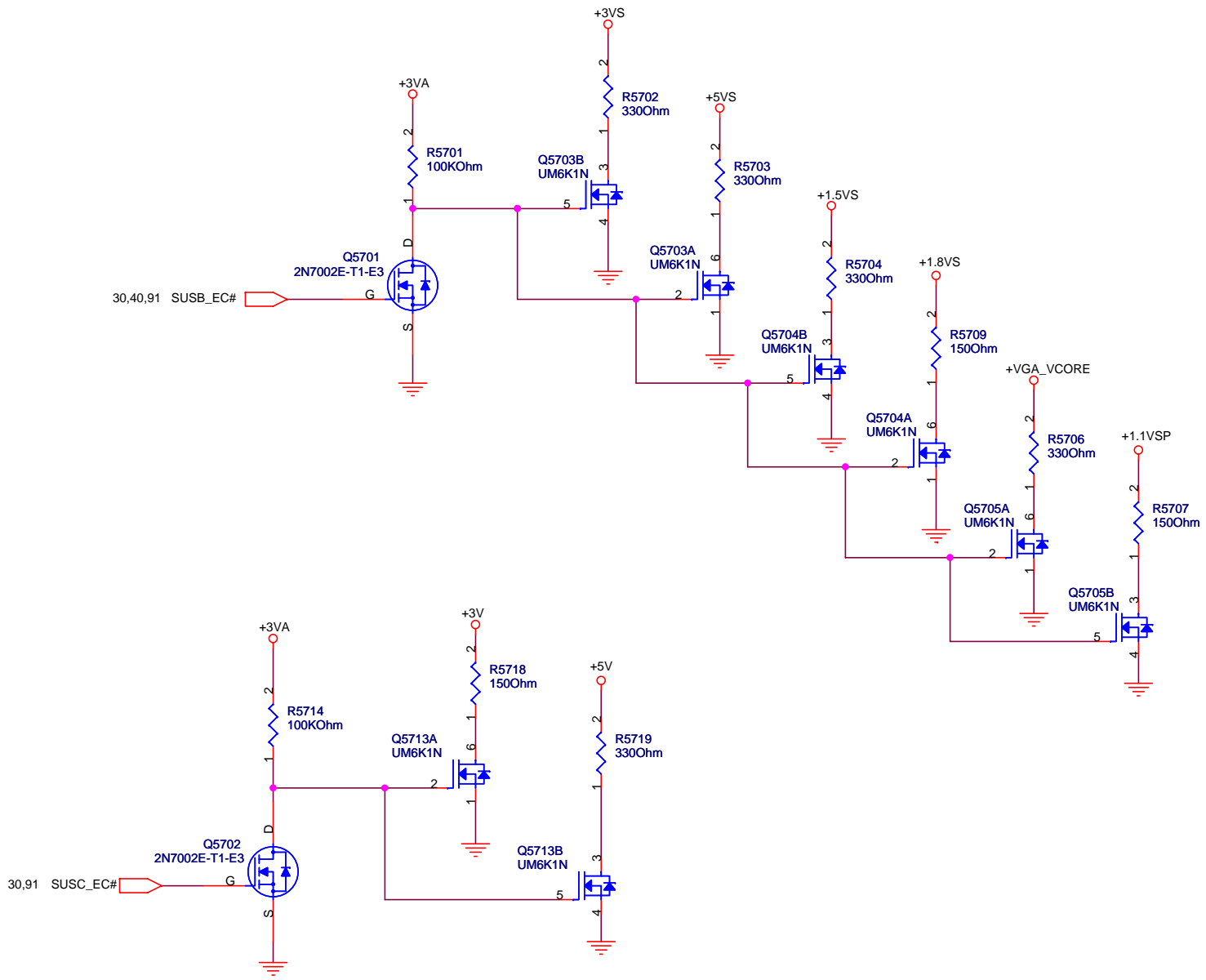
E

LED CONN

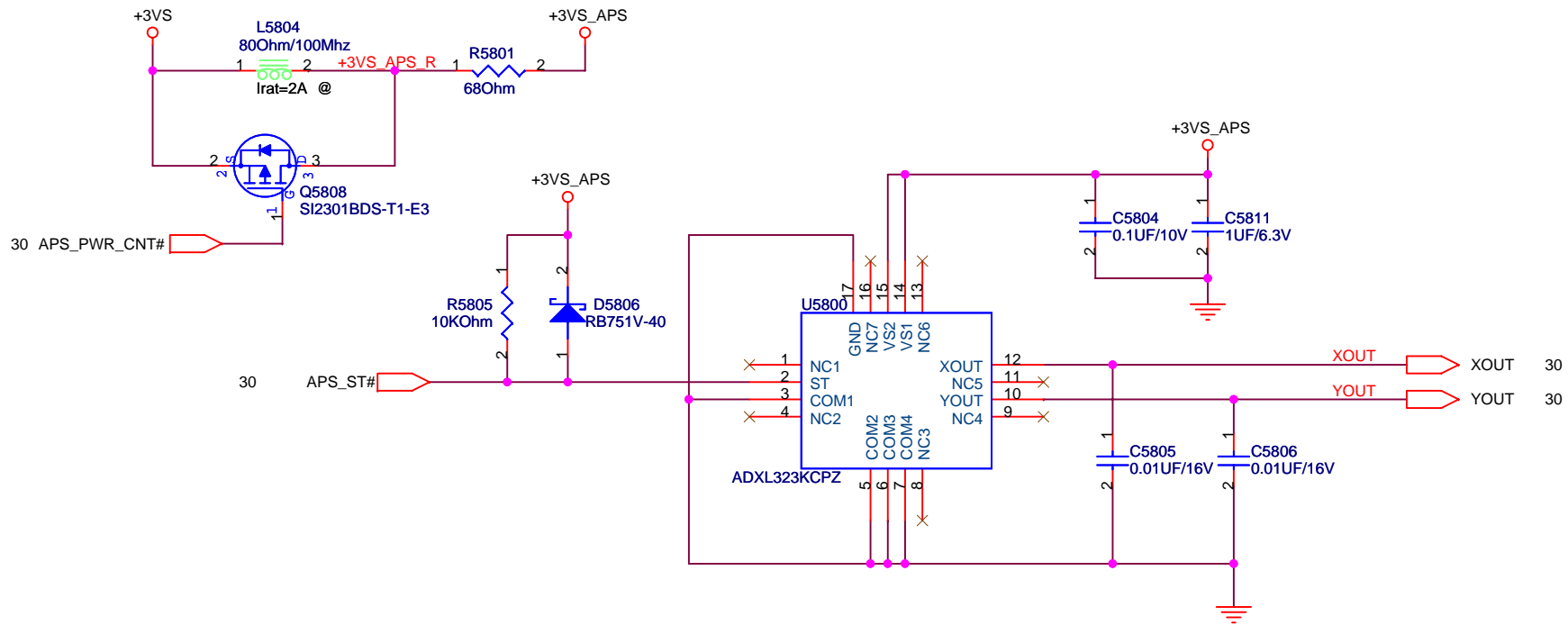


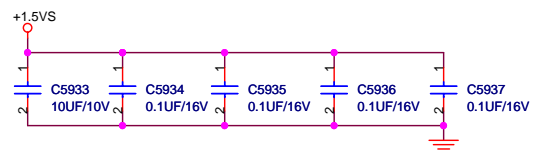
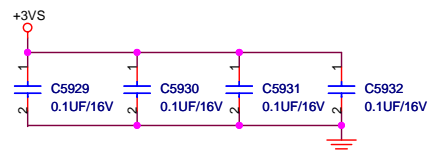
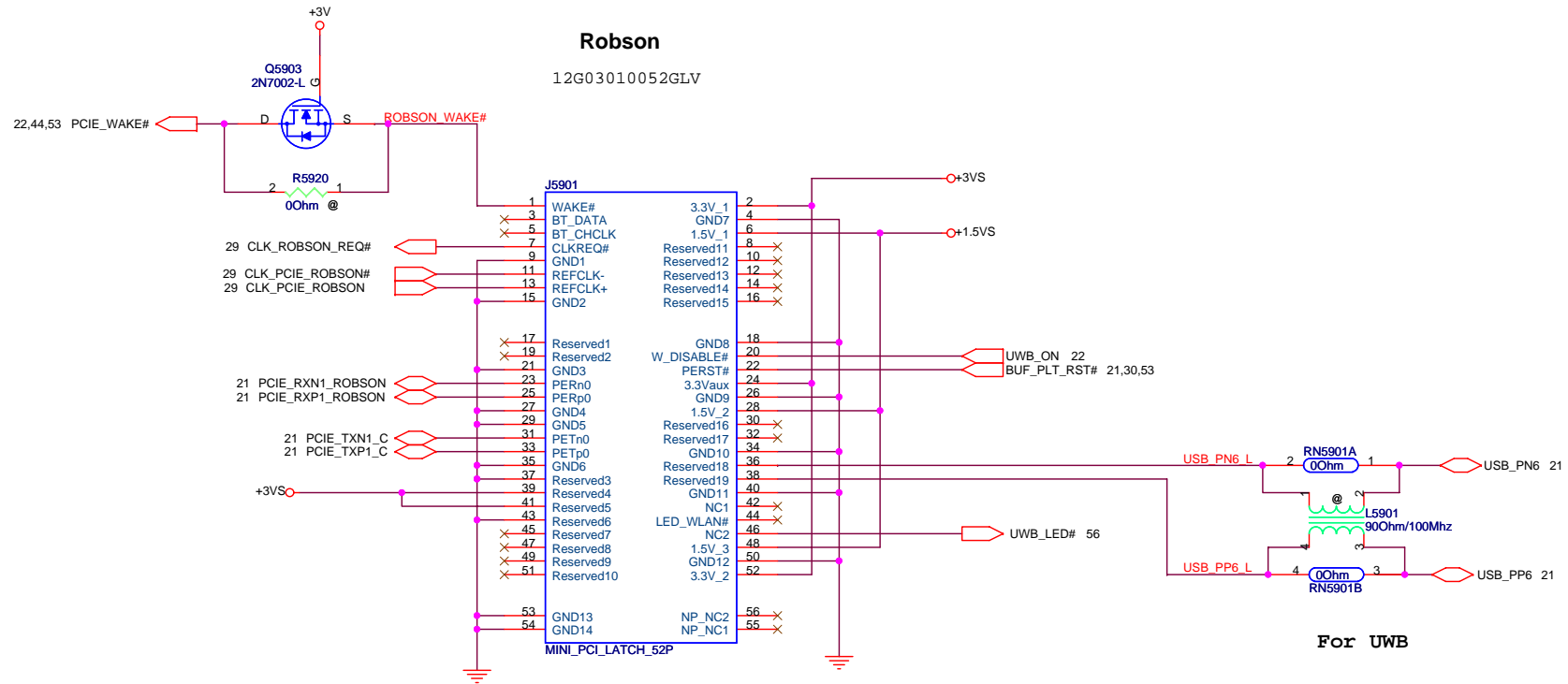
Power Button CONN



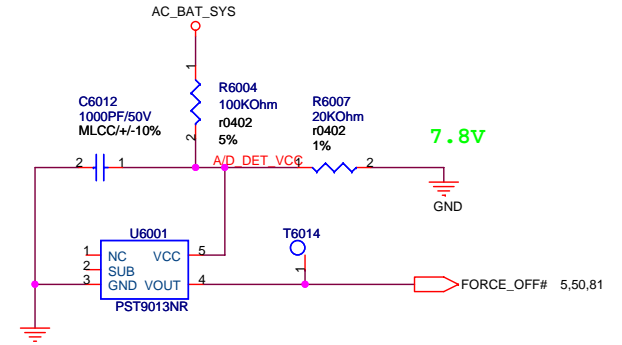
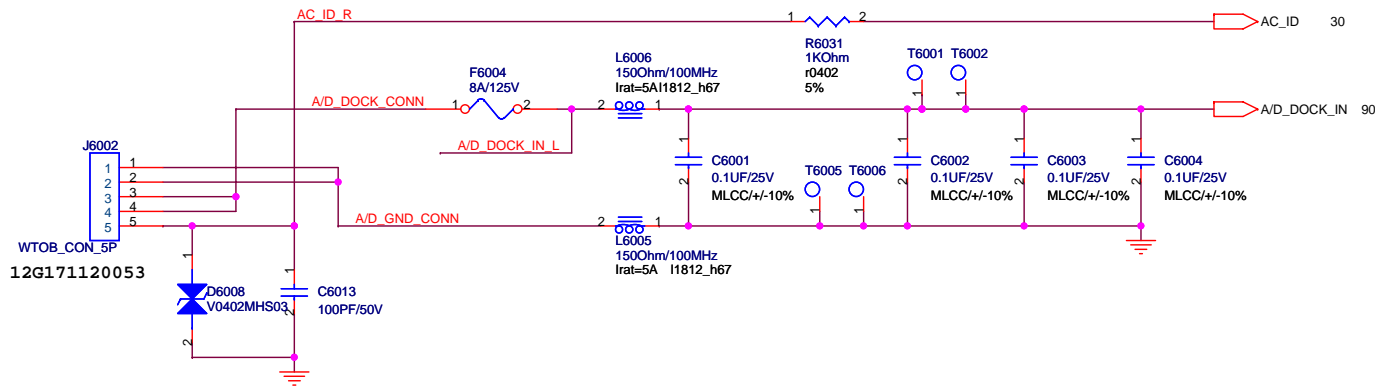


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| | | Title : DISCHARGE |
| | | Engineer: <i>Tina Lee</i> |
| Size | Project Name | Rev |
| Custom | Rocky 40/50 | 1.0 |
| Date: Thursday, December 20, 2007 | | Sheet 57 of 94 |



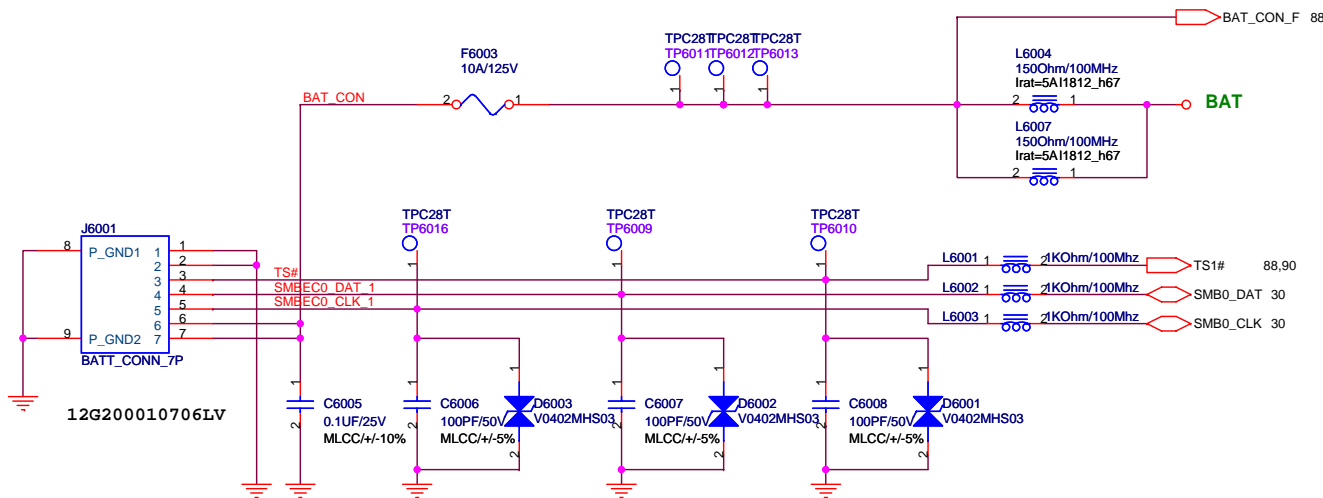


DC IN CONN

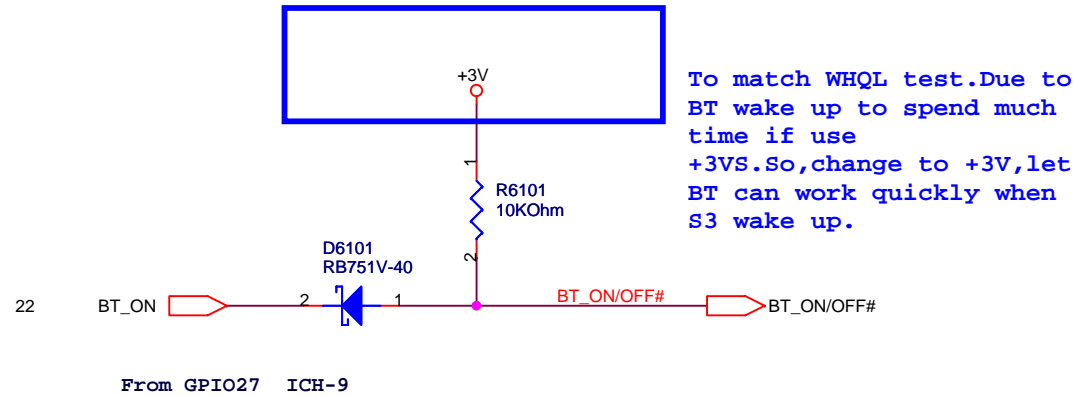
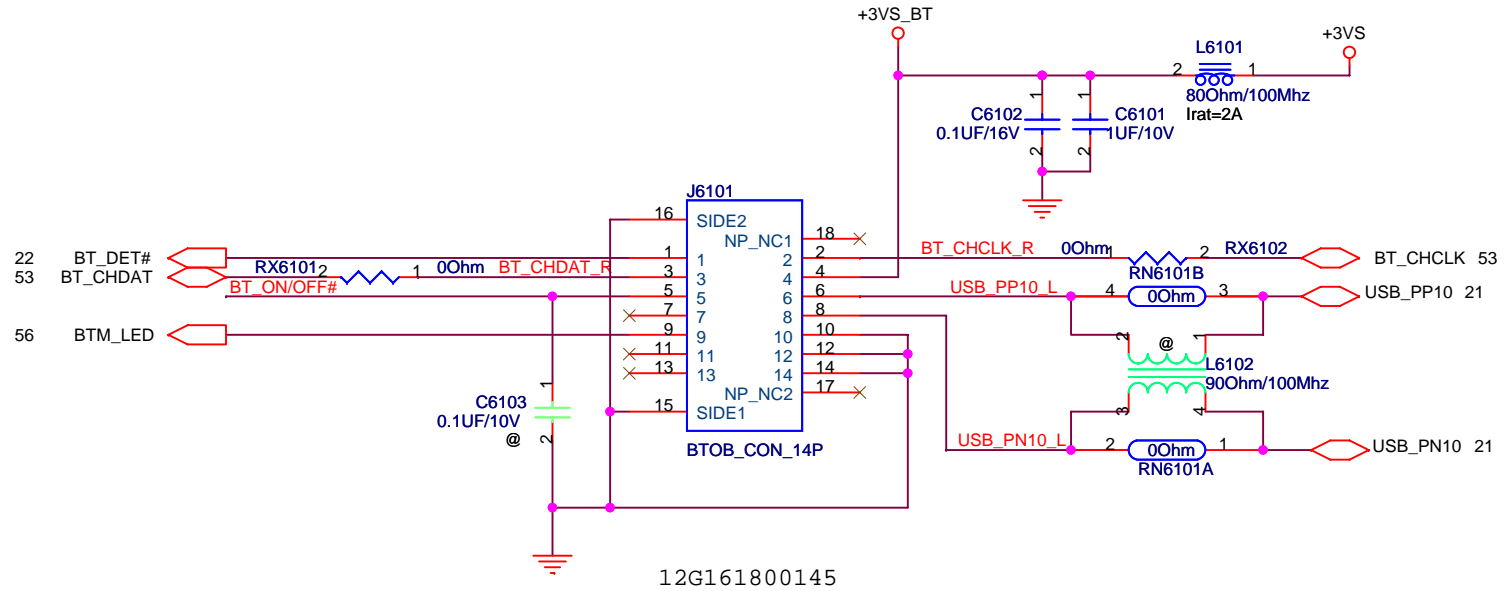


Without Battery & Pull out Adapter

Battery CONN



Blue Tooth



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|  | | Title : TPM | |
| Engineer: Tina Lee | | | |
| Size A4 | Project Name Rocky 40/50 | Rev 1.0 | |
| Date: Monday, December 17, 2007 | | Sheet | 62 of 94 |

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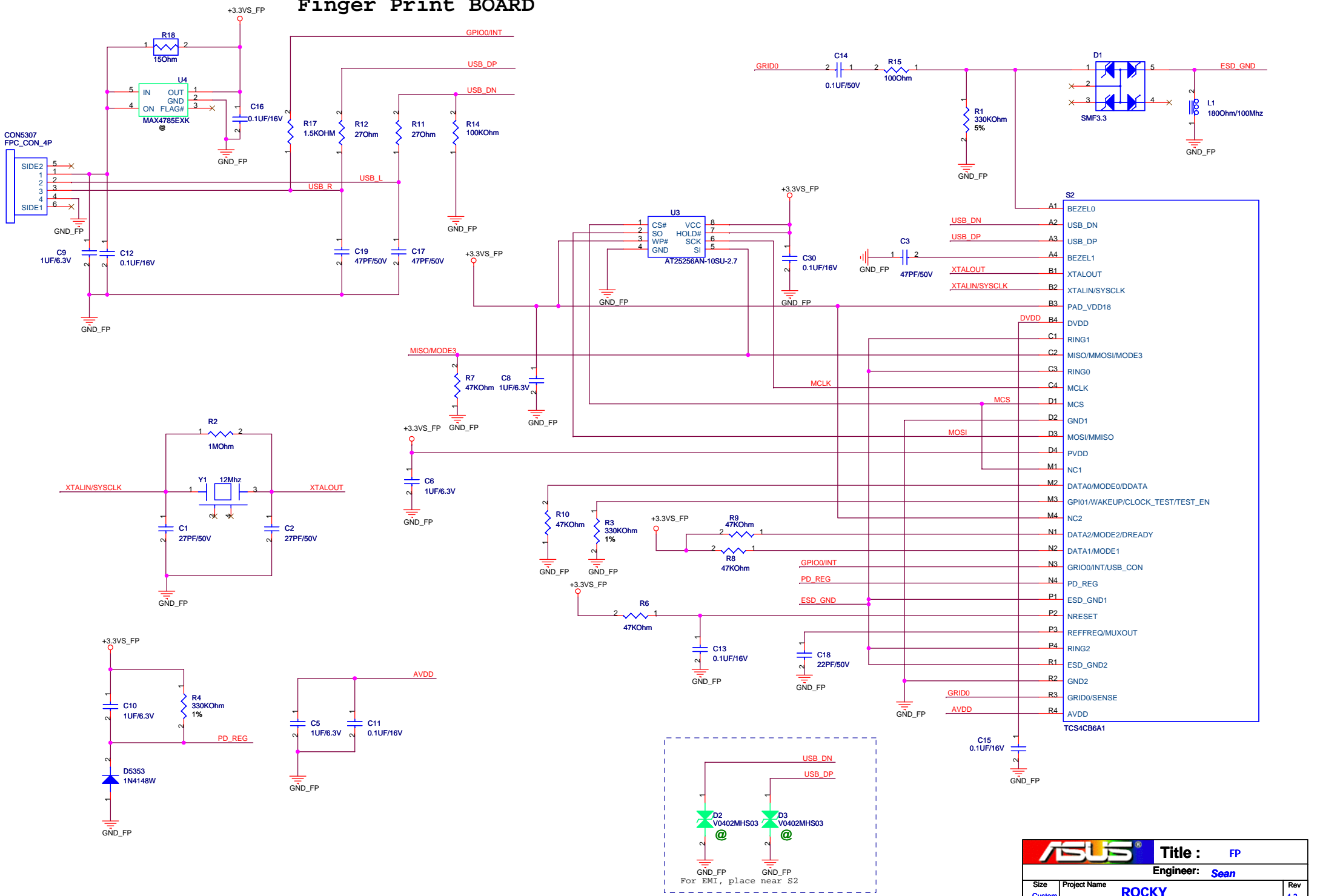
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Finger Print BOARD



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| ASUS | | Title : FP |
| | | Engineer: Sean |
| Size Custom | Project Name ROCKY | Rev 1.3 |
| Date: Monday, December 17, 2007 | Sheet 63 | of 94 |

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|  | | Title : | |
| Engineer: <i>Tina Lee</i> | | | |
| Size | Project Name | | Rev |
| A4 | Rocky 40/50 | | 1.0 |
| Date: Monday, December 17, 2007 | | Sheet | 64 of 94 |

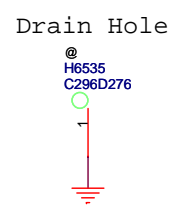
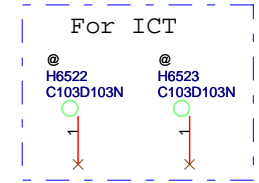
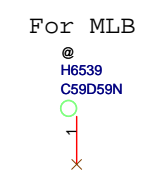
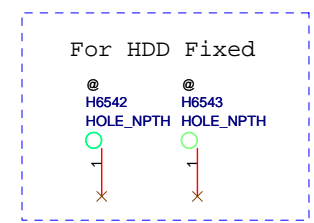
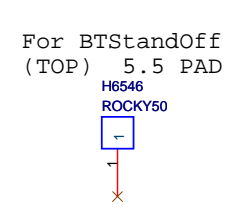
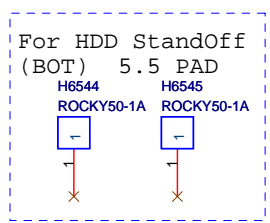
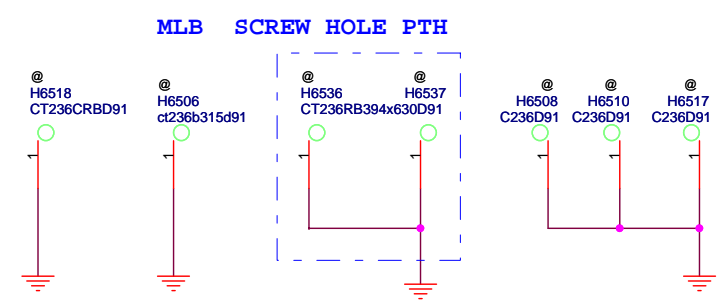
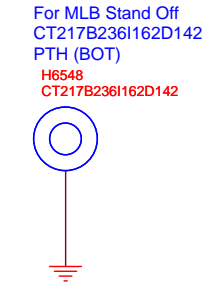
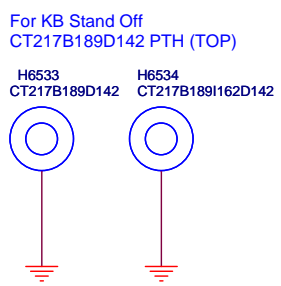
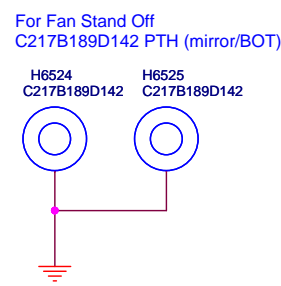
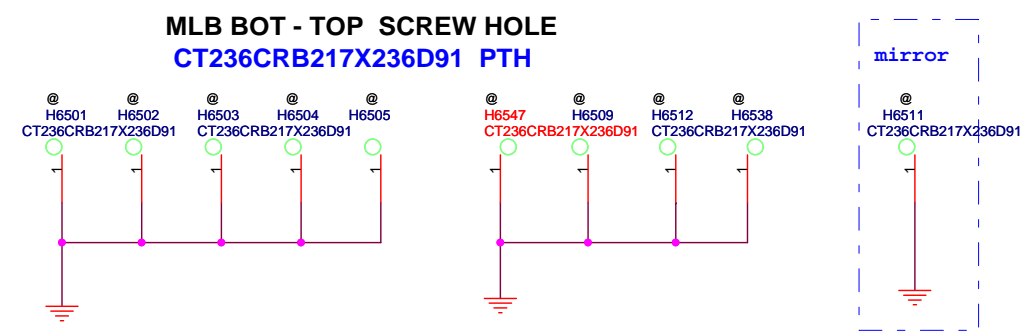
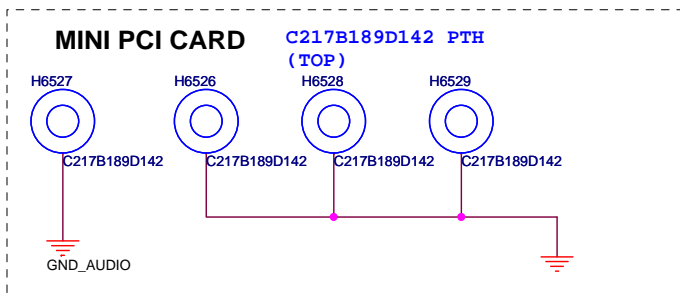
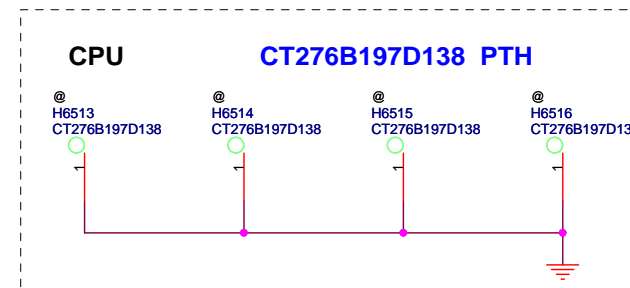
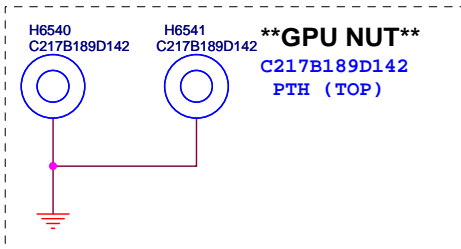
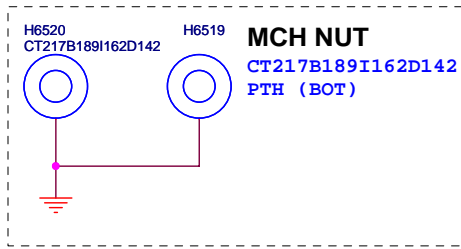
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|  | | Title : E-SATA | |
| Engineer: Tina Lee | | | |
| Size | Project Name | | Rev |
| A4 | Rocky 40/50 | | 1.0 |
| Date: Monday, December 17, 2007 | | Sheet | 66 of 94 |

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|  | | Title :Minicard card & Nut | |
| Engineer: Tina Lee | | | |
| Size | Project Name | Rev | |
| A4 | Rocky 40/50 | 1.0 | |
| Date: Monday, December 17, 2007 | | Sheet | 67 of 94 |

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|  | | Title : XDP | |
| Engineer: Tina Lee | | | |
| Size | Project Name | | Rev |
| A4 | Rocky 40/50 | | 1.0 |
| Date: Monday, December 17, 2007 | | Sheet | 68 of 94 |

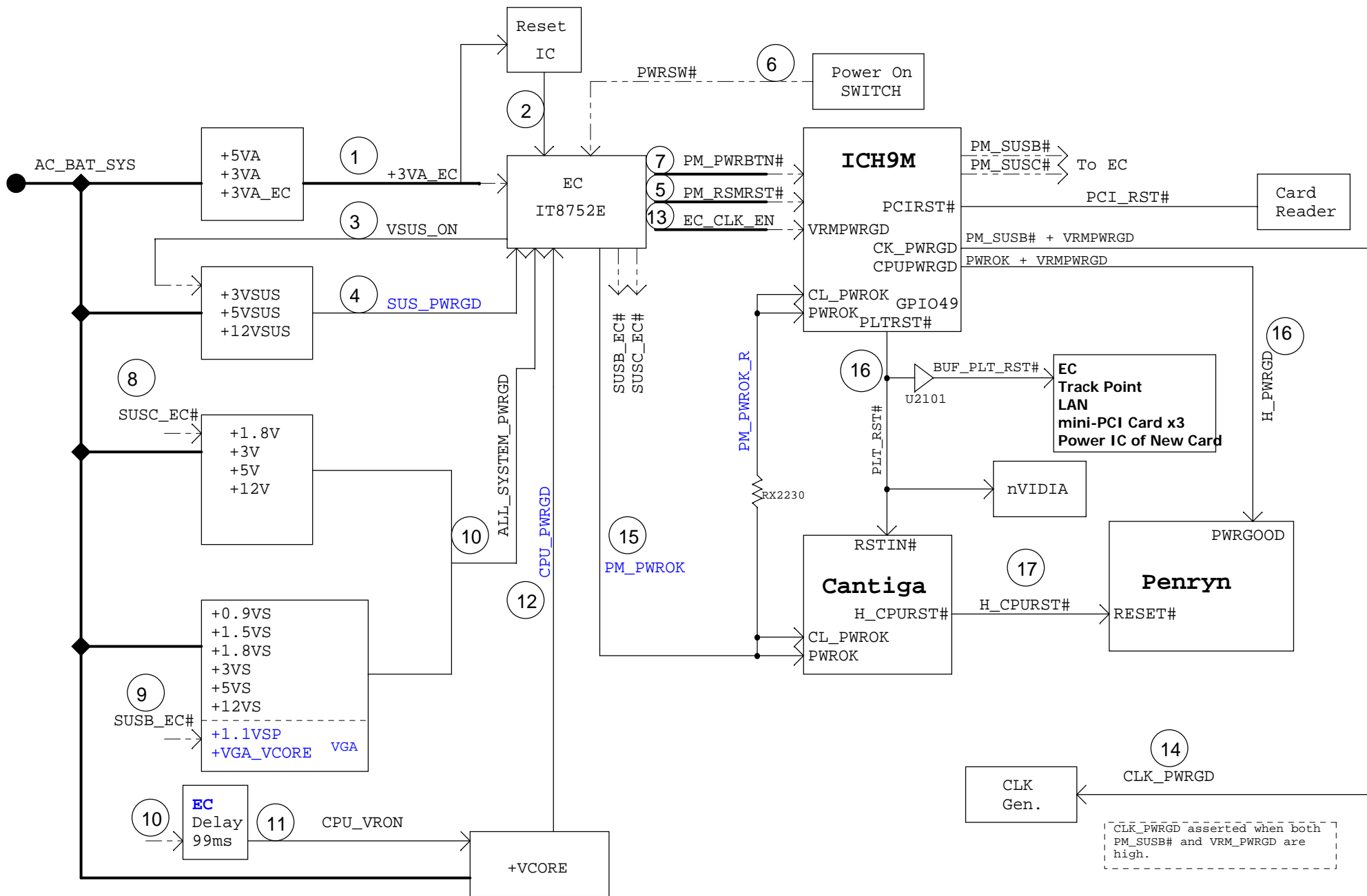
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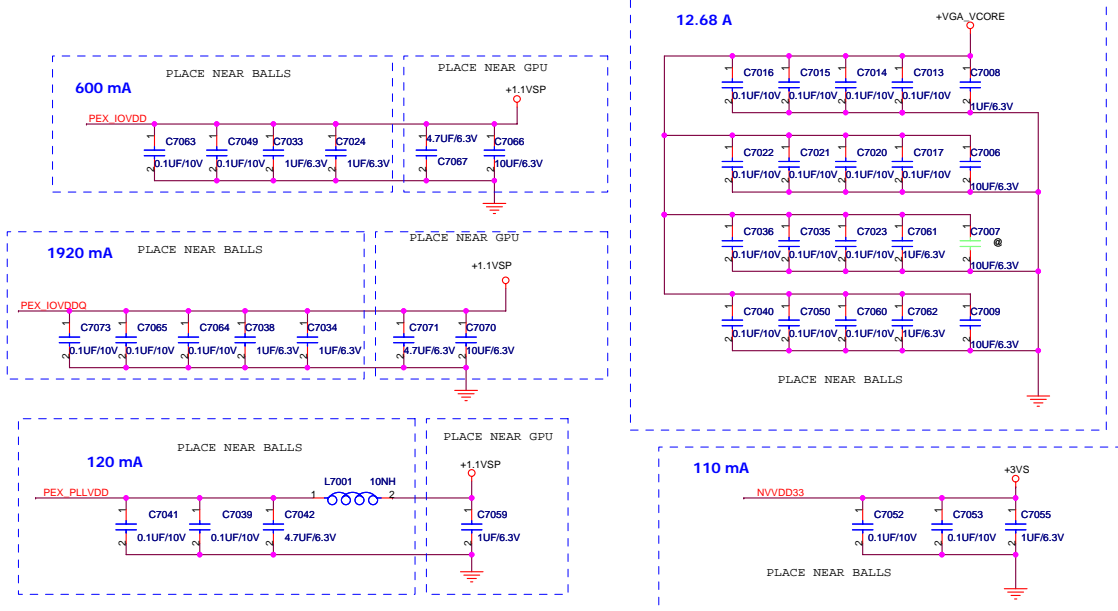
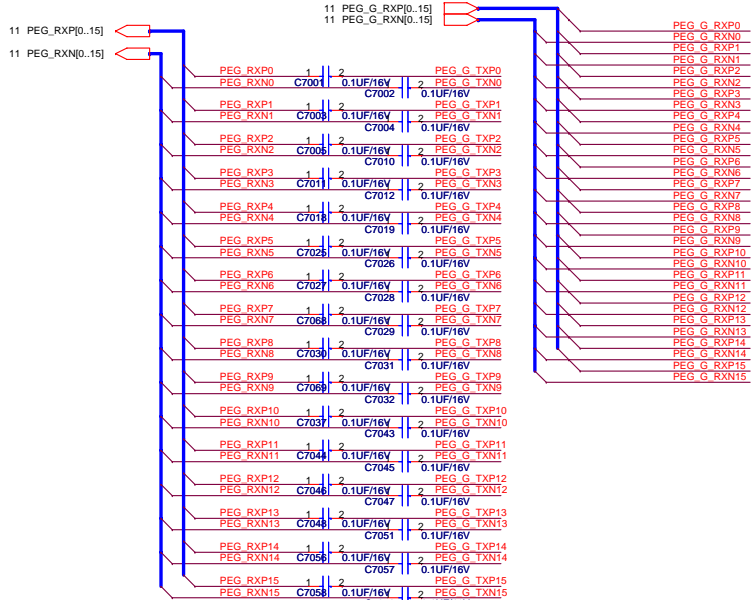
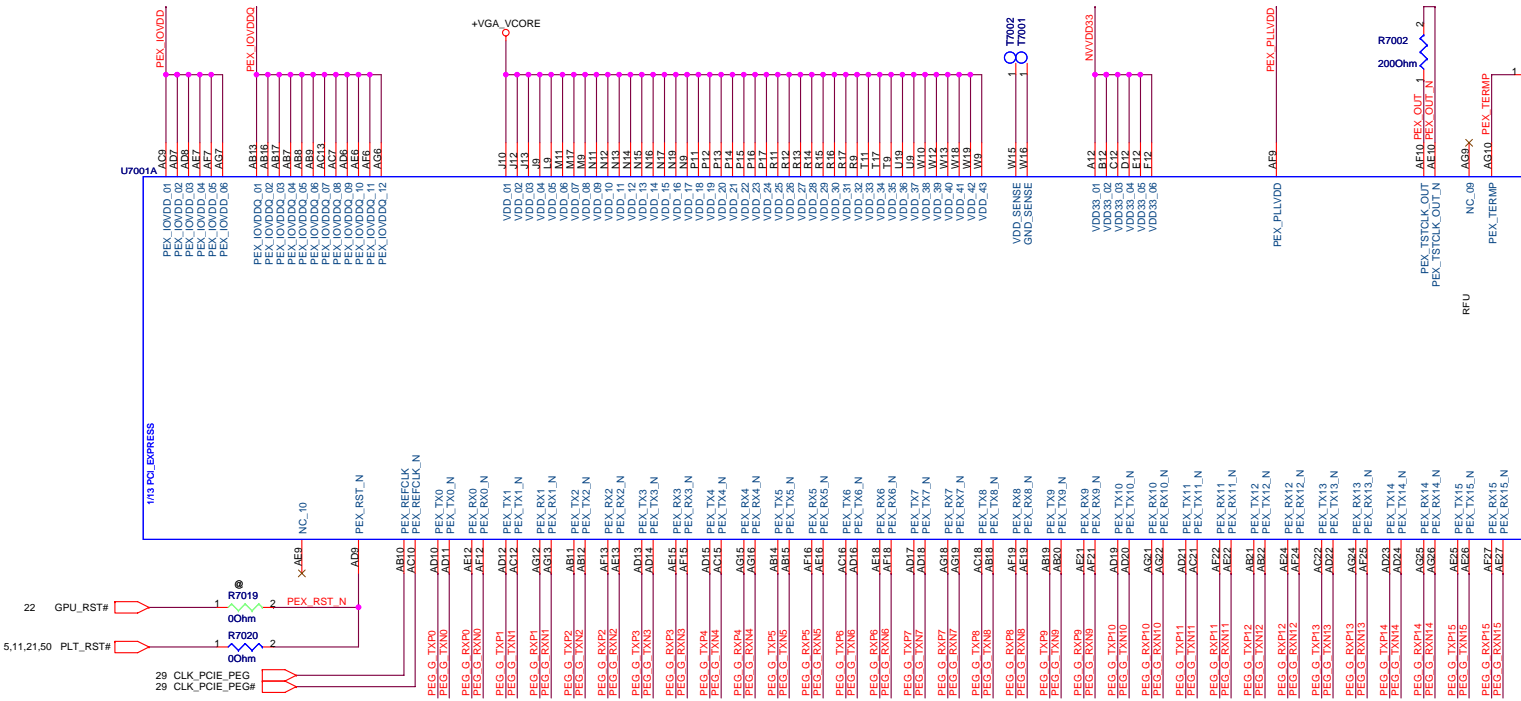
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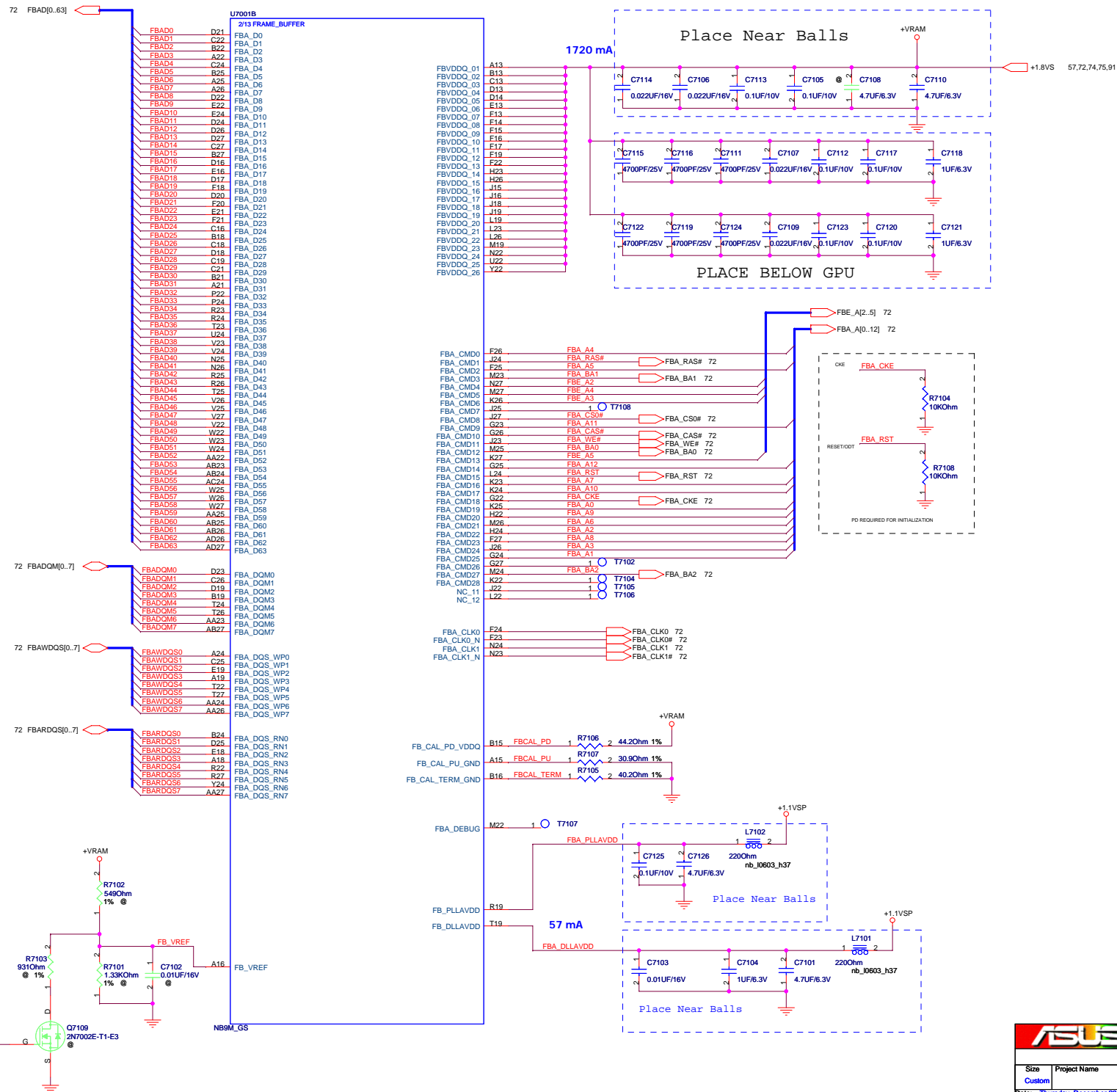
1



Power On Sequence







- 71 FBADQM[0..7]
- 71 FBAD[0..63]
- 71 FBAWDSQ[0..7]
- 71 FBARDQS[0..7]
- 71 FBA_A[0..12]
- 71 FBE_A[2..5]

- 71 FBA_RAS#
- 71 FBA_CAS#
- 71 FBA_WE#
- 71 FBA_CS0#

- FBA_A0
- FBA_A1
- FBA_A2
- FBA_A3
- FBA_A4
- FBA_A5
- FBA_A6
- FBA_A7
- FBA_A8
- FBA_A9
- FBA_A10
- FBA_A11

- FBA_BA0
- FBA_BA1
- FBA_BA2
- FBA_CKE
- FBA_CLK0
- FBA_CLK0#

- FBA_A12
- FBA_RST

- FBAWDSQ3
- FBAWDSQ4
- FBAWDSQ5
- FBAWDSQ6

- FBARDQS2
- FBARDQS3
- FBARDQS4
- FBARDQS5

- FBADQM0
- FBADQM3
- FBADQM1
- FBADQM2

- VSSQ1
- VSSQ5
- VSSQ13
- VSSQ17
- VSSQ9
- VSSQ11
- VSSQ2
- VSSQ4
- VSSQ14
- VSSQ18
- VSSQ7
- VSSQ15
- VSSQ19
- VSSQ10
- VSSQ12
- VSSQ20

- VDD3
- VDD5
- VDD1
- VDD7
- VDD2
- VDD8
- VDD4
- VDD6

- VSS3
- VSS5
- VSS1
- VSS7
- VSS2
- VSS6

- VSS9
- VSS10

- VREF1
- VREF2

- T3 FBAD0
- T2 FBAD1
- T1 FBAD2
- R2 FBAD3
- M3 FBAD4
- N2 FBAD5
- L3 FBAD7
- M2 FBAD8
- T10 FBAD9
- T11 FBAD10
- R10 FBAD11
- R11 FBAD12
- M10 FBAD13
- N10 FBAD14
- A9 FBAD15
- A3 FBAD16
- A7 FBAD17
- A4 FBAD18
- A11 FBAD19

- FBA_BA0
- FBA_BA1
- FBA_BA2
- FBA_CKE
- FBA_CLK0
- FBA_CLK0#

- FBA_A12
- FBA_RST

- FBAD06
- FBAD07
- FBAD08
- FBAD09
- FBAD10
- FBAD11
- FBAD12
- FBAD13
- FBAD14
- FBAD15
- FBAD16
- FBAD17
- FBAD18
- FBAD19

- VDDQ1
- VDD07
- VDD013
- VDD017
- VDD021
- VDD04
- VDD08
- VDD11
- VDD018
- VDD08
- VDD05
- VDD09
- VDD02
- VDD10
- VDD06
- VDD11
- VDD010
- VDD016
- VDD022

- VSSQ1
- VSSQ5
- VSSQ13
- VSSQ17
- VSSQ9
- VSSQ11
- VSSQ2
- VSSQ4
- VSSQ14
- VSSQ18
- VSSQ7
- VSSQ15
- VSSQ19
- VSSQ10
- VSSQ12
- VSSQ20

- VDD3
- VDD5
- VDD1
- VDD7
- VDD2
- VDD8
- VDD4
- VDD6

- VSS3
- VSS5
- VSS1
- VSS7
- VSS2
- VSS6

- VSS9
- VSS10

- VREF1
- VREF2

- FBA_BA2

- FBA_A12
- FBA_RST

- FBA_BA1
- FBA_BA0
- FBA_WE#
- FBA_CLK1
- FBA_CLK1#

- FBA_A12
- FBA_RST

- FBAD20
- FBAD21
- FBAD22
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- FBAD24
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- FBAD26
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- FBAD56

- VDDQ1
- VDD07
- VDD013
- VDD017
- VDD021
- VDD04
- VDD08
- VDD11
- VDD018
- VDD08
- VDD05
- VDD09
- VDD02
- VDD10
- VDD06
- VDD11
- VDD010
- VDD016
- VDD022

- VSSQ1
- VSSQ5
- VSSQ13
- VSSQ17
- VSSQ9
- VSSQ11
- VSSQ2
- VSSQ4
- VSSQ14
- VSSQ18
- VSSQ7
- VSSQ15
- VSSQ19
- VSSQ10
- VSSQ12
- VSSQ20

- VDD3
- VDD5
- VDD1
- VDD7
- VDD2
- VDD8
- VDD4
- VDD6

- VSS3
- VSS5
- VSS1
- VSS7
- VSS2
- VSS6

- VSS9
- VSS10

- VREF1
- VREF2

- RAS#
- CAS#
- WE#
- CS0#

- FBE_A4
- FBE_A5
- FBE_A6
- FBE_A9
- FBE_A11
- FBE_A2
- FBE_A3
- FBE_A8
- FBE_A7

- FBA_BA1
- FBA_BA0
- FBA_WE#
- FBA_CLK1
- FBA_CLK1#

- FBA_A12
- FBA_RST

- FBAD55
- FBAD56
- FBAD57
- FBAD58
- FBAD59
- FBAD60
- FBAD61
- FBAD62
- FBAD63
- FBAD64
- FBAD65
- FBAD66
- FBAD67
- FBAD68
- FBAD69
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- FBAD92
- FBAD93
- FBAD94
- FBAD95
- FBAD96
- FBAD97
- FBAD98
- FBAD99
- FBAD100

- VDDQ1
- VDD07
- VDD013
- VDD017
- VDD021
- VDD04
- VDD08
- VDD11
- VDD018
- VDD08
- VDD05
- VDD09
- VDD02
- VDD10
- VDD06
- VDD11
- VDD010
- VDD016
- VDD022

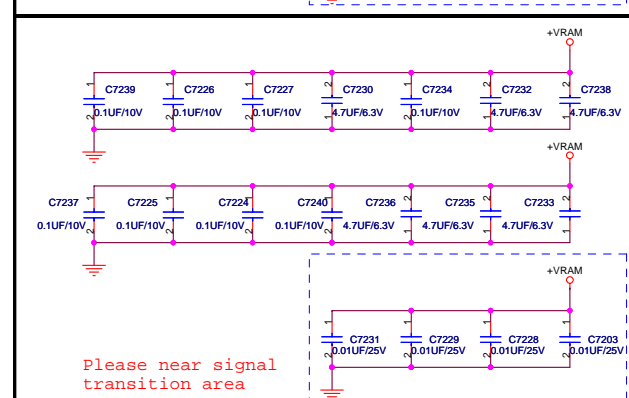
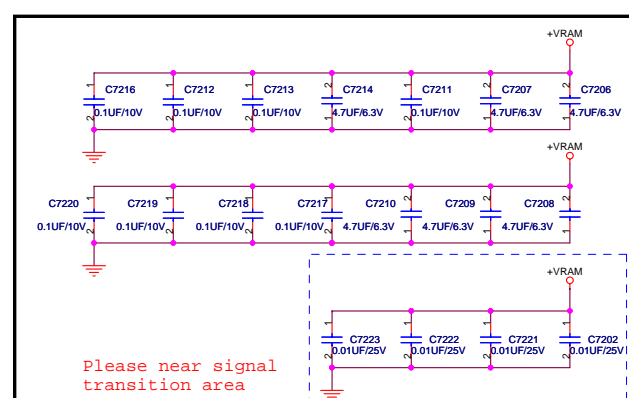
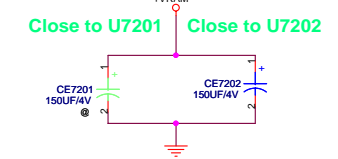
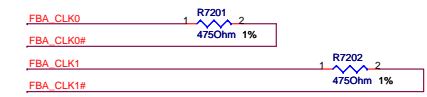
- VSSQ1
- VSSQ5
- VSSQ13
- VSSQ17
- VSSQ9
- VSSQ11
- VSSQ2
- VSSQ4
- VSSQ14
- VSSQ18
- VSSQ7
- VSSQ15
- VSSQ19
- VSSQ10
- VSSQ12
- VSSQ20

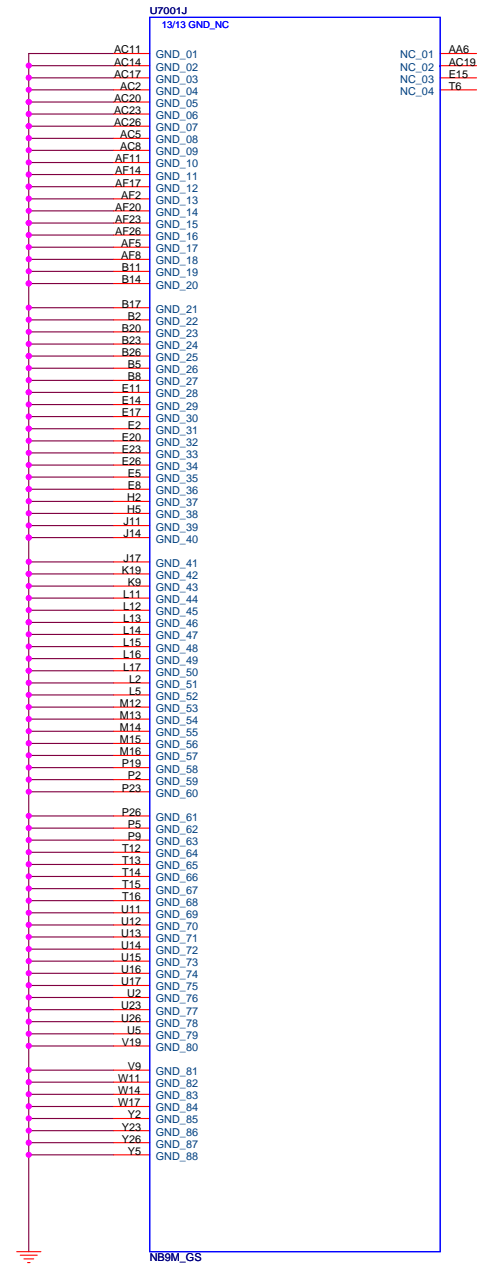
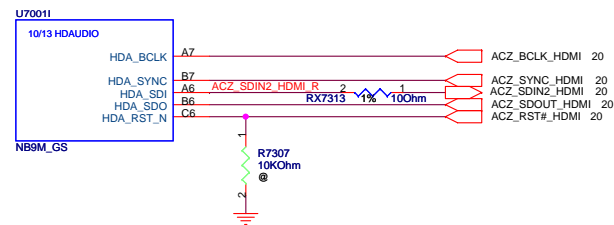
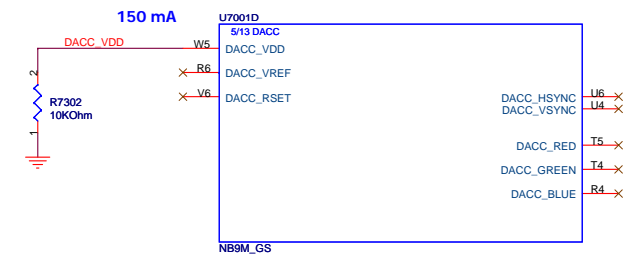
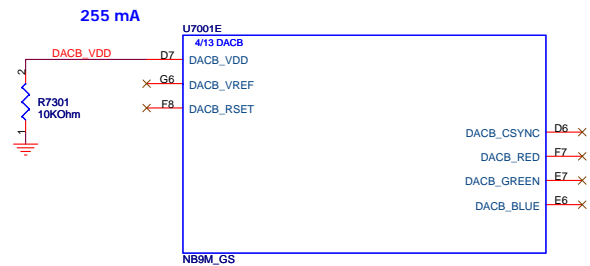
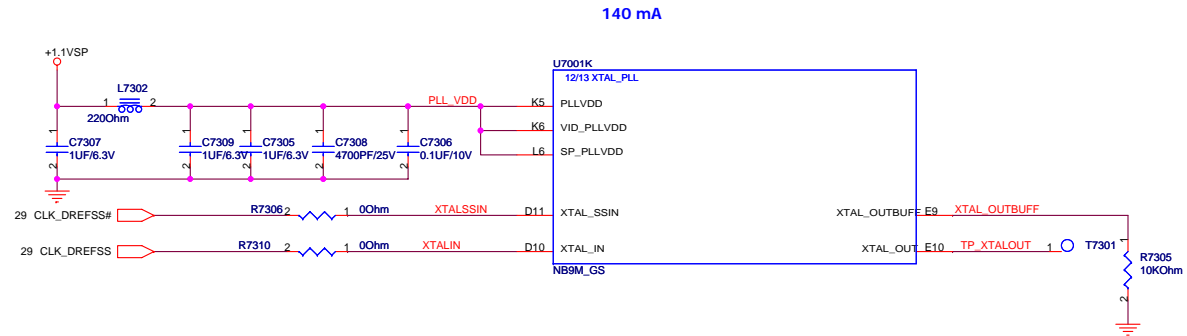
- VDD3
- VDD5
- VDD1
- VDD7
- VDD2
- VDD8
- VDD4
- VDD6

- VSS3
- VSS5
- VSS1
- VSS7
- VSS2
- VSS6

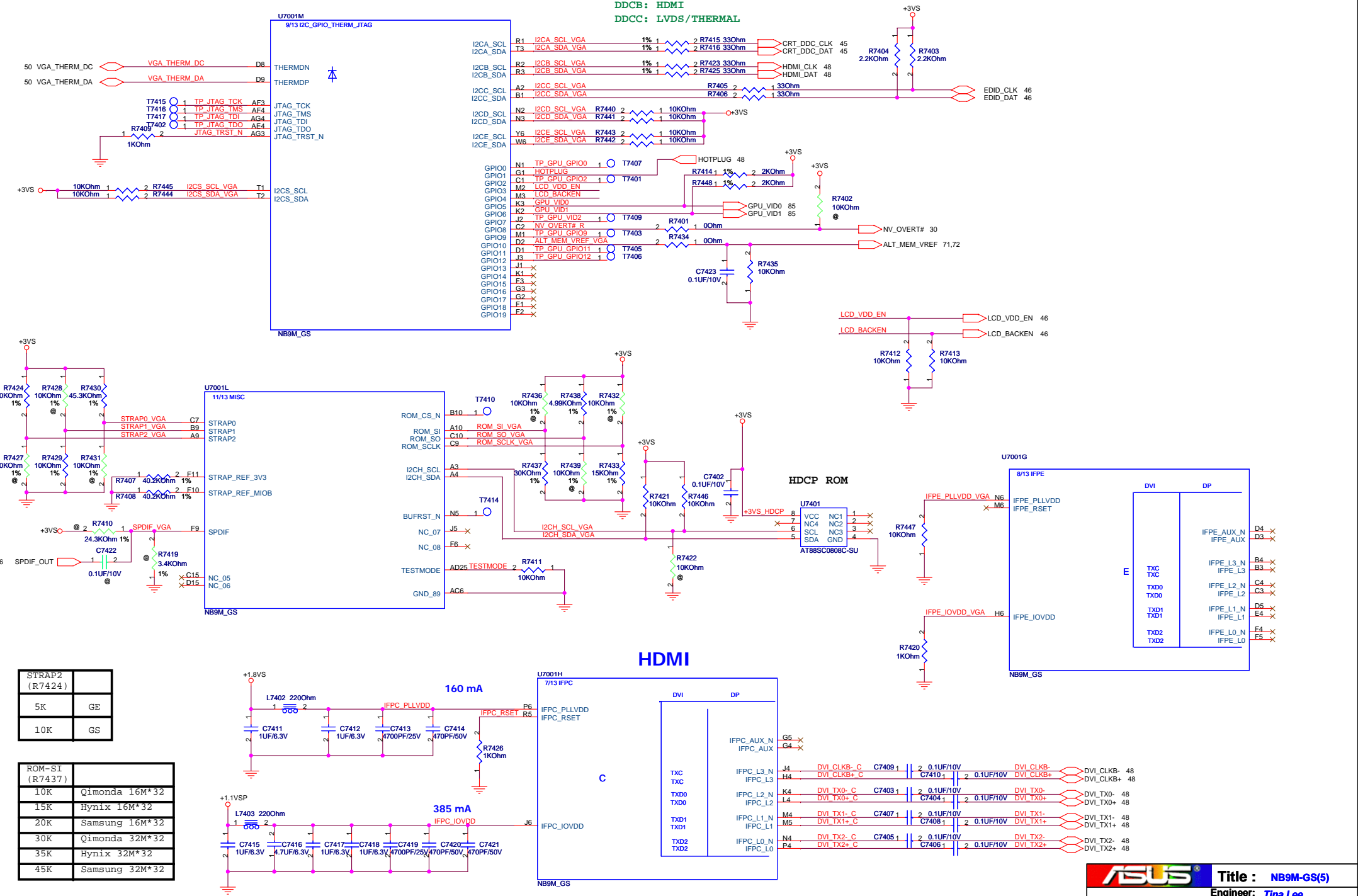
- VSS9
- VSS10

- VREF1
- VREF2



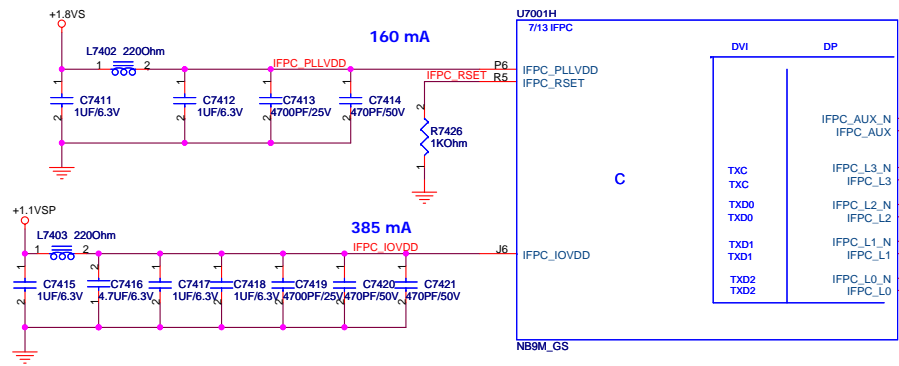


DDCA: CRT
 DDCB: HDMI
 DDCC: LVDS/THERMAL

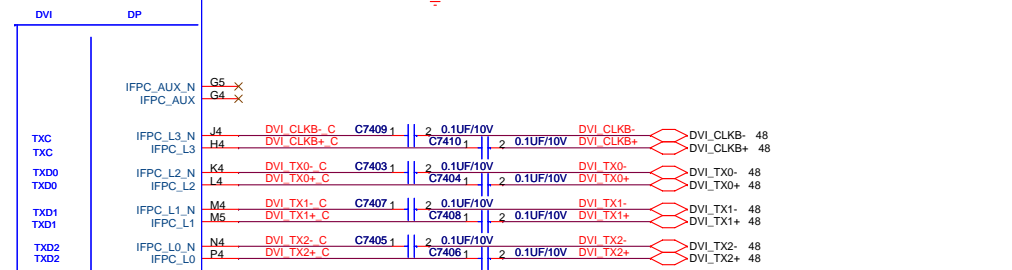


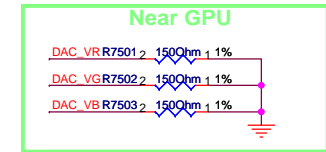
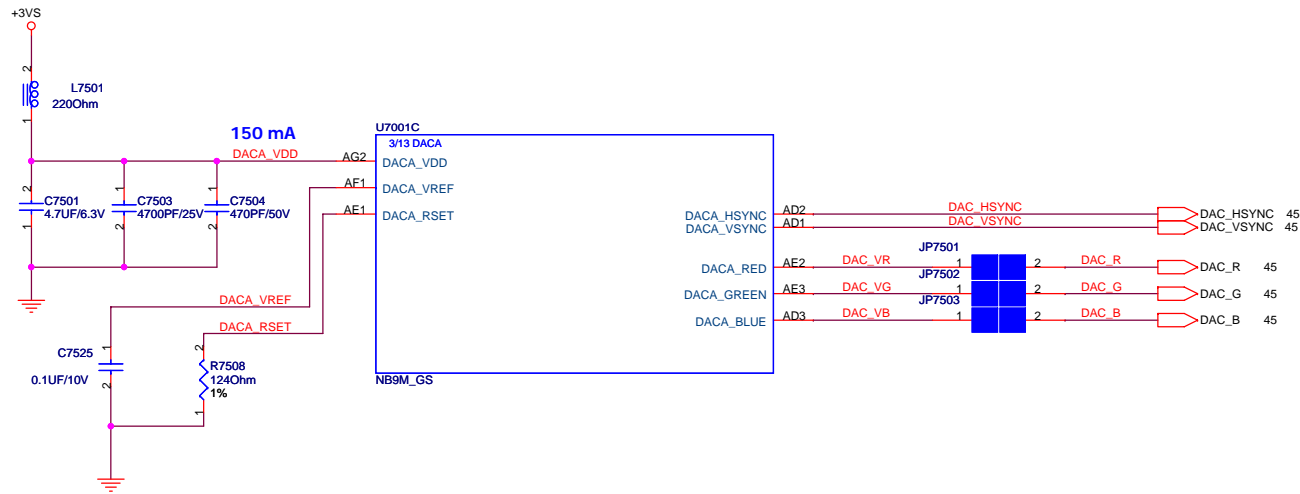
| | |
|----------------|----|
| STRAP2 (R7424) | |
| 5K | GE |
| 10K | GS |

| | |
|----------------|----------------|
| ROM-SI (R7437) | |
| 10K | Qimonda 16M*32 |
| 15K | Hynix 16M*32 |
| 20K | Samsung 16M*32 |
| 30K | Qimonda 32M*32 |
| 35K | Hynix 32M*32 |
| 45K | Samsung 32M*32 |

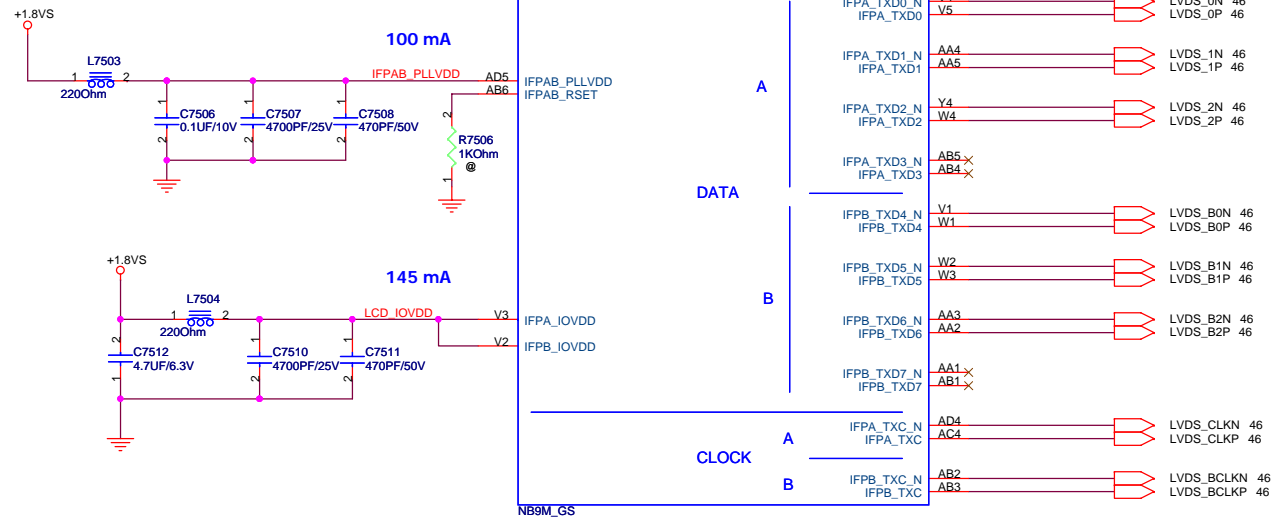
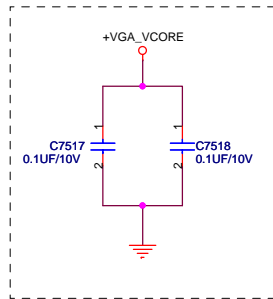


HDMI

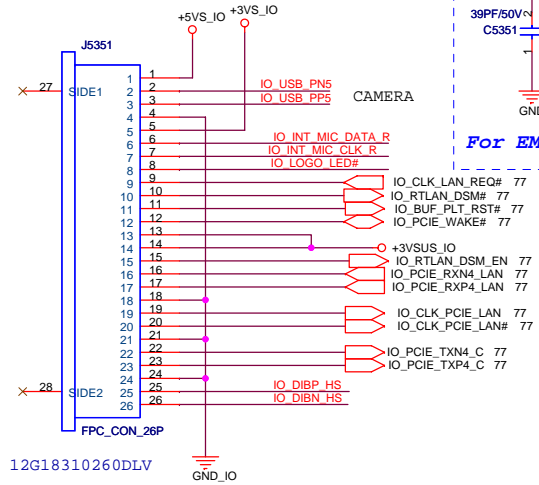




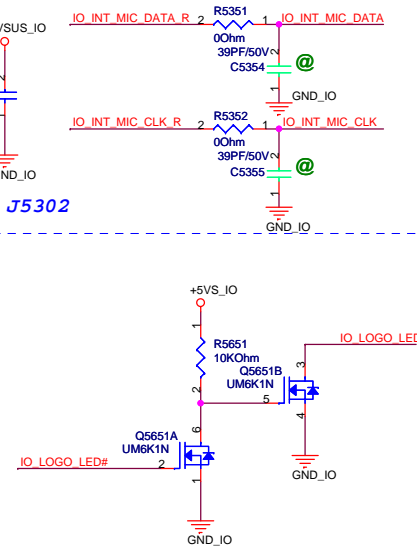
TRANSITION CAPS FOR VSYNC & HSYNC



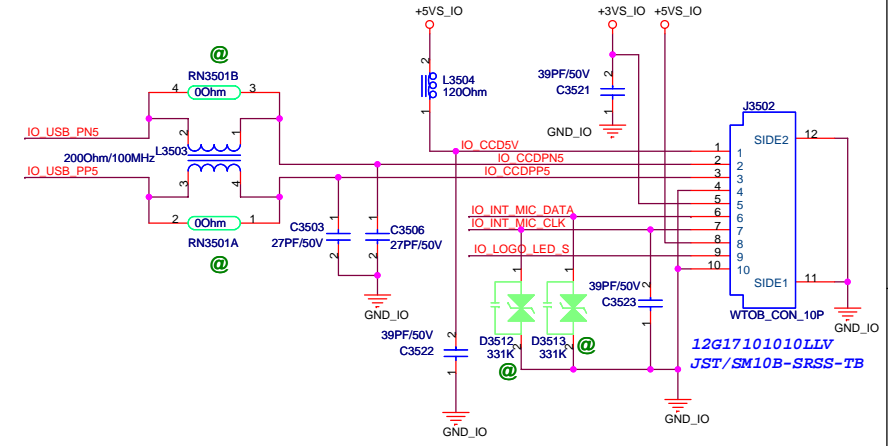
IO BOARD



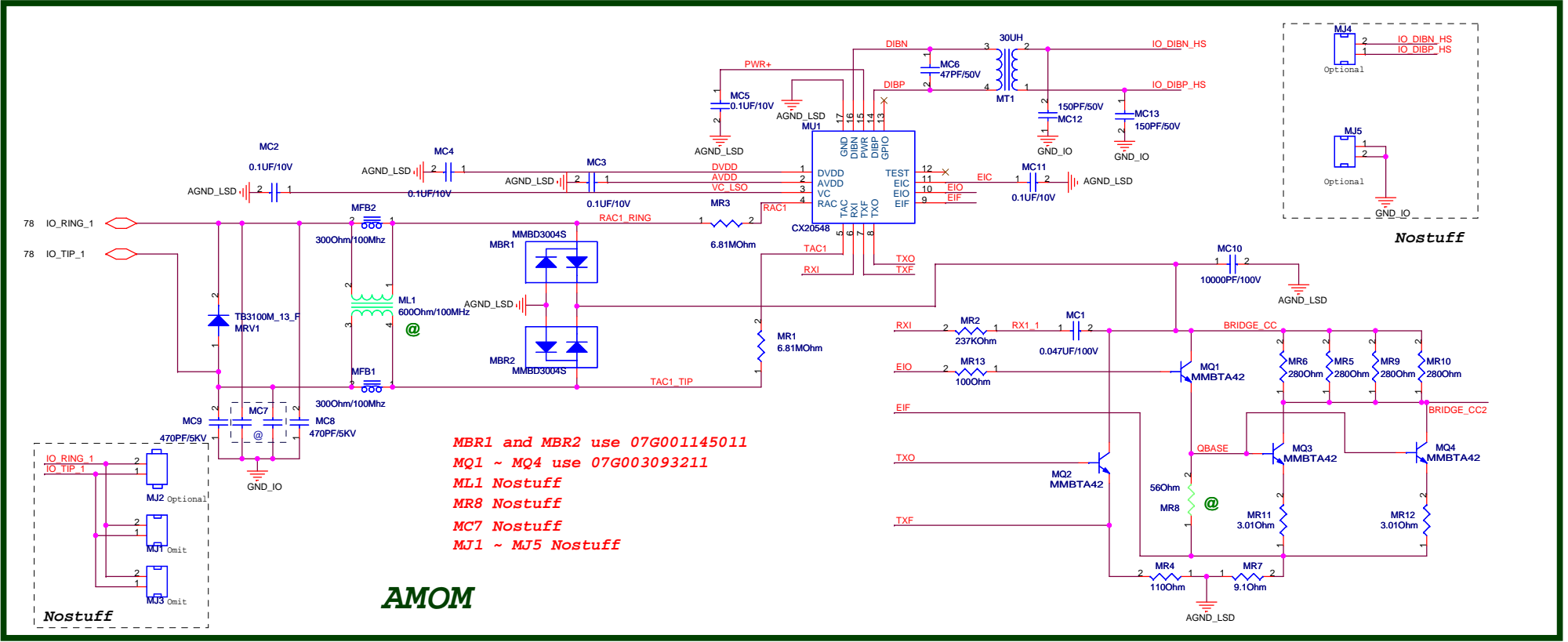
For EMI, Close to J5302



CAMERA



12G18310260DLV

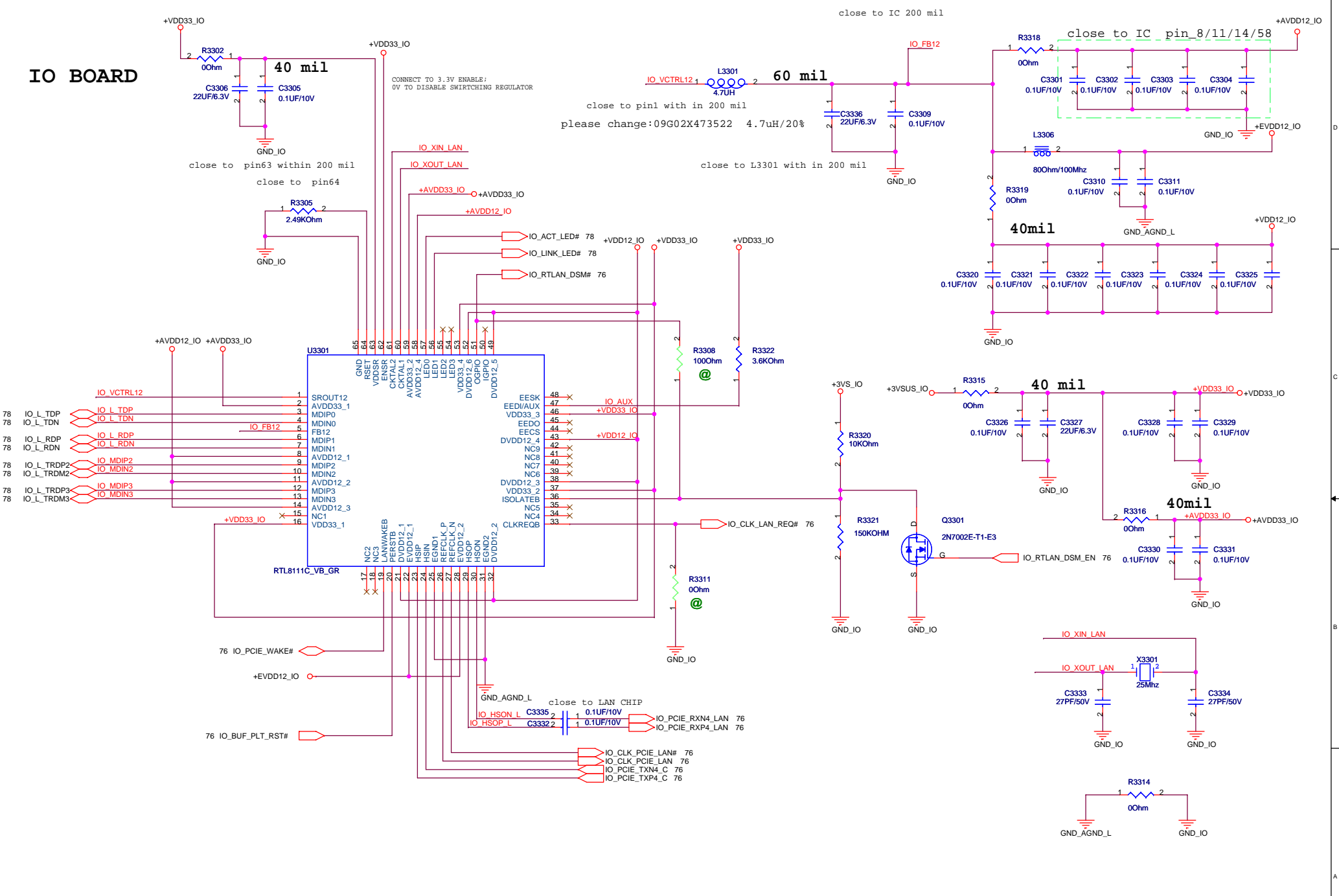


MBR1 and MBR2 use 07G001145011
 MQ1 ~ MQ4 use 07G003093211
 ML1 Nostuff
 MR8 Nostuff
 MC7 Nostuff
 MJ1 ~ MJ5 Nostuff

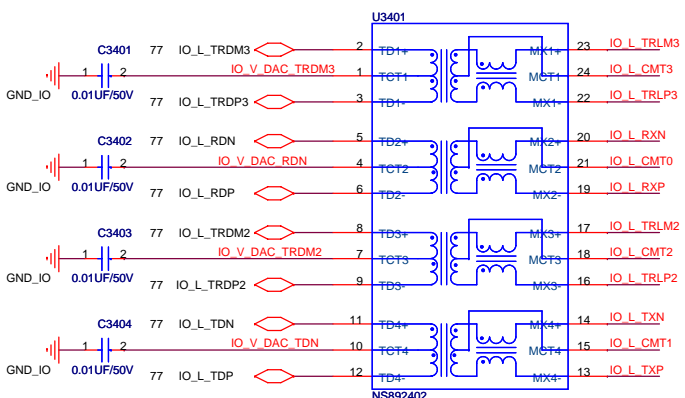
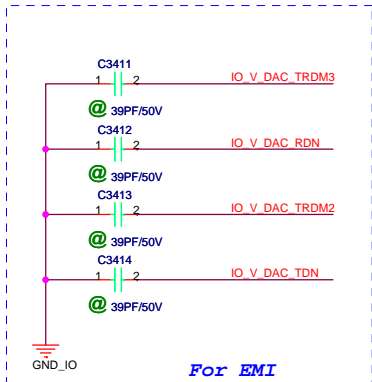
AMOM

| | | | |
|-----------------------------------|--|-----------------------------------|------------|
| ASUS | | Title : IO BRD CONN&DAA | |
| ASUSALPHA ODM NB1 | | Engineer: Warren | |
| Size Custom | Project Name Rocky 50 IO Board | Date: Thursday, December 20, 2007 | Rev 1.1 |
| Date: Thursday, December 20, 2007 | | Sheet 76 of 94 | |

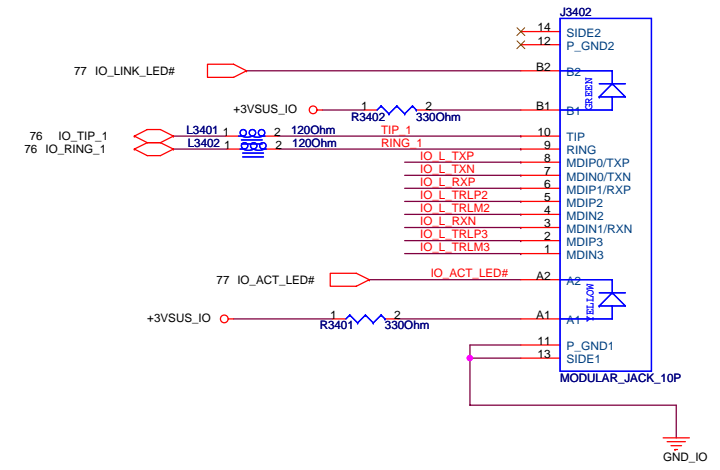
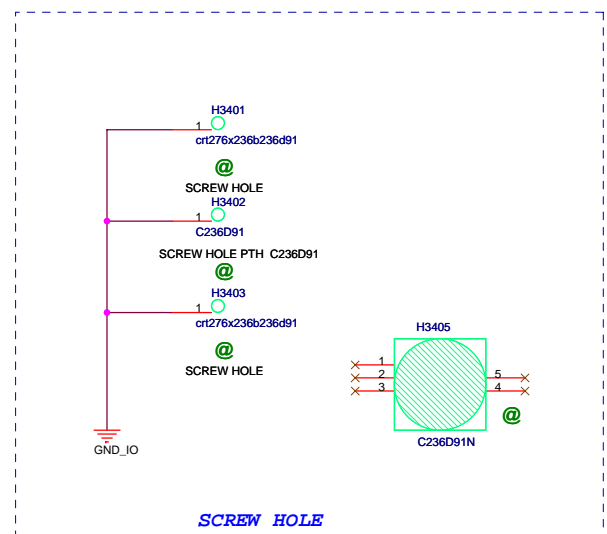
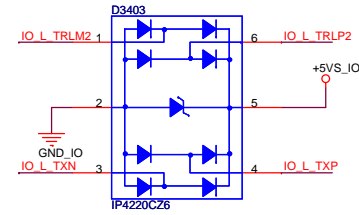
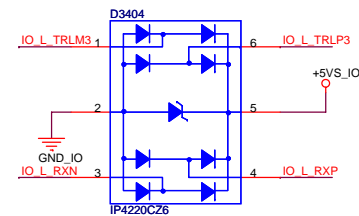
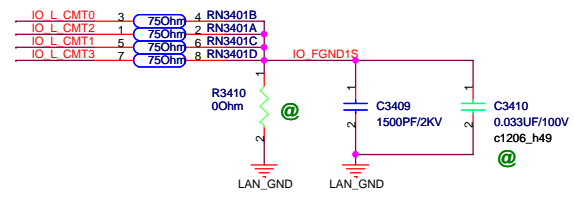
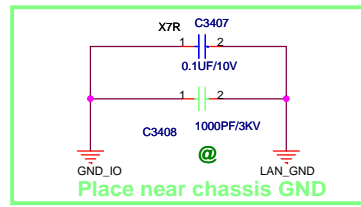
IO BOARD



IO BOARD



Transformer close CN3402



<Variant Name>

| | | |
|-----------------------------------|--|-------------------------|
| ASUS | | Title : LAN-RJ45 |
| ASUSTeK COMPUTER INC | | Engineer: Warren |
| Size Custom | Project Name Rocky 50 IO Board | Rev 1.1 |
| Date: Thursday, December 20, 2007 | Sheet | 78 of 94 |

| | | | | | |
|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | |
| C | | | | | |
| B | | | | | |
| A | | | | | |
| | 5 | 4 | 3 | 2 | 1 |



Title : History

Engineer: Tina Lee

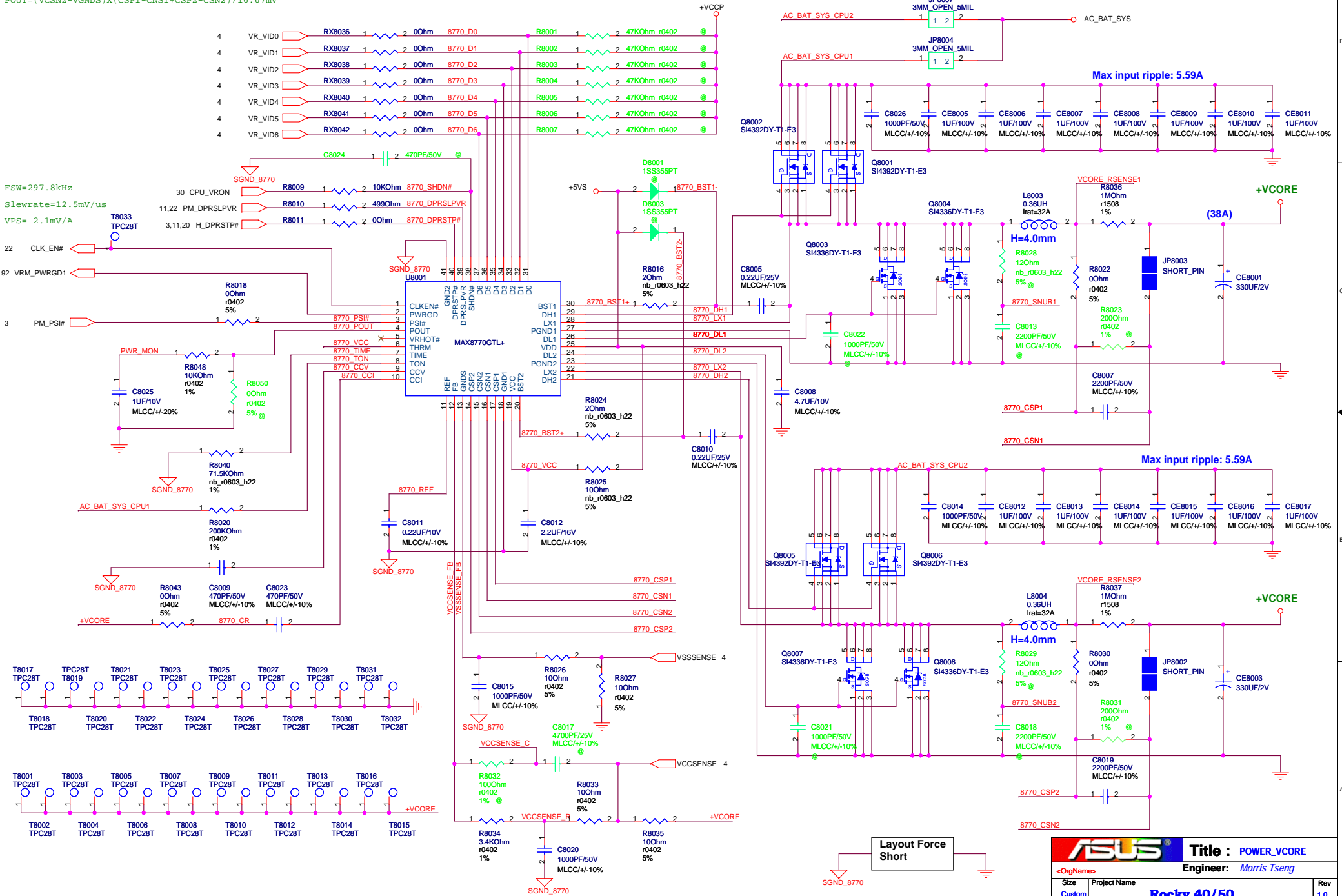
| | | |
|---------------------------------|--------------------|----------------|
| Size | Project Name | Rev |
| A | Rocky 40/50 | 1.0 |
| Date: Monday, December 17, 2007 | | Sheet 79 of 94 |

IMVP6 CPU VCORE REGULATOR

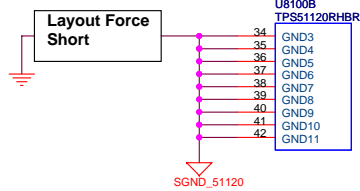
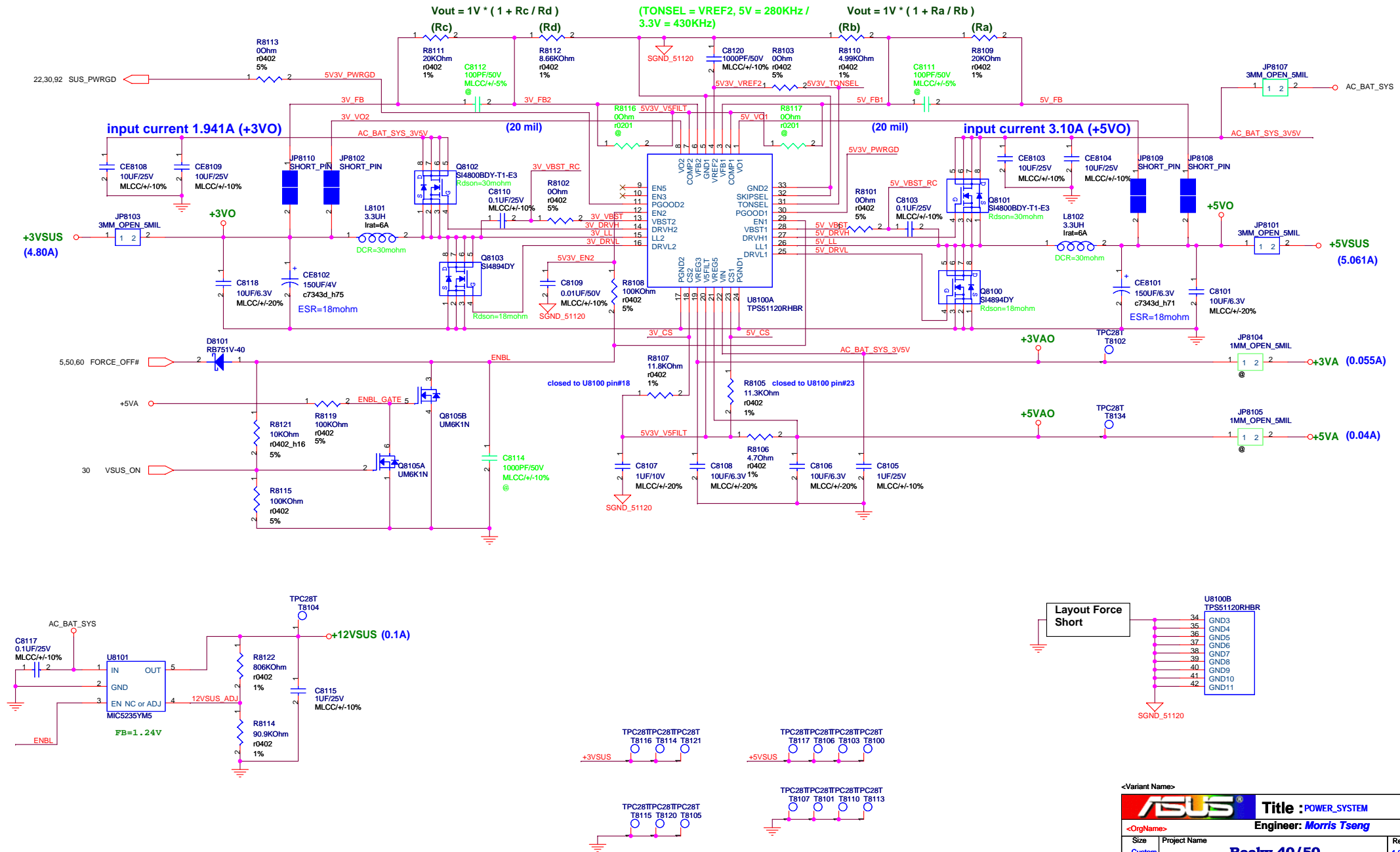
3.3V level logic level: DPRSLPVR, SHDN#

1.05V level logic: VID, PSI#, DPRSTP#

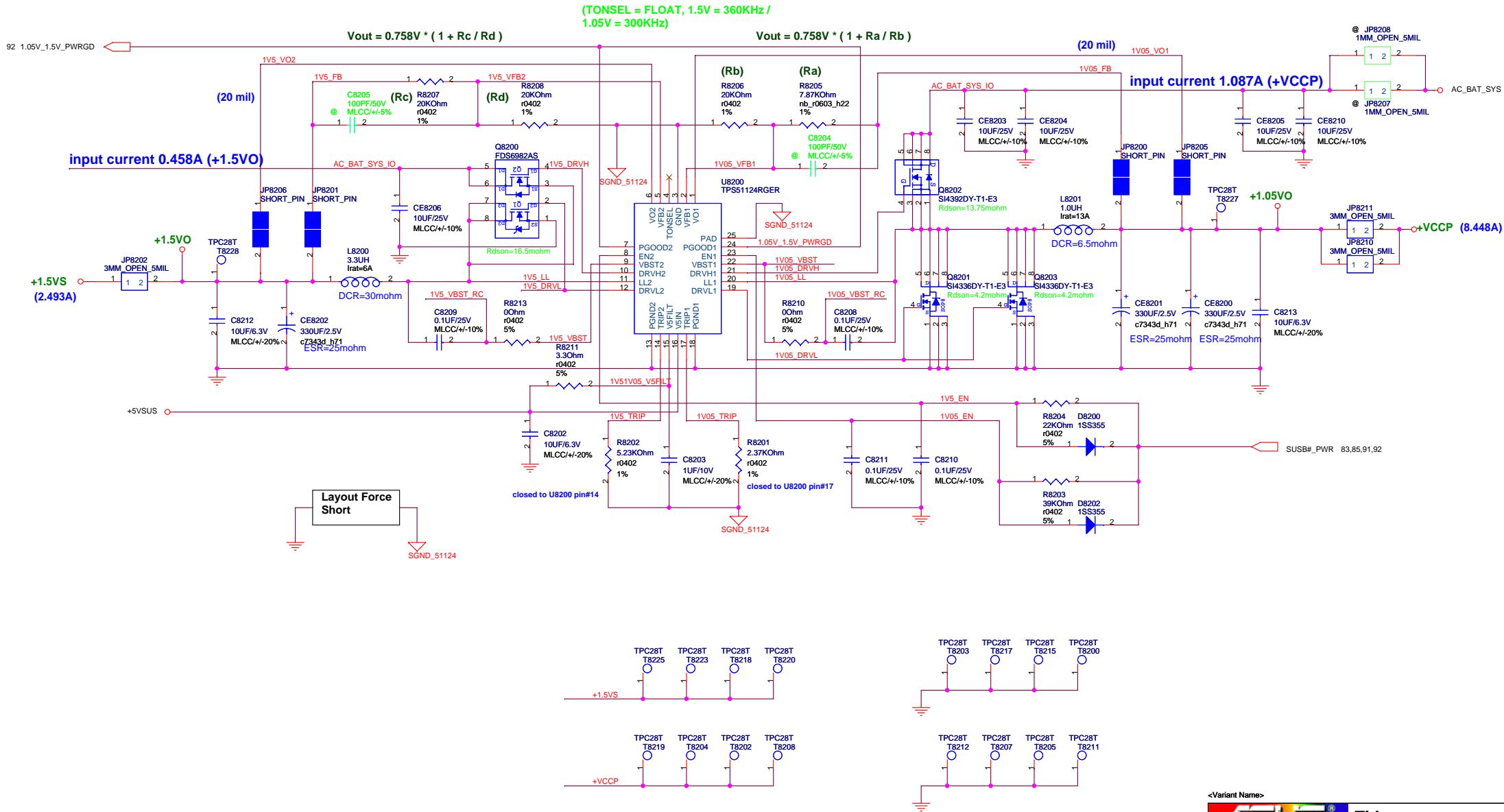
$POUT = (VCSN2 - VGND2) \times (CSP1 - CNS1 + CSP2 - CNS2) / 16.67mV$



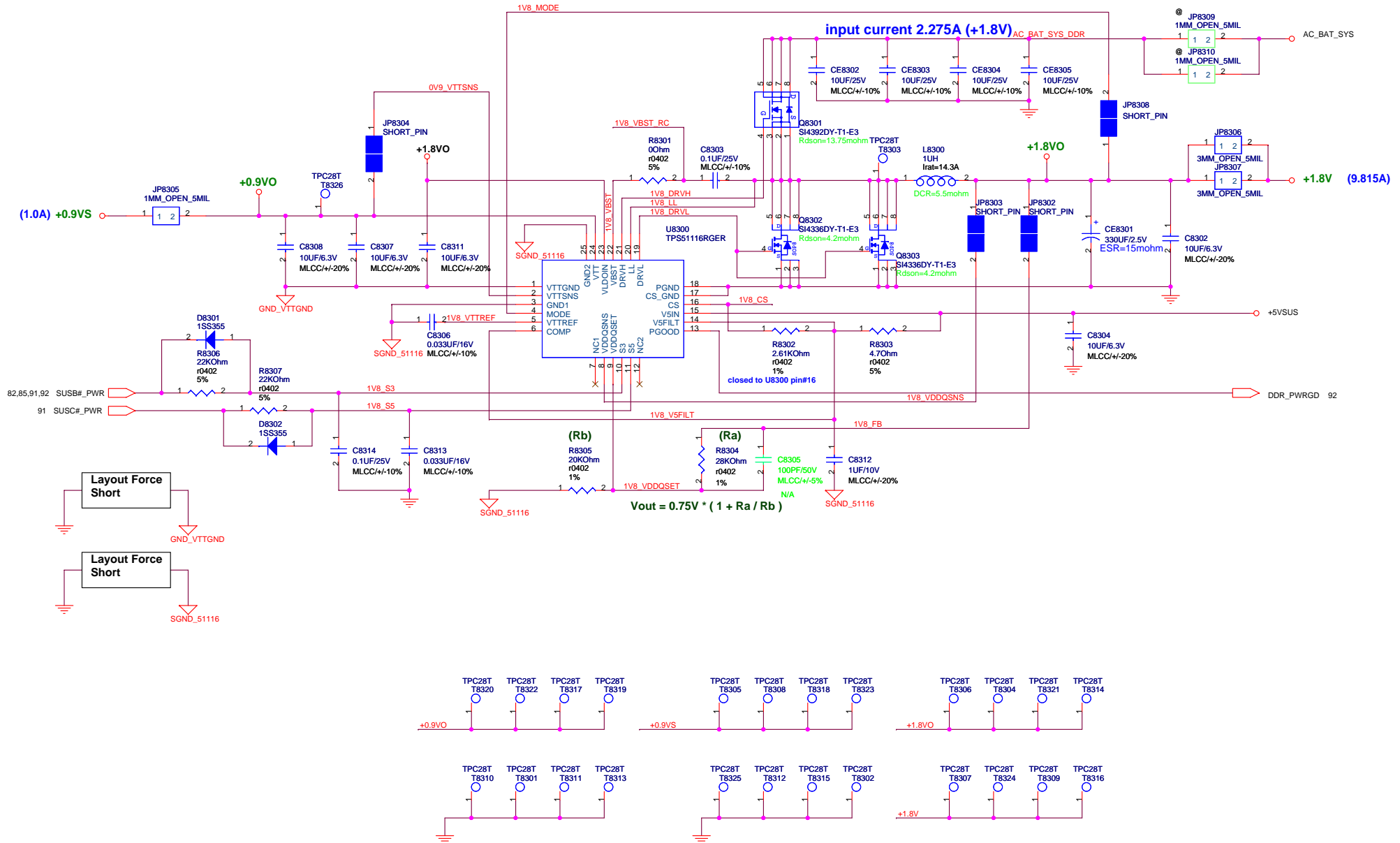
+5V / +3.3V POWER SUPPLY

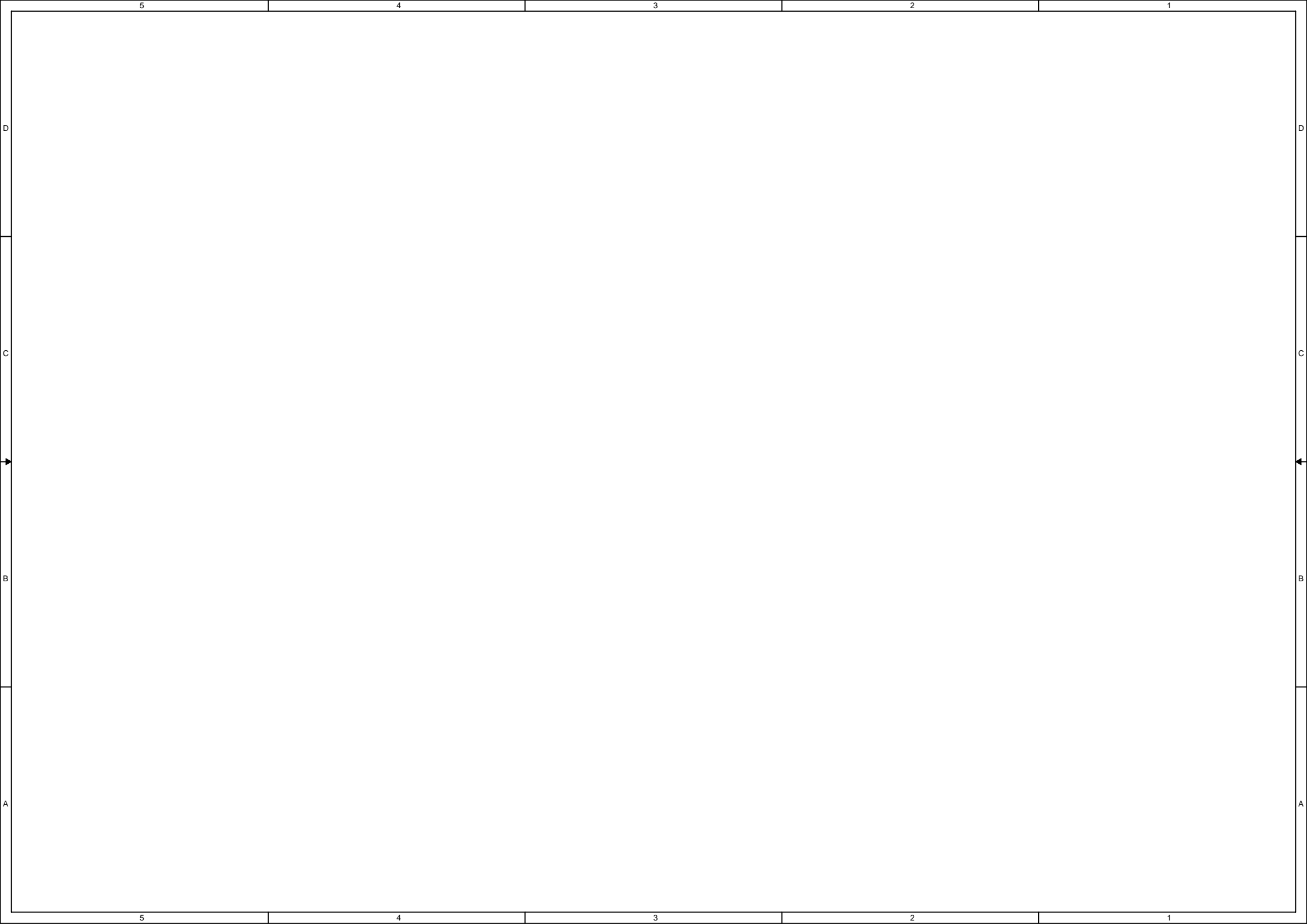


+1.5VS / +VCCP POWER SUPPLY



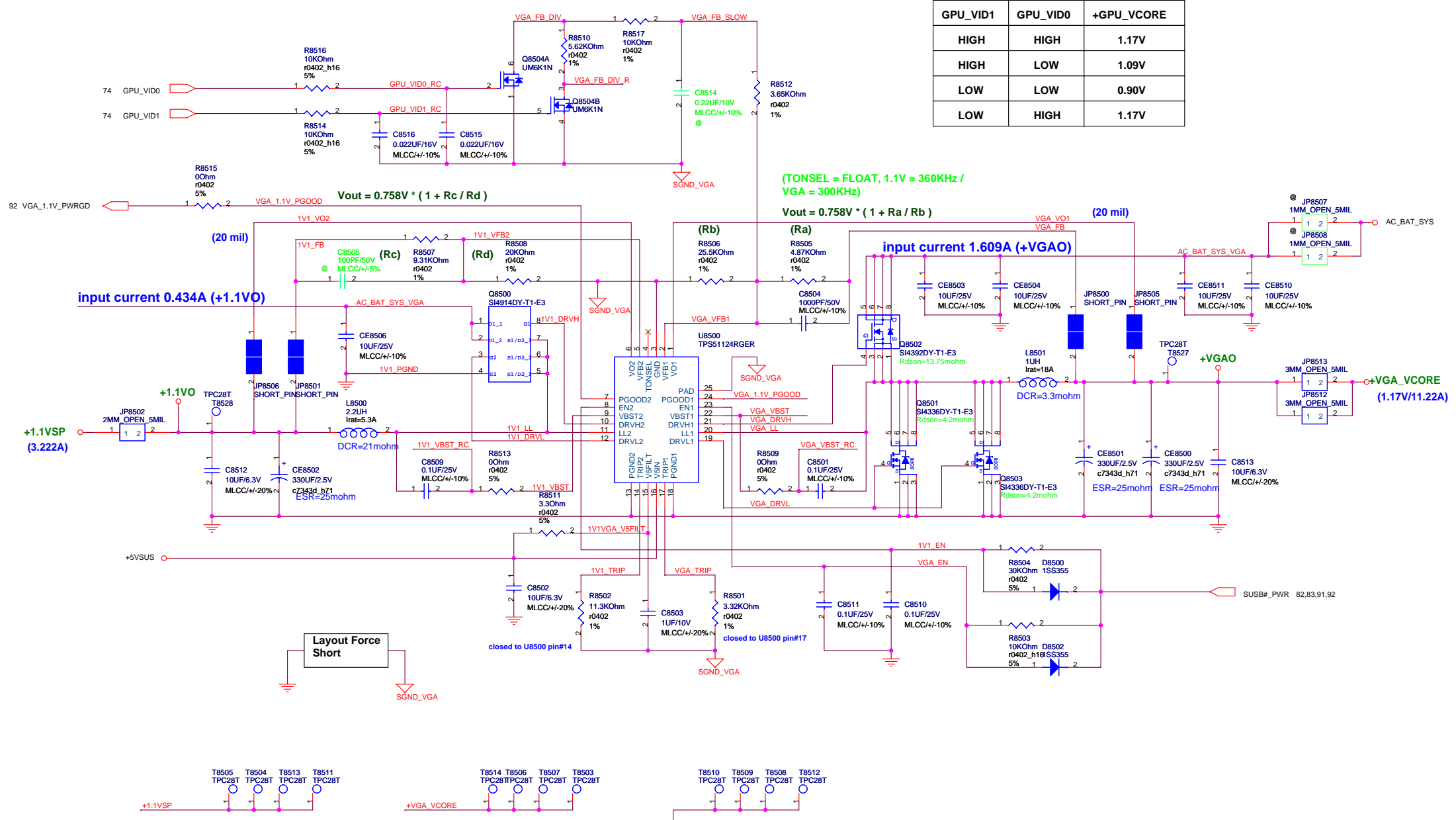
+1.8V / +0.9VS POWER SUPPLY





VGA / +1.1V POWER SUPPLY

| GPU_VID1 | GPU_VID0 | +GPU_VCORE |
|----------|----------|------------|
| HIGH | HIGH | 1.17V |
| HIGH | LOW | 1.09V |
| LOW | LOW | 0.90V |
| LOW | HIGH | 1.17V |



5

4

3

2

1

D

D

C


C

B

B

A

A

| | | |
|---|--------------------|-------------------------------|
|  | | Title : PWR_**** |
| <OrgName> | | Engineer: Morris Tseng |
| Size | Project Name | Rev |
| A4 | Rocky 40/50 | 1.0 |
| Date: Monday, December 17, 2007 | | Sheet 86 of 94 |

5

4

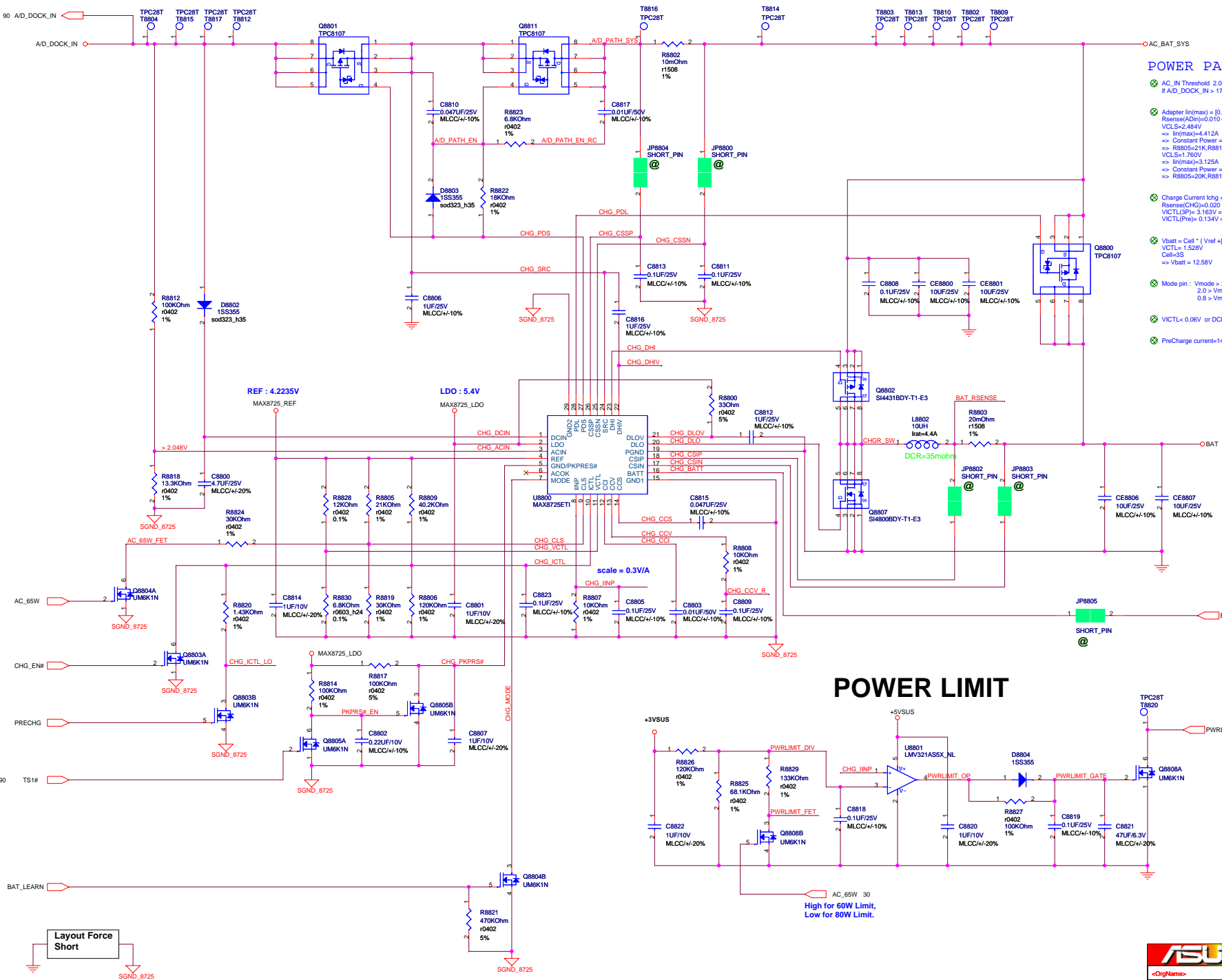
3

2

1

| | | | |
|---|--------------------|--------------------------------|----------|
|  | | Title : POWER_SHUTDOWN# | |
| <OrigName> | | Engineer: <i>Morris Tseng</i> | |
| Size | Project Name | Rev | |
| Custom | Rocky 40/50 | 1.0 | |
| Date: Monday, December 17, 2007 | | Sheet | 87 of 94 |

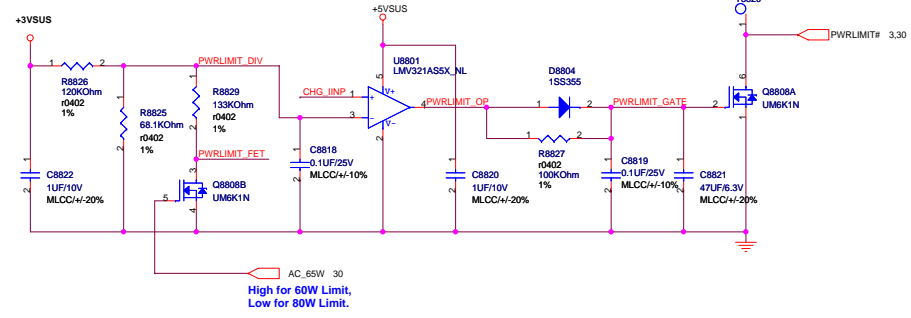
BATTERY CHARGER



POWER PATH & BAT_LEARN

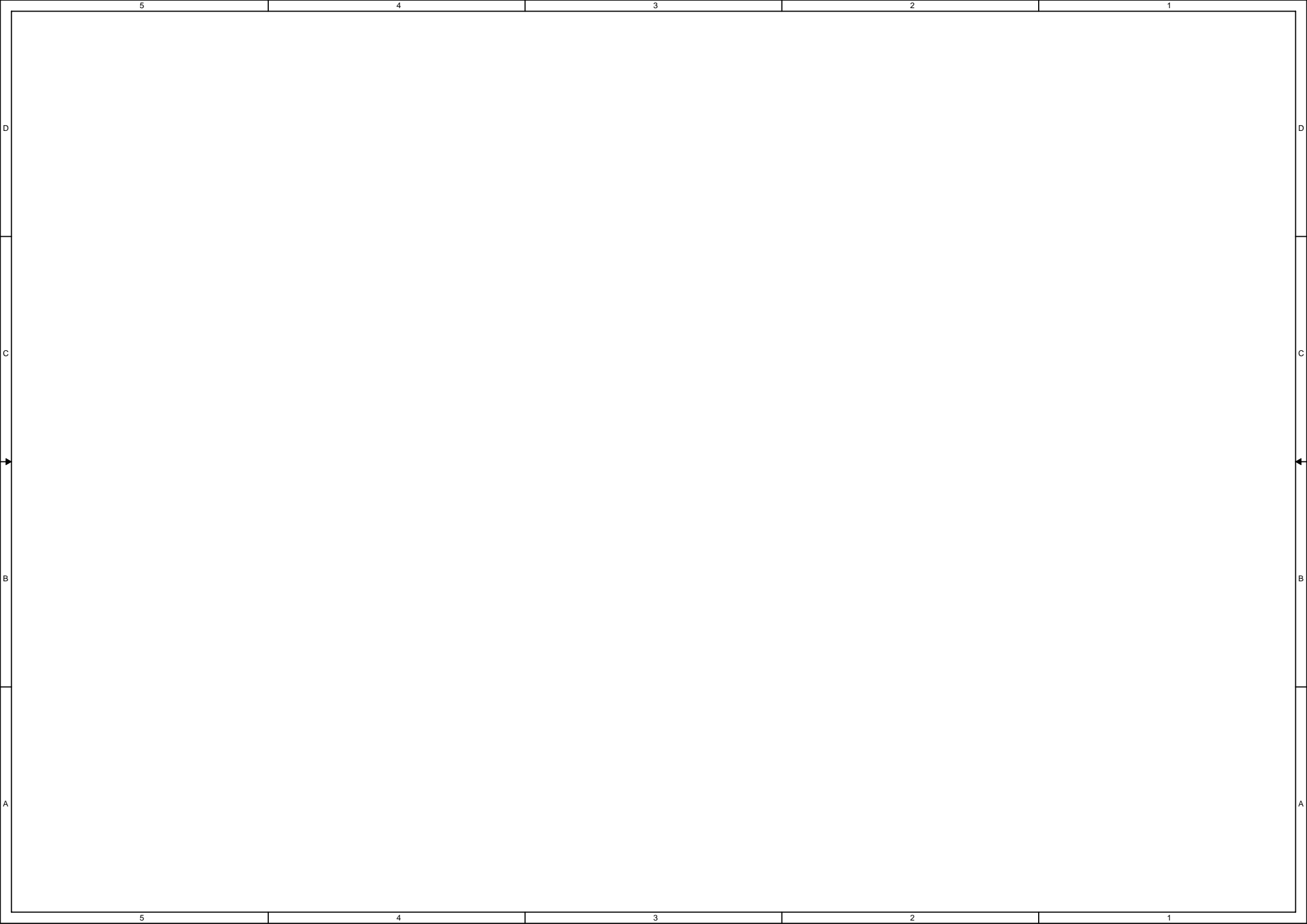
- AC_IN Threshold: 2.048V (max A/D_DOCK_IN > 17.44V active if A/D_DOCK_IN > 17.44V, AC_APR_UC goes to high)
- Adapter In(max) = $[0.075V / \text{Rsense(ADin)}] \cdot [VCL / \text{VREF}]$
 $\text{Rsense(ADin)} = 0.010 \text{ ohm}$
 $VCL = 2.454V$
 $\Rightarrow \text{In(max)} = 4.412A$
 $\Rightarrow \text{Constant Power} = 20 \cdot 4.412 = 88.24W$
 $\Rightarrow R8805 = 21K, R8819 = 30K$
 $VCL = 1.760V$
 $\Rightarrow \text{In(max)} = 3.125A$
 $\Rightarrow \text{Constant Power} = 20 \cdot 3.125 = 62.5W$
 $\Rightarrow R8805 = 20K, R8819 / R8824 = 15K$
- Charge Current $I_{chg} = [0.075V / \text{Rsense(CHG)}] \cdot [VICTL / 3.6V]$
 $\text{Rsense(CHG)} = 0.020 \text{ ohm}$
 $VICTL(Pr) = 5.163V \Rightarrow I_{chg} = 3.296A$
 $VICTL(Pr) = 0.134V \Rightarrow I_{chg} = 0.149A$
- $V_{bat} = \text{Cell} \cdot (V_{ref} + [VCTL - 1.8V] / 9.52)$
 $VCTL = 1.528V$
 $\text{Cell} = 3S$
 $\Rightarrow V_{bat} = 12.58V$
- Mode pin: $V_{mode} > 2.8V$ (tie to LDO pin) \rightarrow 4 Cells
 $2.0 > V_{mode} > 1.6V$ (floating) \rightarrow 3 Cells
 $0.8 > V_{mode}$ (tie to GND) \rightarrow Learning mode
- $VICTL < 0.06V$ or $DCIN < 7V$ \rightarrow Charger Disable
- PreCharge current = 149mA

POWER LIMIT

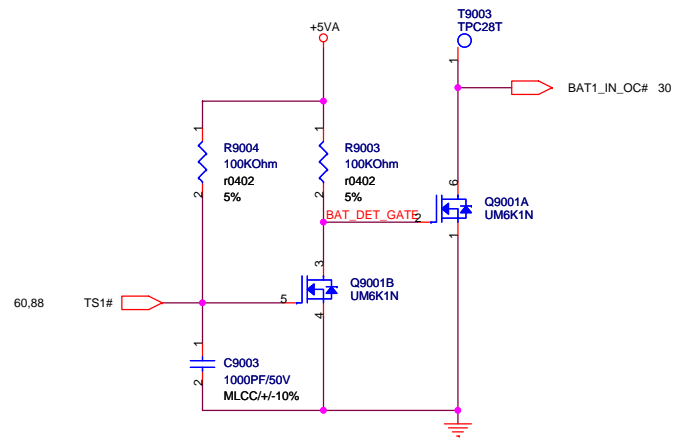


High for 60W Limit,
Low for 80W Limit.

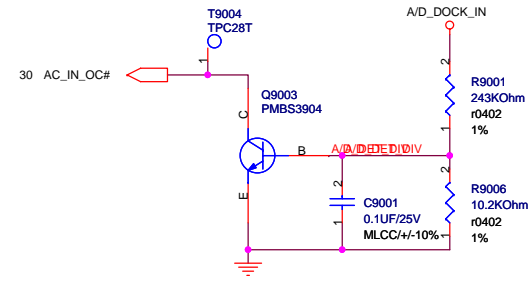
Layout Force Short



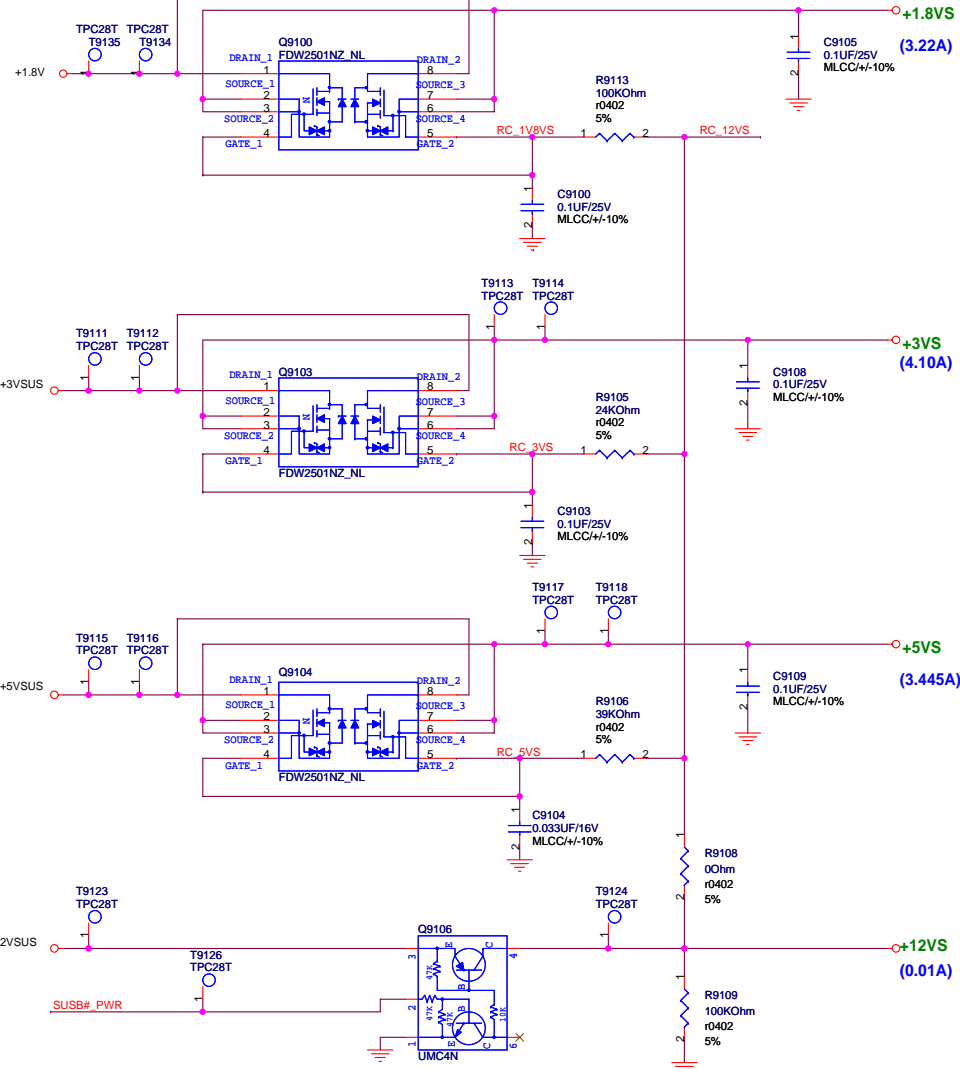
BATTERY IN DETECT



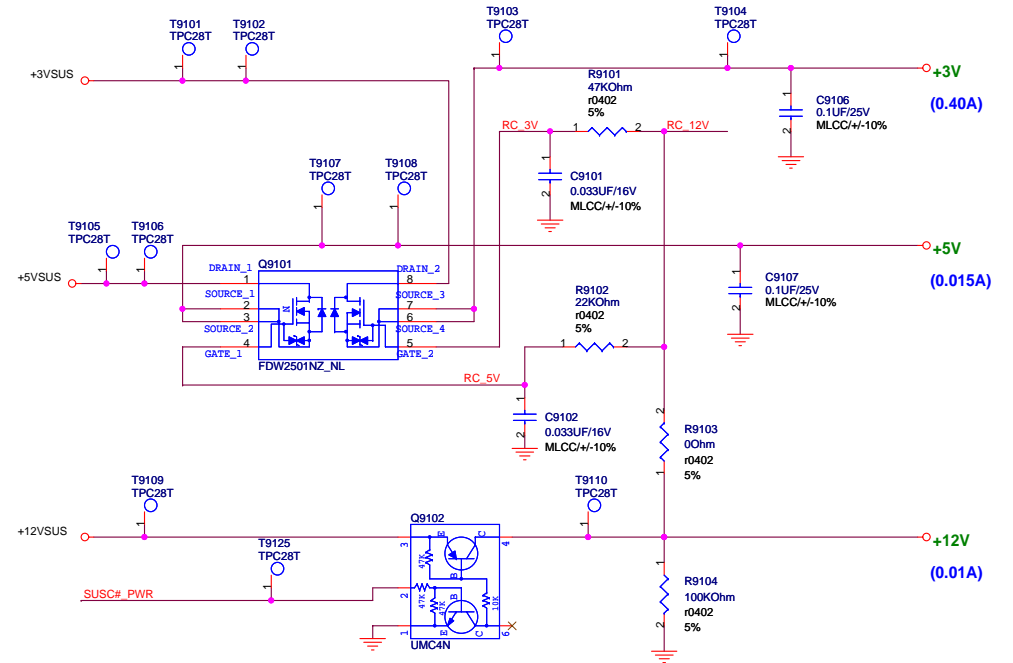
ADAPTER IN DETECT



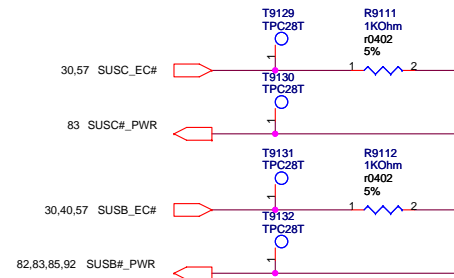
SUSB#_PWR Load SW



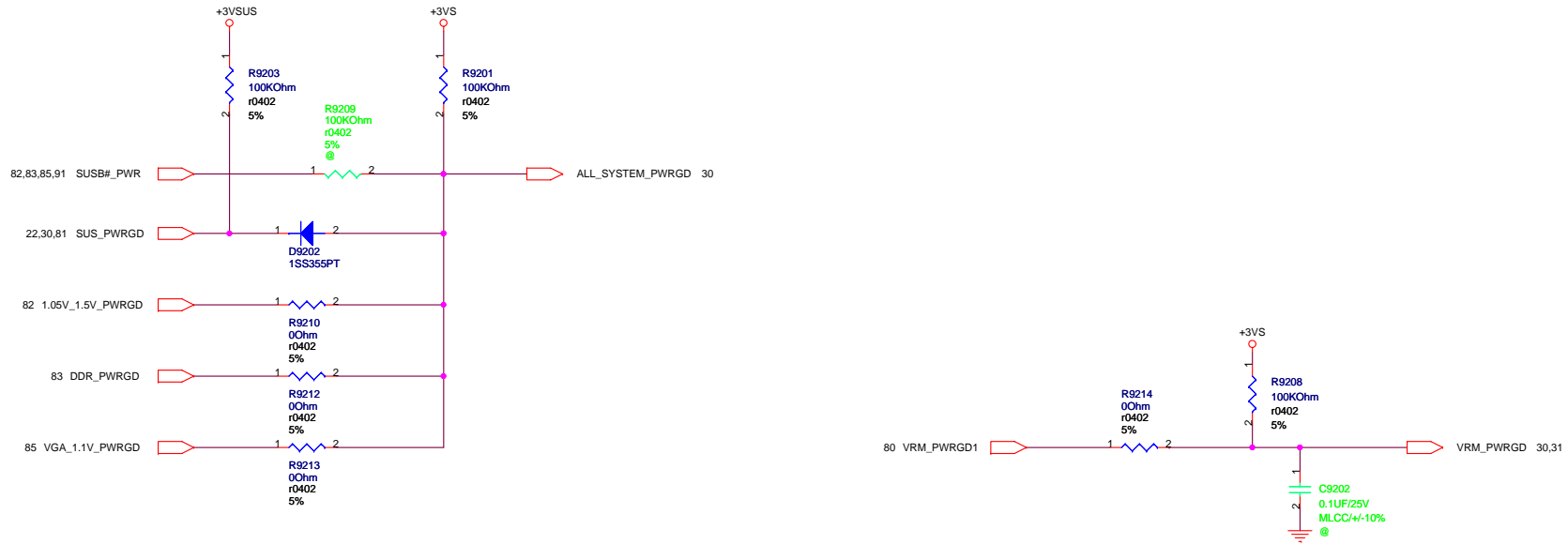
SUSC#_PWR Load SW

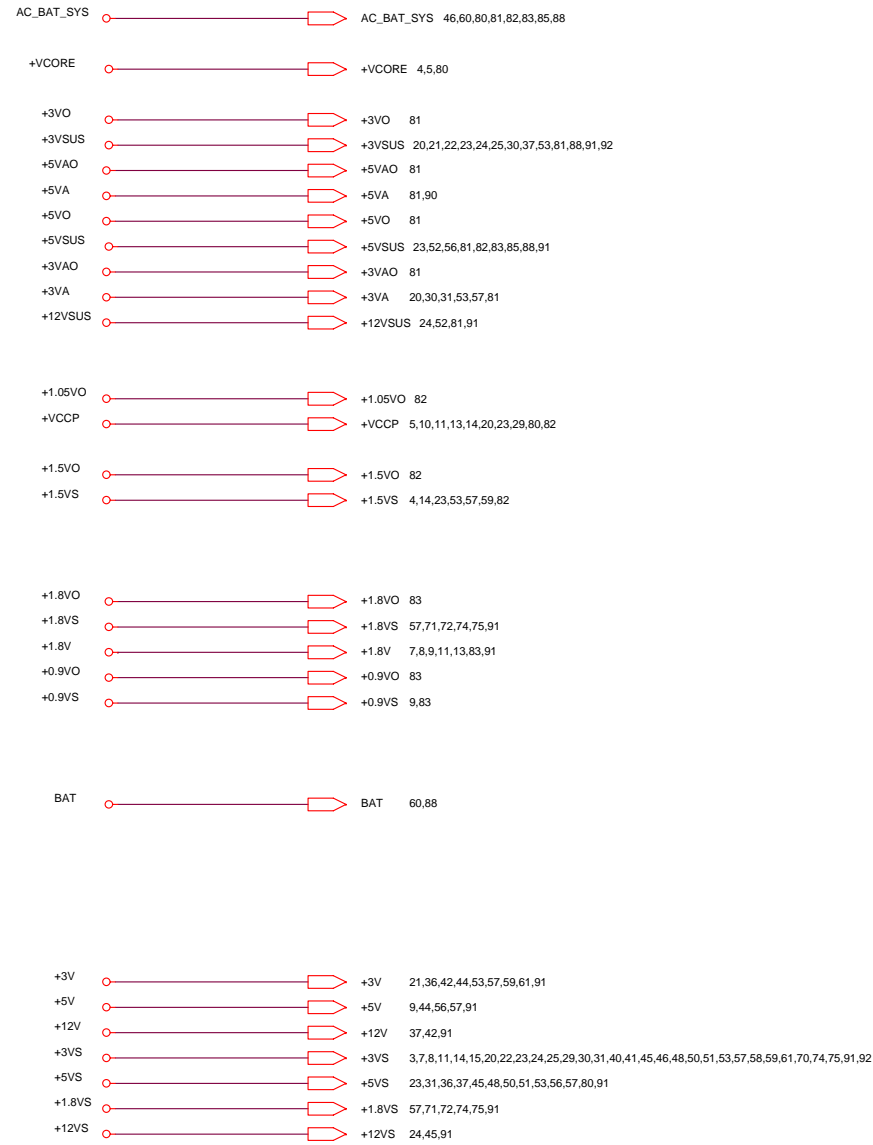


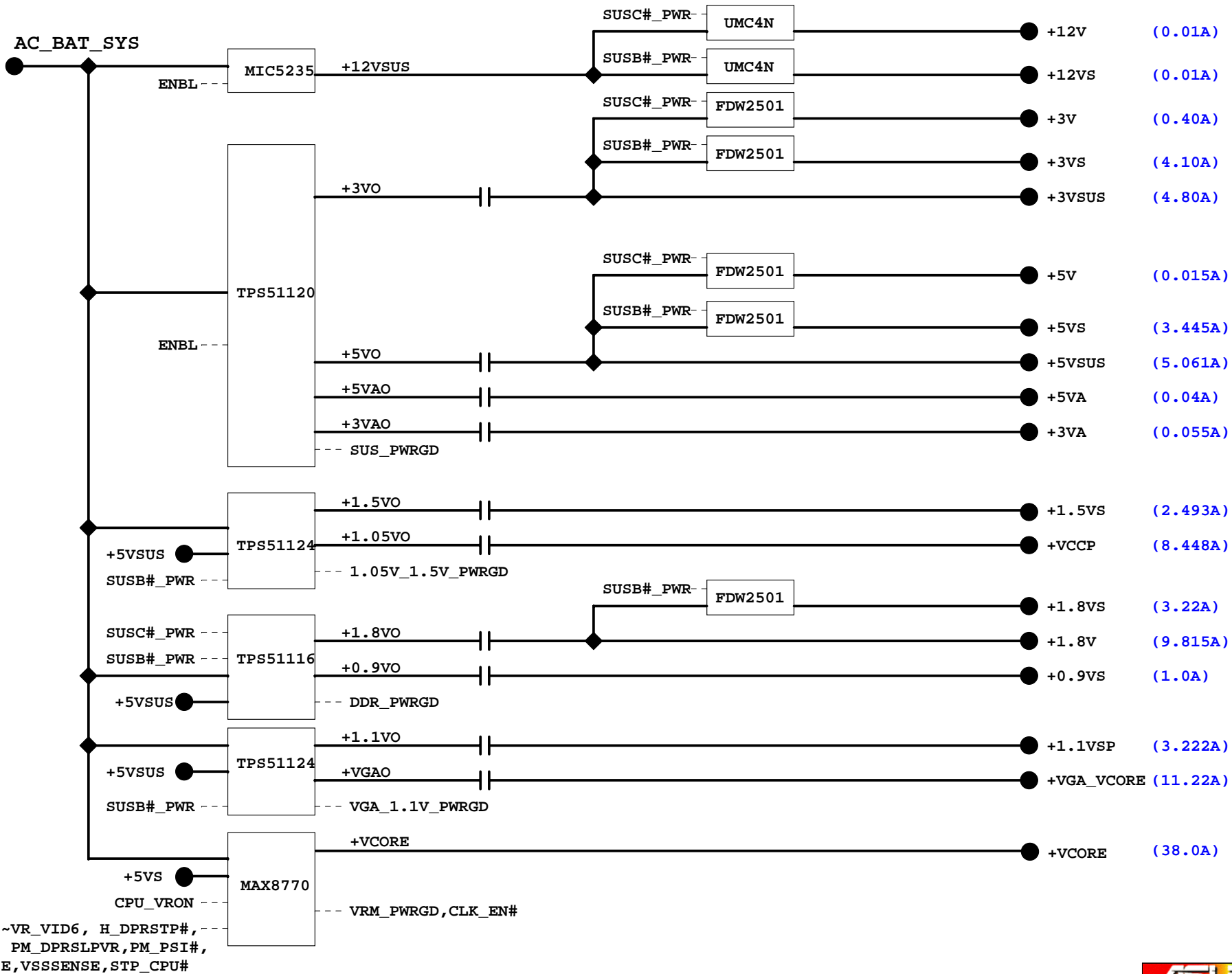
Enable Signal



POWER GOOD DETECTOR







VR_VID0~VR_VID6, H_DPRSTP#,
MCH_OK, PM DPRSLPVR, PM_PSI#,
VCCSENSE, VSSSENSE, STP_CPU#