Audi R0AA SYSTEM DIAGRAM

+3.3V/+5V(TPS51125ARGER) Page 46
+1.1V_SUS(RT8228AZ) Page 44
+1.5_DDR/0.75(TPS51216RUKR) Page 42
+2.5V_RUN(G9334TB1U) Page 41
+CPU VCORE(OZ8321LN) Page 45
+1.2V_VDDPR(RT8228AZ) Page 43
Charger(BQ24707ARGRR) Page 40
+VCC_DGFX_CORE(NCP5269) Page 45

SODIMM0 Max. 4GB Page 13
Dual Channel 1333/1600Mhz
DDR3 Channel A

SODIMM1 Max. 4GB Page 14
Dual Channel 1333/1600Mhz
DDR3 Channel B

AMD
35W
Socket FS1r2-Trinity APU (CPU + GPU)
uPGA 722 pin
Page 3~7

DP2 → HDMI Page 24

DP0 → TRAVIS AX3112 Page 27 → Travis LVDS → LVDS Page 22

P_GFX[0:7] → AMD Thames - Pro
29mm X 29mm
TDP 15~22W
Page 15~19
DDR3 900MHz → VRAM 64x16x8,128bit

THERMAL G781-1P8

IO Board
RJ45 → LAN AR8162 10/100 Page 29 → PCI-E

IO Board
WLAN WiFi+BT4.0 Page 29

Card Reader RTS 5179 Page 26
Webcam Page 22

USB 2.0

IO
USB3.0&2.0 Combo portX1 Page 29
USB3.0&2.0 Combo port Debug port USB Share Page 25
USB3.0&2.0 Combo port_x2 Page 25 & 38

USB 3.0

UMI
DP1
DP to VGA

AMD
FCH
Hudson-M3
FCBGA 656 pin
Page 8~12

CRT → CRT Page 23
SATA0 → HDD Page 28
SATA1 → ODD Page 28

FAN & THERMAL
G990P11U & EMC1422
Page 35

PWR SW Page 34
SW Board

HOTKEY Page 33
HOTKEY Board

LPC → KBC ITE 8518 Page 31
KB Page 33
TP Page 33
TP Board
ROM 512 Byte Page 32

SPI → SPI ROM 4M Byte Page 32

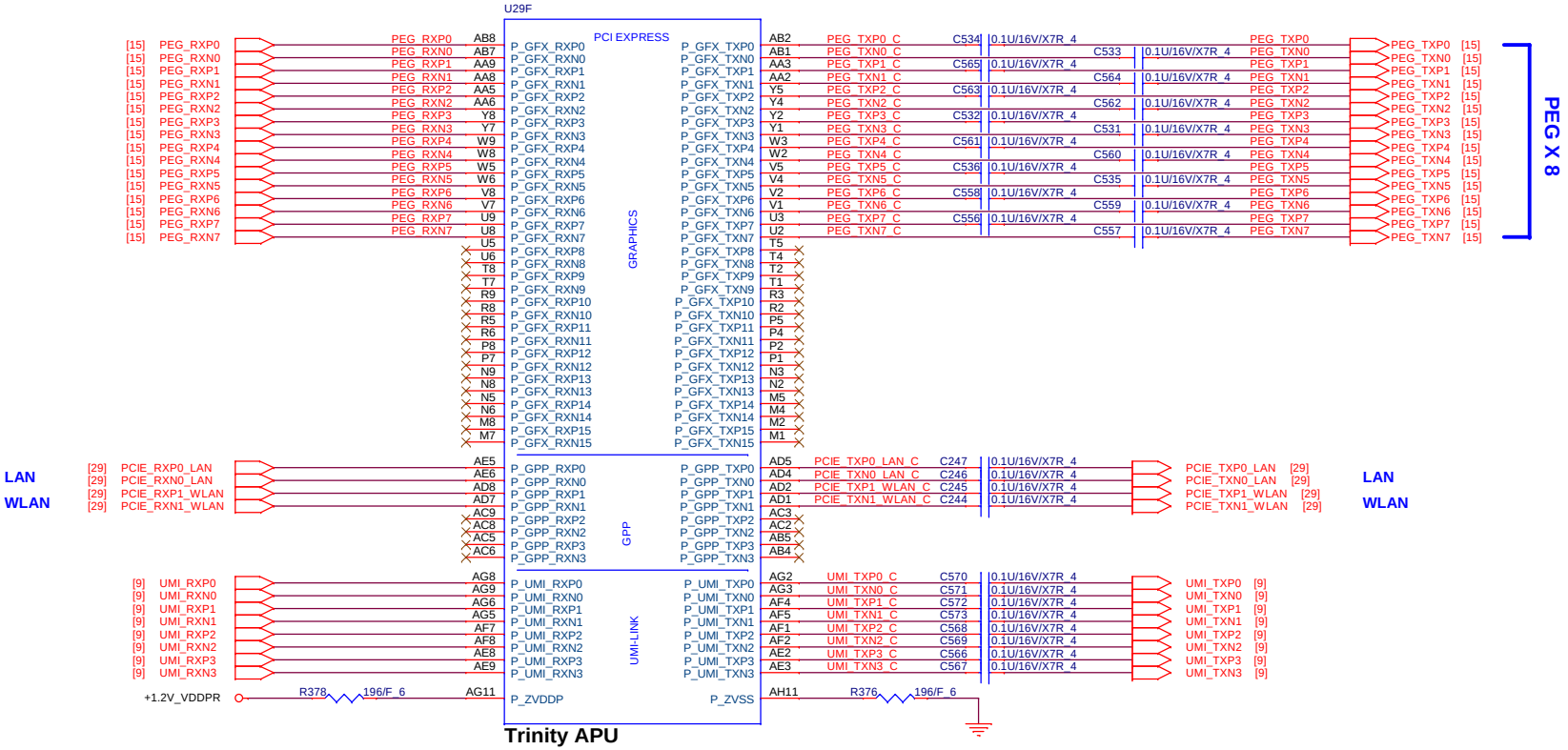
Azalia → AUDIO CODEC CX20672-21Z Page 30
SPEAKER 2W Page 30
HP/MIC Page 30
DIGITAL MIC Page 22

Quanta Computer Inc.
PROJECT : R0AA
Size | Document Number: Block Diagram | Rev B
Date: Monday, June 25, 2012 | Sheet 1 of 55

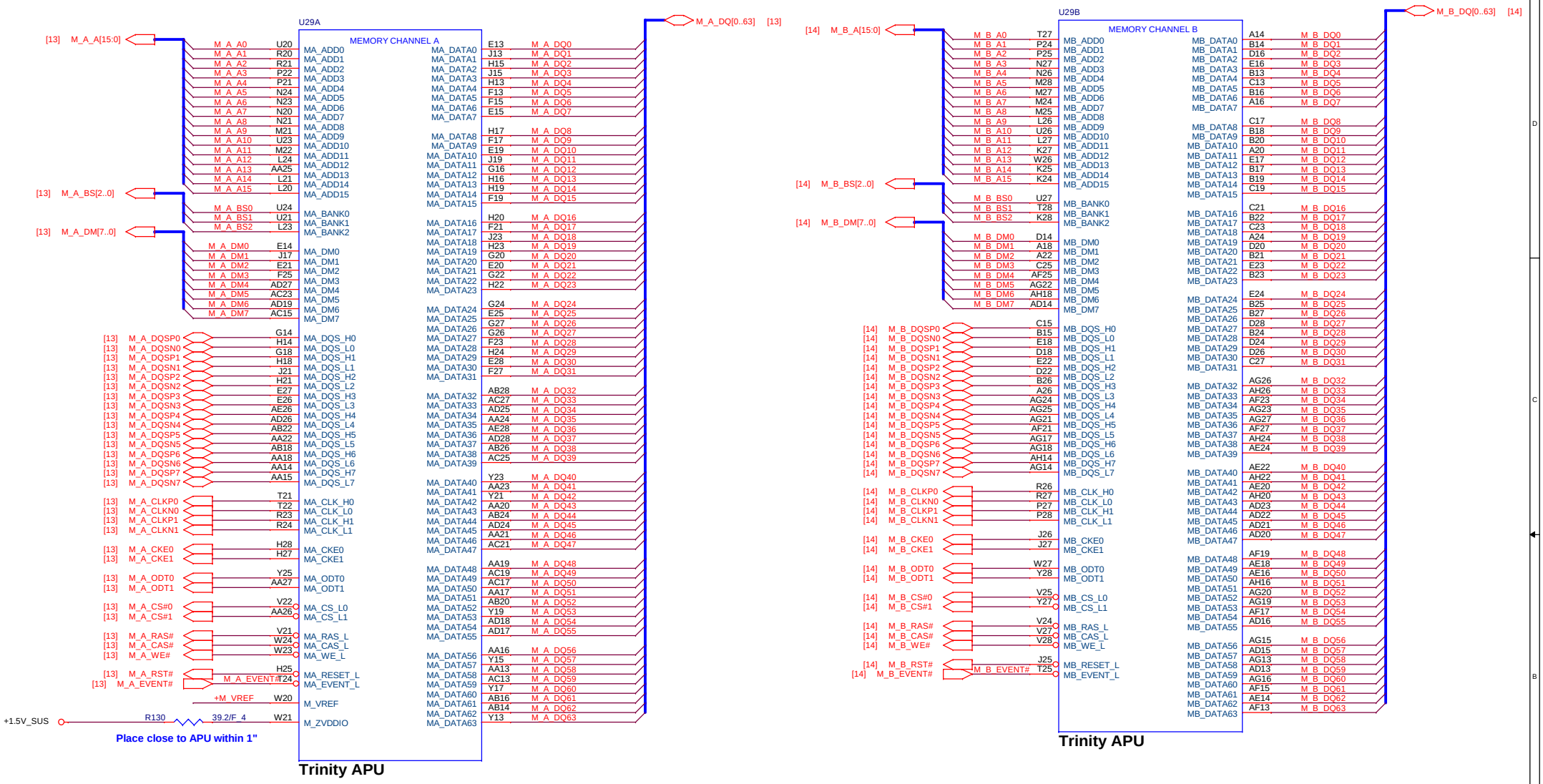
USB Master	Port Assignment
USB0	DEBUG
USB1	MiniCard 1 (WLAN/BT)
USB2	NC
USB3	NC
USB4	NC
USB5	NC
USB6	NC
USB7	Card Reader
USB8	NC
USB9	Camera
USB10	External port#1 (USB3.0)
USB11	External port#2 (USB3.0)
USB12	External port#3 (USB3.0)
USB13	External port#4 (Power share)

SATA Master	Port Assignment
SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

PCIE Master	Port Assignment
CPU_GPP 0	LAN
CPU_GPP 1	WLAN
CPU_GPP 2	NC
CPU_GPP 3	NC
FCH_GPP 0	NC
FCH_GPP 1	NC
FCH_GPP 2	NC
FCH_GPP 3	NC



Quanta Computer Inc.	
PROJECT : R0AA	
Size	Document Number: Trinity PCIE/UMI/GPP — Rev: B
Date: Monday, June 25, 2012	Sheet 3 of 55



Quanta Computer Inc.			
PROJECT : R0AA			
Size	Document Number		Rev
	DDR3 MEM I/F		B
Date: Monday, June 25, 2012	Sheet 4 of 55		

DP0 to LVDS

LVDS

DP1 to FCH VGA

VGA

HDMI

Note: CLK_APU_HCLKP/N is 100MHZ SSC

Note: CLK_DP_NSSCP/N is 100MHZ non-SSC

SVC	SVD	BOOT VOLTAGE VFIX@O2 VRM = GND	VFIX@O2 VRM = HIGH
0	0	1.1	1.4
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

U29C

ANALOG/DISPLAY/MISC

DISPLAY PORT 0 / DISPLAY PORT 1 / DISPLAY PORT 2 / DISPLAY PORT MISC. / CLK / TEST / SER. / CTRL / JTAG / RSVD / SENSE

Trinity APU

Stuff R371 R370

100K R near APU

HDMI Hot-plug

APU to Travis IC

CRT I2C to FCH

LVDS_HPD_Q

CRT Hot-plug

0926 Del Q11,R99,R98
R97 change to 0ohm, Add C614

FS1R2 pin is pulled low by insertion of a non-FS1r2 APU

Ib = (Vb - Vbe<sat>) / Rb => (1.5-0.7)/10=80uA
Ic = (Vc - Vce<sat>) / Rc => (3.3-0.25)/10=305uA

Ib >> (Ic / 40~70) => 80uA > 305/40 [BJT is on sat status]

Ib = (Vb - Vbe<sat>) / Rb => (1.5-0.7)/10=80uA
Ic = (Vc - Vce<sat>) / Rc => (5.0-0.25)/10=47.5uA

Ib >> (Ic / 40~70) => 80uA > 47.5/40 [BJT is on sat status]

QA

DMN5L06DWK
Vgs(th) = 1v , Rds(on) = 190 mΩ , Id = -3A

Vg= 1.5v, Vs= 0.3~1.5v, so MOS will turn on /off

M_TEST CONNECTION TBD

Test35 PU for Internal.
Test35 PD for Customer.

Debug only(Remove after MP)

Quanta Computer Inc.	
PROJECT : R0AA	
Size	Document Number: Display/Misc
Rev	B
Date: Monday, June 25, 2012	Sheet 5 of 55

APU POWER TABLE

PIN NAME	NET NAME	VOLTAGE
VDD	+VDD_CORE	+1.1V
VDDNB	+VDDNB_CORE	
VDDIO	+1.5VSUS	+1.5V
VDDP	+1.2V_VDDP	+1.2V
VDDR	+1.2V_VDDR	+1.2V
VDDA	+2.5V_VDDA	+2.5V

+VDD_CORE=36A

Sequence
GROUP A(VDDIO,VDDA)
↓↓↓
GROUP B(VDD_RUN, VDDNB_RUN, VDDP, VDDR)

+VDDNB_CORE=25A

VDDIO = 3.2A

VDDP_A + VDDP_B = 5

VDDA= 0.75A

VDDR = 1.2A

New Add Internal Regulator

Keep trace from Res to APU within 0.6"
Keep trace from Cap to APU within 1.2"

Trinity APU

BOTTOM SIDE DECOUPLING

If the VSS plane is cut to create a VDDIO plane, ceramic capacitors are connected across the VDDIO and VSS plane split as follows

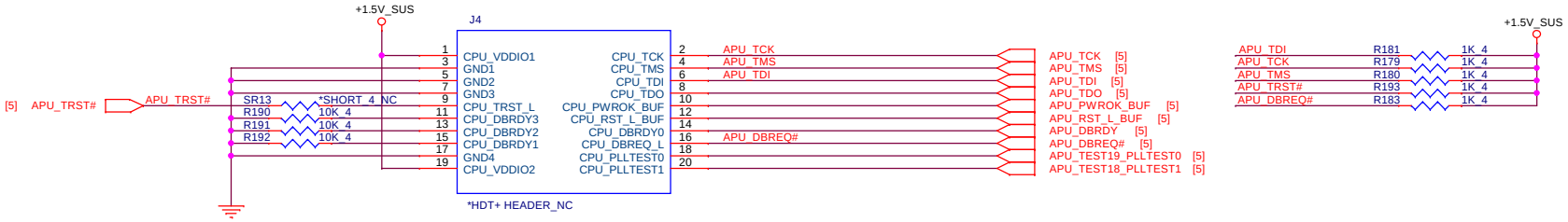
DECOUPLING between PROCESSOR and DIMMs

Across VDDIO and VSS split

Quanta Computer Inc.	
PROJECT : R0AA	
Size	Document Number: POWER/GND
Rev	B
Date: Monday, June 25, 2012	Sheet 6 of 55

HDT+ Connector Debug only

Remove after MP



Quanta Computer Inc.		
PROJECT : R0AA		
Size	Document Number: DEBUG&OTHER	Rev: B
Date: Monday, June 25, 2012	Sheet 7 of 55	

DEL MEMHOT# Function / +3.3V

USB_OC#

Function	FCH port
USB12 (MB)	USB_OC0#
USB13 (MB)	*USB_OC2#
USB11 (MB)	USB_OC1#
USB10 (I/O)	USB_OC6#

+3.3V_SUS

NC,no install by default

R43 *2.2K_4_NC FCH_TEST0
R46 *2.2K_4_NC FCH_TEST1
R30 *2.2K_4_NC FCH_TEST2
R283 *10K_4_NC SIO_SLP_S3#
R286 *10K_4_NC SIO_SLP_S5#
R31 10K_4 GEVENT#9
R48 10K_4 APU_THERMTRIP#

R301 *10K_4_NC AC_PRESENT
R288 10K_4 LLB#

AC_PRESENT high to enter S5+
LLB#, WAKE# and PWR_BTN
need pull up to 3.3V_S5+ (SUS) only if S5+ mode is supported

R289 10K_4 SIO_PWRBTN#
R27 10K_4 SMB_RUN_CLK1
R298 10K_4 SMB_RUN_DAT1
R62 10K_4 SMB_RUN_CLK2
R65 10K_4 SMB_RUN_DAT2
R33 10K_4 USB_OC0#
R304 10K_4 USB_OC1#
R35 10K_4 USB_OC2#
R32 10K_4 USB_OC6#
R275 *10K_4_NC SATA_ODD_PRSNT#
R270 *10K_4_NC SATA_ODD_MD#

R337 10K_4 SMB_LV_CLK
R334 10K_4 SMB_LV_DAT

+3.3V_RUN

R82 2.2K_4 SMB_RUN_CLK0
R83 2.2K_4 SMB_RUN_DAT0

R22 10K_4 FCH_PCIE_WLAN_CLKREQ#
R58 10K_4 EC_KBRST#
R218 10K_4 SIO_A20GATE

R61 10K_4 WD_PWRGD
R306 *10K_4_NC MEMHOT#
R333 *10K_4_NC SIO_EXT_SMI#

R54 10K_4 FCH_PCIE_LAN_CLKREQ#
R459 *10K_4_NC PEG_A_CLKRQ#

U26A

HUDSON-M2
Part 4 of 5

PCIE_RST2#/GEVENT4# ← MEMHOT# (AB6)
RI#/GEVENT22# ← TP51, TP47 (R2)
SPI_CS3#/GBE_STAT1/GEVENT21# (W7)
SLP_S3# ← SIO_SLP_S3# [31,42] (T3)
SLP_S5# ← SIO_SLP_S5# [31,42] (W2)
PWR_BTN# ← SIO_PWRBTN# [31] (J4)
PWR_GOOD ← FCH_PWRGD [36] (N7)

TEST0 ← FCH_TEST0 (T9)
TEST1/TMS ← FCH_TEST1 (T10)
TEST2 ← FCH_TEST2 (V9)
GA20IN/GEVENT0# ← SIO_A20GATE (AE22)
KBRST#/GEVENT1# ← EC_KBRST# [31] (AG19)
PME#/GEVENT3# ← SIO_EXT_SCI# [31] (R9)
LPC_SMI#/GEVENT23# ← SIO_EXT_SMI# [31] (C26)
LPC_PD#/GEVENT5# ← TP45 (T5)
SYS_RESET#/GEVENT19# ← TP43 (U4)
WAKE#/GEVENT8# ← SIO_EXT_WAKE# [31] (K1)
IR_RX1/GEVENT20# (V2)
THRMTRIP#/SMBALERT#/GEVENT2# ← APU_THERMTRIP# (R10)
WD_PWRGD ← WD_PWRGD (AF19)
RSMRST# ← RSMRST# [31] via R276 10K_4 (U2)

CLK_REQ4#/SATA_IS0#/GPIO64 ← FCH_PCIE_LAN_CLKREQ# [29] (AG24)
CLK_REQ3#/SATA_IS1#/GPIO63 (AE24)
SMARTVOLT1/SATA_IS2#/GPIO50 ← TP53 (AE26)
CLK_REQ0#/SATA_IS3#/GPIO60 (AF23)
SATA_IS4#/FANOUT3/GPIO55 (AH17)
SATA_IS5#/FANIN3/GPIO59 (AG18)
SPKR/GPIO66 ← ACZ_SPKR [30] (AF24)
SCL0/GPIO43 ← SMB_RUN_CLK0 [13,14,33] (AD26)
SDA0/GPIO47 ← SMB_RUN_DAT0 [13,14,33] (AD25)
SCL1/GPIO227 ← SMB_RUN_CLK1 (T7)
SDA1/GPIO228 ← SMB_RUN_DAT1 (R7)
CLK_REQ2#/FANIN4/GPIO62 (AG25)
CLK_REQ1#/FANOUT4/GPIO61 ← FCH_PCIE_WLAN_CLKREQ# [29] (AG22)
IR_LED#/LLB#/GPIO184 ← LLB# (J2)
SMARTVOLT2/SHUTDOWN#/GPIO51 (AG26)
DDR3_RST#/GEVENT7#/VGA_PD ← VGA_PD [11] (V8)
GBE_LED0/GPIO183 (W8)
SPI_HOLD#/GBE_LED1/GEVENT9# ← SPI_HOLD# [32] via SR4 *SHORT_4_NC (Y6)
GBE_LED2/GEVENT10# (V10)
GBE_STAT0/GEVENT11# (AA8)
CLK_REQG#/GPIO65/OSCIN/IDLEEXIT# ← PEG_A_CLKRQ# [15] (AF25)

BLINK/USB_OC7#/GEVENT18# (M7)
USB_OC6#/IR_TX1/GEVENT6# ← USB_OC6# [29] (R8)
USB_OC5#/IR_TX0/GEVENT17# ← SATA_ODD_PRSNT# [28] (T1)
USB_OC4#/IR_RX0/GEVENT16# ← SATA_ODD_MD# [28] (P6)
USB_OC3#/AC_PRES/TDO/GEVENT15# ← AC_PRESENT [16,31] (F5)
USB_OC2#/TCK/GEVENT14# ← USB_OC2# [25] (P5)
USB_OC1#/TDI/GEVENT13# ← USB_OC1# [38] (J7)
USB_OC0#/SPI_TPM_CS#/TRST#/GEVENT12# ← USB_OC0# [25] (T8)

AZ_BITCLK ← ACZ_BITCLK [30] via EC45 *22P/50V_4_NC, 27, ER20 33_4, R285 33_4 (AB3)
AZ_SDOUT ← ACZ_SDOUT [30] via ACZ_BITCLK_R, ACZ_SDOUT_R (AB1)
AZ_SDIN0/GPIO167 ← ACZ_SDIN0 [30] (AA2)
AZ_SDIN1/GPIO168 (Y5)
AZ_SDIN2/GPIO169 (Y3)
AZ_SDIN3/GPIO170 (Y1)
AZ_SYNC ← ACZ_SYNC [30] via R279 33_4, ACZ_SYNC_R (AD6)
AZ_RST# ← ACZ_RST# [30] via R280 33_4, ACZ_RST#_R (AE4)

PS2_DAT/SDA4/GPIO187 (K19)
PS2_CLK/CEC/SCL4/GPIO188 (J19)
SPI_CS2#/GBE_STAT2/GPIO166 (J21)

PS2KB_DAT/GPIO189 (D21)
PS2KB_CLK/GPIO190 (C20)
PS2M_DAT/GPIO191 (D23)
PS2M_CLK/GPIO192 (C22)

KSO_0/GPIO209 (F21)
KSO_1/GPIO210 (E20)
KSO_2/GPIO211 (F20)
KSO_3/GPIO212 (A22)
KSO_4/GPIO213 (E18)
KSO_5/GPIO214 (A20)
KSO_6/GPIO215 (J18)
KSO_7/GPIO216 (H18)
KSO_8/GPIO217 (G18)
KSO_9/GPIO218 (B21)
KSO_10/GPIO219 (K18)
KSO_11/GPIO220 (D19)
KSO_12/GPIO221 (A18)
KSO_13/GPIO222 (C18)
KSO_14/XDB0/GPIO223 (B19)
KSO_15/XDB1/GPIO224 (B17)
KSO_16/XDB2/GPIO225 (A24)
KSO_17/XDB3/GPIO226 (D17)

USBCLK/14M_25M_48M_OSC (G8)
USB_RCOMP ← USB_RCOMP_SB via R310 11.8K/F_6 (B9)
USB_FSD1P/GPIO186 (H1)
USB_FSD1N (H3)
USB_FSD0P/GPIO185 (H6)
USB_FSD0N (H5)

Note: USB P/N pairs with trace lengths up to 10"

USB_HSD13P (H10) → USBP13P [25]
USB_HSD13N (G10) → USBP13N [25]
USB 3.0/2.0 Combo

USB_HSD12P (K10) → USBP12P [25]
USB_HSD12N (J12) → USBP12N [25]
USB 3.0/2.0 Combo

USB_HSD11P (G12) → USBP11P [38]
USB_HSD11N (F12) → USBP11N [38]
USB 3.0/2.0 Combo

USB_HSD10P (K12) → USBP10P [29]
USB_HSD10N (K13) → USBP10N [29]
USB 3.0/2.0 Combo

USB_HSD9P (B11) → USBP9P [22]
USB_HSD9N (D11) → USBP9N [22]
Camera

USB_HSD8P (E10)
USB_HSD8N (F10)

USB_HSD7P (C10) → USBP7P [26]
USB_HSD7N (A10) → USBP7N [26]
Card Reader

USB_HSD6P (H9)
USB_HSD6N (G9)

USB_HSD5P (A8)
USB_HSD5N (C8)

USB_HSD4P (F8)
USB_HSD4N (E8)

USB_HSD3P (C6)
USB_HSD3N (A6)

USB_HSD2P (C5)
USB_HSD2N (A5)

USB_HSD1P (C1) → USBP1P [29]
USB_HSD1N (C3) → USBP1N [29]
WLAN

USB_HSD0P (E1) → USBP0P [25]
USB_HSD0N (E3) → USBP0N [25]
Debug

USBSS_CALRP (C16) via R329 1K/F_4
USBSS_CALRN (A16) via R327 1K/F_4 → +1.1V_SUS

USB_SS_TX3P (A14) → USB3_TXP3 [25]
USB_SS_TX3N (C14) → USB3_TXN3 [25]
USB_SS_RX3P (C12) → USB3_RXP3 [25]
USB_SS_RX3N (A12) → USB3_RXN3 [25]
USB 3.0/2.0 Combo (MB)

USB_SS_TX2P (D15) → USB3_TXP2 [25]
USB_SS_TX2N (B15) → USB3_TXN2 [25]
USB_SS_RX2P (E14) → USB3_RXP2 [25]
USB_SS_RX2N (F14) → USB3_RXN2 [25]
USB 3.0/2.0 Combo (MB)

USB_SS_TX1P (F15) → USB3_TXP1 [38]
USB_SS_TX1N (G15) → USB3_TXN1 [38]
USB_SS_RX1P (H13) → USB3_RXP1 [38]
USB_SS_RX1N (G13) → USB3_RXN1 [38]
USB 3.0/2.0 Combo (MB)

USB_SS_TX0P (J16) → USB3_TXP0 [29]
USB_SS_TX0N (H16) → USB3_TXN0 [29]
USB_SS_RX0P (J15) → USB3_RXP0 [29]
USB_SS_RX0N (K15) → USB3_RXN0 [29]
USB 3.0/2.0 Combo (IO)

USB REDRIVER RESERVE , CAP close Connector , C79~C82 stuff 0 ohm

SCL2/GPIO193 (H19) → SMB_RUN_CLK2
SDA2/GPIO194 (G19) → SMB_RUN_DAT2
SCL3_LV/GPIO195 (G22) → SMB_LV_CLK
SDA3_LV/GPIO196 (G21) → SMB_LV_DAT

EC_PWM0/EC_TIMER0/GPIO197 (E22)
EC_PWM1/EC_TIMER1/GPIO198 (H22)
EC_PWM2/EC_TIMER2/WOL_EN/GPIO199 (J22) → EC_PWM2 [12]
EC_PWM3/EC_TIMER3/GPIO200 (H21)

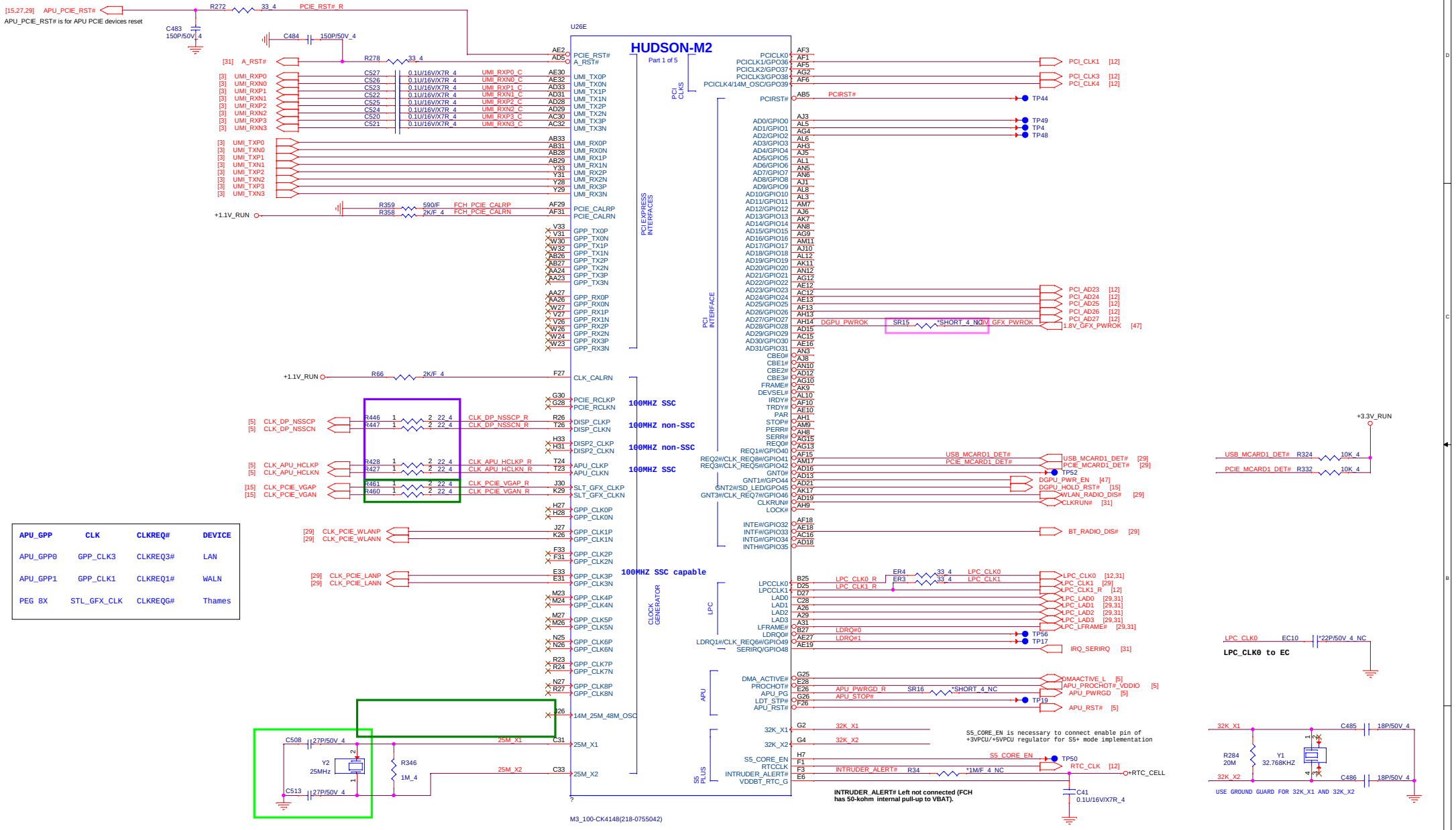
KSI_0/GPIO201 (K21)
KSI_1/GPIO202 (K22)
KSI_2/GPIO203 (F22)
KSI_3/GPIO204 (F24)
KSI_4/GPIO205 (E24)
KSI_5/GPIO206 (B23)
KSI_6/GPIO207 (C24)
KSI_7/GPIO208 (F18)

HUNSON M3
M3_100-CK4148(218-0755042)

Quanta Computer Inc.
PROJECT : R0AA

Size	Document Number	Rev
	Hudson-M3 GPIO/USB/AZ/RGMII	B

Date: Monday, June 25, 2012 Sheet 8 of 55

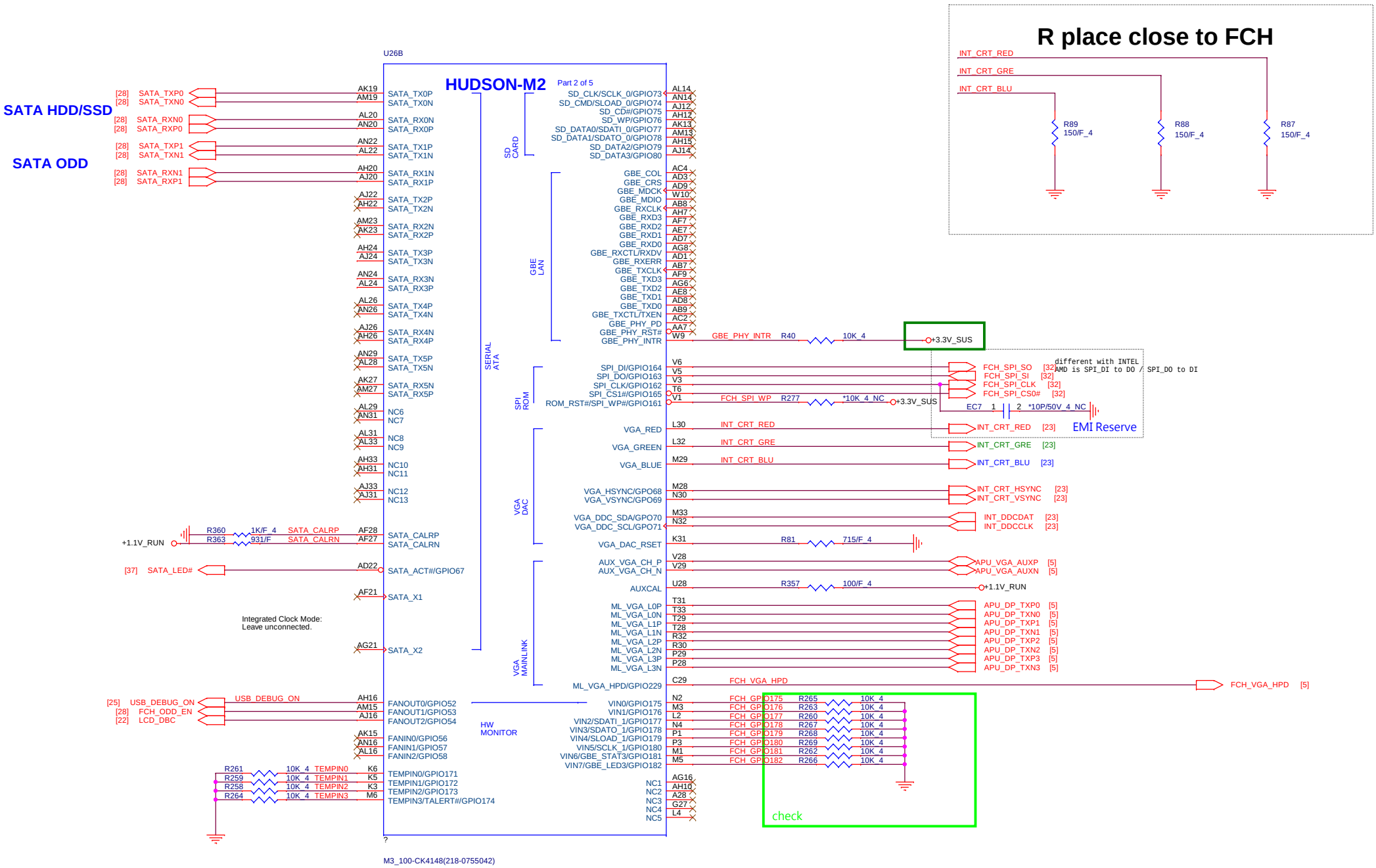


APU_GPP	CLK	CLKREQ#	DEVICE
APU_GPP0	GPP_CLK3	CLKREQ3#	LAN
APU_GPP1	GPP_CLK1	CLKREQ1#	WALN
PEG 8X	STL_GFX_CLK	CLKREQG#	Thames

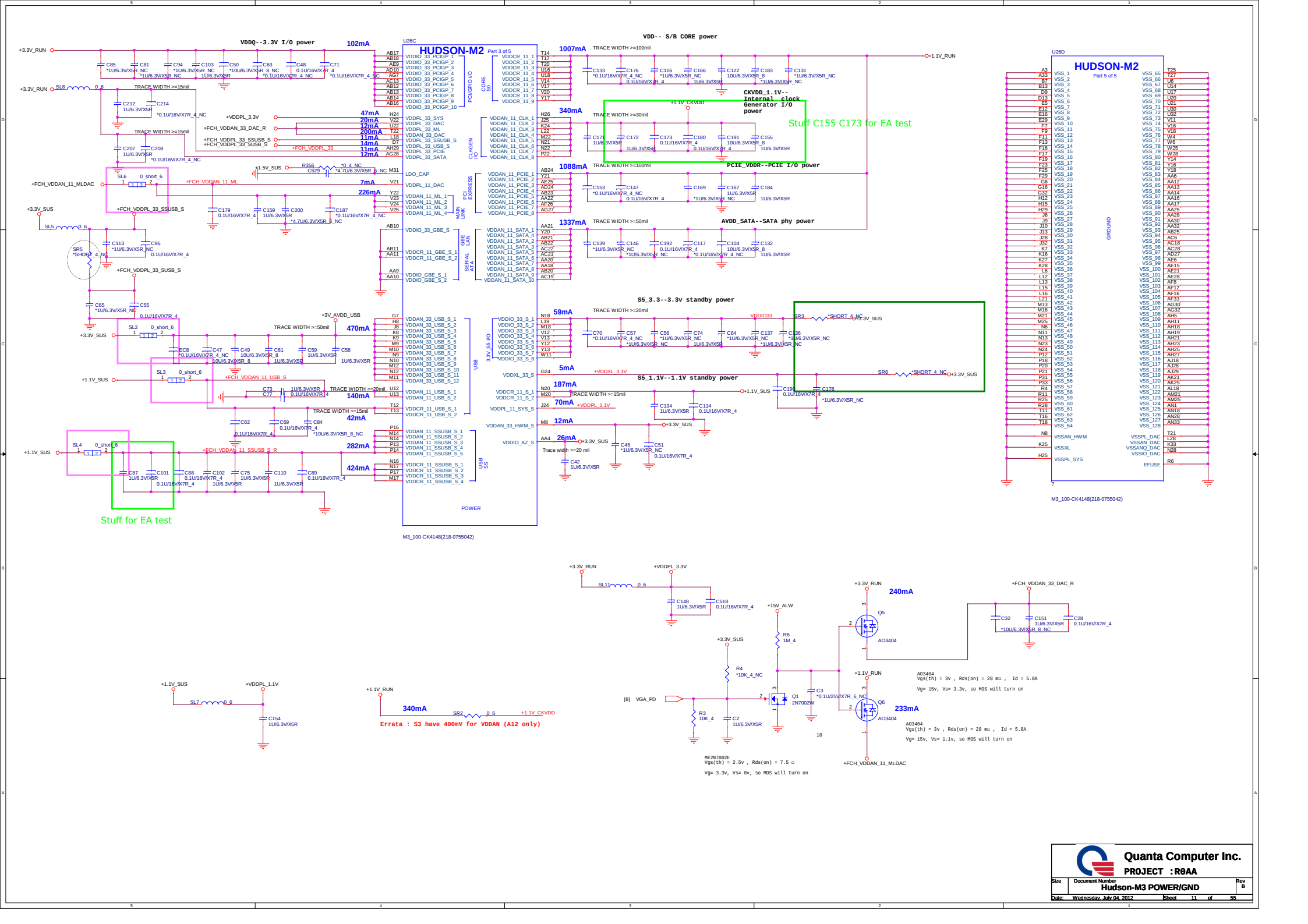
Quanta Computer Inc.
PROJECT : R0AA

Size	Document Number	Rev
	Hudson-M3 ACPI/PCI/CLOCK	B

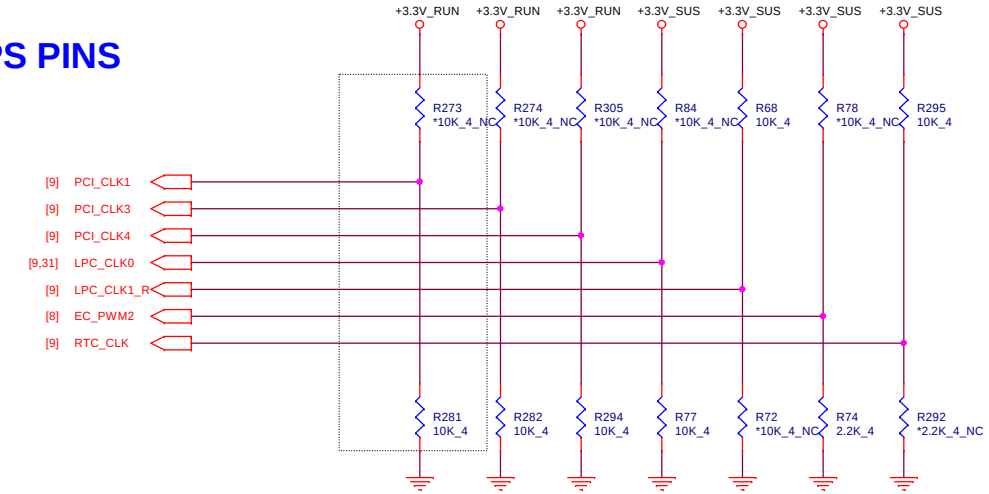
Date: Monday, June 25, 2012 Sheet 9 of 55



Quanta Computer Inc.		
PROJECT : R0AA		
Size	Document Number: Hudson-M3 SATA/HWM/SPI	Rev: B
Date: Monday, June 25, 2012	Sheet 10 of 55	


VDDQ--3.3V I/O power
102mA
HUDSON-M2
Part 3 of 5
U26C
VDD-- S/B CORE power
1007mA
CKVDD_1.1V--Internal clock Generator I/O power
340mA
Stuff C155 C173 for EA test
PCIE_VDDR--PCIE I/O power
1088mA
AVDD_SATA--SATA phy power
1337mA
S5_3.3--3.3v standby power
59mA
S5_1.1V--1.1V standby power
187mA
5mA
70mA
12mA
26mA
47mA
20mA
12mA
200mA
11mA
14mA
11mA
12mA
7mA
226mA
470mA
140mA
42mA
282mA
424mA
Stuff for EA test
POWER
M3_100-CK4148(218-0755042)
HUDSON-M2
Part 5 of 5
U26D
GROUND
M3_100-CK4148(218-0755042)
240mA
233mA
Errata : S3 have 400mV for VDDAN (A12 only)
340mA
Quanta Computer Inc.
PROJECT : R0AA
Hudson-M3 POWER/GND
Rev B
Date: Wednesday, July 04, 2012
Sheet 11 of 55

STRAPS PINS

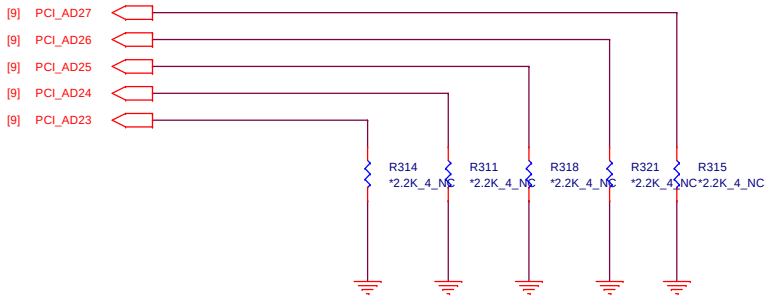


REQUIRED STRAPS

	--------	PCI_CLK1	--------	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	--------	ALLOW PCIE Gen2	--------	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED Setting	LPC ROM	S5 PLUS MODE DISABLED Setting
PULL LOW	--------	FORCE PCIE Gen1 Setting	--------	IGNORE DEBUG STRAP Setting	FUSION CLOCK MODE Setting	EC DISABLED Setting	CLKGEN DISABLED	SPI ROM Setting	S5 PLUS MODE ENABLED

DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

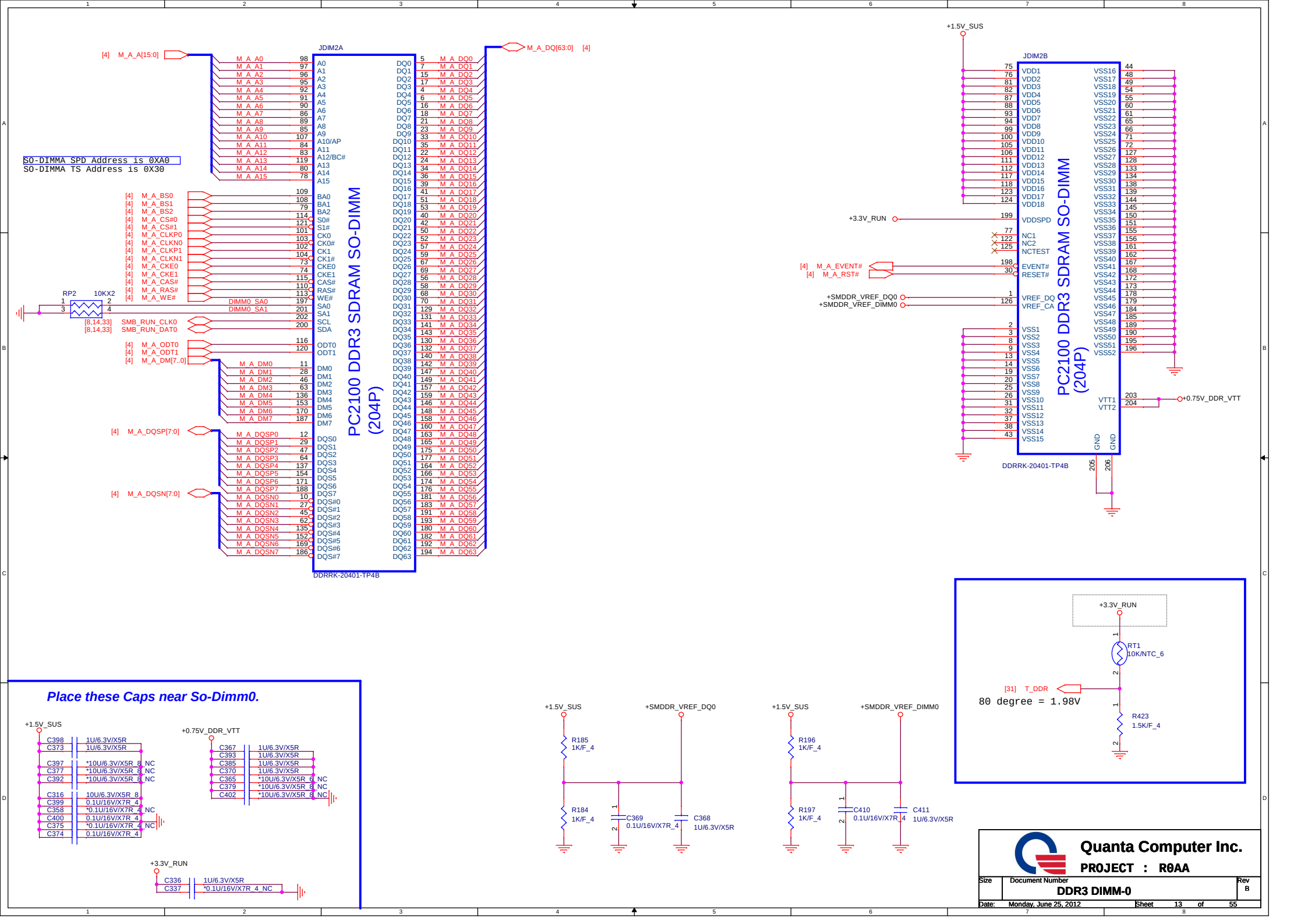


	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL Setting	DISABLE ILA AUTORUN Setting	USE FC PLL Setting	USE DEFAULT PCIE STRAPS Setting	DISABLE PCI MEM BOOT Setting
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Quanta Computer Inc.
PROJECT : R0AA

Size	Document Number	Rev
	Hudson-M3 STRAP/PWRGD	B

Date: Monday, June 25, 2012 Sheet 12 of 55


JDIM2A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDRRK-20401-TP4B
SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30
RP2 10KX2
JDIM2B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDRRK-20401-TP4B
Place these Caps near So-Dimm0.
+1.5V_SUS
+0.75V_DDR_VTT
+3.3V_RUN
+SMDDR_VREF_DQ0
+SMDDR_VREF_DIMM0
80 degree = 1.98V
Quanta Computer Inc.
PROJECT : R0AA
DDR3 DIMM-0
Monday, June 25, 2012
Sheet 13 of 55

SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34

JDIM1A

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP8D

RP1 10KX2

JDIM1B

PC2100 DDR3 SDRAM SO-DIMM (204P)

DDRRK-20401-TP8D

Place these Caps near So-Dimm1.

CH6101M9905
CAP CHIP 10U 6.3V(+-20%,X5R,0603)

C332	*10U/6.3V/X5R_8_NC	
C359	0.1U/16V/X7R_4	
C331	*10U/6.3V/X5R_8_NC	
C361	10U/6.3V/X5R_8	
C395	10U/6.3V/X5R_8	
C357	10U/6.3V/X5R_8	
C360	*0.1U/16V/X7R_4_NC	
C333	0.1U/16V/X7R_4	
C362	0.1U/16V/X7R_4	
C327	0.1U/16V/X7R_4	
C326	0.1U/16V/X7R_4	

C405	*1U/6.3V/X5R_NC	
C394	1U/6.3V/X5R	
C350	1U/6.3V/X5R	
C348	1U/6.3V/X5R	
C407	*10U/6.3V/X5R_8_NC	
C419	*10U/6.3V/X5R_8_NC	
C356	*10U/6.3V/X5R_8_NC	

C378	1U/6.3V/X5R	
C344	*0.1U/16V/X7R_4_NC	

R165 1K/F_4
R164 1K/F_4
C339 0.1U/16V/X7R_4
C340 1U/6.3V/X5R

R186 1K/F_4
R187 1K/F_4
C364 0.1U/16V/X7R_4
C363 1U/6.3V/X5R

Quanta Computer Inc.
PROJECT : R0AA

Size	Document Number	Rev
	DDR3 DIMM-1	B

Date: Monday, June 25, 2012 Sheet 14 of 55

Thames/Whistler/Seymour PCIE-Gen2

0.1uF AC coupling Caps for PCIE GEN1/2

U27A

PART 1 0F 9

PCI EXPRESS INTERFACE

[3] PEG_TXP0	PEG_TXP0	AA38	PCIE_RX0P	PCIE_TX0P	Y33	PEG_RXP0_C	C243	2 1	0.1U/16V/X7R_4	PEG_RXP0	PEG_RXP0 [3]
[3] PEG_TXN0	PEG_TXN0	Y37	PCIE_RX0N	PCIE_TX0N	Y32	PEG_RXN0_C	C227	2 1	0.1U/16V/X7R_4	PEG_RXN0	PEG_RXN0 [3]
[3] PEG_TXP1	PEG_TXP1	Y35	PCIE_RX1P	PCIE_TX1P	W33	PEG_RXP1_C	C242	2 1	0.1U/16V/X7R_4	PEG_RXP1	PEG_RXP1 [3]
[3] PEG_TXN1	PEG_TXN1	W36	PCIE_RX1N	PCIE_TX1N	W32	PEG_RXN1_C	C226	2 1	0.1U/16V/X7R_4	PEG_RXN1	PEG_RXN1 [3]
[3] PEG_TXP2	PEG_TXP2	W38	PCIE_RX2P	PCIE_TX2P	U33	PEG_RXP2_C	C238	2 1	0.1U/16V/X7R_4	PEG_RXP2	PEG_RXP2 [3]
[3] PEG_TXN2	PEG_TXN2	V37	PCIE_RX2N	PCIE_TX2N	U32	PEG_RXN2_C	C239	2 1	0.1U/16V/X7R_4	PEG_RXN2	PEG_RXN2 [3]
[3] PEG_TXP3	PEG_TXP3	V35	PCIE_RX3P	PCIE_TX3P	U30	PEG_RXP3_C	C236	2 1	0.1U/16V/X7R_4	PEG_RXP3	PEG_RXP3 [3]
[3] PEG_TXN3	PEG_TXN3	U36	PCIE_RX3N	PCIE_TX3N	U29	PEG_RXN3_C	C237	2 1	0.1U/16V/X7R_4	PEG_RXN3	PEG_RXN3 [3]
[3] PEG_TXP4	PEG_TXP4	U38	PCIE_RX4P	PCIE_TX4P	T33	PEG_RXP4_C	C232	2 1	0.1U/16V/X7R_4	PEG_RXP4	PEG_RXP4 [3]
[3] PEG_TXN4	PEG_TXN4	T37	PCIE_RX4N	PCIE_TX4N	T32	PEG_RXN4_C	C233	2 1	0.1U/16V/X7R_4	PEG_RXN4	PEG_RXN4 [3]
[3] PEG_TXP5	PEG_TXP5	T35	PCIE_RX5P	PCIE_TX5P	T30	PEG_RXP5_C	C234	2 1	0.1U/16V/X7R_4	PEG_RXP5	PEG_RXP5 [3]
[3] PEG_TXN5	PEG_TXN5	R36	PCIE_RX5N	PCIE_TX5N	T29	PEG_RXN5_C	C235	2 1	0.1U/16V/X7R_4	PEG_RXN5	PEG_RXN5 [3]
[3] PEG_TXP6	PEG_TXP6	R38	PCIE_RX6P	PCIE_TX6P	P33	PEG_RXP6_C	C230	2 1	0.1U/16V/X7R_4	PEG_RXP6	PEG_RXP6 [3]
[3] PEG_TXN6	PEG_TXN6	P37	PCIE_RX6N	PCIE_TX6N	P32	PEG_RXN6_C	C231	2 1	0.1U/16V/X7R_4	PEG_RXN6	PEG_RXN6 [3]
[3] PEG_TXP7	PEG_TXP7	P35	PCIE_RX7P	PCIE_TX7P	P30	PEG_RXP7_C	C228	2 1	0.1U/16V/X7R_4	PEG_RXP7	PEG_RXP7 [3]
[3] PEG_TXN7	PEG_TXN7	N36	PCIE_RX7N	PCIE_TX7N	P29	PEG_RXN7_C	C229	2 1	0.1U/16V/X7R_4	PEG_RXN7	PEG_RXN7 [3]
		N38	PCIE_RX8P	PCIE_TX8P	N33						
		M37	PCIE_RX8N	PCIE_TX8N	N32						
		M35	PCIE_RX9P	PCIE_TX9P	N30						
		L36	PCIE_RX9N	PCIE_TX9N	N29						
		L38	PCIE_RX10P	PCIE_TX10P	L33						
		K37	PCIE_RX10N	PCIE_TX10N	L32						
		K35	PCIE_RX11P	PCIE_TX11P	L30						
		J36	PCIE_RX11N	PCIE_TX11N	L29						
		J38	PCIE_RX12P	PCIE_TX12P	K33						
		H37	PCIE_RX12N	PCIE_TX12N	K32						
		H35	PCIE_RX13P	PCIE_TX13P	J33						
		G36	PCIE_RX13N	PCIE_TX13N	J32						
		G38	PCIE_RX14P	PCIE_TX14P	K30						
		F37	PCIE_RX14N	PCIE_TX14N	K29						
		F35	PCIE_RX15P	PCIE_TX15P	H33						
		E37	PCIE_RX15N	PCIE_TX15N	H32						

CLOCK

[9] CLK_PCIE_VGAP — CLK_PCIE_VGAP — AB35 — PCIE_REFCLKP

[9] CLK_PCIE_VGAN — CLK_PCIE_VGAN — AA36 — PCIE_REFCLKN

2 R323 1 1K_4 — AH16 — TEST_PG

GPU_RST# — AA30 — PERSTB

CALIBRATION

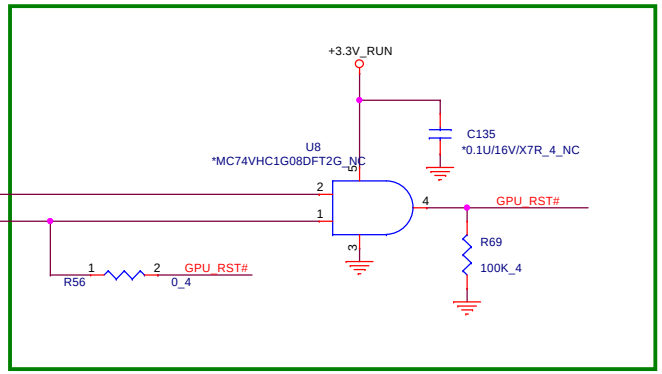
PCIE_CALR_TX — Y30 — PCIE_CALRP — 2 R91 1 1.27K/F_4

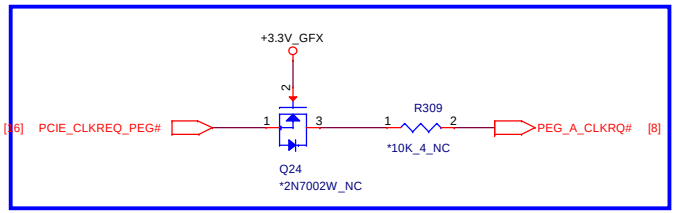
PCIE_CALR_RX — Y29 — PCIE_CALRN — 2 R70 1 2K/F_4 — +1.0V_GFX

HEATHROW M2

Support Themas & Seymour only

Part Description,
Part Number,
Footprint need update





Quanta Computer Inc.

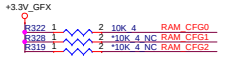
PROJECT : R0AA

Size	Document Number	Rev
	London_PCIE I/F	B
Date: Monday, June 25, 2012	Sheet 15 of 55	

CONFIGURATION STRAPS

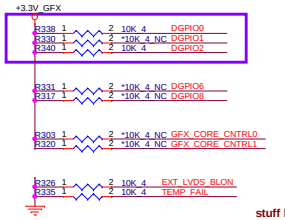
STRAPS	PIN	DESCRIPTION	SET
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0 = 50% Tx output swing 1 = Full Tx output swing	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = Disable ; 1 = Enable	0
BIF_GEN3_EN_A	GPIO2	PCIE Gen2 Enable 0 = GEN2 not supported at power-on 1= GEN2 supported at power-on	1
BIF_VGA DIS	GPIO9	0: VGA Controller capacity enabled 1: VGA Controller capacity disabled (for multi-GPU)	0
ROMIDCFG[2:0]	GPIO[13:11]	Serial ROM type or Memory Aperture Size Select If GPIO22 = 0, defines memory aperture size If GPIO22 = 1, defines ROM type 100 - 512Kbit M25P05A (ST) 101 - 1Mbit M25P10A (ST) 101 - 2Mbit M25P20 (ST) 101 - 4Mbit M25P40 (ST) 101 - 8Mbit M25P80 (ST) 100 - 512Kbit Pm25LV512 (Chingis) 101 - 1Mbit Pm25LV010 (Chingis)	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0 = Disable ; 1 = Enable	0
AUD[1] AUD[0]	VGAHSYNC VGAVSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI.	00
CEC_DIS	GENLK_VSYNC	Enable CEC function. Reserved for Thames/Whistler/Seymour 0 = Disable ; 1 = Enable	0
RESERVED RESERVED RESERVED RESERVED	GENLK_CLK GPIO8 GPIO21 GENERICC	Allow for Pull-up PADS for the reserved straps but do not install resistor If these GPIOS are used, they must keep low and not conflict during reset RESERVED RESERVED RESERVED Reserved (for Thames/Whistler/Seymour only)	

APERTURE SIZE



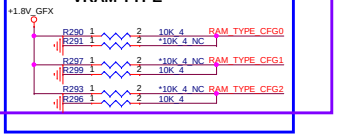
MEMORY APERTURE SIZE SELECT

MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0

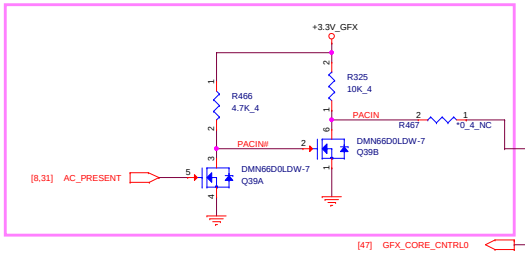


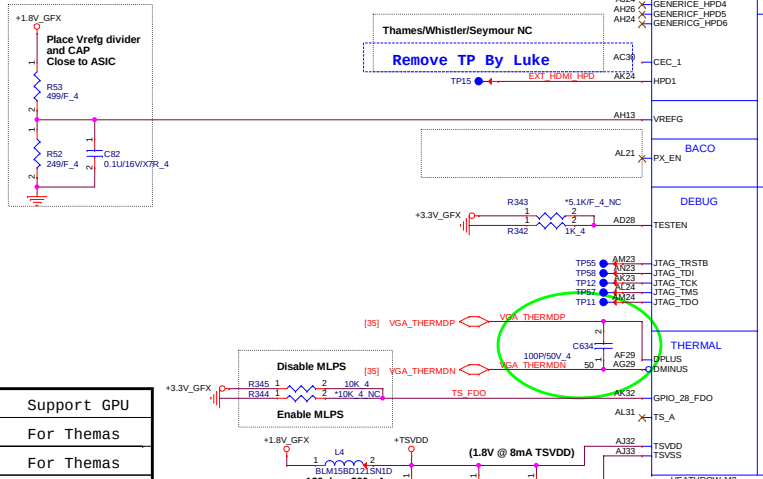
stuff by BOM

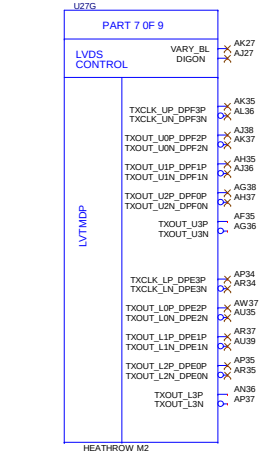
VRAM TYPE

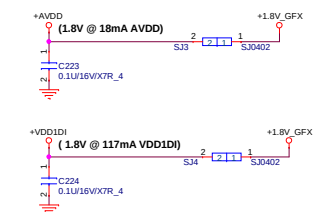


Memory Straps	RAM_TYPE _CFG2	RAM_TYPE _CFG1	RAM_TYPE _CFG0	Quanta PN (QuantaBuy)	Vendor PN	Support GPU
900MHz Samsung 1GB(64M*16*8pcs)	0	0	1	AKD5EGGT509	K4W1G1646G-BC11	For Themas
900MHz Hynix 1GB(64M*16*8pcs)	0	1	0	AKD5LZWTW07	H5TQ1G63DFR-11C	For Themas
900MHz Micron 1GB(64M*16*8pcs)	1	0	0	AKD5EGSTL01	MT41J64M16JT	For Themas



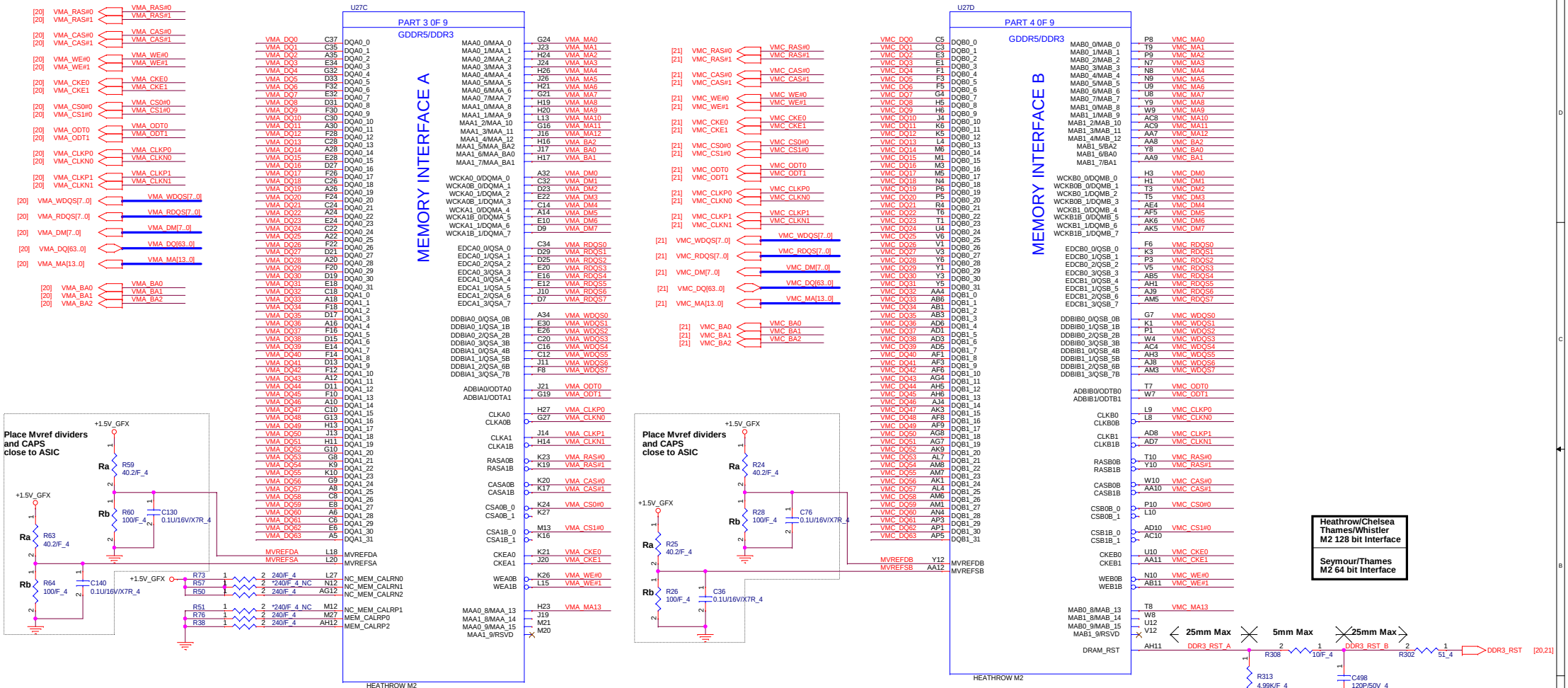






Reserve 0 ohm for Dual mode DDC/AUX

Quanta Computer Inc.	PROJECT : R0AA
Size	Document Number: London_IO & STRAP
Rev	B
Date: Tuesday, July 03, 2012	Sheet 16 of 55



	L27	N12	AG12	M12	M27	AH12
	R73	R57	R50	R51	R76	R38
Heathrow/Chelsea	NC	NC	NC	NC	Stuff 120	Stuff 120
Thames/Whistler	Stuff 240	NC	Stuff 240	NC	Stuff 240	Stuff 240
Seymour	NC	Stuff 240	NC	Stuff 240	NC	NC

GPU (Pkg)	Preliminary Branding*	Memory Size	Mem Width	Memory Type	Mem Devices	Pro Perf (TDP)*	XT Perf (TDP)*
Chelsea (M2)	HD 7700	2 GB	128bit	128M x16 DDR3	8 pcs	P5500 (25W)	P5800 (35W)
	HD 7700	1 GB	128bit	64M x16 DDR3	8 pcs	P5500 (25W)	P5800 (35W)
Thames (M2)	HD 7600	2GB	128bit	128M x16 DDR3	8 pcs	P4600 (18W)	P5200 (22W)
	HD 7600	1GB	128-bit	64M x16 DDR3	8 pcs	P4600 (18W)	P5200 (22W)
	HD 7500	1GB	64-bit	128M x16 DDR3	4 pcs	P3000 (15W)	P3200 (18W)

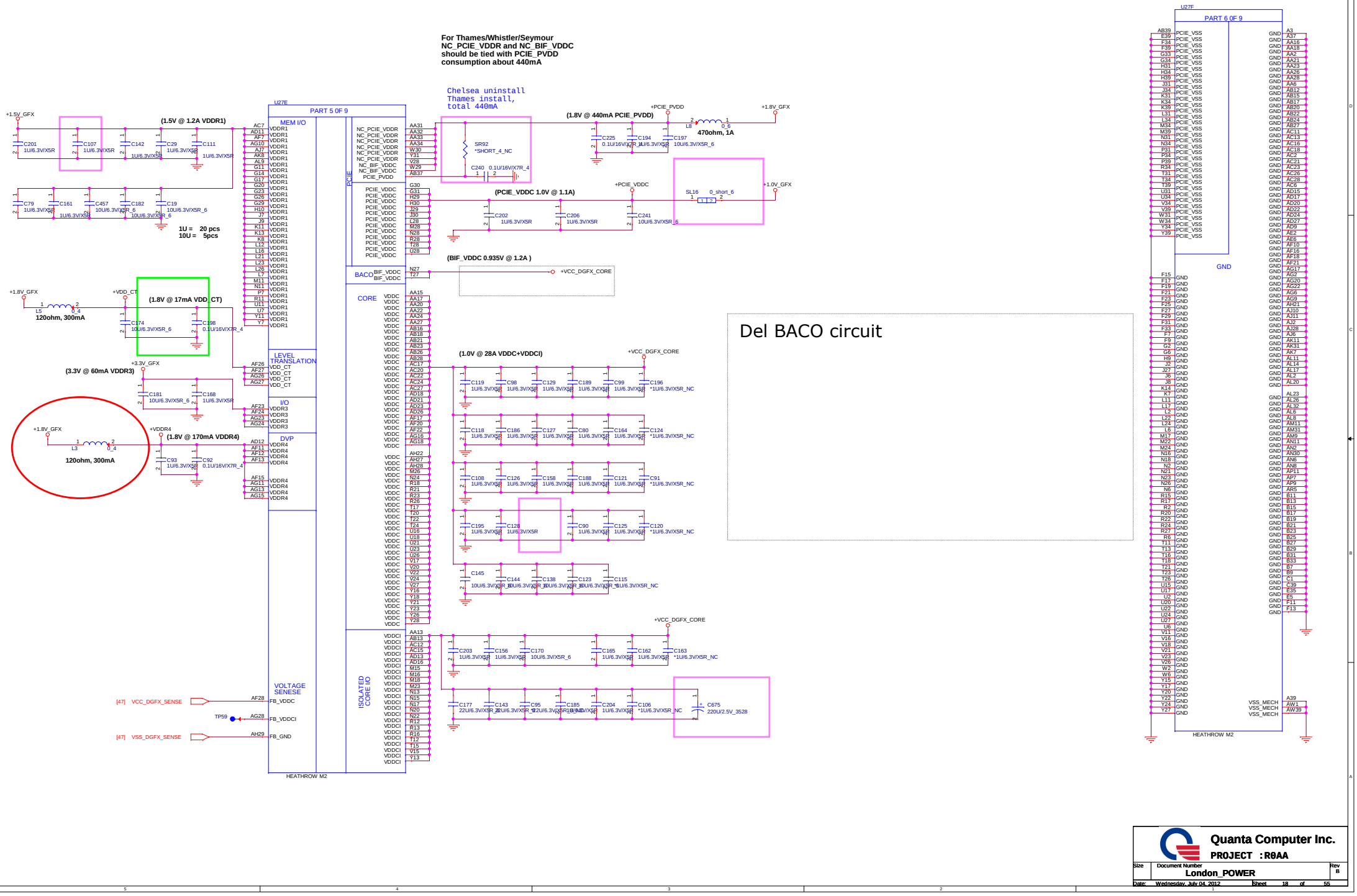
GPU (Pkg)	Series Branding*	Mem Size	Mem width	Mem TYpe	Mem Devices	Pro Perf (TDP)*	XT Perf (TDP)*
Thames (M2)	HD 7600	1 GB	64-bit	128Mx16 GDDR5	(4pcs)	P3800 (18W)	-
Chelsea (M2)	HD 7700	2 GB	128-bit	128Mx16 GDDR5	(8 pcs)	P6600 (25W)	P7500 (35W)
	HD 7700	1 GB	128-bit	64Mx16 GDDR5	(8 pcs)	P6600(25W)	P7500 (35W)
Heathrow (M2)	HD 7800	2 GB	128-bit	128Mx16 GDDR5	(8 pcs)	P8000 (35W)	P9500 (45W)
	HD 7800	1 GB	128-bit	64Mx16 GDDR5	(8 pcs)	P8000 (35W)	P9500 (45W)

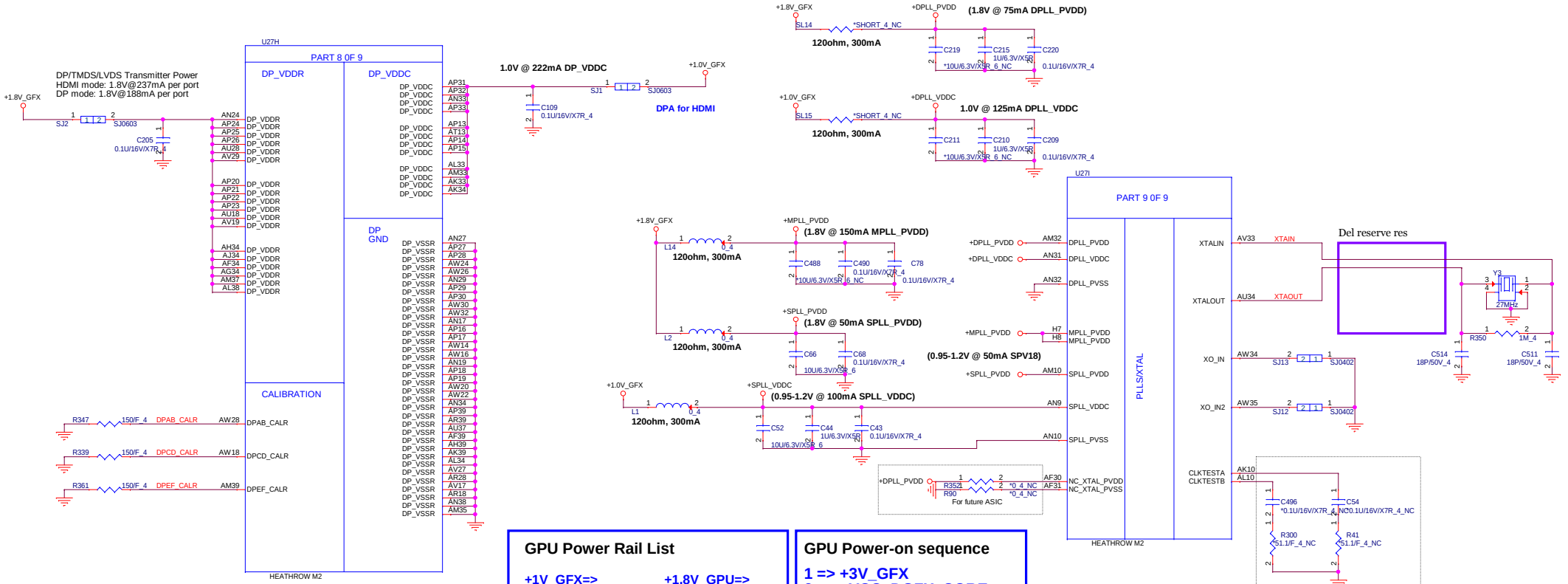
GPU	Series Branding*	Mem Size	Mem width	Mem TYpe	Mem Devices	Pro Perf (TDP)*	XT Perf (TDP)*
Seymour XTX (M2)	HD 7400	512 MB	64-bit	64Mx32 GDDR5	(2pcs)		P2700 (20W)
Thames (M2)	HD7600	1 GB	128-bit	64Mx32 GDDR5	(4pcs)	P5200 (22W)	-
	HD 7600	512 MB	64-bit	64Mx32 GDDR5	(2pcs)	P3800 (18W)	P4200 (25W)
Chelsea (M2)	HD 7700	1GB	128-bit	64Mx32 GDDR5	(4pcs)	P6600 (25W)	P7500 (35W)
	HD 7700	512 MB	128-bit	32Mx32 GDDR5	(4pcs)	P6600 (25W)	P7500 (35W)
Heathrow (M2)	HD 7800	1GB	128-bit	64Mx32 GDDR5	(4pcs)	P8000 (35W)	P9500 (45W)

Quanta Computer Inc.
PROJECT : R0AA

Size	Document Number	Rev
	London_MEMORY	B

Date: Monday, June 25, 2012 Sheet 17 of 55


For Thames/Whistler/Seymour
NC_PCIE_VDDR and NC_BIF_VDDC
should be tied with PCIE_PVDD
consumption about 440mA
Chelsea uninstall
Thames install,
total 440mA
U27E
PART 5 0F 9
MEM I/O
PCIE
BACO
CORE
LEVEL TRANSLATION
I/O
DVP
VOLTAGE SENESE
ISOLATED CORE I/O
HEATHROW M2
(1.5V @ 1.2A VDDR1)
(1.8V @ 17mA VDD_CT)
(3.3V @ 60mA VDDR3)
(1.8V @ 170mA VDDR4)
120ohm, 300mA
1U = 20 pcs
10U = 5pcs
(1.8V @ 440mA PCIE_PVDD)
470ohm, 1A
(PCIE_VDDC 1.0V @ 1.1A)
(BIF_VDDC 0.935V @ 1.2A)
(1.0V @ 28A VDDC+VDDCI)
Del BACO circuit
U27F
PART 6 0F 9
GND
HEATHROW M2
Quanta Computer Inc.
PROJECT : R0AA
Size
Document Number
London_POWER
Rev
B
Date: Wednesday, July 04, 2012
Sheet 18 of 55



GPU Power Rail List

+1V_GFX=>
- +DP_VDDC
- +PCIE_VDDC
- +DPLL_VDDC
- +SPLL_VDDC

+1.8V_GPU=>
- +DP_VDDR
- +PCIE_PVDD
- +AVDD
- +DPLL_PVDD
- +TSVDD
- +VDD1DI
- +VDD_CT
- +VDDR4

GPU Power-on sequence

1 => +3V_GFX
2 => +VCC_DGFX_CORE
3 => +1V_GFX
4 => +1.5V_GFX
5 => +1.8V_GFX
6 => dGPU_PWROK

For Thames/Whistler/Seymour
+PCIE_VDDC= 1V@1.1A

For Heathrow/Chelsea
+PCIE_VDDC= 0.935V@1.88A (PCIE Gen2)
+PCIE_VDDC= 0.935V@2.5A (PCIE Gen3)

Quanta Computer Inc.
PROJECT : R0AA

Size	Document Number	Rev
	London_DP POWER	B

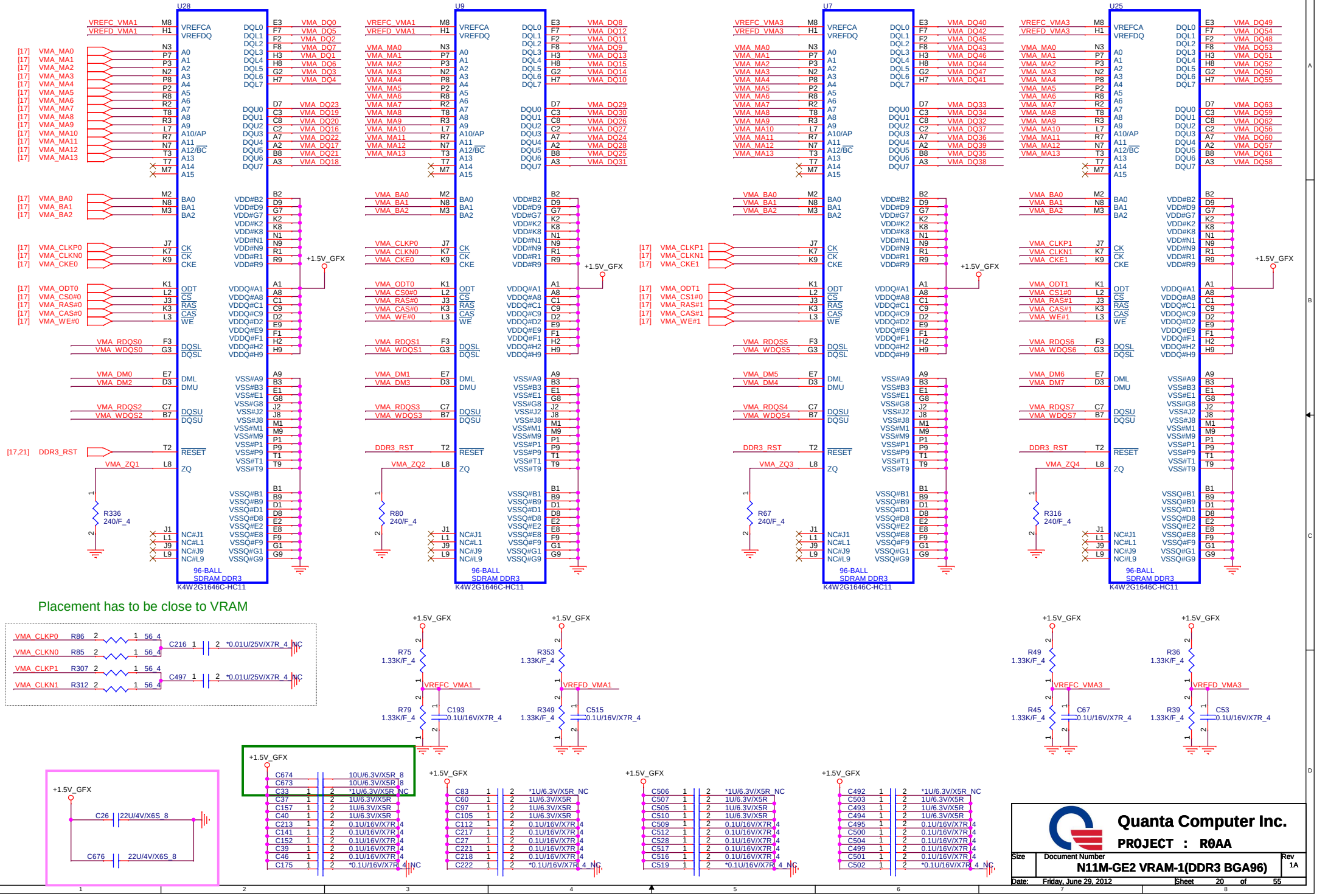
Date: Thursday, June 28, 2012 Sheet 19 of 55

CHANNEL A: 1024MB DDR3

[17] VMA_MA[13..0]
[17] VMA_DQ[63..0]
[17] VMA_DM[7..0]
[17] VMA_WDQS[7..0]
[17] VMA_RDQS[7..0]

U28 / U9 / U7 / U25 — 96-BALL SDRAM DDR3 — K4W2G1646C-HC11

Placement has to be close to VRAM



Quanta Computer Inc.		
PROJECT : R0AA		
Size	Document Number: N11M-GE2 VRAM-1(DDR3 BGA96)	Rev: 1A
Date: Friday, June 29, 2012	Sheet 20 of 55	

CHANNEL B: 1024MB DDR3

[17] VMC_MA[13..0]
[17] VMC_DQ[63..0]
[17] VMC_DM[7..0]
[17] VMC_WDQS[7..0]
[17] VMC_RDQS[7..0]

U4 — K4W2G1646C-HC11 (96-BALL SDRAM DDR3)

VREFC_VMC1 M8 VREFCA
VREFD_VMC1 H1 VREFDQ

[17] VMC_MA0 N3 A0
[17] VMC_MA1 P7 A1
[17] VMC_MA2 P3 A2
[17] VMC_MA3 N2 A3
[17] VMC_MA4 P8 A4
[17] VMC_MA5 P2 A5
[17] VMC_MA6 R8 A6
[17] VMC_MA7 R2 A7
[17] VMC_MA8 T8 A8
[17] VMC_MA9 R3 A9
[17] VMC_MA10 L7 A10/AP
[17] VMC_MA11 R7 A11
[17] VMC_MA12 N7 A12/BC
[17] VMC_MA13 T3 A13
T7 A14
M7 A15

[17] VMC_BA0 M2 BA0
[17] VMC_BA1 N8 BA1
[17] VMC_BA2 M3 BA2

[17] VMC_CLKP0 J7 CK
[17] VMC_CLKN0 K7 CK
[17] VMC_CKE0 K9 CKE

[17] VMC_ODT0 K1 ODT
[17] VMC_CS0#0 L2 CS
[17] VMC_RAS#0 J3 RAS
[17] VMC_CAS#0 K3 CAS
[17] VMC_WE#0 L3 WE

VMC_RDQS0 F3 DQSL
VMC_WDQS0 G3 DQSL

VMC_DM0 E7 DML
VMC_DM3 D3 DMU

VMC_RDQS3 C7 DQSU
VMC_WDQS3 B7 DQSU

[17,20] DDR3_RST T2 RESET
VMC_ZQ1 L8 ZQ

R7 240/F_4

NC#J1 J1
NC#L1 L1
NC#J9 J9
NC#L9 L9

DQL0 E3 VMC_DQ4
DQL1 F7 VMC_DQ3
DQL2 F2 VMC_DQ7
DQL3 F8 VMC_DQ0
DQL4 H3 VMC_DQ6
DQL5 H8 VMC_DQ1
DQL6 G2 VMC_DQ5
DQL7 H7 VMC_DQ2

DQU0 D7 VMC_DQ26
DQU1 C3 VMC_DQ29
DQU2 C8 VMC_DQ28
DQU3 C2 VMC_DQ30
DQU4 A7 VMC_DQ24
DQU5 A2 VMC_DQ31
DQU6 B8 VMC_DQ25
DQU7 A3 VMC_DQ27

VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9
+1.5V_GFX

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

U22 — K4W2G1646C-HC11 (96-BALL SDRAM DDR3)

VREFC_VMC1 M8 VREFCA
VREFD_VMC1 H1 VREFDQ

VMC_MA0 N3 A0
VMC_MA1 P7 A1
VMC_MA2 P3 A2
VMC_MA3 N2 A3
VMC_MA4 P8 A4
VMC_MA5 P2 A5
VMC_MA6 R8 A6
VMC_MA7 R2 A7
VMC_MA8 T8 A8
VMC_MA9 R3 A9
VMC_MA10 L7 A10/AP
VMC_MA11 R7 A11
VMC_MA12 N7 A12/BC
VMC_MA13 T3 A13
T7 A14
M7 A15

VMC_BA0 M2 BA0
VMC_BA1 N8 BA1
VMC_BA2 M3 BA2

VMC_CLKP0 J7 CK
VMC_CLKN0 K7 CK
VMC_CKE0 K9 CKE

VMC_ODT0 K1 ODT
VMC_CS0#0 L2 CS
VMC_RAS#0 J3 RAS
VMC_CAS#0 K3 CAS
VMC_WE#0 L3 WE

VMC_RDQS2 F3 DQSL
VMC_WDQS2 G3 DQSL

VMC_DM2 E7 DML
VMC_DM1 D3 DMU

VMC_RDQS1 C7 DQSU
VMC_WDQS1 B7 DQSU

DDR3_RST T2 RESET
VMC_ZQ2 L8 ZQ

R251 240/F_4

NC#J1 J1
NC#L1 L1
NC#J9 J9
NC#L9 L9

DQL0 E3 VMC_DQ19
DQL1 F7 VMC_DQ21
DQL2 F2 VMC_DQ16
DQL3 F8 VMC_DQ18
DQL4 H3 VMC_DQ20
DQL5 H8 VMC_DQ22
DQL6 G2 VMC_DQ17
DQL7 H7 VMC_DQ23

DQU0 D7 VMC_DQ15
DQU1 C3 VMC_DQ11
DQU2 C8 VMC_DQ14
DQU3 C2 VMC_DQ10
DQU4 A7 VMC_DQ12
DQU5 A2 VMC_DQ9
DQU6 B8 VMC_DQ13
DQU7 A3 VMC_DQ8

VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9
+1.5V_GFX

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

U5 — K4W2G1646C-HC11 (96-BALL SDRAM DDR3)

VREFC_VMC3 M8 VREFCA
VREFD_VMC3 H1 VREFDQ

VMC_MA0 N3 A0
VMC_MA1 P7 A1
VMC_MA2 P3 A2
VMC_MA3 N2 A3
VMC_MA4 P8 A4
VMC_MA5 P2 A5
VMC_MA6 R8 A6
VMC_MA7 R2 A7
VMC_MA8 T8 A8
VMC_MA9 R3 A9
VMC_MA10 L7 A10/AP
VMC_MA11 R7 A11
VMC_MA12 N7 A12/BC
VMC_MA13 T3 A13
T7 A14
M7 A15

VMC_BA0 M2 BA0
VMC_BA1 N8 BA1
VMC_BA2 M3 BA2

[17] VMC_CLKP1 J7 CK
[17] VMC_CLKN1 K7 CK
[17] VMC_CKE1 K9 CKE

[17] VMC_ODT1 K1 ODT
[17] VMC_CS1#0 L2 CS
[17] VMC_RAS#1 J3 RAS
[17] VMC_CAS#1 K3 CAS
[17] VMC_WE#1 L3 WE

VMC_RDQS6 F3 DQSL
VMC_WDQS6 G3 DQSL

VMC_DM6 E7 DML
VMC_DM5 D3 DMU

VMC_RDQS5 C7 DQSU
VMC_WDQS5 B7 DQSU

DDR3_RST T2 RESET
VMC_ZQ3 L8 ZQ

R287 240/F_4

NC#J1 J1
NC#L1 L1
NC#J9 J9
NC#L9 L9

DQL0 E3 VMC_DQ52
DQL1 F7 VMC_DQ50
DQL2 F2 VMC_DQ55
DQL3 F8 VMC_DQ48
DQL4 H3 VMC_DQ53
DQL5 H8 VMC_DQ49
DQL6 G2 VMC_DQ54
DQL7 H7 VMC_DQ51

DQU0 D7 VMC_DQ41
DQU1 C3 VMC_DQ42
DQU2 C8 VMC_DQ40
DQU3 C2 VMC_DQ46
DQU4 A7 VMC_DQ47
DQU5 A2 VMC_DQ45
DQU6 B8 VMC_DQ43
DQU7 A3 VMC_DQ44

VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9
+1.5V_GFX

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

U23 — K4W2G1646C-HC11 (96-BALL SDRAM DDR3)

VREFC_VMC3 M8 VREFCA
VREFD_VMC3 H1 VREFDQ

VMC_MA0 N3 A0
VMC_MA1 P7 A1
VMC_MA2 P3 A2
VMC_MA3 N2 A3
VMC_MA4 P8 A4
VMC_MA5 P2 A5
VMC_MA6 R8 A6
VMC_MA7 R2 A7
VMC_MA8 T8 A8
VMC_MA9 R3 A9
VMC_MA10 L7 A10/AP
VMC_MA11 R7 A11
VMC_MA12 N7 A12/BC
VMC_MA13 T3 A13
T7 A14
M7 A15

VMC_BA0 M2 BA0
VMC_BA1 N8 BA1
VMC_BA2 M3 BA2

VMC_CLKP1 J7 CK
VMC_CLKN1 K7 CK
VMC_CKE1 K9 CKE

VMC_ODT1 K1 ODT
VMC_CS1#0 L2 CS
VMC_RAS#1 J3 RAS
VMC_CAS#1 K3 CAS
VMC_WE#1 L3 WE

VMC_RDQS4 F3 DQSL
VMC_WDQS4 G3 DQSL

VMC_DM4 E7 DML
VMC_DM7 D3 DMU

VMC_RDQS7 C7 DQSU
VMC_WDQS7 B7 DQSU

DDR3_RST T2 RESET
VMC_ZQ4 L8 ZQ

R248 240/F_4

NC#J1 J1
NC#L1 L1
NC#J9 J9
NC#L9 L9

DQL0 E3 VMC_DQ36
DQL1 F7 VMC_DQ39
DQL2 F2 VMC_DQ33
DQL3 F8 VMC_DQ35
DQL4 H3 VMC_DQ37
DQL5 H8 VMC_DQ32
DQL6 G2 VMC_DQ38
DQL7 H7 VMC_DQ34

DQU0 D7 VMC_DQ62
DQU1 C3 VMC_DQ59
DQU2 C8 VMC_DQ63
DQU3 C2 VMC_DQ56
DQU4 A7 VMC_DQ61
DQU5 A2 VMC_DQ57
DQU6 B8 VMC_DQ60
DQU7 A3 VMC_DQ58

VDD#B2 B2
VDD#D9 D9
VDD#G7 G7
VDD#K2 K2
VDD#K8 K8
VDD#N1 N1
VDD#N9 N9
VDD#R1 R1
VDD#R9 R9
+1.5V_GFX

VDDQ#A1 A1
VDDQ#A8 A8
VDDQ#C1 C1
VDDQ#C9 C9
VDDQ#D2 D2
VDDQ#E9 E9
VDDQ#F1 F1
VDDQ#H2 H2
VDDQ#H9 H9

VSS#A9 A9
VSS#B3 B3
VSS#E1 E1
VSS#G8 G8
VSS#J2 J2
VSS#J8 J8
VSS#M1 M1
VSS#M9 M9
VSS#P1 P1
VSS#P9 P9
VSS#T1 T1
VSS#T9 T9

VSSQ#B1 B1
VSSQ#B9 B9
VSSQ#D1 D1
VSSQ#D8 D8
VSSQ#E2 E2
VSSQ#E8 E8
VSSQ#F9 F9
VSSQ#G1 G1
VSSQ#G9 G9

Placement has to be close to VRAM

VMC_CLKP0 R8 2 — 1 56_4
VMC_CLKN0 R9 2 — 1 56_4
C10 1 — 2 *0.01U/25V/X7R_4_NC
VMC_CLKP1 R257 2 — 1 56_4
VMC_CLKN1 R256 2 — 1 56_4
C467 1 — 2 *0.01U/25V/X7R_4_NC

+1.5V_GFX
R10 1.33K/F_4 — VREFC_VMC1 — R250 1.33K/F_4 — C474 0.1U/16V/X7R_4

+1.5V_GFX
R249 1.33K/F_4 — VREFD_VMC1 — R247 1.33K/F_4 — C462 0.1U/16V/X7R_4

+1.5V_GFX
R254 1.33K/F_4 — VREFC_VMC3 — R255 1.33K/F_4 — C476 0.1U/16V/X7R_4

+1.5V_GFX
R253 1.33K/F_4 — VREFD_VMC3 — R252 1.33K/F_4 — C475 0.1U/16V/X7R_4

+1.5V_GFX
C12 1 — 2 *1U/6.3V/X5R_NC
C11 1 — 2 1U/6.3V/X5R
C9 1 — 2 1U/6.3V/X5R
C8 1 — 2 1U/6.3V/X5R
C473 1 — 2 0.1U/16V/X7R_4
C34 1 — 2 0.1U/16V/X7R_4
C38 1 — 2 0.1U/16V/X7R_4
C35 1 — 2 0.1U/16V/X7R_4
C22 1 — 2 0.1U/16V/X7R_4
C24 1 — 2 *0.1U/16V/X7R_4_NC

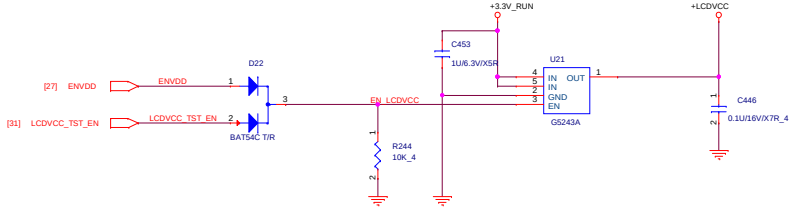
+1.5V_GFX
C16 1 — 2 *1U/6.3V/X5R_NC
C7 1 — 2 1U/6.3V/X5R
C21 1 — 2 1U/6.3V/X5R
C6 1 — 2 1U/6.3V/X5R
C5 1 — 2 0.1U/16V/X7R_4
C30 1 — 2 0.1U/16V/X7R_4
C31 1 — 2 1U/6.3V/X5R
C14 1 — 2 0.1U/16V/X7R_4
C13 1 — 2 0.1U/16V/X7R_4
C15 1 — 2 *0.1U/16V/X7R_4_NC

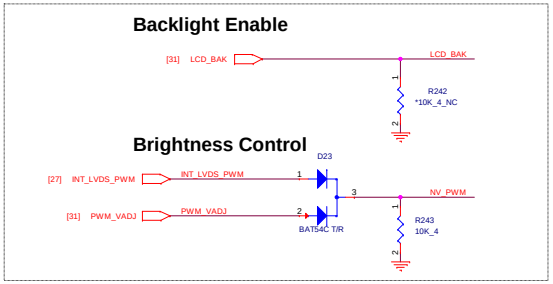
+1.5V_GFX
C489 1 — 2 *1U/6.3V/X5R_NC
C465 1 — 2 1U/6.3V/X5R
C479 1 — 2 1U/6.3V/X5R
C464 1 — 2 1U/6.3V/X5R
C487 1 — 2 0.1U/16V/X7R_4
C481 1 — 2 0.1U/16V/X7R_4
C471 1 — 2 0.1U/16V/X7R_4
C461 1 — 2 0.1U/16V/X7R_4
C458 1 — 2 0.1U/16V/X7R_4
C469 1 — 2 *0.1U/16V/X7R_4_NC

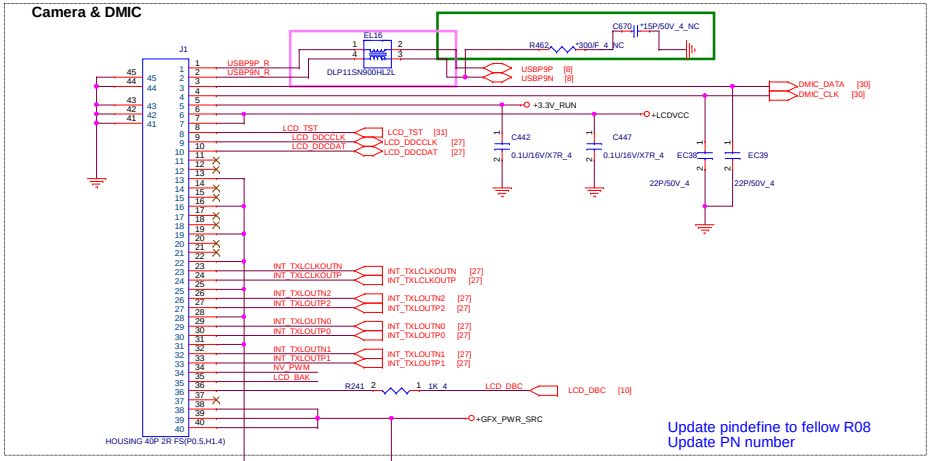
+1.5V_GFX
C470 1 — 2 *1U/6.3V/X5R_NC
C466 1 — 2 1U/6.3V/X5R
C463 1 — 2 1U/6.3V/X5R
C459 1 — 2 1U/6.3V/X5R
C468 1 — 2 0.1U/16V/X7R_4
C480 1 — 2 0.1U/16V/X7R_4
C472 1 — 2 0.1U/16V/X7R_4
C491 1 — 2 0.1U/16V/X7R_4
C477 1 — 2 0.1U/16V/X7R_4
C460 1 — 2 *0.1U/16V/X7R_4_NC

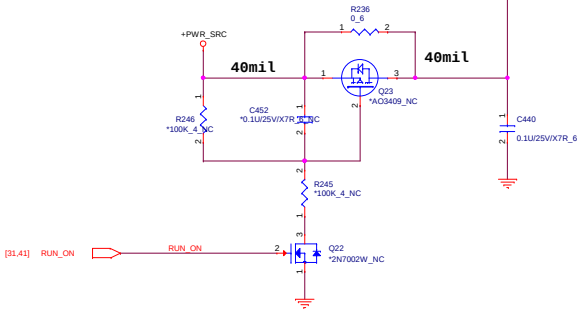
Quanta Computer Inc.
PROJECT : R0AA

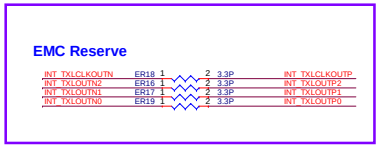
Size	Document Number	Rev
	N11M-GE2 VRAM-2(DDR3 BGA96)	1A
Date: Monday, June 25, 2012	Sheet 21 of 55	









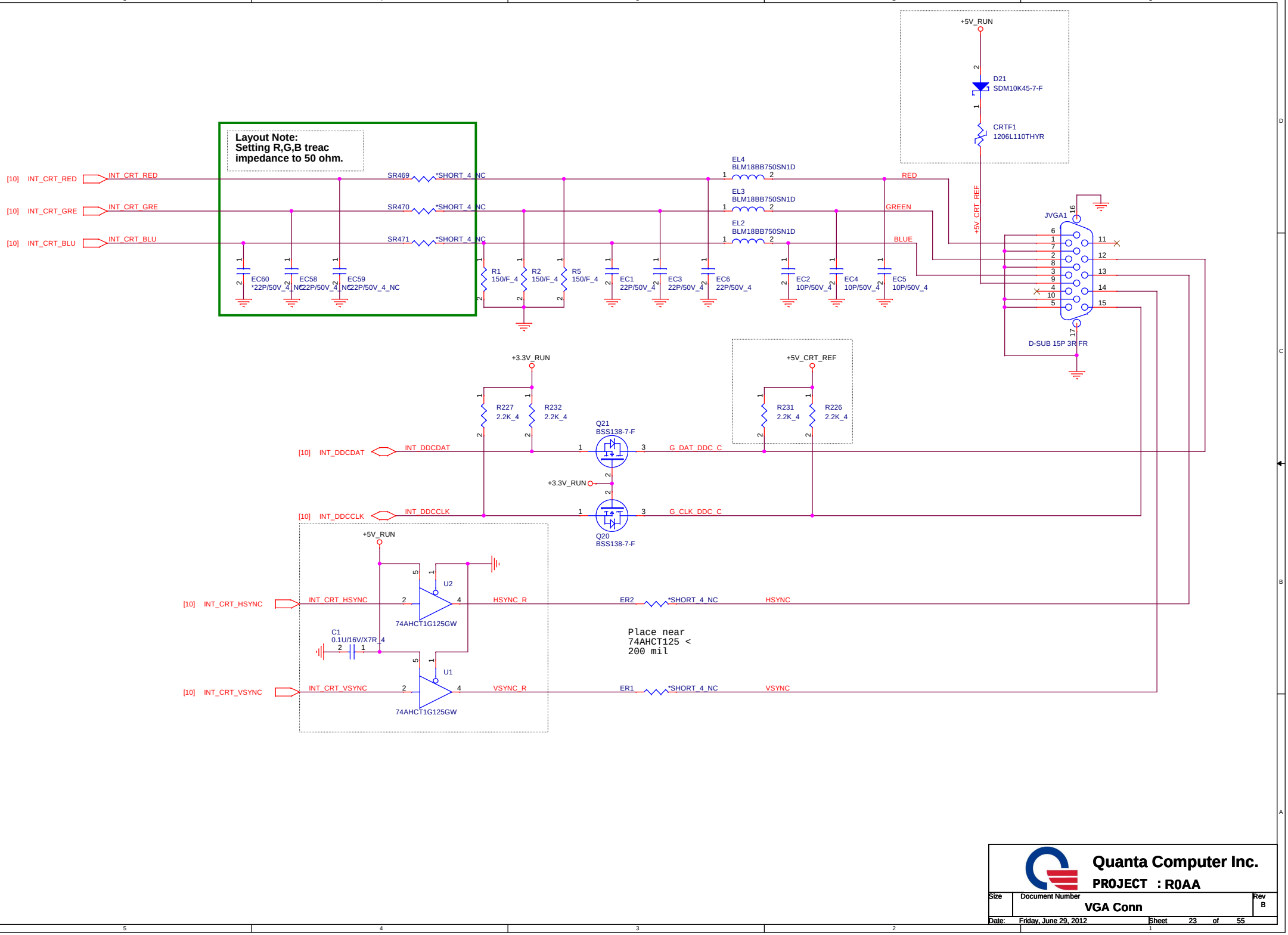


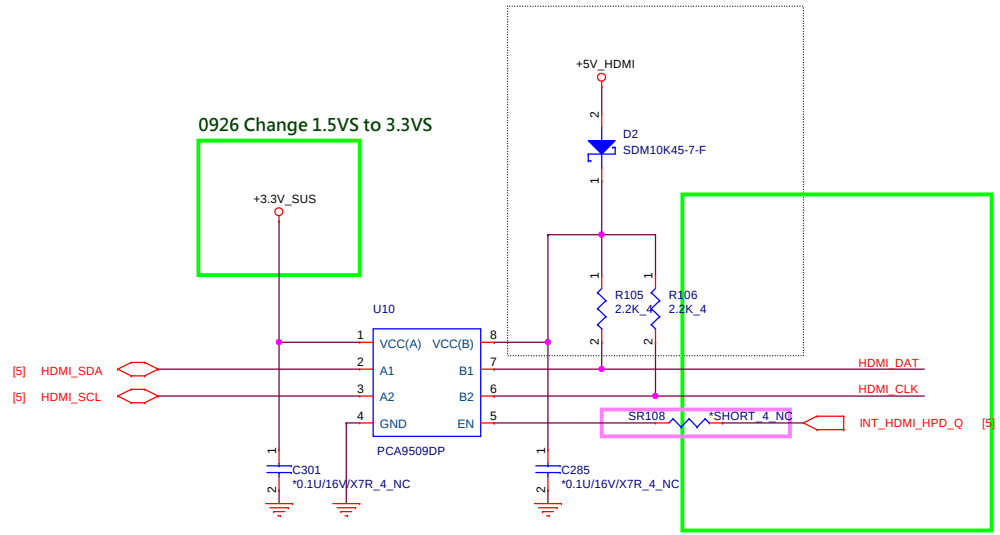
Quanta Computer Inc.

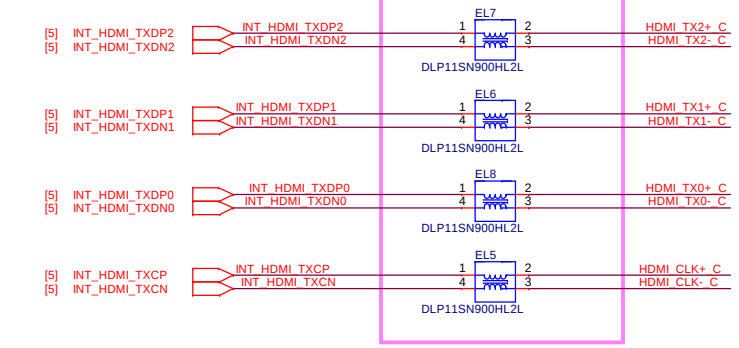
PROJECT : R0AA

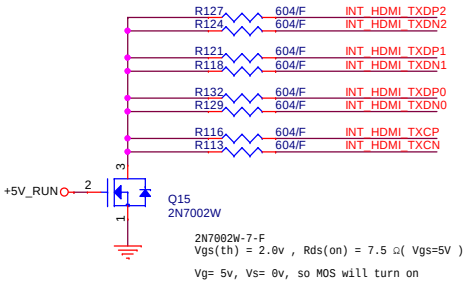
Size	Document Number	Rev
	LVDS Conn.	B

Date: Monday, July 02, 2012 Sheet 22 of 55

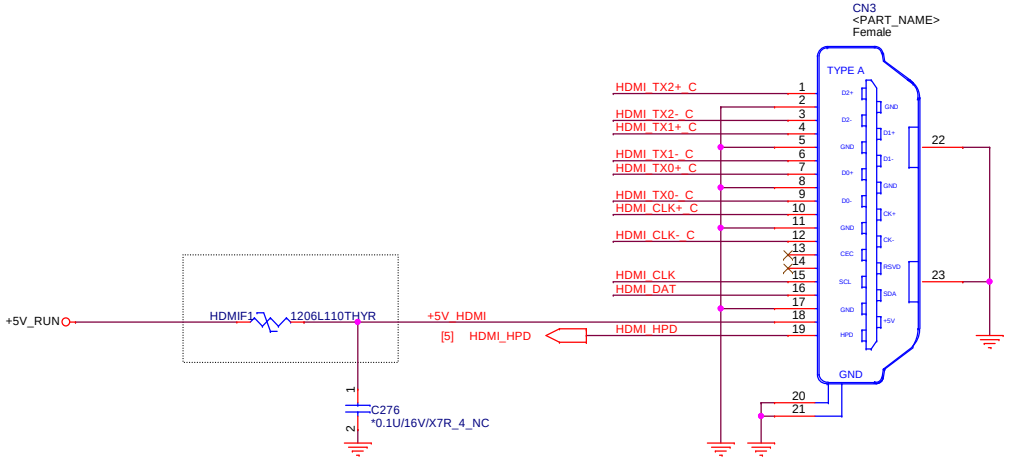

Layout Note:
Setting R,G,B treac
impedance to 50 ohm.
+5V_RUN
D21
SDM10K45-7-F
CRTF1
1206L110THYR
+5V_CRT_REF
[10] INT_CRT_RED
[10] INT_CRT_GRE
[10] INT_CRT_BLU
INT_CRT_RED
INT_CRT_GRE
INT_CRT_BLU
SR469 *SHORT_4_NC
SR470 *SHORT_4_NC
SR471 *SHORT_4_NC
EL4 BLM18BB750SN1D
EL3 BLM18BB750SN1D
EL2 BLM18BB750SN1D
RED
GREEN
BLUE
EC60 *22P/50V_4_NC
EC58 22P/50V_4_NC
EC59 22P/50V_4_NC
R1 150/F_4
R2 150/F_4
R5 150/F_4
EC1 22P/50V_4
EC3 22P/50V_4
EC6 22P/50V_4
EC2 10P/50V_4
EC4 10P/50V_4
EC5 10P/50V_4
JVGA1
D-SUB 15P 3R FR
+3.3V_RUN
+5V_CRT_REF
R227 2.2K_4
R232 2.2K_4
R231 2.2K_4
R226 2.2K_4
Q21 BSS138-7-F
Q20 BSS138-7-F
[10] INT_DDCDAT
[10] INT_DDCCLK
INT_DDCDAT
INT_DDCCLK
G_DAT_DDC_C
G_CLK_DDC_C
+5V_RUN
U2
U1
74AHCT1G125GW
74AHCT1G125GW
C1
0.1U/16V/X7R_4
[10] INT_CRT_HSYNC
[10] INT_CRT_VSYNC
INT_CRT_HSYNC
INT_CRT_VSYNC
HSYNC_R
VSYNC_R
ER2 *SHORT_4_NC
ER1 *SHORT_4_NC
HSYNC
VSYNC
Place near
74AHCT125 <
200 mil
Quanta Computer Inc.
PROJECT : R0AA
Size
Document Number
VGA Conn
Rev
B
Date: Friday, June 29, 2012
Sheet 23 of 55







HDMI Conn.



Quanta Computer Inc.		
PROJECT : R0AA		
Size	Document Number: HDMI CONN	Rev: B
Date: Thursday, June 28, 2012	Sheet 24 of 55	

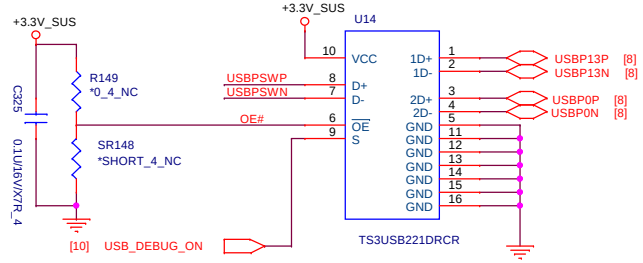
S	OE	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D

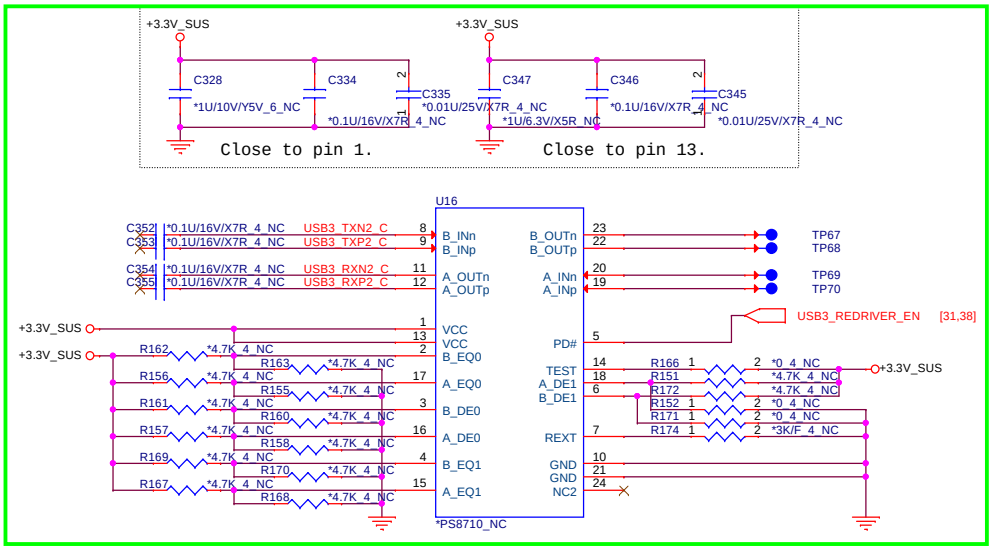
USB Power share

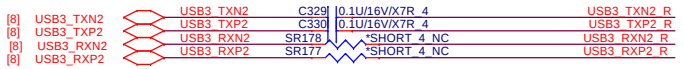
USBP0_BUS_SW_CB0	Mode
Low	DCP, Auto-detect
High	CDP, BC Spec 1.1

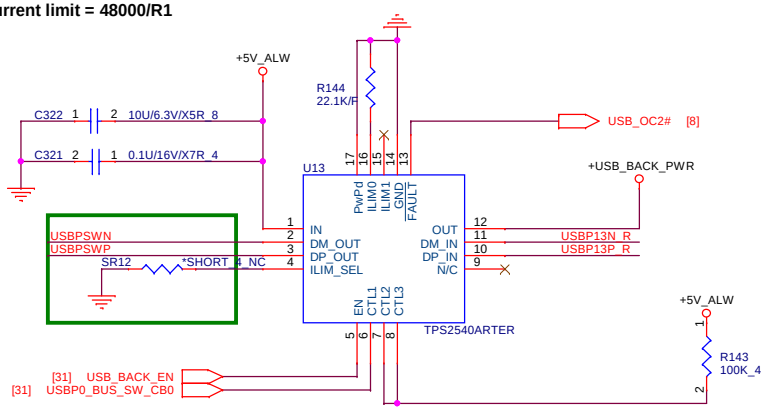
	R1	mA	
OC limitation	100k ohm	480	
	22.1k ohm	2171	Applied Now

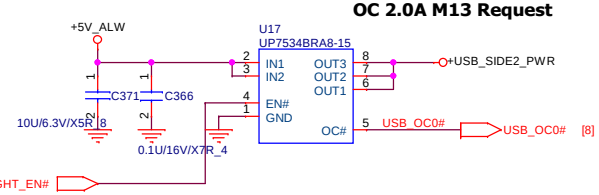
Current limit = 48000/R1

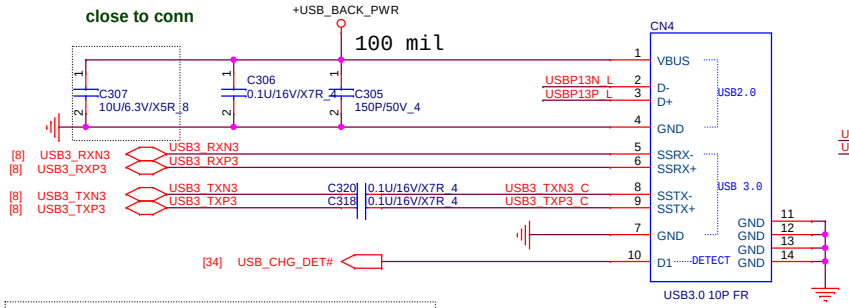


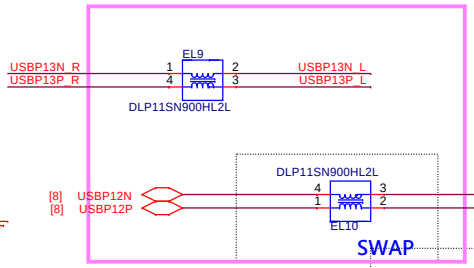


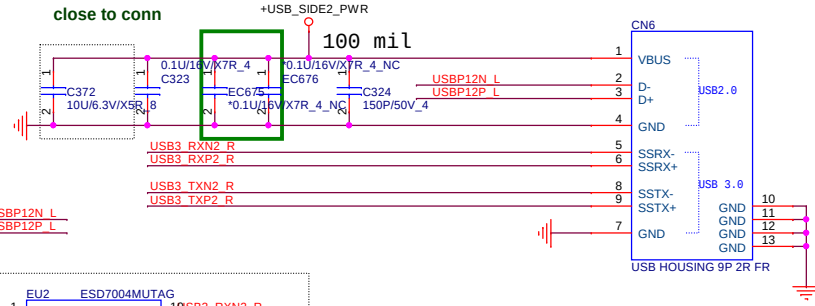


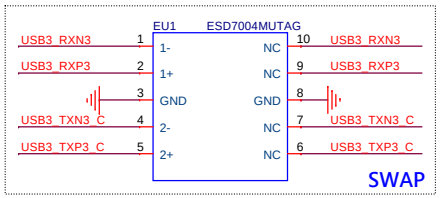






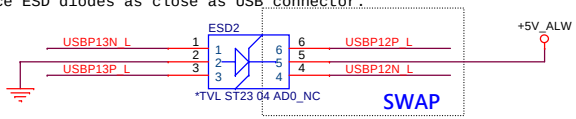


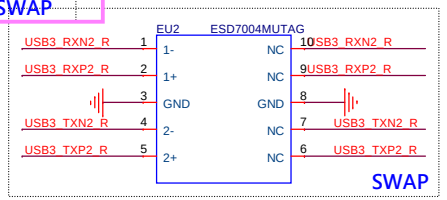




ESD Function

Place ESD diodes as close as USB connector.





Quanta Computer Inc.

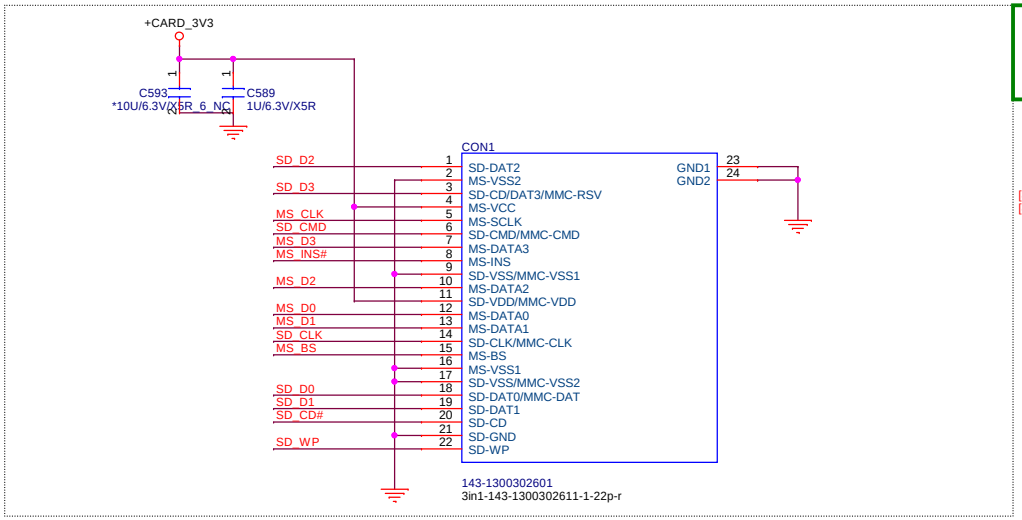
PROJECT : R0AA

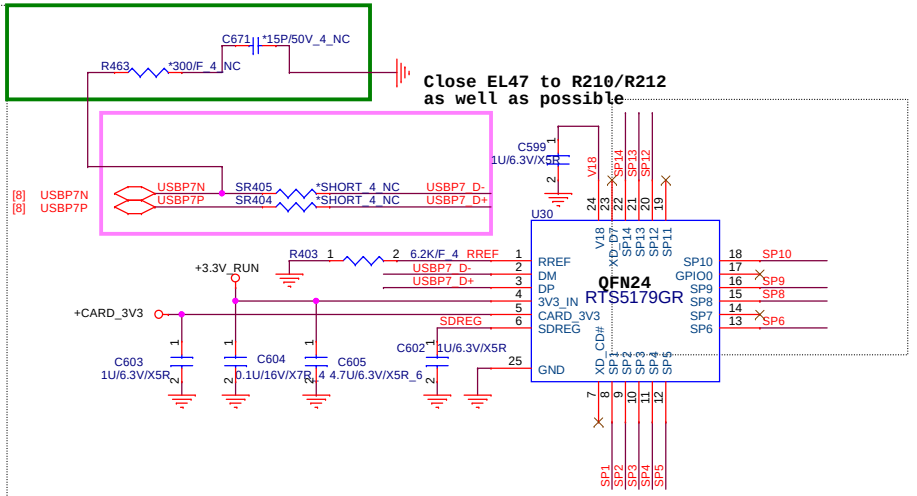
Size	Document Number	Rev
	USB 3.0 port / USB power share	B

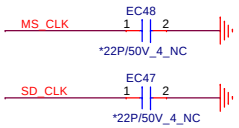
Date: Thursday, June 28, 2012 Sheet 25 of 55

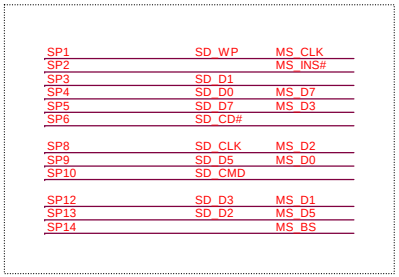
Cardreader (RTS5179GR) Support SD3.0 USH50

Change CON1 footprint to 3in1-143-1300302611-1-22p-r(follow R09)









Share Pin

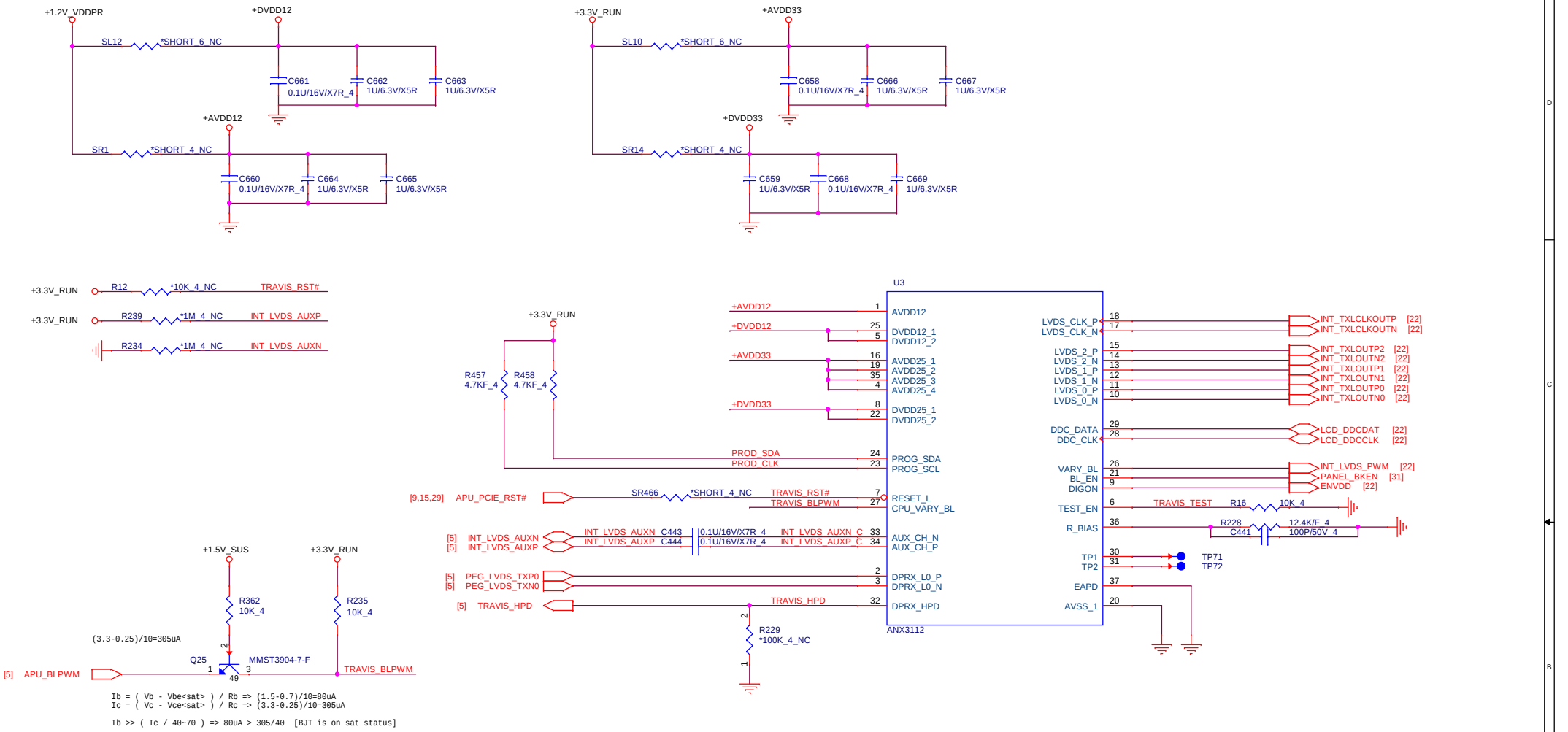
	SD CARD	MS CARD
SP1	SW_WP	MS_CLK
SP2		MS_INS#
SP3	SD_D1	
SP4	SD_D0	MS_D7
SP5	SD_D7	MS_D3
SP6	SD_CD#	
SP7	SD_D6	MS_D6
SP8	SD_CLK	MS_D2
SP9	SD_D5	MS_D0
SP10	SD_CMD	
SP11	SD_D4	MS_D4
SP12	SD_D3	MS_D1
SP13	SD_D2	MS_D5
SP14		MS_BS

Quanta Computer Inc.

PROJECT : R0AA

Size	Document Number	Rev
	Cardreader (RTS5179GR)	1A

Date: Thursday, June 28, 2012 Sheet 26 of 55



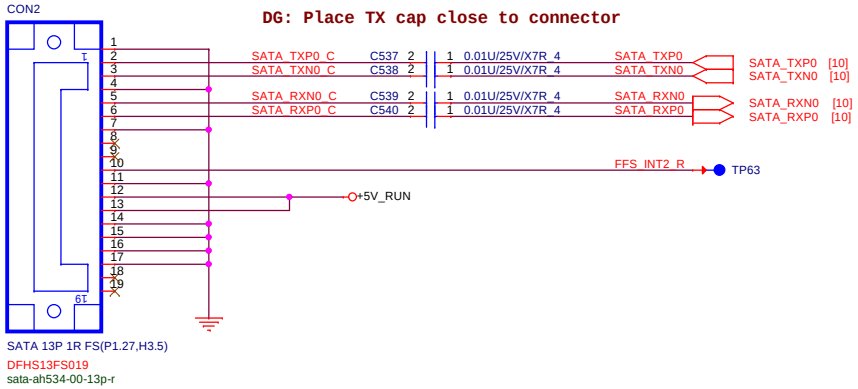
Quanta Computer Inc.

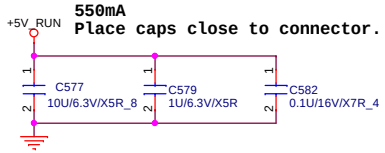
PROJECT : R0AA

Size	Document Number	Rev
	AXN3112	B

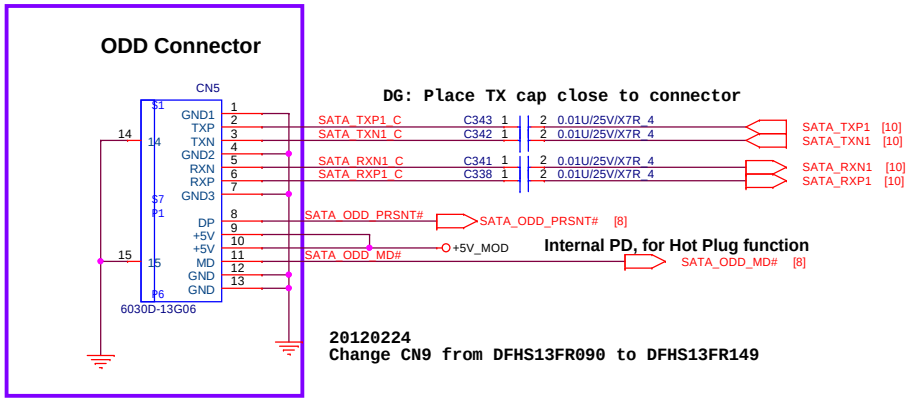
Date: Monday, June 25, 2012 Sheet 27 of 55

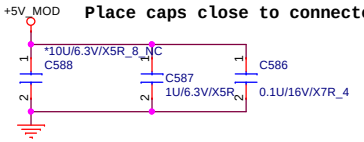
HDD



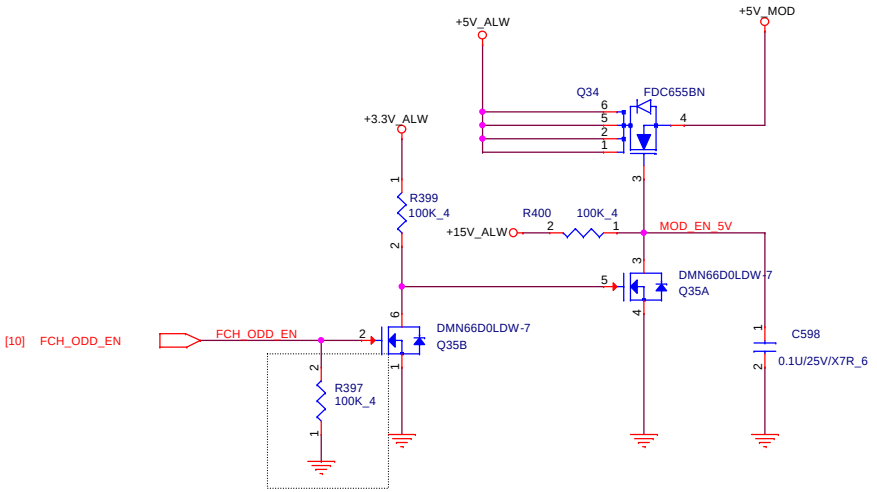


ODD





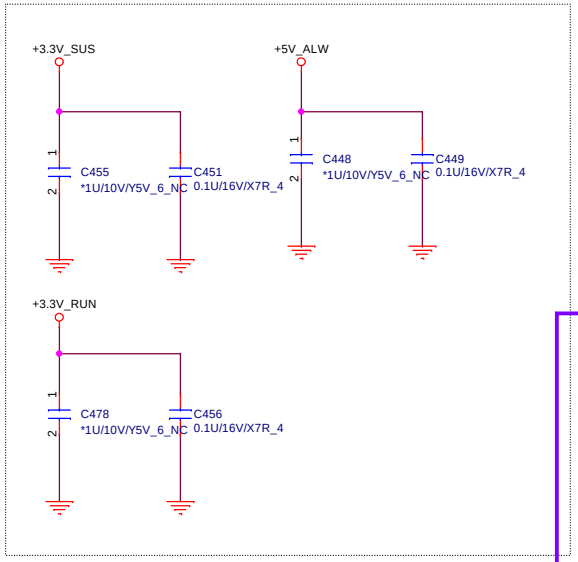
Support Zero power ODD



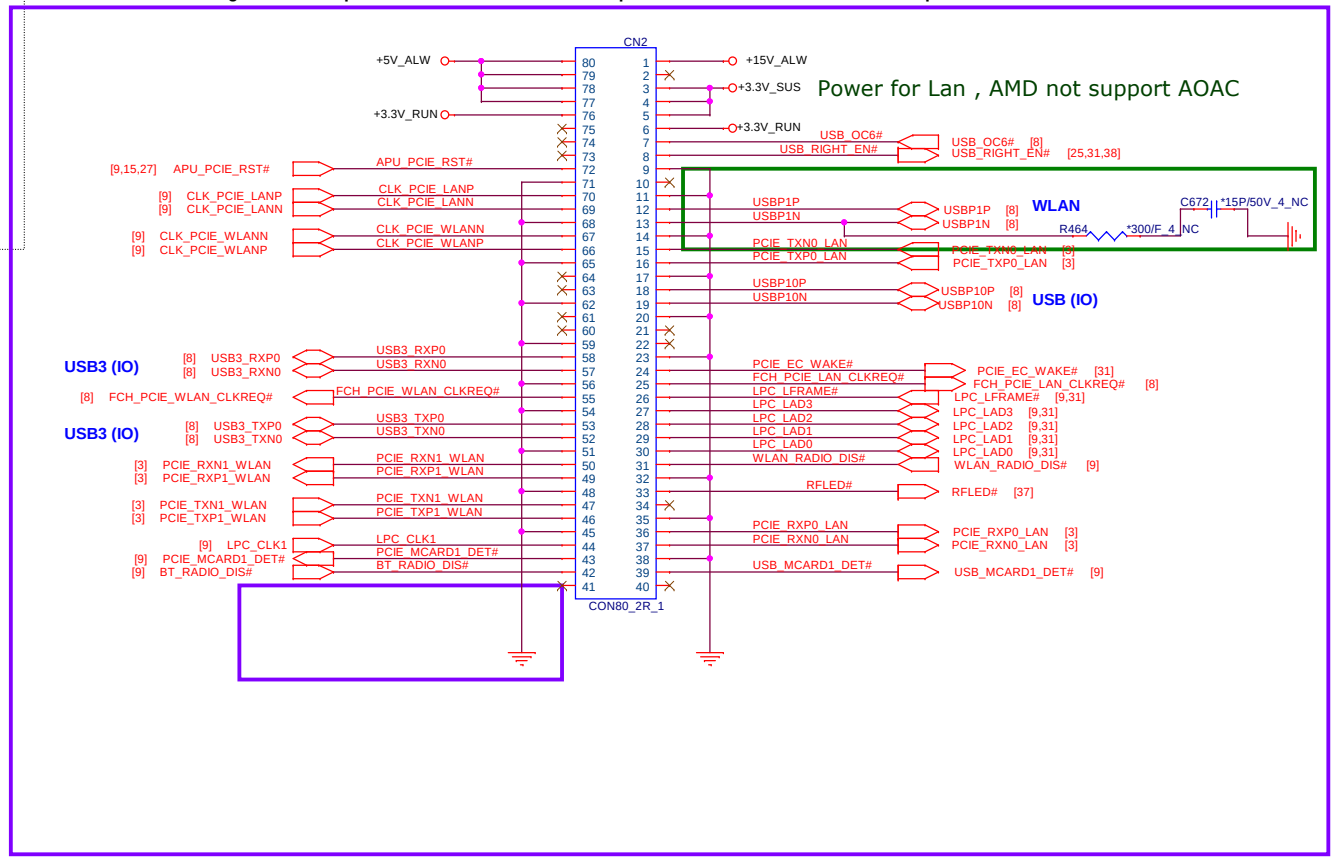
Quanta Computer Inc.

PROJECT : R0AA

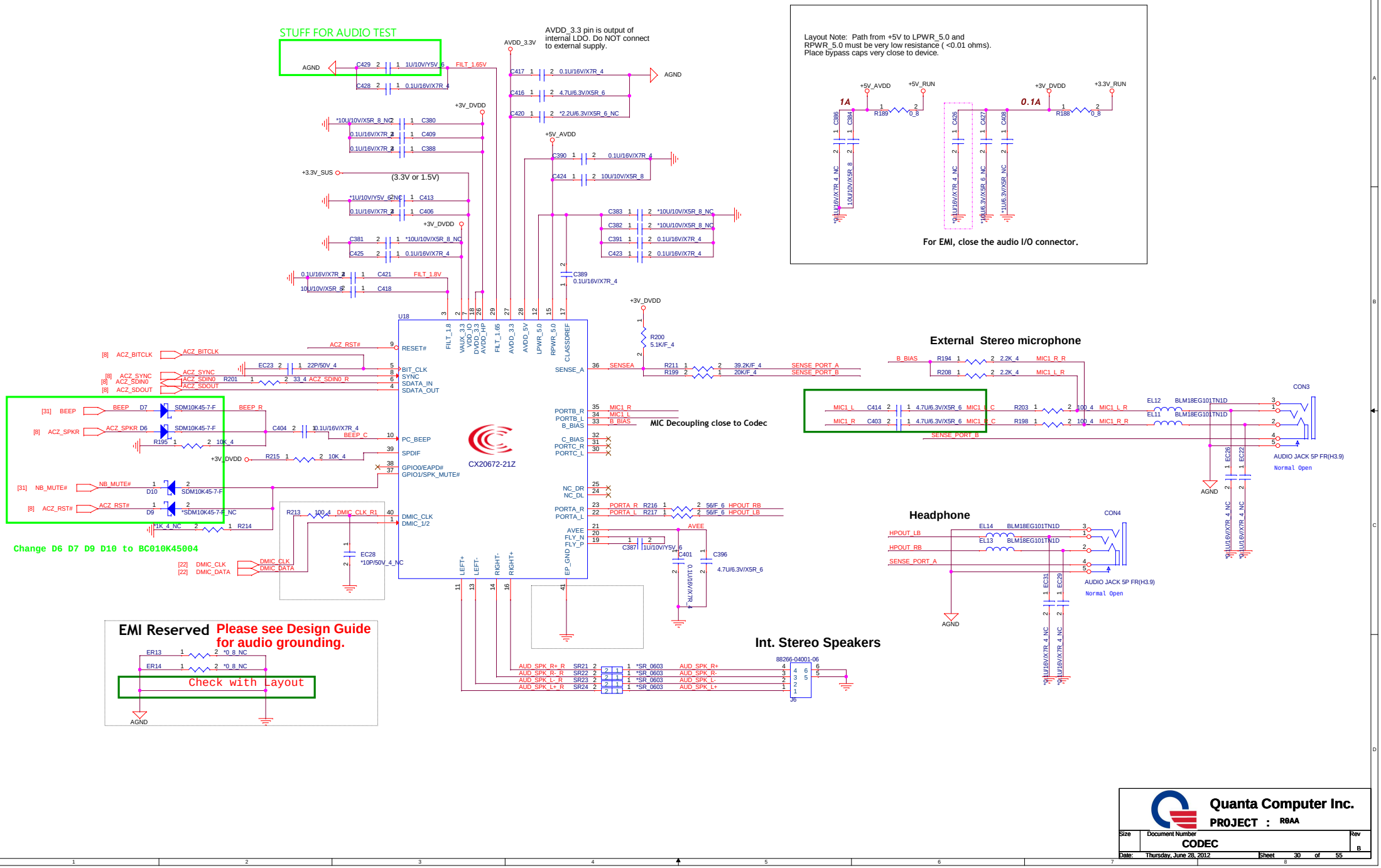
Size	Document Number	Rev
	SATA HDD/ODD	B
Date: Monday, June 25, 2012	Sheet 28 of 55	

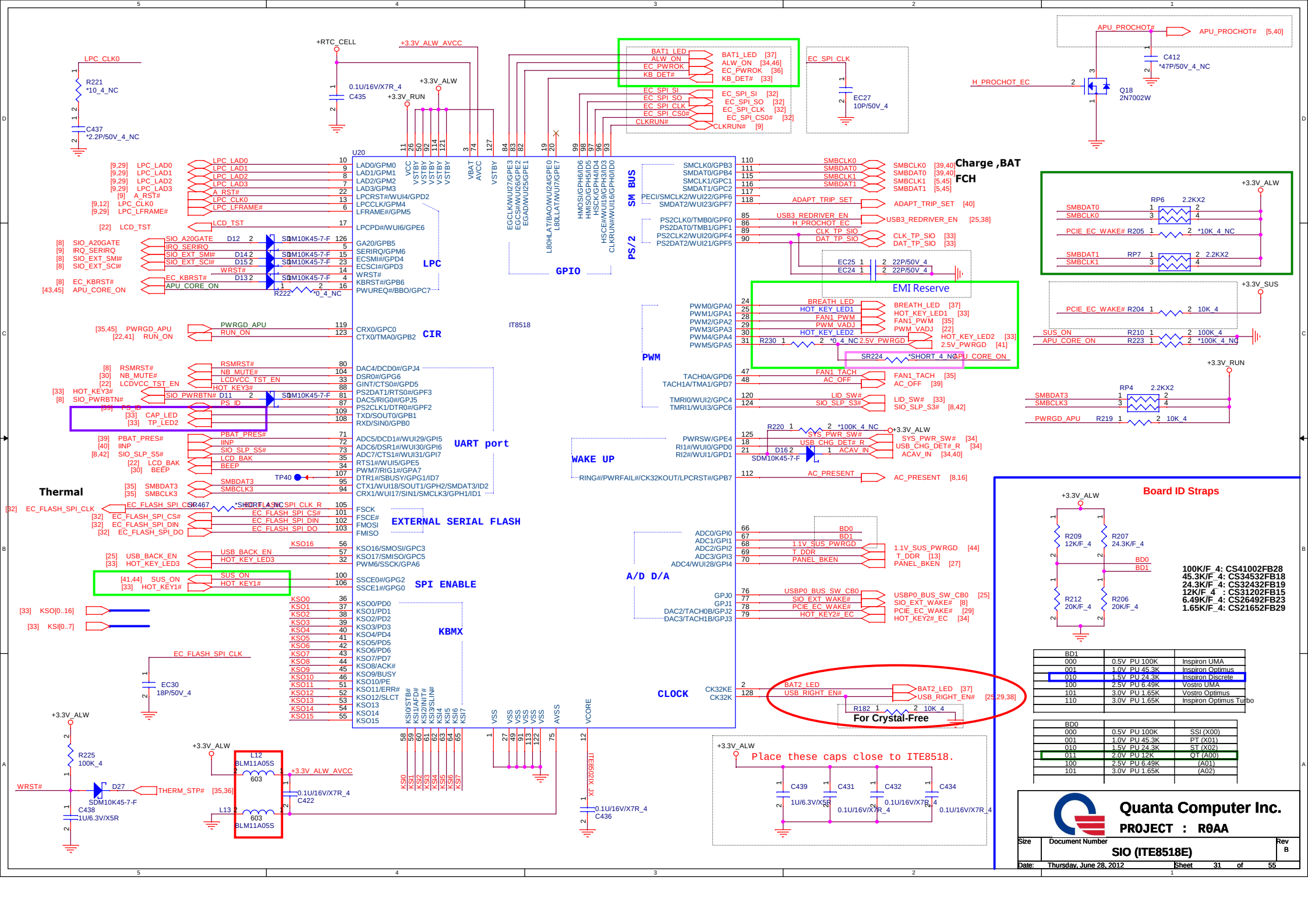


20120229
Change CN9 footprint from "88161-08001-80p-ldh" to "88069-8001b-bs-80p-ldh-smt"



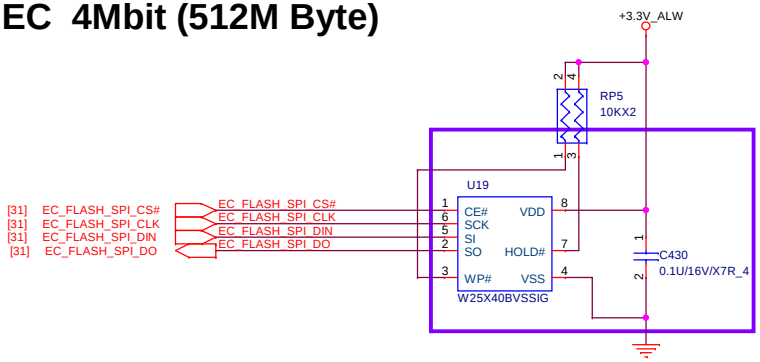
Quanta Computer Inc.		
PROJECT : R0AA		
Size	Document Number: BTB CONN	Rev: B
Date: Monday, June 25, 2012	Sheet 29 of 55	


STUFF FOR AUDIO TEST
AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.
Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms). Place bypass caps very close to device.
For EMI, close the audio I/O connector.
External Stereo microphone
Headphone
Int. Stereo Speakers
MIC Decoupling close to Codec
CX20672-21Z
U18
Change D6 D7 D9 D10 to BC010K45004
EMI Reserved
Please see Design Guide for audio grounding.
Check with Layout
AUDIO JACK 5P FR(H3.9)
Normal Open
Quanta Computer Inc.
PROJECT : R0AA
CODEC
Date: Thursday, June 28, 2012
Sheet 30 of 55

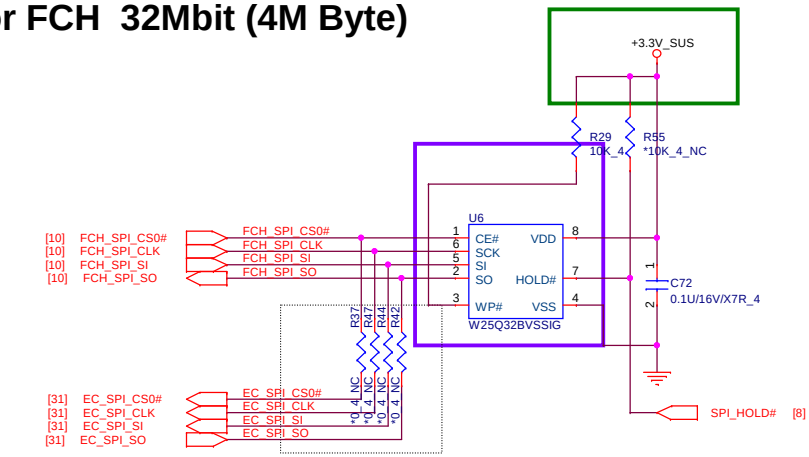

U20
IT8518
LPC
CIR
GPIO
SM BUS
PS/2
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
EMI Reserve
Charge ,BAT
FCH
Thermal
Board ID Straps
For Crystal-Free
Place these caps close to ITE8518.
100K/F_4: CS41002FB28
45.3K/F_4: CS34532FB18
24.3K/F_4: CS32432FB19
12K/F_4 : CS31202FB15
6.49K/F_4: CS26492FB23
1.65K/F_4: CS21652FB29
Quanta Computer Inc.
PROJECT : R0AA
SIO (ITE8518E)
Thursday, June 28, 2012
Sheet 31 of 55

FLASH / RTC

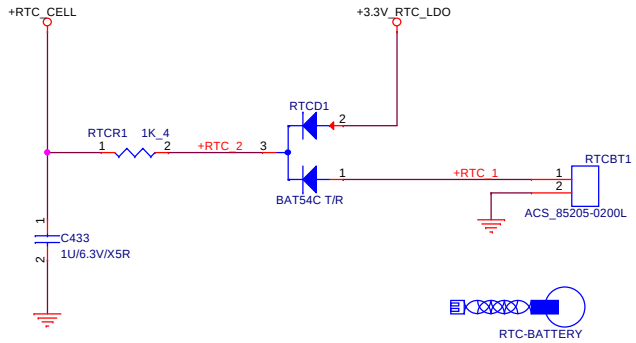
For EC 4Mbit (512M Byte)



For FCH 32Mbit (4M Byte)



RTC



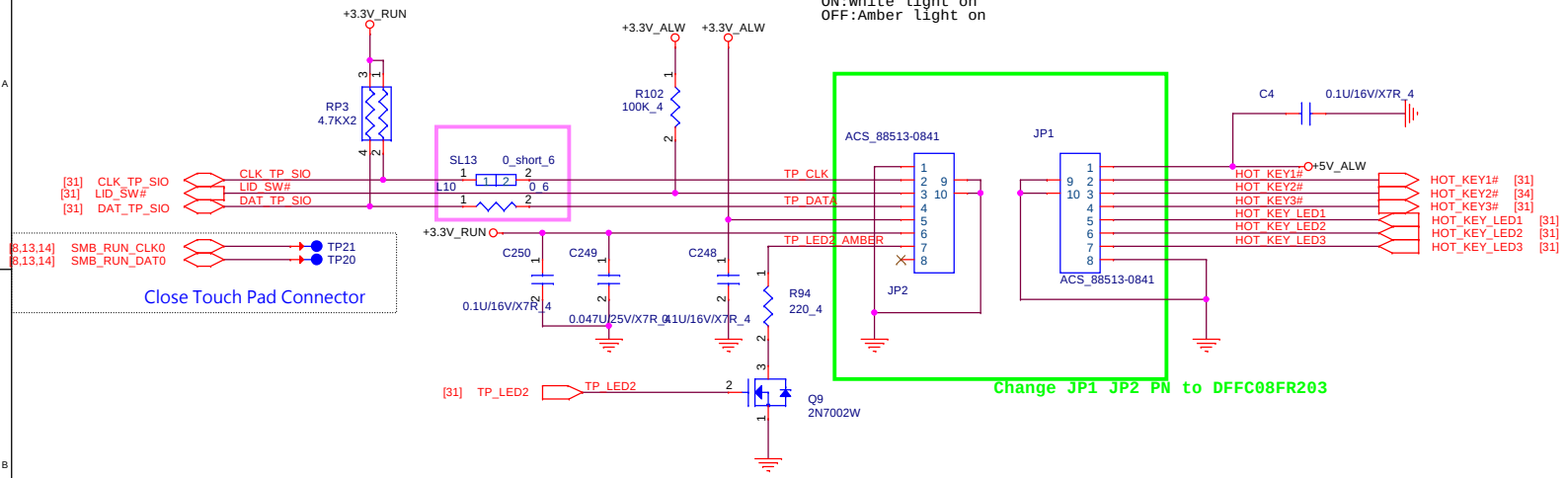
Double, 25'C, Vf=0.4V, If=25mA
one, 25'C, Vf=0.35V, If=15.8mA

Quanta Computer Inc.		
PROJECT : R0AA		
Size	Document Number: FLASH / RTC	Rev: B
Date: Monday, June 25, 2012	Sheet 32 of 55	

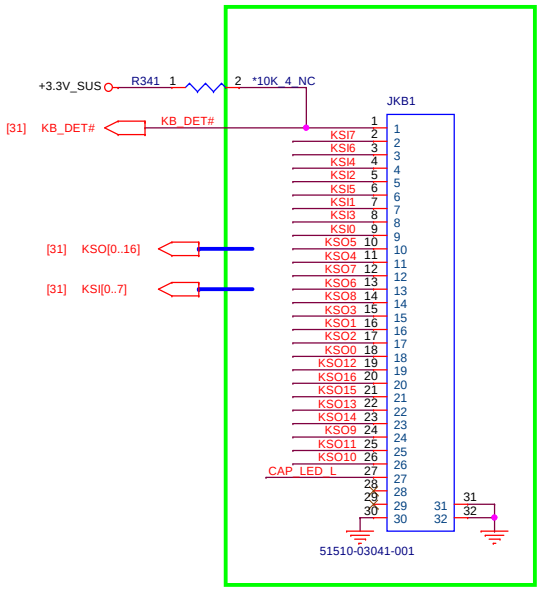
KEYBOARD CONNECTOR

Touch Pad

ON:White light on
OFF:Amber light on

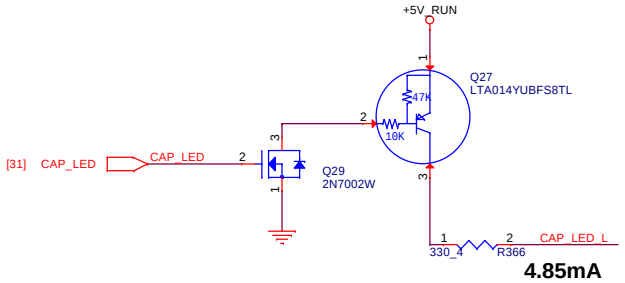


Change JP1 JP2 PN to DFFC08FR203



Change JKB1 PN to DFFC30FR075

Vi(on_max)= -1.4V
Vi(off_min)=-0.3

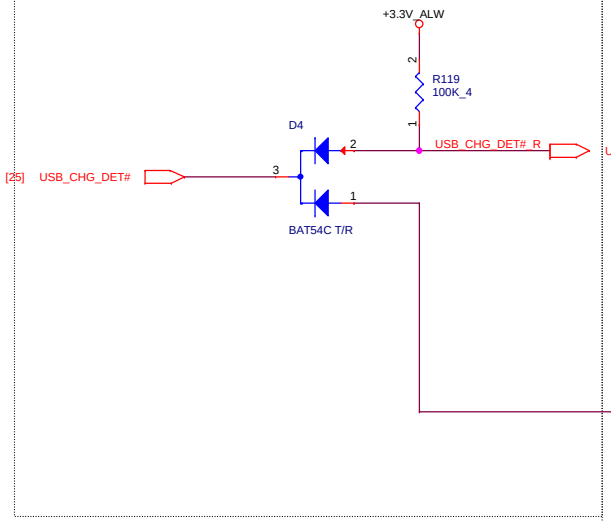


4.85mA

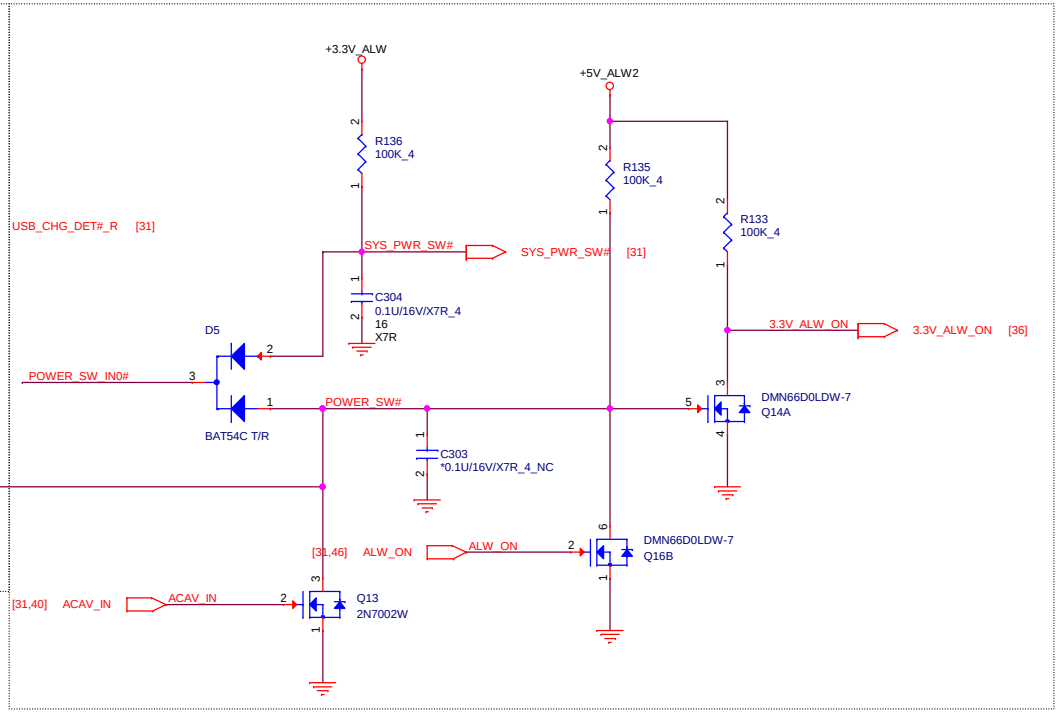
Quanta Computer Inc.
PROJECT : R07

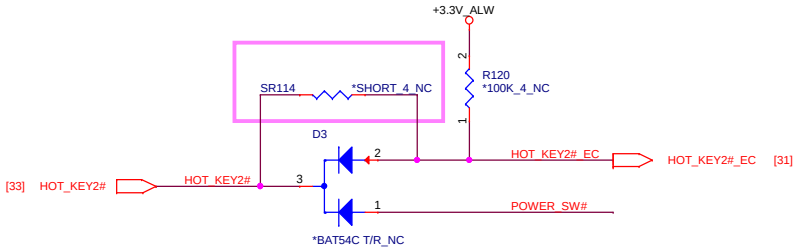
Size	Document Number	Rev
	TP / KB	1A
Date: Thursday, June 28, 2012	Sheet 33 of 55	

For USB charger usage

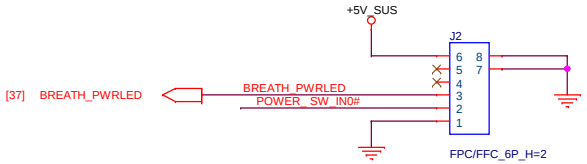


3V ALW ON POWER LOGIC





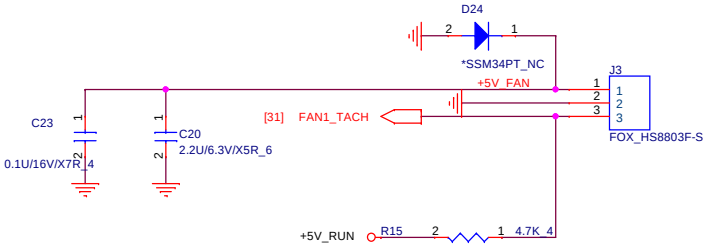
TO PWR button board

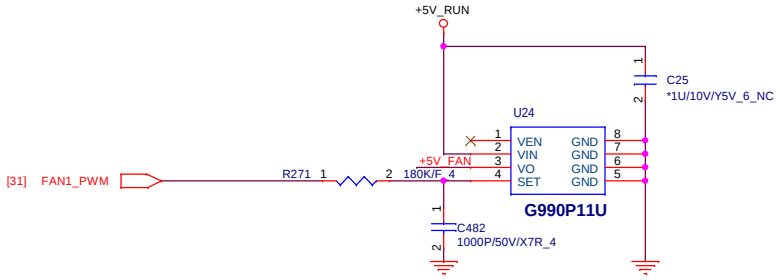


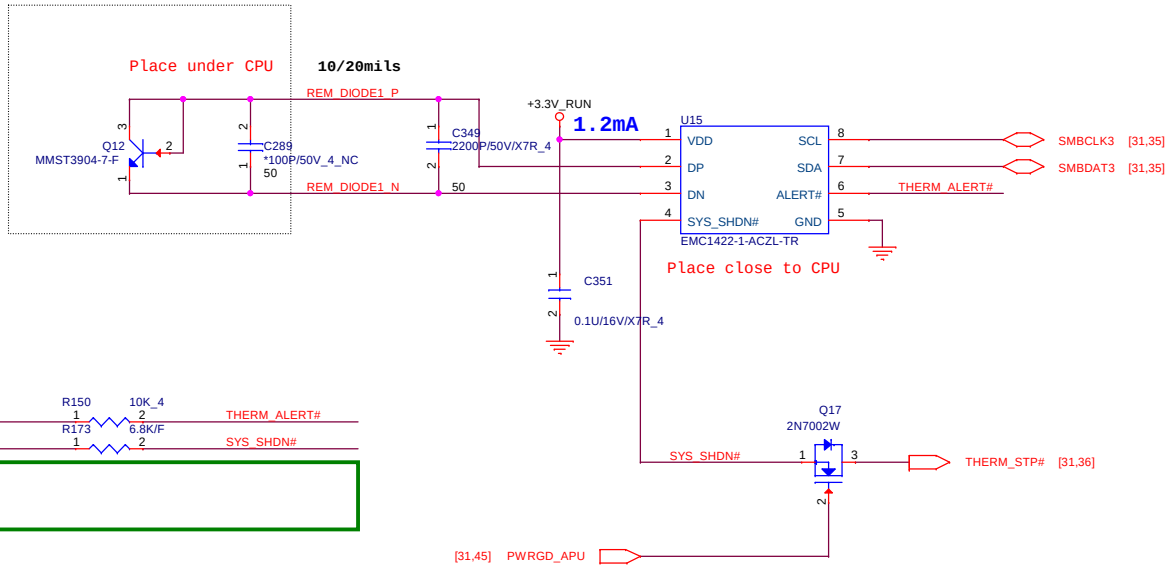
Quanta Computer Inc.

PROJECT : R07

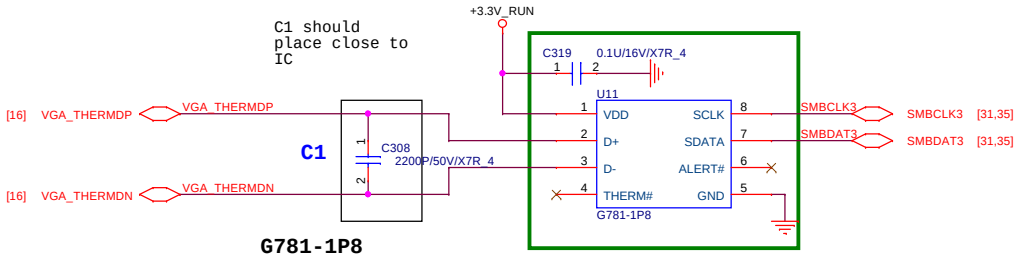
Size	Document Number	Rev
	PWR SW/LED	B
Date: Friday, July 06, 2012	Sheet 34 of 55	







SYS_SHD# / ALERT#	4.7K	6.8K	10K	15K	22K	33K
4.7K	77'C	83'C	89'C	95'C	101'C	107'C
6.8K	78'C	84'C	90'C	96'C	102'C	108'C
10K	79'C	85'C	91'C	97'C	103'C	109'C
15K	80'C	86'C	92'C	98'C	104'C	110'C
22K	81'C	87'C	93'C	99'C	105'C	111'C
33K	82'C	88'C	94'C	100'C	106'C	112'C



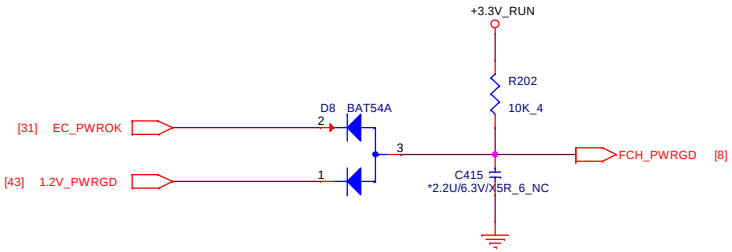
G781-1P8

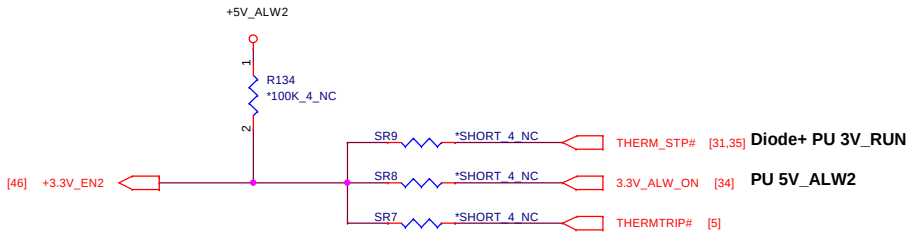
SMBus address is 1001101xb (9Ah) (x is R/W bit).

Quanta Computer Inc.

PROJECT : R07

Size	Document Number	Rev
	FAN & THERMAL	B
Date: Monday, June 25, 2012	Sheet 35 of 55	





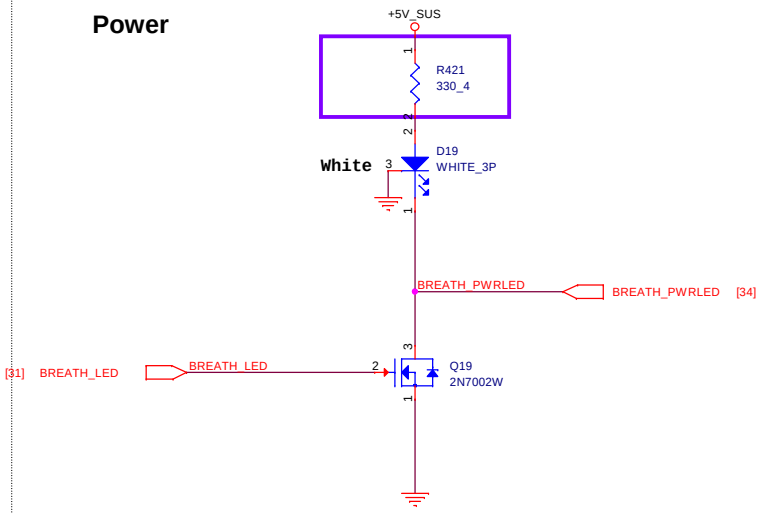
Quanta Computer Inc.

PROJECT : R07

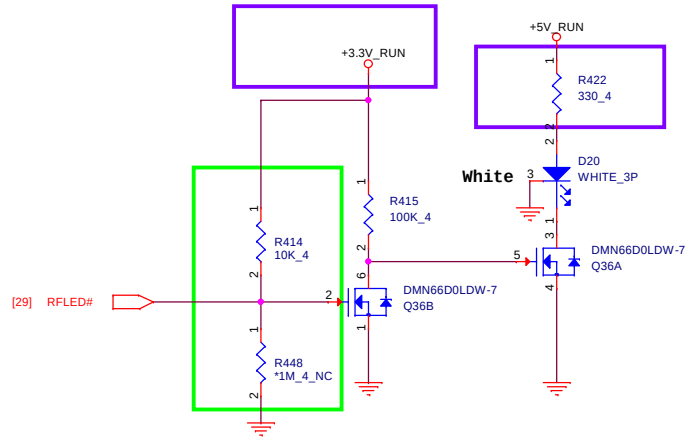
Size	Document Number	Rev
	System Reset Circuit	1A

Date: Monday, June 25, 2012 Sheet 36 of 55

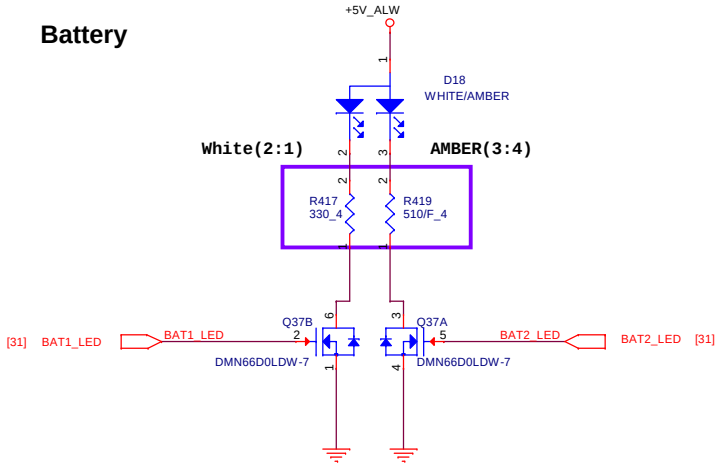
Power



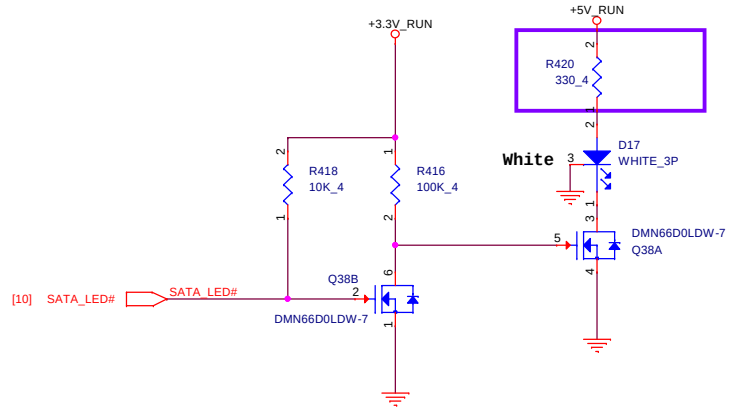
Bluetooth / WLAN on/off LED



Battery



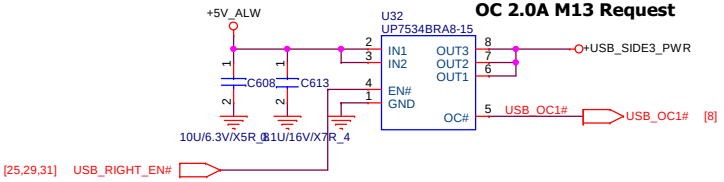
HDD activity LED.



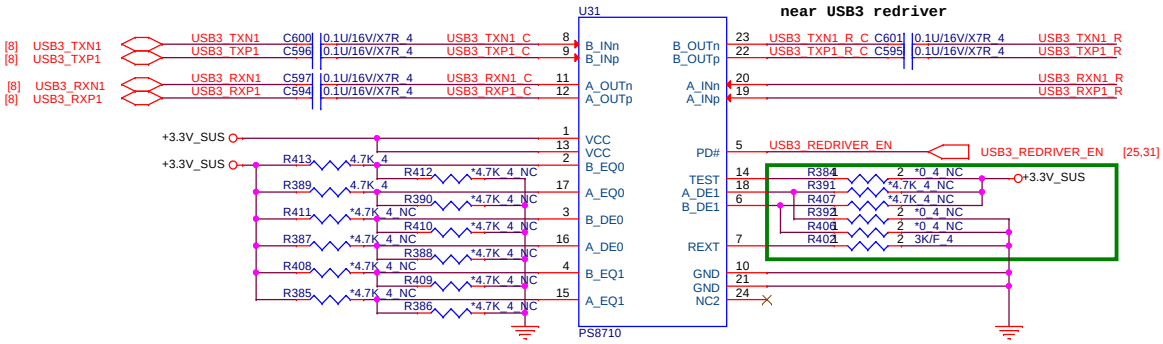
Quanta Computer Inc.		
PROJECT : R07		
Size	Document Number: LED	Rev: 1A
Date: Monday, June 25, 2012	Sheet 37 of 55	

Del Colay reserve

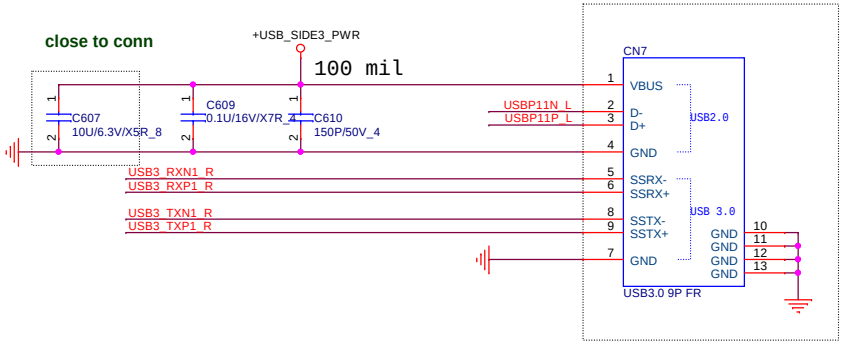
I continuous 1.5A
OC 2.0A M13 Request

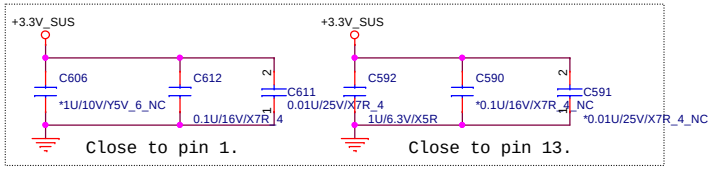


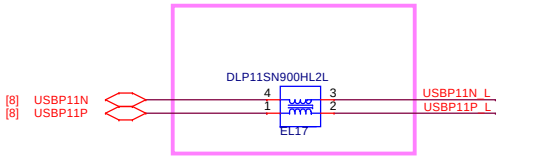
near USB3 redriver

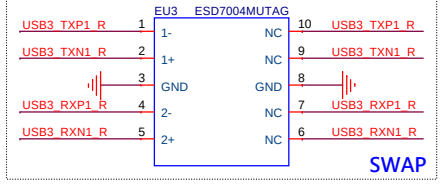


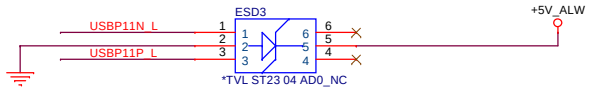
close to conn











Chip test mode enable.
3.3V tolerant. Internally pulled down at ~ 150K ohm
TEST ==
L: Normal operation (default)
H: Test mode enable

Programmable output pre-emphasis level setting for channel A
3.3V tolerant. Internally pulled down at ~ 150K ohm
[A_DE1, A_DE0] ==
LL: 3.5dB de-emphasis
LH: No de-emphasis
HL: 7dB de-emphasis with boost output swing
HH: 5dB de-emphasis with boost output swing

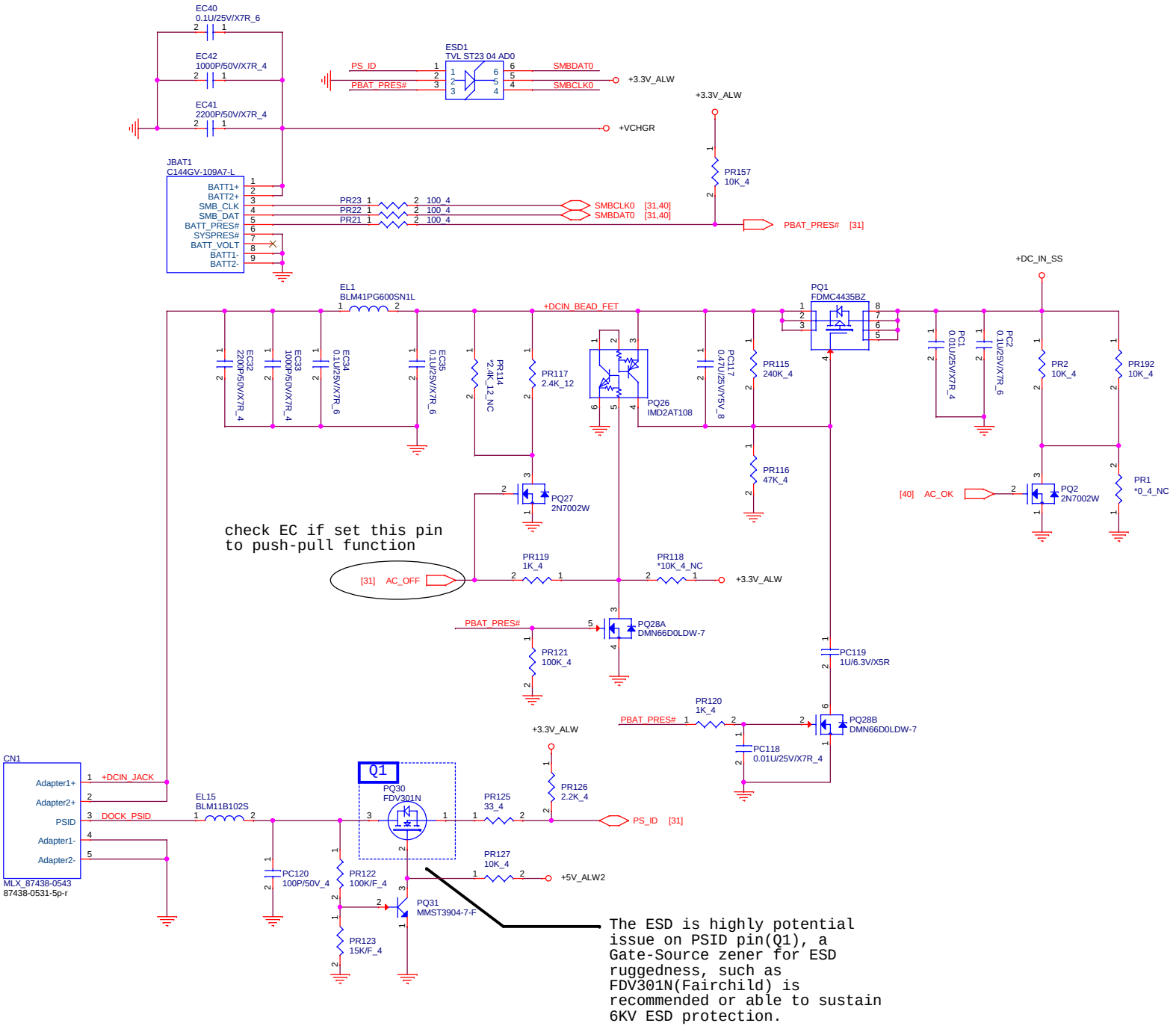
Equalizer control and program for channel A
3.3V tolerant. Internally pulled down at ~ 150K ohm
[A_EQ1, A_EQ0] ==
LL: adaptive EQ enable
LH: program EQ for channel loss up to 7dB
HL: program EQ for channel loss up to 14.5dB
HH: program EQ for channel loss up to 11.5dB

Programmable output pre-emphasis level setting for channel B
3.3V tolerant. Internally pulled down at ~ 150K ohm
[B_DE1, B_DE0] ==
LL: 3.5dB de-emphasis
LH: No de-emphasis
HL: 7dB de-emphasis with boost output swing
HH: 5dB de-emphasis with boost output swing

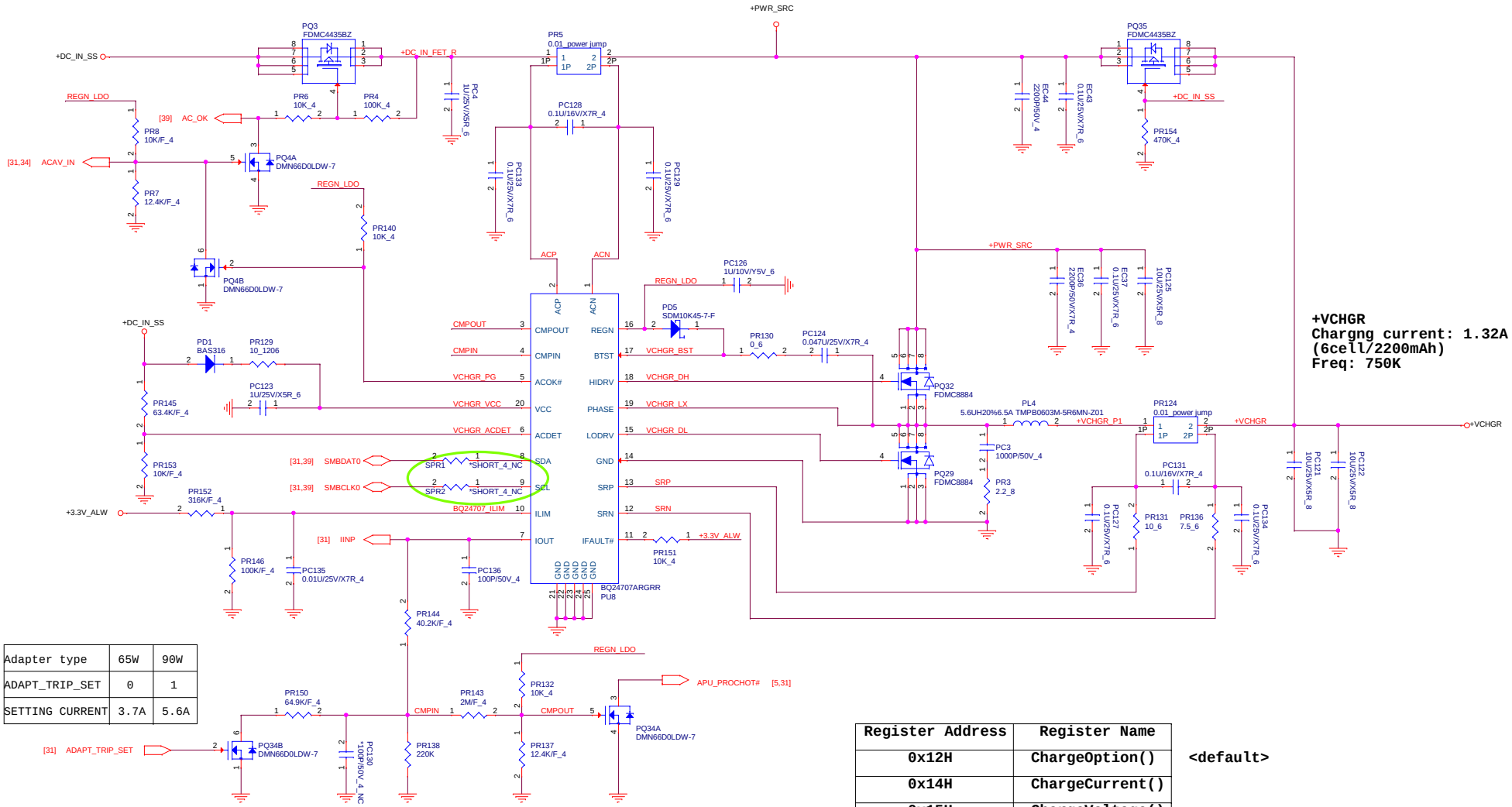
Equalizer control and program for channel B
3.3V tolerant. Internally pulled down at ~ 150K ohm
[B_EQ1, B_EQ0] ==
LL: adaptive EQ enable
LH: program EQ for channel loss up to 7dB
HL: program EQ for channel loss up to 14.5dB
HH: program EQ for channel loss up to 11.5dB

Quanta Computer Inc.
PROJECT : R0AA

Size	Document Number	Rev
	USB 3.0 Left	B
Date: Thursday, June 28, 2012	Sheet 38 of 55	



Quanta Computer Inc.		
PROJECT : R0AA		
Size	Document Number: DCIN & BATT	Rev: B
Date:	Sheet 39 of 55	



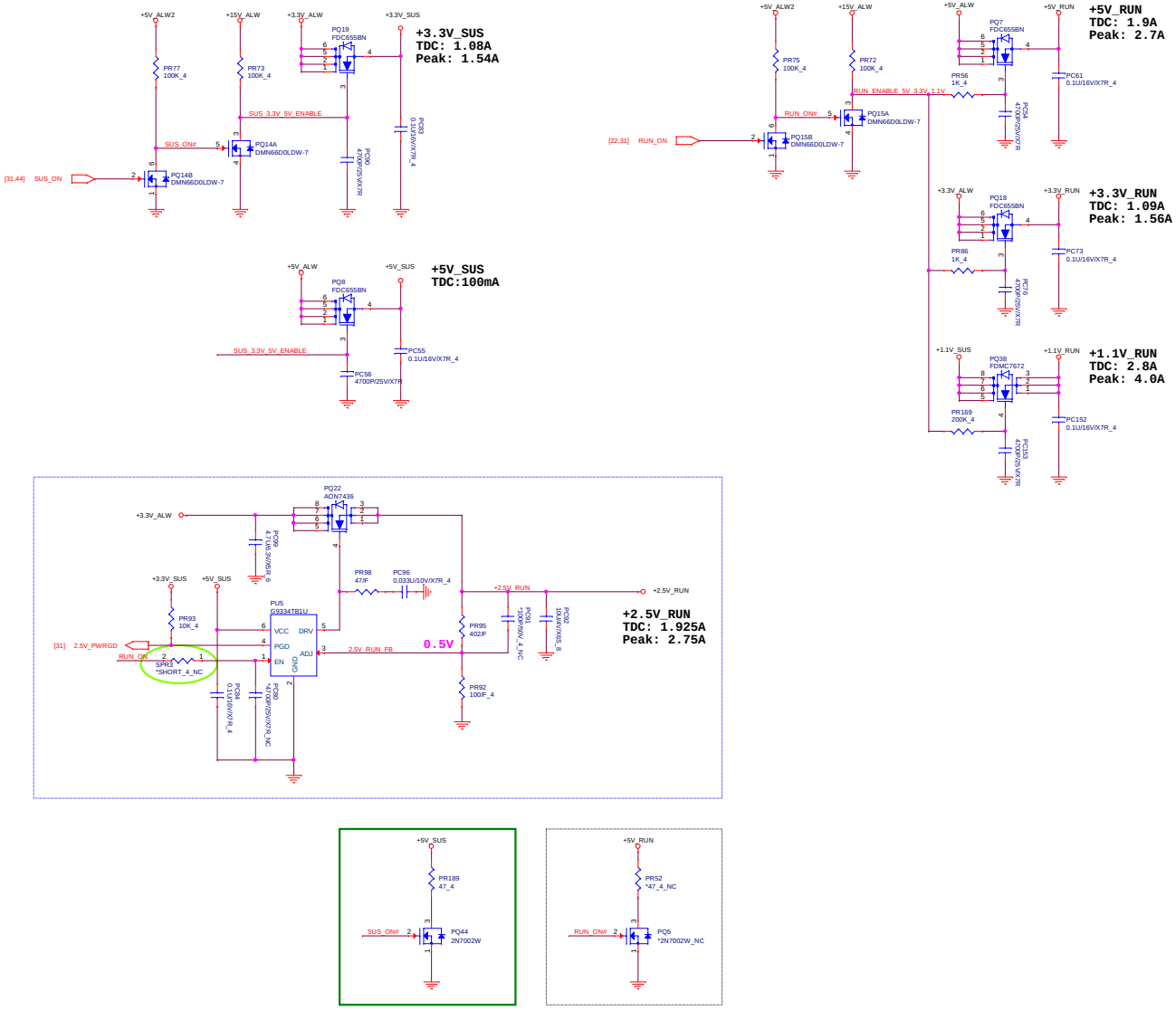
+VCHGR
Chargng current: 1.32A
(6cell/2200mAh)
Freq: 750K

Adapter type	65W	90W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	3.7A	5.6A

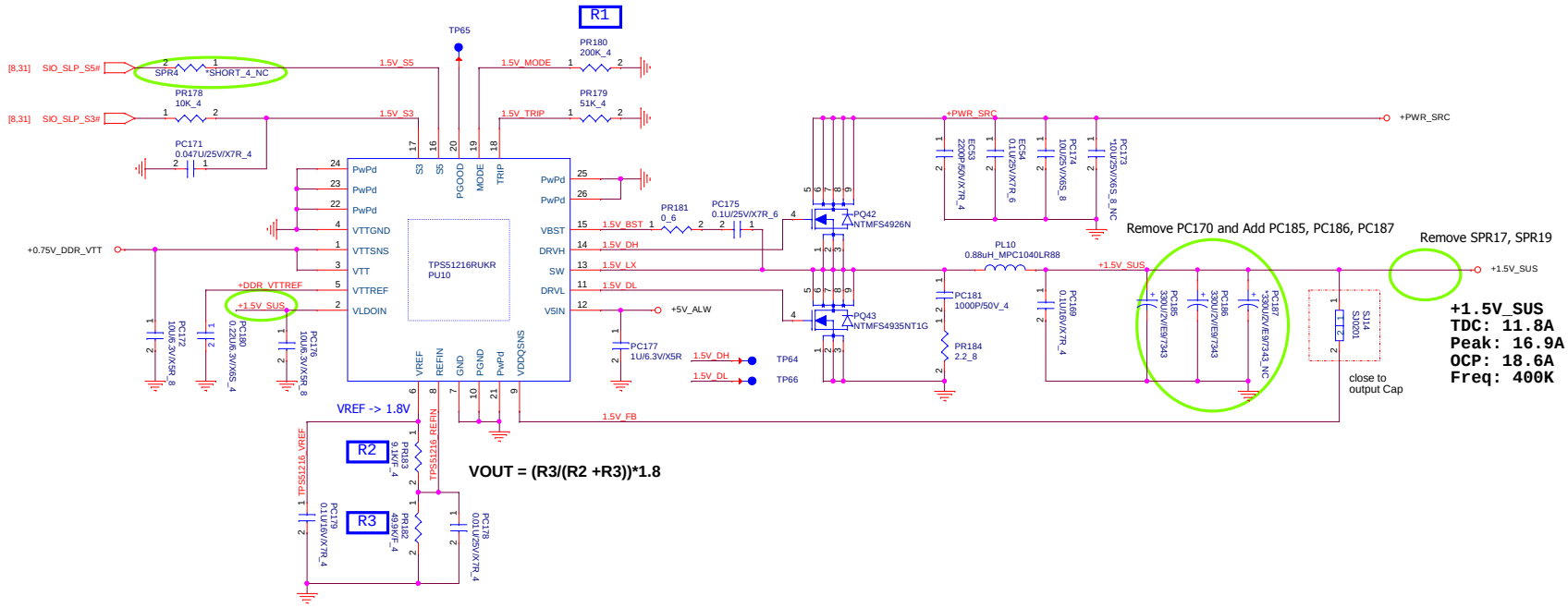
Register Address	Register Name	
0x12H	ChargeOption()	<default>
0x14H	ChargeCurrent()	
0x15H	ChargeVoltage()	
0x3FH	InputCurrent()	
0xFEH	ManufacturerID()	
0xFFH	DeviceID()	

Quanta Computer Inc.
PROJECT : R0AA

Size	Document Number	Rev
	Charger	B
Date:	Sheet 40 of 55	



Quanta Computer Inc.			
PROJECT : R0AA			
Size	Document Number		Rev
	Run Power Switch / +2.5V		B
Date:		Sheet 41 of 55	



Outputs Management by S3, S5 control

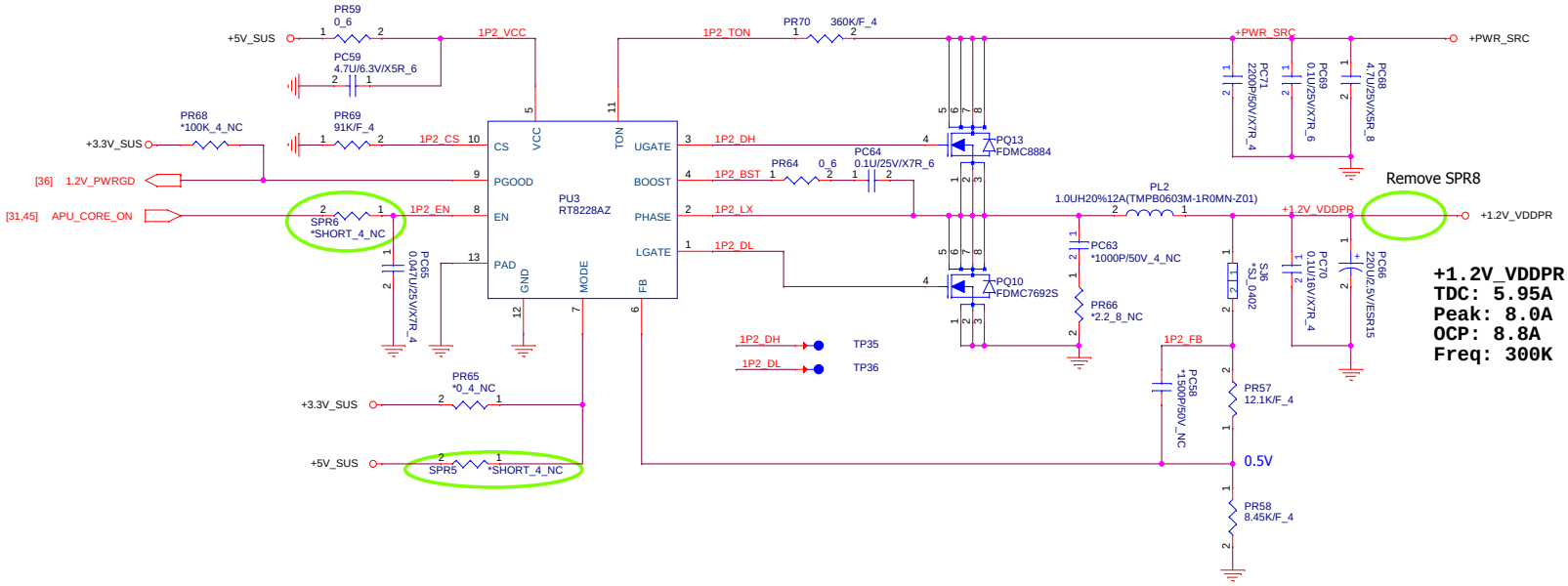
State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	Off (discharge)	Off (discharge)	Off (discharge)

MODE Selection				
	Resistance between MODE and GND		Frequency	Discharge Mode
R1	200K_4	CS42002JB14	400k Hz	Tracking Discharge
R1	100K_4	CS41002JB20	300k Hz	
R1	68K_4	CS36802JB12	300k Hz	Non-tracking Discharge
R1	47K_4	CS34702JB21	400k Hz	

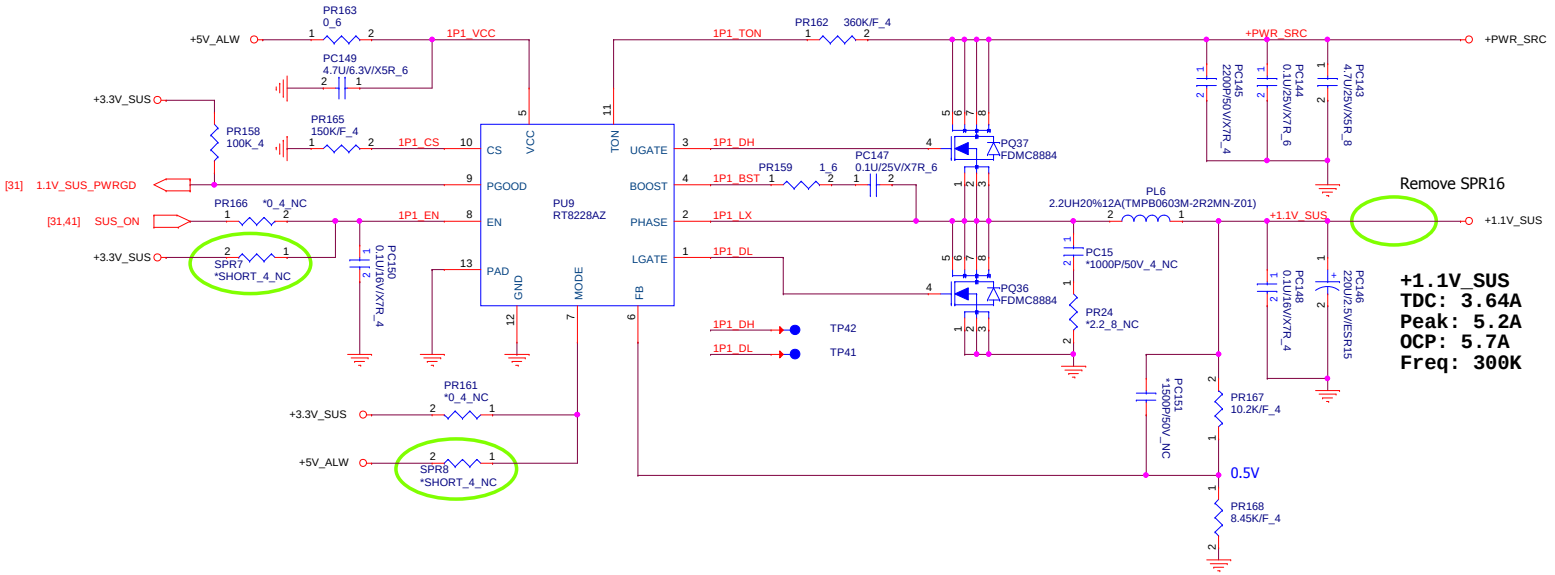
Quanta Computer Inc.
PROJECT : R0AA

Size	Document Number	Rev
	+1.5V_DDR/0.75V(TPS51216)	B

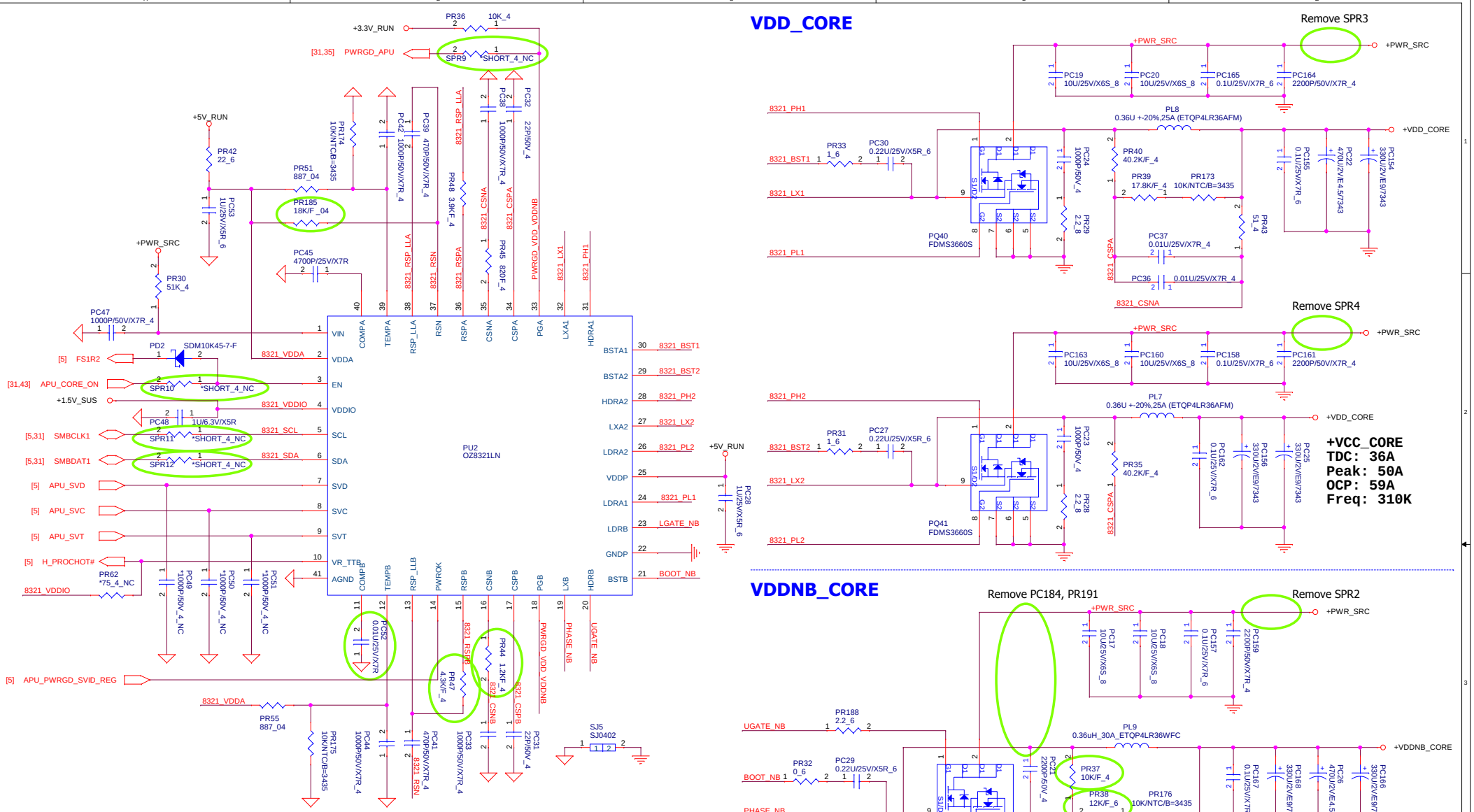
Date: Sheet 42 of 55



Quanta Computer Inc.		
PROJECT : R0AA		
Size	Document Number: +1.2V_VDDPR(RT8228AZ)	Rev: B
Date:	Sheet 43 of 55	

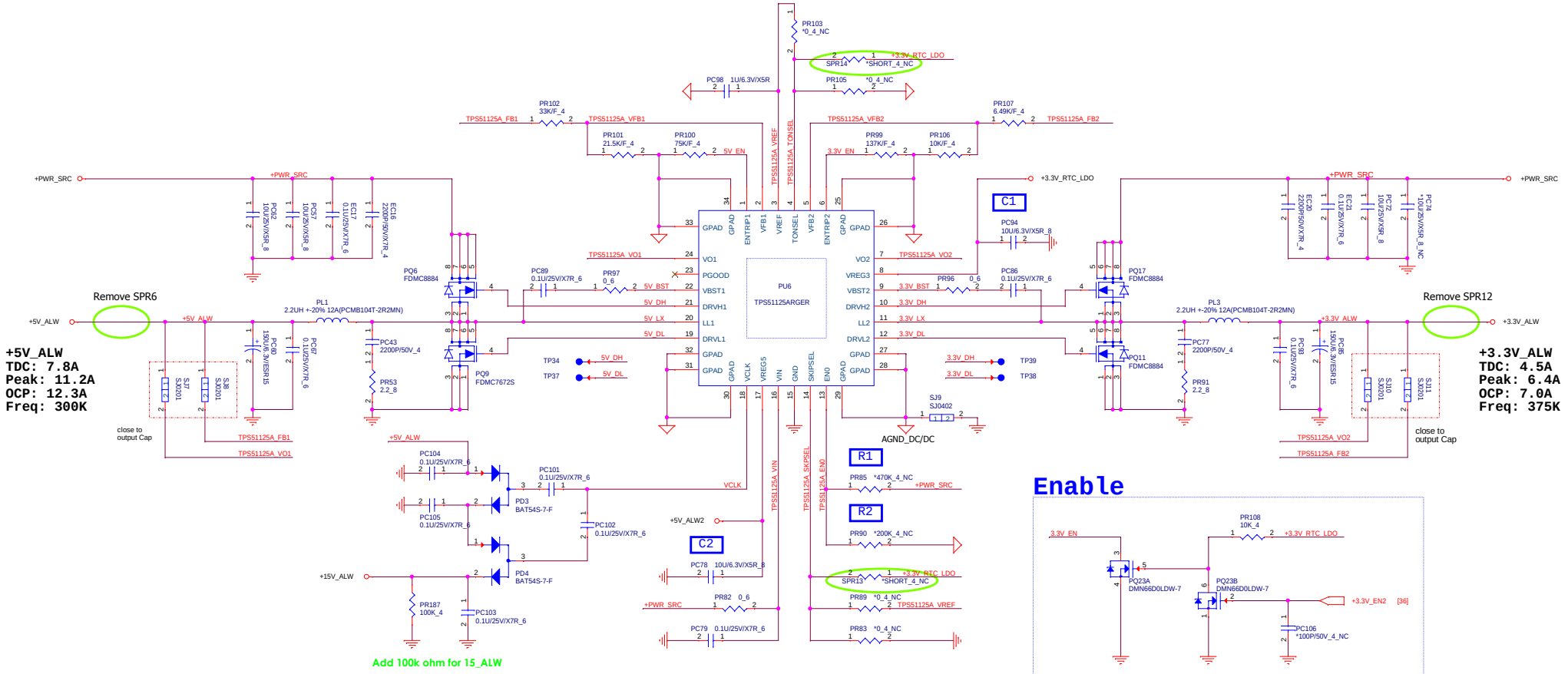


Quanta Computer Inc.		
PROJECT : R0AA		
Size	Document Number: +1.1V_SUS(RT8228AZ)	Rev: B
Date:	Sheet 44 of 55	



Register Name		Default Value		Address (HEX)	Notes
		Value	Hex	i2C R/W	
Initial_offset	RailA	0V	00H	A1H	Default
	RailB	0V	00H	E1H	Default
IDDSpike	RailA	64A	0FH	A3H	Default
	RailB	32A	0FH	E3H	Default
Slew rate	RailA	10mV/us	03H	A4H	Default
	RailB	10mV/us	03H	E4H	Default
Special offset	RailA	0V	00H	A8H	Default
	RailB	0V	00H	E8H	Default
Temp_max	RailA	100C	01H	A6H	Default
	RailB	100C	01H	or E6H	Default
Freq	RailA	3.06usV	12H	A5H	Setting by EC
	RailB	3.06usV	12H	or E5H	Setting by EC

Quanta Computer Inc.
PROJECT : R0AA
Size: Document Number: +VDD_CORE(OZ8321_LN) Rev: B
Date: Sheet 45 of 55

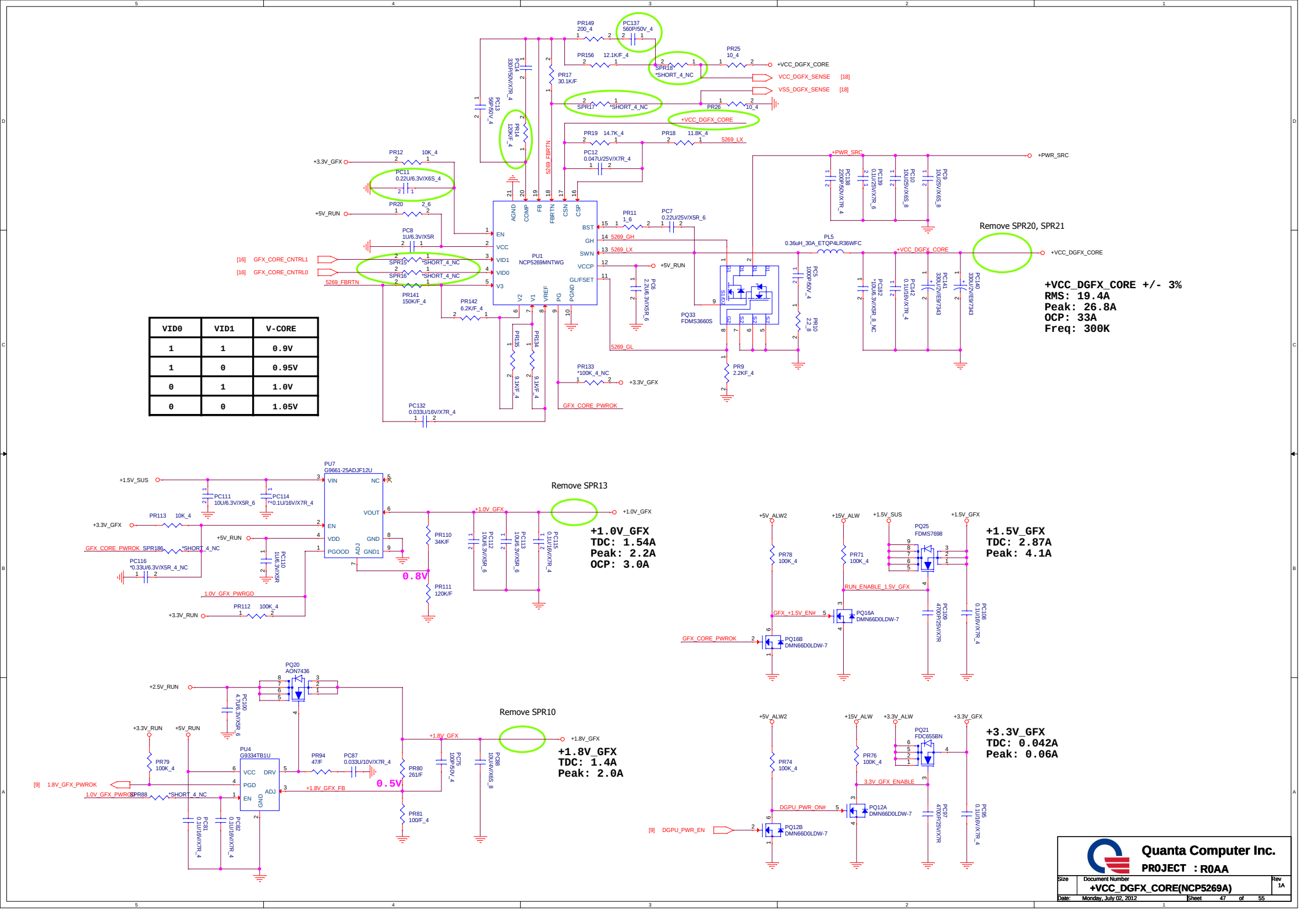


TPS51125A and RT8205N components differentia table					
	TPS51125A	AL051125002		RT8205N	P/N not ready
R1	NC	N/A	R1	470K	CS44702JB15
R2	NC	N/A	R2	200K	CS42002JB14
R3	0_6	CS00003J951	R3	0_6	N/A
C1	10uF/6.3V_8	CH61001KA94	C1	4.7uF/6.3V_8	CH5471K1A00
C2	10uF/6.3V_8	CH61001KA94	C2	4.7uF/6.3V_8	CH5471K1A00
Q1	DDTA114YUA	N/A	Q1	DDTA114YUA	BA001140001
Q2	2N7002W-7-F	N/A	Q2	2N7002W-7-F	BAM70020040

TPS51125A TONSEL Connection and Switching Frequency				
Ton	REG5	REG3	VREF	GND
Channel1 Fs	365 kHz	300 kHz	245 kHz	200 kHz
Channel2 Fs	460 kHz	375 kHz	305 kHz	250 kHz

Quanta Computer Inc.
PROJECT : R0AA

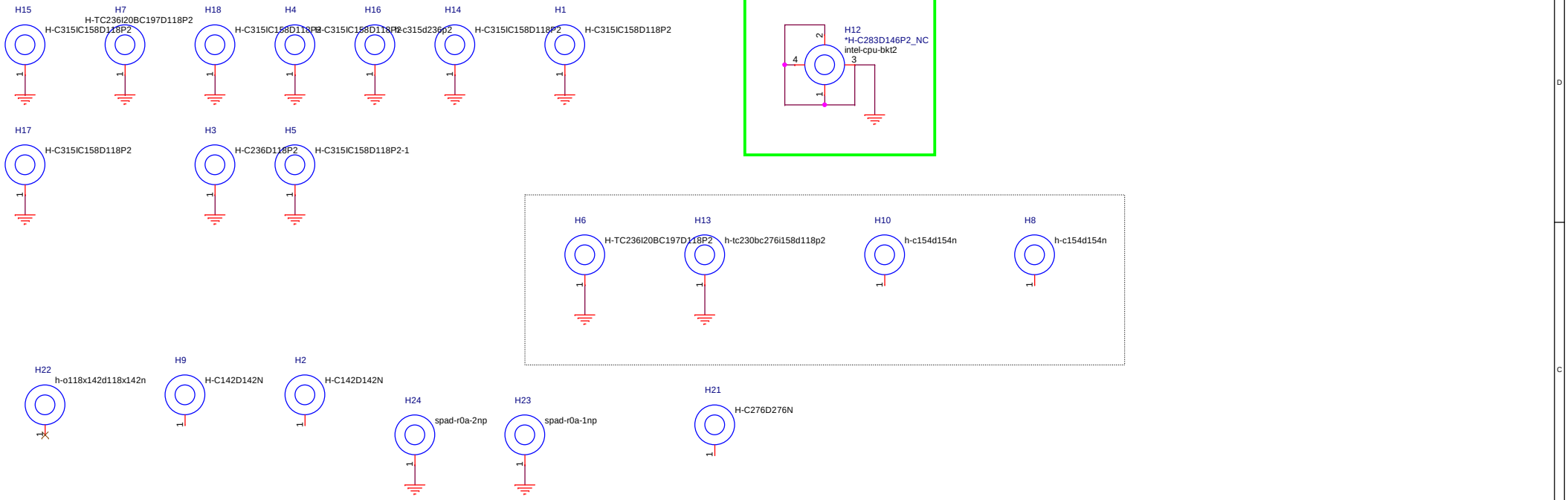
Size	Document Number	Rev
	+3.3V_ALW /+ 5V_ALW (TPS51125ARGER)	B
Date: Monday, July 02, 2012	Sheet 46 of 55	



VID0	VID1	V-CORE
1	1	0.9V
1	0	0.95V
0	1	1.0V
0	0	1.05V

Quanta Computer Inc.
PROJECT : R0AA

Size	Document Number	Rev
	+VCC_DGFX_CORE(NCP5269A)	1A
Date: Monday, July 02, 2012	Sheet 47 of 55	



Quanta Computer Inc.

PROJECT : R02

Size	Document Number	Rev
	SCREW PAD	B

Date: Monday, June 25, 2012 Sheet 48 of 55