

Compal Confidential

KIUN0 Schematics Document

Intel Diamondville Processor with Calistoga(945GSE) + DDRII + ICH7M

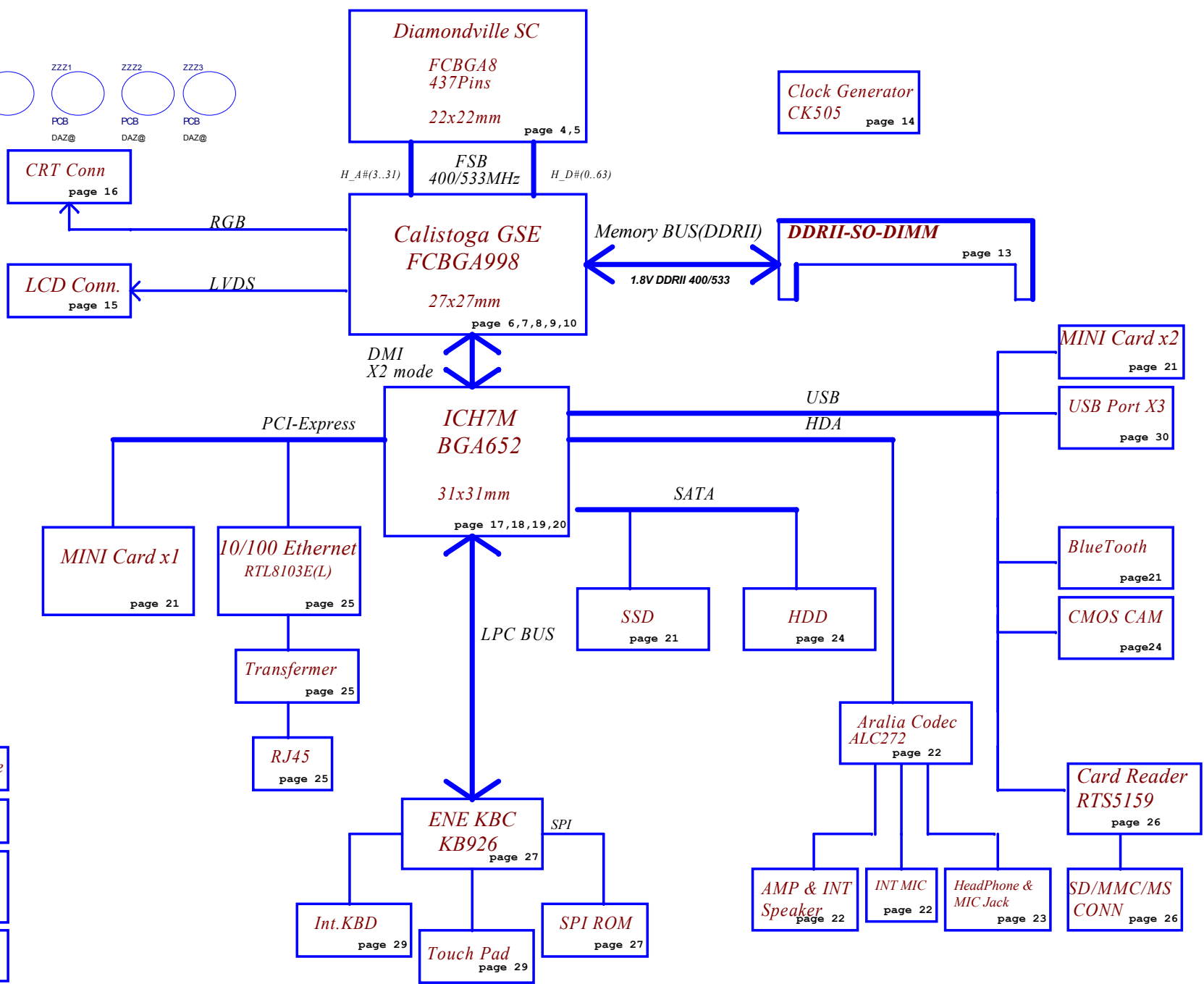
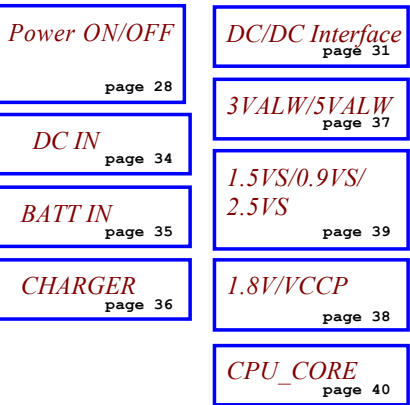
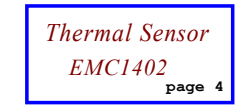
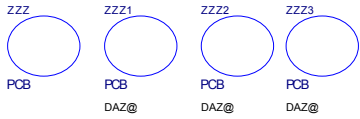
2009-03-31

REV: 1.0

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Model Name : KIUN0
File Name : LA-5071P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+VCCP	VCCP switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SIGNAL						
		SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	ClOCK
Full ON		HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table(Page 25)

ID	BRD ID	Ra	Rb	Vab
0	R01 (EVT)	NC	0	0V
1	R02 (DVT)	100K	8.2K	0.25V
2	R03 (PVT)	100K	18K	0.50V
3	R10A (MP)	100K	NC	3.3V

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
--------	---------	-----------	------

No PCI Device

EC SM Bus1 address

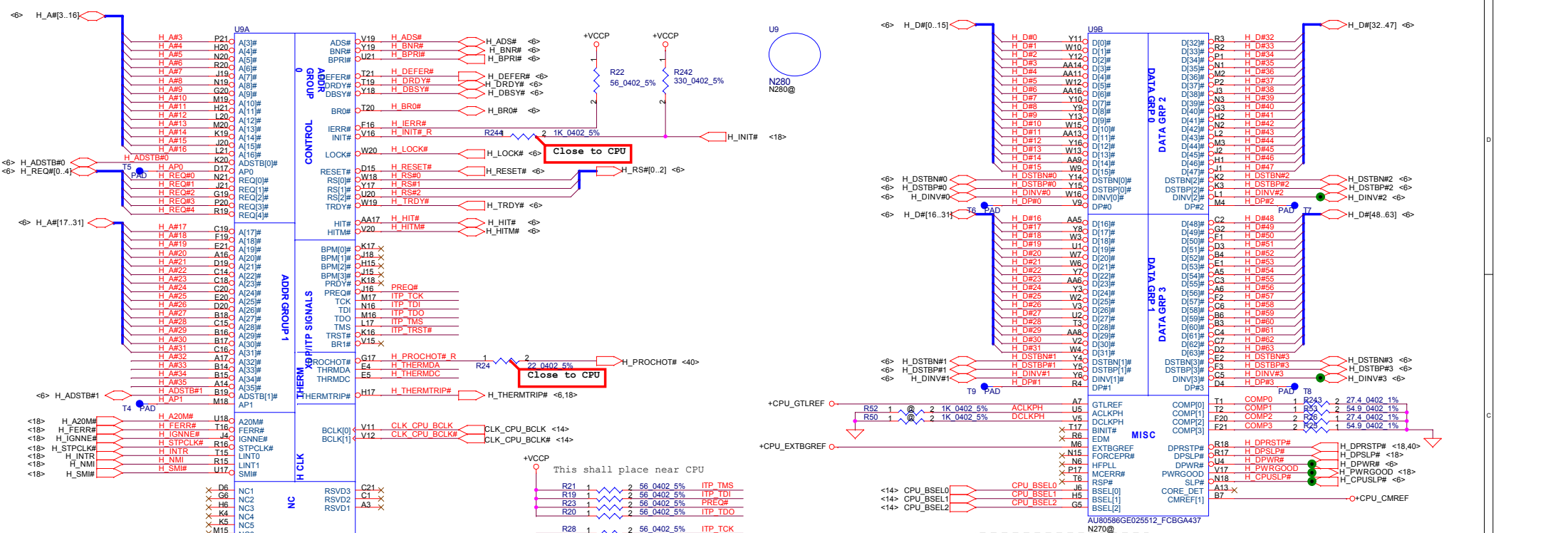
EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	EMC1402	100_1100

ICH7M SM Bus address

Device	Address
Clock Generator (SLG8SP556VTR)	1101 001Xb
DDR DIMMA	1010 000Xb

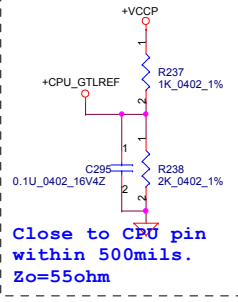
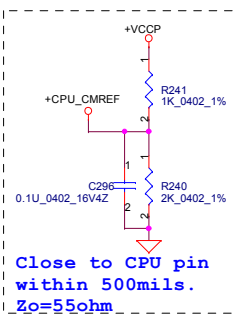
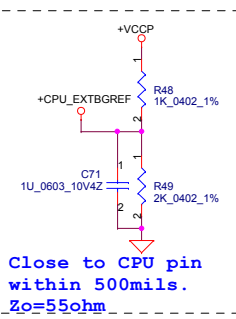
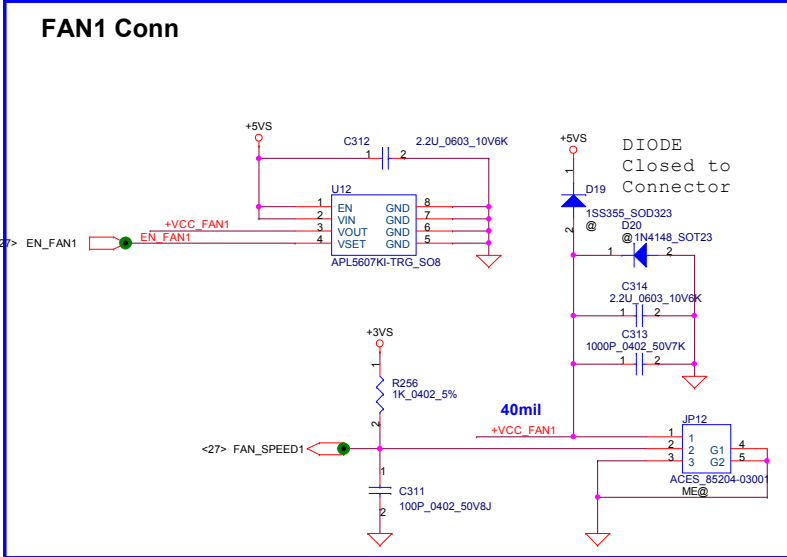
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Close to CPU

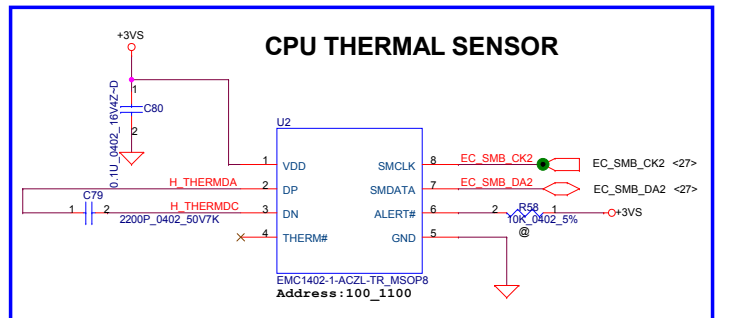
Close to CPU

This shall place near CPU

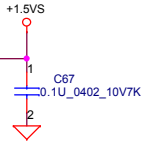
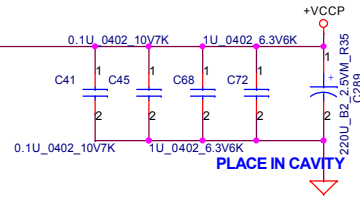
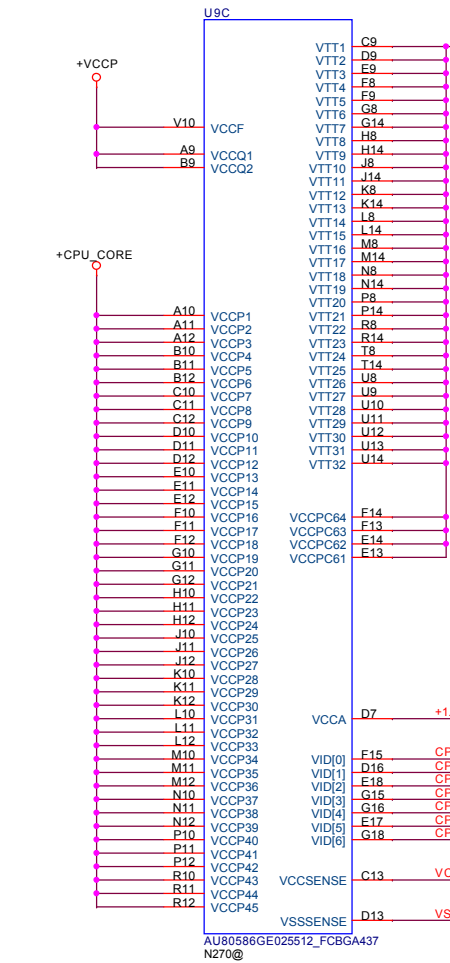
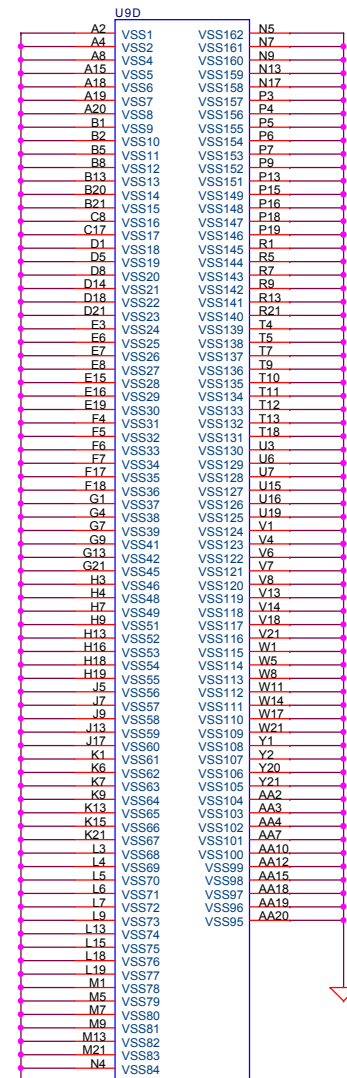


Layout note:
 COMP0,2 connect with $Z_0=27.4\text{ohm} \pm 15\%$, make trace length shorter than 0.5"
 COMP1,3 connect with $Z_0=55\text{ohm} \pm 15\%$, make trace length shorter than 0.5"

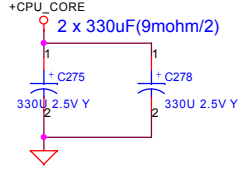
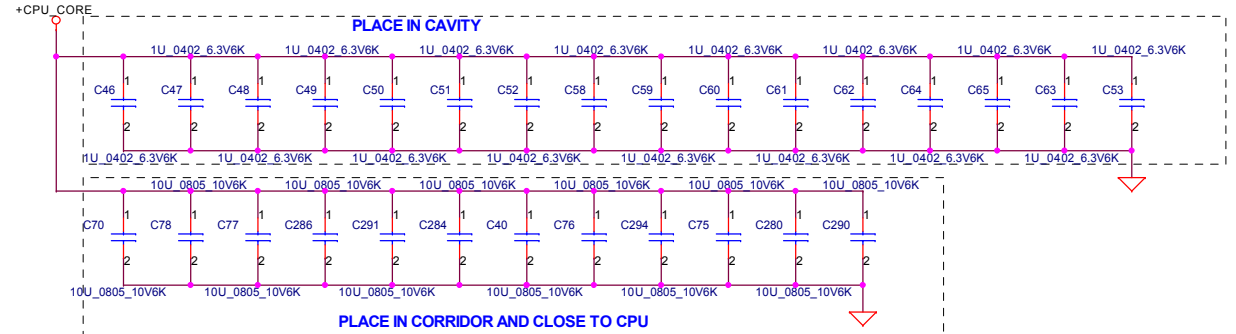
H_THERMDA, H_THERMDC routing together. Trace width / Spacing = 10 / 10 mil



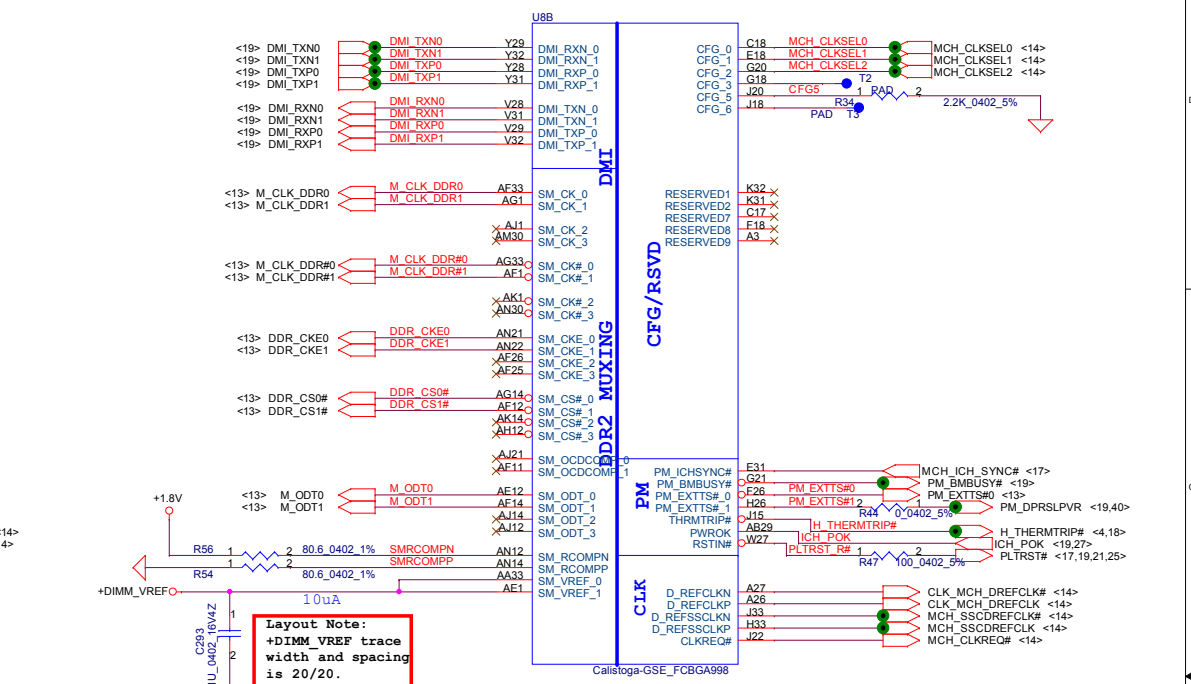
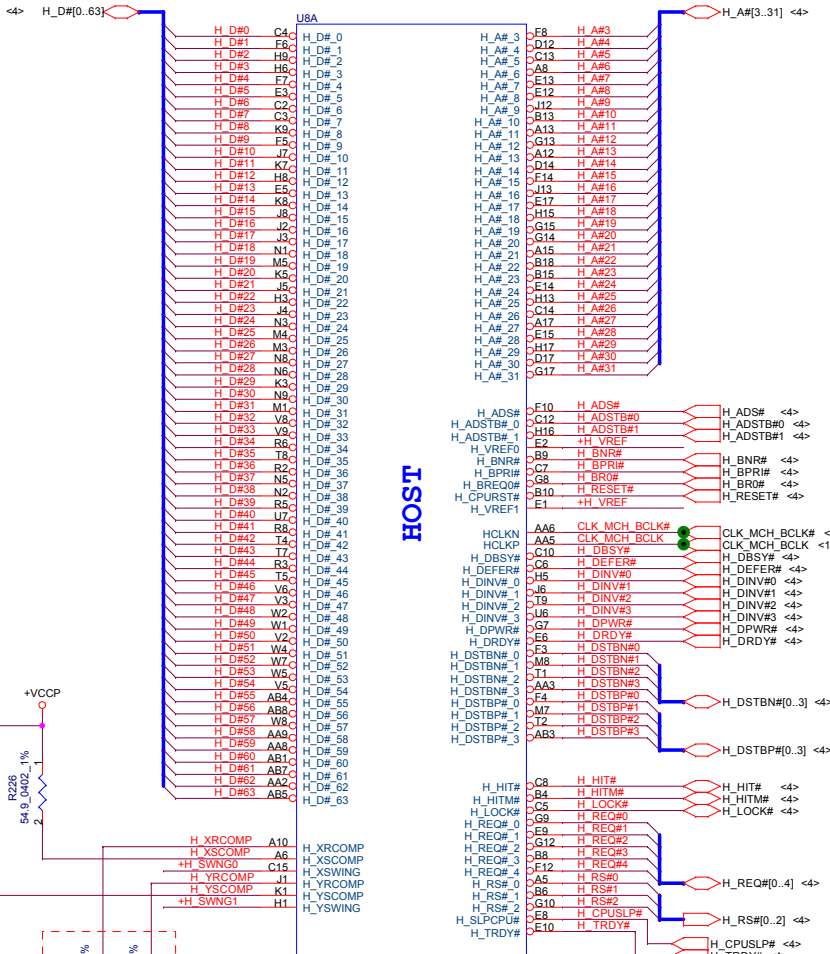
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Length match within 25 mils
The trace space 7 mils,
 $Z_0=27.4\text{ohm}$



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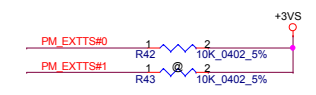
Layout Note:
+DIMM_VREF trace width and spacing is 20/20.

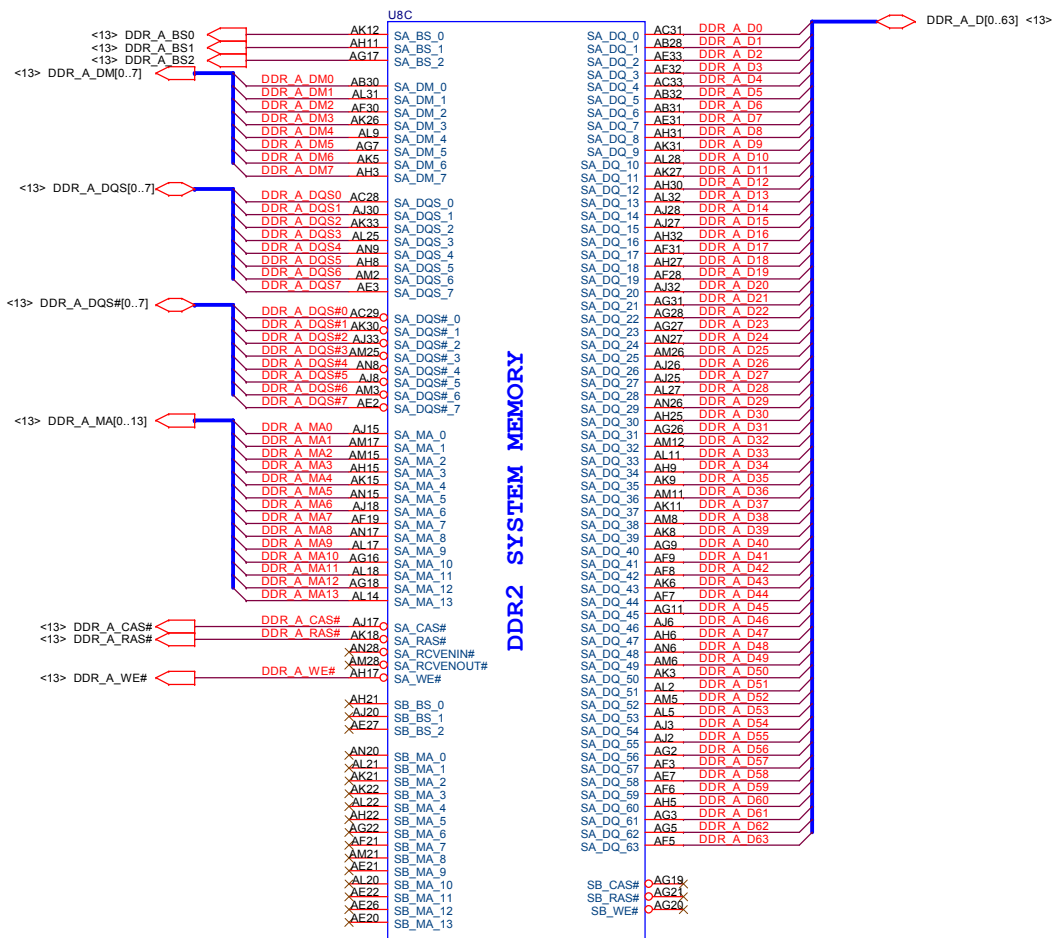
Strap Pin Table

CFG5	Low = DMI x 2 *
	High = DMI x 4

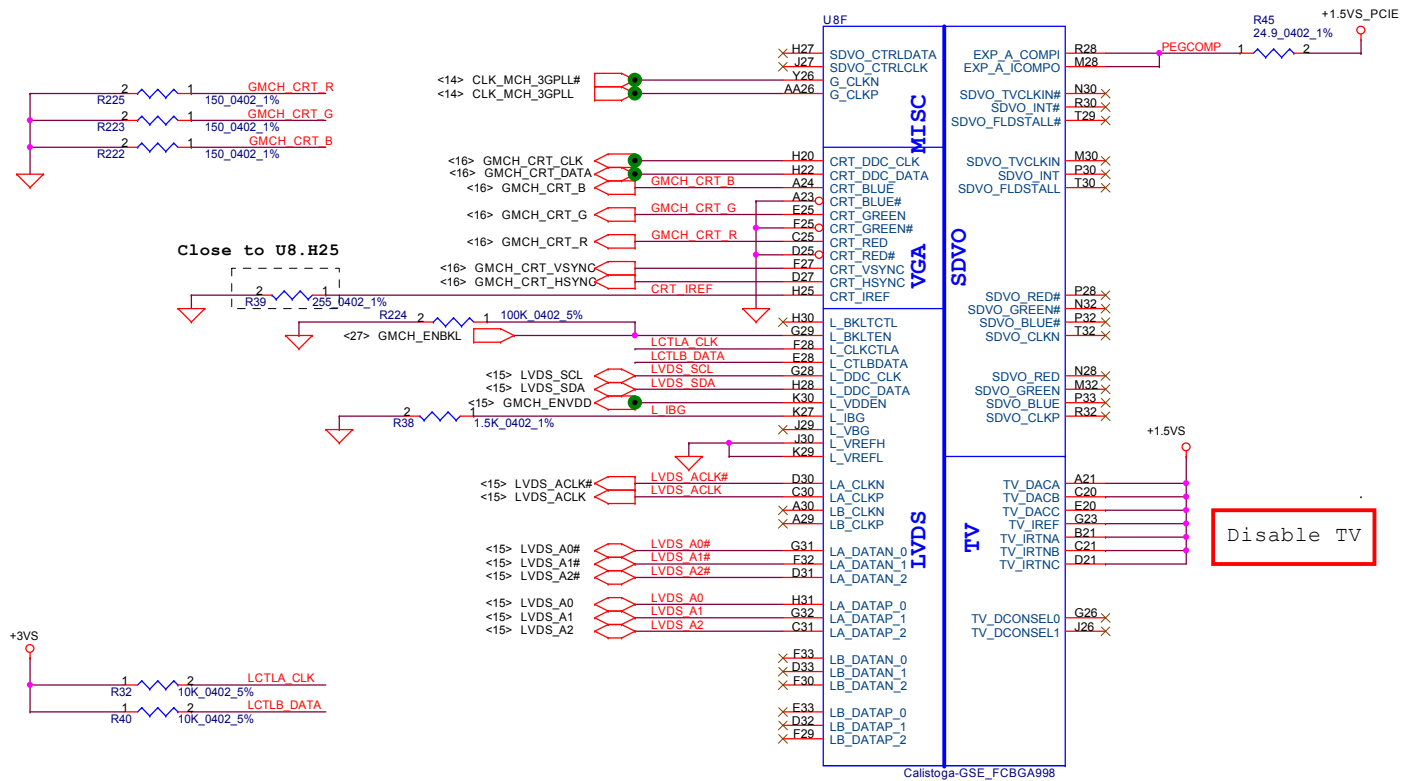
Layout Note:
H_XRCOMP / H_YRCOMP / H_VREF / H_SWNG0 / H_SWNG1 trace width and spacing is 10/20.

C be placed <100mils from GMR pin

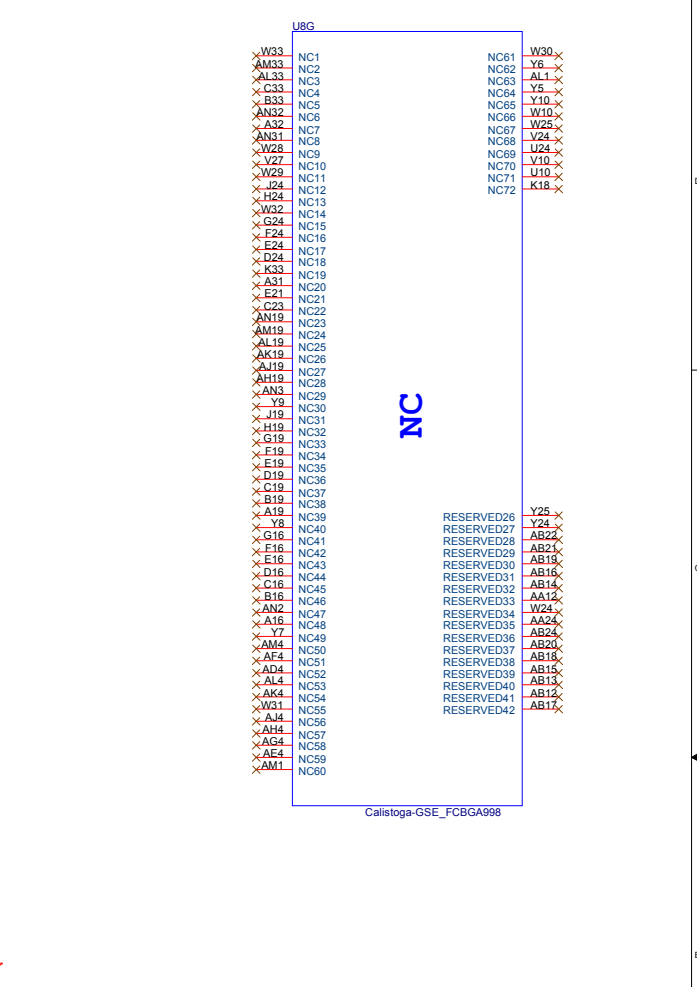
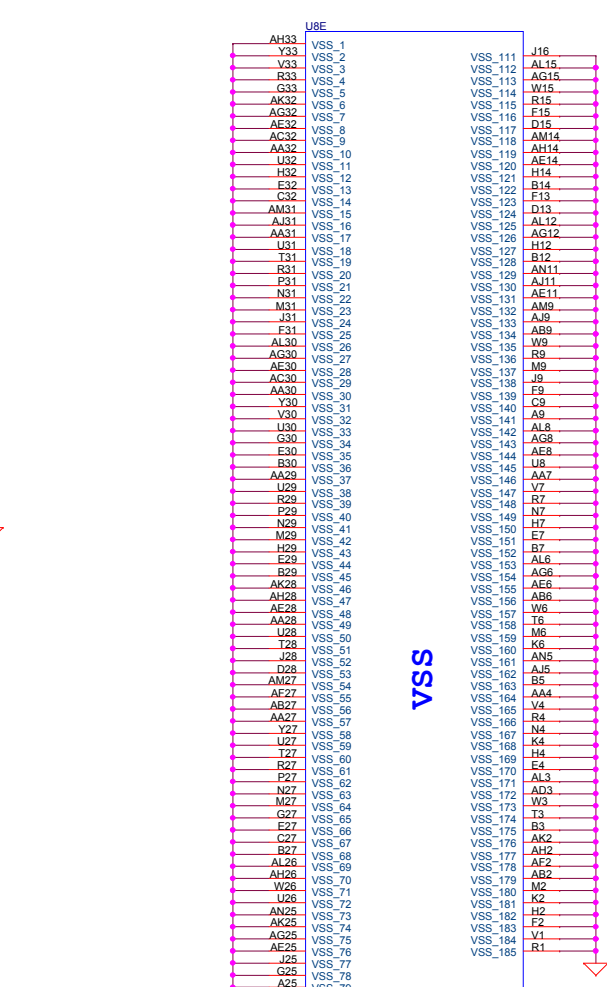
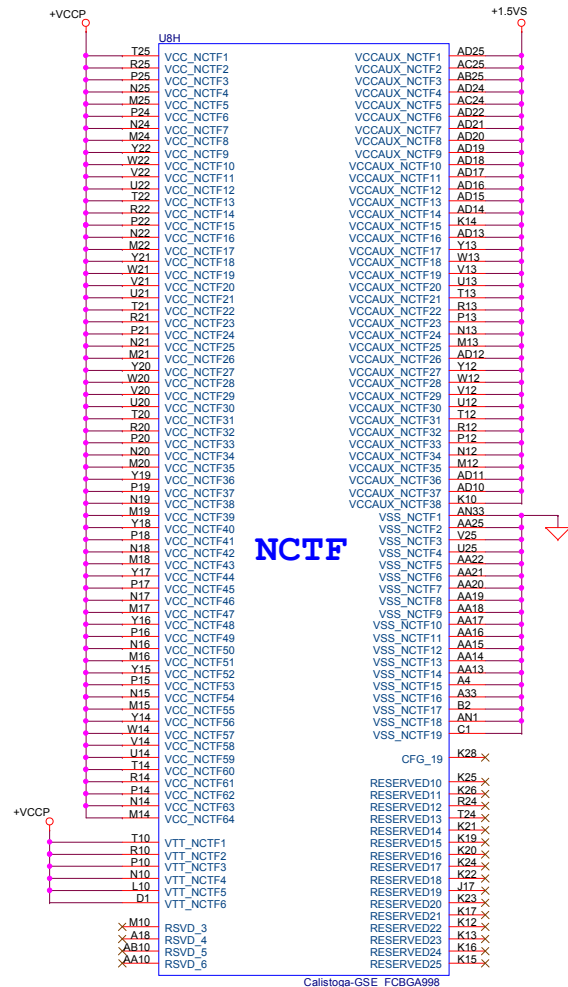




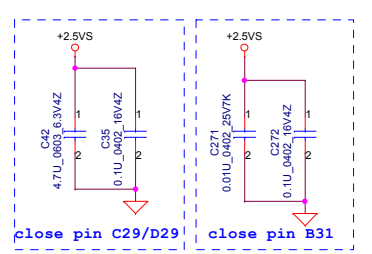
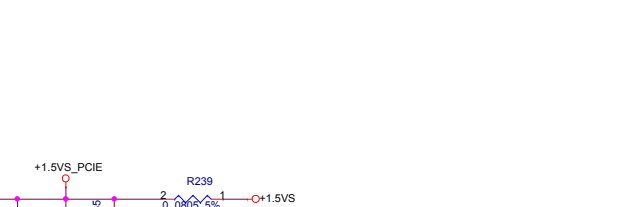
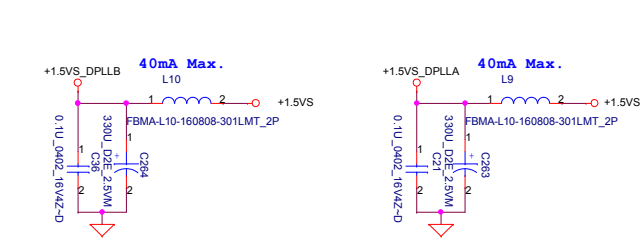
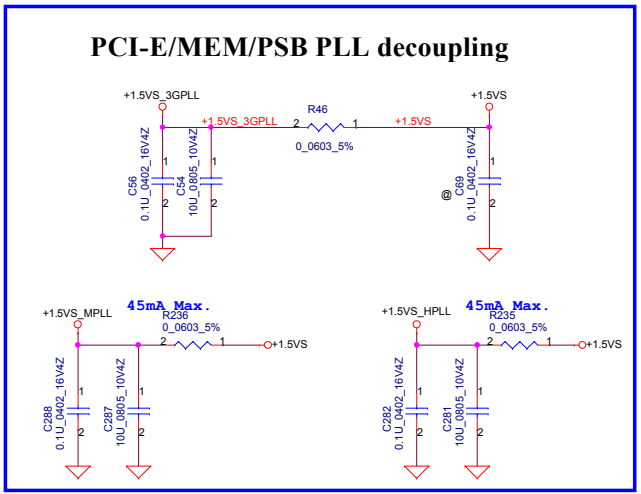
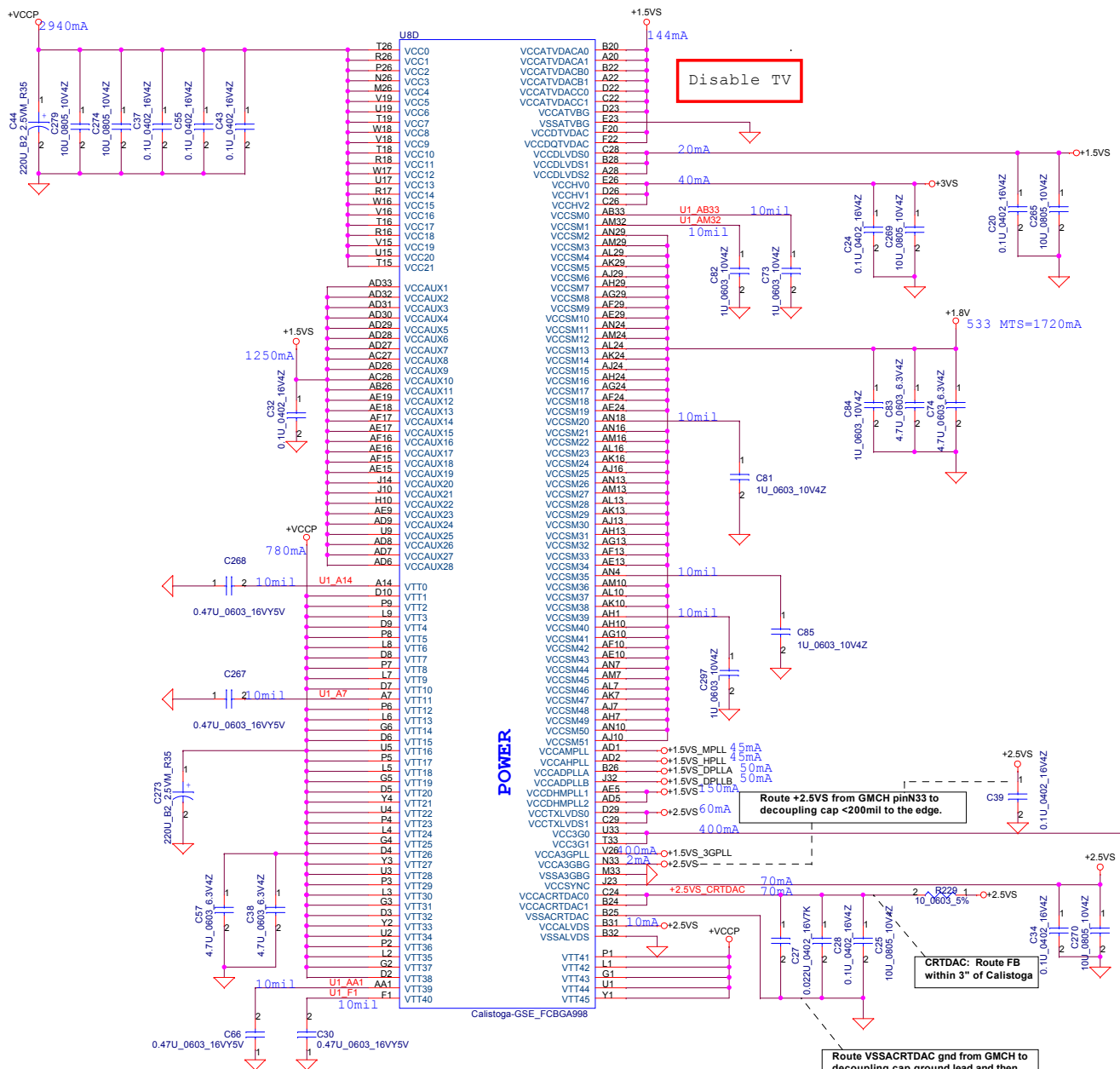
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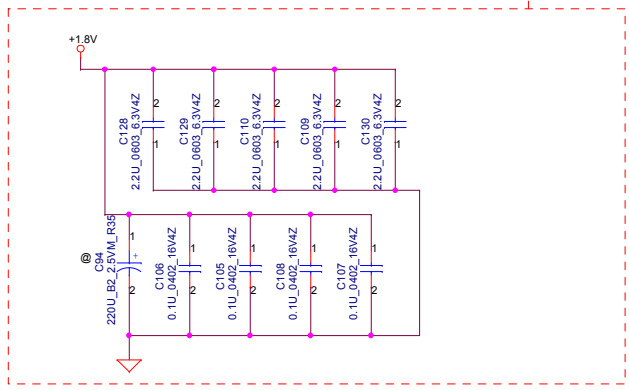
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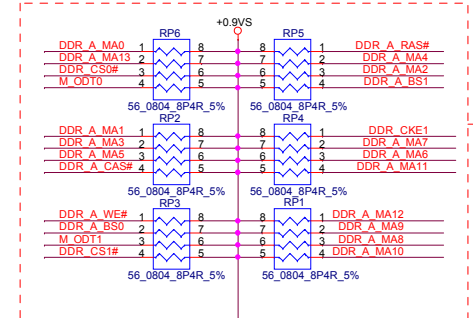
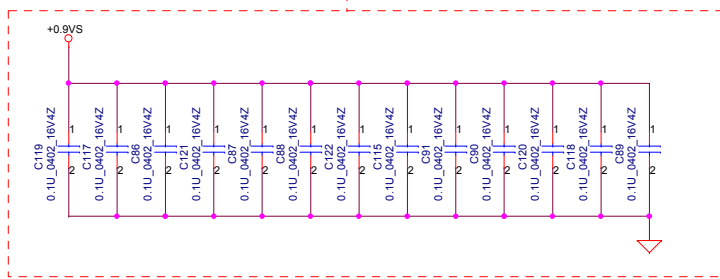
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- <7> DDR_A_DQS#[0..7]
- <7> DDR_A_D[0..63]
- <7> DDR_A_DM[0..7]
- <7> DDR_A_DQS[0..7]
- <7> DDR_A_MA[0..13]

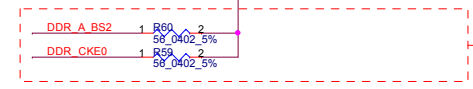
Layout Note:
Place near JDIM1



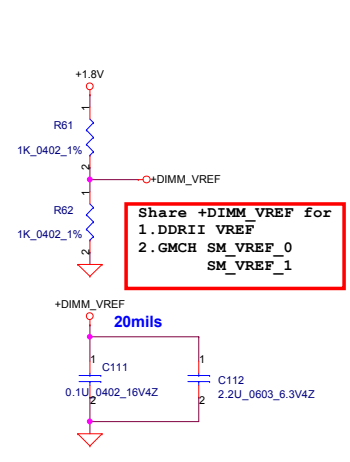
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place this resistor closely DIMMA, all trace length < 750 mil

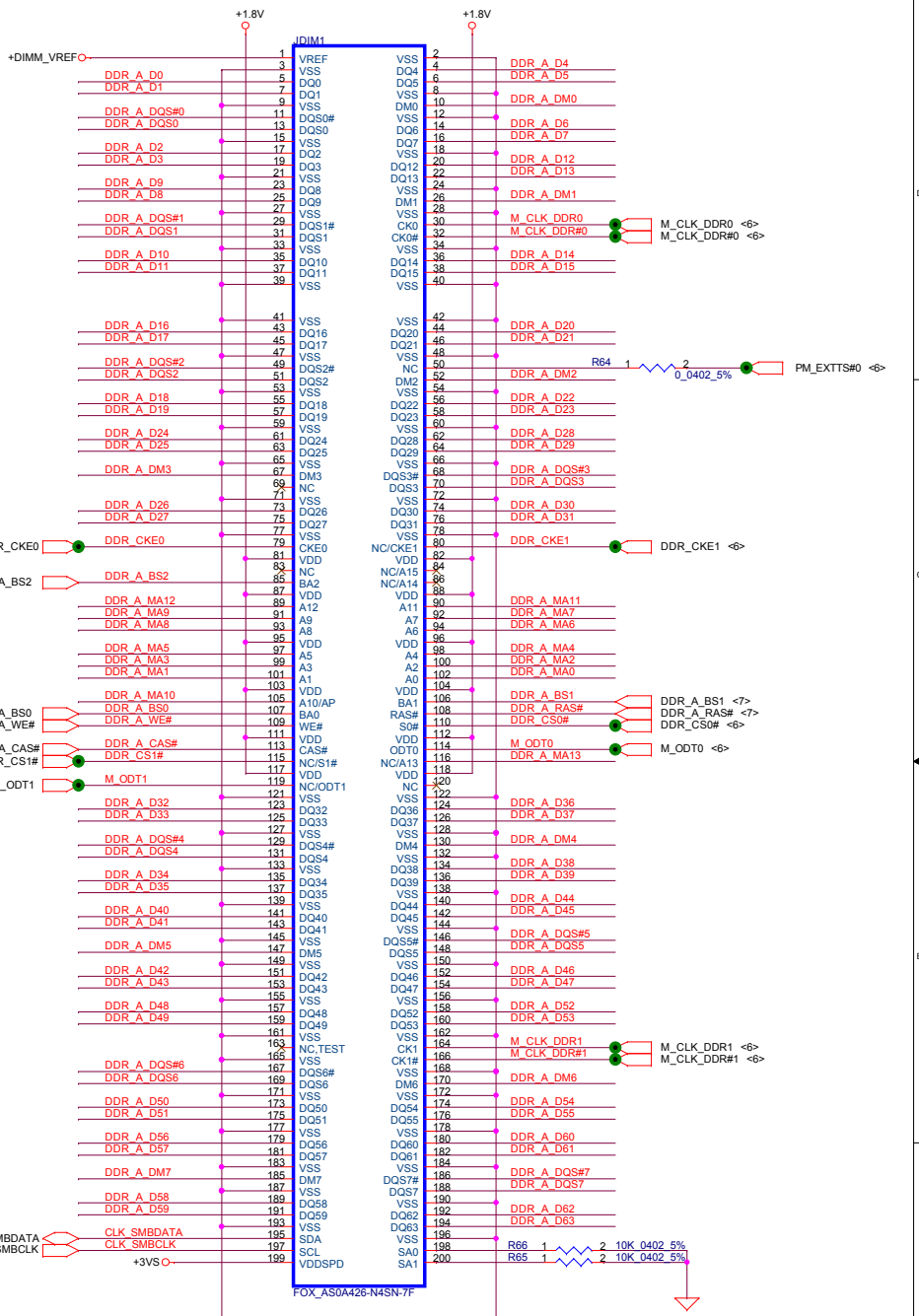
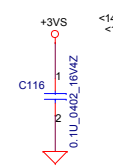


Layout Note:
Place this resistor closely DIMMA, all trace length Max=1.3"



Share +DIMM_VREF for
1. DDRII VREF
2. GMCH SM_VREF_0
SM_VREF_1

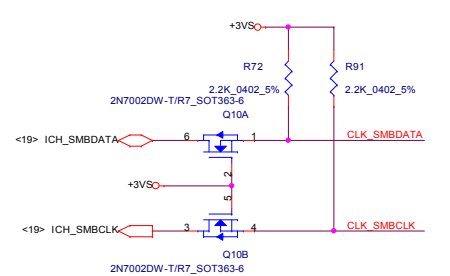
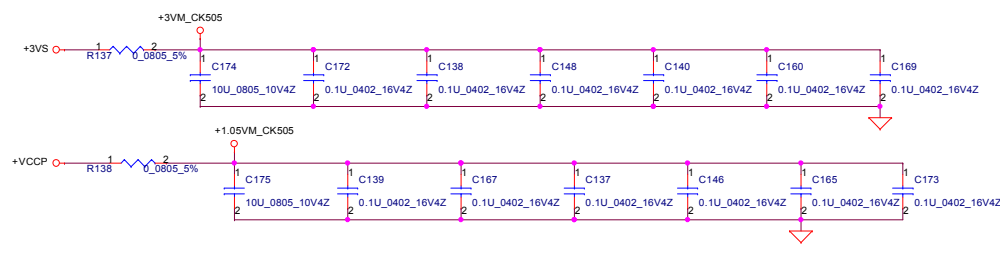
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- <7> DDR_A_BS2
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- <6> DDR_CAS#
- <6> DDR_CS1#
- <6> M_ODT1



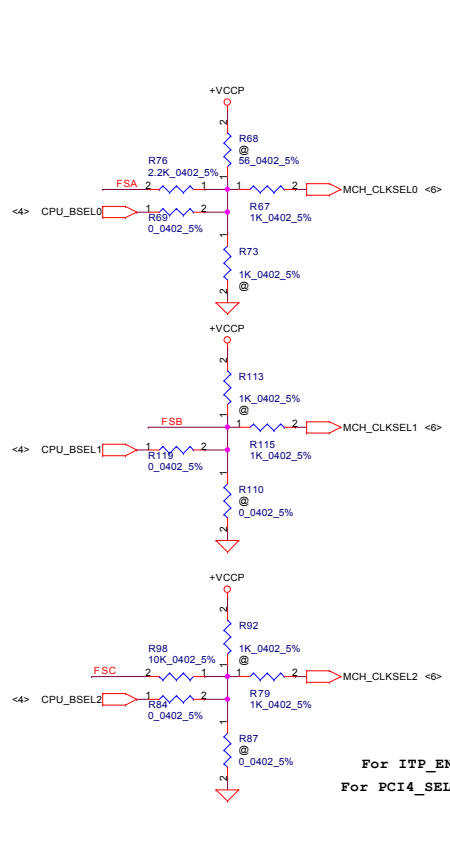
DIMMA

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FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1						
Reserved								

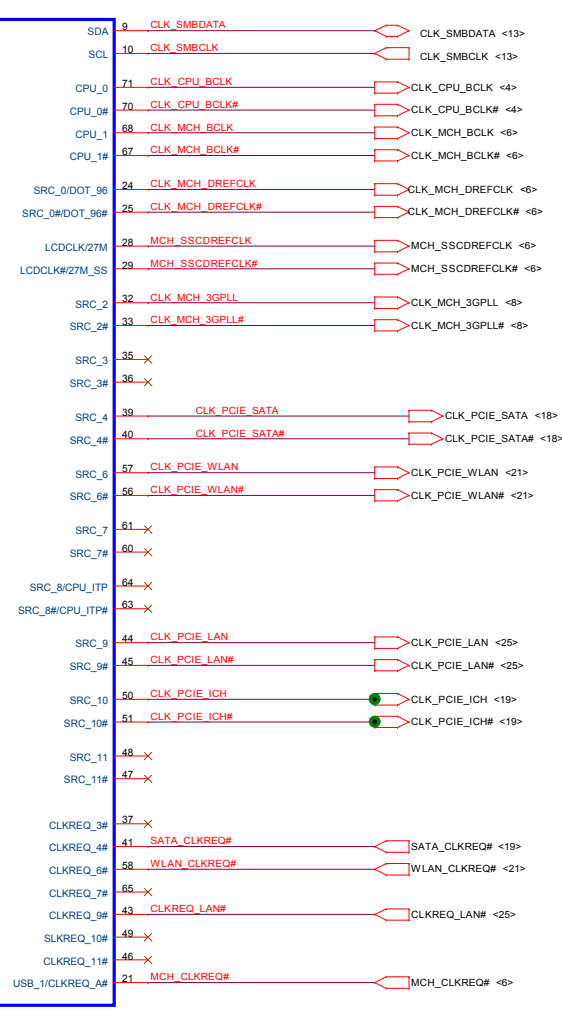
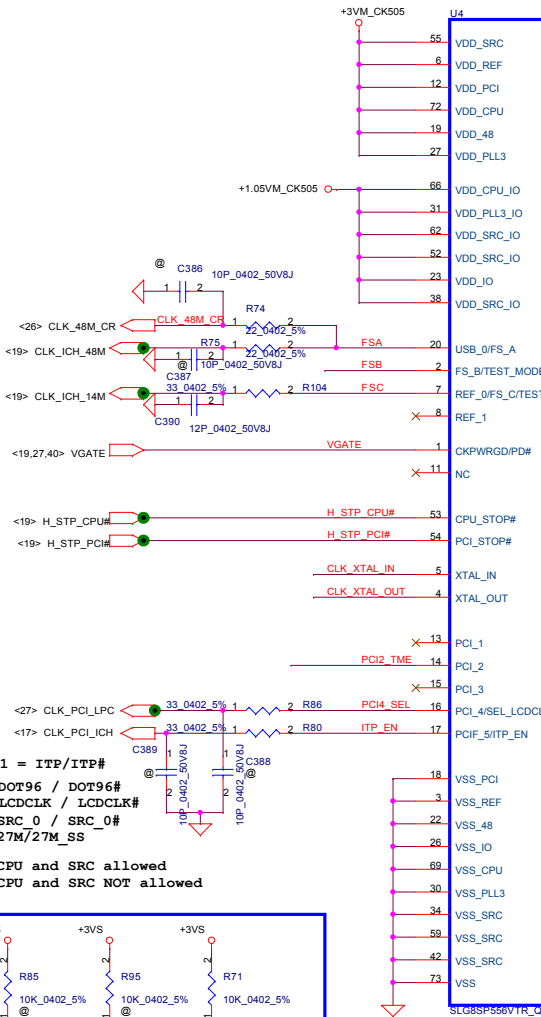


SA000020K00 (Silego : SLG8SP556VTR)
SA000020H10 (ICS : ICS9LPRS387AKLFT)



For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

For PCI2_TME=0=Overclocking of CPU and SRC allowed
(ICS only) 1=Overclocking of CPU and SRC NOT allowed

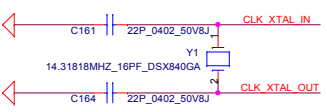


SRC PORT LIST

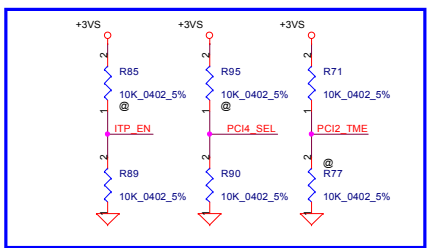
PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	
SRC4	PCIE SATA
SRC6	PCIE WLAN
SRC7	
SRC8	
SRC9	PCIE LAN
SRC10	PCIE ICH
SRC11	

REQ PORT LIST

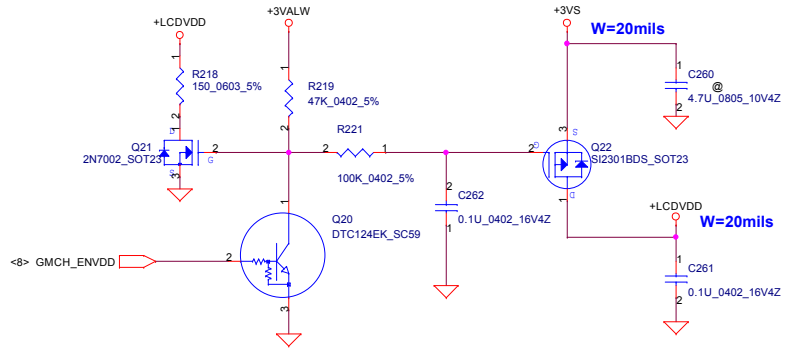
PORT	DEVICE
REQ_3#	
REQ_4#	PCIE SATA
REQ_6#	PCIE WLAN
REQ_7#	
REQ_9#	PCIE LAN
REQ_10#	
REQ_11#	
REQ_A#	MCH_3GPLL



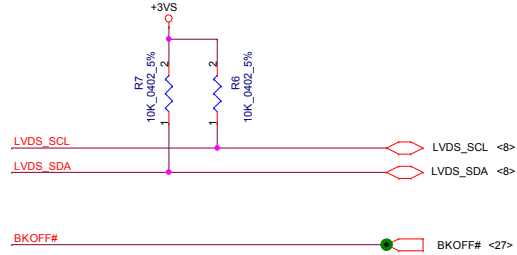
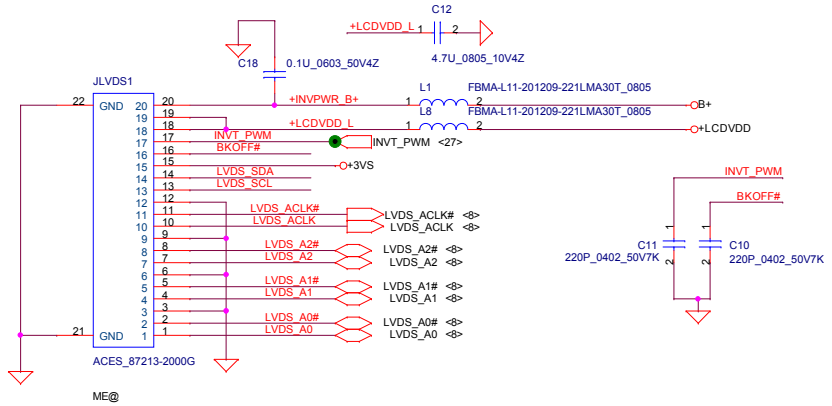
Routing the trace at least 10mil



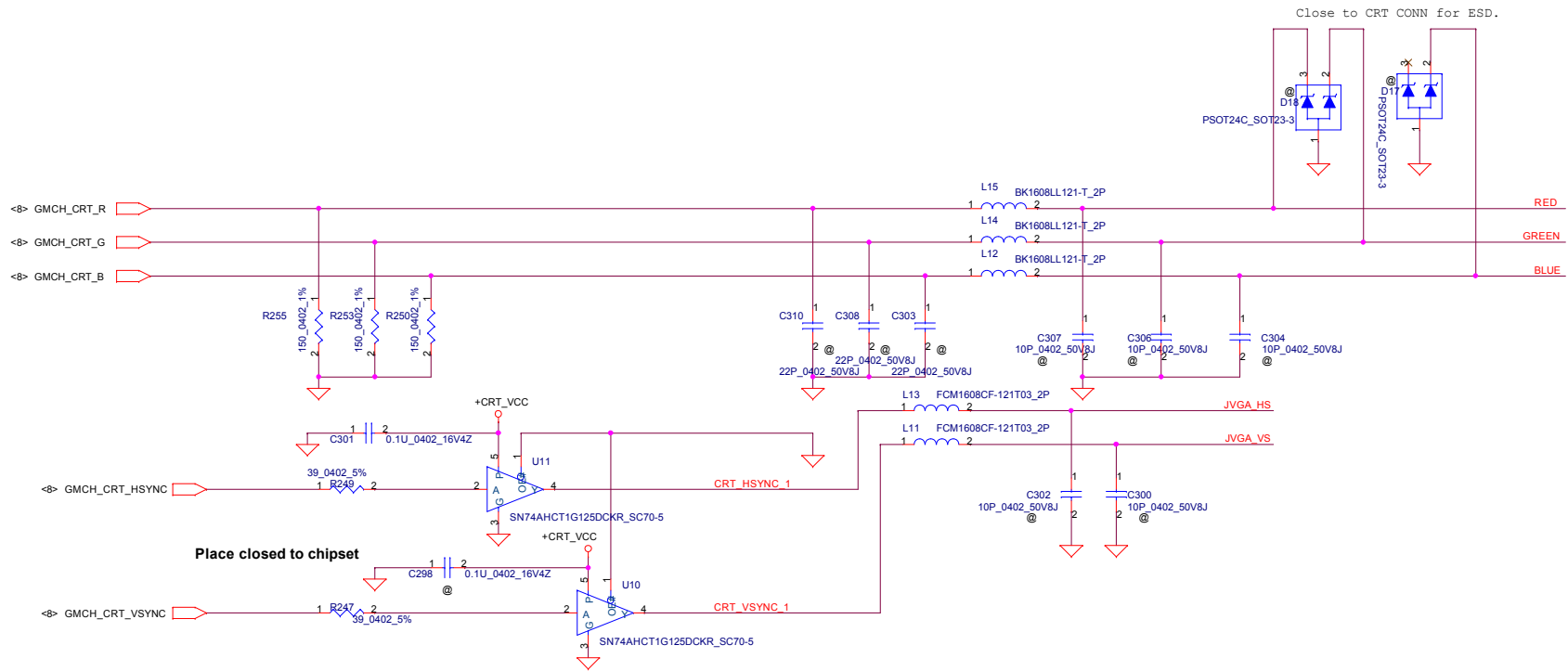
LCD POWER CIRCUIT



LCD/PANEL BD. Conn.



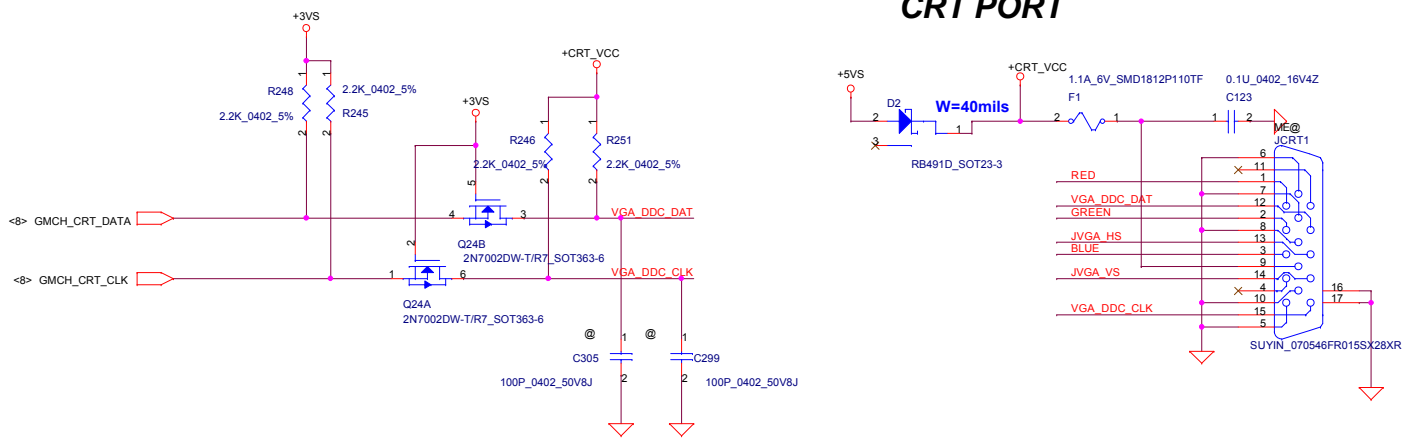
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title LVDS /INVERTER		
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Place closed to chipset

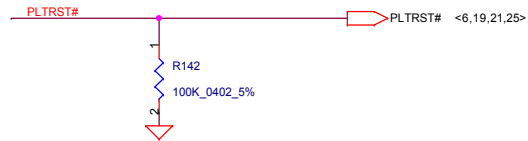
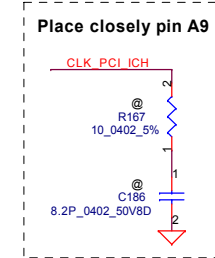
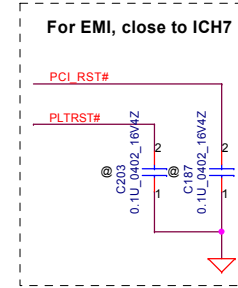
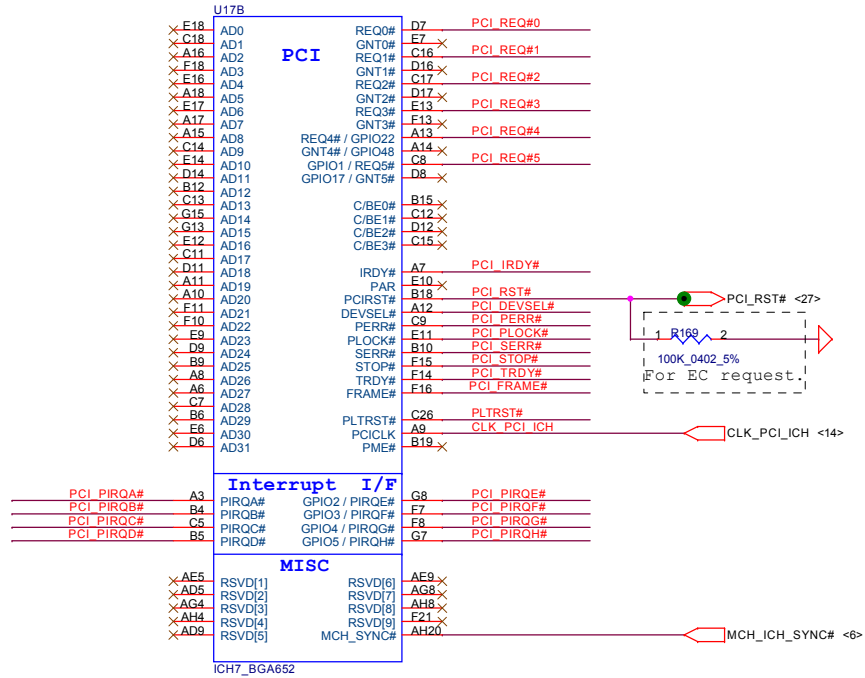
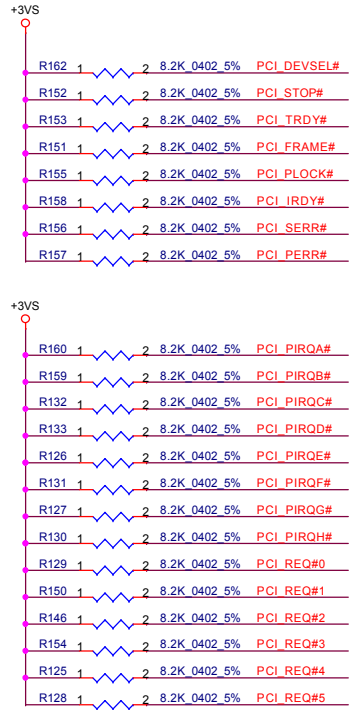
Close to CRT CONN for ESD.

CRT PORT

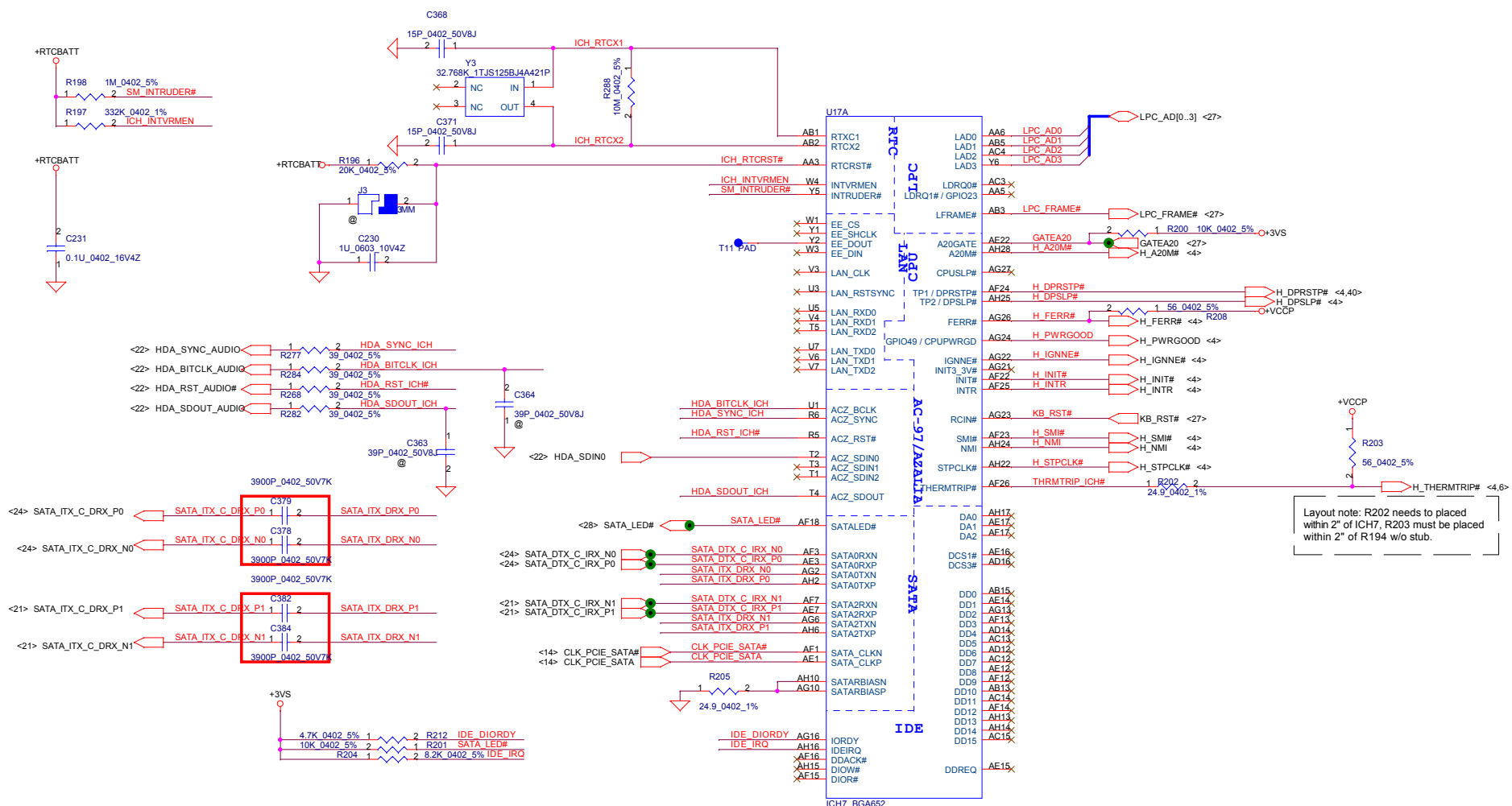


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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
				CRT PORT	
Size B	Document Number	LA-4421P		Rev	0.2
Date:	Monday, April 06, 2009	Sheet	16	of	42

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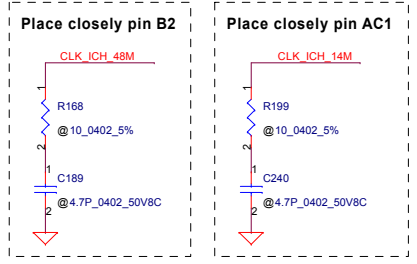
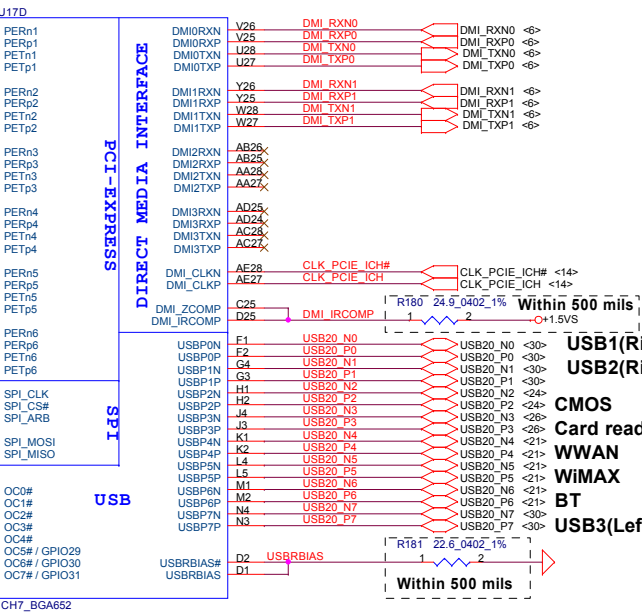
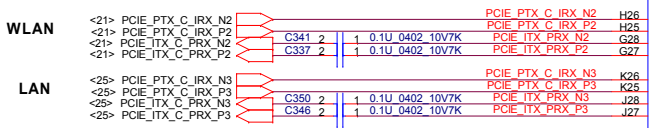
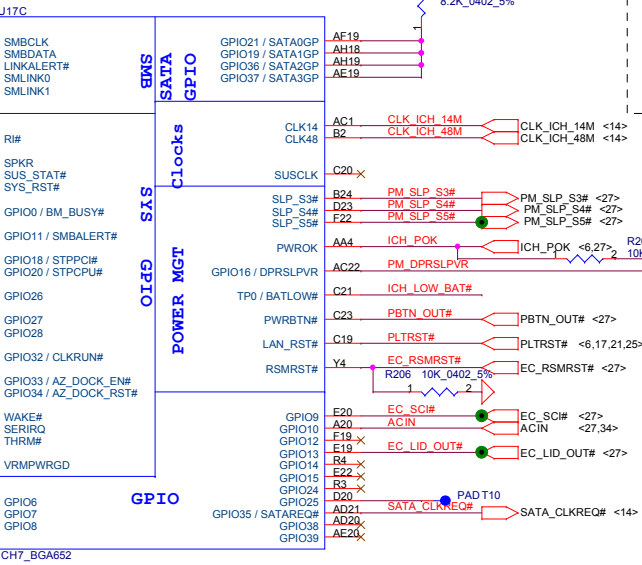
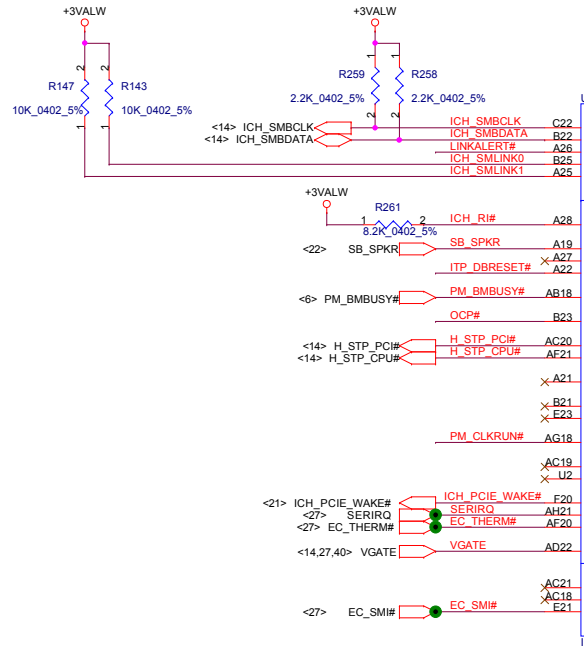
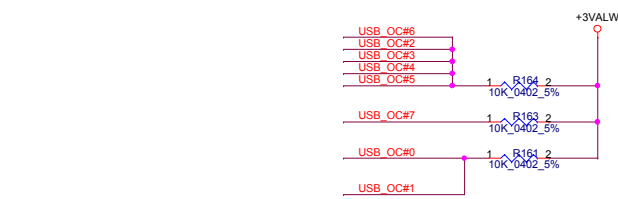
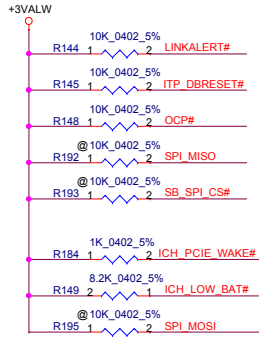
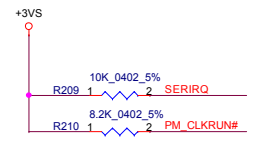


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Size	Document Number			Rev	
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Layout note: R202 needs to be placed within 2" of ICH7. R203 must be placed within 2" of R194 w/o stub.

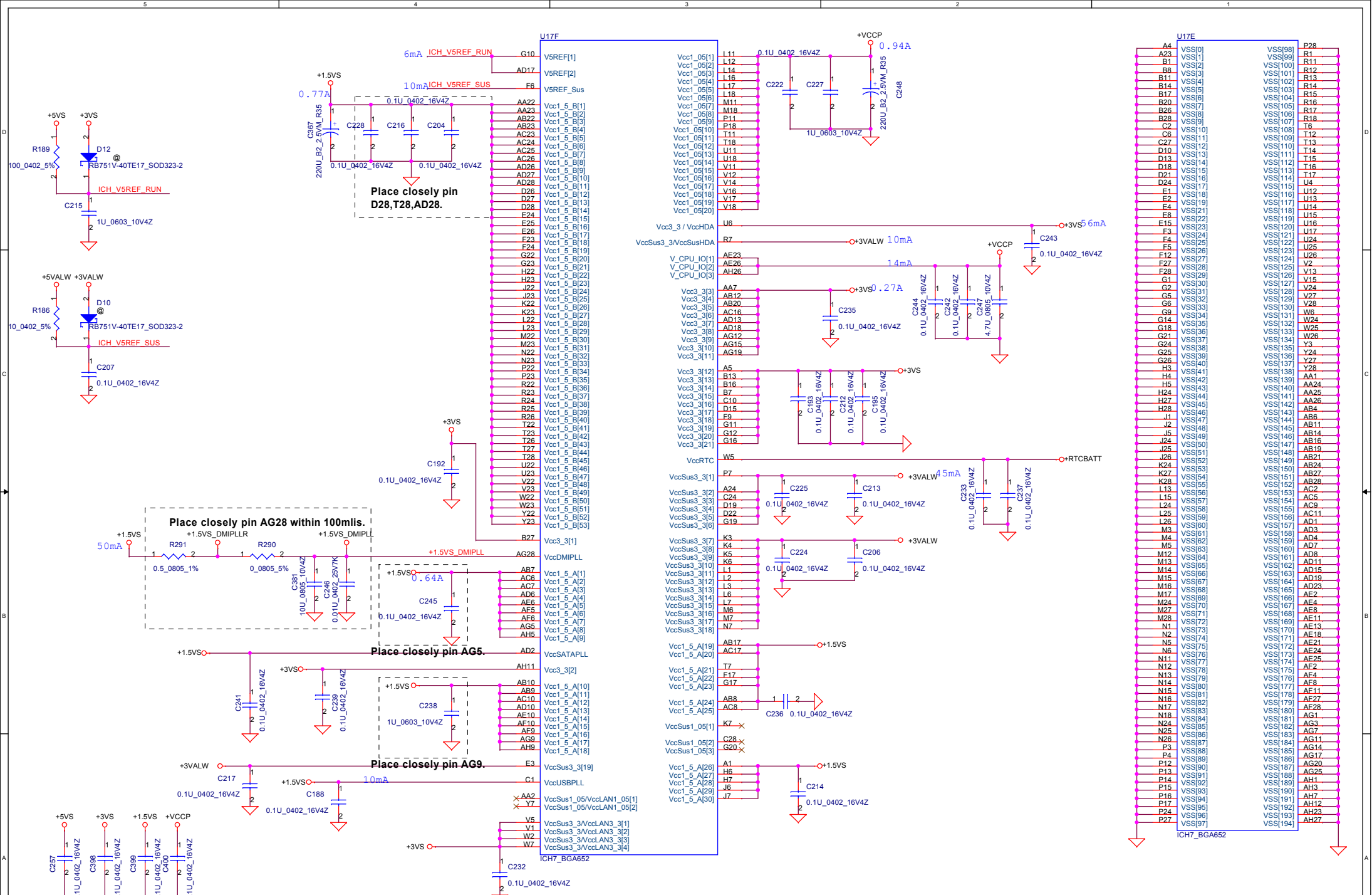
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title
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Issued Date	2006/08/18	Deciphered Date
		2007/8/18

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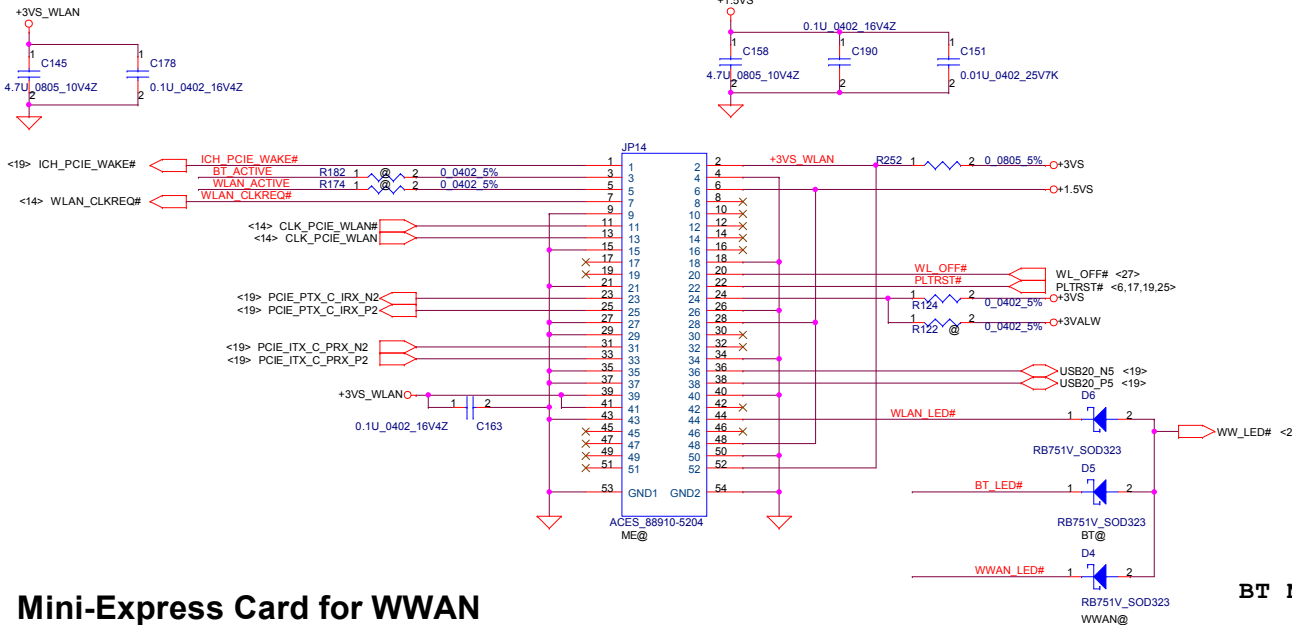
Compal Electronics, Inc.		
Title		
ICH7M(3/4)USB,GPIO,PCIE		
Size	Document Number	Rev
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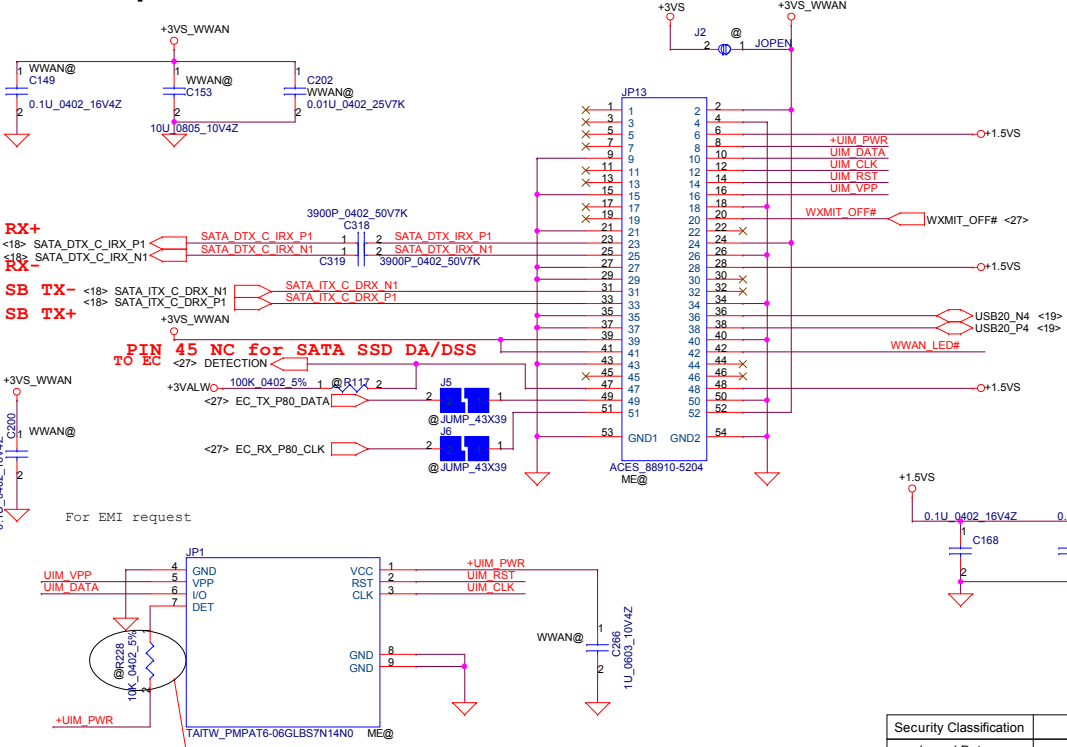
Security Classification		Compal Secret Data	
Issued Date	2006/08/18	Deciphered Date	2007/8/18
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Compal Electronics, Inc.			
Title ICH7M(4/4)POWER/GND			
Size	Document Number	Rev	
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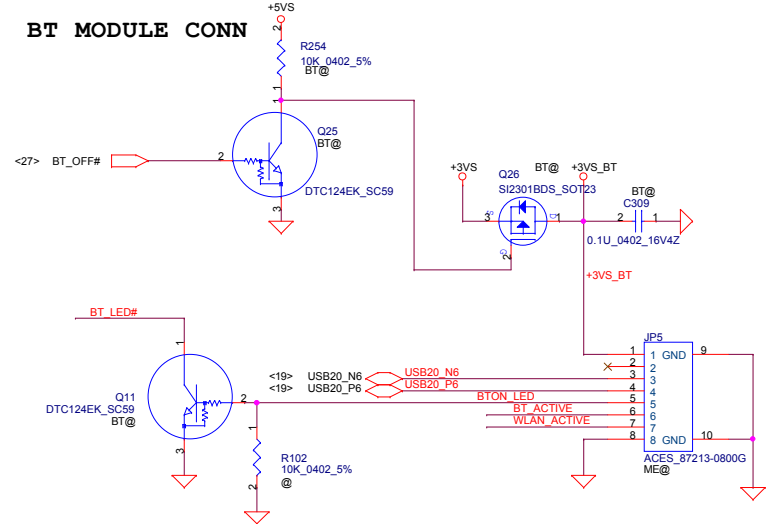
Mini-Express Card for WLAN



Mini-Express Card for WWAN

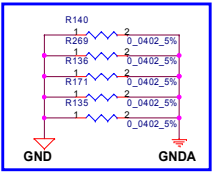
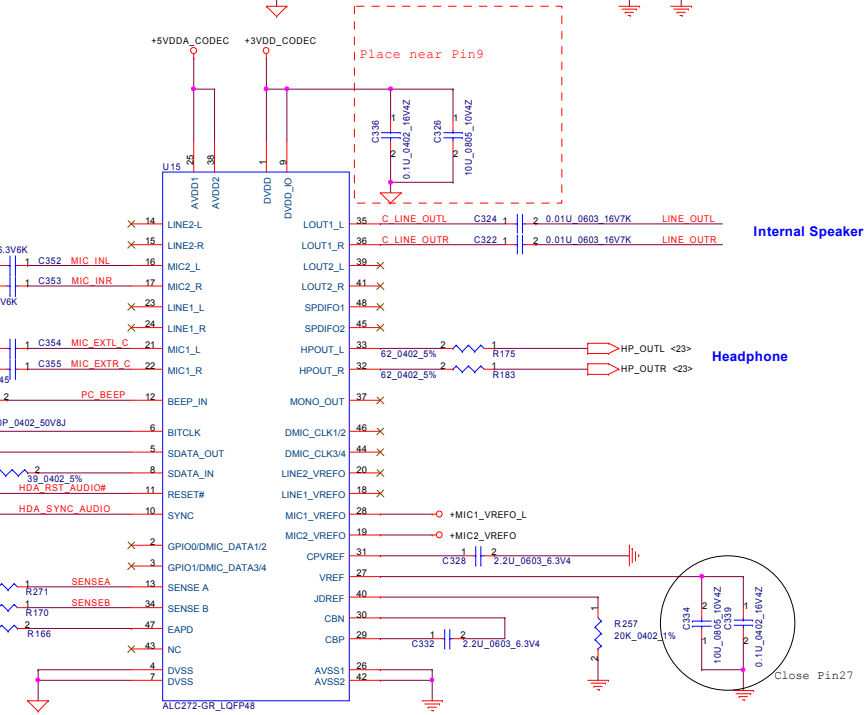
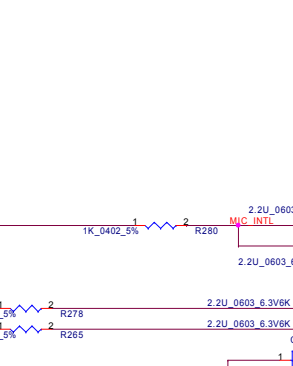
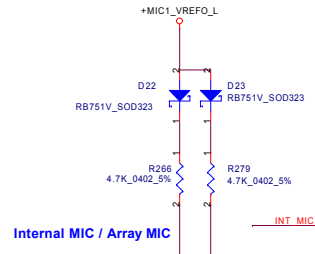
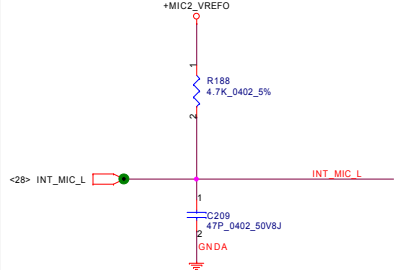
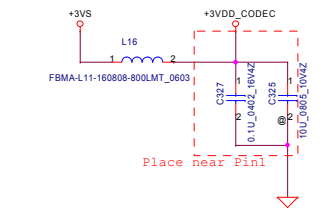
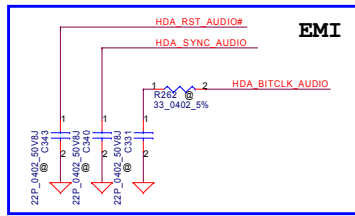
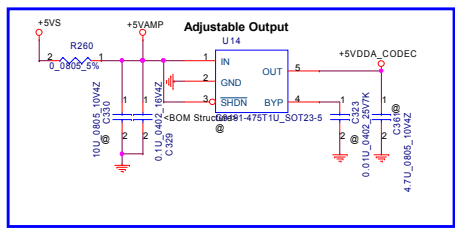


BT MODULE CONN



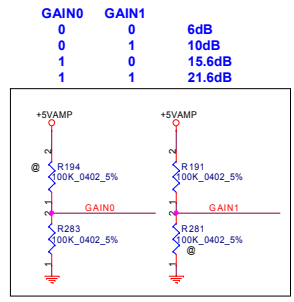
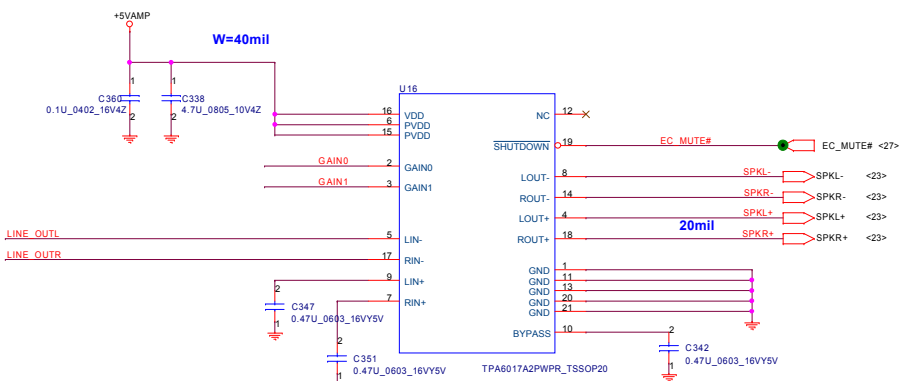
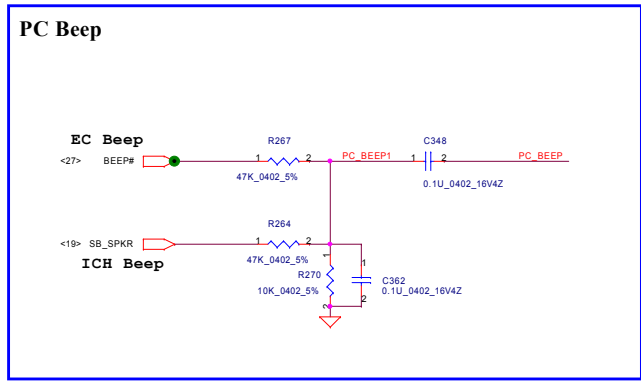
Reserve for SIM card does not meet rise time and pull-up is needed.

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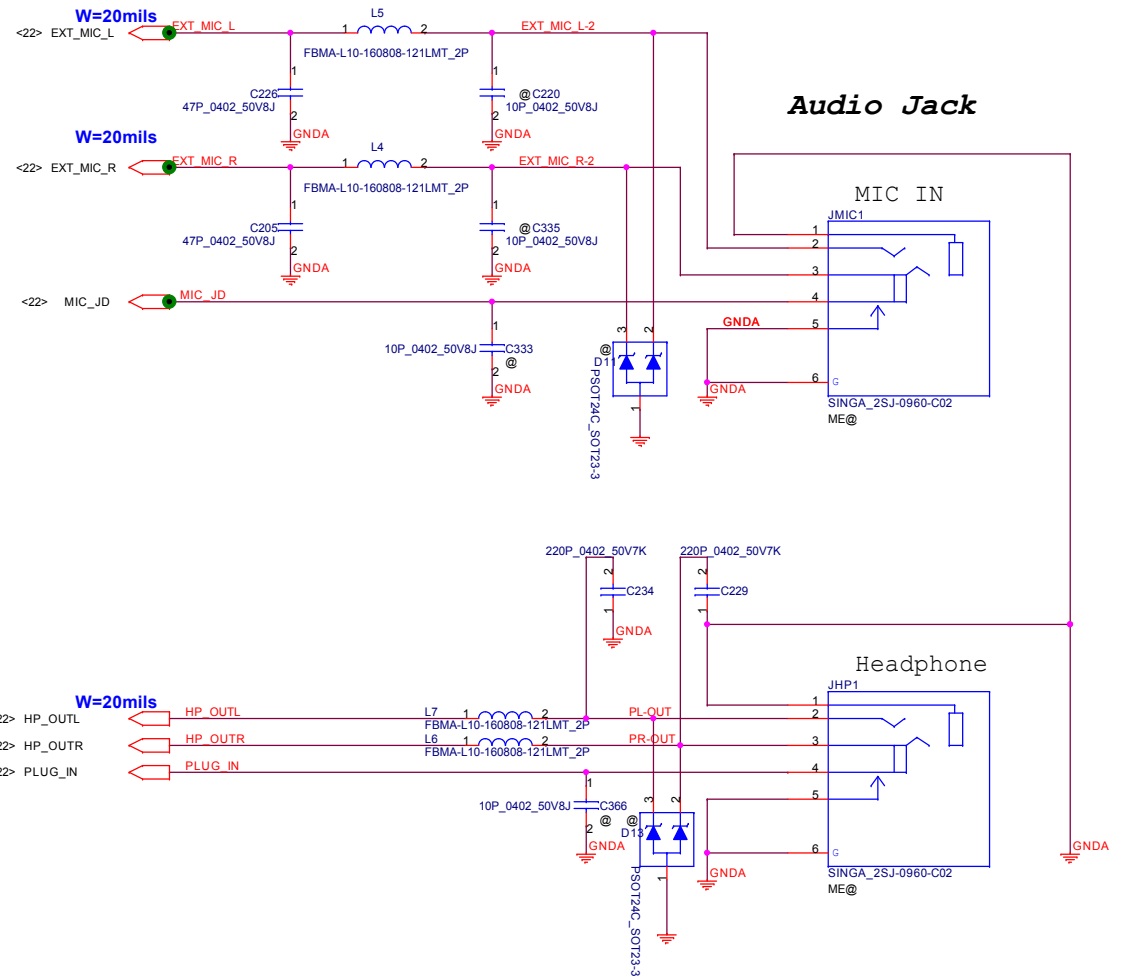
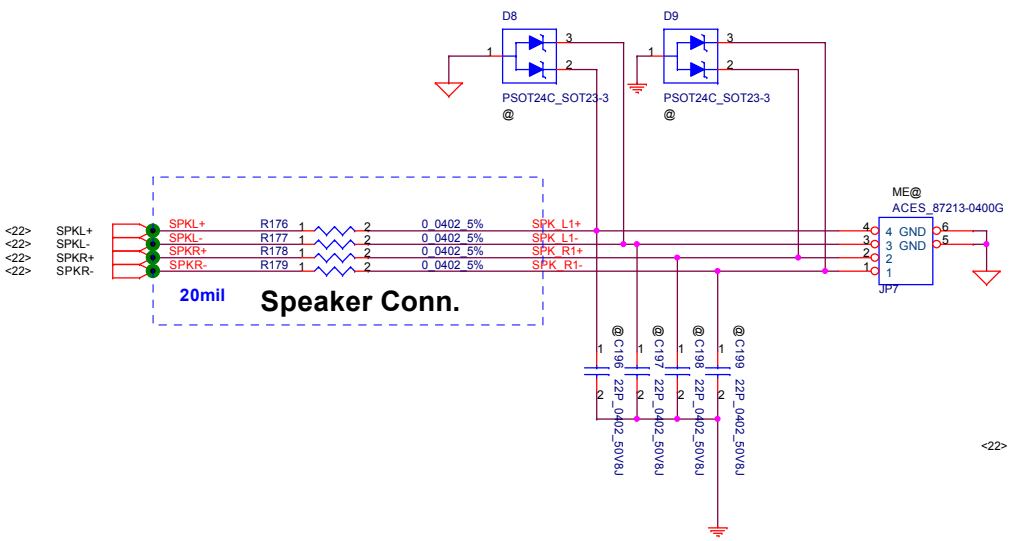


MIC Sense
 R271 place near pin13
 Capless HP Sense
 R170 place near pin34

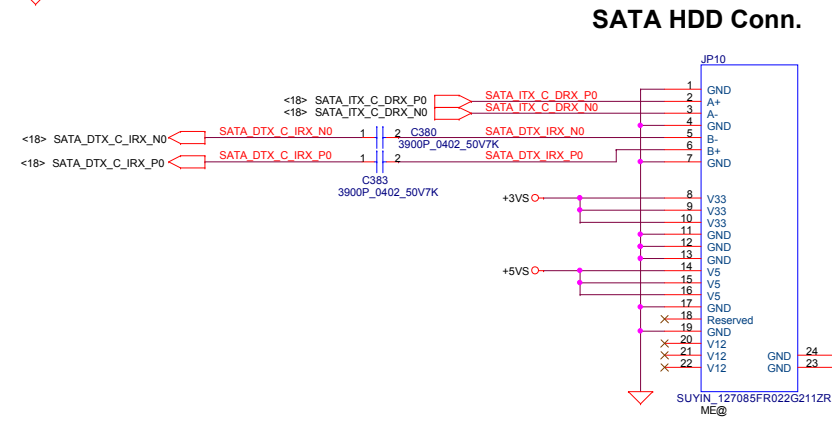
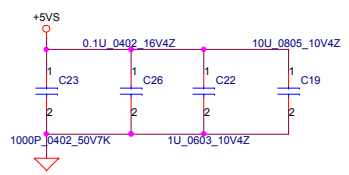
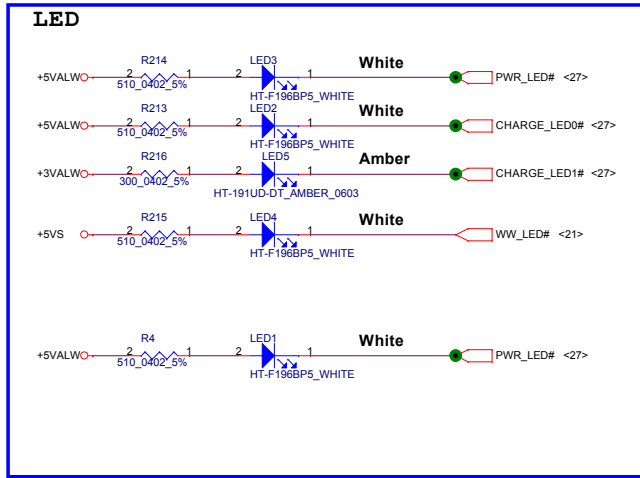
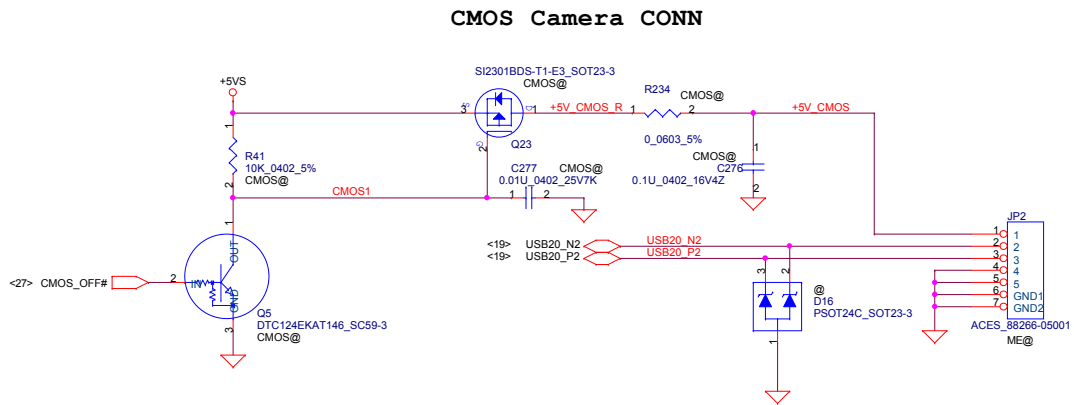
Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	
MIC1 (Pin21/22)	External	Mic in
MONO-OUT (Pin37)	Internal	
MIC2 (Pin16/17)	Internal	Internal Mic



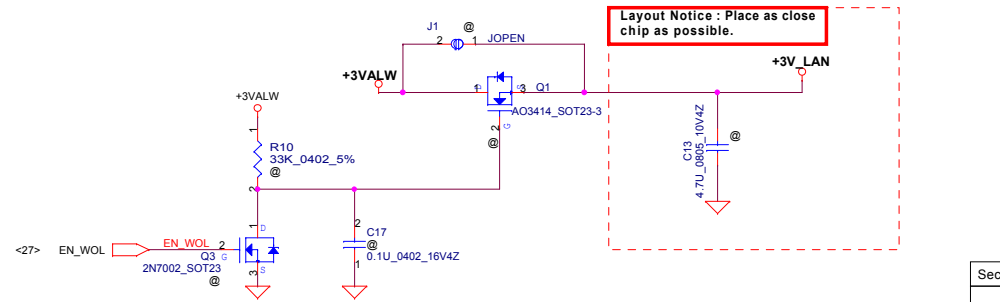
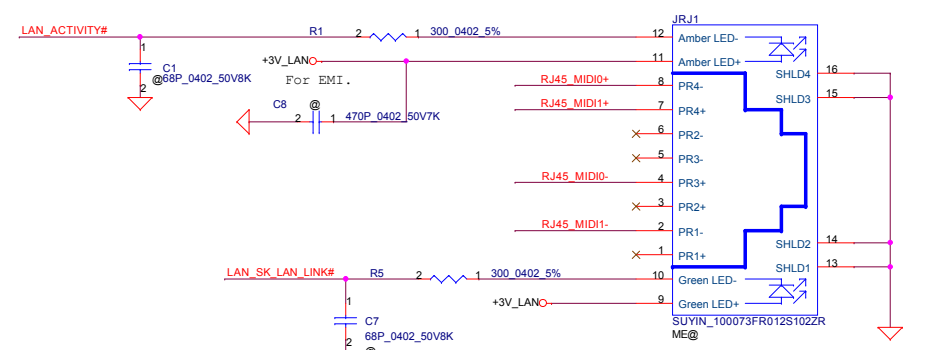
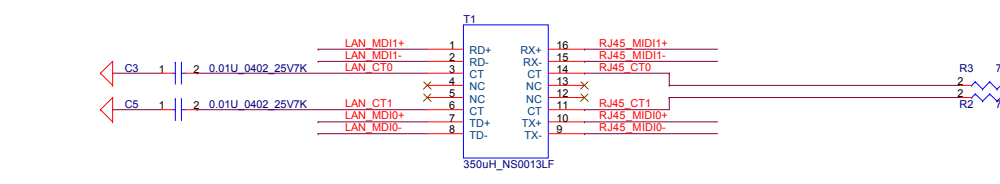
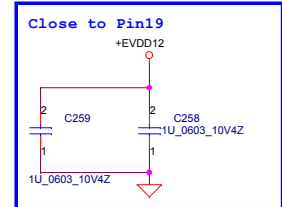
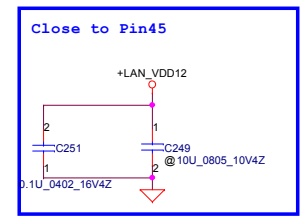
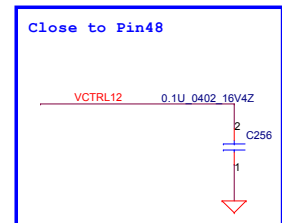
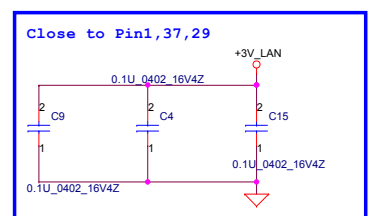
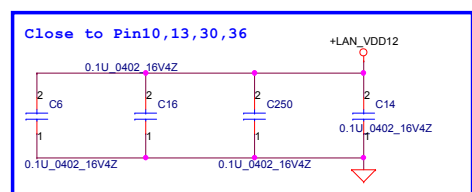
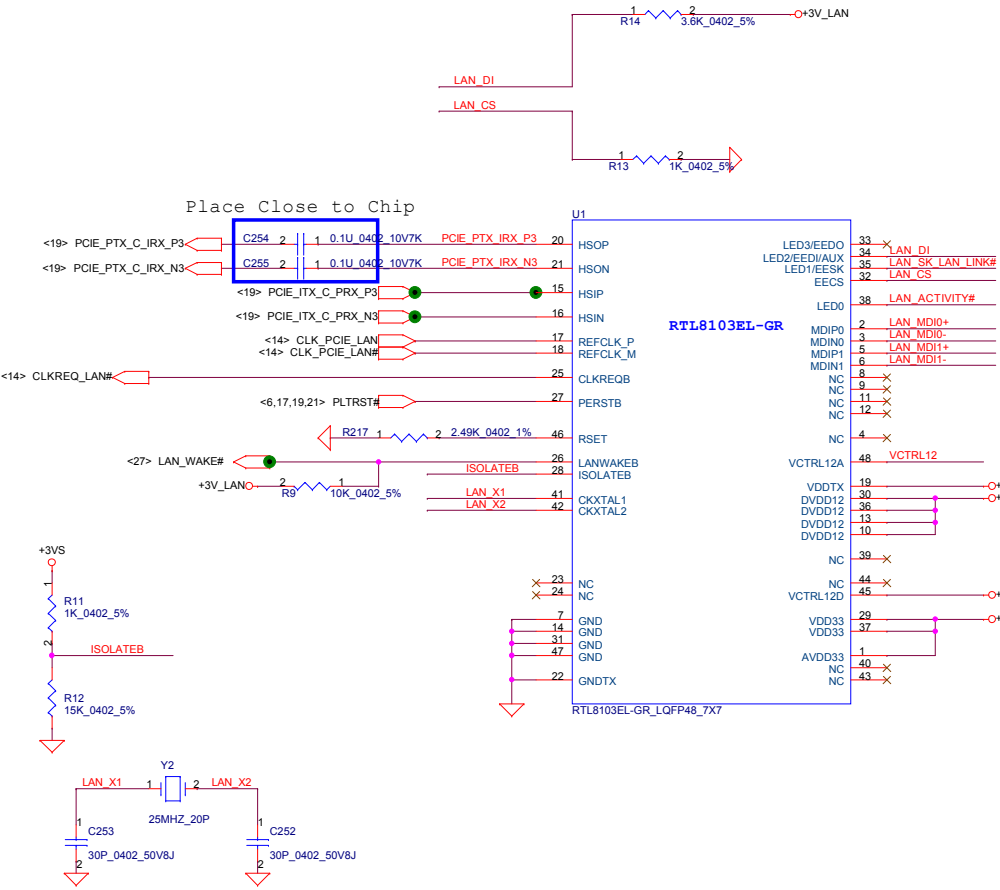
GAIN0	GAIN1	Gain
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



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				AMP, Audio speaker CONN	
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				Custom	KIWB1/B2_LA4601P
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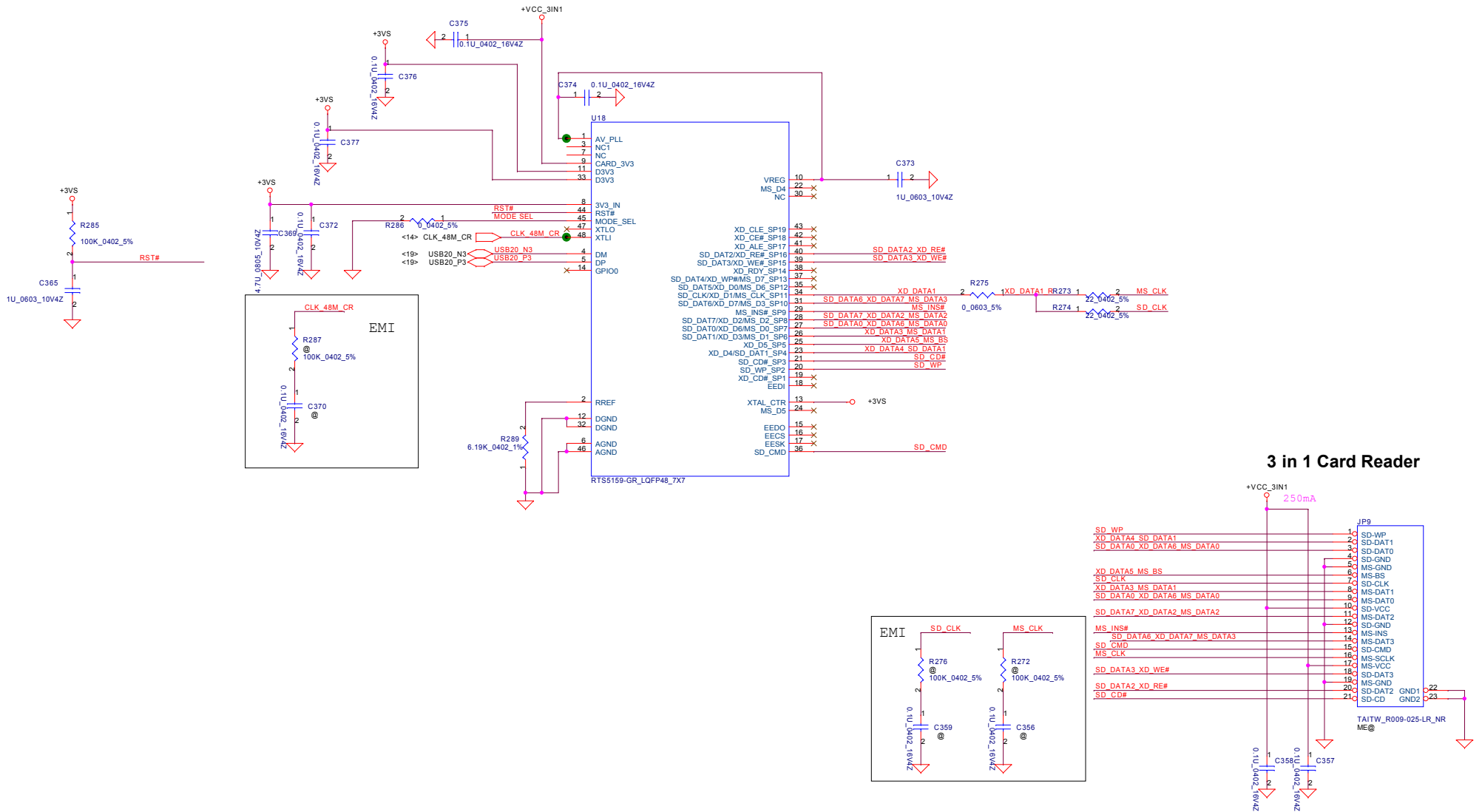


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Size B	Document Number	Rev	0.2	
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Date:	Monday, April 06, 2009	Sheet	24	of 42

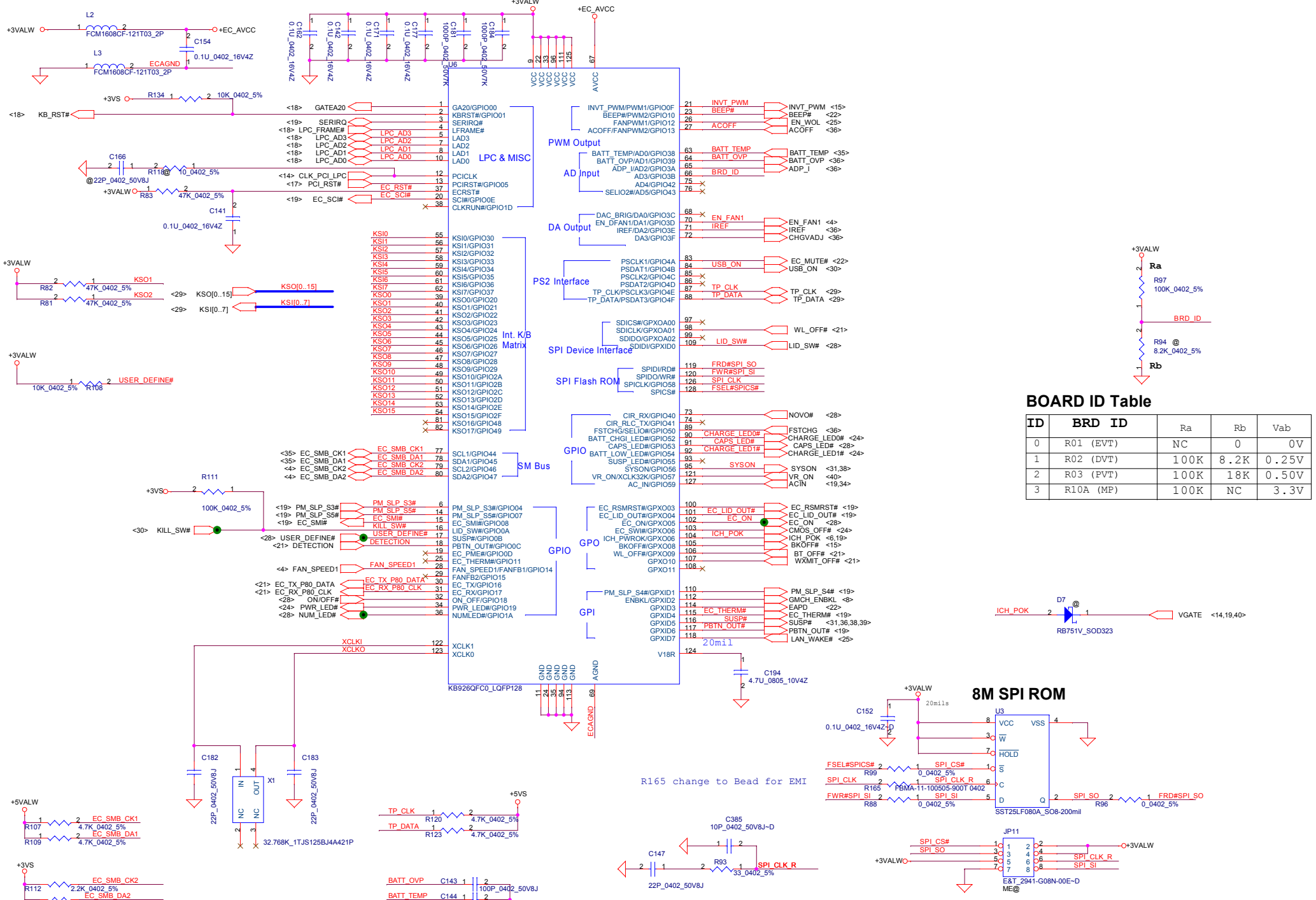


Layout Notice : Place as close as possible.

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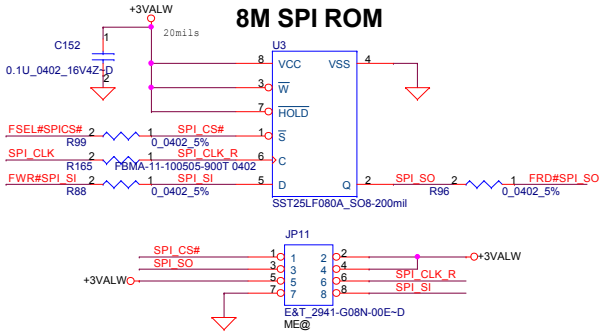


BOARD ID Table

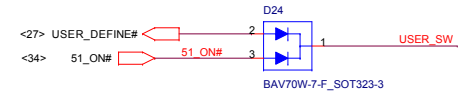
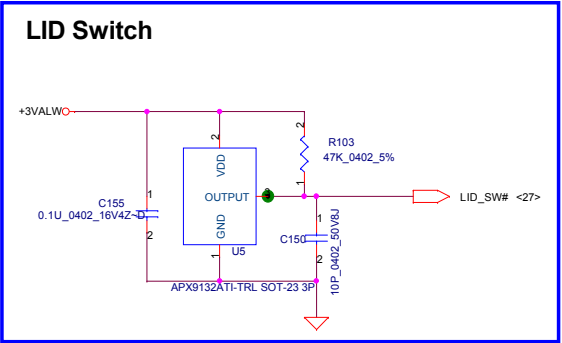
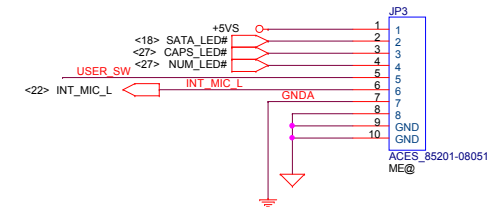
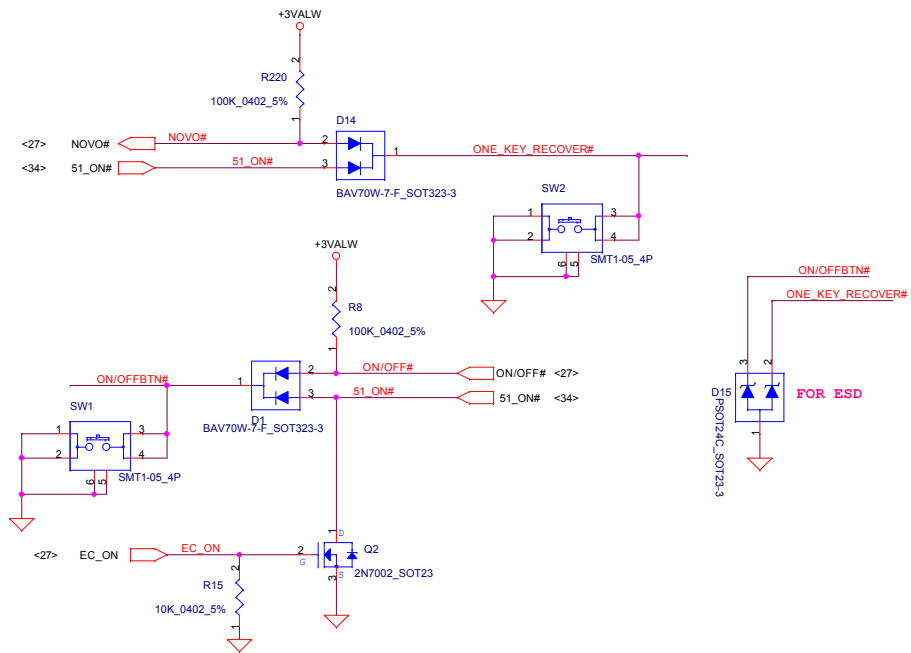
ID	BRD ID	Ra	Rb	Vab
0	R01 (EVT)	NC	0	0V
1	R02 (DVT)	100K	8.2K	0.25V
2	R03 (PVT)	100K	18K	0.50V
3	R10A (MP)	100K	NC	3.3V



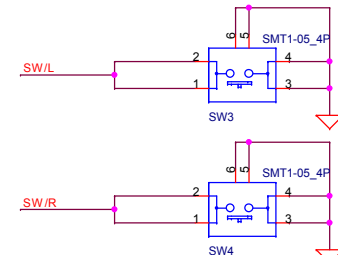
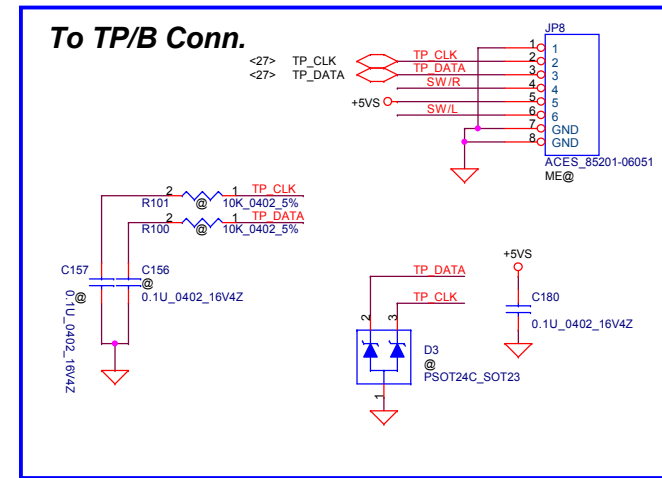
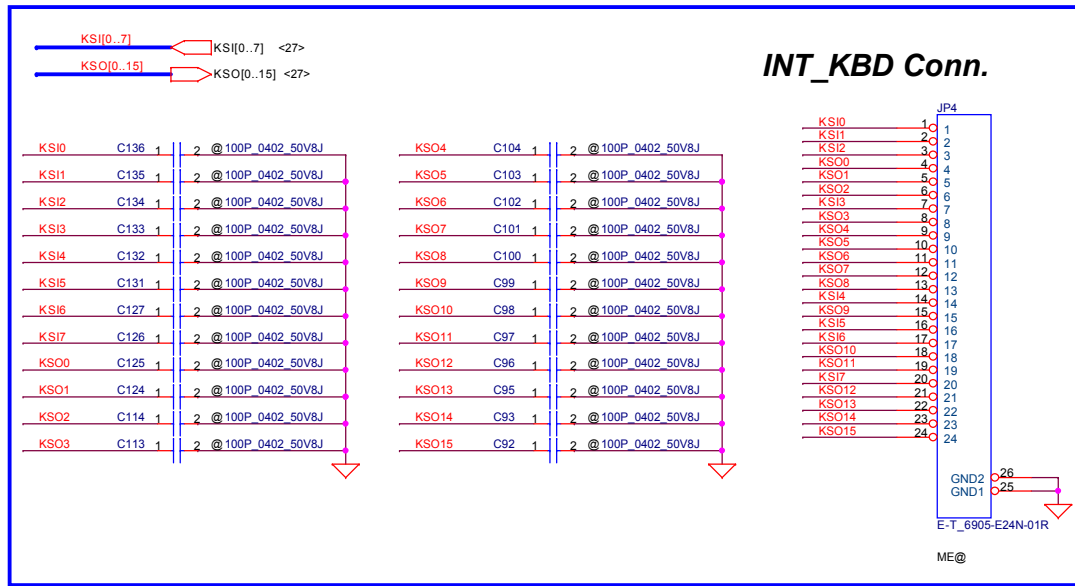
8M SPI ROM



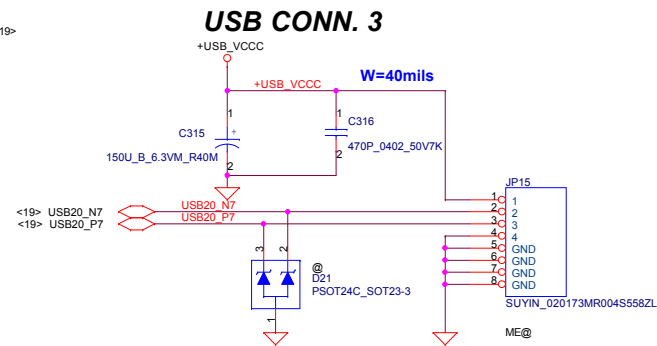
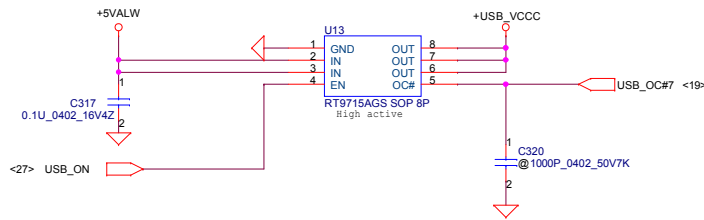
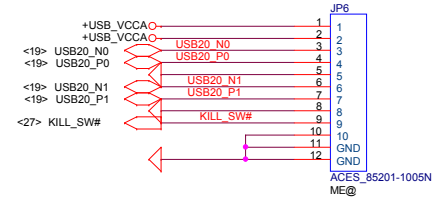
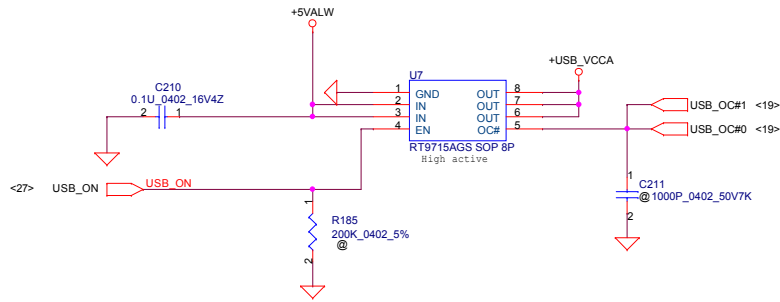
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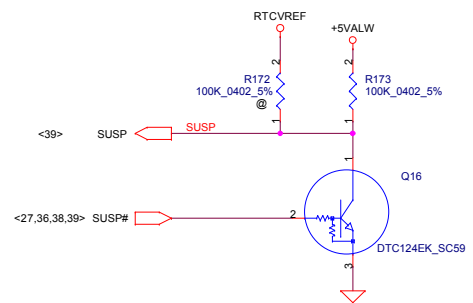
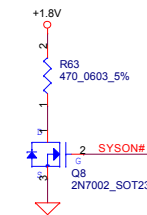
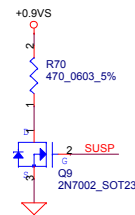
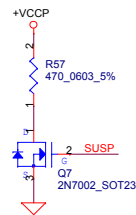
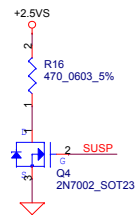
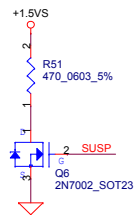
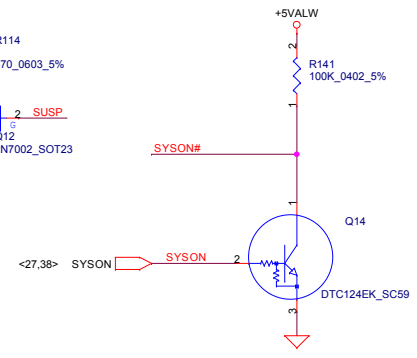
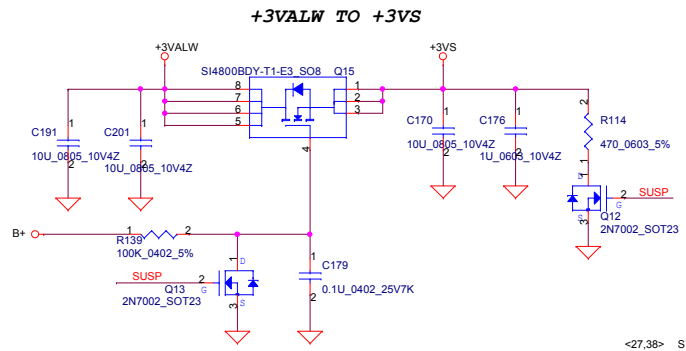
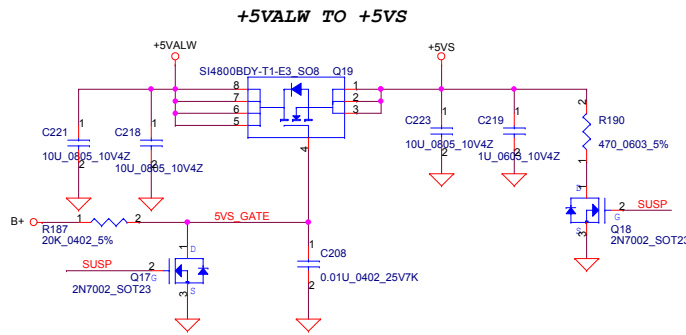
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title	
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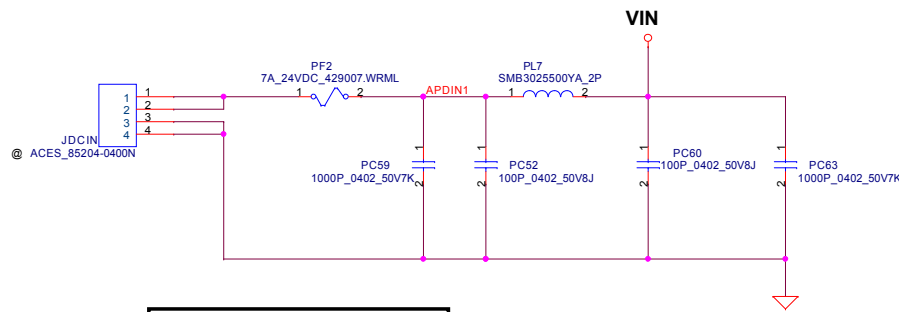
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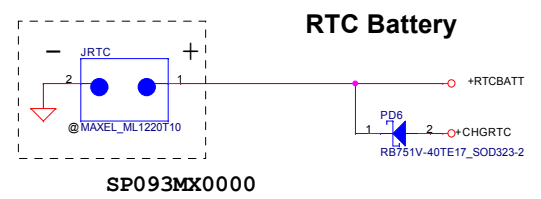
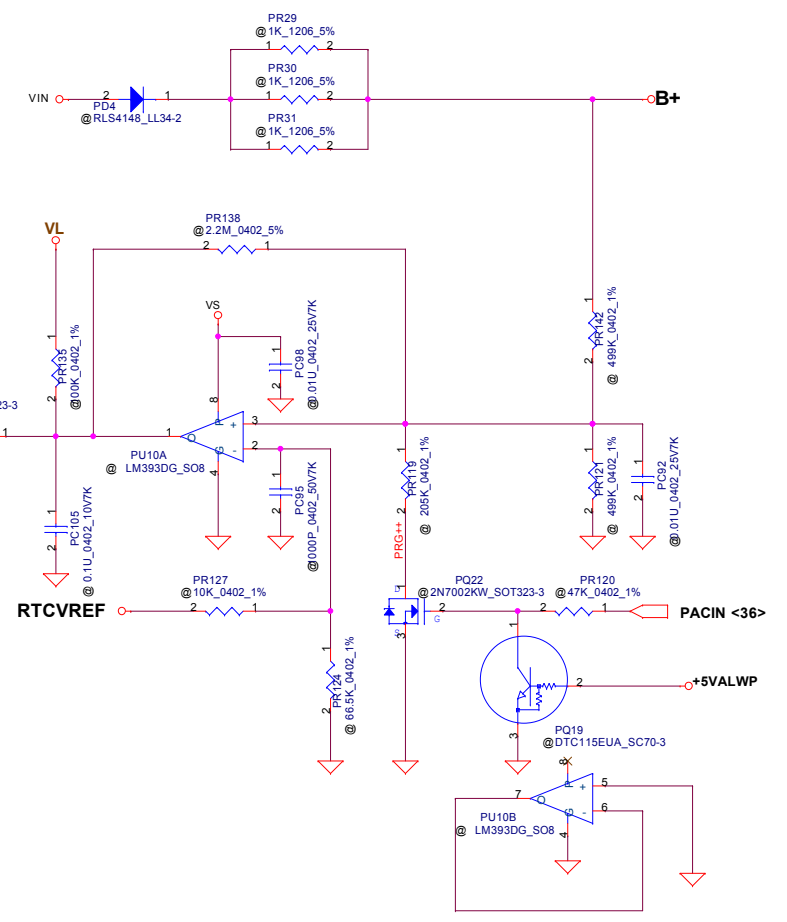
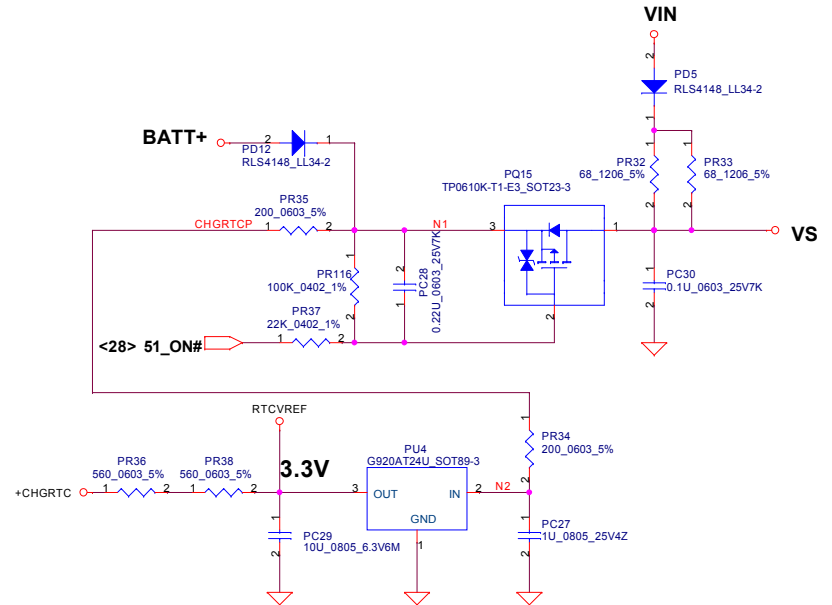
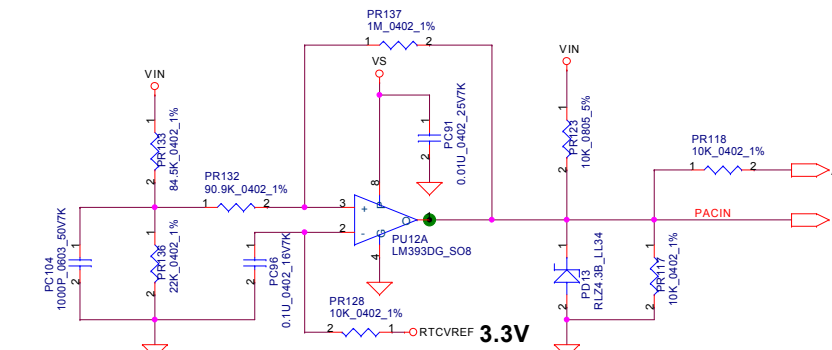
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Issued Date	2006/08/18	Deciphered Date	2007/8/18	Title Screw		
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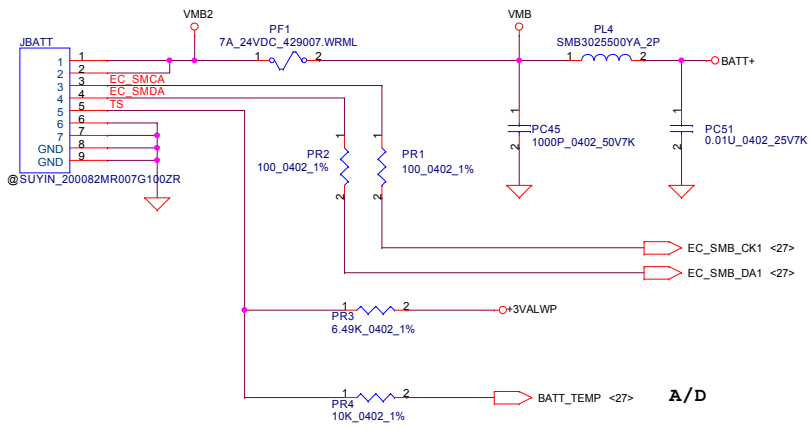
Vin Detector		
High	17.944	17.706
Low	16.242	16.027
	17.470	15.808

ACIN Precharge detector			
	Min.	typ.	Max.
High	14.936V	15.381V	15.814V
Low	13.843V	14.247V	14.636V

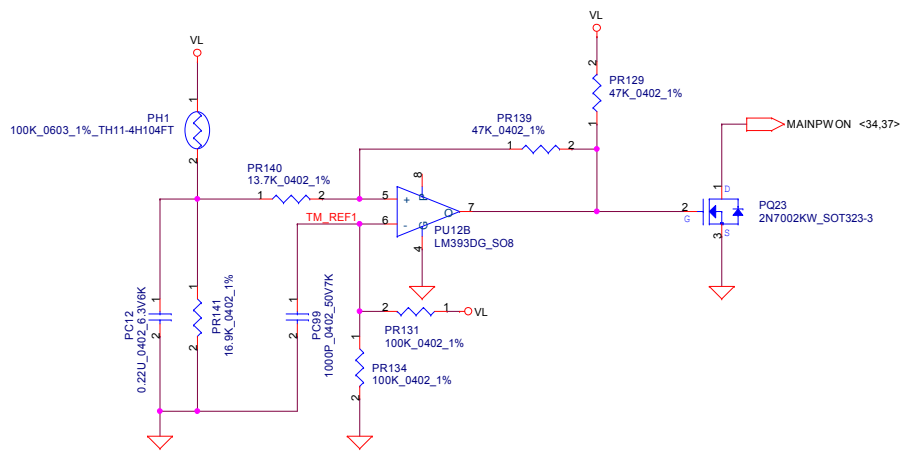
BATT ONLY Precharge detector			
	Min.	typ.	Max.
High	7.196V	7.349V	7.505V
Low	6.138V	6.214V	6.359V



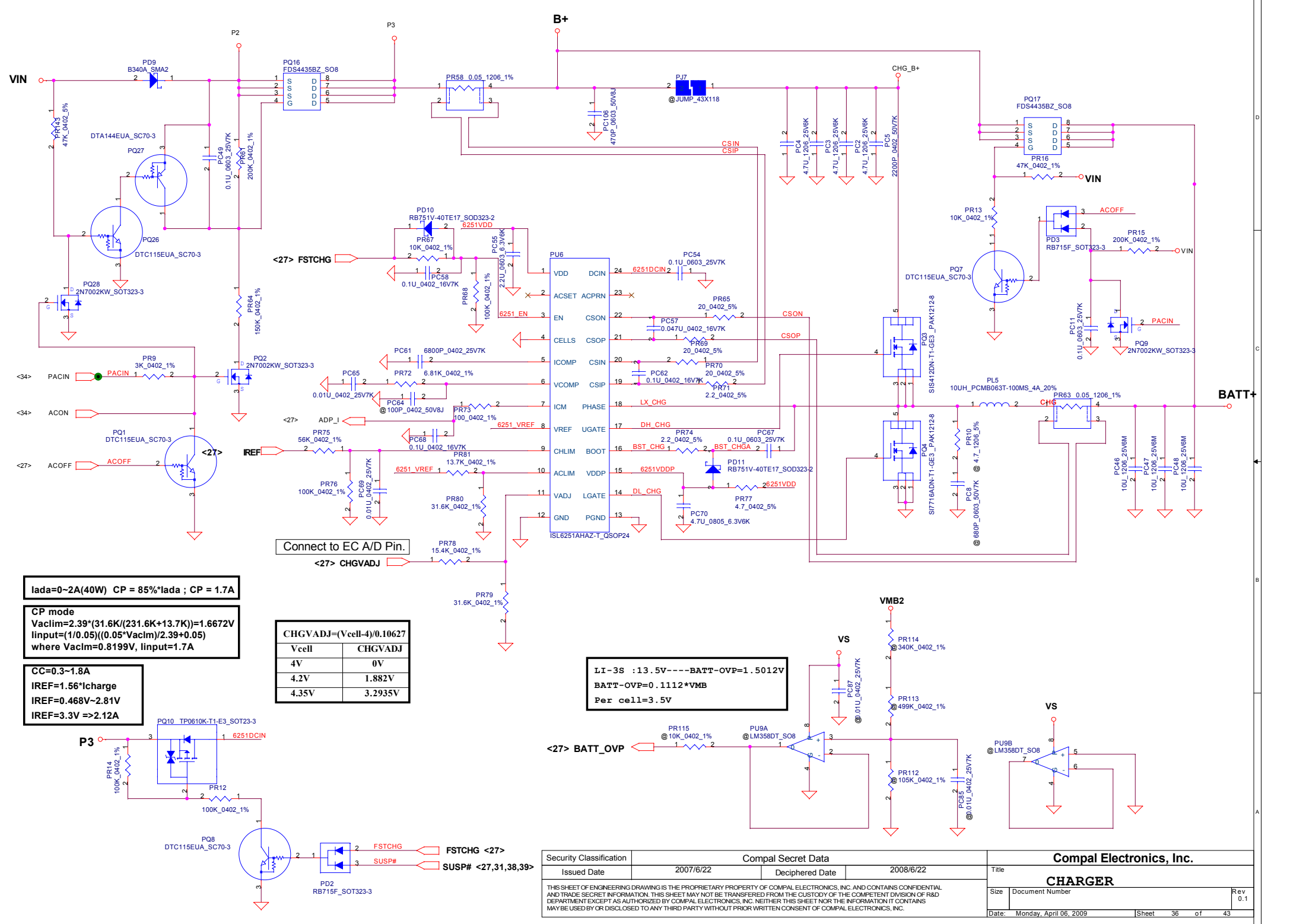
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PH3 under CPU botten side :
 CPU thermal protection at 90 degree C
 Recovery at 45 degree C



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lada=0~2A(40W) CP = 85%*lada ; CP = 1.7A

CP mode
 $V_{acli} = 2.39 * (31.6K / (231.6K + 13.7K)) = 1.6672V$
 $I_{in} = (1/0.05) * ((0.05 * V_{acli}) / 2.39 + 0.05)$
 where $V_{acli} = 0.8199V$, $I_{in} = 1.7A$

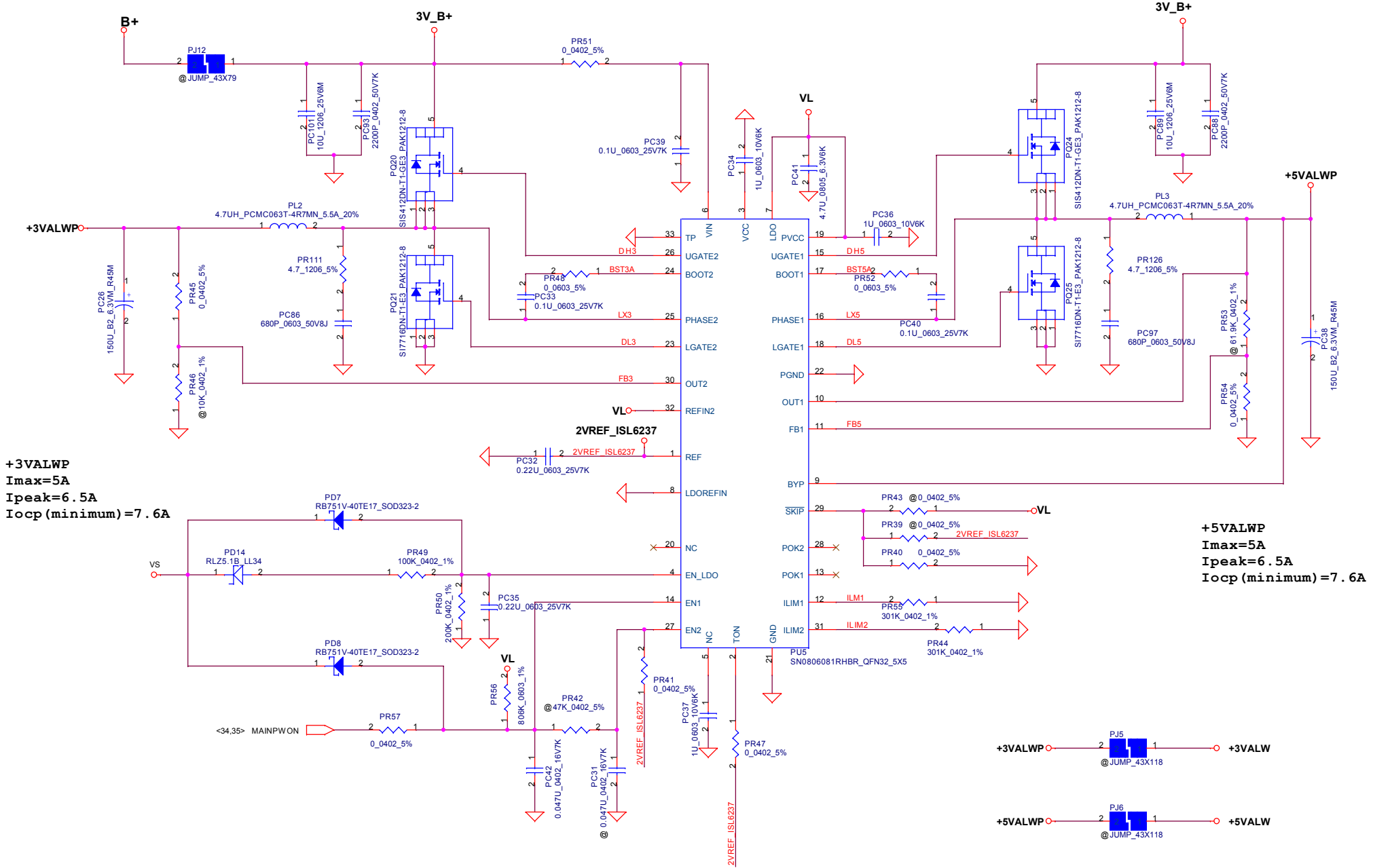
CC=0.3~1.8A
 $I_{REF} = 1.56 * I_{charge}$
 $I_{REF} = 0.468V \sim 2.81V$
 $I_{REF} = 3.3V \Rightarrow 2.12A$

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

LI-3S : 13.5V --- BATT-OVP=1.5012V
 $BATT-OVP = 0.1112 * VMB$
 Per cell=3.5V

<27> BATT_OVP

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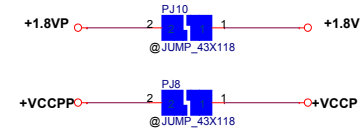
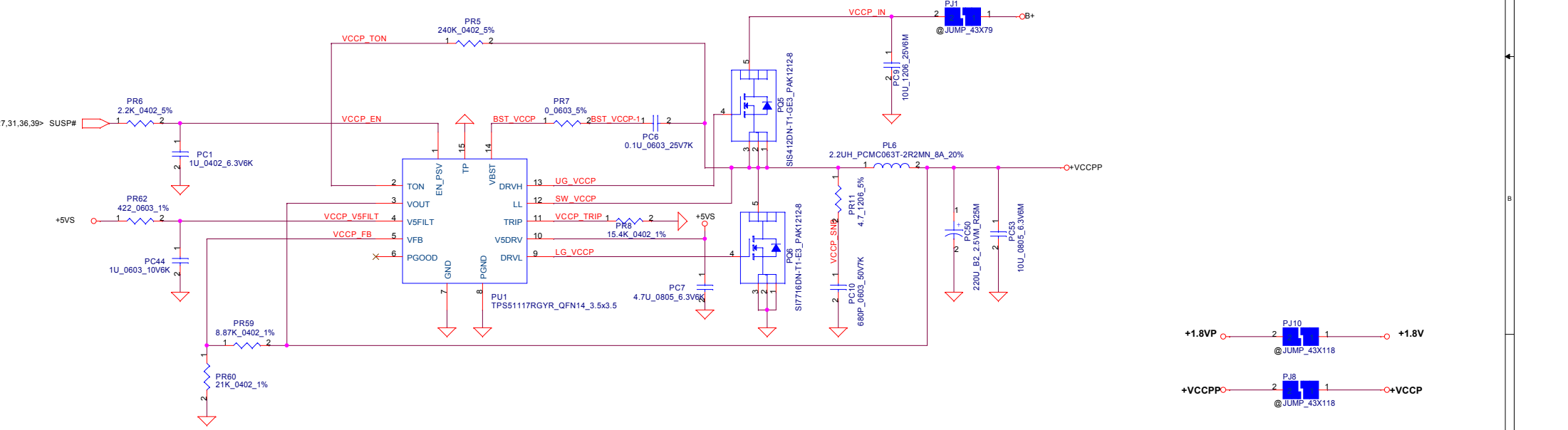
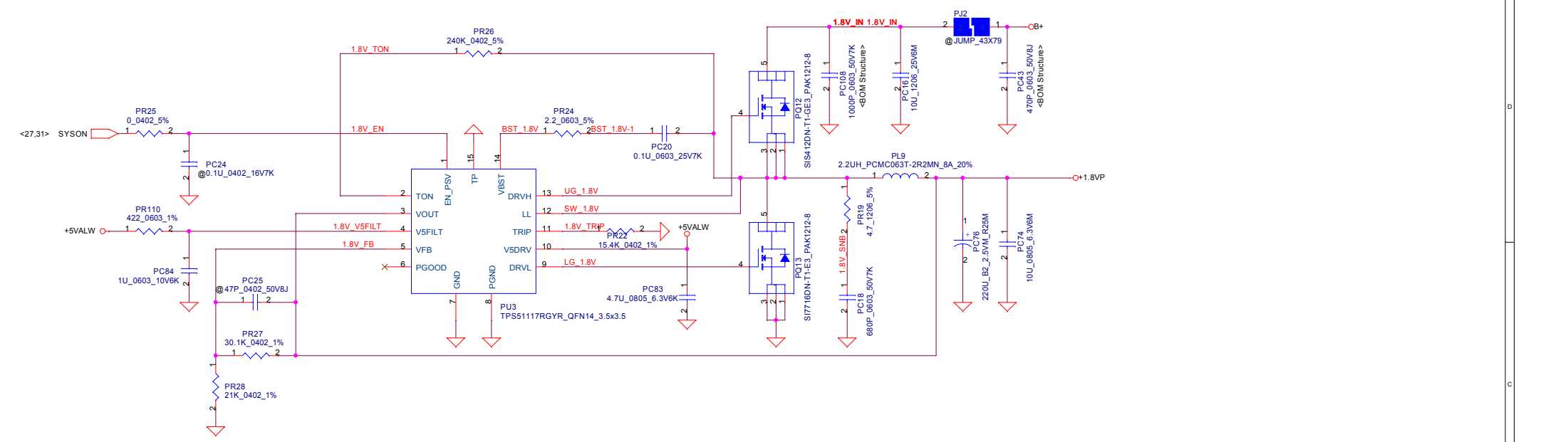
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I_{max}=5A
I_{peak}=6.5A
I_{oip} (minimum)=7.6A

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I_{peak}=6.5A
I_{oip} (minimum)=7.6A

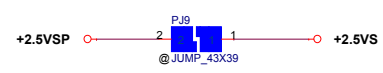
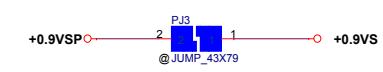
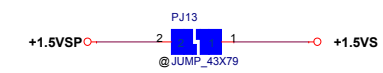
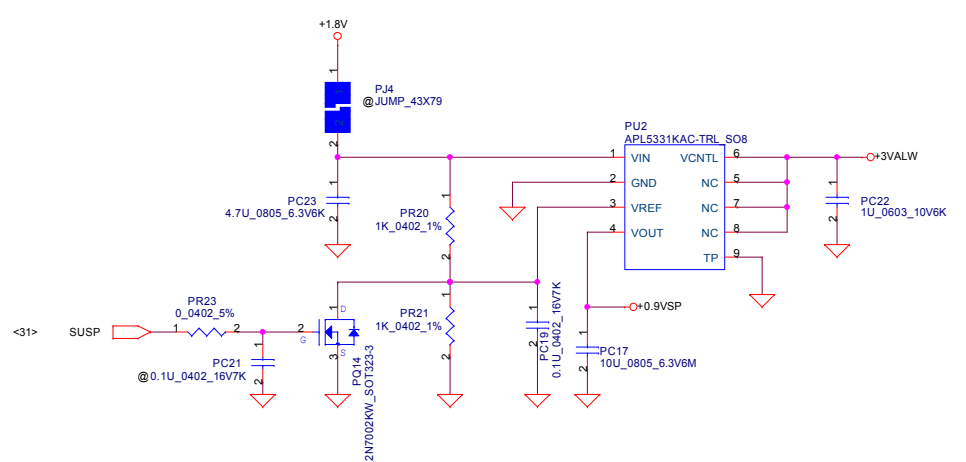
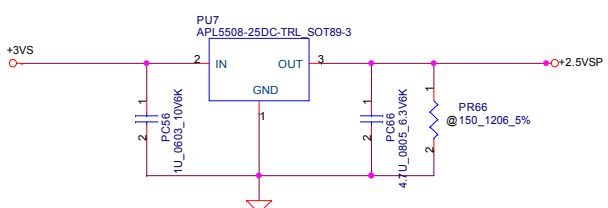
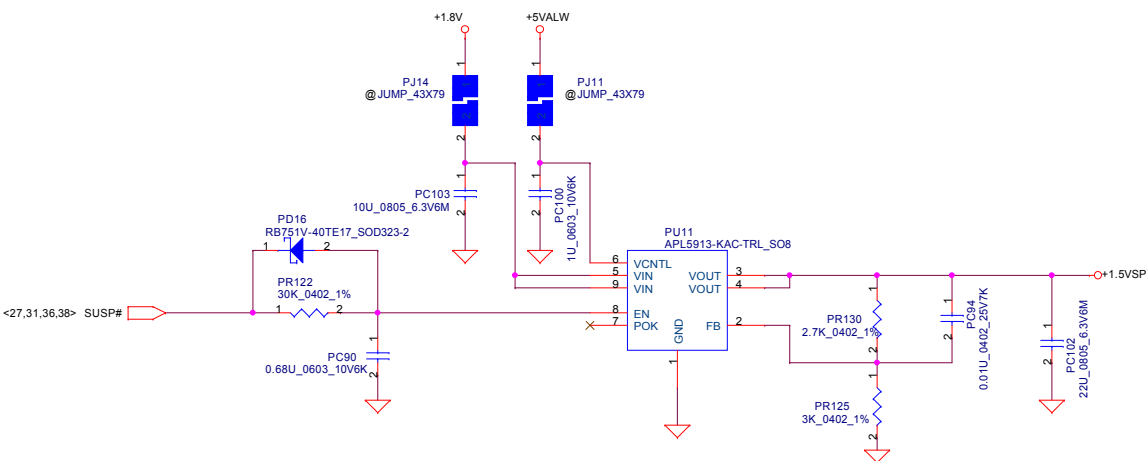
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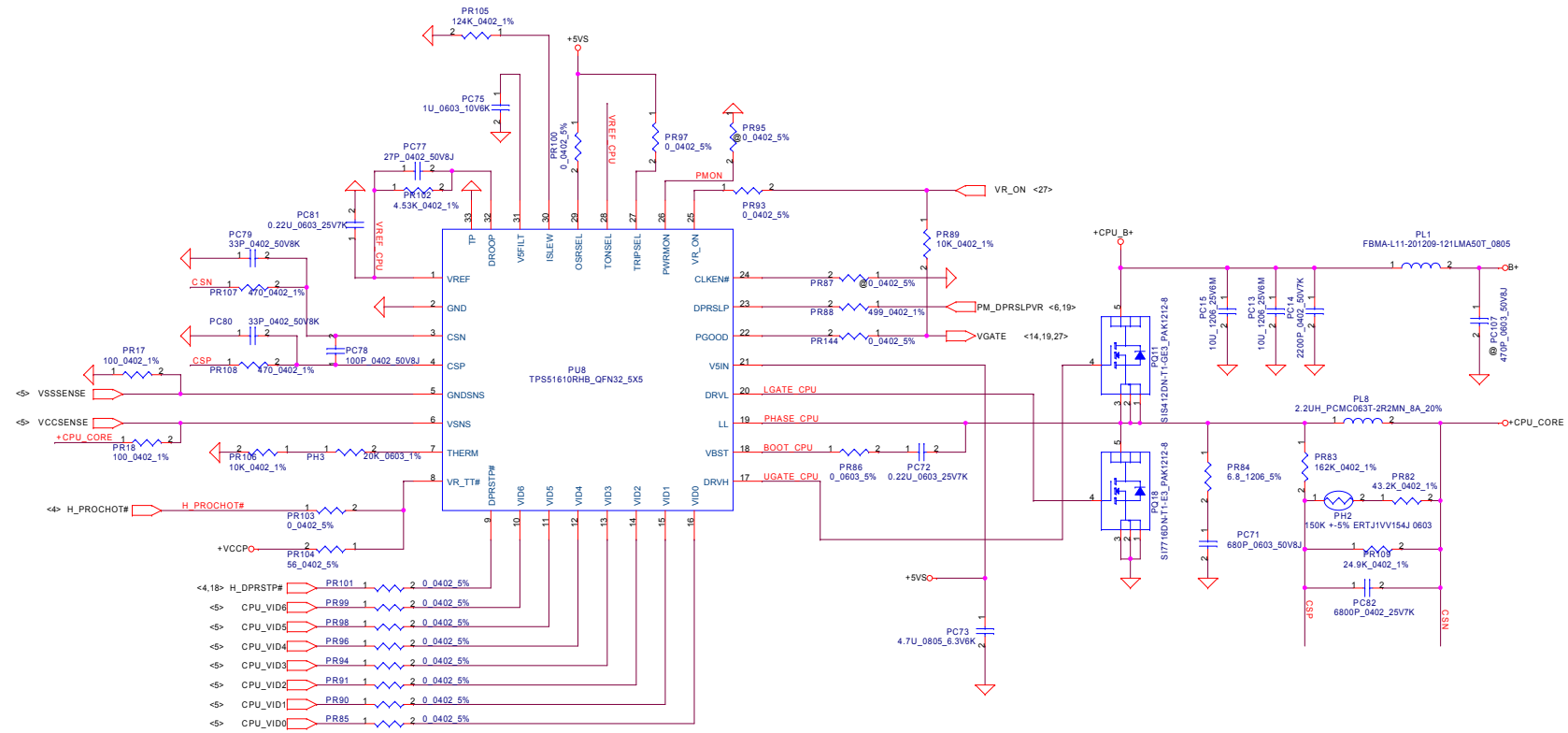
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Item	Fixed Issue	Rev.	PG#	Modify List
1	LAN JRJ1	0.2	P25	Change JRJ1 Pin define
2	Change NB,SB P/N	0.2		Change NB to SA00002KQ50 SB to SA00000V1D0
3	Customer request	0.2	P29	TP l2pin change to 6pin
4		0.2		Q26 3413 change to 2301
5		0.2	P29	SW3,4 change to SN100000K00
6	Customer request	0.2	P28	change net name NOVO_BTN# to ONE_KEY_RECOVER#
7		0.2	P22	Change C352,C353,C354,C355 to SE107225K80
8		0.2	P04	Change C312,C314 to SE000003H00
9		0.2	F13	Change C109,C110,C128,C129,C130,C112 to SE103225Z80
10	Modify LCD power squnce	0.2	F15	Change R221 to I00K
11	Fix WLAN card leakage	0.2	P21	Delete WLAN port80 and cut WWAN port80
12	User define key support power on	0.2	P28	Add D24 for user define key power on and pull up change to +3valv
13	ESD request	0.2	P28	D15 change to SCA00000R00
14	Realtek recommend	0.2	P25	C258 change to luf
15		0.2		C71 and C81 change to 0603
16	For B Phase	0.2	P27	Add R97 I00k and change R94 to 8.2K
17	EMI request	0.2	P27,15	Add R93,C385,C147,C10,C11 Change R165 to 33 ohm
18	ESD request	0.2	P4	Add C391~C397
19	For N280	0.2	F14	Unpop: R68,I10,87 Pop:R69,119,84
20	Realtek recommend	0.2	P25	Delete C257
21		0.2	P10	C30 change to SE027474Z80
22	Customer request	0.2	F30	U7,30 change to high active unpop R185
23		0.2	P22	Unpop C325 POP C326
24	EC code for MP	1.0	P27	Unpop R94
25	SSD pin change	1.0	P21	JP13 32pin change to 47pin
26		1.0	P28	Change D14,D24 foorprint
27		1.0		Change BT connect
28		1.0	P16	Change D2 from SC1B491D000 to SCS00002000
29		1.0		Change C373, C297, C71, C73, C81, C82, C84 and C85 to SE052105Z80
30		1.0	P20	Unpop D12
31	EMI request	1.0	P20	Add C257,C398,C399,C400
32		1.0	P04	Unpop R58
33	SSD	1.0	P21	Unpop R117
34	EMI request	1.0	P27	R165 change to bead for EMI request
35	3G request	1.0	F14	Pop C390
36		1.0	P28	Change D1,14,24 P/N SC2N202U010 to SC6AV70W110
37		1.0	P27	Unpop D7

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Adjust charging current	Adjust charging current		P36	Change PR75 from 88.7K to 56K.	2008.12.30	EVT
2	EMI	EMI requests to add soltion		P40	Add PC107	2009.02.13	PVT
3	Adjust charging voltage	Adjust charging voltage		P36	Change PR78 from 18.2K to 15.4K.	2009.02.13	PVT
4	EMI	EMI requests to add soltion		P36	Add PC106	2009.02.13	PVT
5	EMI	EMI requests to add soltion		P38	Add PC108 and PC43	2009.02.13	PVT
6	Design change	Adjust +1.5VSP turn on timing		P39	Add PD16 Change PR122 from 10K to 30K. Change PC90 from 0.47u to 0.68u.	2009.02.13	PVT
7	Thermal	Adjust CPU OTP from 85 degree C to 90 degree C		P35	Change PR141 from 21.5k to 16.9k.	2009.03.13	Pre-MP
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Item	Fixed Issue	Rev.	PG#	Modify List
1	LAN JRJ1	0.2	P25	Change JRJ1 Pin define
2	Modify LCD power squence		P15	Change R221 to 100K
3	Customer request	0.2	P29	TP 12pin change to 6pin
4	Fix WLAN card leakage	0.2	P21	Delete WLAN port80 and cut WWAN port80
5	User define key support power on	0.2		Add D24 for user define key power on and pull up change to +3valw
6	Customer request	0.2	P28	Change net name NOVO_BTN# to ONE_KEY_RECOVER#
7	ESD request	0.2	P28	D15 change to SCA00000R00
8	Realtek recommend	0.2	P25	C258 change to 1uF
9	For B Phase	0.2	P27	Add R97 100k and change R94 to 8.2K
10	EMI request	0.2	P27,15	Add R93,C385,C147,C10,C11 Change R165 to 33 ohm
11	ESD request	0.2	P4	Add C391-C397
12	For N280	0.2	P14	Unpop: R68,110,87 Pop:R69,119,84
13	Customer request	0.2	P30	U7,30 change to high active unpop R185
14	EC code for MP	1.0	P27	Unpop R94
15	Mini SSD pin define change	1.0	P21	JP13 pin 32 change to 47 30 change to 45
16				
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22		0.2		
23		0.2		
24				

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