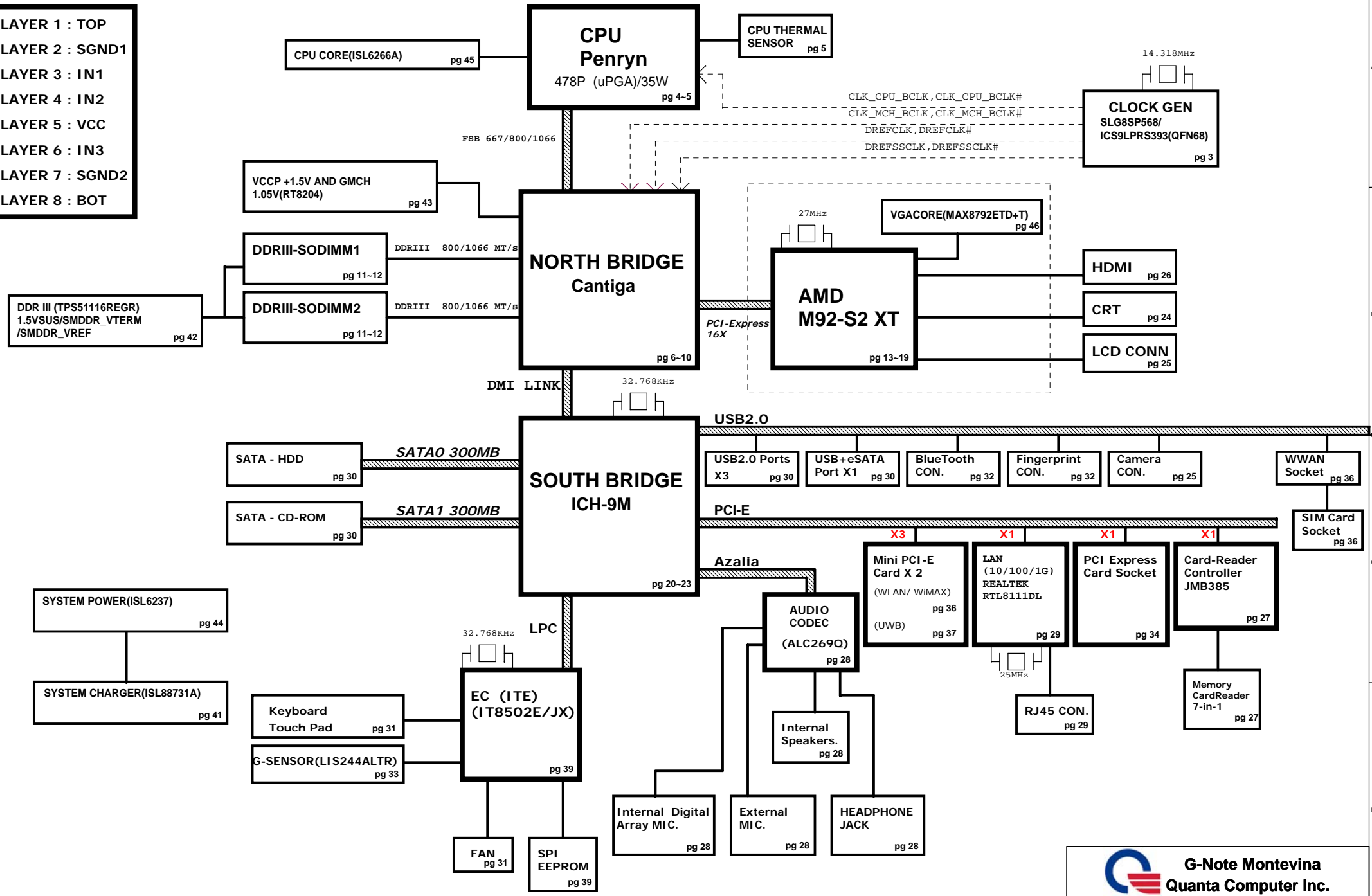


- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT




		Document Number	Rev 2A
		Block Diagram	
Date: Tuesday, March 03, 2009	Sheet 1 of 56		

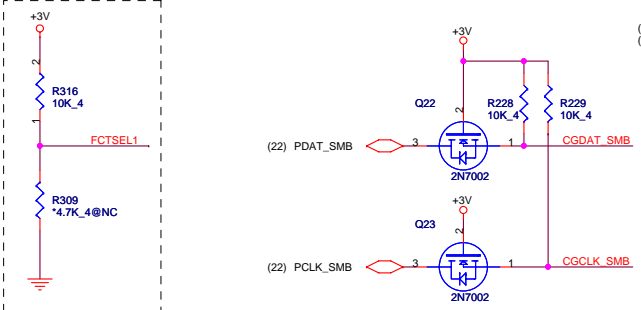
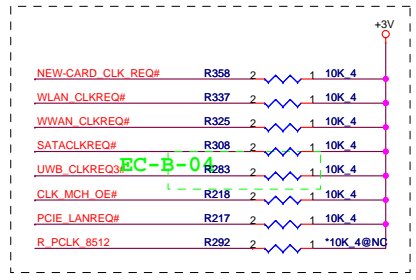
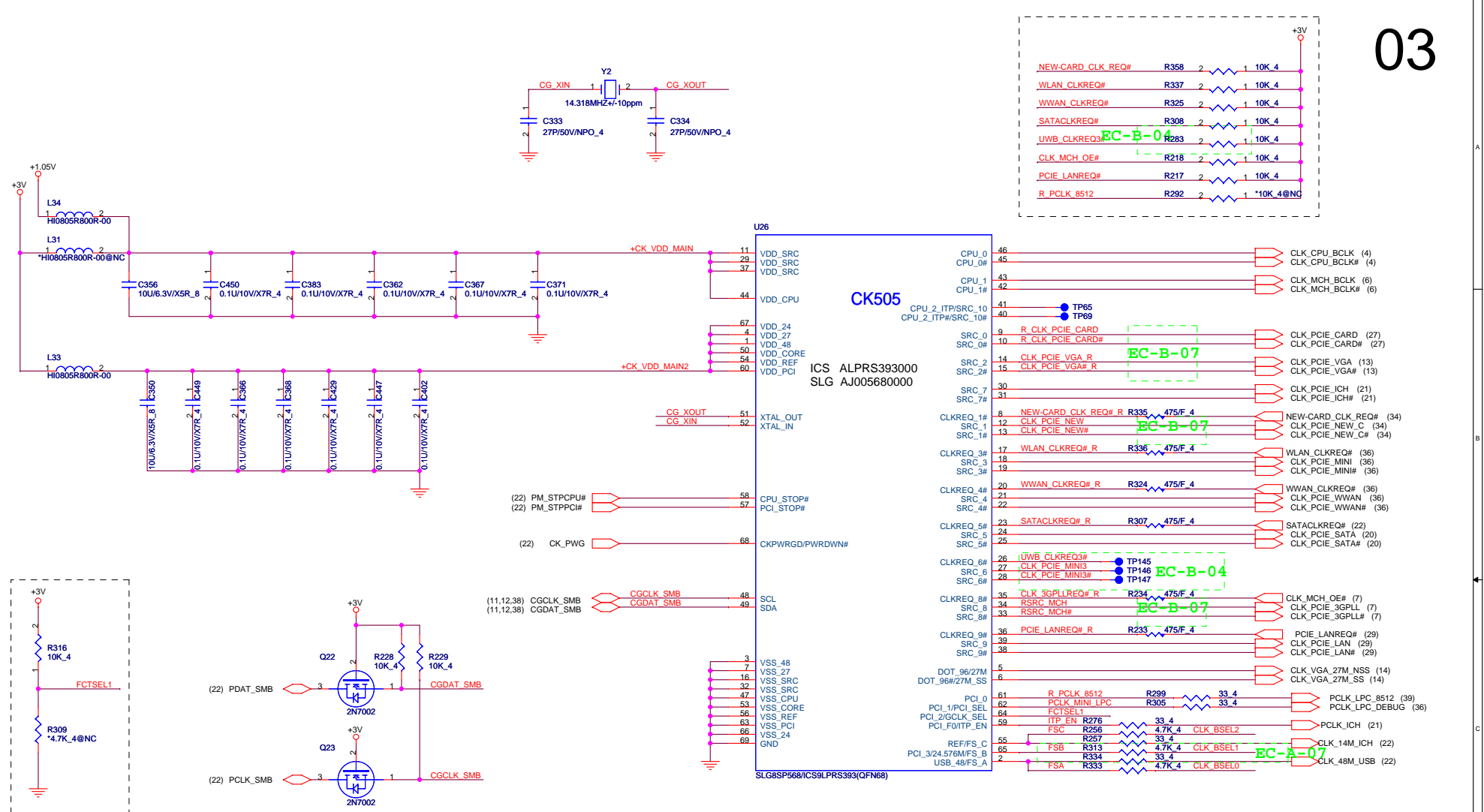
Will chang after circuit  
finished

Power States

02

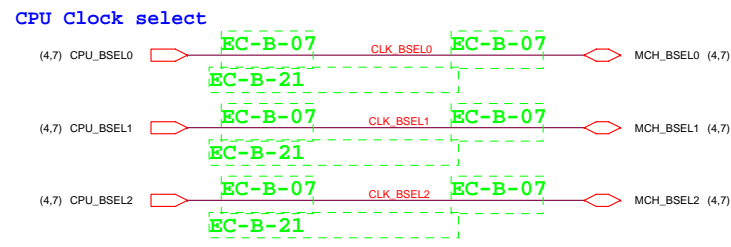
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+19V	25,40,41,42,43,44,45,46,47	MAIN POWER		S0~S5
+3VRTC	+3.0V~+3.3V	20,23,39	RTC		S0~S5
3VPCU	+3.3V	20,25,29,31,37,39,40,41,44	8051 POWER		S0~S5
5VPCU	+5V	27,30,37,40,41,42,43,44,45,46,47	LCD/CHARGE POWER		S0~S5
+15V	+15V	25,40,44,47	LARGE POWER	5VPCU	S0~S5
LANVCC	+3.3V	29,40	LAN POWER	LAN_ON	
5VSUS	+5V	25,30,37,40,43,45,46	SLP_S5# CTRLD POWER	SUSON	
3VSUS	+3.3V	21,22,34,35,36,39,40,45	SLP_S5# CTRLD POWER	SUSON	
1.8VSUS	+1.8V	40,43,47	SODIMM POWER	SUSON	
+0.9V_DDR_VTT	+0.9V		SODIMM POWER	MAINON	
+5V	+5V	23,24,25,26,28,30,31,39,40,41	SLP_S3# CTRLD POWER	MAINON	
+3V	+3.3V	3,5,7,10,11,12,14,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42,43,44,45,47	SLP_S3# CTRLD POWER	MAINON	
+1.8V	+1.8V	14,15,16,17,18,19,47	VGA POWER	MAINON	
+1.5V	+1.5V	5,10,20,21,22,23,34,35,36,40,43	CALISTOGA/ICH8 POWER	MAINON	
+1.05V	+1.05V	3,4,5,6,7,9,10,20,23,40,43,45	CPU/CALISTOGA/ICH8 POWER	MAINON	
VCC_CORE	+0.7V~+1.77V	4,5,40,45	CPU CORE POWER	VRON	
LCDVCC	+3.3V	25	LCD Power	INT_DISP_ON & EXT_LVDS_DIGON	
+5VHDD	+5V	30	HDD Power	MAINON	
MBATV	+10V~+17V	39,41	MAIN BATTERY	D/C#	

 <b>G-Note Montevina</b> <b>Quanta Computer Inc.</b>		Document Number	Rev
		FRON TPAGE	2A
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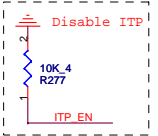
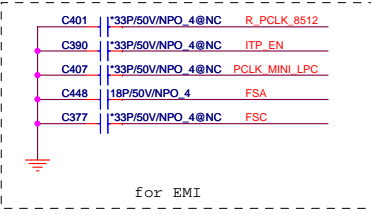


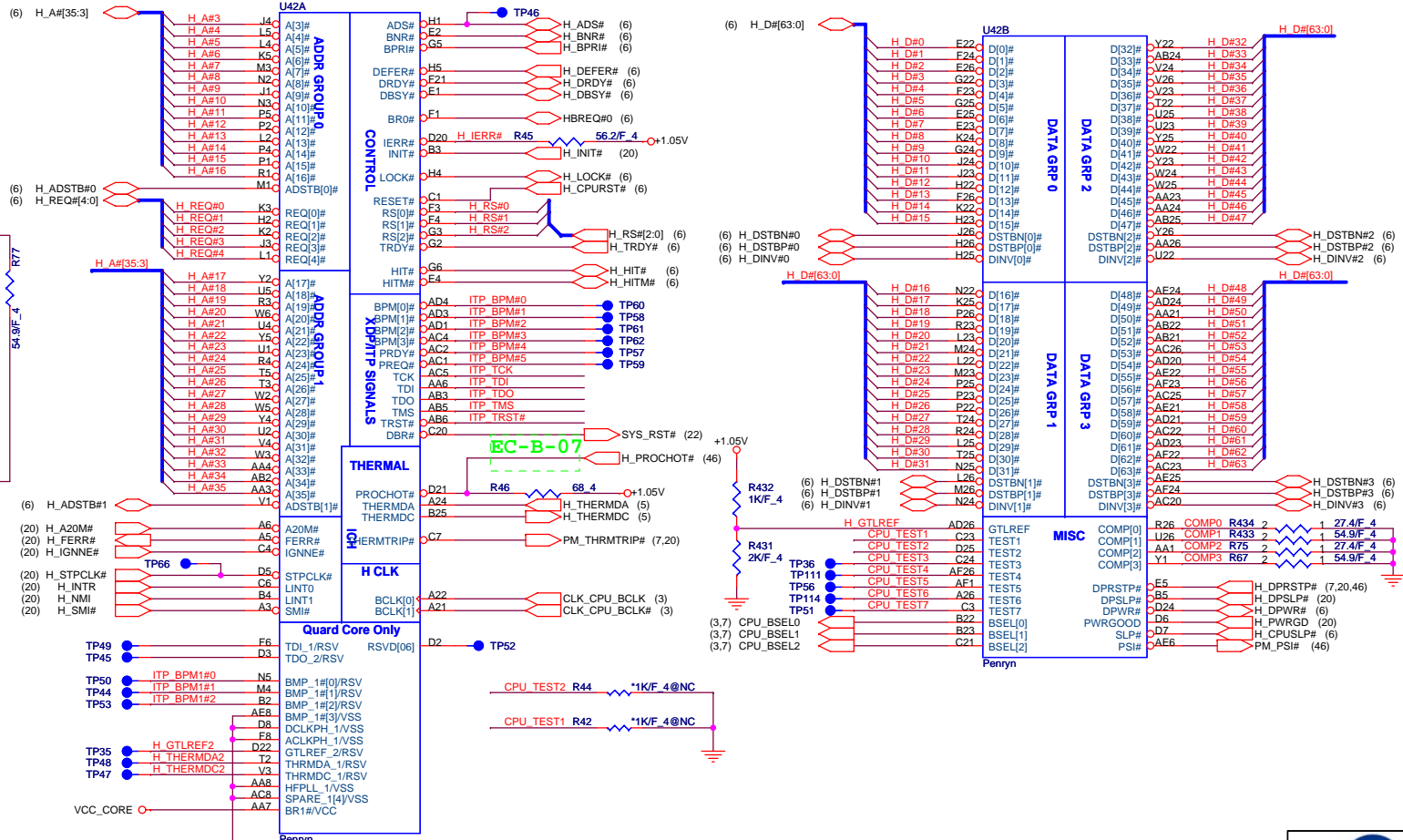
**GCLK\_SEL = FCTSEL1**


FCTSEL1 (PIN64)	PIN5	PIN6
0	DOT96	DOT96#
1	27Mout-NSS	27Mout-SS



FSC	FSB	FSA	CPU	SRC	PCI
0	0	0	266.6	100	33
0	0	1	133.3	100	33
0	1	0	200.0	100	33
0	1	1	166.6	100	33
1	0	0	Reserved		
1	0	1	Reserved		
1	1	0	Reserved		
1	1	1	Reserved		

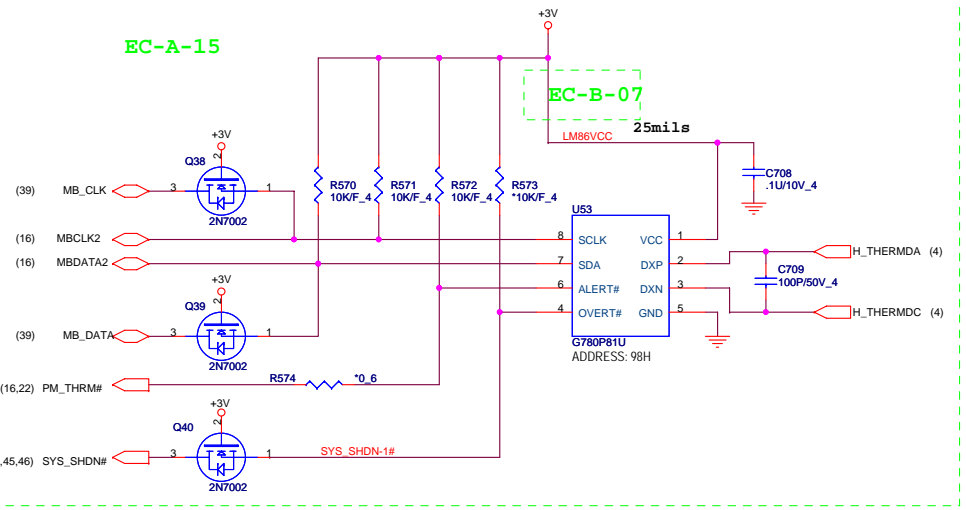
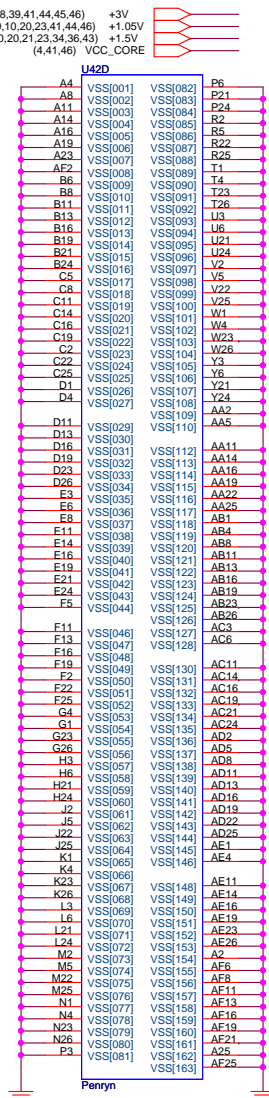
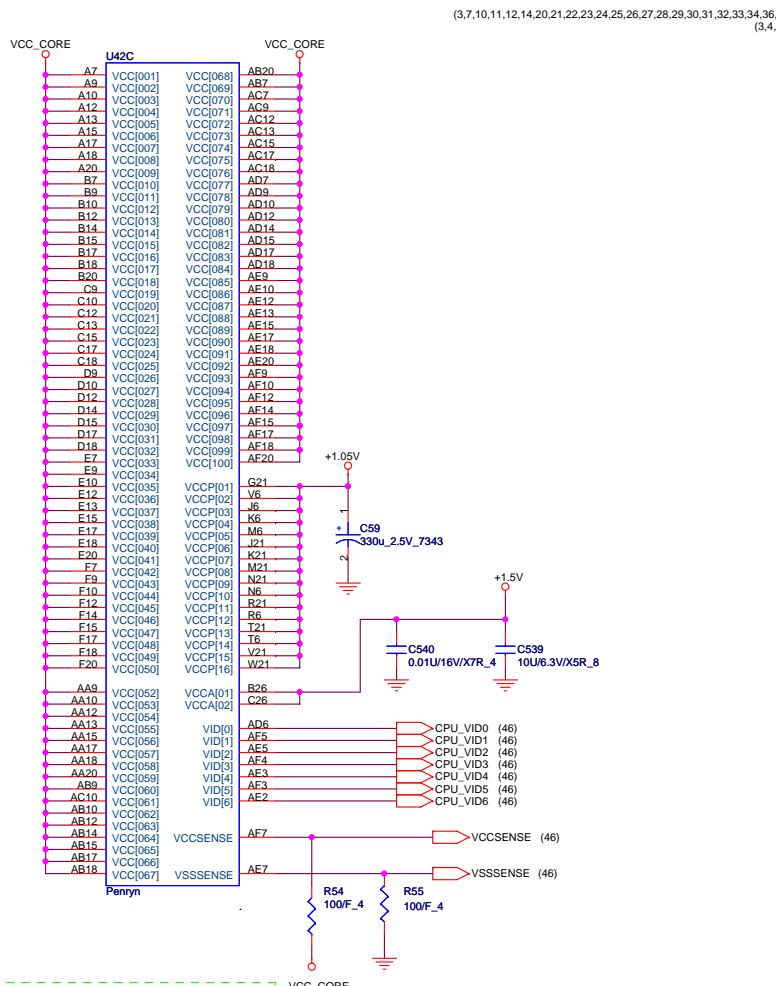
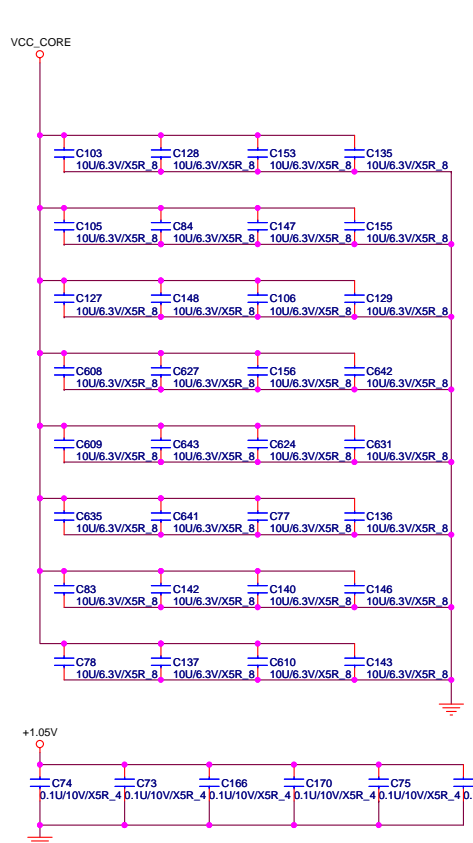






**G-Note Montevina**  
**Quanta Computer Inc.**

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Custom	Penryn 1/2	2A
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MCH\_CFG\_5 DMiX2 selection

- Low: DMiX2
- High: DMiX4 (Default)
- MCH\_CFG\_16 FSB Dynamic ODT
- Low: Dynamic ODT disabled
- High: Dynamic ODT enabled (Default)
- MCH\_CFG\_9 PCI Express Graphic Lane
- Low: Reverse Lane
- High: Normal operation(Default)
- MCH\_CFG\_19 DMI Lane Reversal
- Low: Normal (Default)
- High: Lane Reserved

MCH\_CFG\_6 TPM Host Interface

- Low: TPM Host Interface enabled
- High: TPM Host Interface disabled (Default)

MCH\_CFG\_7 Intel (R) Management Engine Crypto

- Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
- High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)

MCH\_CFG\_10 PCIe Lookback Enable

- Low: Enabled
- High: Disabled (Default)

MCH\_CFG\_12 XOR/ALL/CLOCK Un-gating

- Low: XOR Mode enabled
- High: All-Z Mode enabled (Default)

MCH\_CFG\_13 MCH\_CFG\_12 Configuration

0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

MCH\_CFG\_15 MCH\_CFG\_12 Configuration

0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

MCH\_CFG\_17 MCH\_CFG\_12 Configuration

0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

MCH\_CFG\_19 MCH\_CFG\_12 Configuration

0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

MCH\_CFG\_21 MCH\_CFG\_12 Configuration

0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

MCH\_CFG\_23 MCH\_CFG\_12 Configuration

0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

MCH\_CFG\_25 MCH\_CFG\_12 Configuration

0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

MCH\_CFG\_27 MCH\_CFG\_12 Configuration

0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

MCH\_CFG\_29 MCH\_CFG\_12 Configuration

0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

MCH\_CFG\_31 MCH\_CFG\_12 Configuration

0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

MCH\_CFG\_33 MCH\_CFG\_12 Configuration

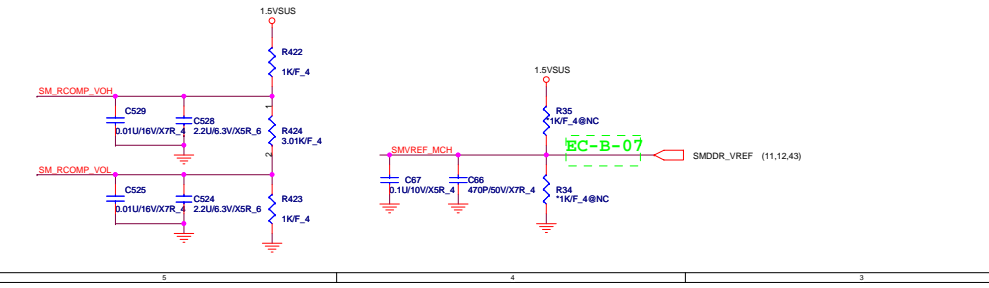
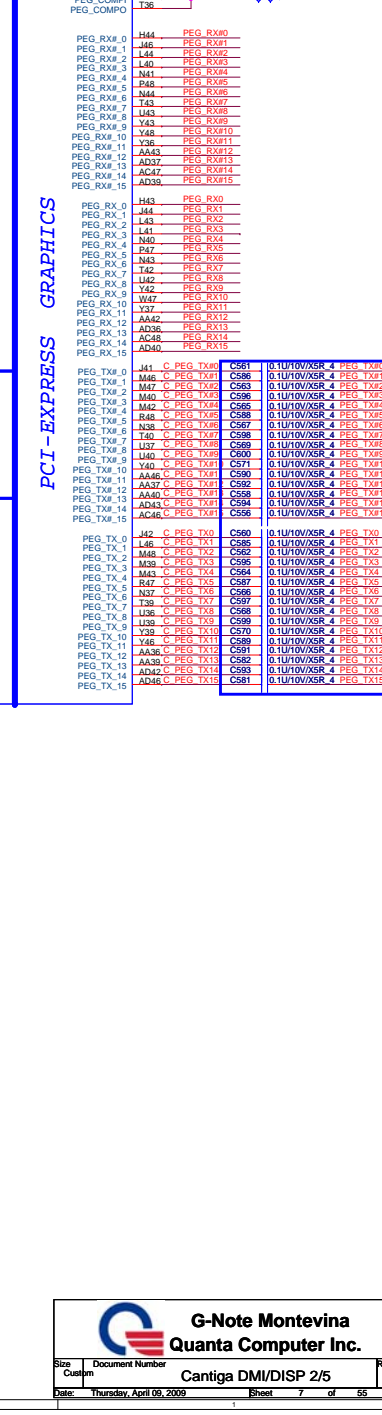
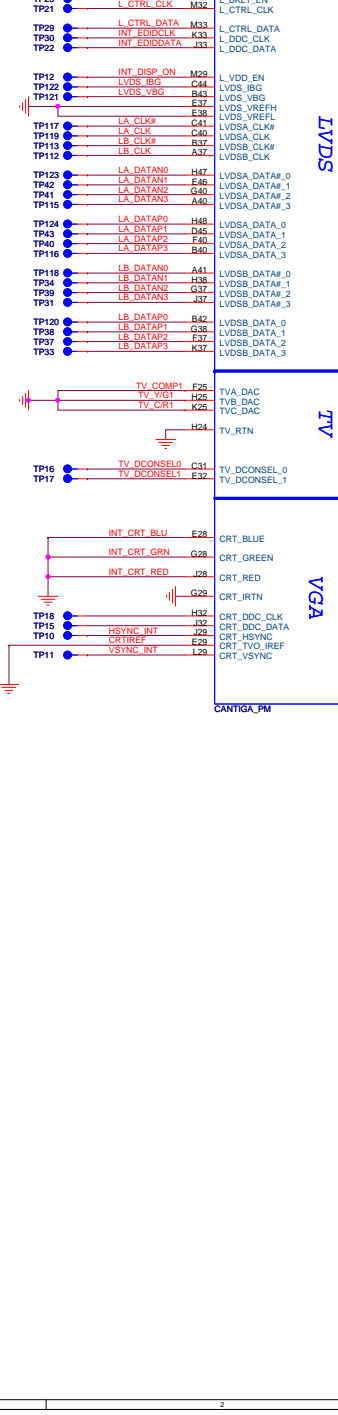
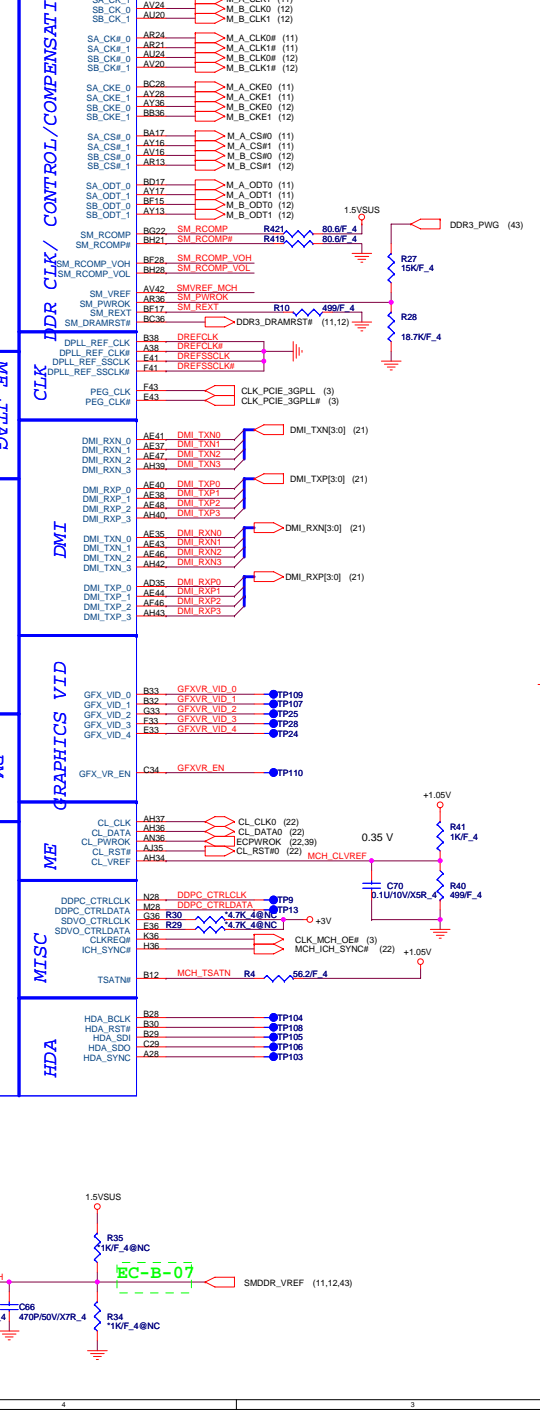
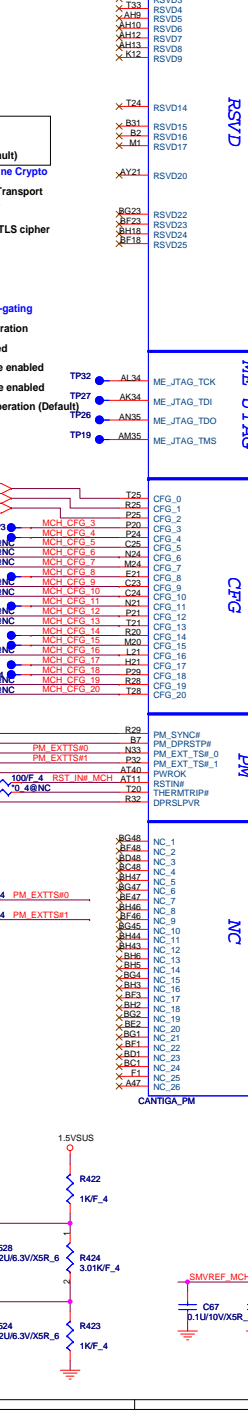
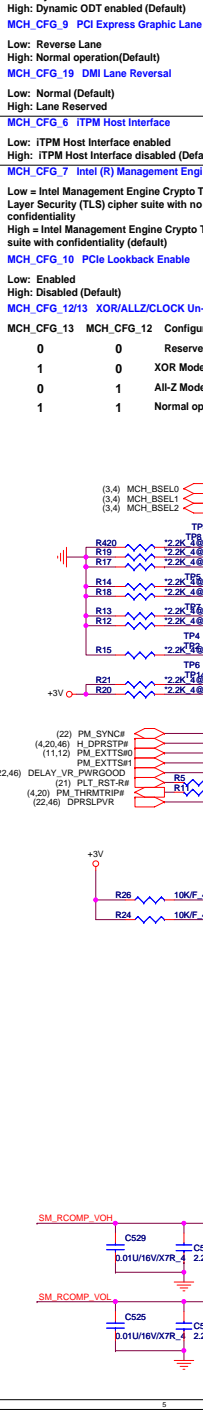
0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

MCH\_CFG\_35 MCH\_CFG\_12 Configuration

0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

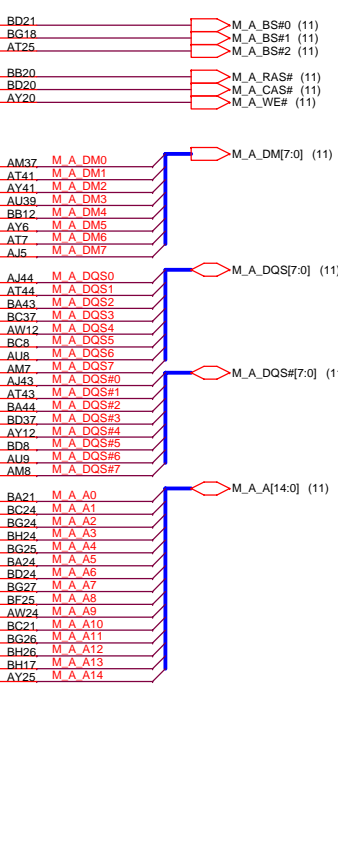
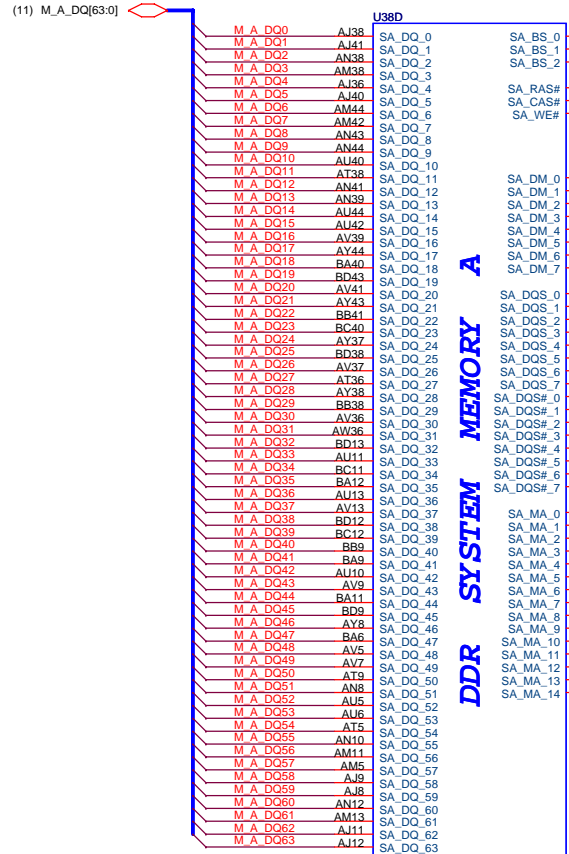
MCH\_CFG\_37 MCH\_CFG\_12 Configuration

0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)



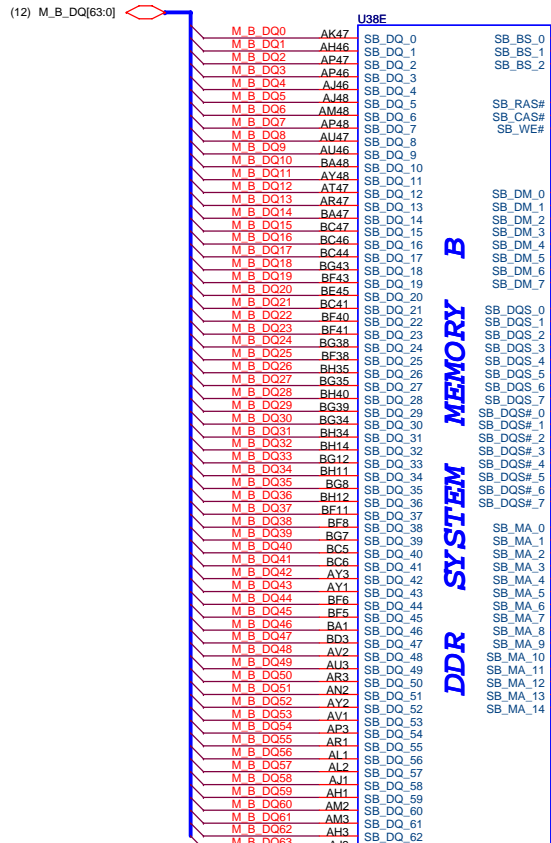
**G-Note Montevina**  
**Quanta Computer Inc.**

Size: Custom Document Number: CANTIGA DM/DISP 2/5 Rev: 2A  
Date: Thursday, April 05, 2009 Sheet: 7 of 55



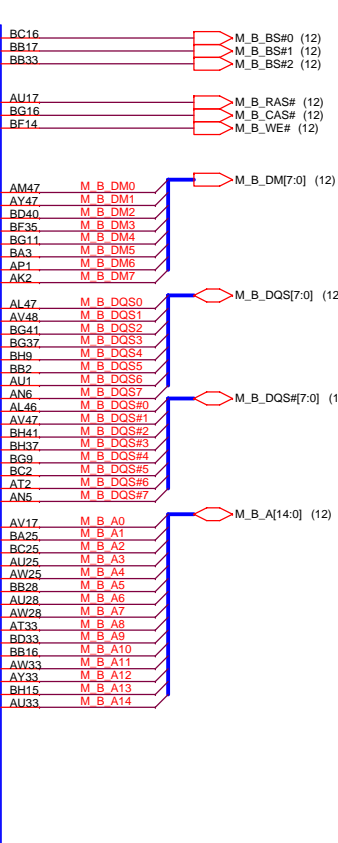
**DDR SYSTEM MEMORY A**

CANTIGA\_PM

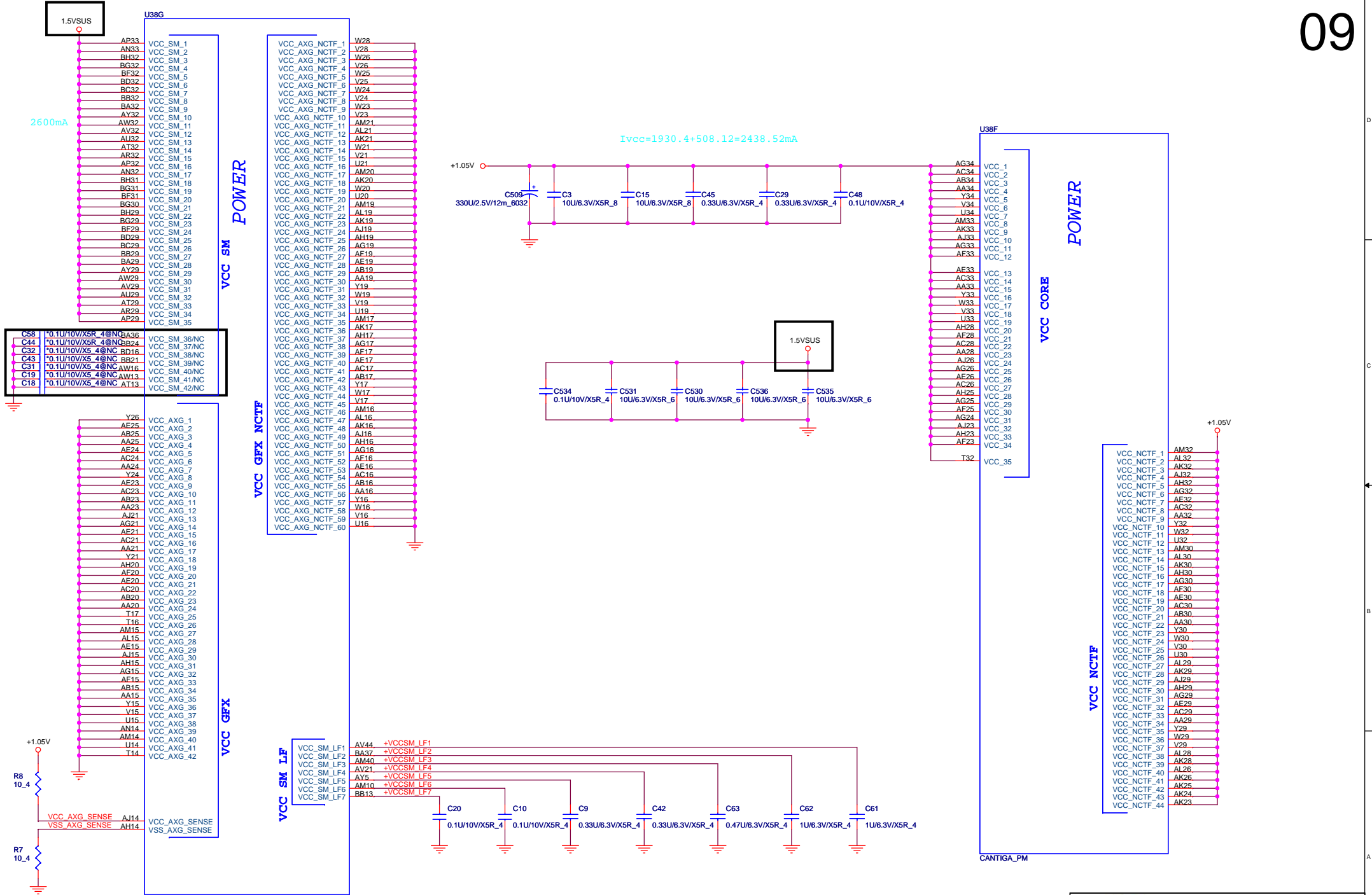


**DDR SYSTEM MEMORY B**

CANTIGA\_PM







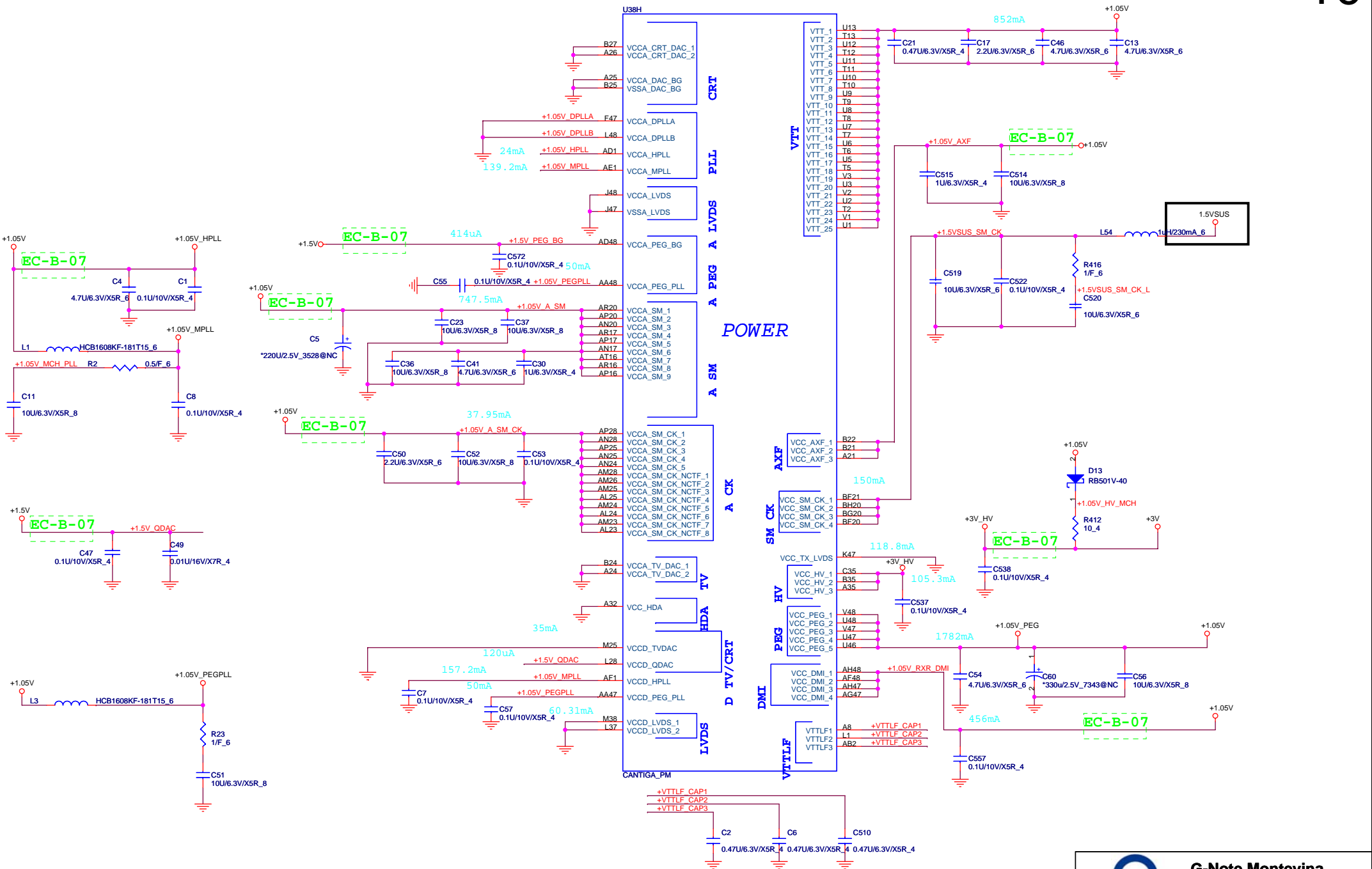
**G-Note Montevina**  
**Quanta Computer Inc.**

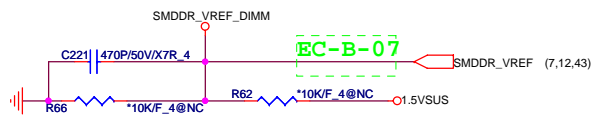
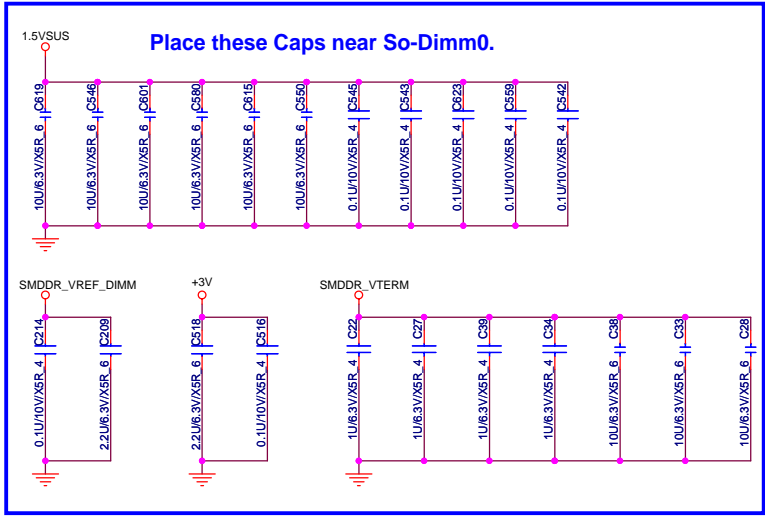
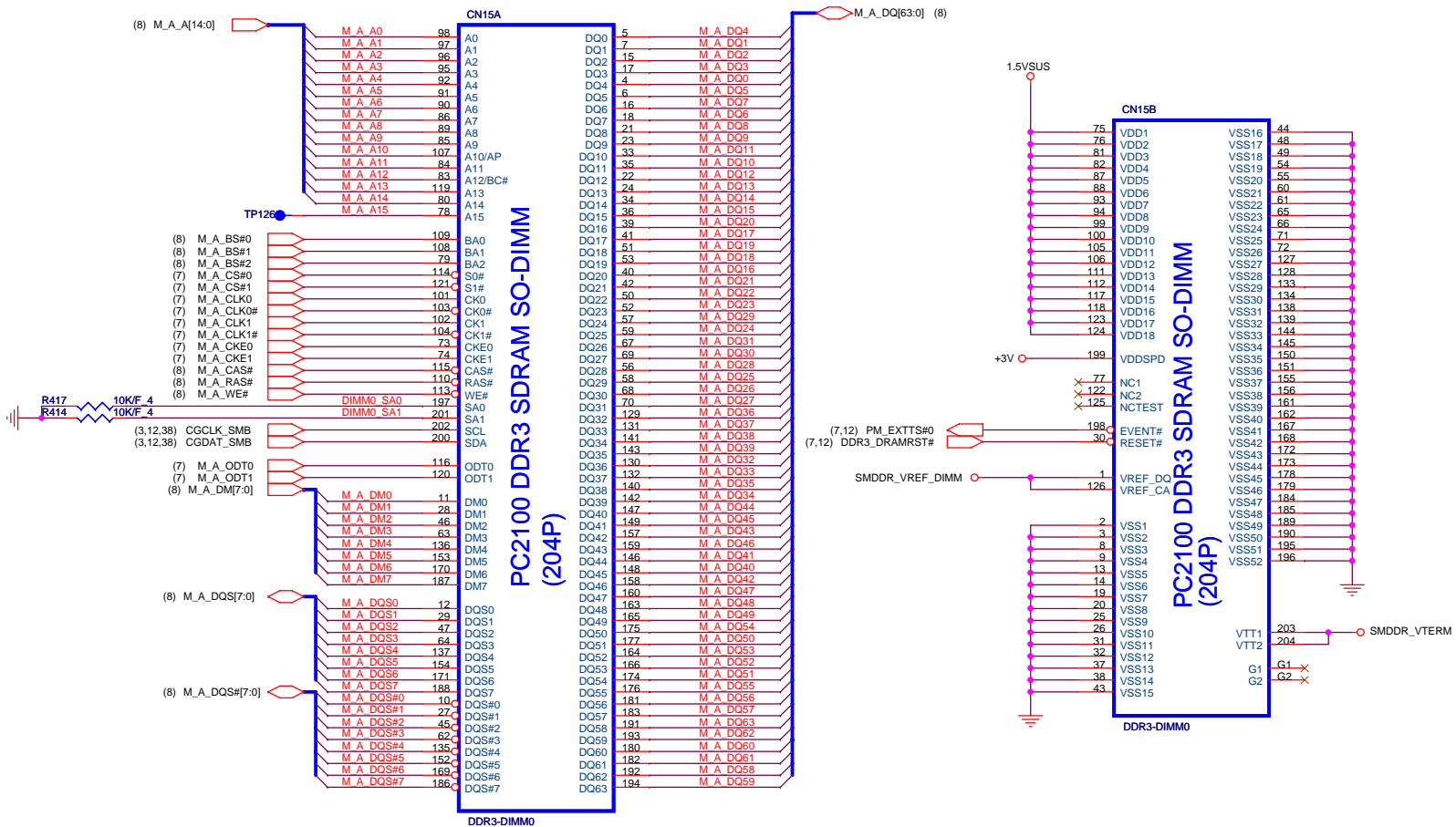
Size: Custom Document Number: Cantiga Vcc 4/5 Rev: 2A  
 Date: Thursday, April 09, 2009 Sheet: 9 of 55

(7,10,11,12,41,43,47) 1.5VSUS  
 (3,4,5,6,7,10,20,23,41,44,46) +1.05V



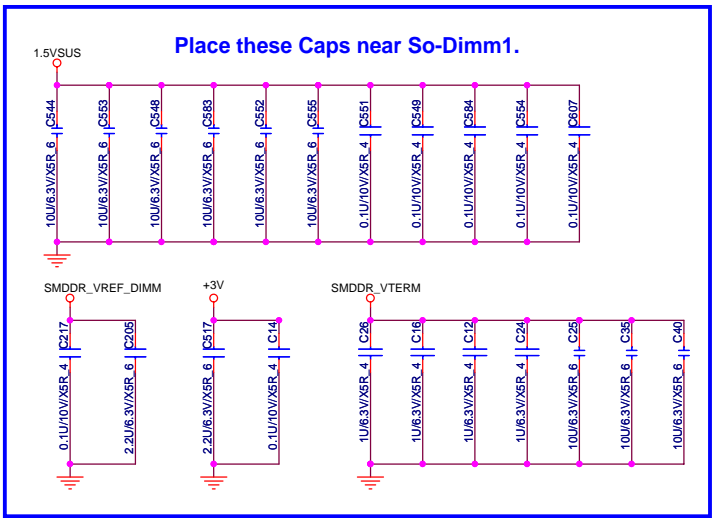
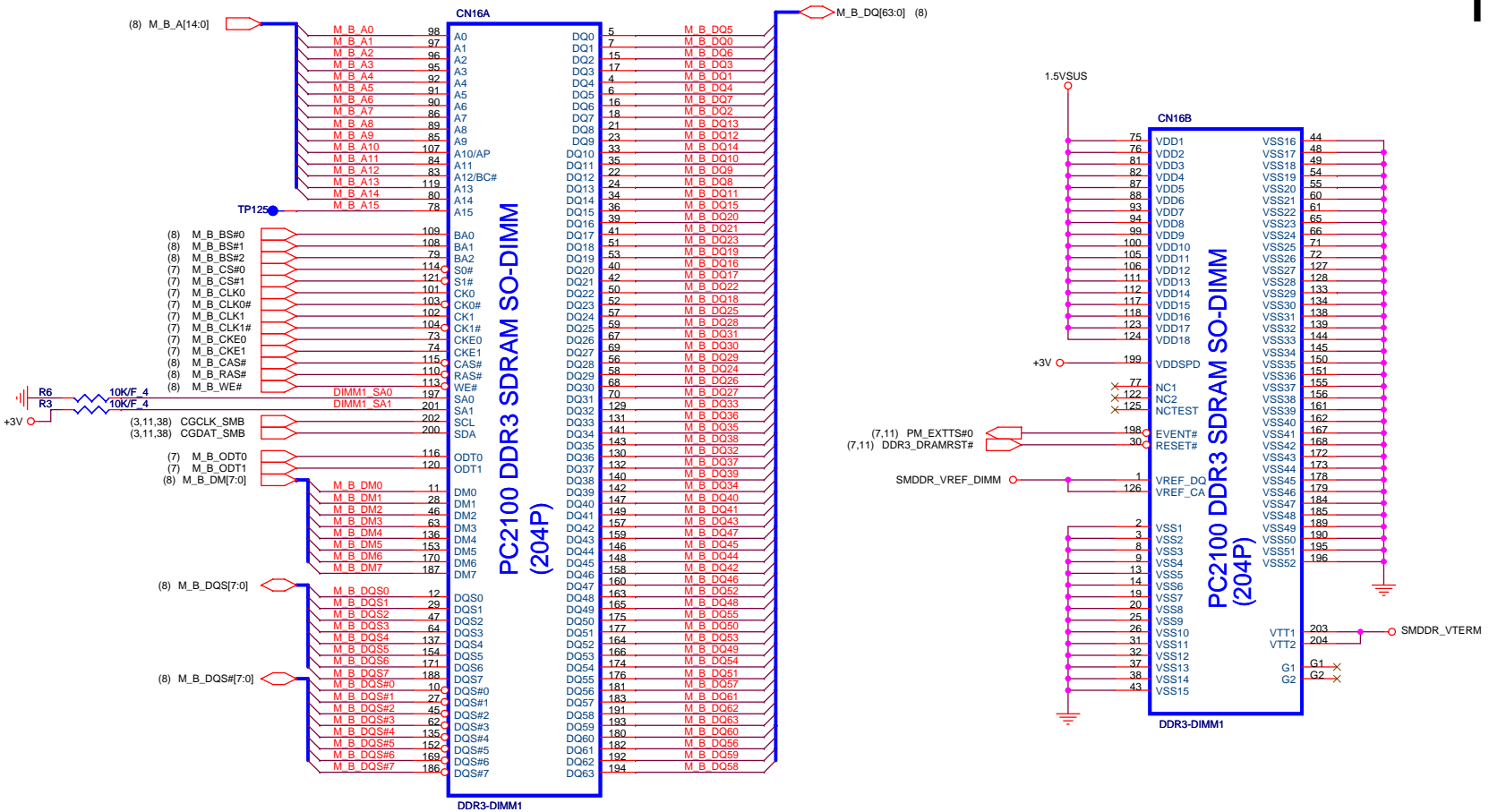
+1.05V (3,4,5,6,7,9,20,23,41,44,46)  
 +3V (3,5,7,11,12,14,20,21,22,23,24,25,26,27,28,29,30,31,32,33,34,36,37,38,39,41,44,45,46)  
 +1.5V (5,20,21,23,34,36,43)  
 +1.05V\_PEG (3,4,5,6,7,9,20,23,41,44,46)





**G-Note Montevina**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	DDR3 DIMM-0(H=5.2)	2A
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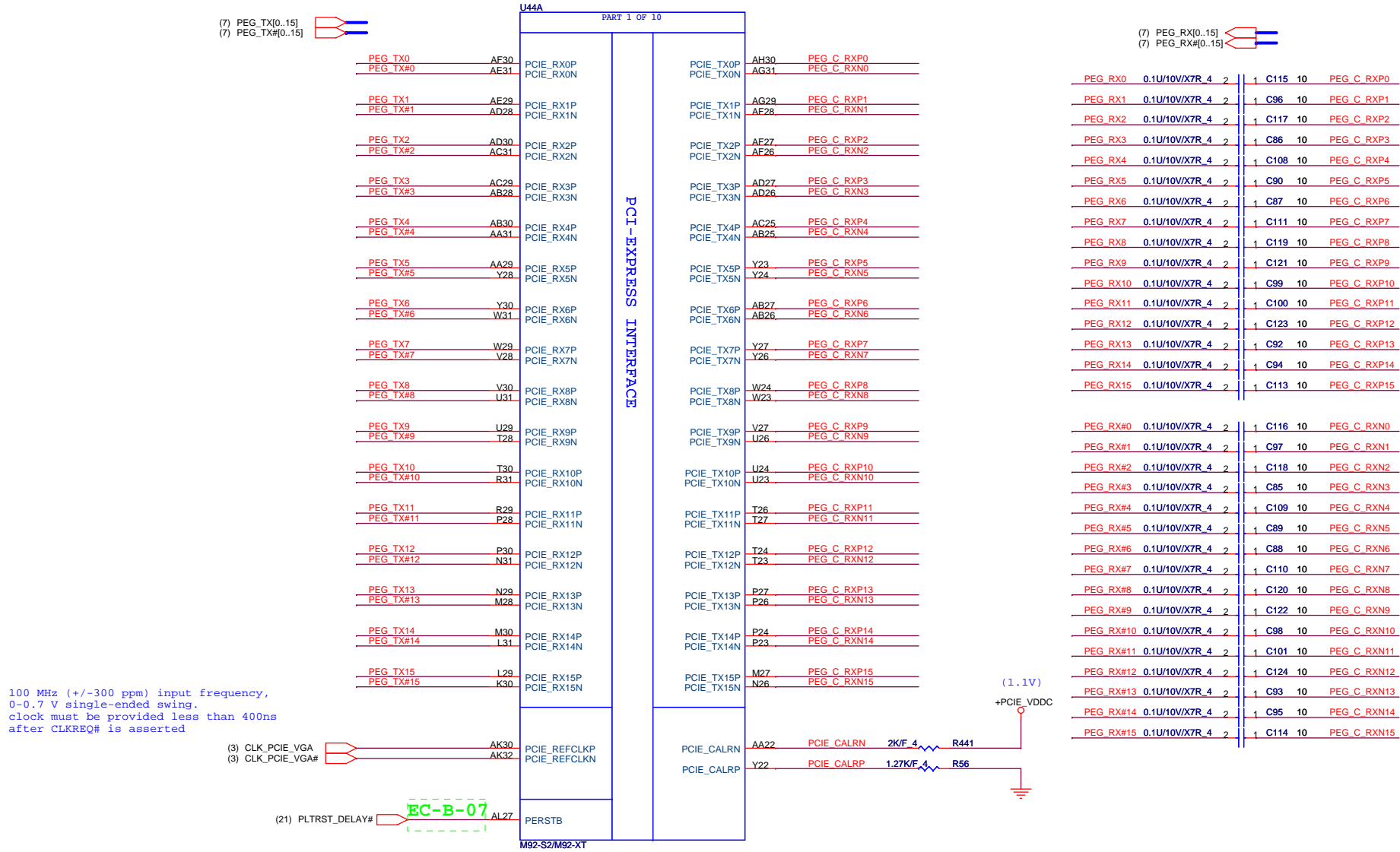


**G-Note Montevina**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	DDR3 DIMM-1(H=9.2)	2A
Date:	Thursday, April 09, 2009	Sheet 12 of 55

(7) PEG\_TX[0..15]  
 (7) PEG\_TX#(0..15)

(7) PEG\_RX[0..15]  
 (7) PEG\_RX#(0..15)

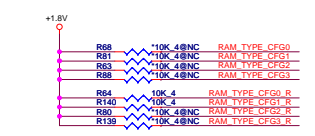


MEMORY APERTURE SIZE SELECT			
MEMORY SIZE	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	0	0	0
256MB	0	0	1
64MB	0	1	0

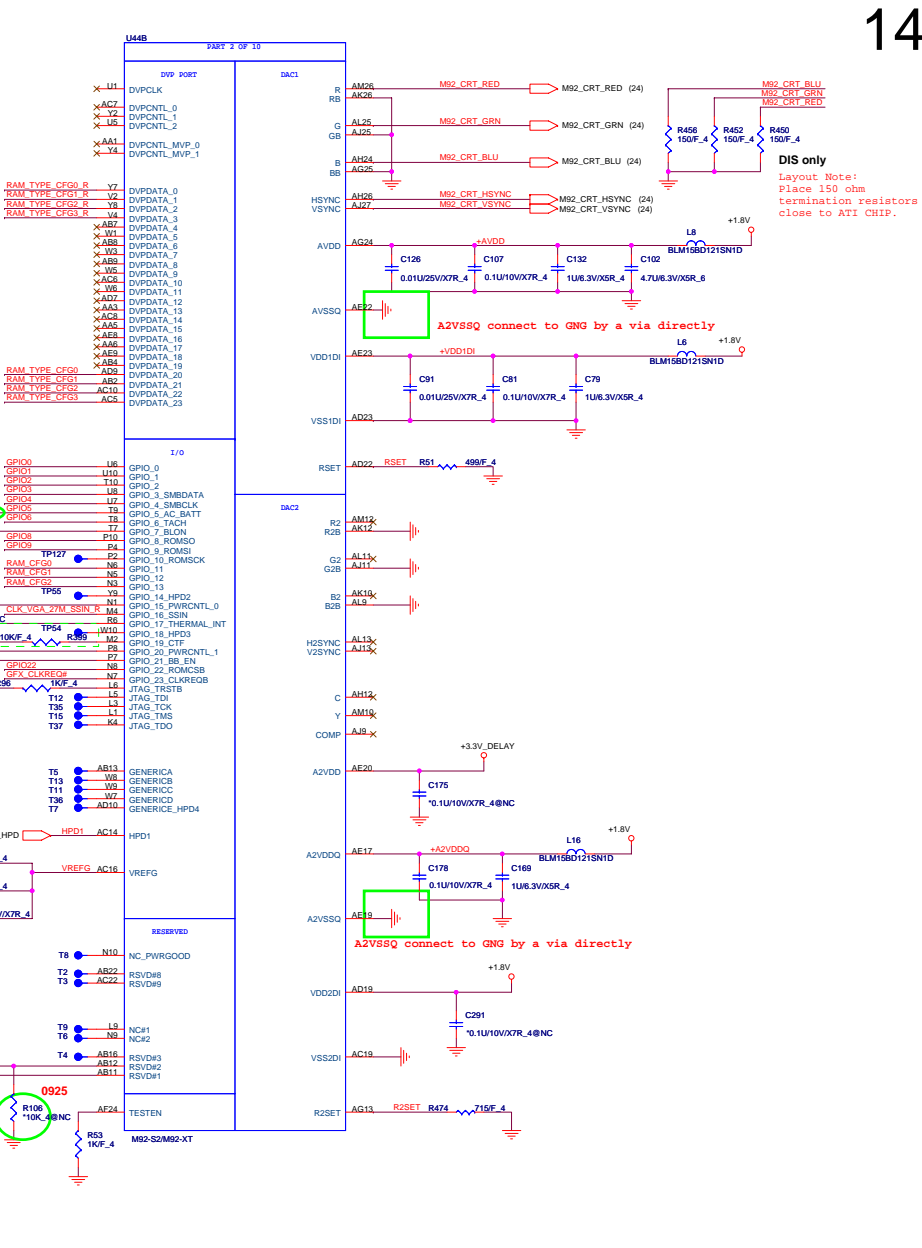
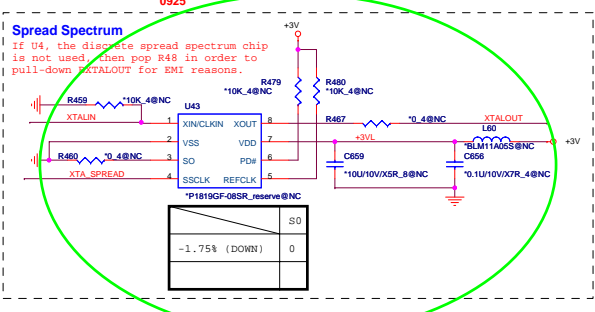
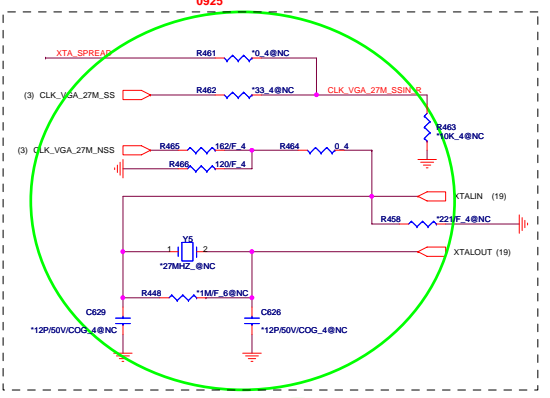
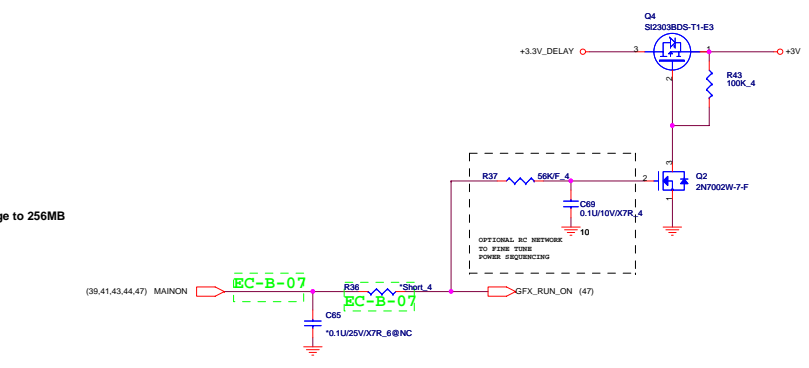
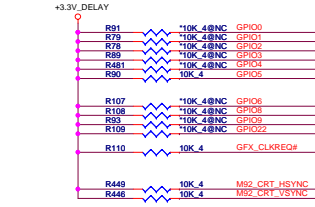
Remove 512MB



Memory Straps	RAM_TYPE_CFG3_R	RAM_TYPE_CFG2_R	RAM_TYPE_CFG1_R	RAM_TYPE_CFG0_R
900MHz 128MB(32M*32) Hynix H5RS1H23MFR11C	0	0	0	0
900MHz 128MB(32M*32) Qimonda HYB18H1G321AF-11	0	0	0	1
900MHz 128MB(32M*32) Qimonda HYB18H1G321A2F-11	0	0	1	1
800MHz 128MB(32M*32) Samsung K4J10324QD-HC12	0	1	0	0



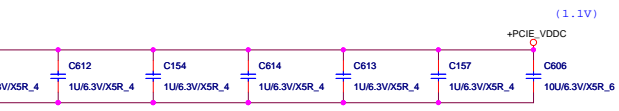
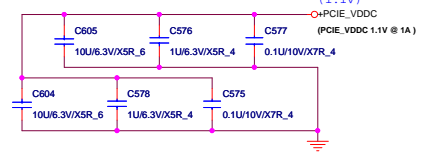
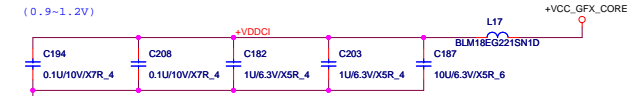
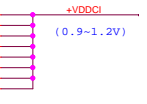
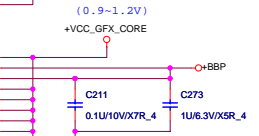
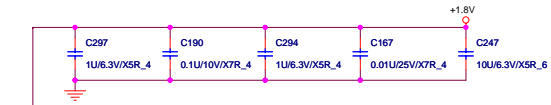
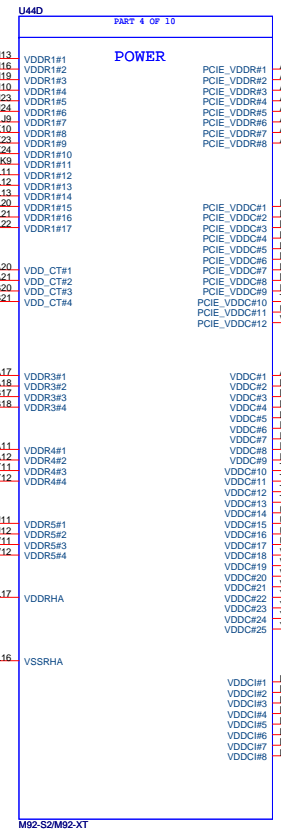
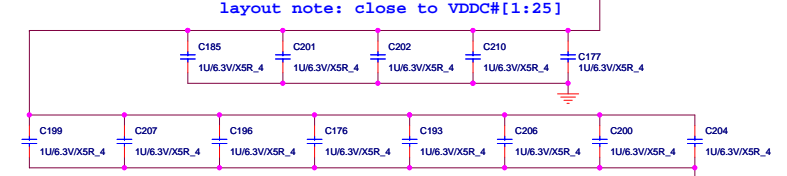
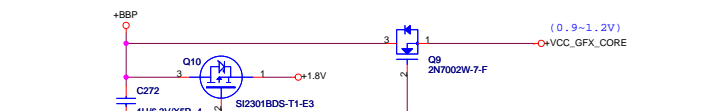
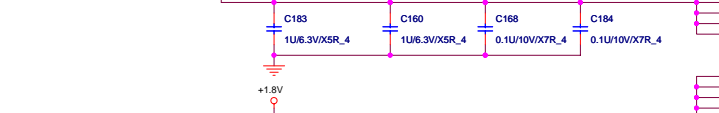
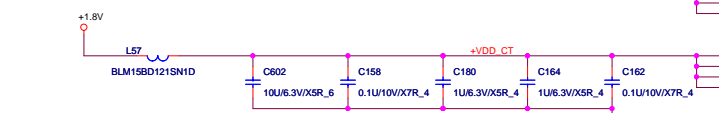
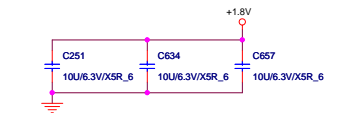
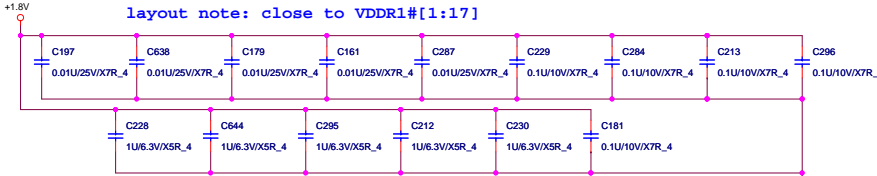
GPIO Straps table	DESCRIPTION OF DEFAULT SETTINGS	G NOTE Setting
GPIO0	GPIO0 - Tx, PWR5, ENB (Transmitter Power Swings Enable) 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
GPIO1	GPIO1 - Tx, DEEMPH, EN (Transmitter Deemphasis Enable) 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	0
GPIO2	GPIO2 - BIF, GEN2, EN (S.6 GTfs Enable) 0: Default (Driver Controlled Gen2) 1: Strap Controlled Gen2	0
GPIO3	ATI reserved configuration straps.	0
GPIO4	ATI reserved configuration straps.	0
GPIO5	GPIO_5_AC_BATT 0: Battery saving mode = 0.0 V 1: AC (Performance mode) = 3.3 V	1
GPIO6	ATI Internal use only	0
GPIO8	ATI reserved configuration straps.	0
GPIO9	VGA Disable 0 - VGA Controller capacity enabled 1 - The device will not recognized as the system's VGA controller	0
GPIO22	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0
HSYNC	AUD[1:0] 00 - No audio function 01 - Audio for DisplayPort and HDMI if adapter is detected 10 - Audio for DisplayPort only 11 - Audio for both DisplayPort and HDMI	1
VSNC		1



DIS only  
Layout Note:  
Place 150 ohm termination resistors close to ATI CHIP.

Spread Spectrum  
If U4, the discrete spread spectrum chip is not used, then pop R48 in order to pull-down XTALOUT for EMI reasons.

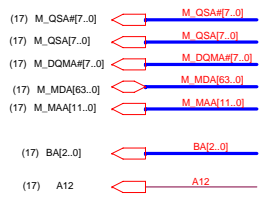
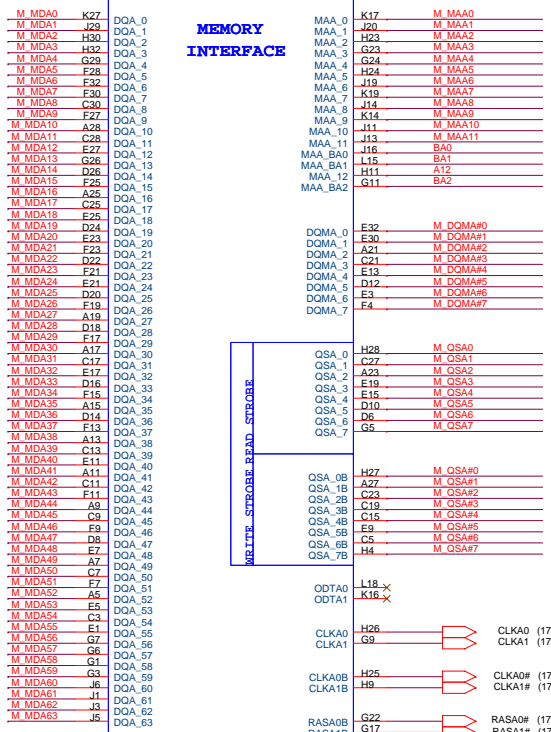




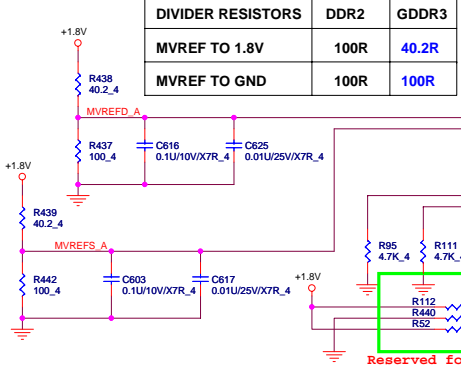
# MEMORY INTERFACE

U44C PART 3 OF 10

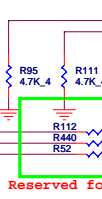
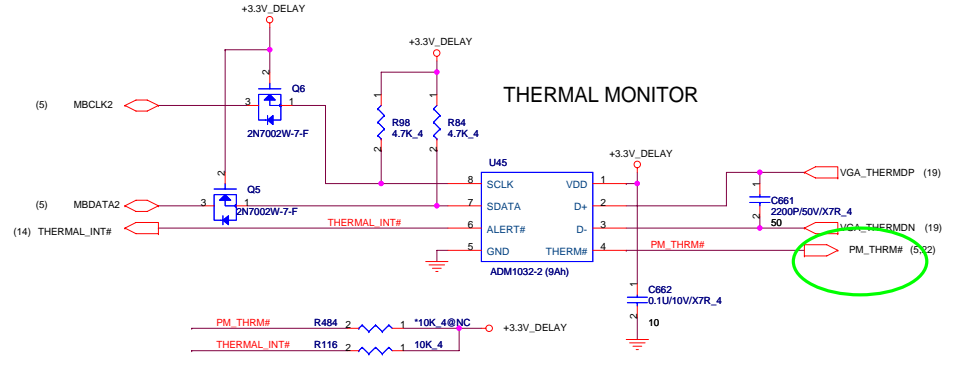
## MEMORY INTERFACE



DIVIDER RESISTORS	DDR2	GDDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R



WRITE STROBE PLEAD STORE

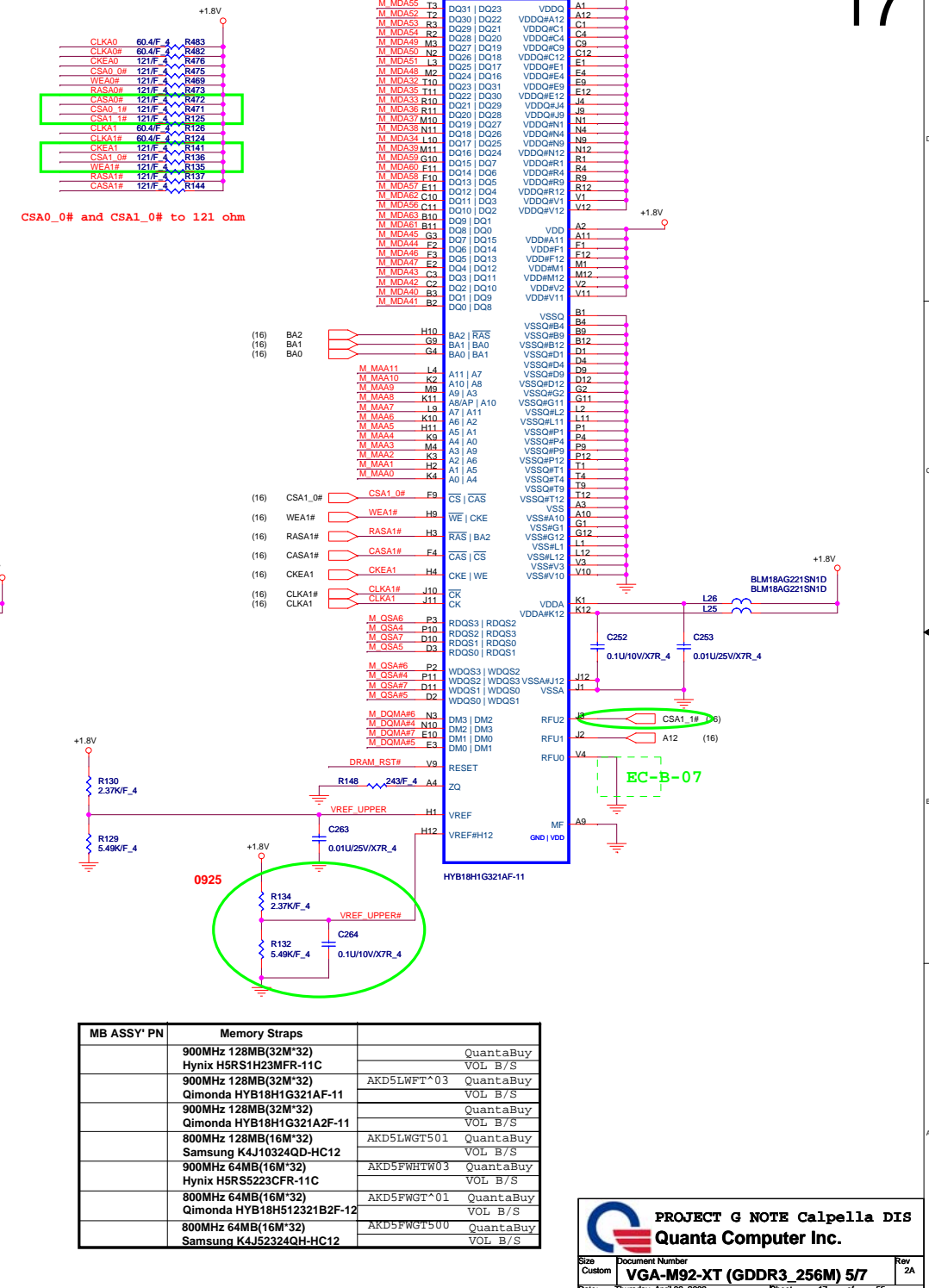
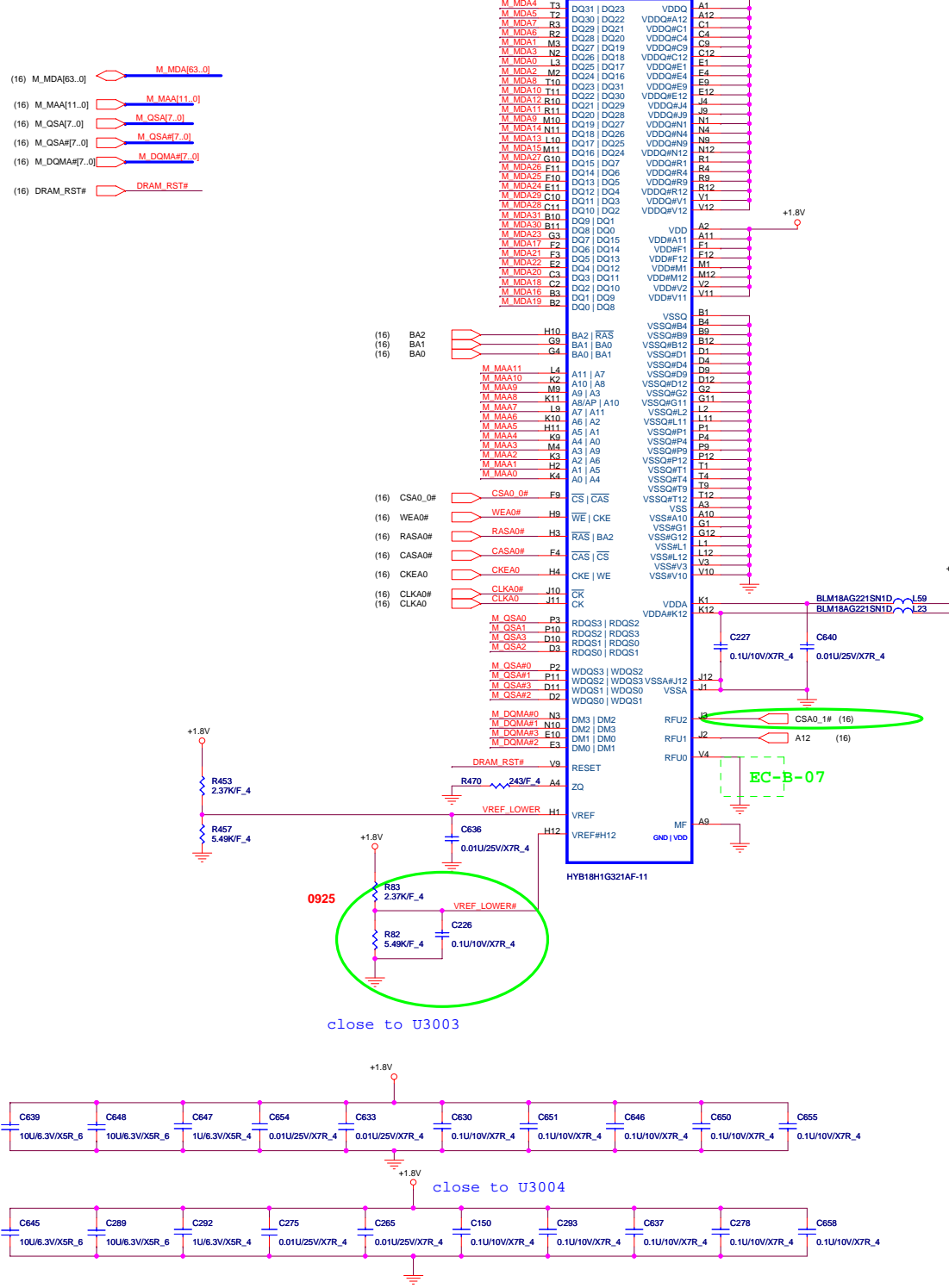


Reserved for future ASIC

**G-Note Montevina**  
**Quanta Computer Inc.**

Size: Custom Document Number: M92-XT\_MEMORY/THERM Rev: 2A  
Date: Thursday, April 09, 2009 Sheet: 16 of 55

GDDR3

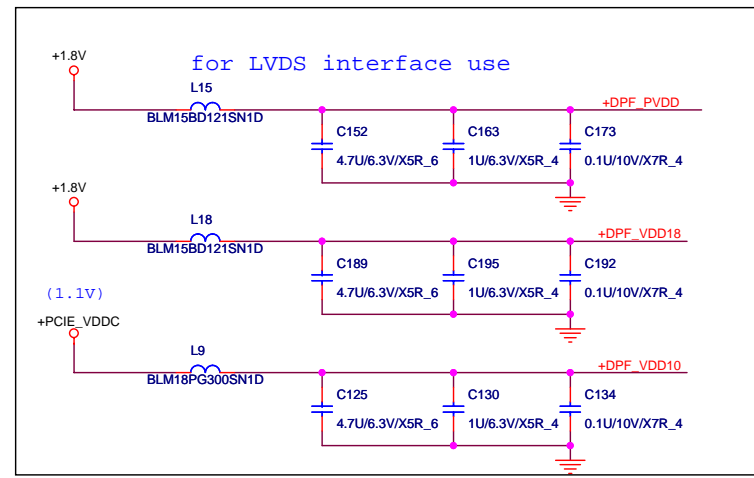
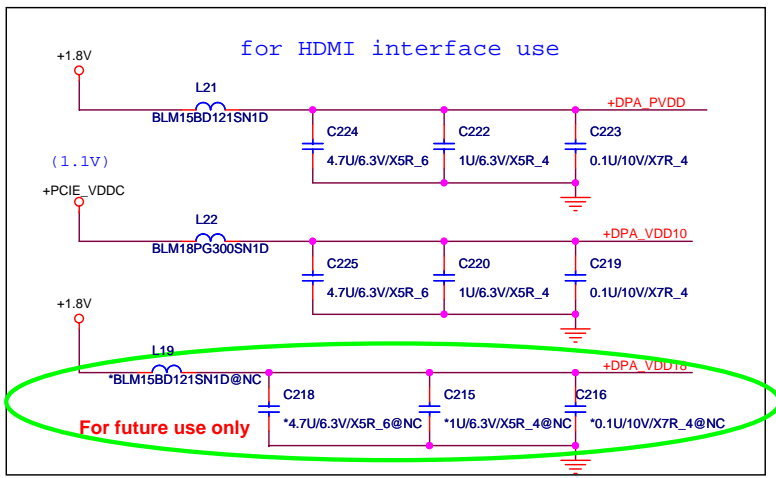
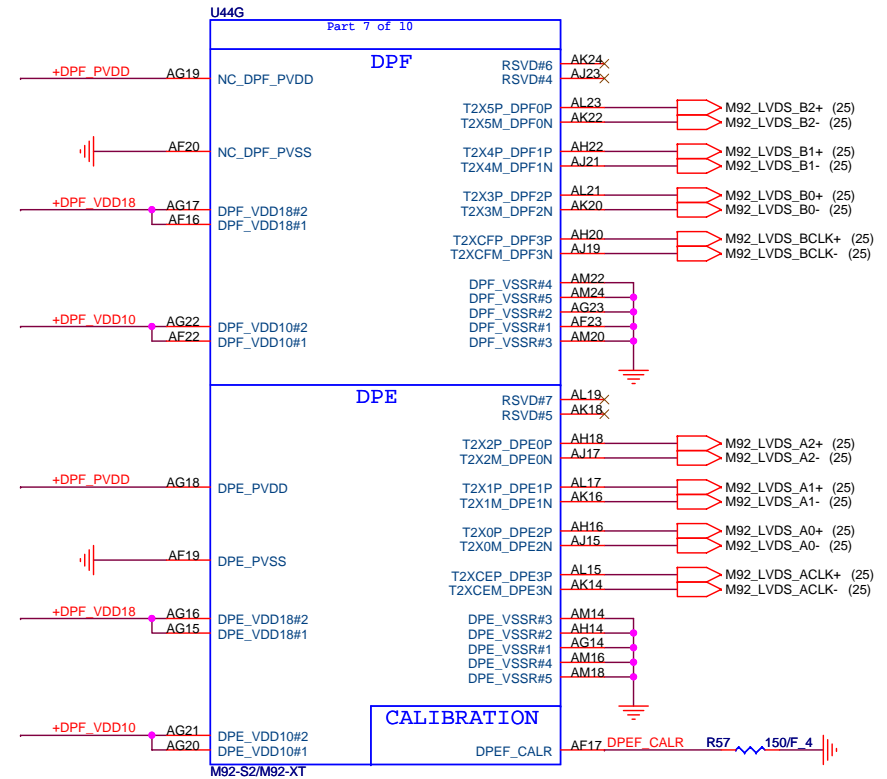
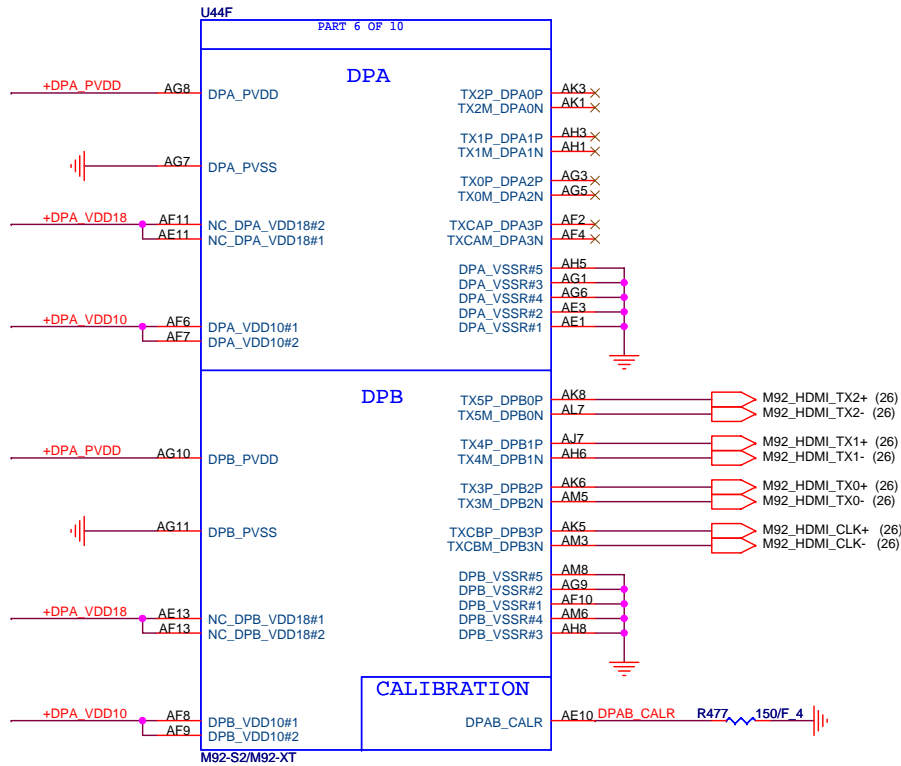


MB ASSY' PN	Memory Straps	
	900MHz 128MB(32M*32)	QuantaBuy
	Hynix H5RS1H23MFR-11C	VOL B/S
	900MHz 128MB(32M*32)	QuantaBuy
	AKD5LWFT^03	VOL B/S
	Qimonda HYB18H1G321AF-11	VOL B/S
	900MHz 128MB(32M*32)	QuantaBuy
	Qimonda HYB18H1G321A2F-11	VOL B/S
	800MHz 128MB(16M*32)	AKD5LWGT501
	Samsung K4J10324QD-HC12	VOL B/S
	900MHz 64MB(16M*32)	AKD5FWHTW03
	Hynix H5RS5223CFR-11C	VOL B/S
	800MHz 64MB(16M*32)	AKD5FWGT^01
	Qimonda HYB18H512321B2F-12	VOL B/S
	800MHz 64MB(16M*32)	AKD5FWGT^500
	Samsung K4J5224QH-HC12	VOL B/S

**PROJECT G NOTE Calpella DIS**  
**Quanta Computer Inc.**

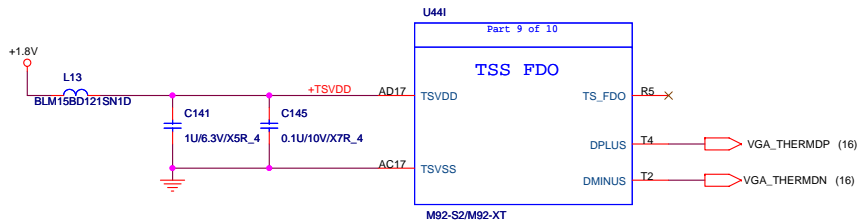
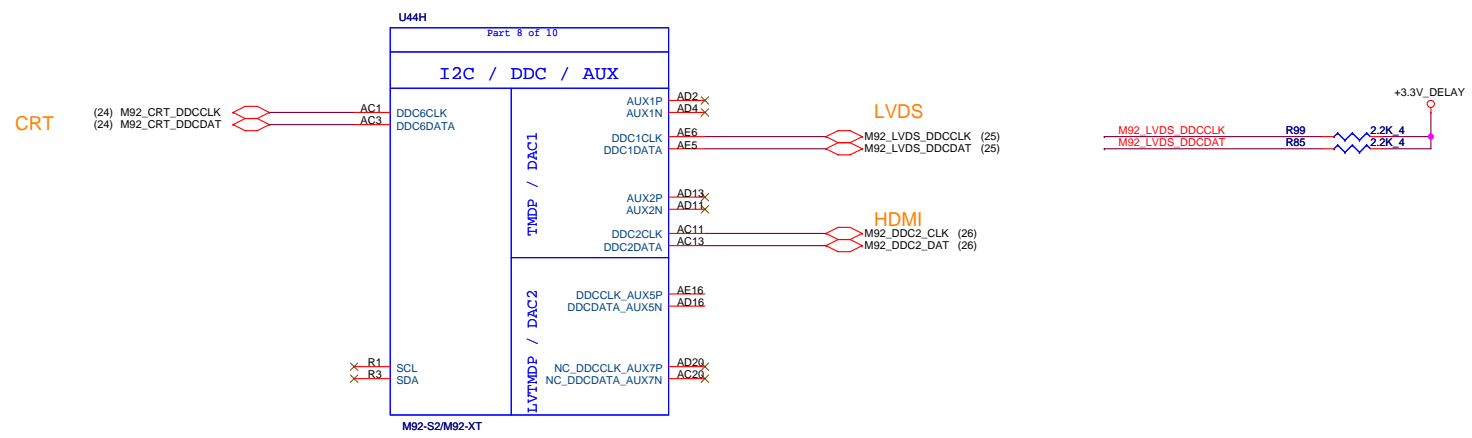
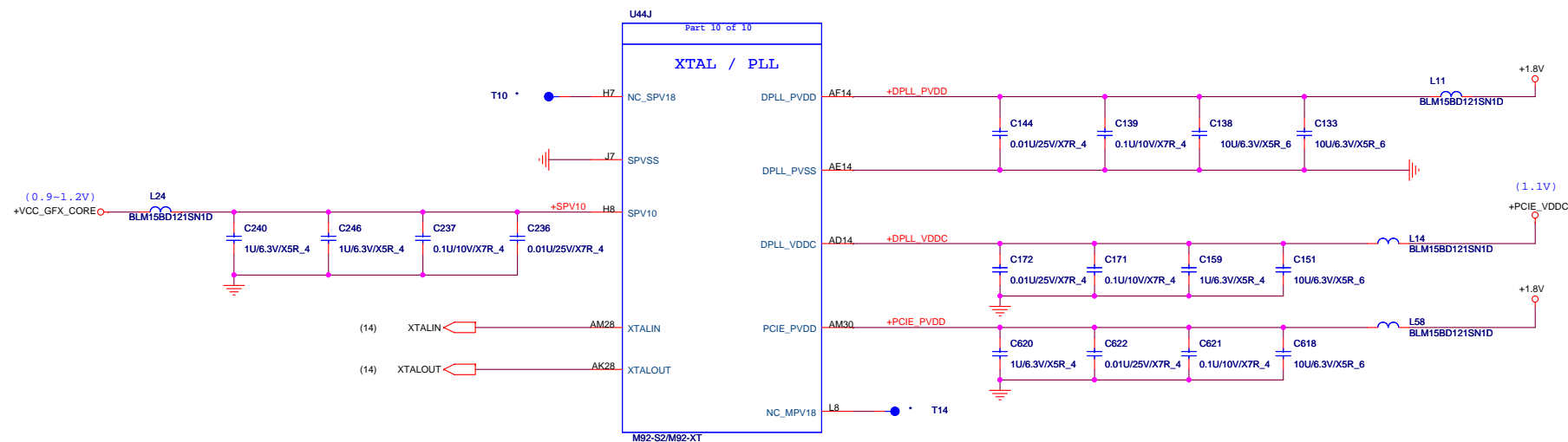
## TMDP(HDMI) INTERFACE

## LVDS INTERFACE

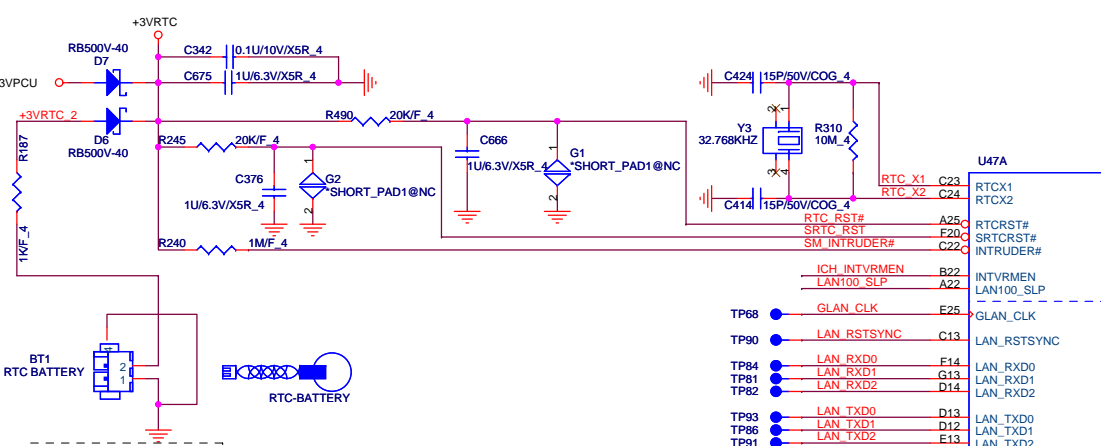


**G-Note Montevina  
Quanta Computer Inc.**

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M92-XT_TMDP I/F		
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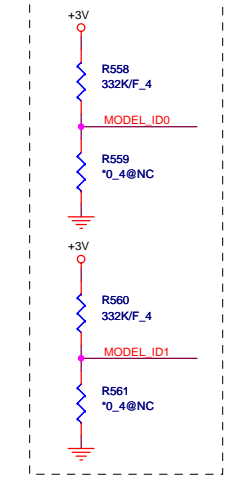


(25,27,29,31,37,39,41,42,45) 3VPCU  
 (23,39) +3VRTC  
 +3V  
 (5,10,21,23,34,36,43) +1.5V  
 (3,4,5,6,7,9,10,23,41,44,46) +1.05V



**MODEL ID**

STRAP	MODEL_ID1	MODEL_ID0
13"	0	0
14"	0	1
15"	1	0

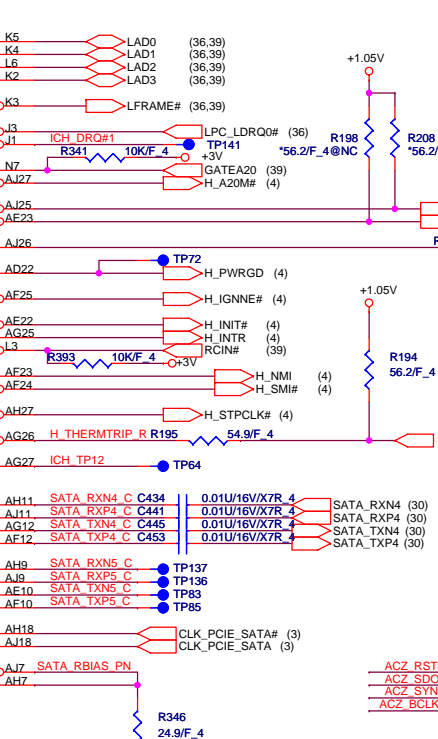
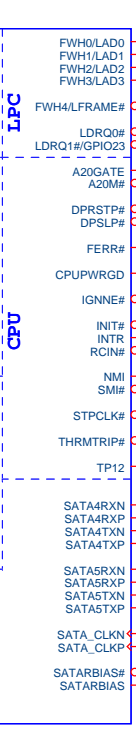
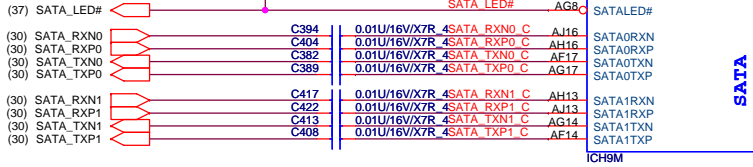


**SATA HDD**

- (37) SATA\_LED#
- (30) SATA\_RXN0
- (30) SATA\_RXP0
- (30) SATA\_TXN0
- (30) SATA\_TXP0

**SATA ODD**

- (30) SATA\_RXN1
- (30) SATA\_RXP1
- (30) SATA\_TXN1
- (30) SATA\_TXP1



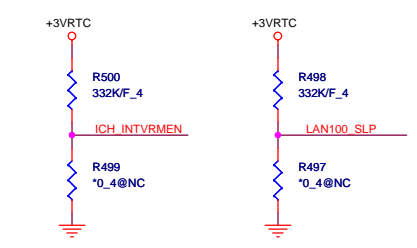
**E-SATA CONNECTOR**



**SB Strap**

**ICH9-M Internal VR Enable strap**  
 (Internal VR for VccSus1\_05, VccSus1\_5 and VccCL1\_5)

**ICH9-M LAN100\_SLP Strap**  
 (Internal VR for VccLAN1\_05 and VccCL1\_05)



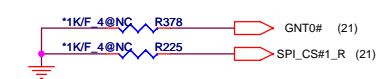
**XOR Chain Entrance Strap**

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

**ICH9 Boot BIOS select**

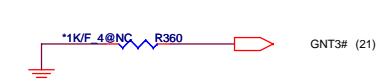
STRAP	PCI_GNT0#	SPL_CS#1
SPI	0	1
PCI	1	0
LPC	1	1

(default)



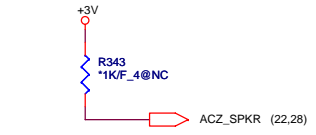
**A16 swap override strap**

PCI_GNT#3	Low = A16 swap override enabled	Hi = Default



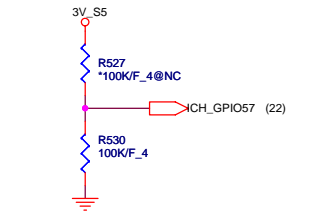
**No Reboot Strap**

ACZ_SPKR	Low: Default	Hi: No reboot



**TPM physical presence**

ICH_GPIO57	Low: Default

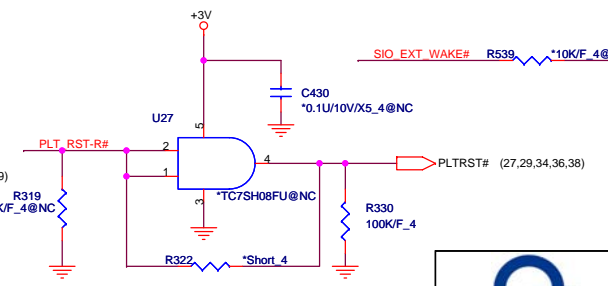
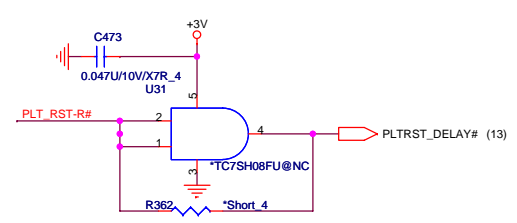
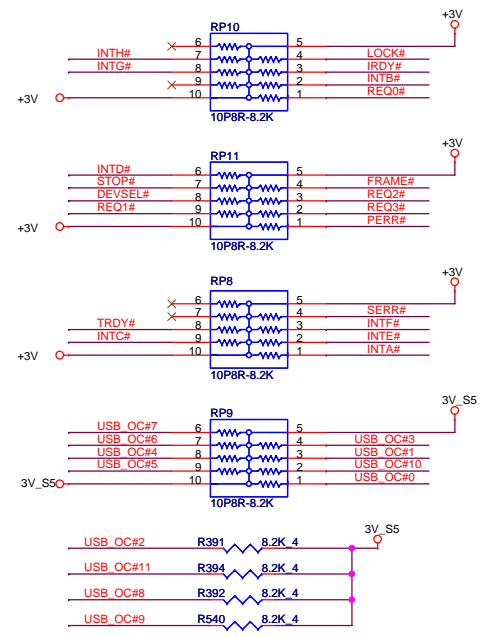
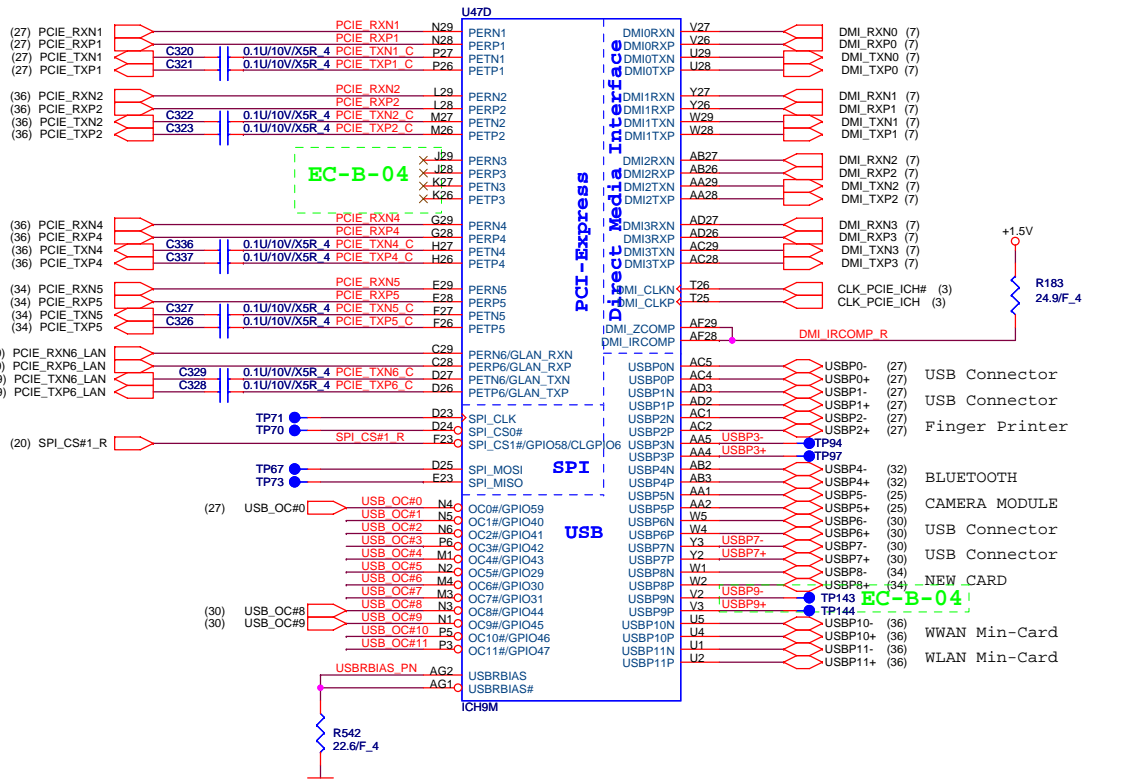




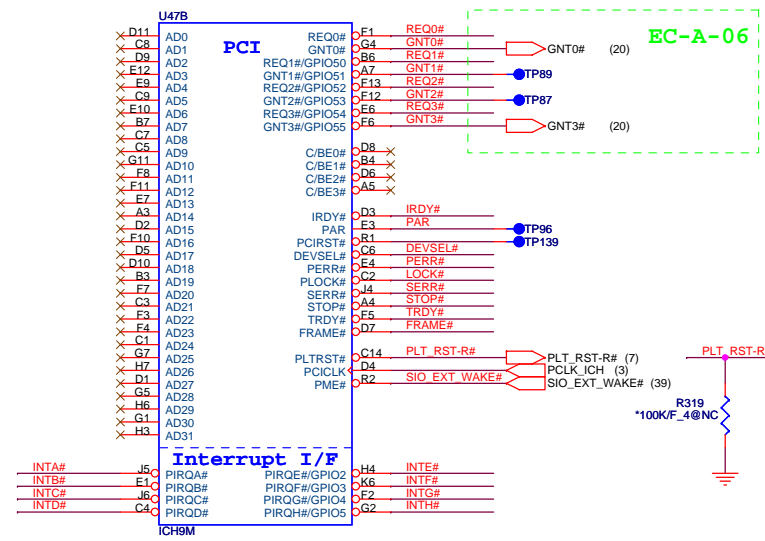
(3,5,7,10,11,12,14,20,22,23,24,25,26,27,28,29,30,31,32,33,34,36,37,38,39,41,44,45,46) +1.5V  
 (22,27,34,39,41,43,46,47) +3V 3VSUS



- CARD-READER
- MINI CARD PCI-E(WWAN)
- MINI CARD PCI-E(WLAN)
- EXPRESS CARD (NEW CARD)
- PCI-E-LAN



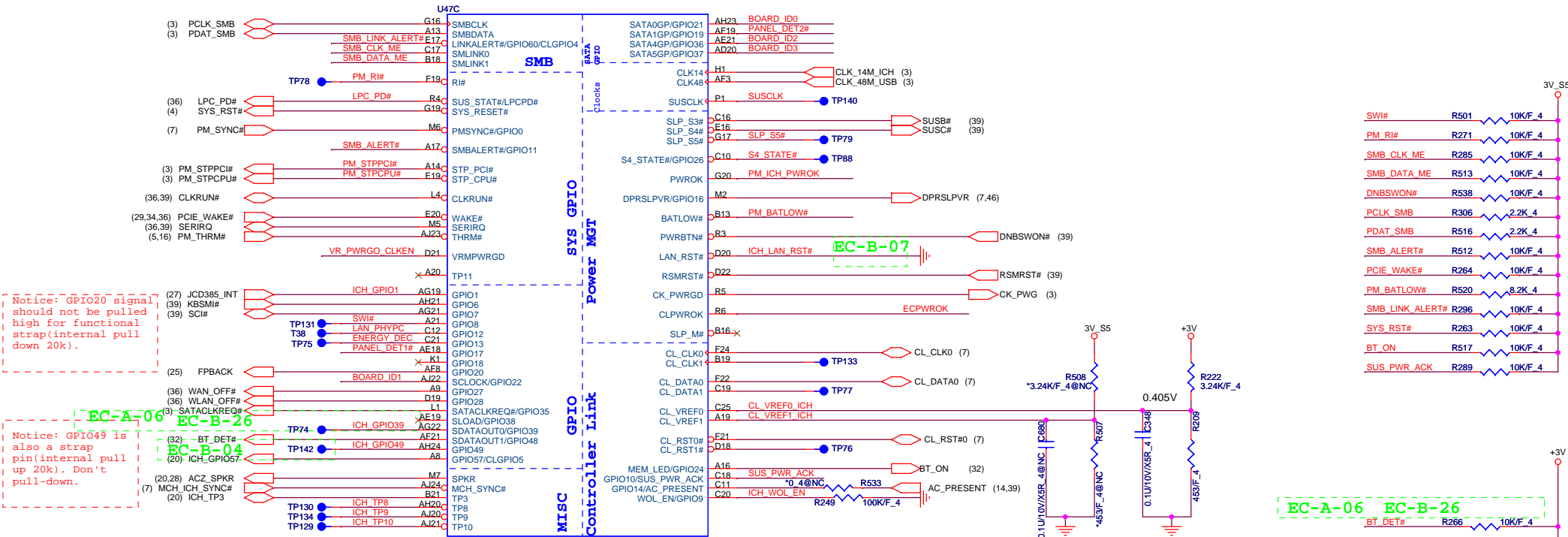
PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD21	INTE#, F#, G#	RICOH R5C847



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**Quanta Computer Inc.**

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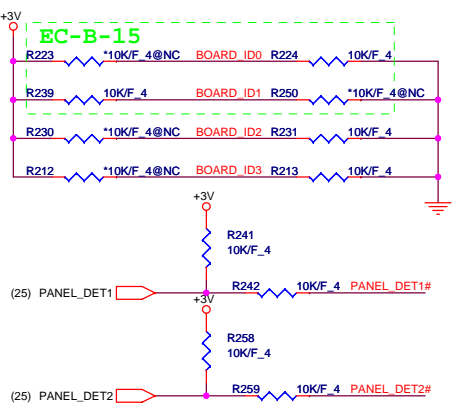
(3,5,7,10,11,12,14,20,21,23,24,25,26,27,28,29,30,31,32,33,34,36,37,38,39,41,44,45,46)  
 (5,10,20,21,23,34,36,43) +1.5V  
 +3V  
 (20,21,23,41) 3V\_S5  
 (21,27,34,39,41,43,46,47) 3VSUS



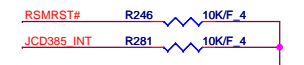
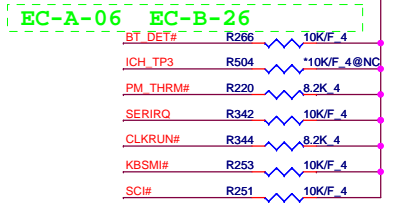
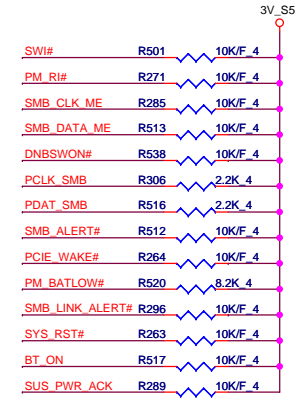
Notice: GPIO20 signal should not be pulled high for functional strap(internal pull down 20k).

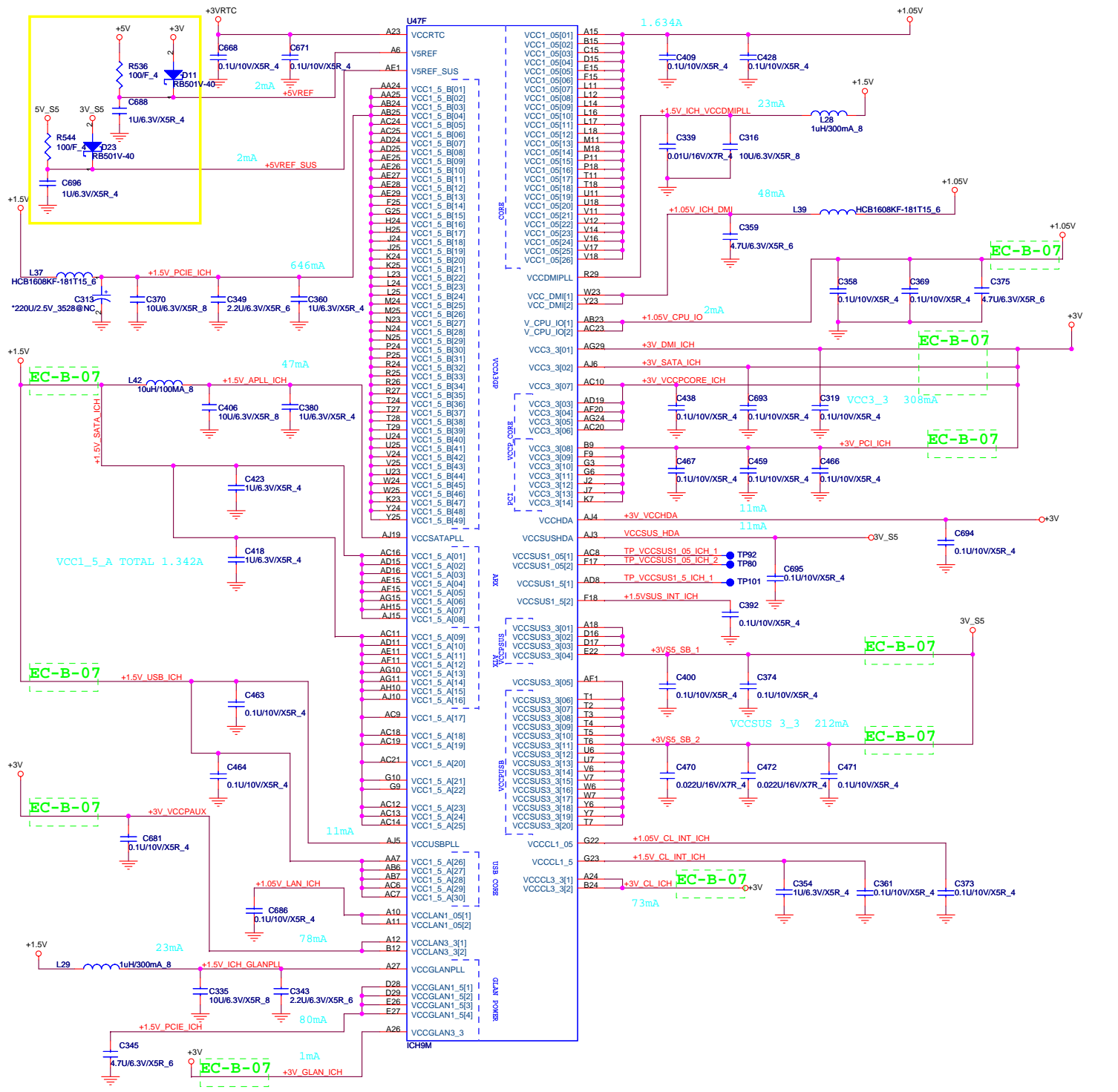
Notice: GPIO49 is also a strap pin(internal pull up 20k). Don't pull-down.

Board ID For Function	ID3 GPIO37	ID2 GPIO36	ID1 GPIO22	ID0 GPIO21
SDV	0	0	0	0
SIV	0	0	0	1
SIT	0	0	1	0
SVT	0	0	1	1
SOVP	0	1	0	0
	0	1	0	1
	0	1	1	0
	0	1	1	1
	1	0	0	0
	1	0	0	1
	1	0	1	0
	1	0	1	1
	1	1	0	0
	1	1	1	0
	1	1	1	1



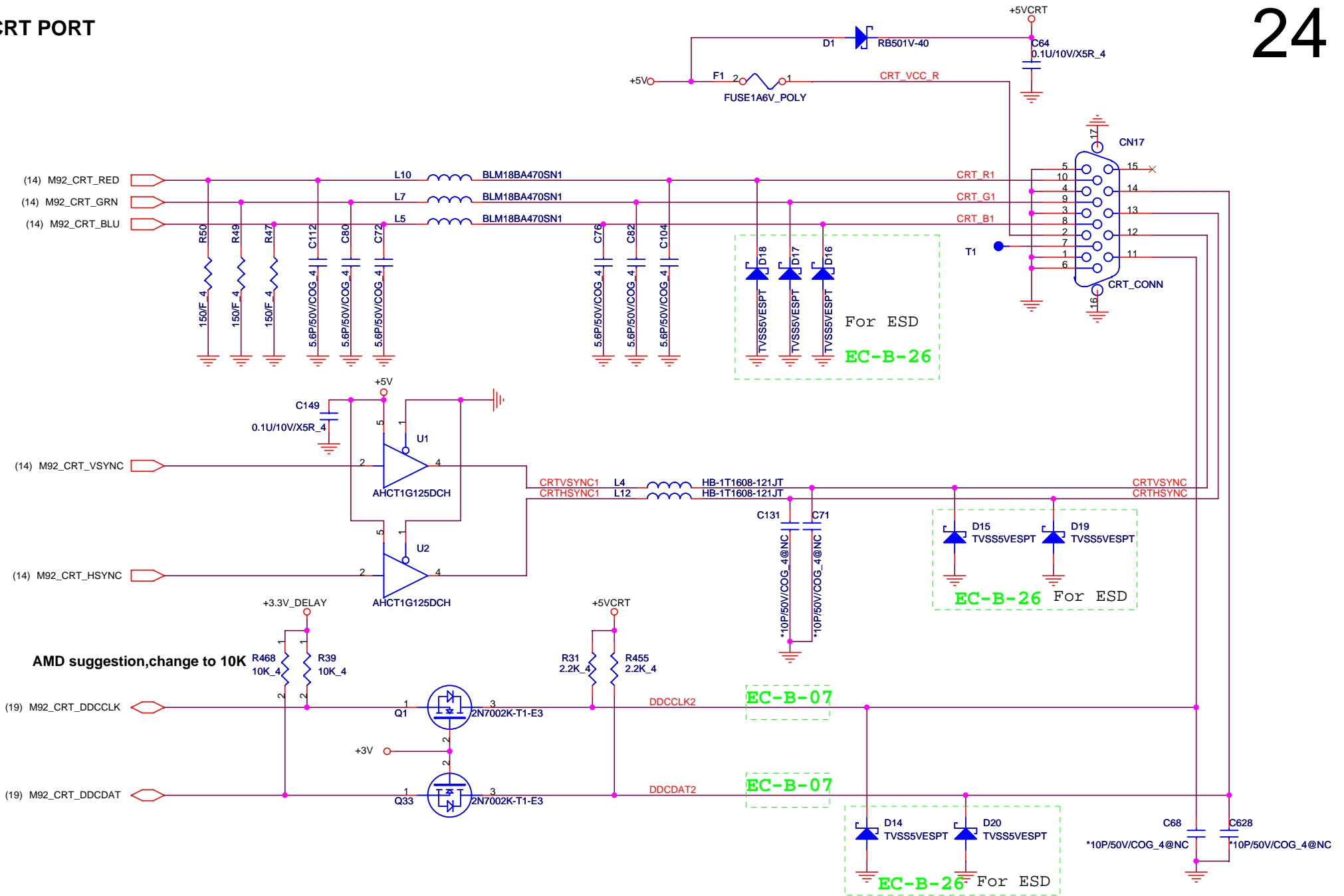
Model ID	PANEL_DET2	PANEL_DET1
13"	0	0
14"	0	1
15"	1	0
Default	1	1





U47E	VSS	VSS	H5
AA26	VSS1001	VSS1077	H5
AA27	VSS1002	VSS1088	J23
AA3	VSS1003	VSS1099	J26
AA6	VSS1004	VSS1110	J27
AB1	VSS1005	VSS1121	AC22
AA23	VSS1006	VSS1132	K28
AB28	VSS1007	VSS1143	K19
AB29	VSS1008	VSS1154	L15
AB4	VSS1009	VSS1165	L2
AB5	VSS1010	VSS1176	L26
VSS1011	VSS1011	VSS1187	L27
AC17	VSS1012	VSS1198	L5
AC26	VSS1013	VSS1209	L7
AC27	VSS1014	VSS1220	L7
AD1	VSS1015	VSS1231	IM12
AD10	VSS1016	VSS1242	M13
AD12	VSS1017	VSS1253	M14
AD13	VSS1018	VSS1264	M15
AD14	VSS1019	VSS1275	M16
AD17	VSS1020	VSS1286	M17
AD18	VSS1021	VSS1297	M23
AD21	VSS1022	VSS1308	M28
AD28	VSS1023	VSS1319	M29
AD29	VSS1024	VSS1330	N11
AD5	VSS1025	VSS1341	N12
AD6	VSS1026	VSS1352	N13
AD7	VSS1027	VSS1363	N14
AD9	VSS1028	VSS1374	N15
AE12	VSS1029	VSS1385	N16
AE13	VSS1030	VSS1396	N17
AE14	VSS1031	VSS1407	N18
VSS1032	VSS1032	VSS1418	N26
AE17	VSS1033	VSS1429	N27
AE2	VSS1034	VSS1440	P12
AE20	VSS1035	VSS1451	P13
AE24	VSS1036	VSS1462	P14
AE3	VSS1037	VSS1473	P16
AE4	VSS1038	VSS1484	P17
AE6	VSS1039	VSS1495	P2
AE9	VSS1040	VSS1506	P12
AE13	VSS1041	VSS1517	P28
VSS1042	VSS1042	VSS1528	P29
AE16	VSS1043	VSS1539	P4
AE18	VSS1044	VSS1550	P4
AF22	VSS1045	VSS1561	R1
AH26	VSS1046	VSS1572	R11
AF26	VSS1047	VSS1583	R12
AF27	VSS1048	VSS1594	R13
AF5	VSS1049	VSS1605	R14
AF7	VSS1050	VSS1616	R16
AF9	VSS1051	VSS1627	R17
AG13	VSS1052	VSS1638	R18
AG16	VSS1053	VSS1649	R28
AG18	VSS1054	VSS1660	T12
AG20	VSS1055	VSS1671	T13
AG23	VSS1056	VSS1682	T14
AG3	VSS1057	VSS1693	T16
AG6	VSS1058	VSS1704	T17
AG9	VSS1059	VSS1715	T23
AH12	VSS1060	VSS1726	T3
AH14	VSS1061	VSS1737	T3
AH17	VSS1062	VSS1748	U12
AH19	VSS1063	VSS1759	U13
AH2	VSS1064	VSS1770	U26
AH22	VSS1065	VSS1781	U14
AH25	VSS1066	VSS1792	U16
AH28	VSS1067	VSS1803	U17
AH5	VSS1068	VSS1814	AD23
AH8	VSS1069	VSS1825	J27
AJ2	VSS1070	VSS1836	U3
AJ12	VSS1071	VSS1847	V1
AJ14	VSS1072	VSS1858	V13
AJ8	VSS1073	VSS1869	V14
VSS1074	VSS1074	VSS1880	V16
B11	VSS1075	VSS1891	V23
B14	VSS1076	VSS1902	V28
B17	VSS1077	VSS1913	V28
B2	VSS1078	VSS1924	V29
B20	VSS1079	VSS1935	V4
B23	VSS1080	VSS1946	V5
C26	VSS1081	VSS1957	W26
C27	VSS1082	VSS1968	W27
E11	VSS1083	VSS1979	W3
E14	VSS1084	VSS1990	Y1
E18	VSS1085	VSS2001	Y28
E2	VSS1086	VSS2012	Y29
E21	VSS1087	VSS2023	Y4
E24	VSS1088	VSS2034	Y5
E27	VSS1089	VSS2045	AG28
E5	VSS1090	VSS2056	AH6
FB	VSS1091	VSS2067	AH6
F16	VSS1092	VSS2078	BF2
F28	VSS1093	VSS2089	A25
F29	VSS1094	VSS2100	A1
G12	VSS1095	VSS2111	A2
G14	VSS1096	VSS2122	A28
G18	VSS1097	VSS2133	A29
G21	VSS1098	VSS2144	AH1
G24	VSS1099	VSS2155	AH29
G26	VSS1100	VSS2166	AJ2
G27	VSS1101	VSS2177	AJ2
G8	VSS1102	VSS2188	AJ28
H2	VSS1103	VSS2199	AJ29
H23	VSS1104	VSS2210	B1
H28	VSS1105	VSS2221	B29
H29	VSS1106	VSS2232	

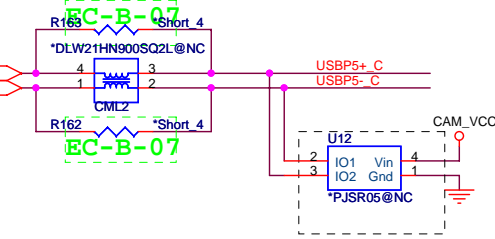
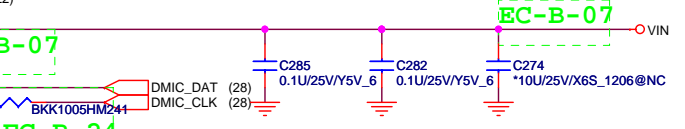
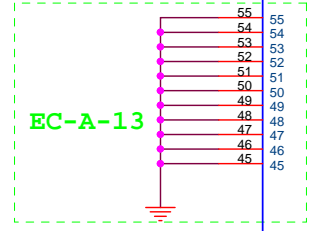
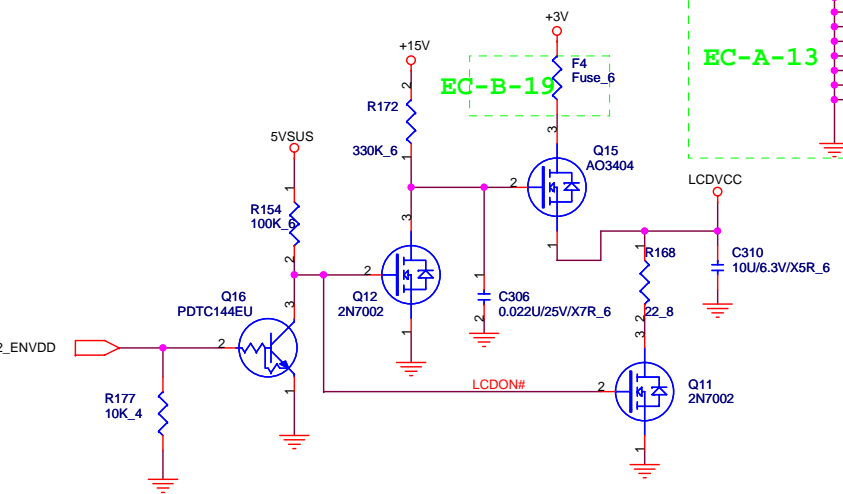
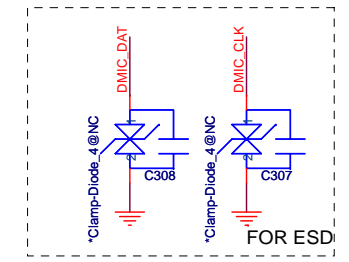
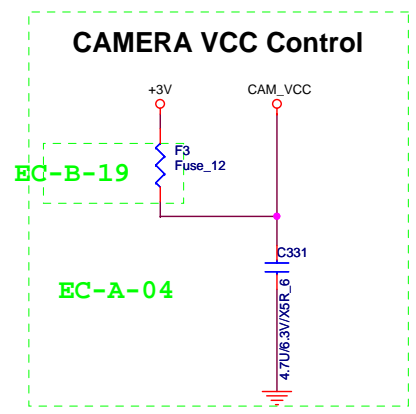
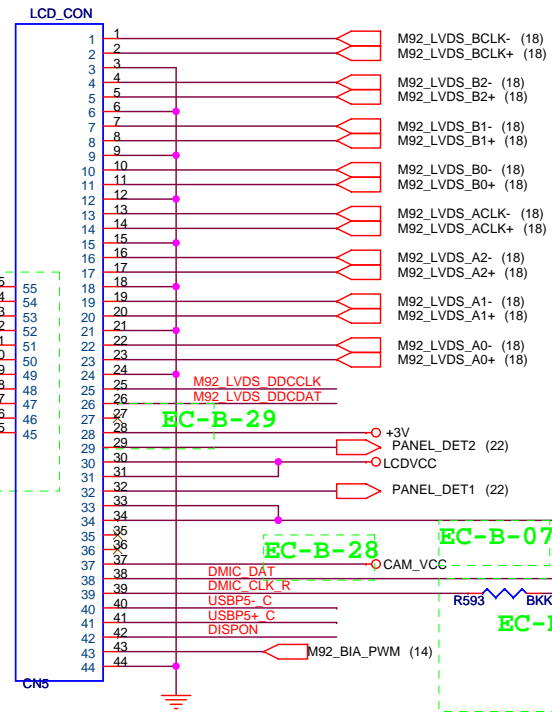
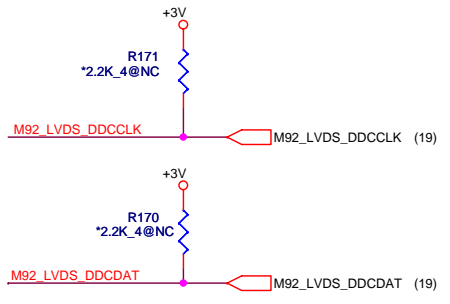
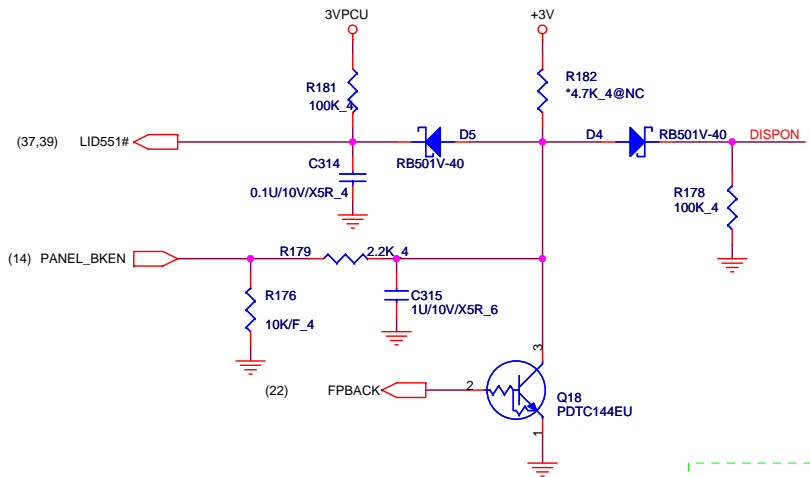
# CRT PORT



**G-Note Montevina**  
**Quanta Computer Inc.**

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LCD panel control & connector

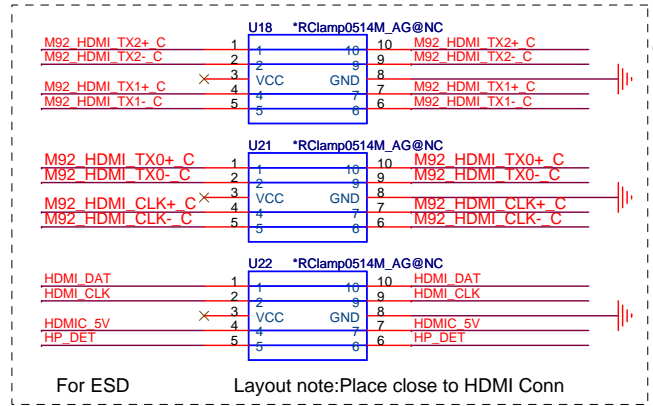
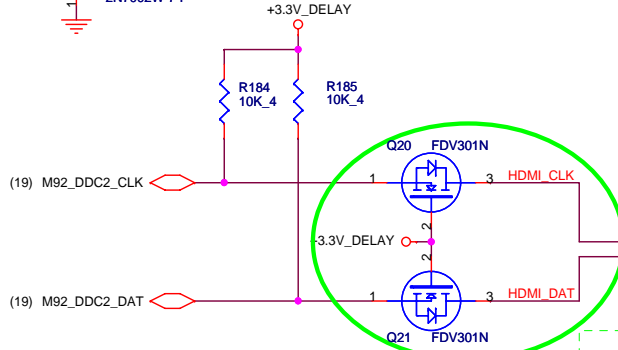
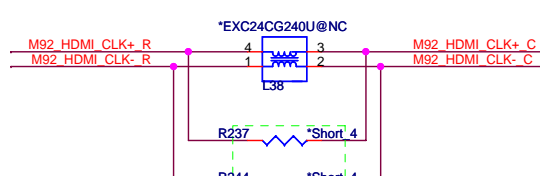
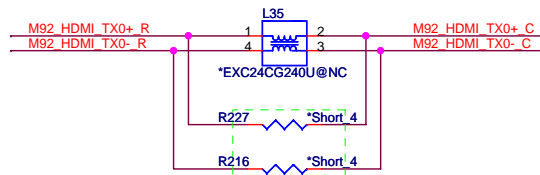
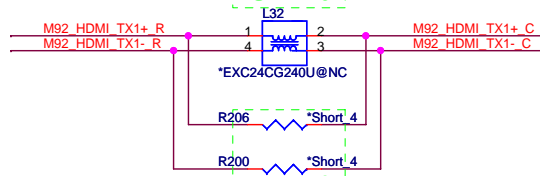
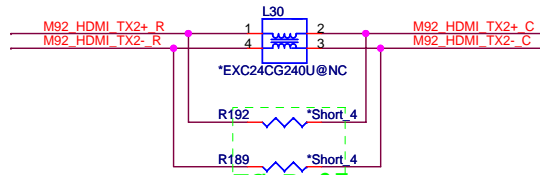
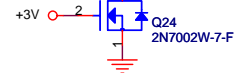


**G-Note Montevina**  
**Quanta Computer Inc.**

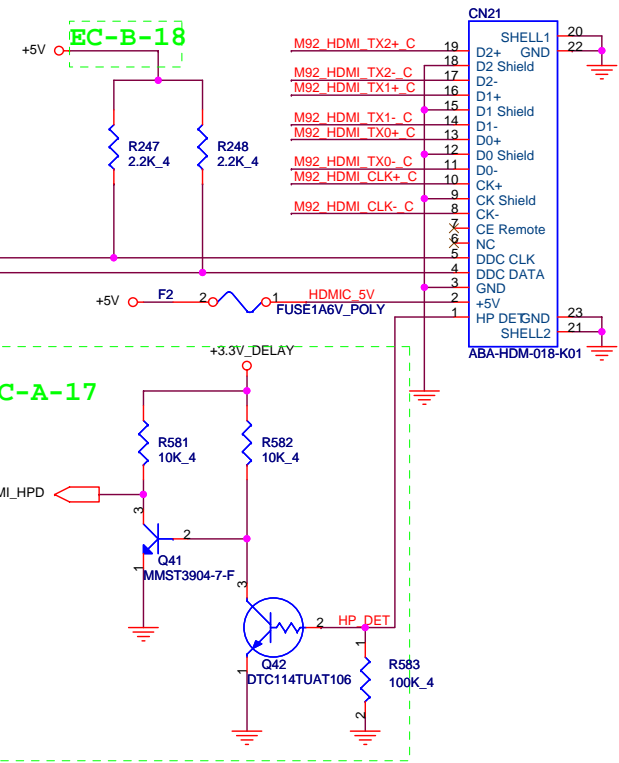
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(18) M92_HDMI_TX2+	C332	0.1U/10V/X7R 4	M92_HDMI_TX2+ R
(18) M92_HDMI_TX2-	C330	0.1U/10V/X7R 4	M92_HDMI_TX2- R
(18) M92_HDMI_TX1+	C344	0.1U/10V/X7R 4	M92_HDMI_TX1+ R
(18) M92_HDMI_TX1-	C340	0.1U/10V/X7R 4	M92_HDMI_TX1- R
(18) M92_HDMI_TX0+	C355	0.1U/10V/X7R 4	M92_HDMI_TX0+ R
(18) M92_HDMI_TX0-	C352	0.1U/10V/X7R 4	M92_HDMI_TX0- R
(18) M92_HDMI_CLK+	C364	0.1U/10V/X7R 4	M92_HDMI_CLK+ R
(18) M92_HDMI_CLK-	C372	0.1U/10V/X7R 4	M92_HDMI_CLK- R

R191	499/F 4	M92_HDMI_TX2+ C
R188	499/F 4	M92_HDMI_TX2- C
R205	499/F 4	M92_HDMI_TX1+ C
R199	499/F 4	M92_HDMI_TX1- C
R226	499/F 4	M92_HDMI_TX0+ C
R215	499/F 4	M92_HDMI_TX0- C
R236	499/F 4	M92_HDMI_CLK+ C
R243	499/F 4	M92_HDMI_CLK- C



### HDMI PORT

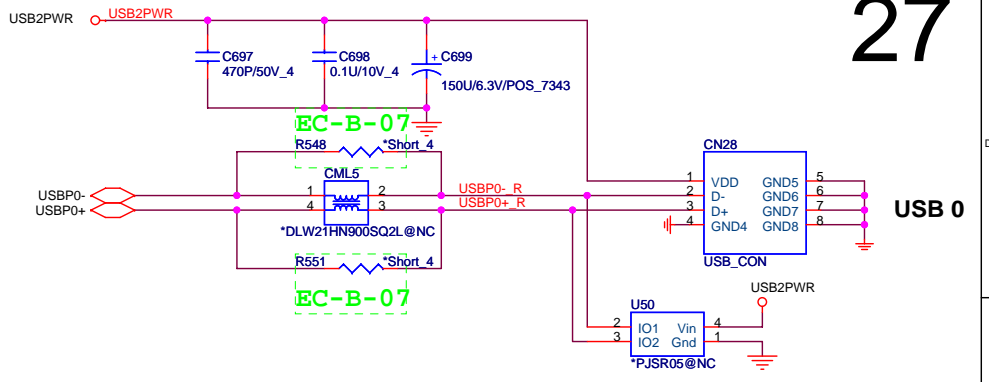
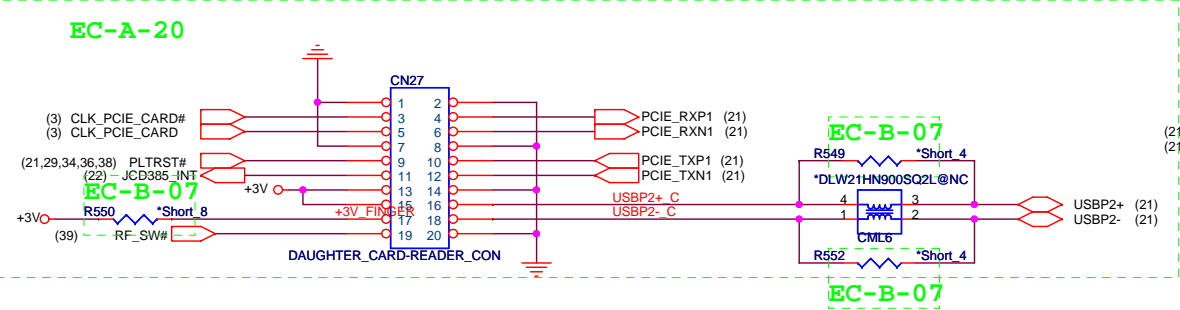



**G-Note Montevina**  
**Quanta Computer Inc.**

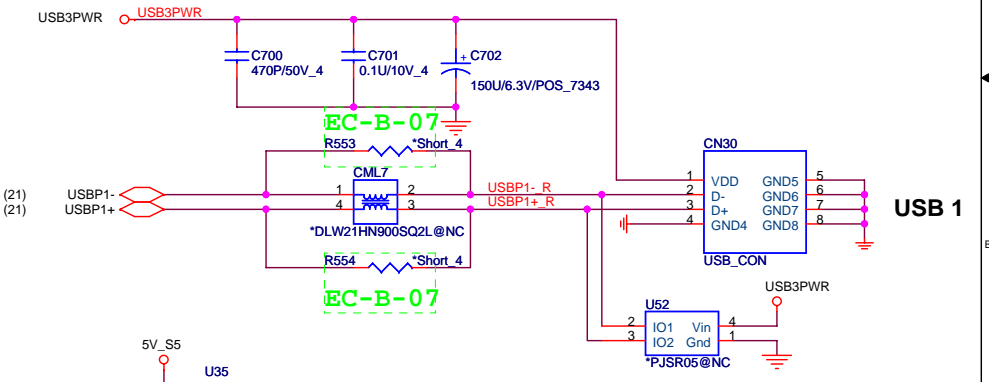
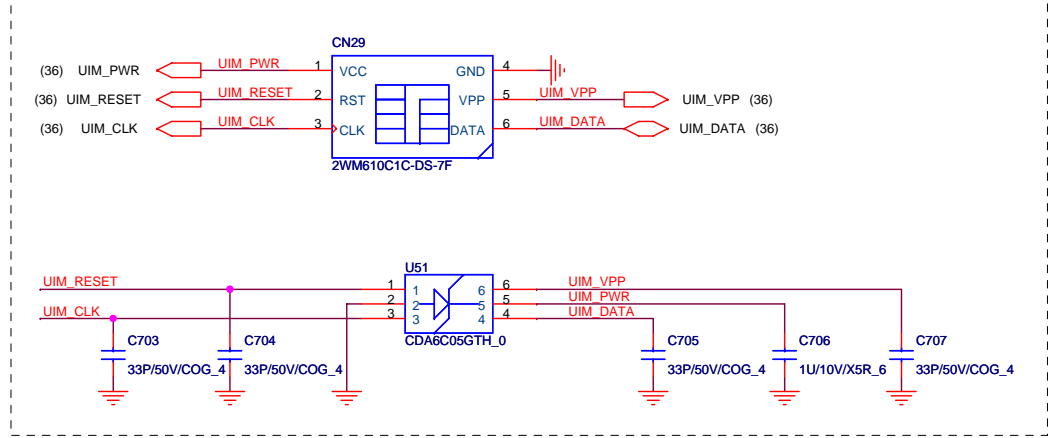
Size	Document Number	Rev
Custom	HDMI PORT	2A
Date:	Thursday, April 09, 2009	Sheet 26 of 55



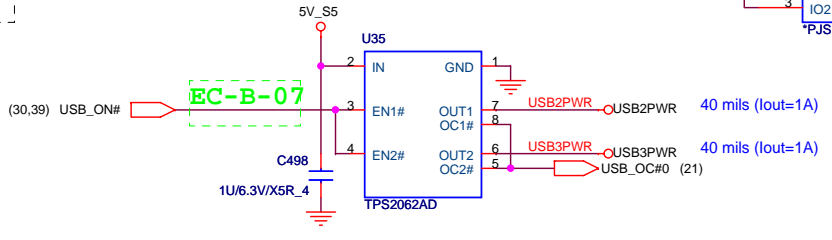
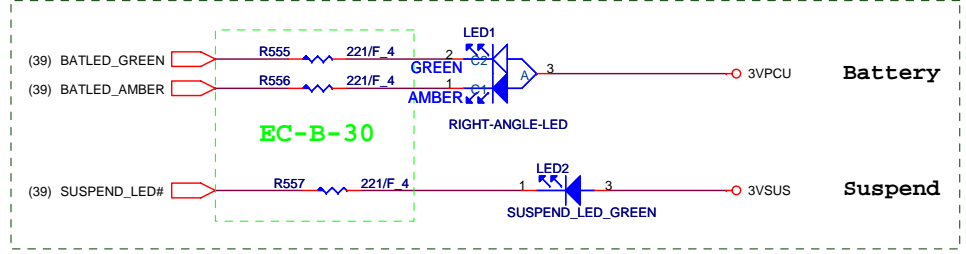
## WIRE TO BOARD CONN CARD READER & FINGERPRINT




## SIM Card CONN



## FRONT LEDs

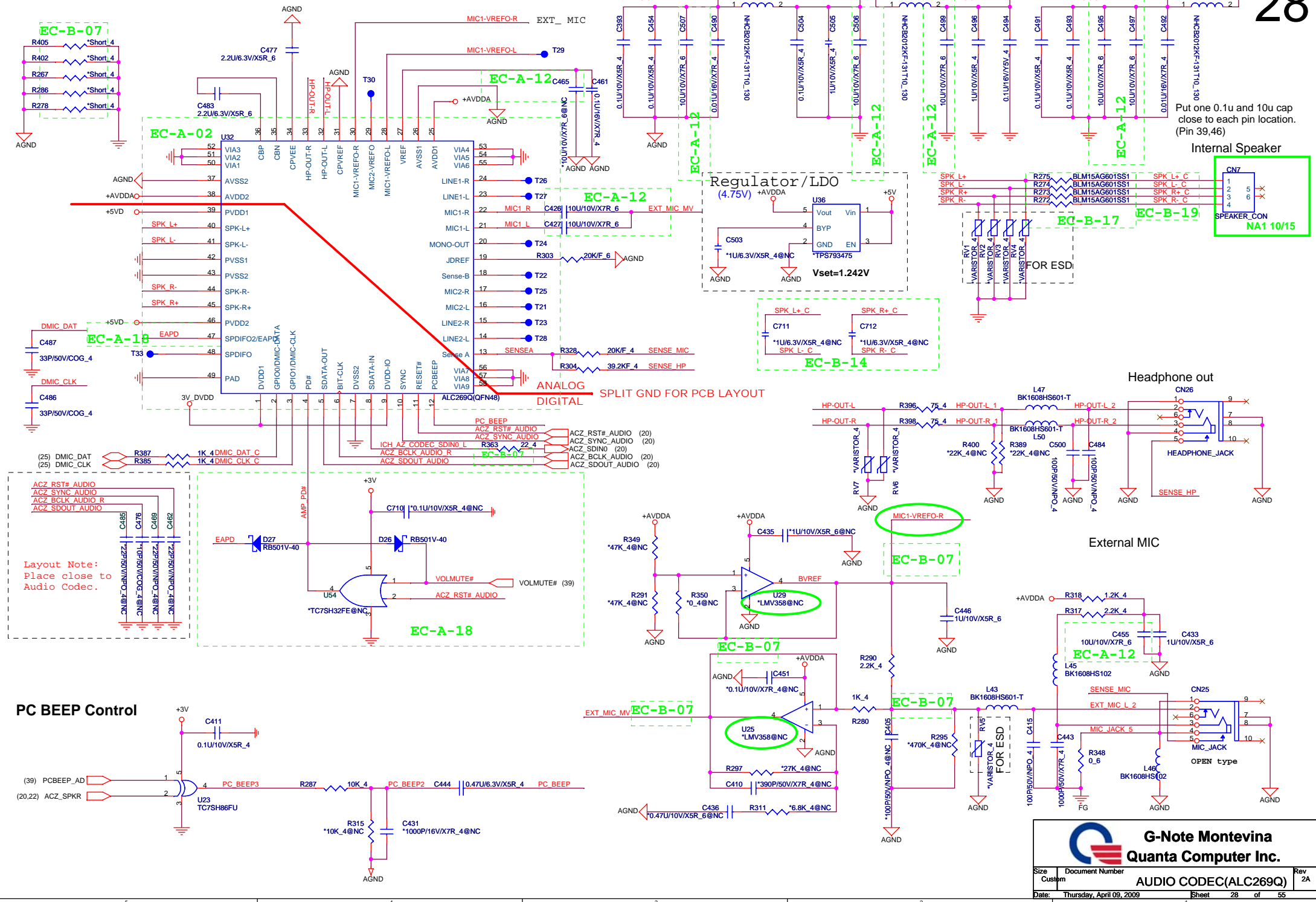


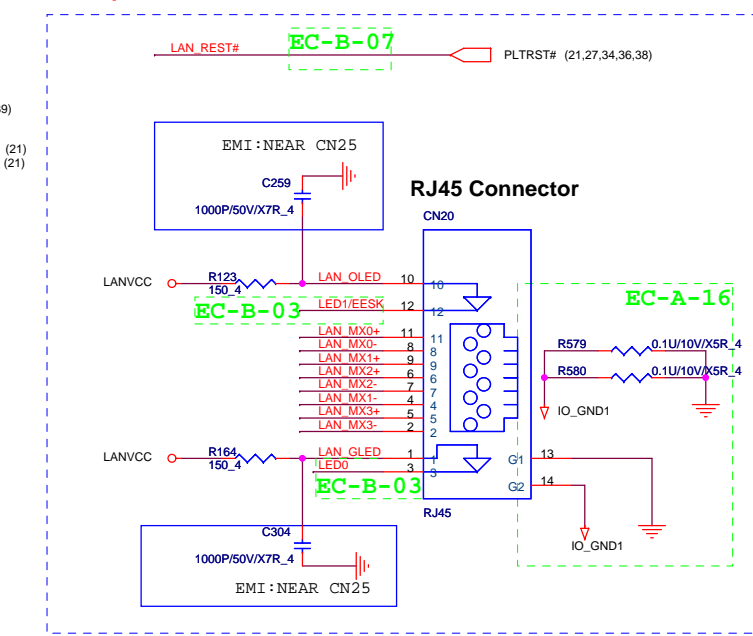
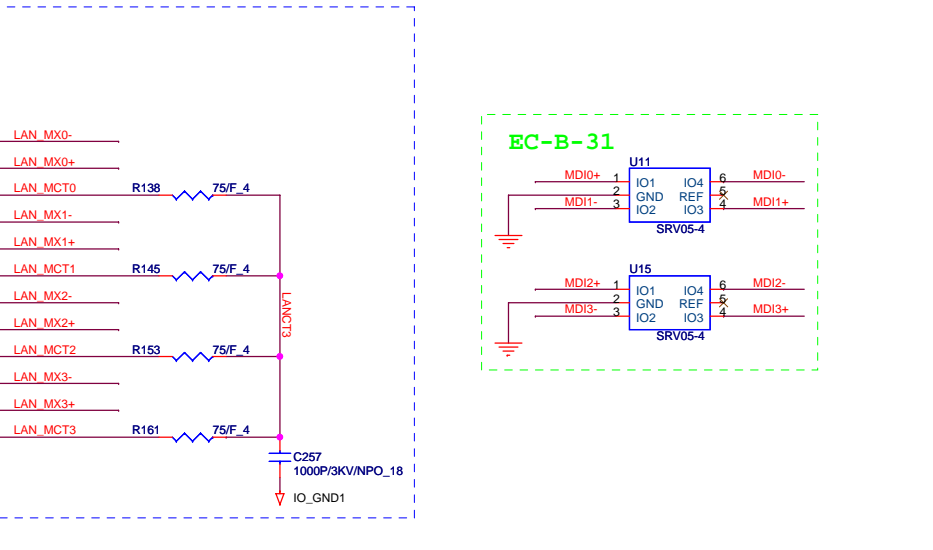
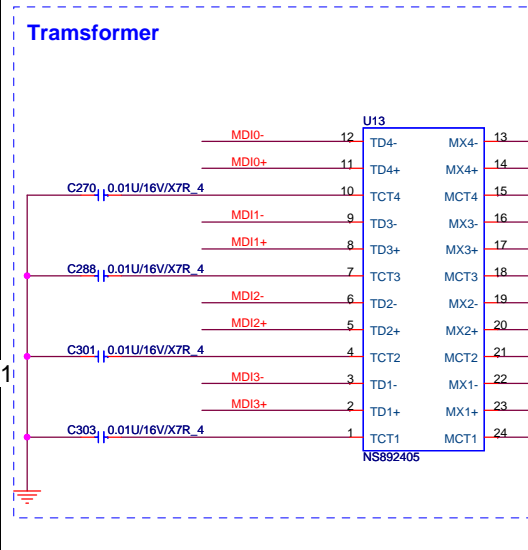
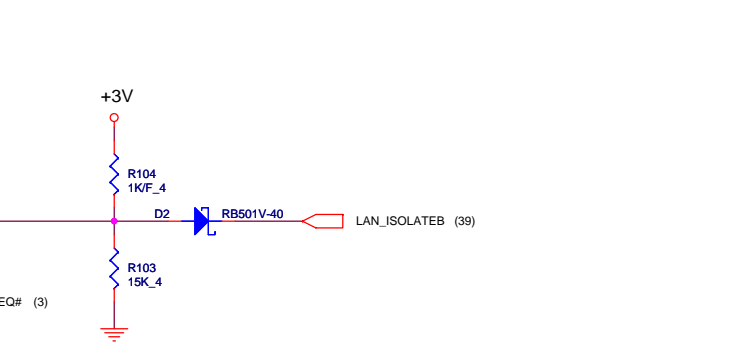
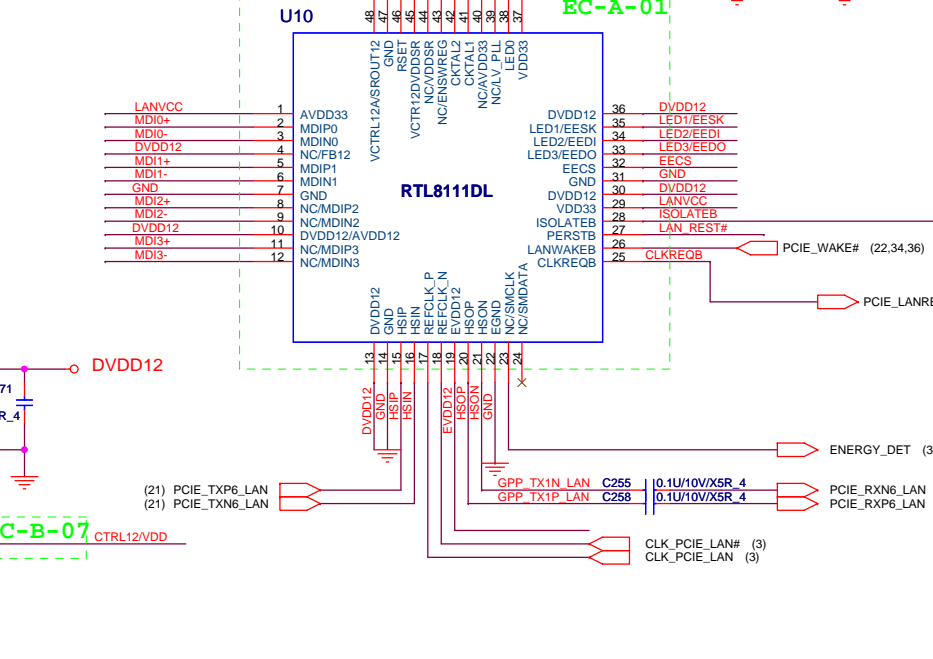
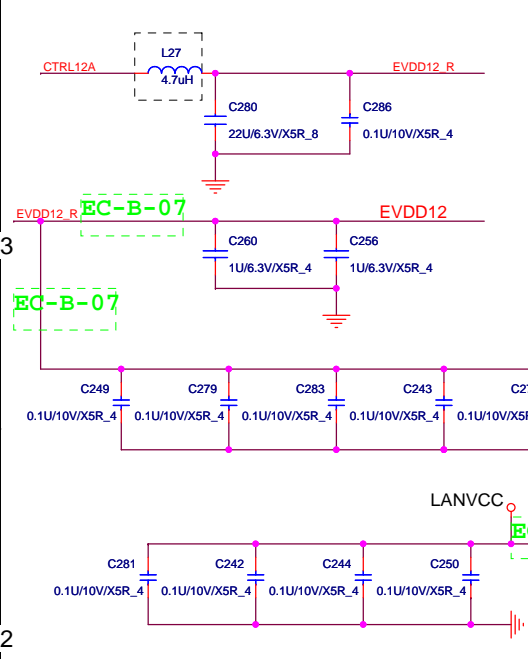
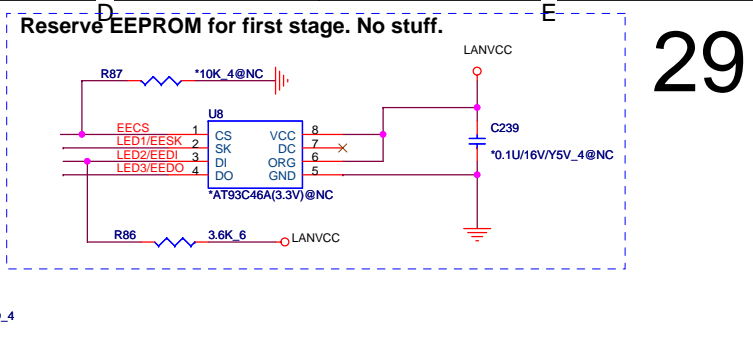
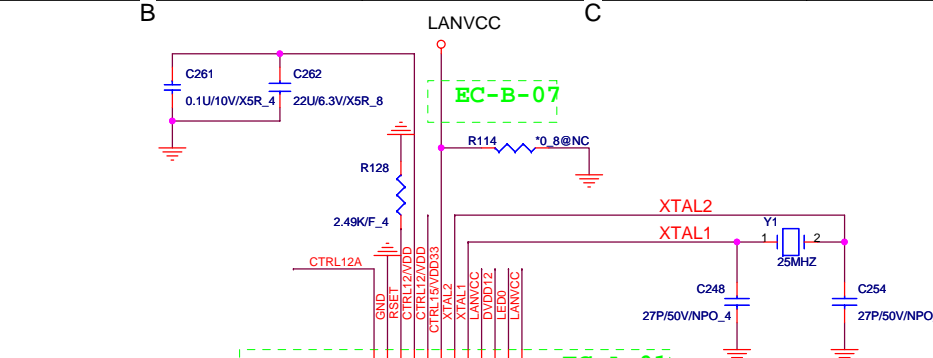
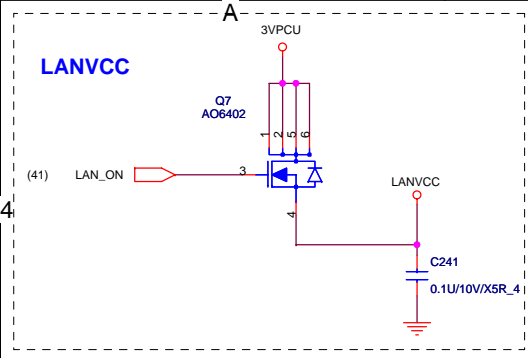


**PROJECT :G NOTE**  
**Quanta Computer Inc.**

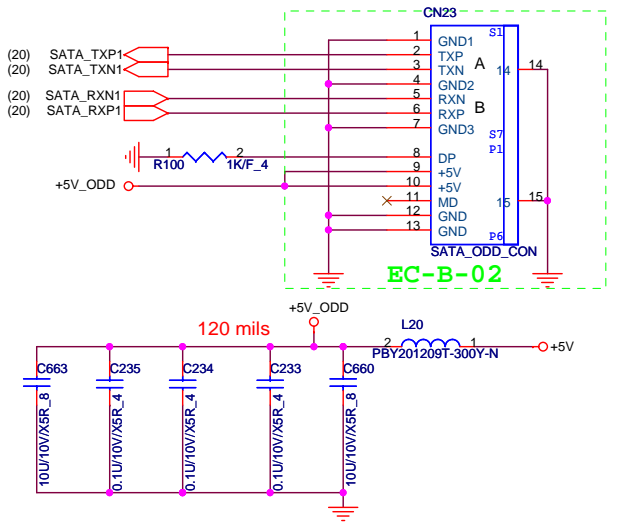
Size	Document Number	Rev
Custom	<b>USB X2/SIM_CARD/LEDs/RF</b>	2A
Date:	Thursday, April 09, 2009	Sheet 27 of 55

# HDAudio Codec

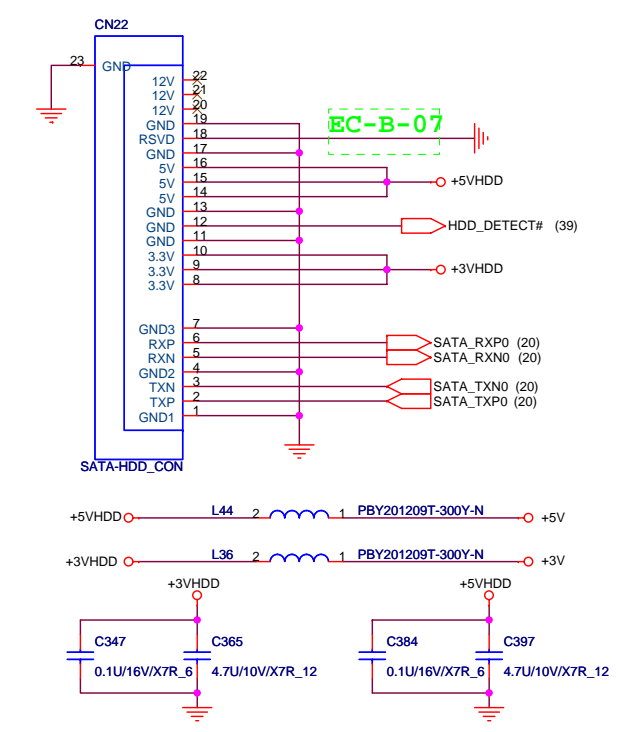




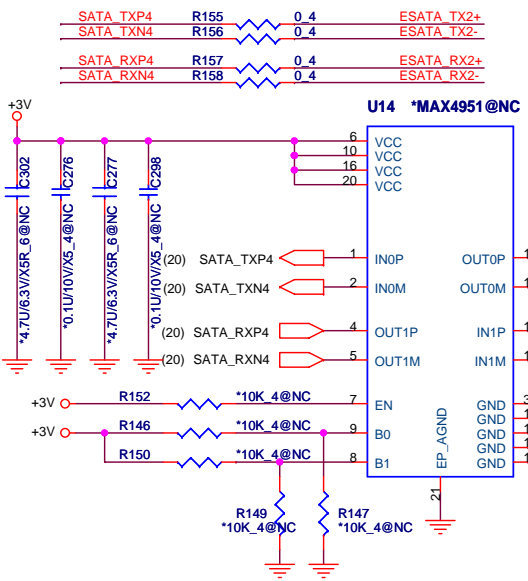
## SATA CD-ROM



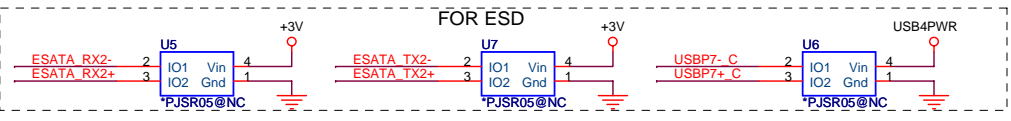
## SATA-HDD



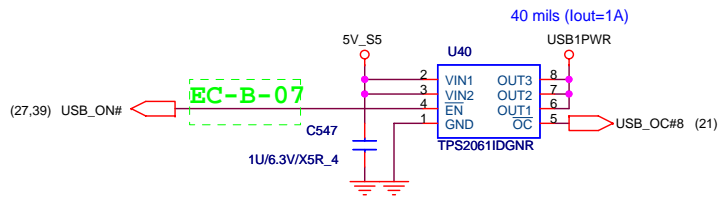
## E-SATA RE-DRIVER



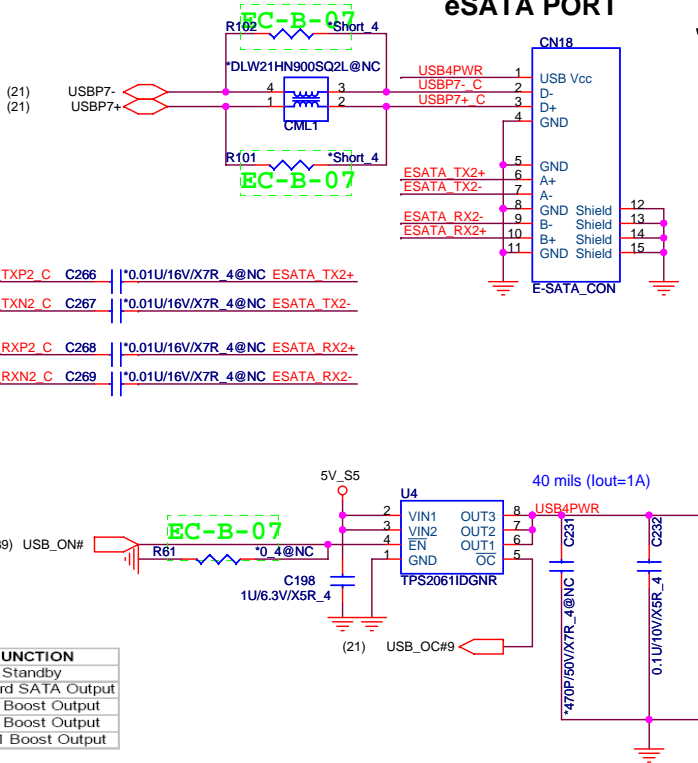
EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output



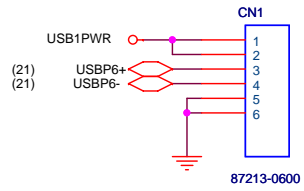
## USB x1(on board)



## eSATA PORT



## REAR\_USB/B connector

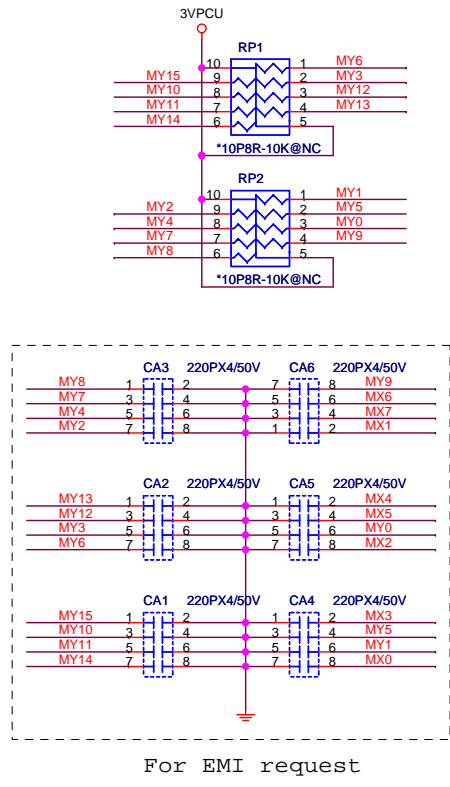
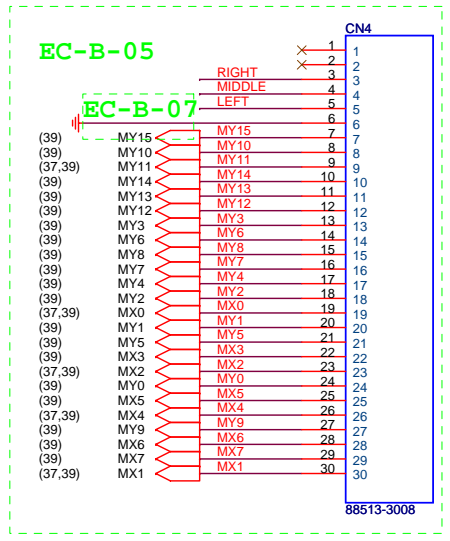


**G-Note Montevina**  
**Quanta Computer Inc.**

Size B	Document Number	Rev 2A
<b>SATA HDD/ ODD/ eSATA/USB</b>		
Date:	Thursday, April 09, 2009	Sheet 30 of 55

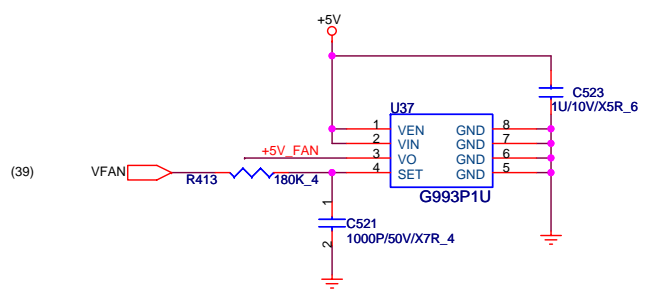
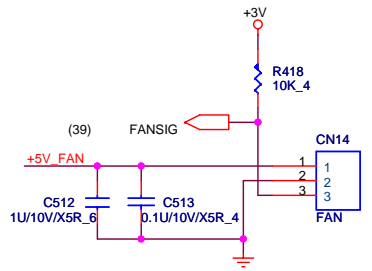
FAN, K/B, T/P & Track Point

KEYBOARD connector

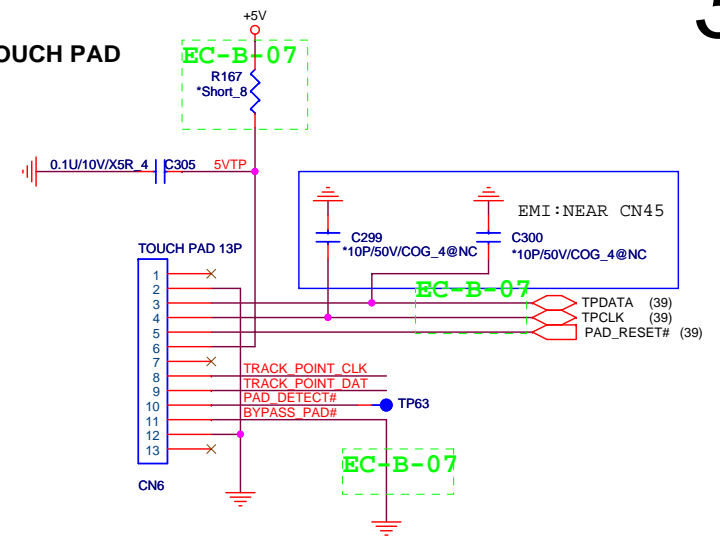


For EMI request

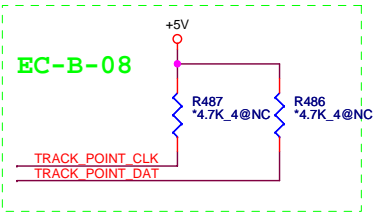
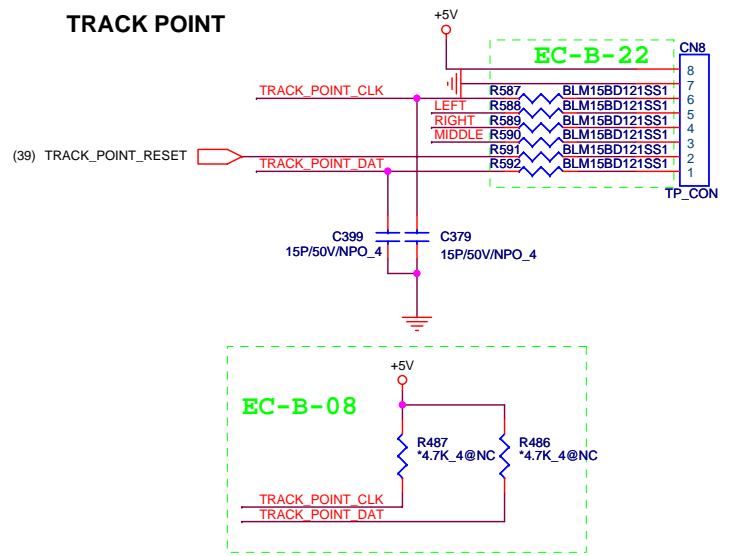
FAN Controller



TOUCH PAD



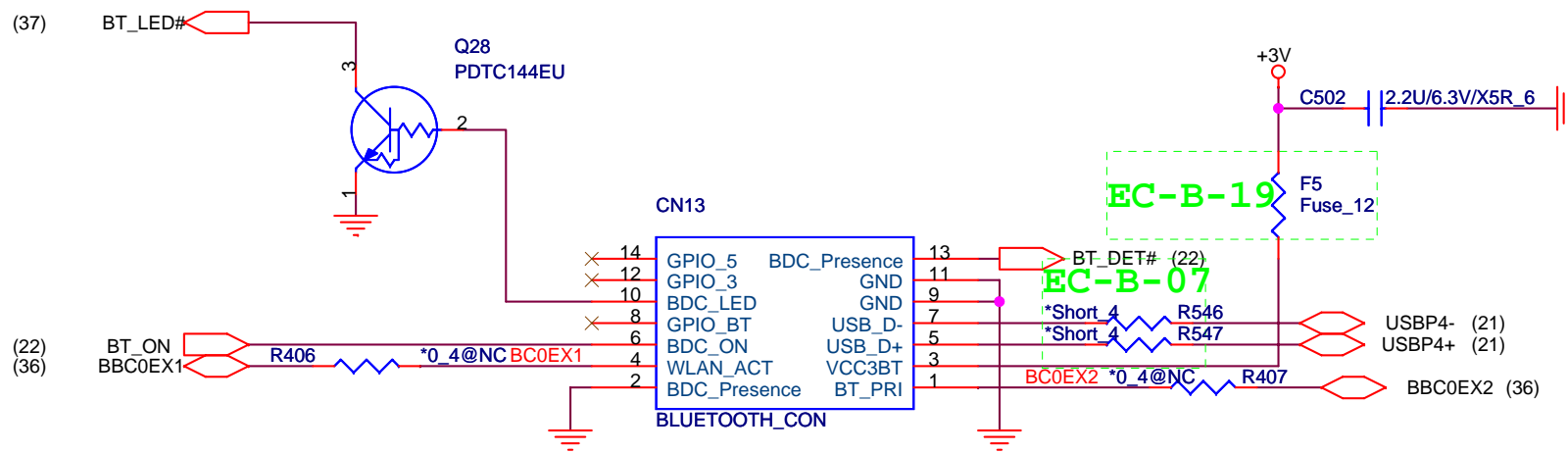
TRACK POINT




**G-Note Montevina**  
**Quanta Computer Inc.**

Size B	Document Number	KB/ TP/ FAN Control	Rev 2A
Date:	Thursday, April 09, 2009	Sheet 31 of 55	

## BLUETOOTH

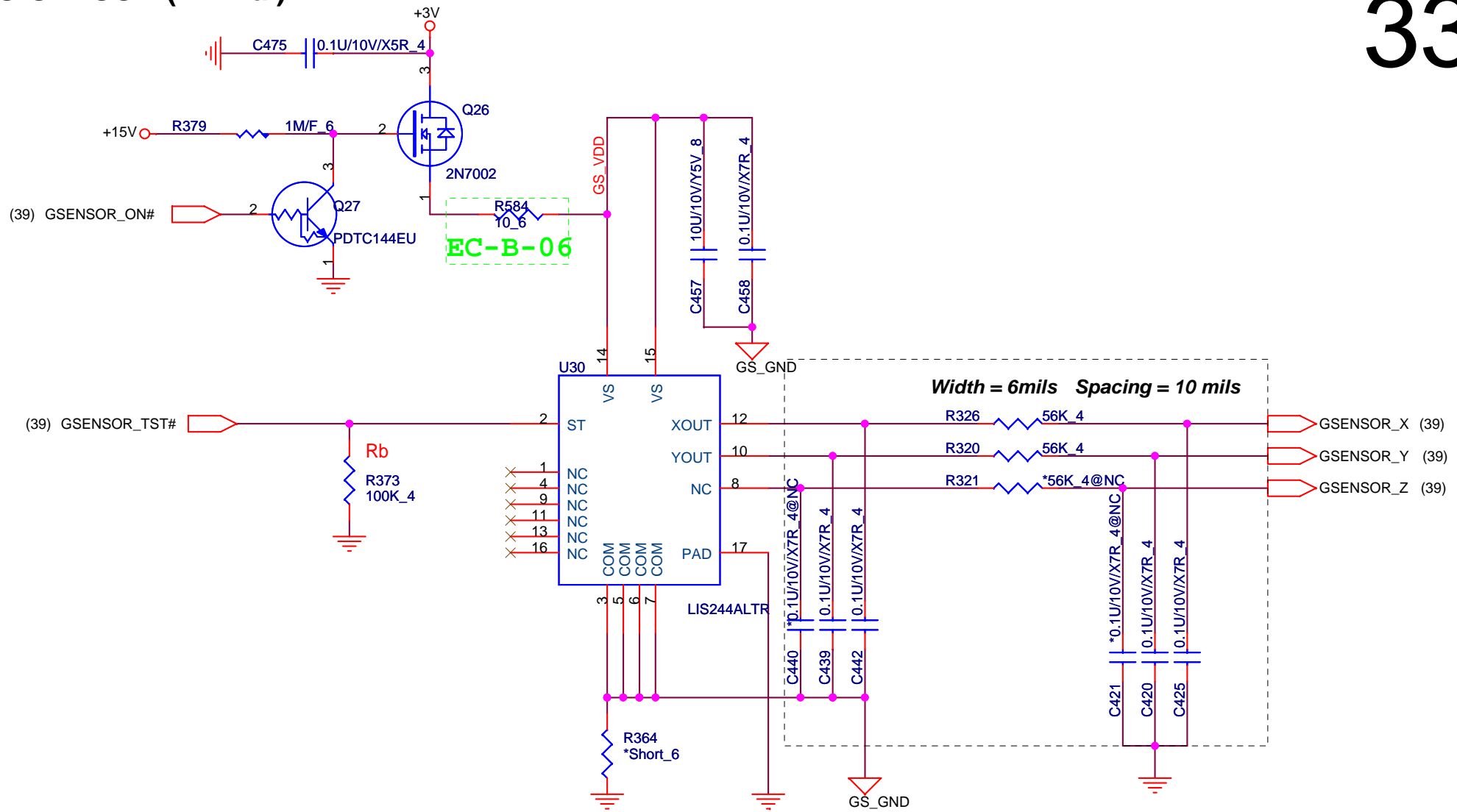


 <b>G-Note Montevina</b> <b>Quanta Computer Inc.</b>		Rev
		2A
Size	Document Number	
A	B/T	
Date:	Thursday, April 09, 2009	Sheet 32 of 55



# G-SENSOR (2-Axial)

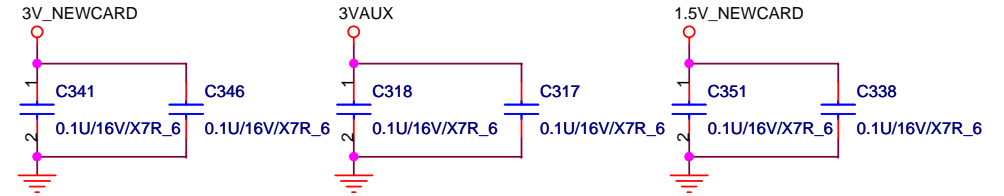
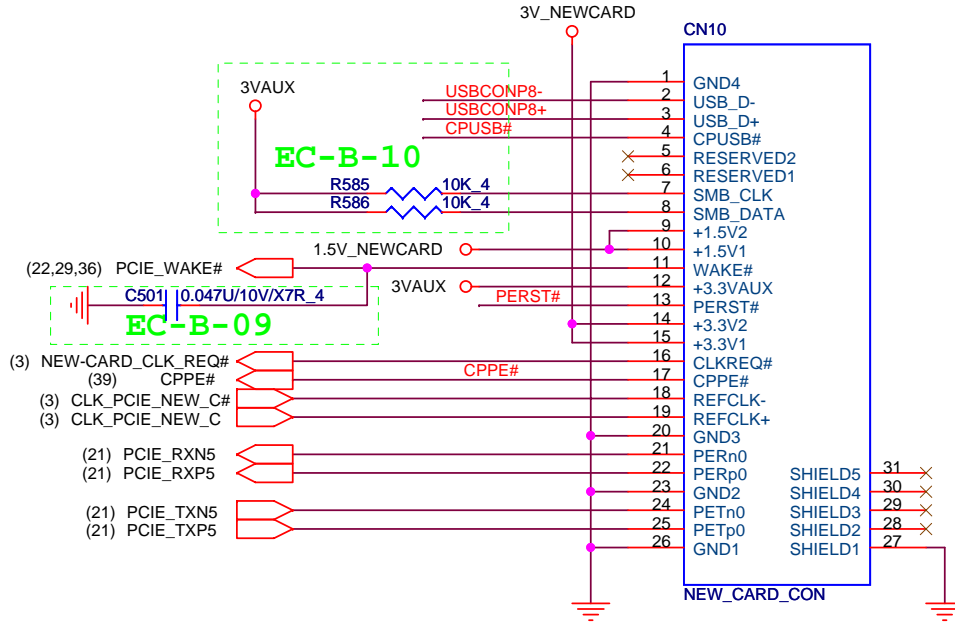
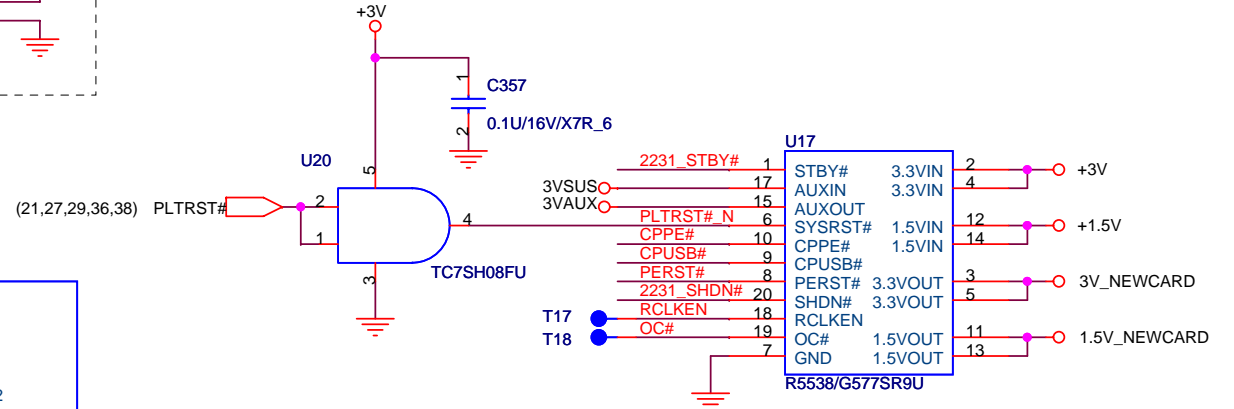
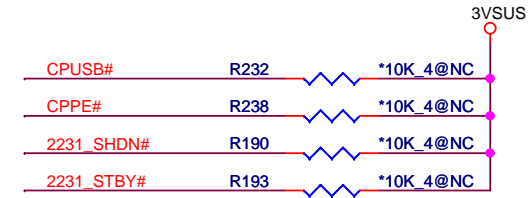
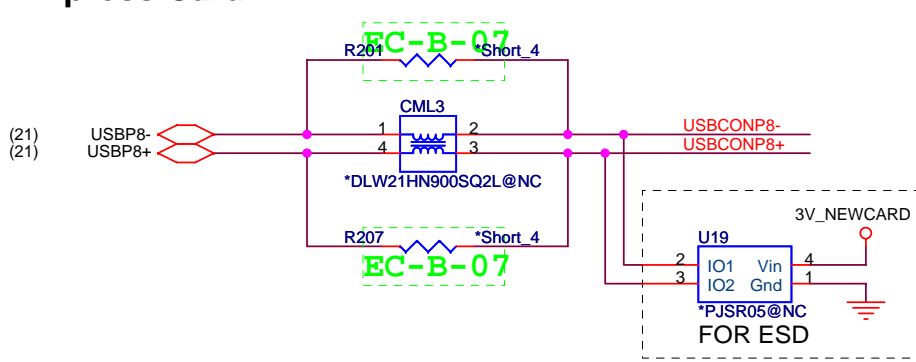
# 33




**G-Note Montevina**  
**Quanta Computer Inc.**

Size A	Document Number <b>G-SENSOR</b>	Rev 2A
Date: Thursday, April 09, 2009		Sheet 33 of 55

# PCI Express Card





## G-Note Montevina Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCI Express Card	2A
Date:	Thursday, April 09, 2009	Sheet 34 of 55

Mini PCI-E Card

EC-B-04

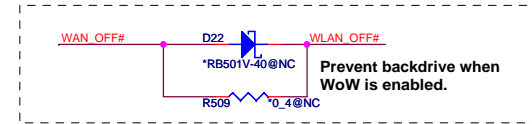
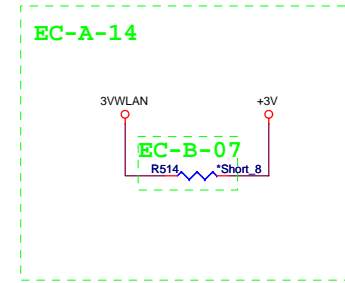
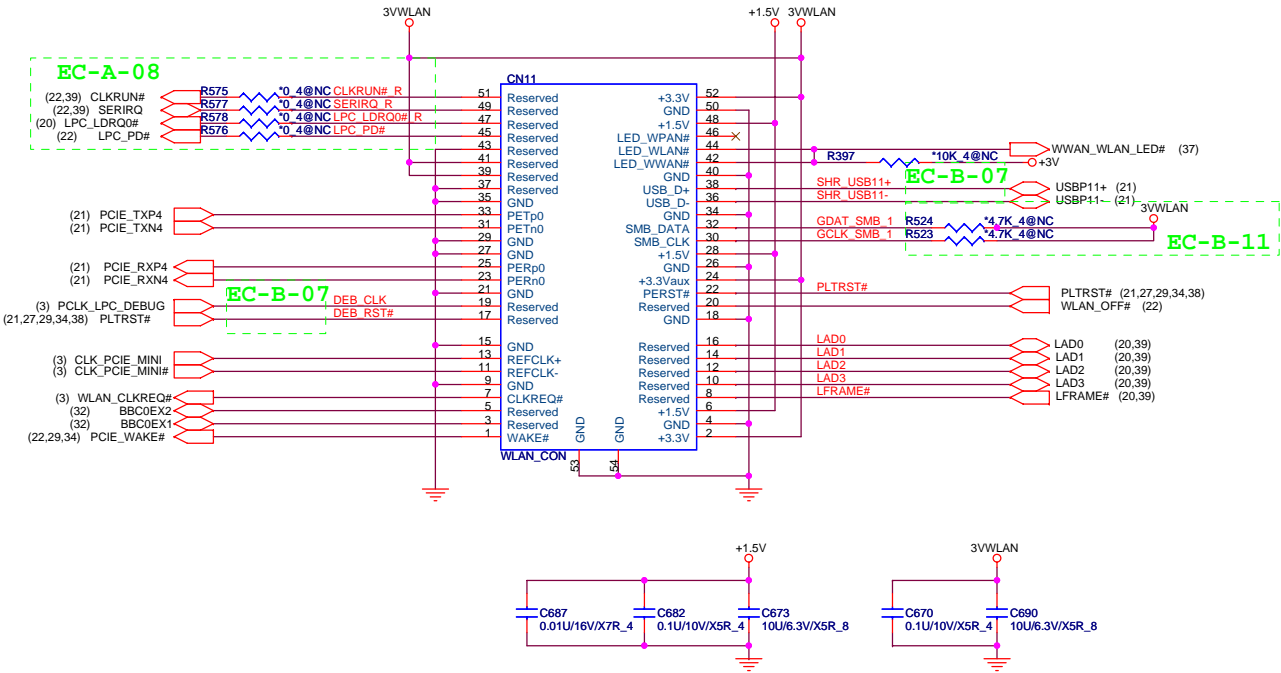
35



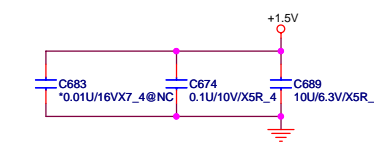
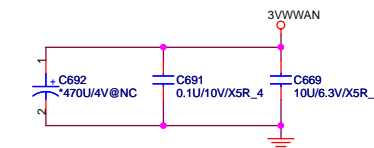
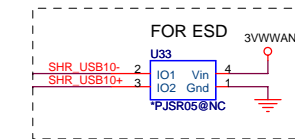
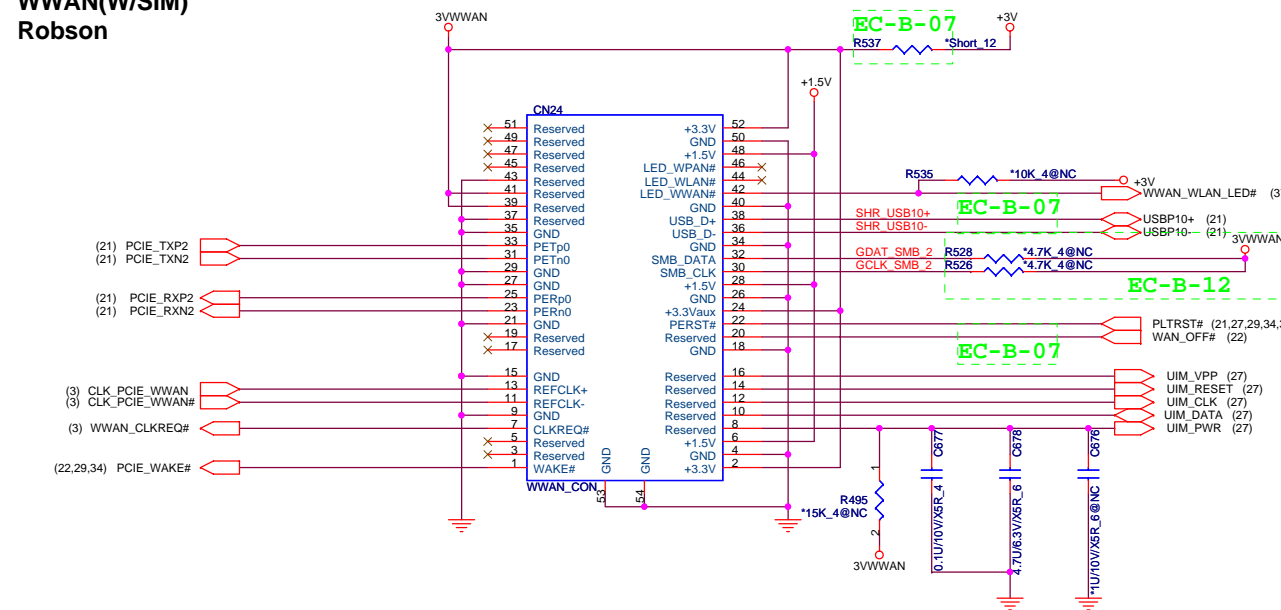
**G-Note Montevina**  
**Quanta Computer Inc.**

Size A	Document Number Mini PCI-E Card	Rev 2A
Date:	Friday, March 06, 2009	Sheet 35 of 55

Mini PCI-E Card (F2)  
(WLAN/ WiMAX)



Mini PCI-E Card (F1)  
WWAN(W/SIM)  
Robson

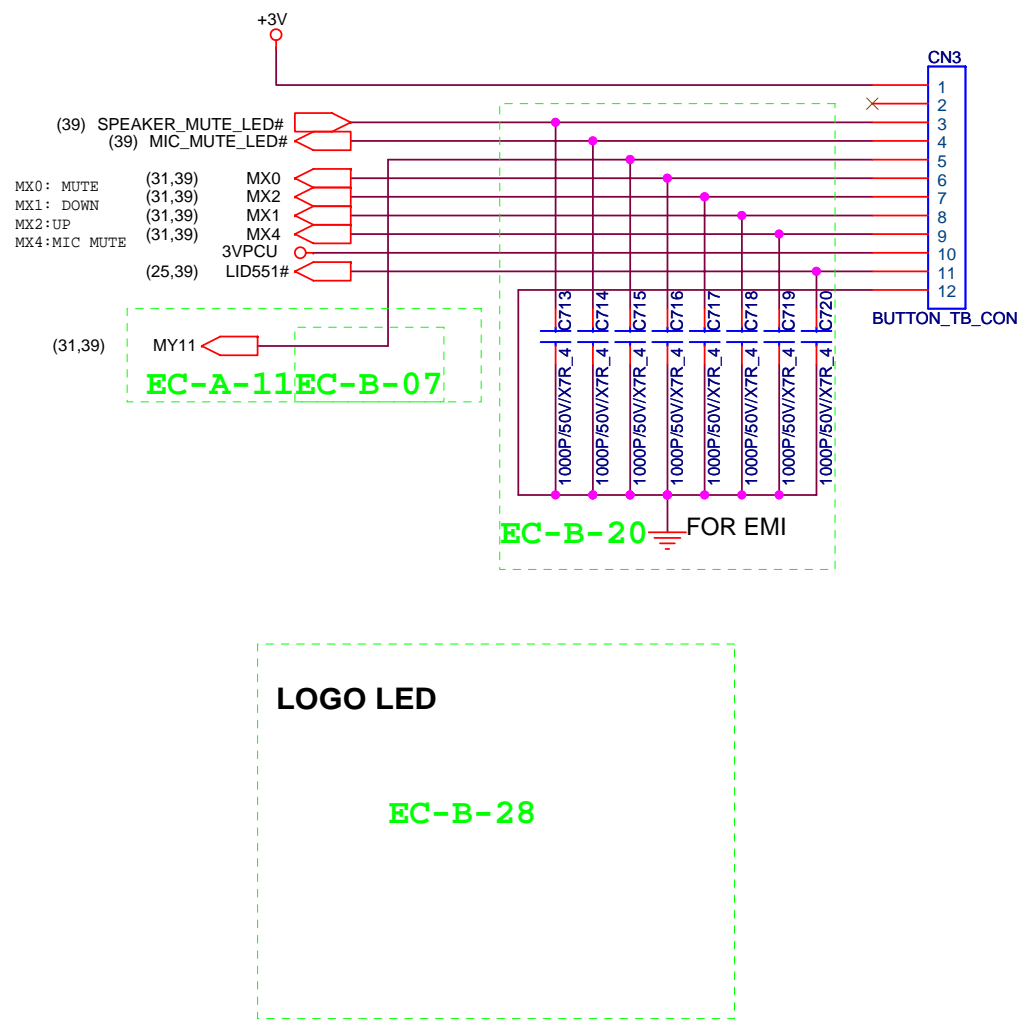


**G-Note Montevina**  
**Quanta Computer Inc.**

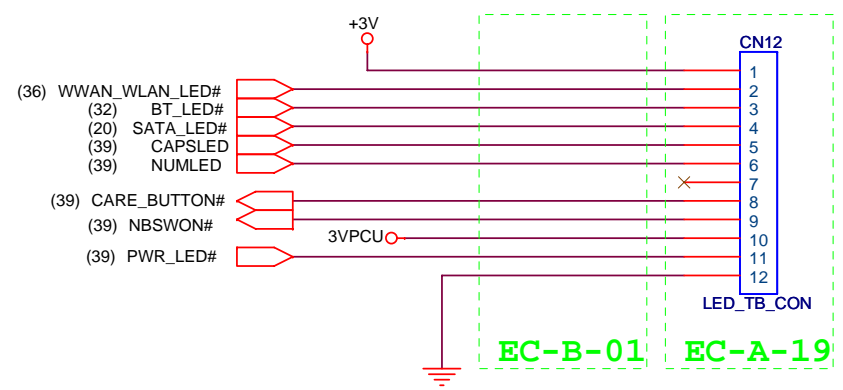
Size	Document Number	Rev
Custom	WLAN & WWAN Slot	2A
Date:	Thursday, April 09, 2009	Sheet 36 of 55


## Daughter Boards for LEDs & Ports

### FFC TO KBD LEFT SIDE CONNECTOR

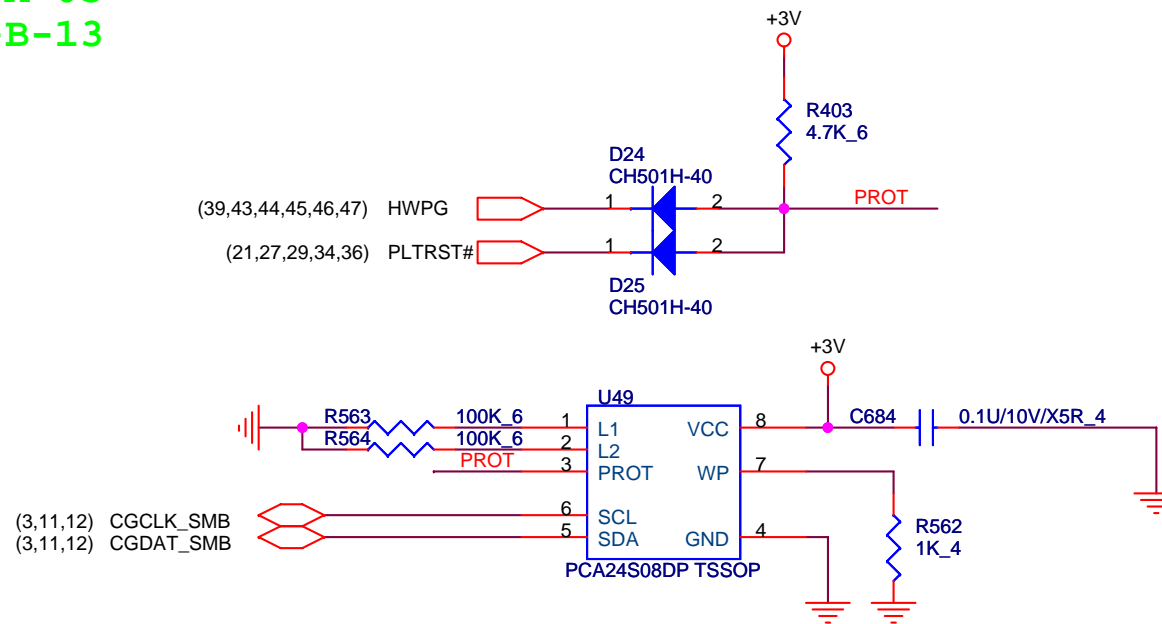


### FFC TO LED RIGHT SIDE CONNECTOR



 <b>G-Note Montevina</b> <b>Quanta Computer Inc.</b>		Size	Document Number	Rev
		Custom	Daughter Boards	2A
Date:	Thursday, April 09, 2009	Sheet	37 of 55	

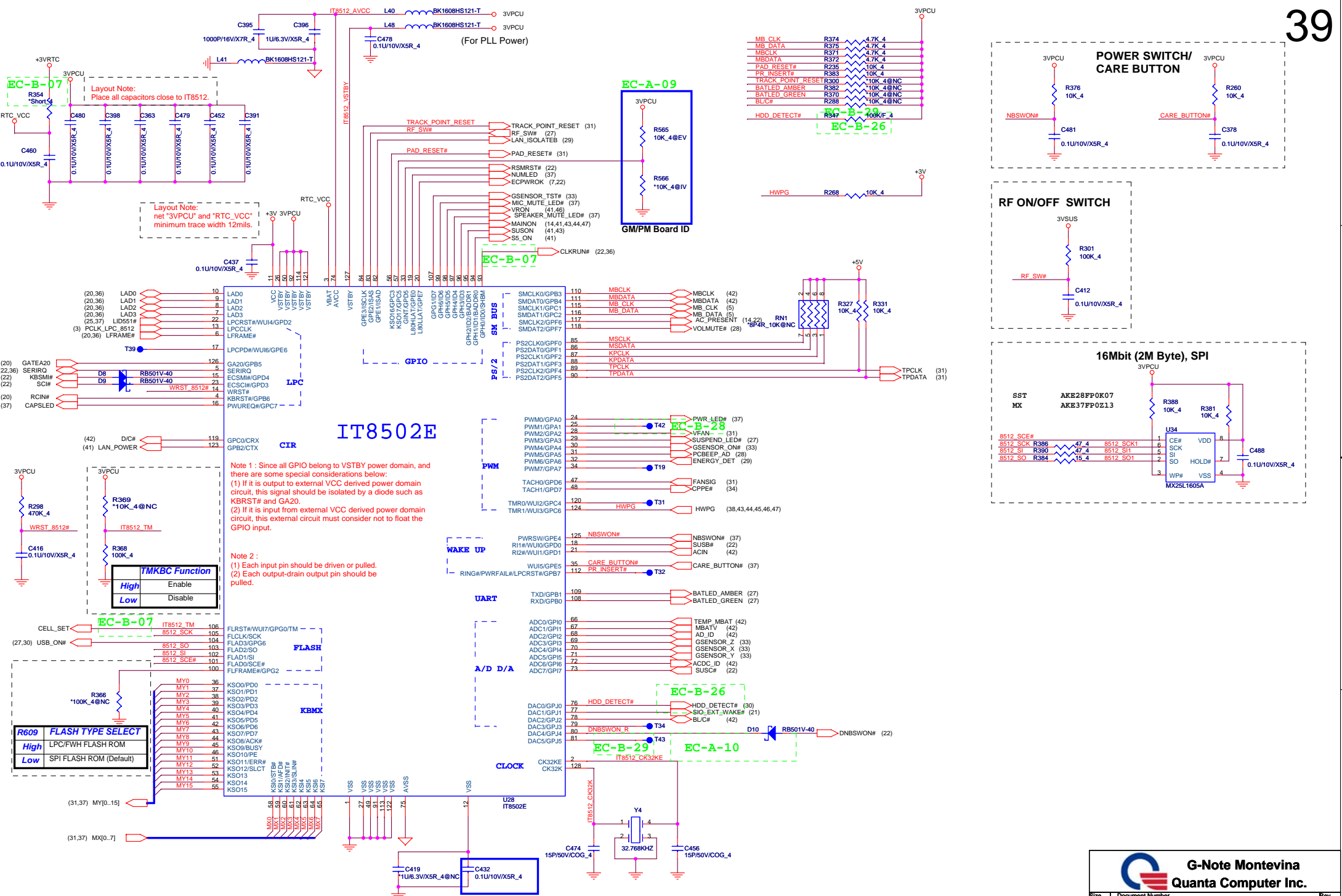
EC-A-03  
EC-B-13



**G-Note Montevina**  
**Quanta Computer Inc.**

Size A	Document Number RFID EEPROM	Rev 2A
Date: Thursday, April 09, 2009		Sheet 38 of 55





**EC-B-07**  
RTC VCC

**Layout Note:**  
Place all capacitors close to IT8512.

**Layout Note:**  
net "3VPCU" and "RTC\_VCC"  
minimum trace width 12mils.

**EC-B-07**  
WRST#\_8512#

**EC-B-07**  
IT8512\_TM

R609	FLASH TYPE SELECT
High	LPC/FWH FLASH ROM
Low	SPI FLASH ROM (Default)

**IT8502E**

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:  
 (1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.  
 (2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :  
 (1) Each input pin should be driven or pulled.  
 (2) Each output-drain output pin should be pulled.

TMKBC Function	Enable
High	Enable
Low	Disable

**FLASH**

FLRST#/WU17/GPG0/TM  
 FLCLK/SCK  
 FLAD3/GPG6  
 FLAD0/SO  
 FLAD1/SI  
 FLAD0/SCE#  
 FLFRAME#/GPG2

**KBMX**

MY0-15, MX0-15

**CLOCK**

CK32KE  
 CK32K

**GPIO**

**CIR**

**PWM**

**WAKE UP**

**UART**

**A/D D/A**

**CLOCK**

**U28 IT8502E**

**EC-A-09**  
GM/PM Board ID

**EC-B-28**  
PWR\_LED#

**EC-B-23**  
SUSPEND\_LED#

**EC-B-29**  
DNBSWON#

**EC-B-26**  
HDD\_DETECT#

**EC-B-29**  
DNBSWON#

**EC-A-10**  
IT8512 CK32KE

**EC-B-29**  
HDD\_DETECT#

**EC-B-26**  
HDD\_DETECT#

**EC-B-07**  
CLKRUN#

**EC-B-28**  
PWR\_LED#

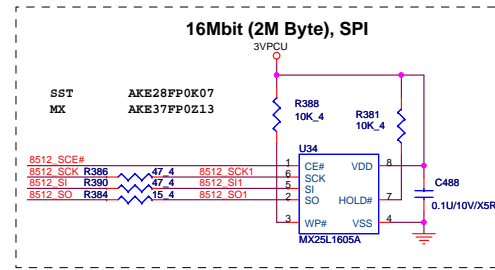
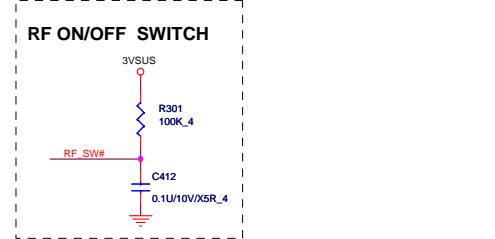
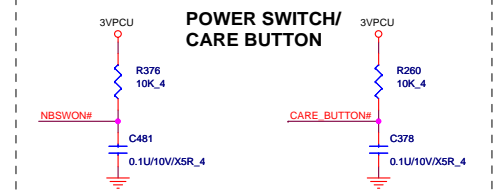
**EC-B-23**  
SUSPEND\_LED#

**EC-B-29**  
DNBSWON#

**EC-B-26**  
HDD\_DETECT#

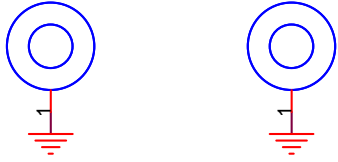
**EC-B-29**  
DNBSWON#

**EC-A-10**  
IT8512 CK32KE



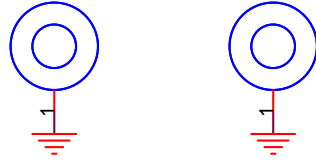
### 3mm minicard nut

HOLE10 H-T-C197BC142D102P2  
HOLE12 H-T-C197BC142D102P2



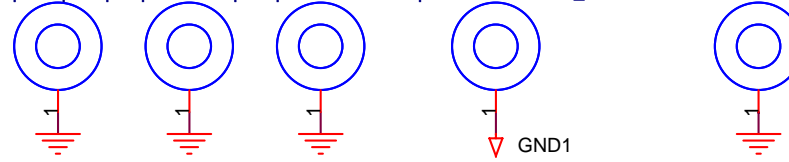
### 7mm minicard nut

HOLE26 H-T-C236BC102D63P2  
HOLE27 H-T-C236BC102D63P2



### PAD

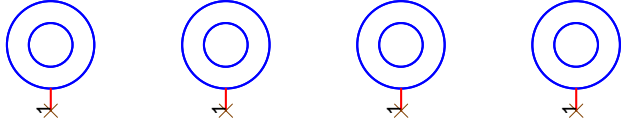
GP1 \*Spad-spe1np GP2 \*spad-c181np GP3 \*Spad-re197x216np  
GP4 \*H-TSHBC276I2\_7D91P2-1 GP5 \*SPAD-SPE3NP



# 40

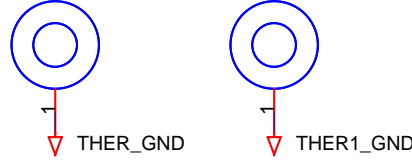
### Hole for CPU support

HOLE20 \*H-C142D142N HOLE21 \*H-C142D142N  
HOLE23 \*H-C142D142N HOLE24 \*H-C142D142N



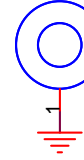
### VGA nut

HOLE22 H-T-C197BC158D122P2 HOLE25 H-T-C197BC158D122P2



### Bluetooth nut

HOLE14 H-T-C217BC154D118P2

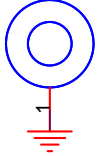


### Card reader board nut

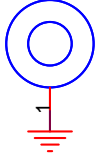
HOLE28 h-tc189bc157d122p2 HOLE29 h-c189d122pt



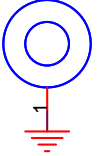
HOLE2 \*H-C276D91P2



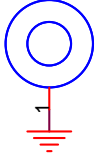
HOLE5 \*H-C276D91P2



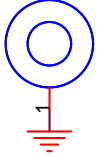
HOLE6 \*H-C276D91P2



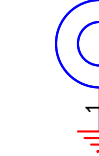
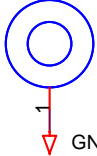
HOLE9 \*H-C276D91P2



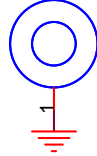
HOLE15 \*H-C276D91P2



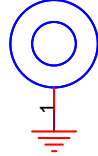
HOLE16 \*H-C276H107D91P2 HOLE17 \*H-C276D91P2



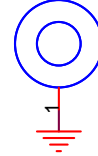
HOLE18 \*H-C276D91P2



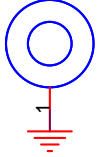
HOLE31 \*H-C276D91P2



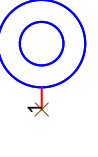
HOLE8 \*h-tshapebc276d91p2



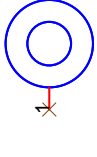
HOLE1 \*H-T-C276BC216D91P2



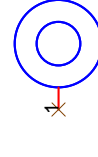
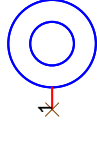
HOLE4 \*H-C91D91N



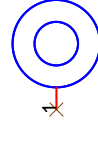
HOLE7 \*H-C298D298N



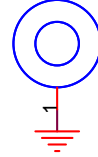
HOLE3 \*H-C79D79N HOLE19 \*H-C79D79N



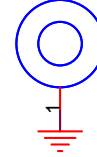
HOLE30 \*H-C98D98N



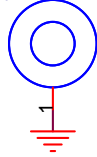
HOLE32 \*h-tc236bc217d87p2



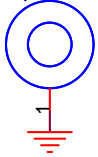
HOLE33 \*h-tc236bc217d87p2



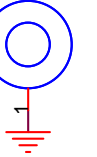
HOLE34 \*spad-c323np



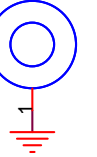
HOLE37 \*spad-c276np



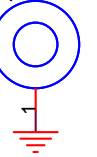
HOLE38 \*H-C276D87P2



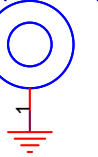
HOLE39 \*H-C276D87P2



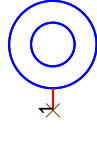
HOLE40 \*spad-c276np



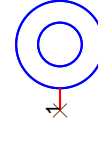
HOLE41 \*spad-c276np



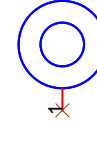
HOLE35 \*H-C87D87N



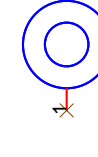
HOLE43 \*O-GC3-1



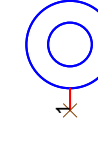
HOLE44 \*O-GC3-2



HOLE45 \*O-GC3-3



HOLE46 \*O-GC3-4



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**Quanta Computer Inc.**

Size A Document Number

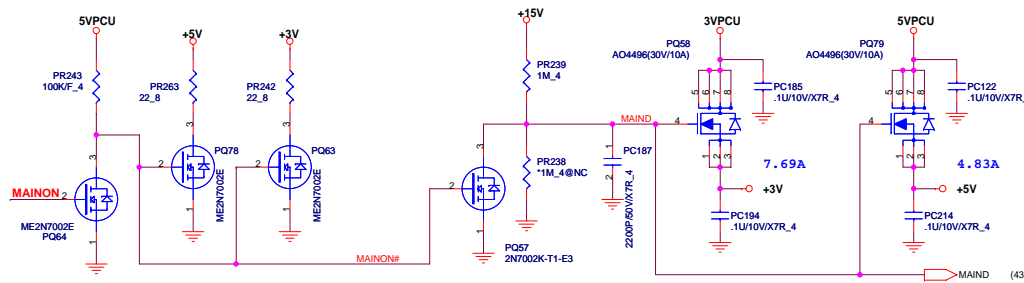
**SCREW HOLE**

Rev 2A

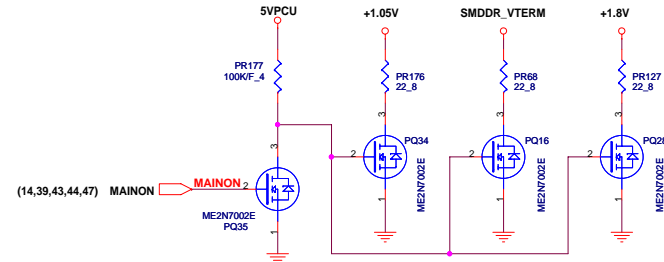
Date: Friday, April 03, 2009

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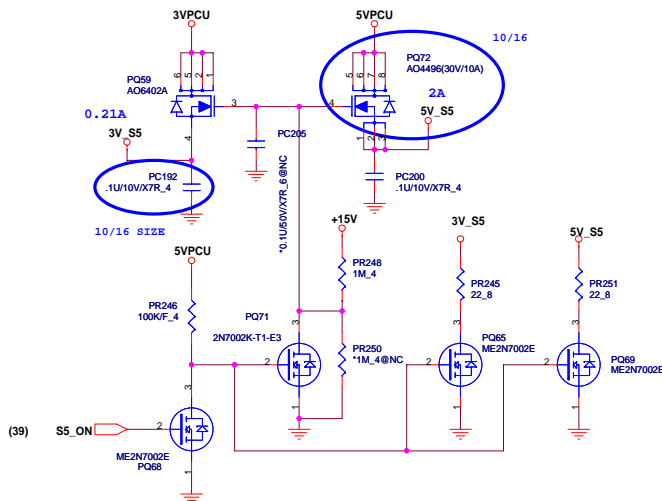
+3V, +5V



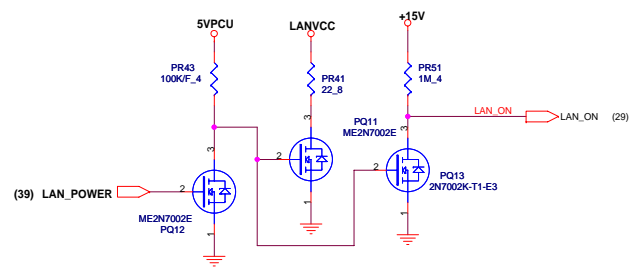
+1.8V, +1.05V, SMDDR\_VTERM



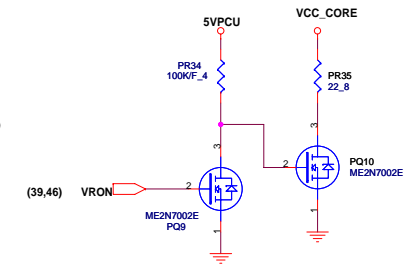
3V\_S5, 5V\_S5



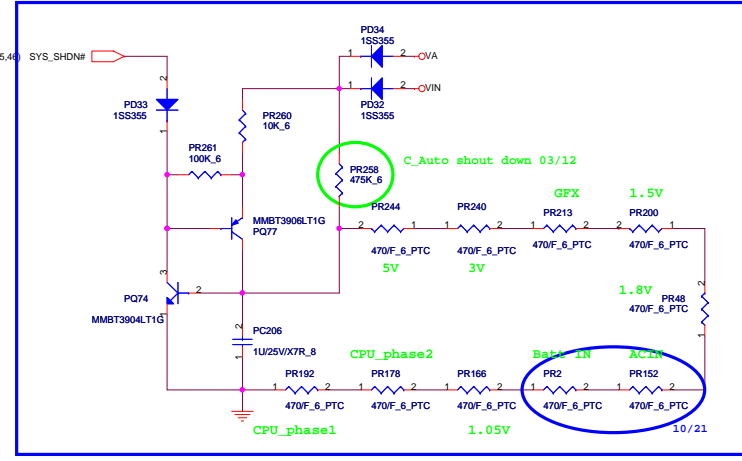
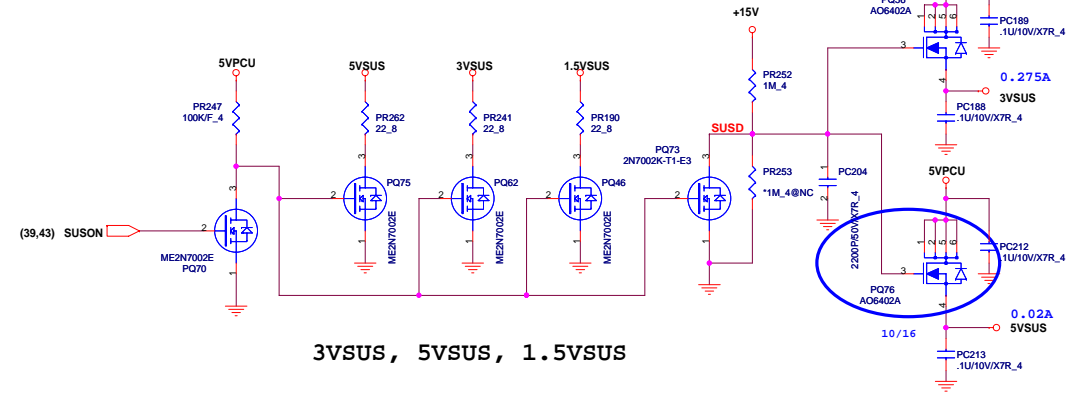
LANVCC

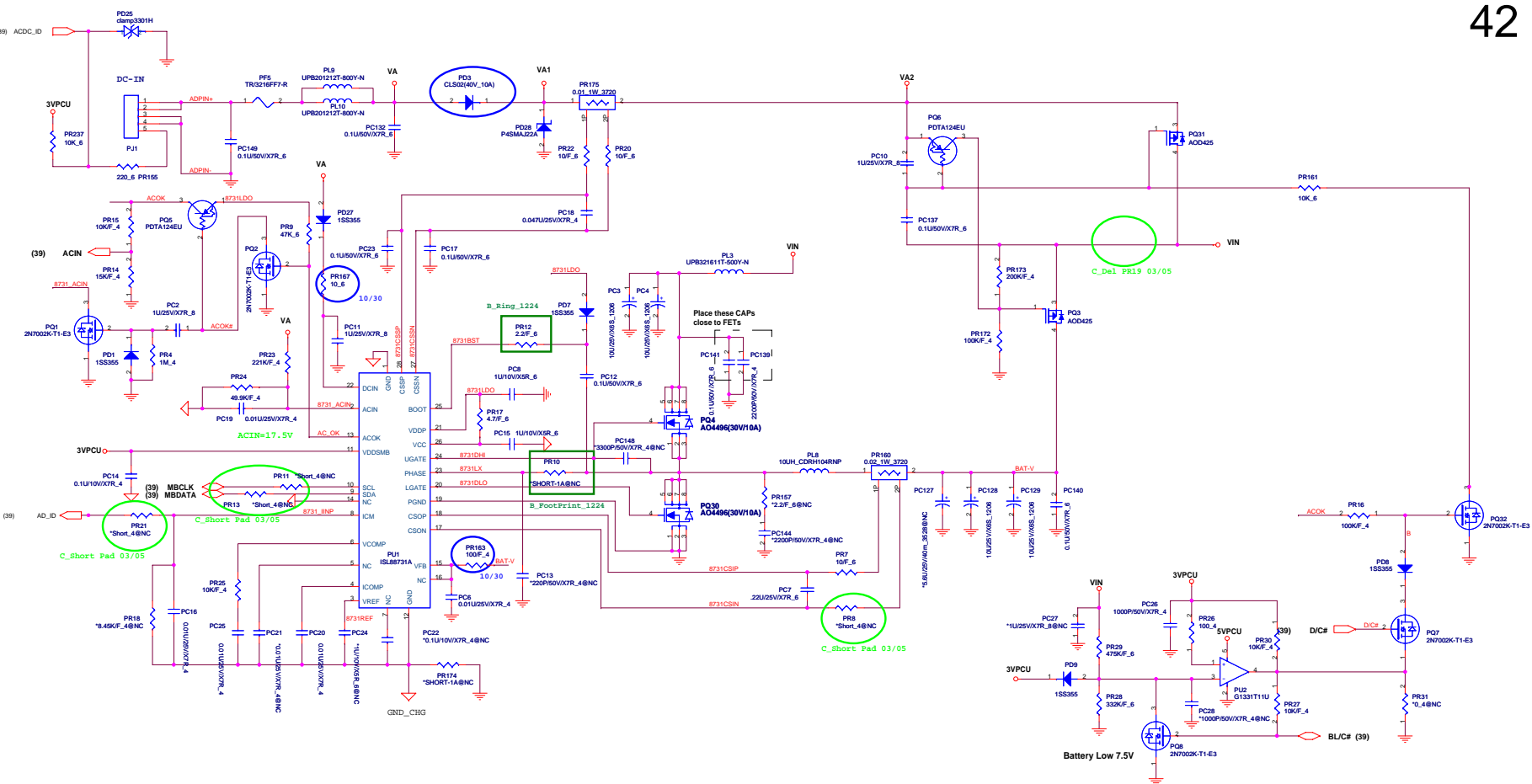


VCC\_CORE

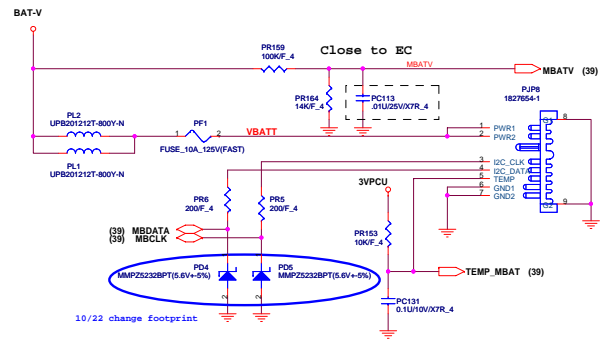


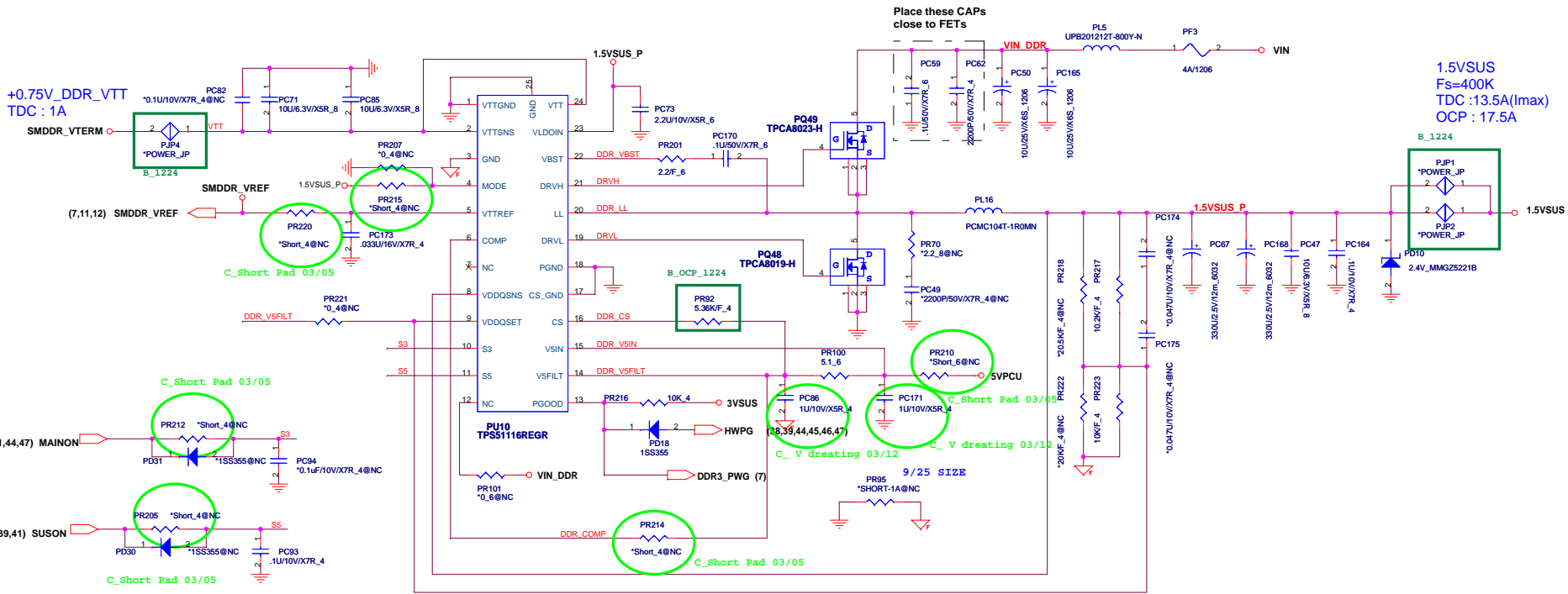
9/25 SIZE





C\_Delete circuit 03/05



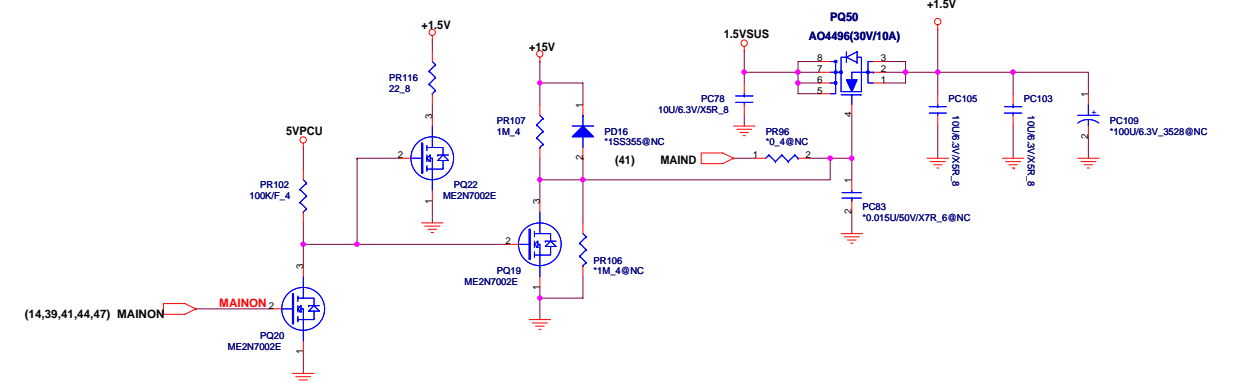
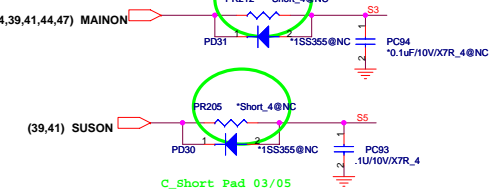


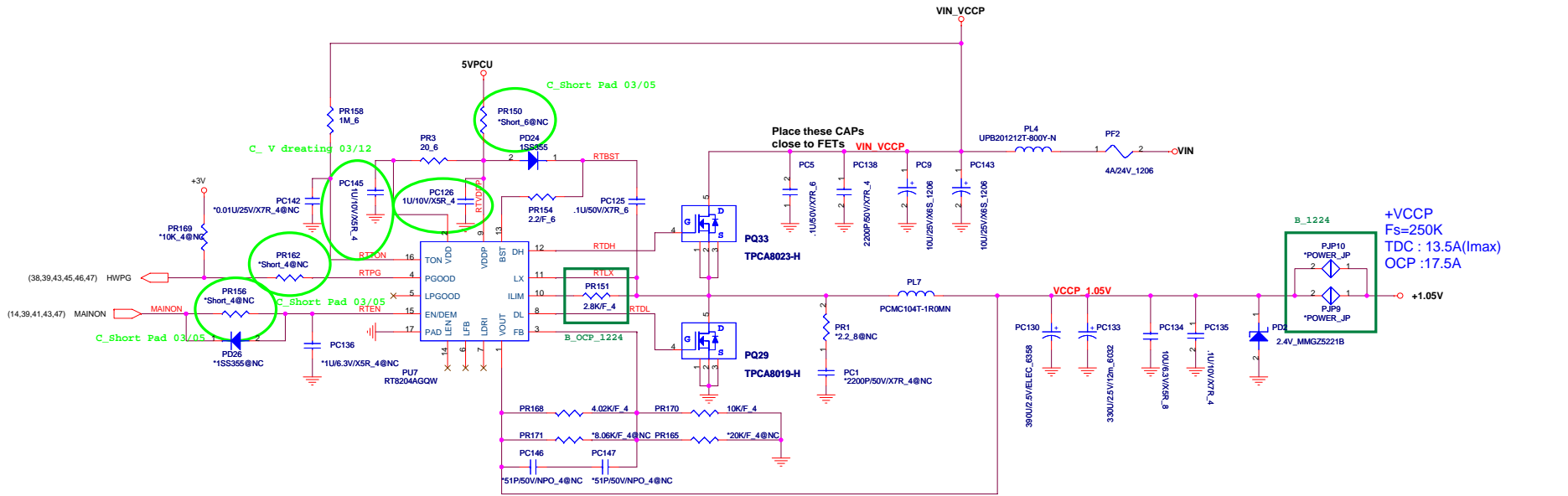
+0.75V\_DDR\_VTT  
TDC : 1A

1.5VSUS  
Fs=400K  
TDC :13.5A(I<sub>max</sub>)  
OCP : 17.5A

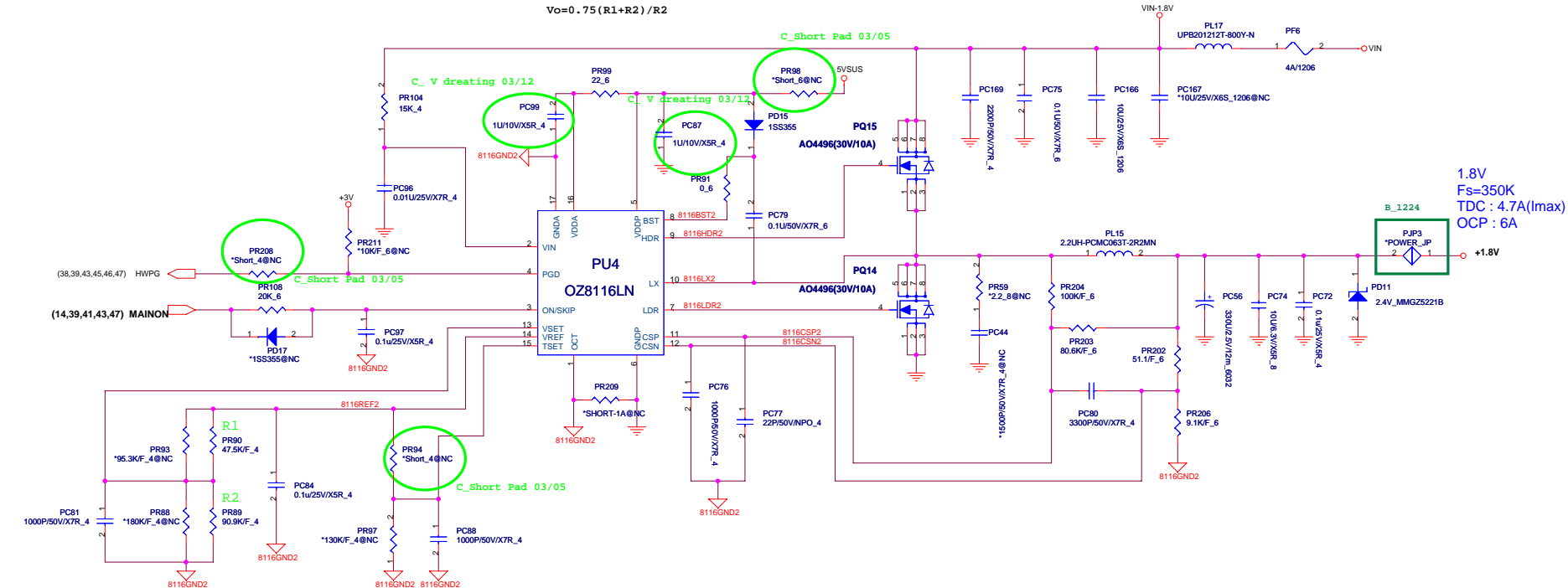
Place these CAPs  
close to FETs

MAX :3.2A



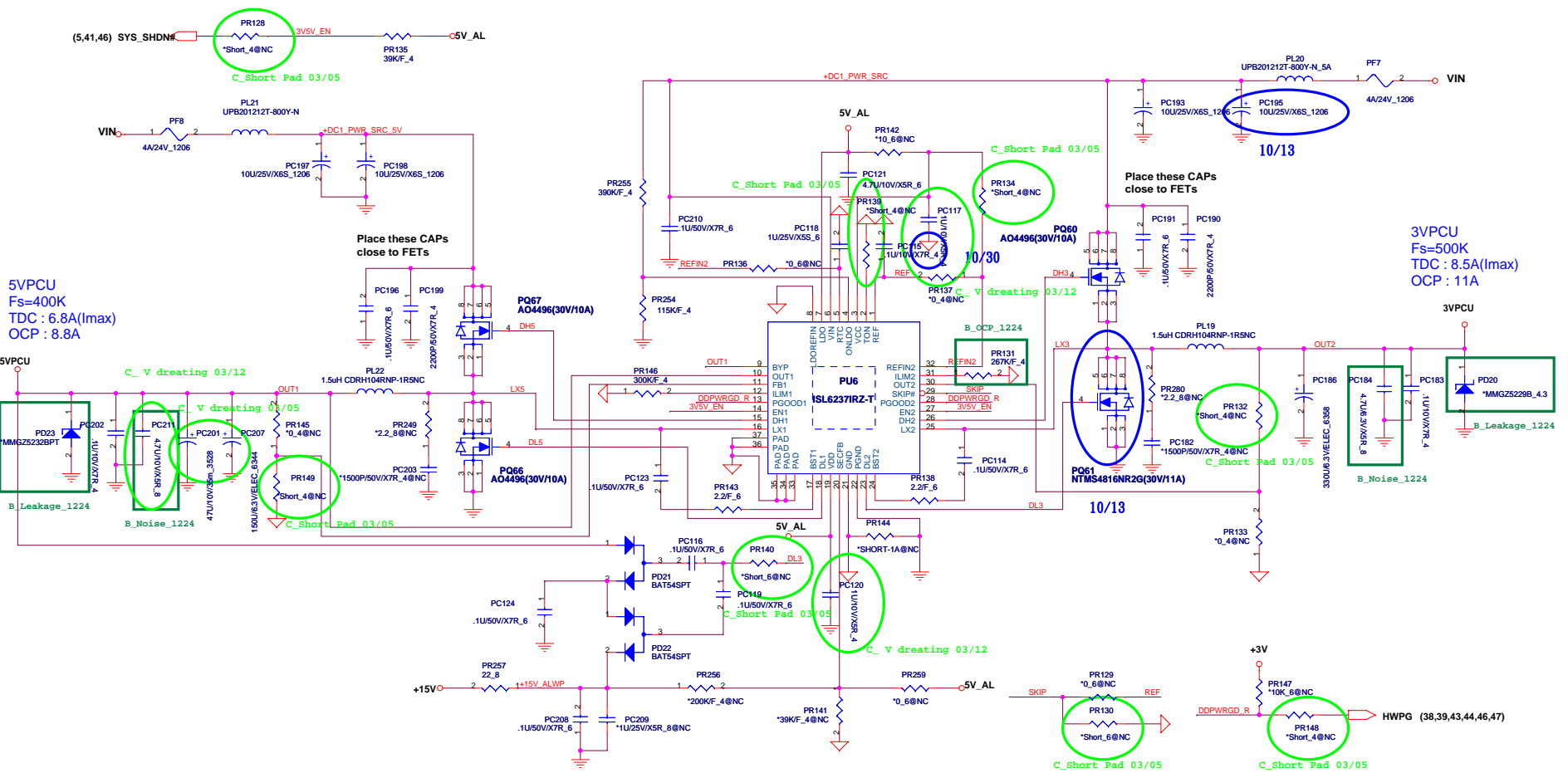


$$V_o = 0.75 (R1 + R2) / R2$$



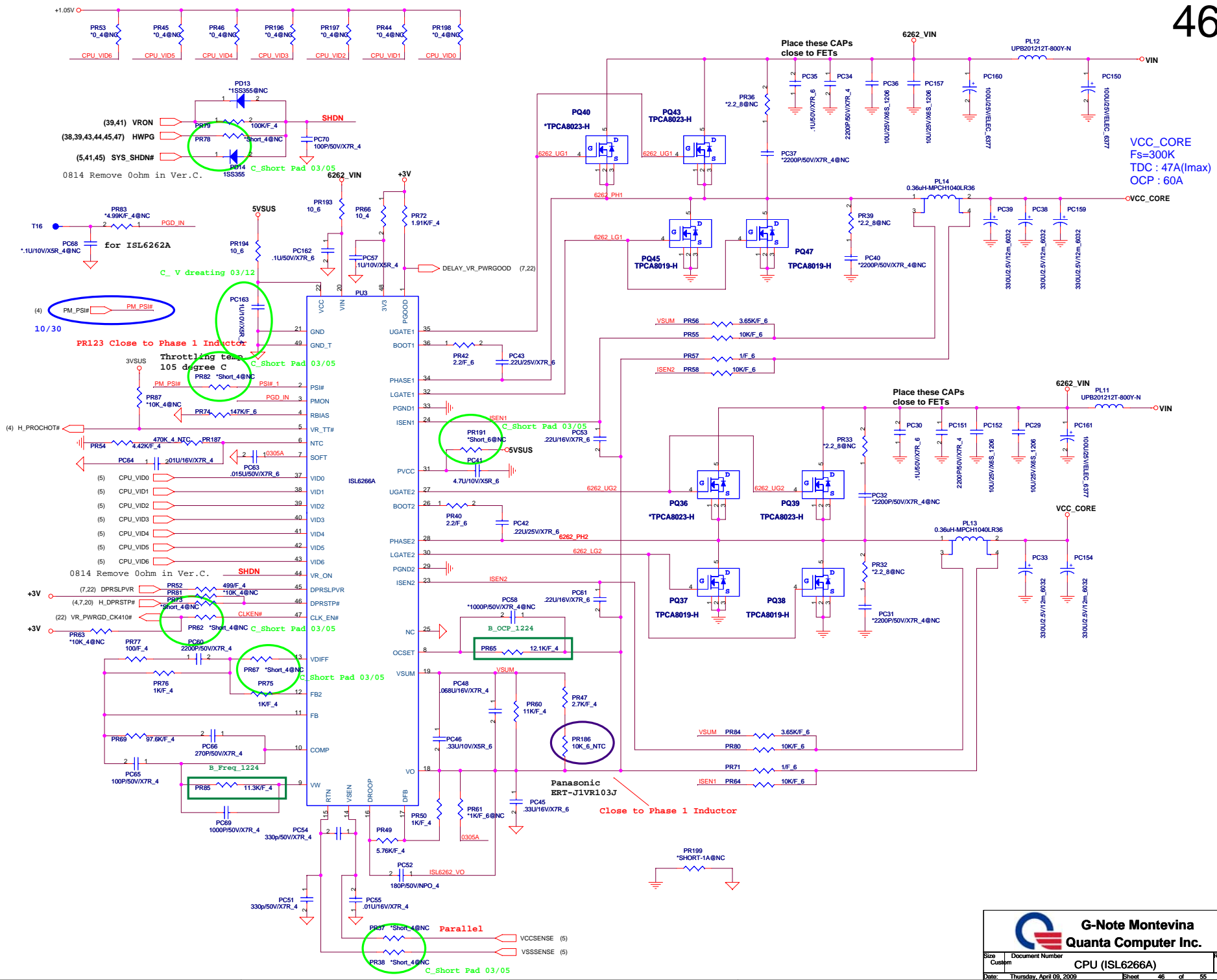


(20,25,27,29,31,37,38,41,42) 3VPCU  
 (41,42,43,44,47) 5VPCU  
 (25,33,41,43) +15V  
 (25,41,42,43,44,46,47) VIN

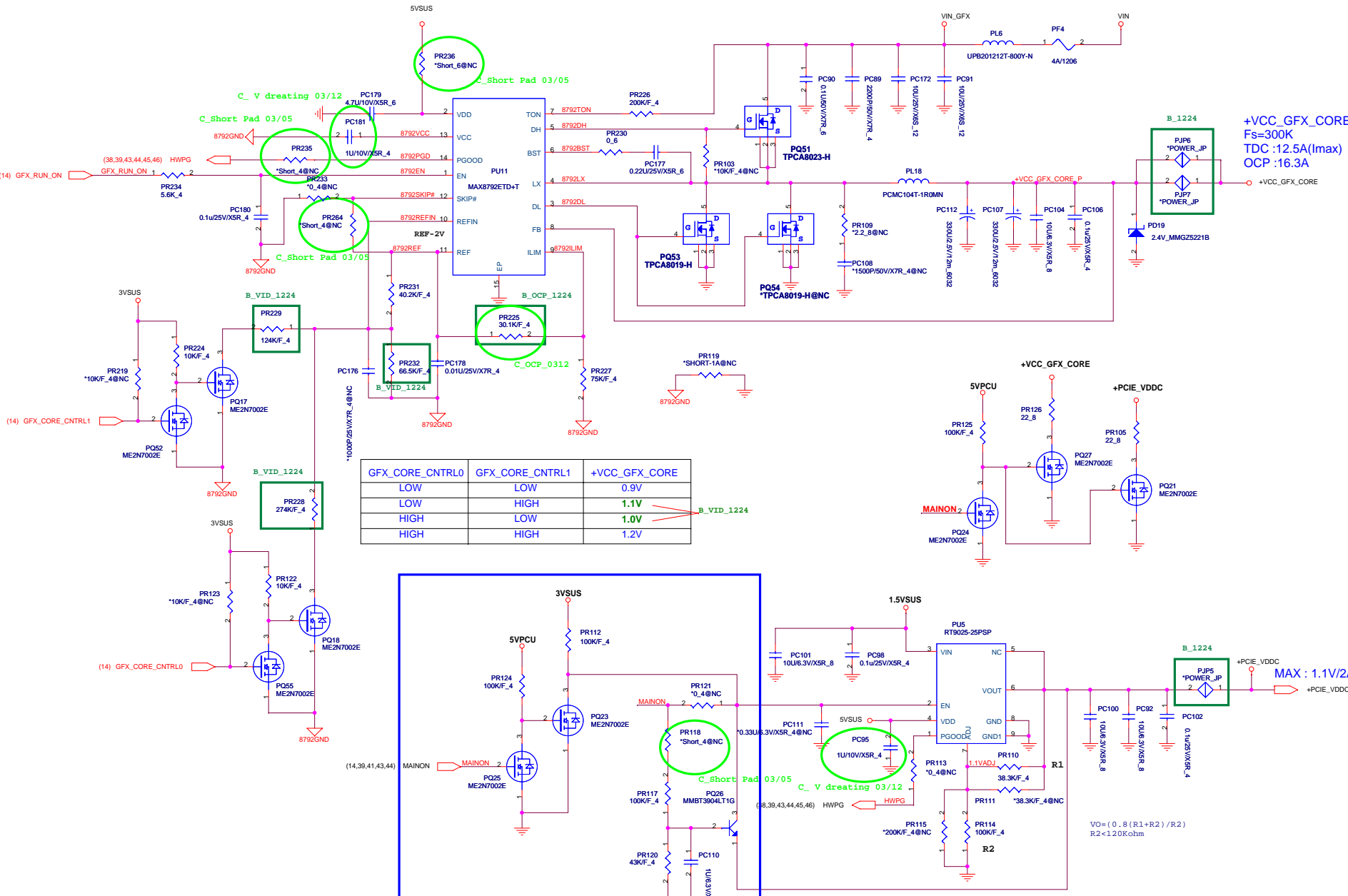


5VPCU  
 Fs=400K  
 TDC : 6.8A(I<sub>max</sub>)  
 OCP : 8.8A

3VPCU  
 Fs=500K  
 TDC : 8.5A(I<sub>max</sub>)  
 OCP : 11A



VCC CORE  
 Fs=300K  
 TDC : 47A(I<sub>max</sub>)  
 OCP : 60A



GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
LOW	HIGH	1.1V
HIGH	LOW	1.0V
HIGH	HIGH	1.2V

+VCC\_GFX\_CORE  
 Fs=300K  
 TDC :12.5A(I<sub>max</sub>)  
 OCP :16.3A

MAX : 1.1V/2A

# Revision History

Revision	Date	Phase	Change List	Release Schematic Date	Release Gerber File Date
1A		DV	Initial release		

## Schematic Value Explanation Description :

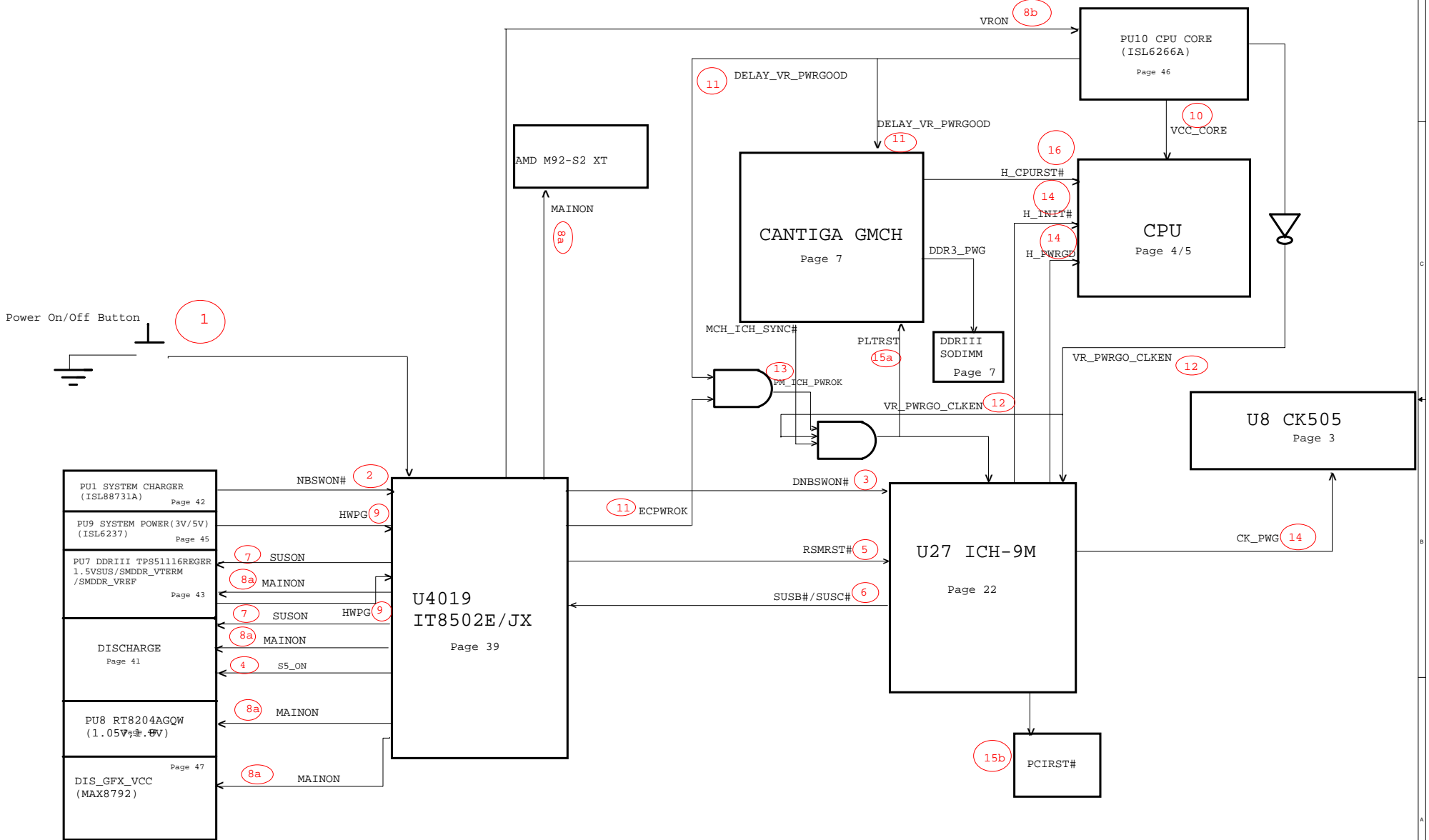
### RESISTOR

Value	F	4	6	8	12	1210	*	Description
*1K/F_4	1%	0402 (1005 )					DE POP	1K ohm 1% SMD 0402 package and DE POP
1K_6	5%		0603 (1608 )				POP	1K ohm 5% SMD 0603 package and POP
1K_8	5%			0805 (2125 )			POP	1K ohm 5% SMD 0805 package and POP
1K_12	5%				1206 (3216 )		POP	1K ohm 5% SMD 1206 package and POP
1K_1210	5%					1210 (3225 )	POP	1K ohm 5% SMD 1210 package and POP

### CAPACITOR

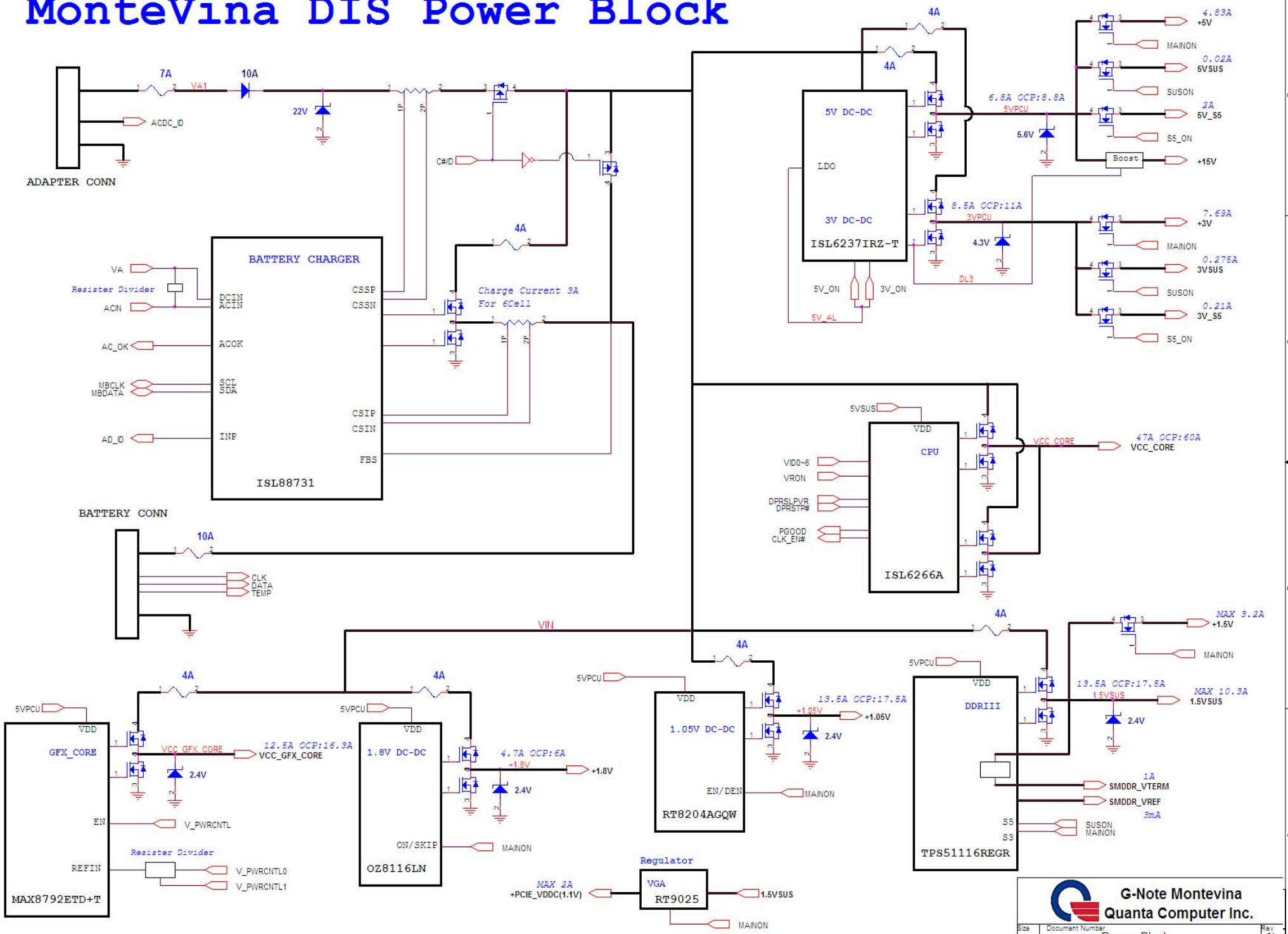
Value	Voltage	Material	6				*	Description
*0.1U/10V/X5R_4	10V	X5R	0402 (1005 )				DE POP	0.1UF 10V X5R SMD 0402 package DE POP
1U/25V/X7R_6	25V	X7R	0603 (1608 )				POP	0.1UF 25V X7R SMD 0603 package POP







# MonteVina DIS Power Block



EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-A-01	42	12/24	PR10	Change Footprint
EC-A-02	42	12/24	PR12	Change to 2.2 ohm reduce phase ring
EC-A-03	42	12/24	PD6	Delete Footprint
EC-A-04	43	12/24	PJP1,PJP2,PJP4	Change Footprint
EC-A-05	43	12/24	PR92	Change to 5.36K for OCP
EC-A-06	44	12/24	PR151	Change to 2.8K for OCP
EC-A-07	44	12/24	PJP3,PJP9,PJP10	Change Footprint
EC-A-08	45	12/24	PR131	Change to 267K for OCP
EC-A-09	45	12/24	PC134,PC211	Change to 4.7u reduce H.F. noise reduce
EC-A-10	45	12/24	PD20,PD23	NA to reduce leakage current
EC-A-11	46	12/24	PR65	Change to 12.1K for OCP
EC-A-12	46	12/24	PR85	Change to 11.3K for frequency 300KHz
EC-A-13	47	12/24	PJP5,PJP6,PJP7	Change Footprint
EC-A-14	47	12/24	PR225	Change to 80.6K for OCP
EC-A-15	47	12/24	PR228,PR229,PR232	Change for VID point setting



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	EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION	
<b>A stage</b>	2008	EC-A-01	29	12/08	U10	Change LAN IC footprint from (LQFP48-9X9-4)0.4 to (LQFP48-9X9-5)0.5 pitch
		EC-A-02	28	12/08	U32	Change Codec IC footprint to qfn48-7x7-5-58p-0_9h.(Add 9 via at the center PAD of original IC footprint)
		EC-A-03	38	12/08	U49	Change U49 schematic by adding R562,R563,R564 and D24 to solve F4 error code issue.
		EC-A-04	25	12/08	R196	Delete CCD_ON which was use to control CAM_VCC by change R196 from depop to pop and delete U16,C353,R204,R211,R219,R221.
		EC-A-05	14	12/08	R399	Add R399 to pull low CPIO_19_CTF according to AMD FAE suggestion.
		EC-A-06	22	12/08	R347	Replace CCD_ON with HDD_DETECT#, original HDD_DETECT# will cause FF error code while attached HDD.
		EC-A-07	03	12/08	R313	Change to 4.7Kohm To solve N.B. cannot get correct FSB frequency selection (error coed 02)
		EC-A-08	36	12/08	CN11	Add CLKRUN#,SERIRQ,LPC_LDRQ0#,LPC_PD#
		EC-A-09	39	12/08	R565,R566	Add adapter selection board ID by adding R565 an R566.
		EC-A-10	25	12/08	Q13	Change Q13 connection.
		EC-A-11	37	12/08	R567,R568	Add optional resistor between MY11 and MY13
		EC-A-12	28	12/11	C465,C426,C427, C506,C507,C499, C495,C497,C455	Change footprint from 0805 to 0603 per mechanical request.
		EC-A-13	25	12/19	CN5	Connect LCD connector shielding to GND for better EMI performance.
		EC-A-14	36	12/23	C679,Q35,Q36A, Q36B,R506,R510, R511,R519,R521	Delete redundunt schematic to save space for layout.
		EC-A-15	05	12/23	C708,C709,Q38, Q39,Q40,R569, R570,R571,R572, R573,R574,U53	Change thermal sensor.
		EC-A-16	29	12/23	R579,R580	Add IO_GND1 for LAN connector per EMI request.
		EC-A-17	26	12/24	R581,R582,R583, Q41,Q42	Change HP_DET schematic for better ESD protection and prevent floating
		EC-A-18	28	12/30	U54,D26,D27, C710	Add new schematic to prevent "POP" sound.
		EC-A-19	37	12/30	CN12	Add CN12 for 14" PCB due to mechanical design limit.
2009	EC-A-20	27	01/07	CN27	Change pin define of CN27 by intercept GND pin between differential pair per EMI request.	




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EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
2009	37	02/24	CN2	Delete CN2(extra right button/b connector)
	30	02/24	CN19	Delete CN23 (extra ODD connector)
	29	02/24	CN20	Swap PIN3 and PIN14 to correct the LED behavior.
	3	02/26	C664,C665,C667, C672,C685,CN9, R488,R489,R491, R492,R494,R496, R515,U46,C324, C325,RP4,R293	Delete one minicard slot per customer request.
	21			
	35			
	30	02/26	CN4	Reverse the pin define of KB connector for the convenience of assembly.
	33	02/26	R584	Insert 10 ohm resistor(10_6) between FET and VDD(G-sensor) for Analog noise reduction.
	03	02/27	C403,L2,L56,R322, R105,R113,R127,R131, R133,R142,R143,R151, R159,R16,R160,R167, R180,R186,R579,R261, R269,R329,R339,R355, R356,R214,R22,R252, R255,R267,R550,R278, R282,R284,R286,R294, R312,R314,R33,R332, R338,R340,R547,R351, R353,R354,R367,R377, R401,R402,R405,R415, R429,R435,R436,R454, R493,R502,R505,R514, R518,R522,R567,R568 R525,R529,R531,R534, R537,R580,R543,R545, R546,R9,R38,R65,RP3, RP4,RP5,RP6,RP7, R569,R48,R362,R92, R119,R32,R36,R444, R447,R485R162,R163, R189,R192,R200,R206, R216,R227,R237,R244, R548,R549,R551,R552, R553,R554,R60,R101, R102,R364,R201,R207	Delete redundant 0 ohm or change it to short pad in the circuit.
	10			
	13			
	14			
	17			
	22			
	23			
	24			
	25			
	27			
	28			
	29			
	30			
	31			
	32			
	36			
	39			


B stage

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2009

**B stage**

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-B-08	31	03/03	R486,R487	Add but no assembly
EC-B-09	34	03/03	C501	Add
EC-B-10	34	03/03	R585,R586	Disconnect SMB and change it to pull high 10K to 3VAUX
EC-B-11	36	03/03	R523,R524	Change to 4.7K and pull high to 3VWLAN
EC-B-12	36	03/03	R526,R528	Change to 4.7K and pull high to 3VWWAN
EC-B-13	38	03/03	C684,D24,D25, R403,R562,R563, R564,U49	Change RFID IC package to TSSOP.
EC-B-14	28	03/04	C711,C712	Reserve 1u capacitor between L+,L- and R+,R- for EMI
EC-B-15	22	03/04	R223,R224, R239,R250	Change board ID for SIT stage.
EC-B-17	28	03/06	R272,R273,R274, R275	Add R272,R273,R274,R275 for EMI
EC-B-18	26	03/06	D21	
EC-B-19	25 32	03/12	F3,F4,F5	
EC-B-20	37	03/09	C713,C714,C715, C716,C717,C718, C719,C720	Add capacitor for EMI
EC-B-21	03	03/09	R357,R323,R279	Due cpu clock already fix,so delete redundant parts.
EC-B-22	31	03/10	R587,R588,R589, R590,R591,R592	Add EMI filter for RF
EC-B-23	44	03/16	PD17	Assembly PD17 to correct VGA graphic power off sequence.
EC-B-24	25	03/12	R593,C311,C312	Add bead for EMI
EC-B-26	24	03/17	D14,D15,D16, D17,D18,D19, D20	Change CRT ESD protection from Switching Diode to Transient Voltage Suppressors.
EC-B-27	22,39	03/30	R347	Change HDD_DETECT# connection from ICH9 to KBC
EC-B-28	25,37 39	04/07	Q17,Q19,R169, R174,R175	Delete LOGO Led for cost down
EC-B-29	25 39	04/07	R541,C309,Q13, Q14,R165,R166	Delete THINK light for cost down
EC-B-30	27	04/08	R555,R556,R557	Fine tune battery and suspend LED brightness
EC-B-31	29	04/10	U11,U15	Replace TVS between transformer and LAN IC for Hi-pot test



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