Compal Confidential

PEW71/91/51 M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M

NV N11P-GV2H and N11P-GE,N12P-GS N12P-GV-OP With Optimus

2010-12-29

REV:1.0

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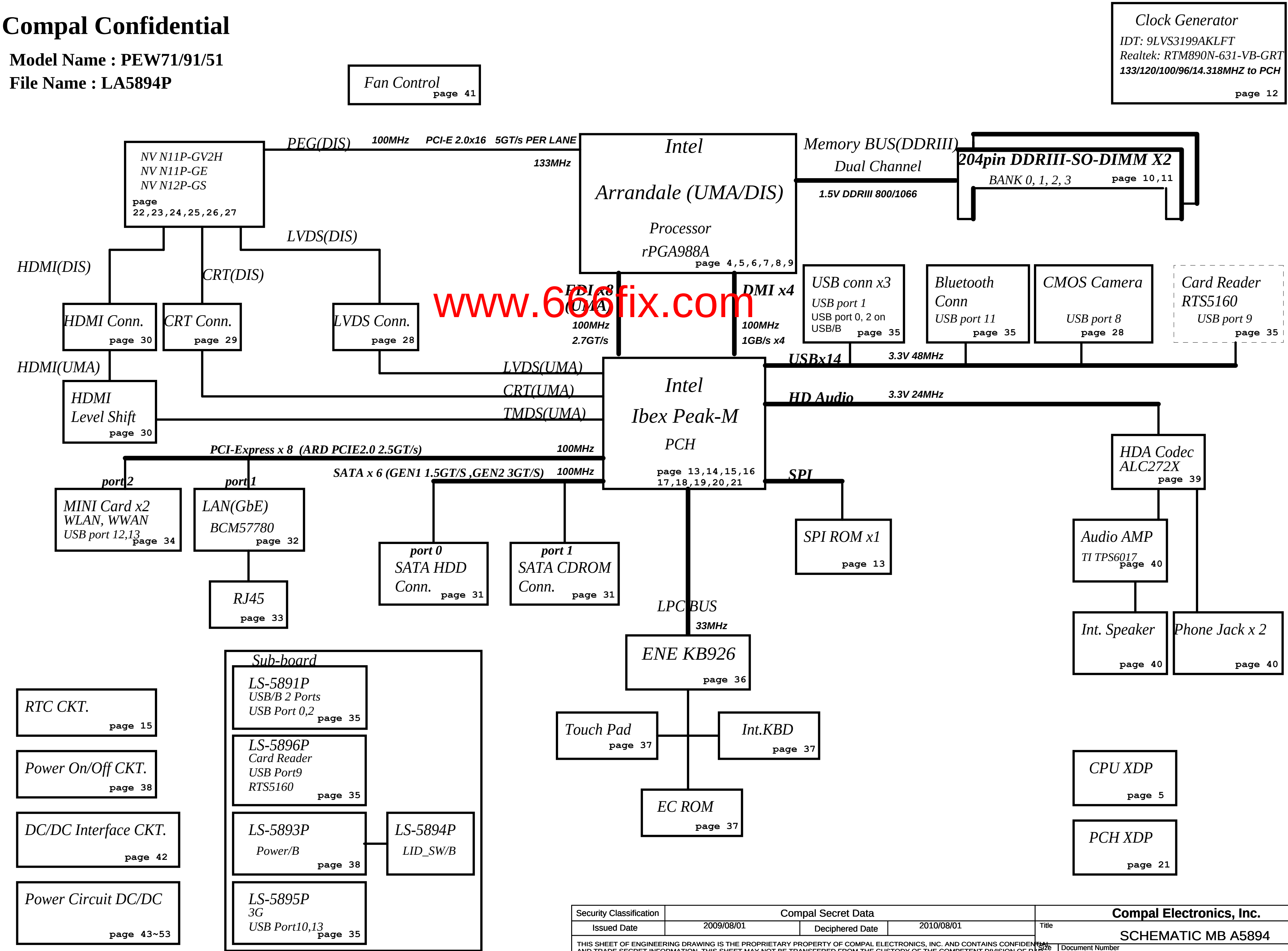
Model Name : PEW71/91/51

File Name : LA5894P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for Arrandale GPU (only for arrandaleCPU)	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for ARD CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3V	+3VALW to +3V power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V	+5VALW to +5V switched power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA ONLY	UMA ONLY@
Discrete	DIS@
Discrete Only	DIS ONLY@
VRAM	X76@
Switchable	SG@
UMA ONLY & OPTIMUS	UMOP@
3G	3G@
Blue Tooth	BT@
OPTIMUS	OPT@
NonSG SKU	NonSG@
NEW71	71@
NEW91	91@
N11P-GV2H	GV2H@
N11P-GE1	GE1@
N11P-GV2H-A2	GV2HA2@
N11P-GV2H-A3	GV2HA3@
Non OPT SKU	NonOPT@
SG or OPT	SGOPT@
N11P-GE	GE@
N12P-GS	GS@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
	UHCI1	2	USB/B (Right Side)
		3	
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Camera
		9	Card Reader
	UHCI5	10	SIM Card
		11	Blue Tooth
	UHCI6	12	Mini Card(WLAN)
		13	Mini Card(GPS)

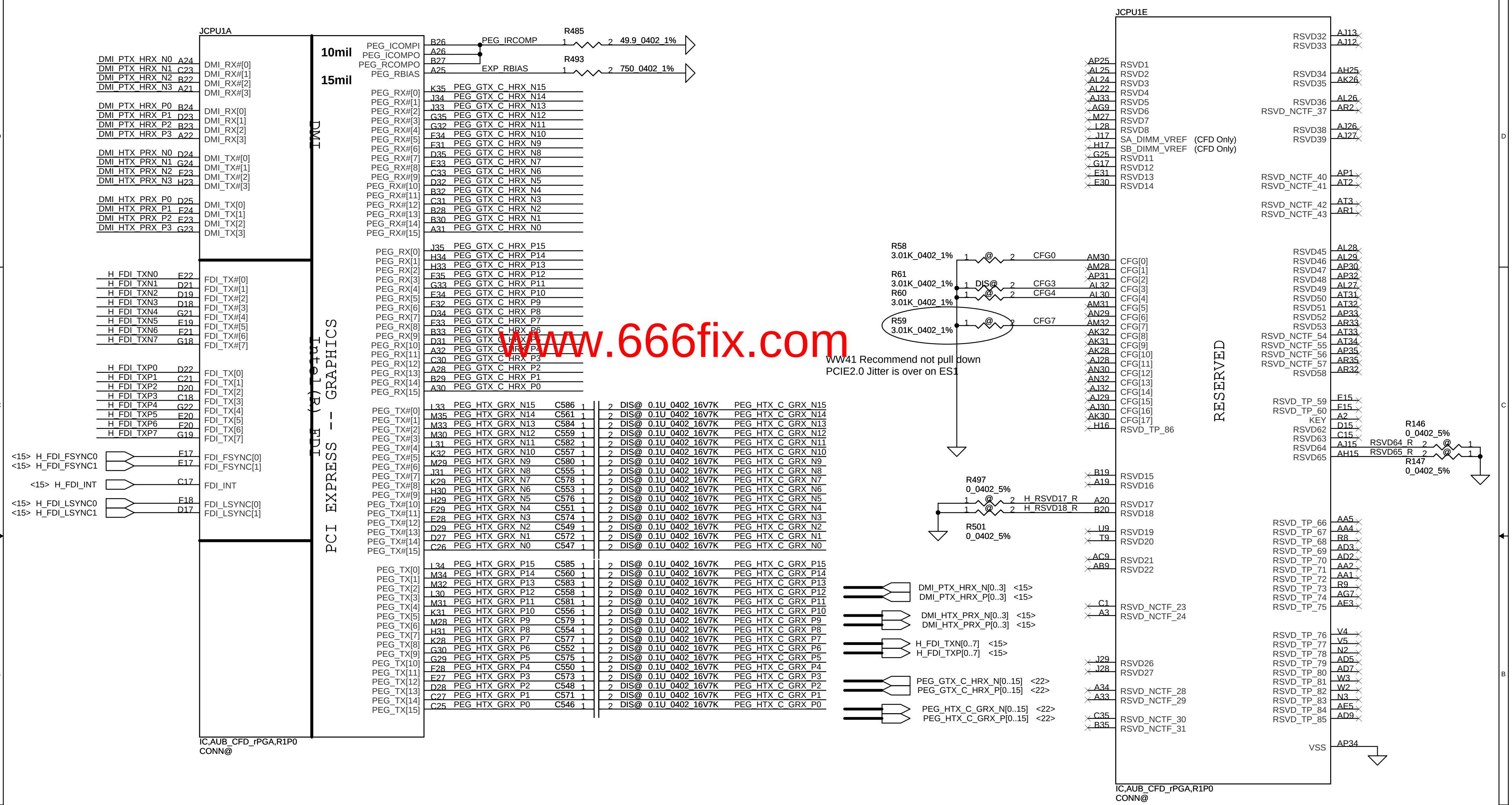
BOM Config move to page 56

VRAM BOM Config

X7621@: X76198BOL21 ALT. GROUP PARTS 1G SAM

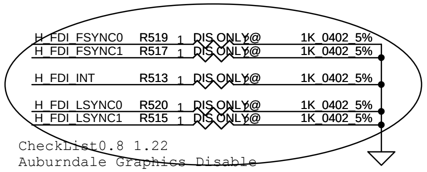
X7622@ X76198BOL22 ALT. GROUP PARTS 1G HYN

VRAM P/N :
Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)
Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO!)



eDP Signals Mapping

eDP Singal	PEG Singals	Lane Reversal
eDP_TX0	PEG_HTX_C_GRX_P15	PEG_HTX_C_GRX_P0
eDP_TX#0	PEG_HTX_C_GRX_N15	PEG_HTX_C_GRX_N0
eDP_TX1	PEG_HTX_C_GRX_P14	PEG_HTX_C_GRX_P1
eDP_TX#1	PEG_HTX_C_GRX_N14	PEG_HTX_C_GRX_N1
eDP_TX2	PEG_HTX_C_GRX_P13	PEG_HTX_C_GRX_P2
eDP_TX#2	PEG_HTX_C_GRX_N13	PEG_HTX_C_GRX_N2
eDP_TX3	PEG_HTX_C_GRX_P12	PEG_HTX_C_GRX_P3
eDP_TX#3	PEG_HTX_C_GRX_N12	PEG_HTX_C_GRX_N3
eDP_AUX	PEG_GTX_C_HRX_P13	PEG_GTX_C_HRX_P2
eDP_AUX#	PEG_GTX_C_HRX_N13	PEG_GTX_C_HRX_N2
eDP_HPD#	PEG_GTX_C_HRX_P12	PEG_GTX_C_HRX_P3



CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

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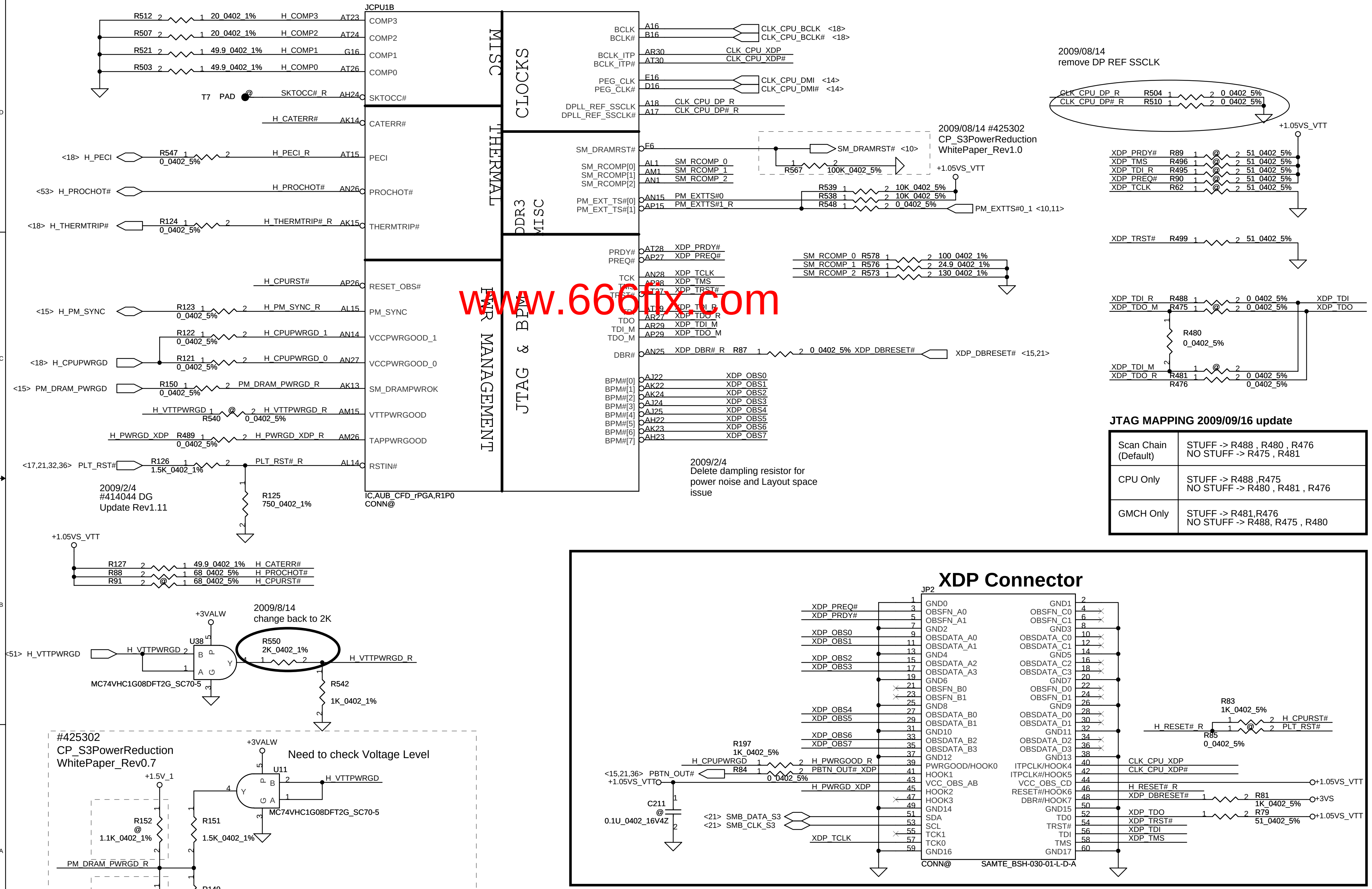

JTAG MAPPING 2009/09/16 update

Scan Chain (Default)	STUFF -> R488 , R480 , R476 NO STUFF -> R475 , R481
CPU Only	STUFF -> R488 ,R475 NO STUFF -> R480 , R481 , R476
GMCH Only	STUFF -> R481,R476 NO STUFF -> R488, R475 , R480

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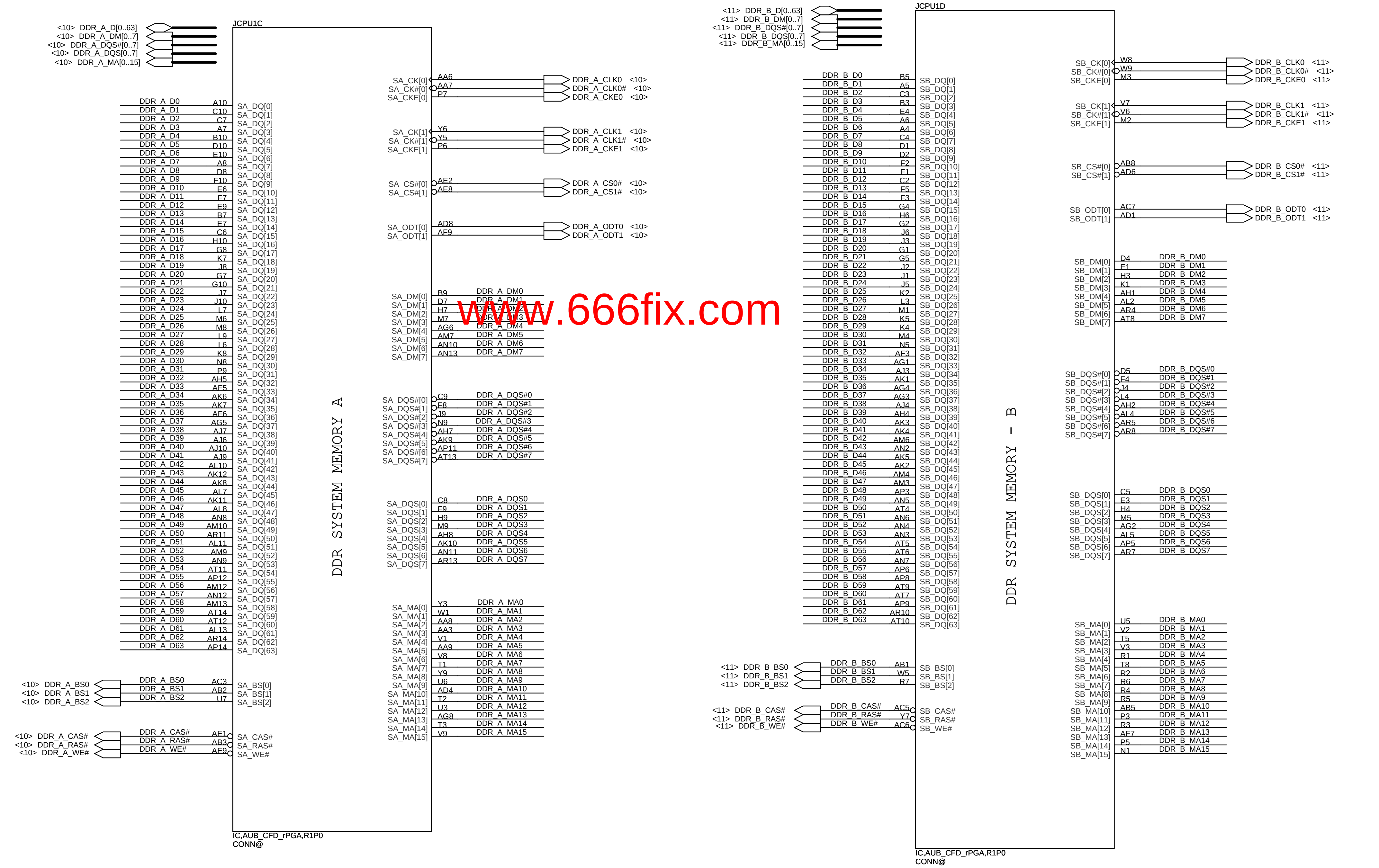

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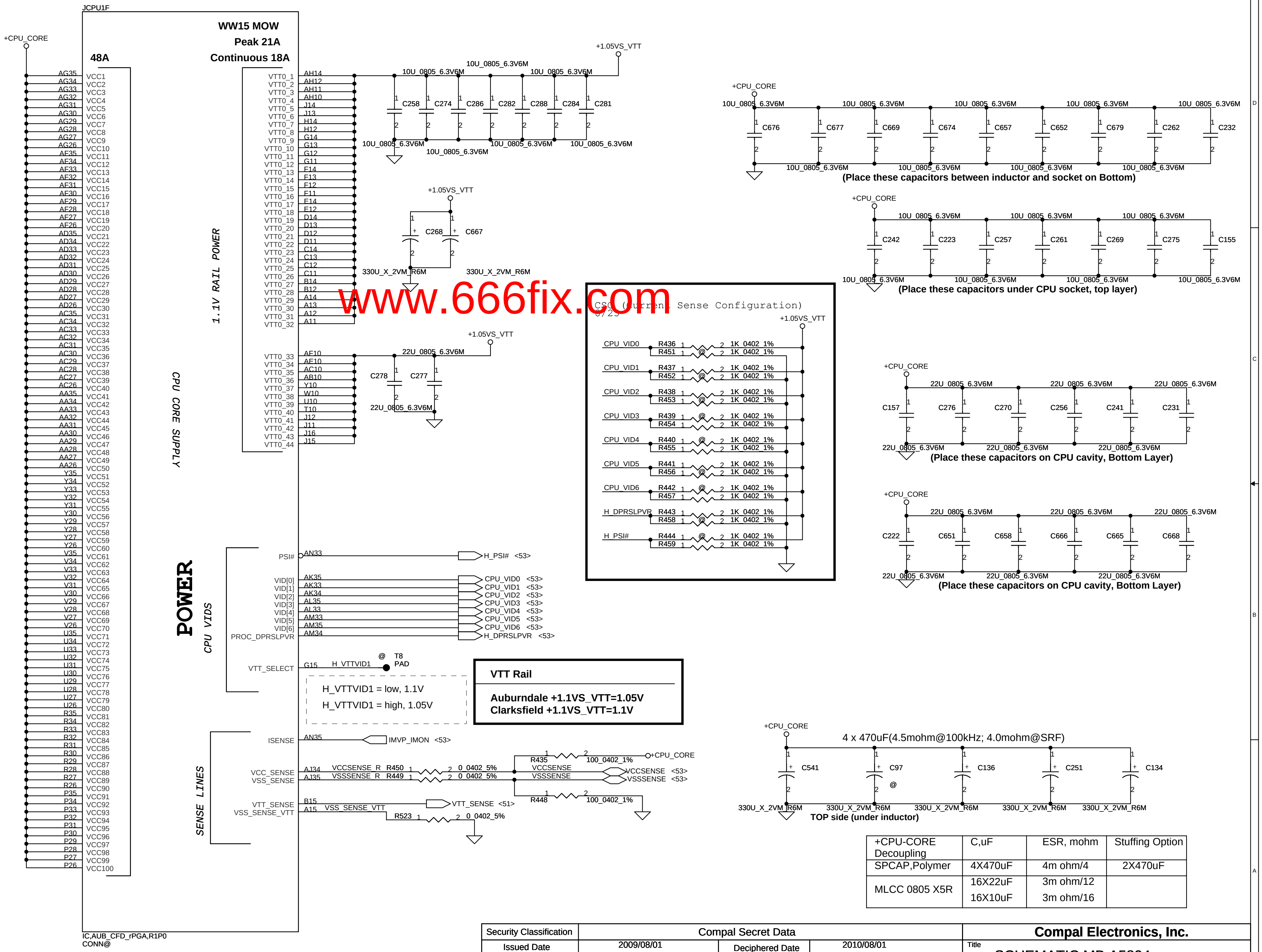

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF	3m ohm/12	
	16X10uF	3m ohm/16	

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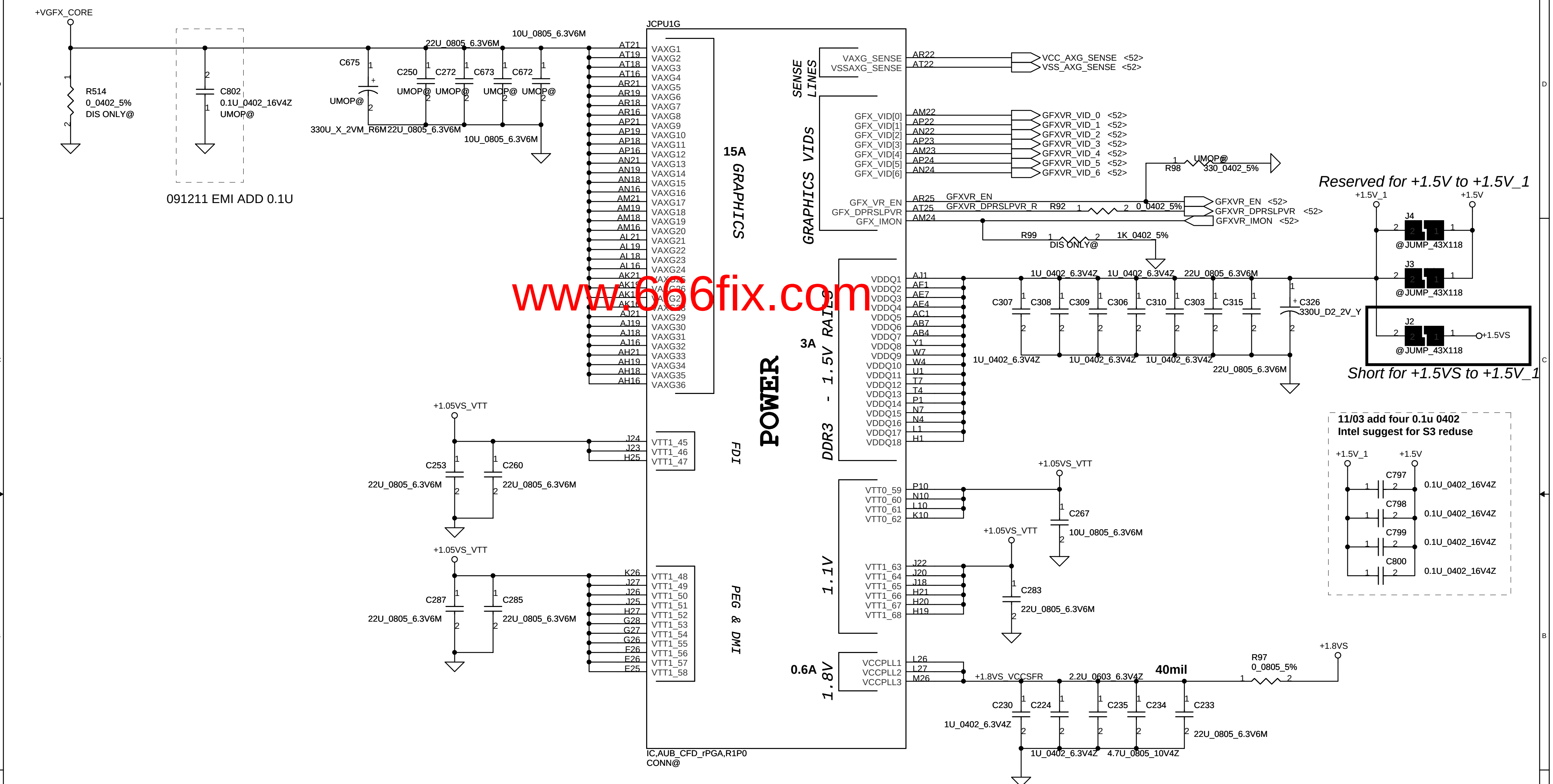

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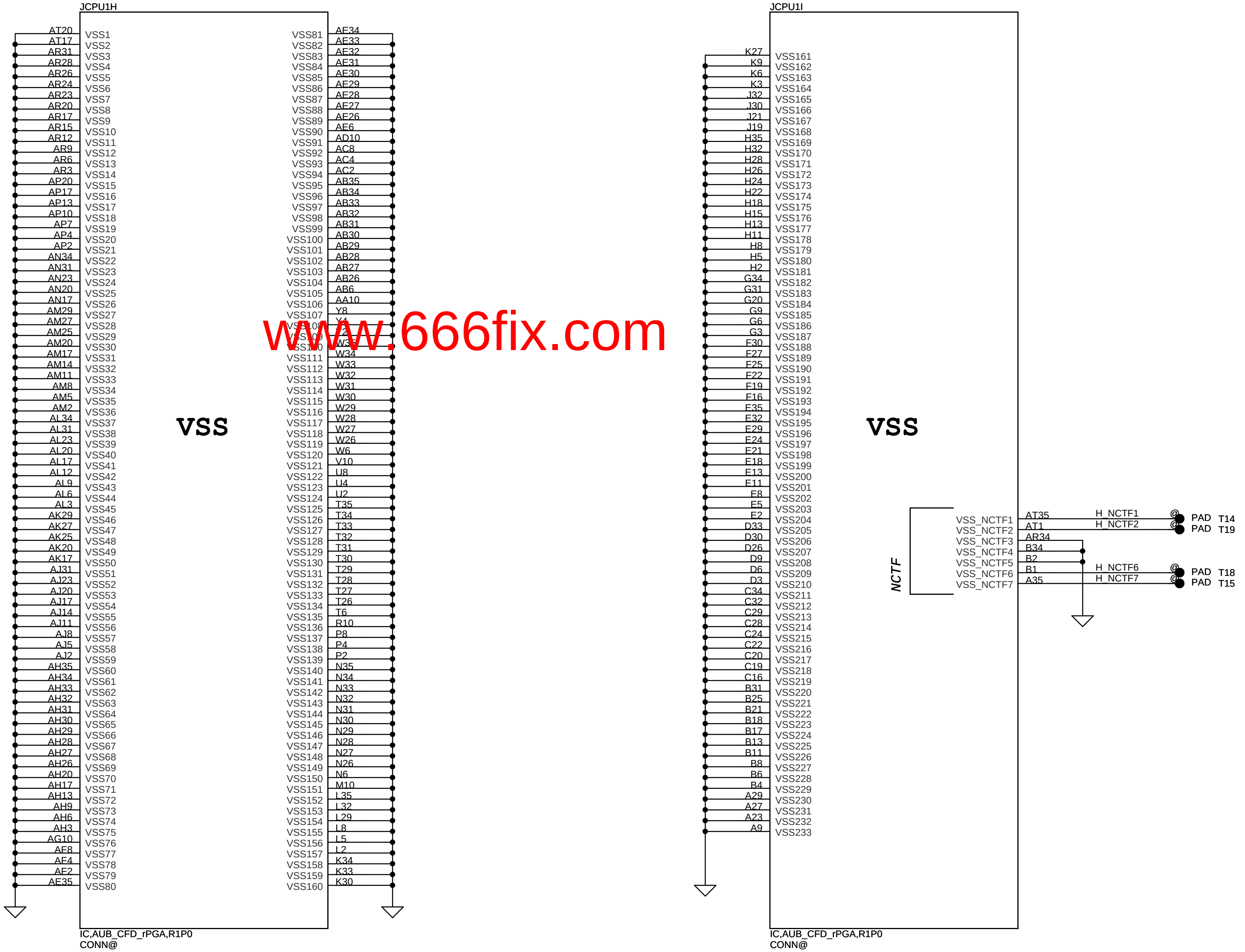

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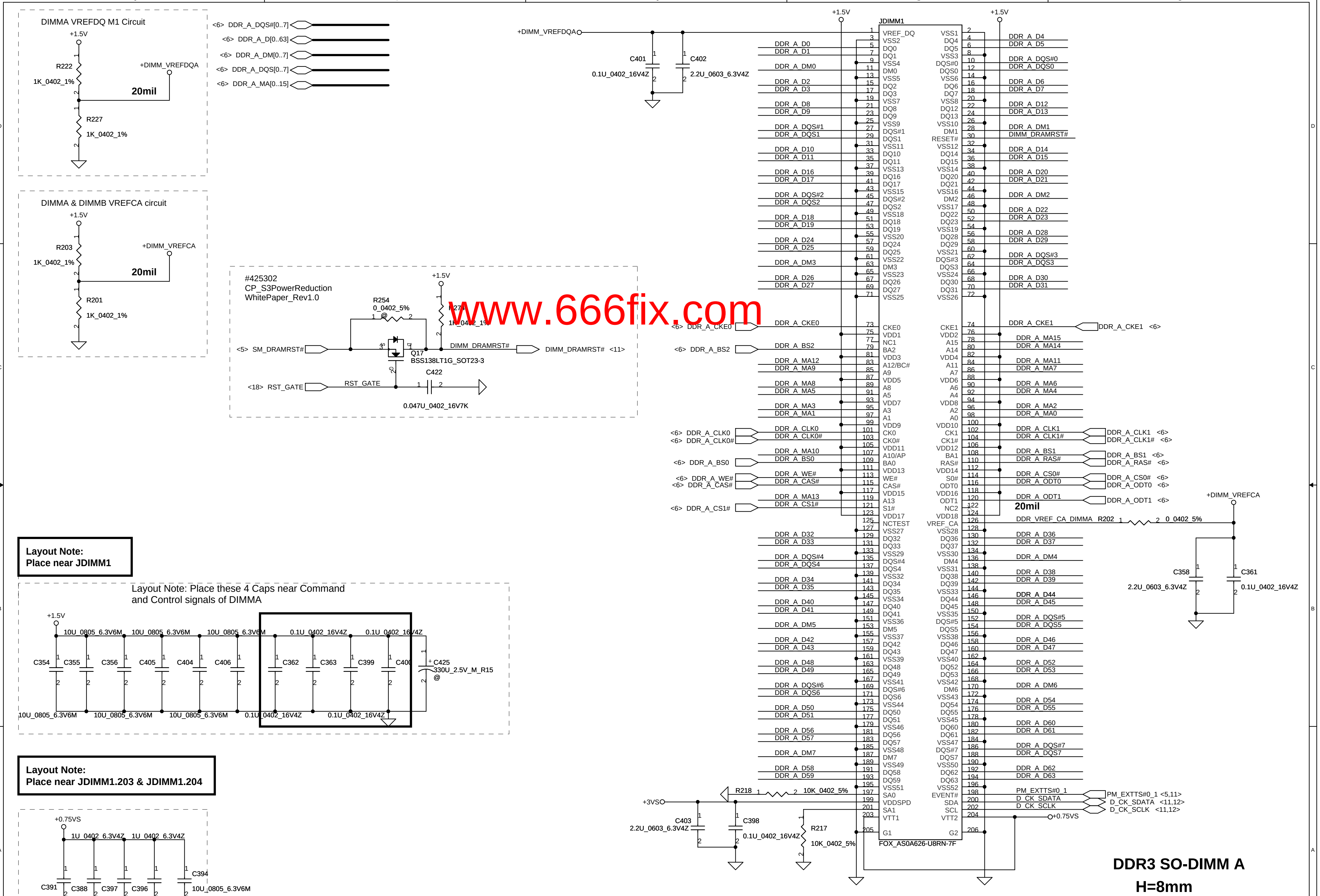

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DDR3 SO-DIMM A
H=8mm

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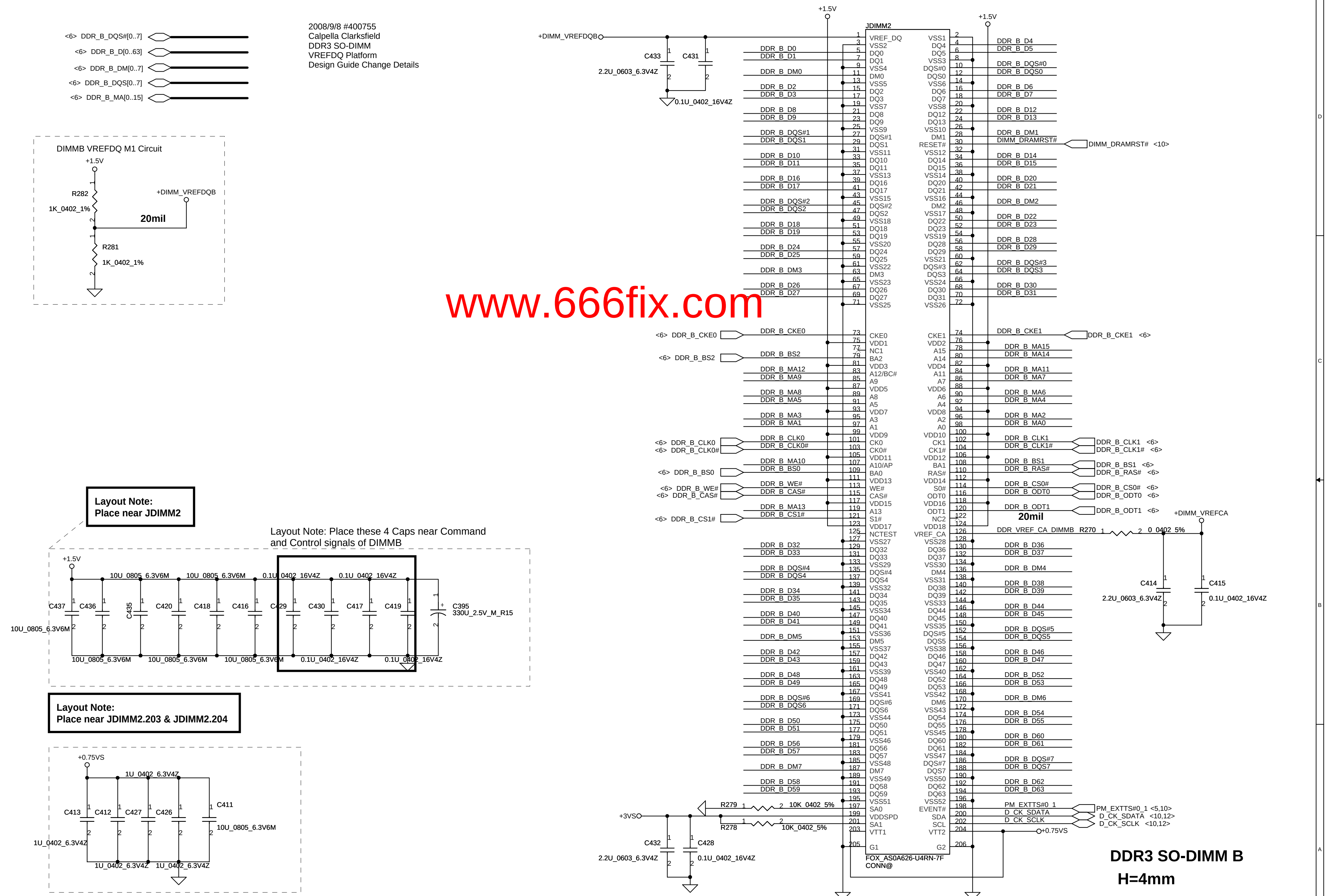

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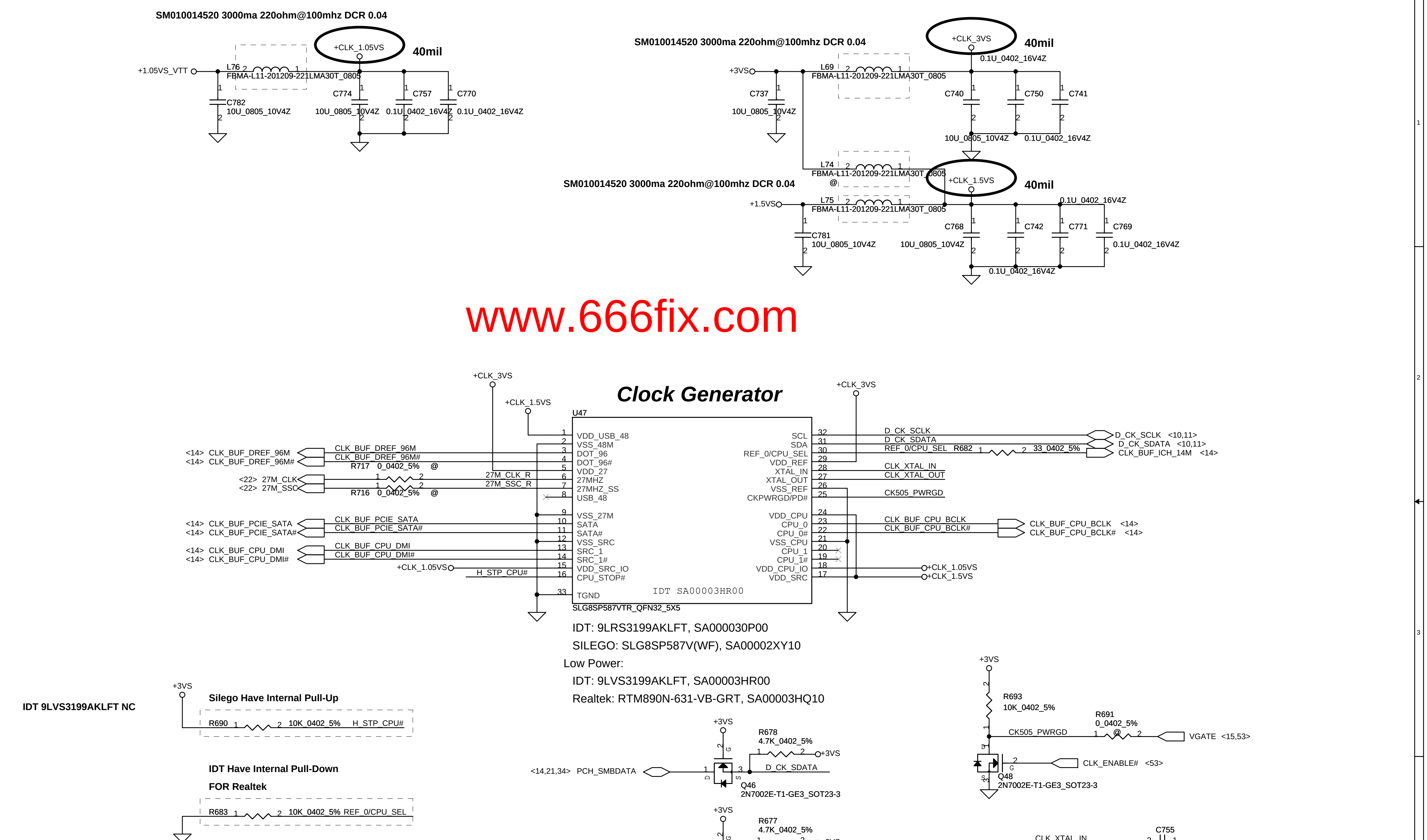

PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

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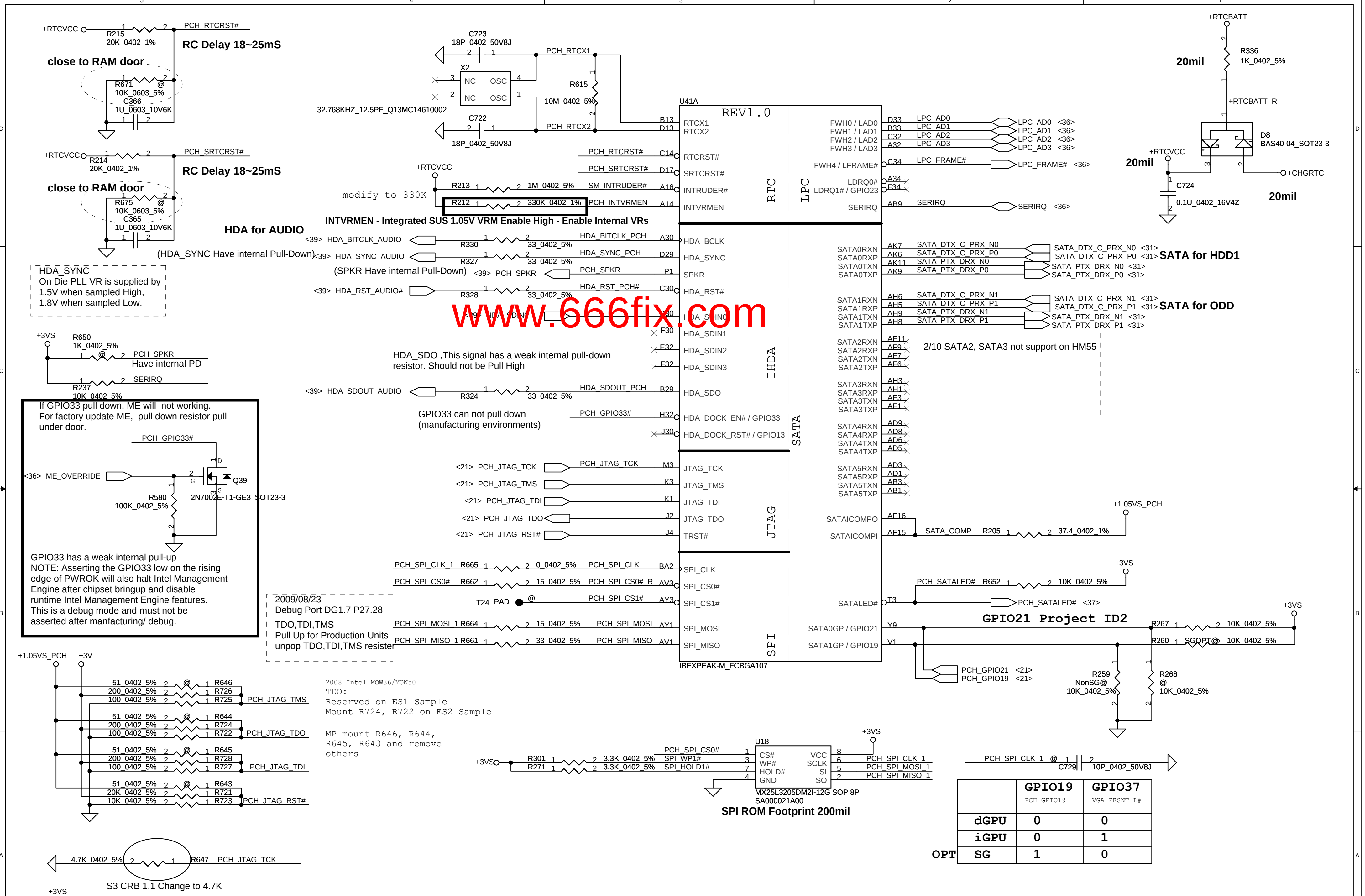

	GPIO19 (PCH_GPIO19)	GPIO37 (VGA_PRSNT_L#)
dGPU	0	0
iGPU	0	1
OPT SG	1	0

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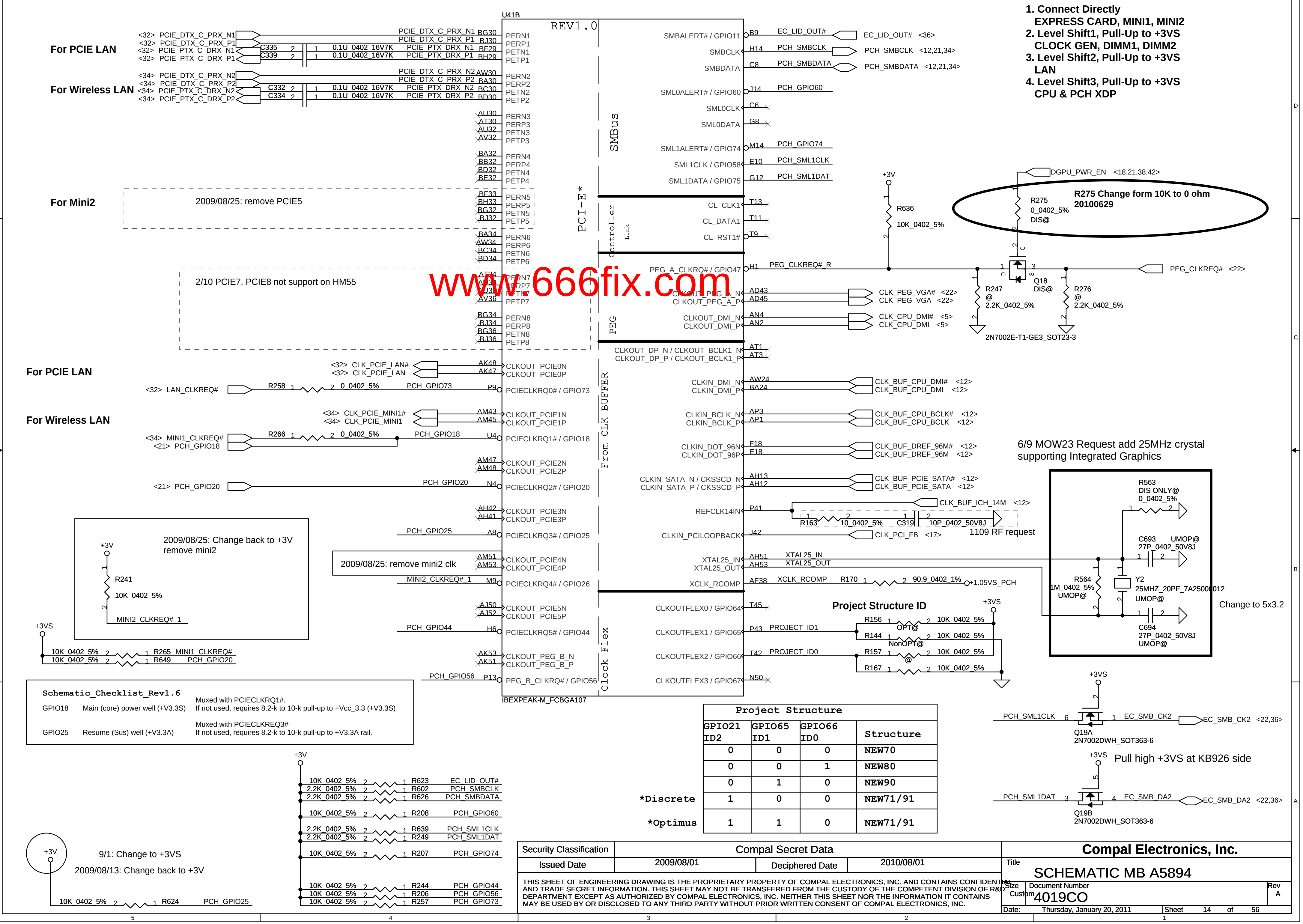

Schematic_Checklist_Rev1.6

GPIO18	Main (core) power well (+V3.3S)	Muxed with PCIECLKRQ1#. If not used, requires 8.2-k to 10-k pull-up to +Vcc_3.3 (+V3.3S)
GPIO25	Resume (Sus) well (+V3.3A)	Muxed with PCIECLKREQ3# If not used, requires 8.2-k to 10-k pull-up to +V3.3A rail.

Project Structure

	GPIO21 ID2	GPIO65 ID1	GPIO66 ID0	Structure
	0	0	0	NEW70
	0	0	1	NEW80
	0	1	0	NEW90
*Discrete	1	0	0	NEW71/91
*Optimus	1	1	0	NEW71/91

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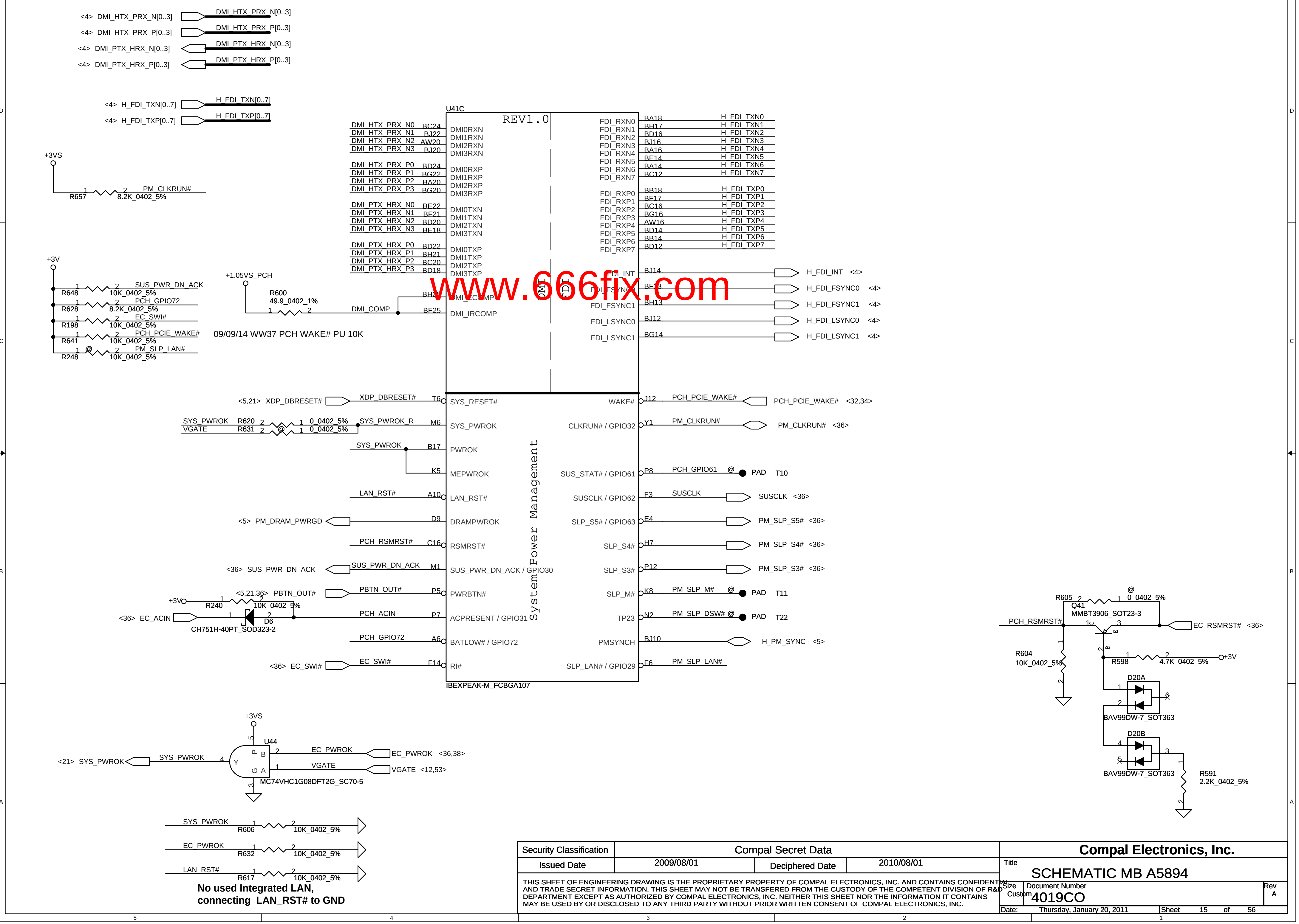

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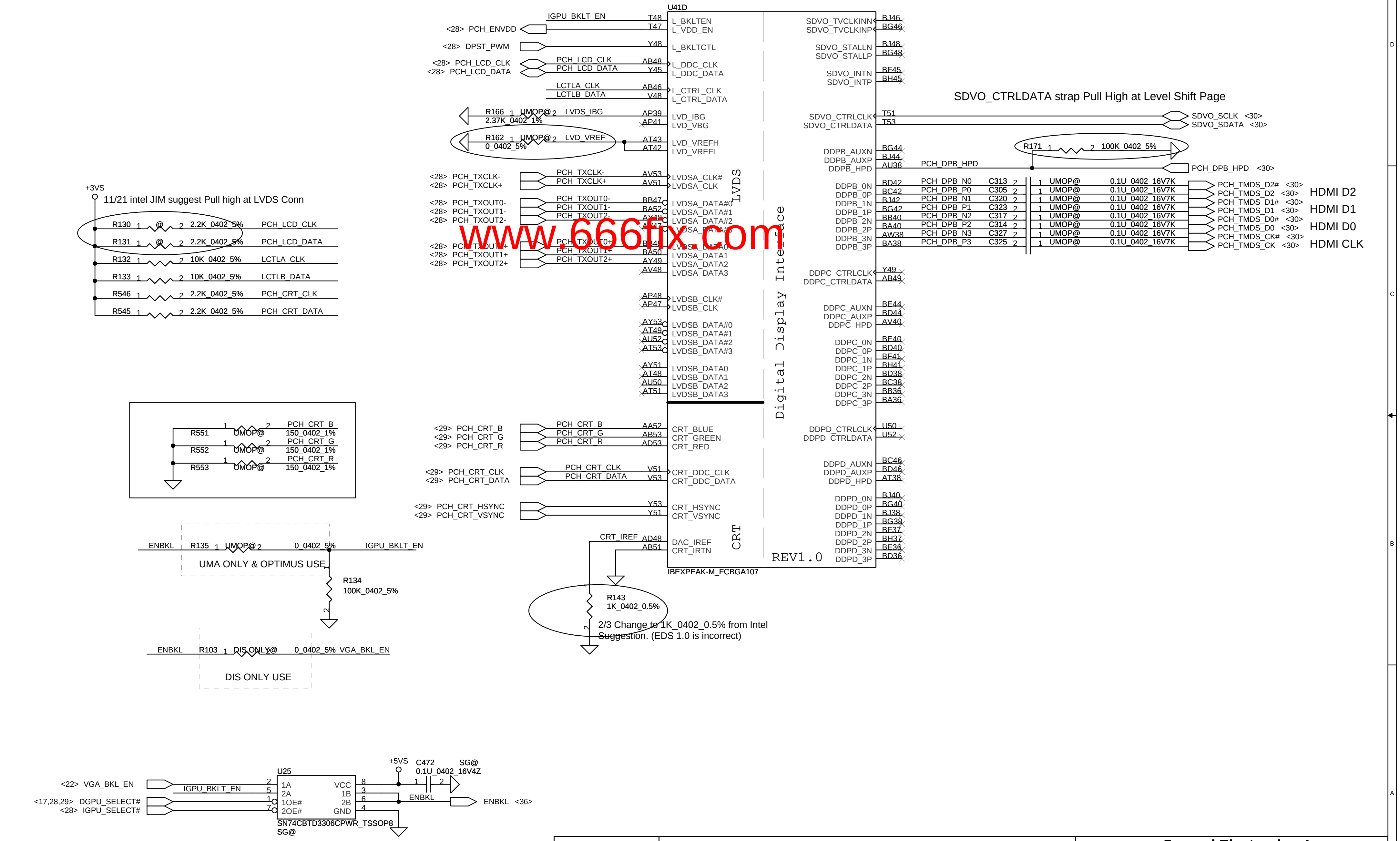

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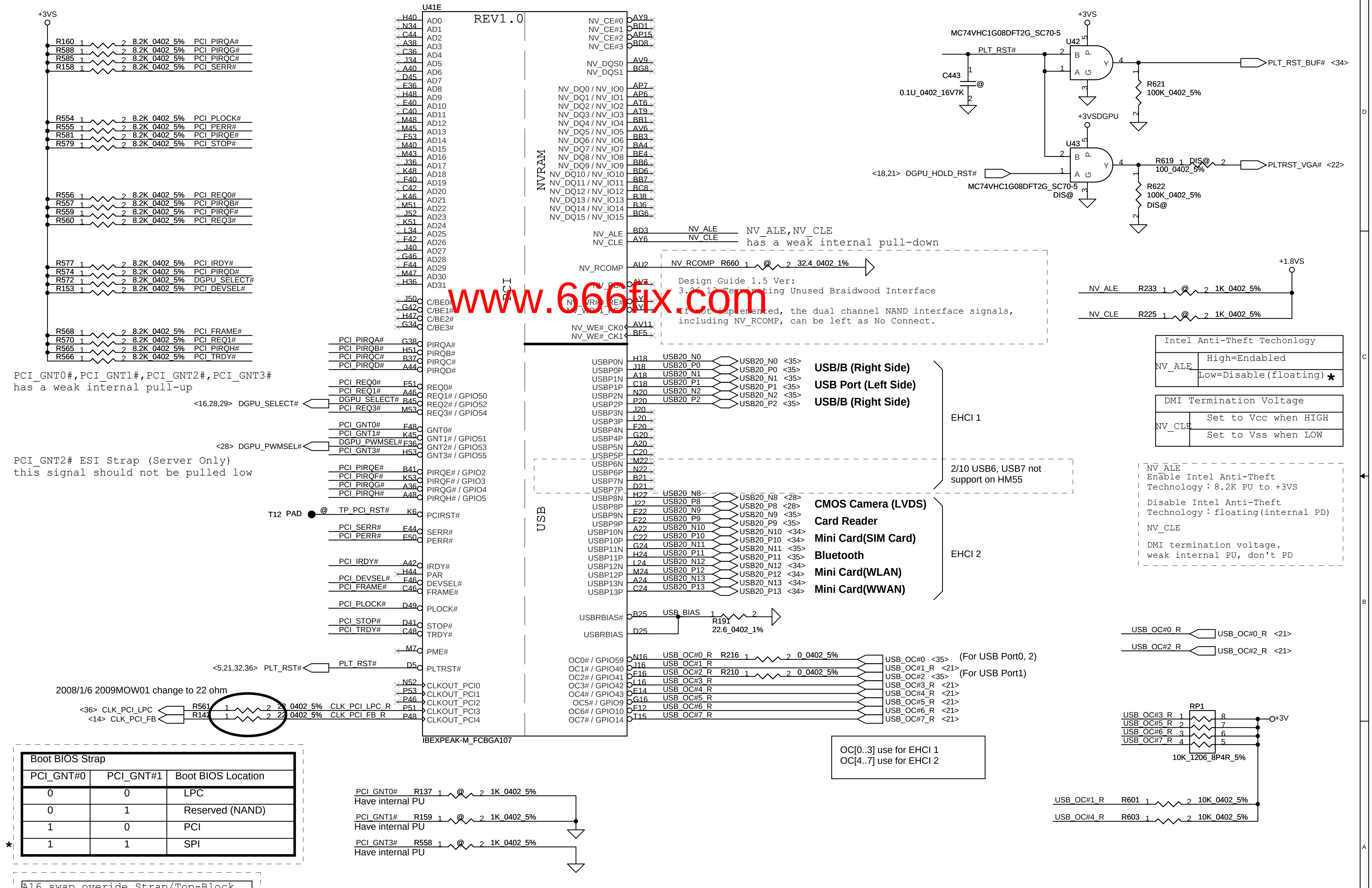

Intel Anti-Theft Techonlogy	
NV_ALE	High=Endabled
	Low=Disable(floating) ★

DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

Boot BIOS Strap

PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
★ 1	1	SPI

A16 swap overide Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low=A16 swap override/Top-Block Swap Override enabled High=Default ★

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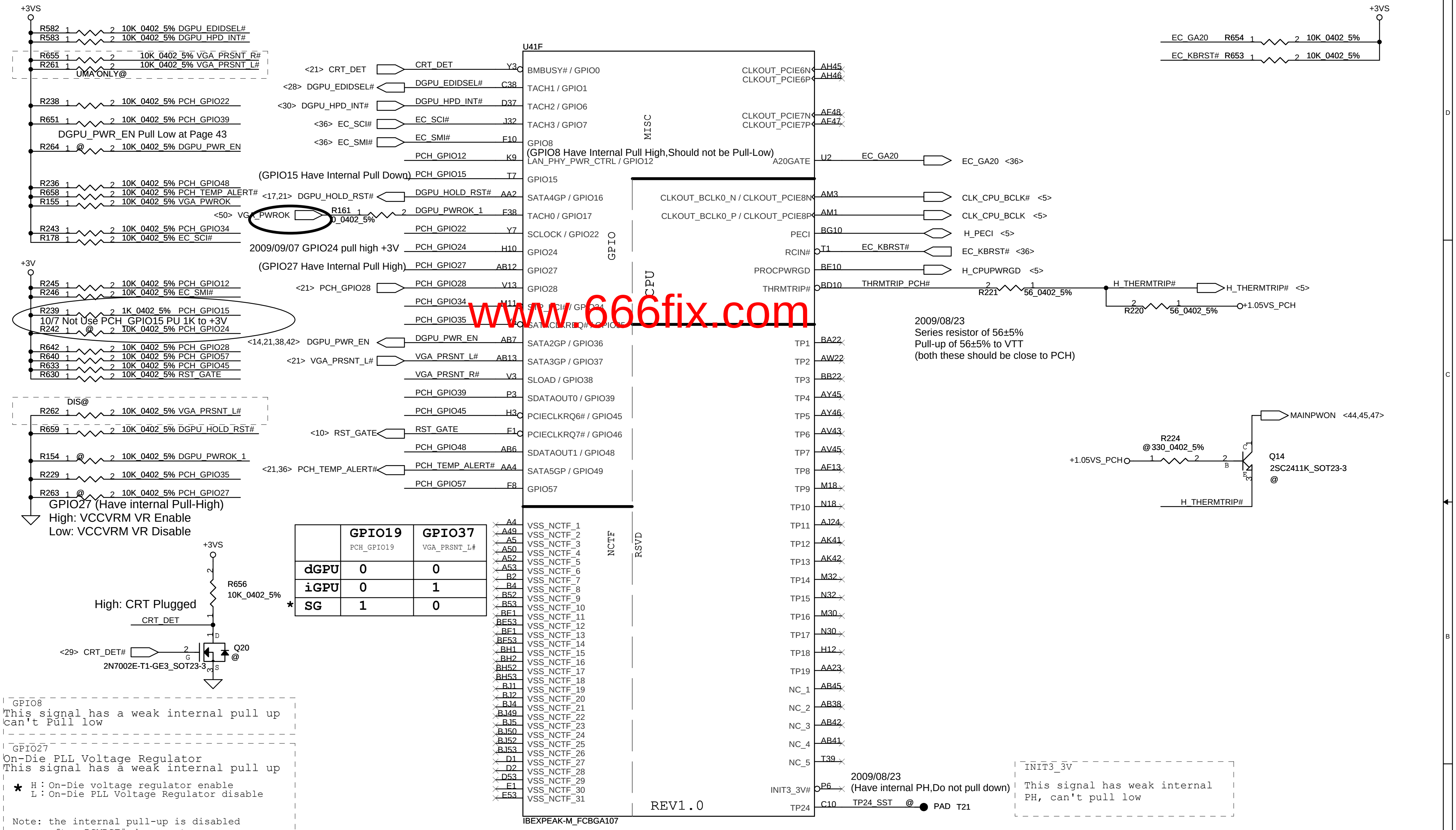

	GPIO19 PCH_GPIO19	GPIO37 VGA_PRSNT_L#
dGPU	0	0
iGPU	0	1
* SG	1	0

GPIO8
This signal has a weak internal pull up
can't Pull low

GPIO27
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

Note: the internal pull-up is disabled after RSMRST# de-asserts.
The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.

INIT3_3V
This signal has weak internal PH, can't pull low

GPIO15
★ L : Intel ME Crypto Transport Layer Security(TLS) chiper suite with no confidentiality

H : Intel ME Crypto Transport Layer Security(TLS) chiper suite with confidentiality

CRB has a 1-k pull-up on this signal to +3.3VA rail.

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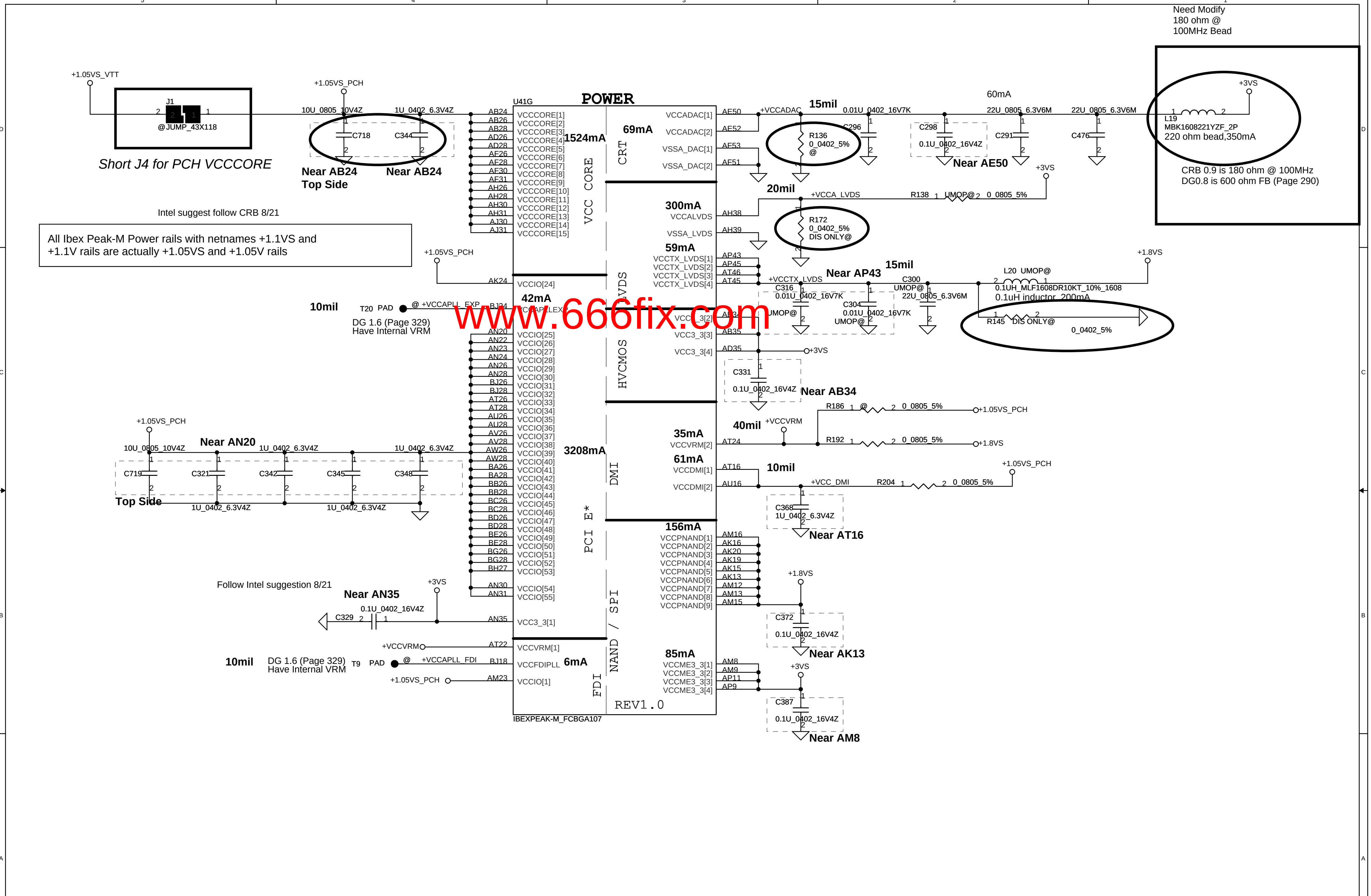

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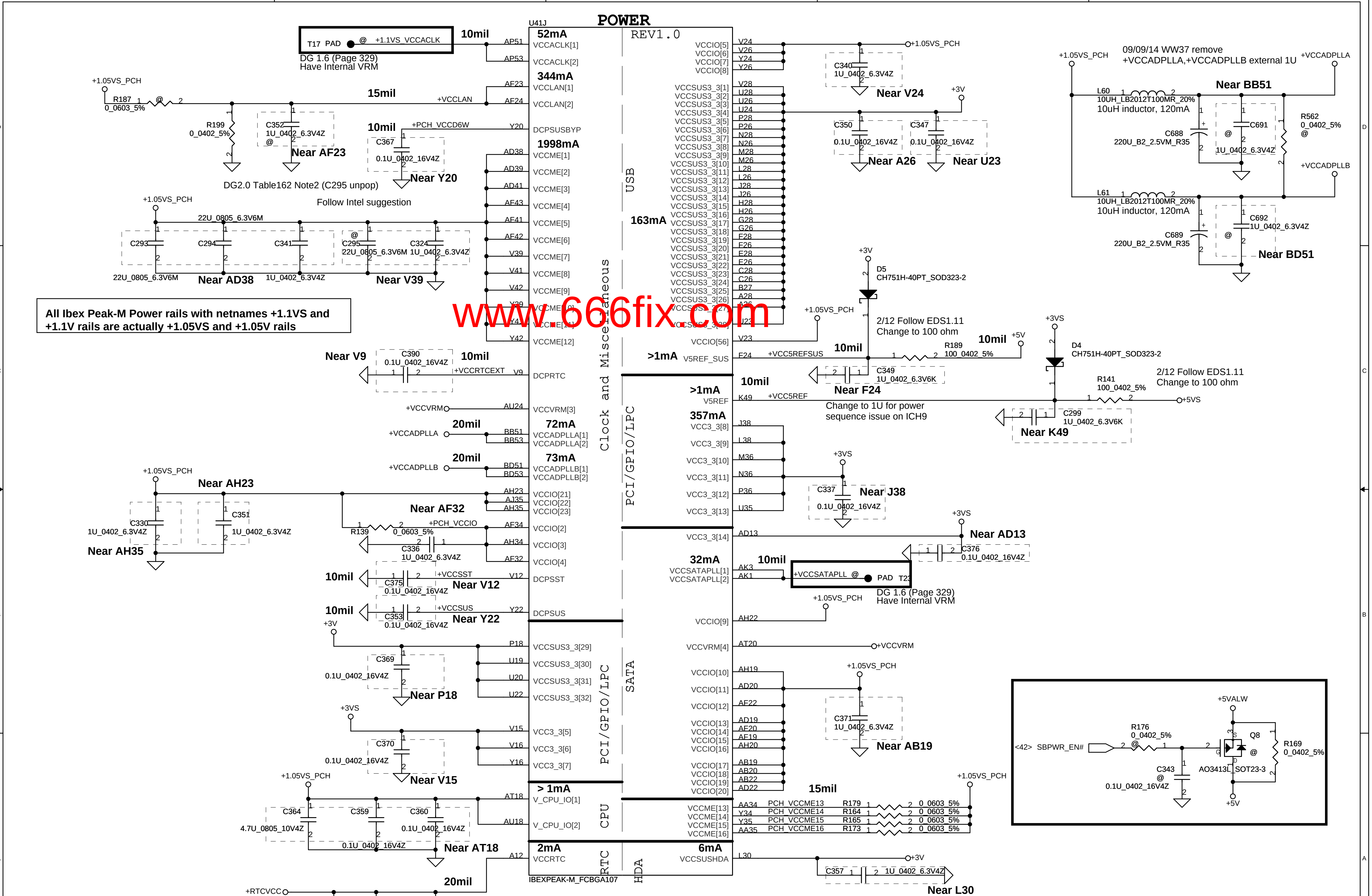

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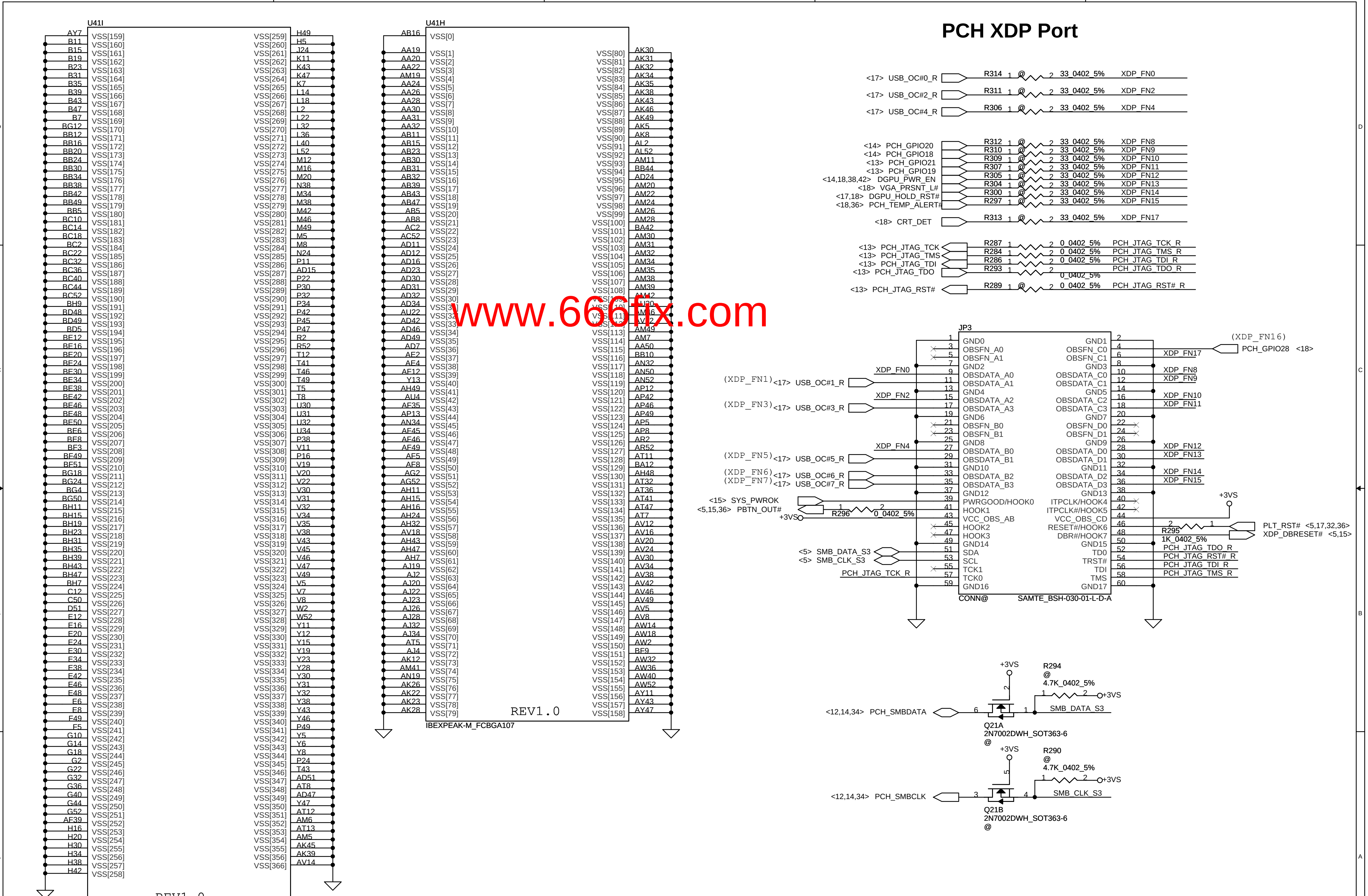

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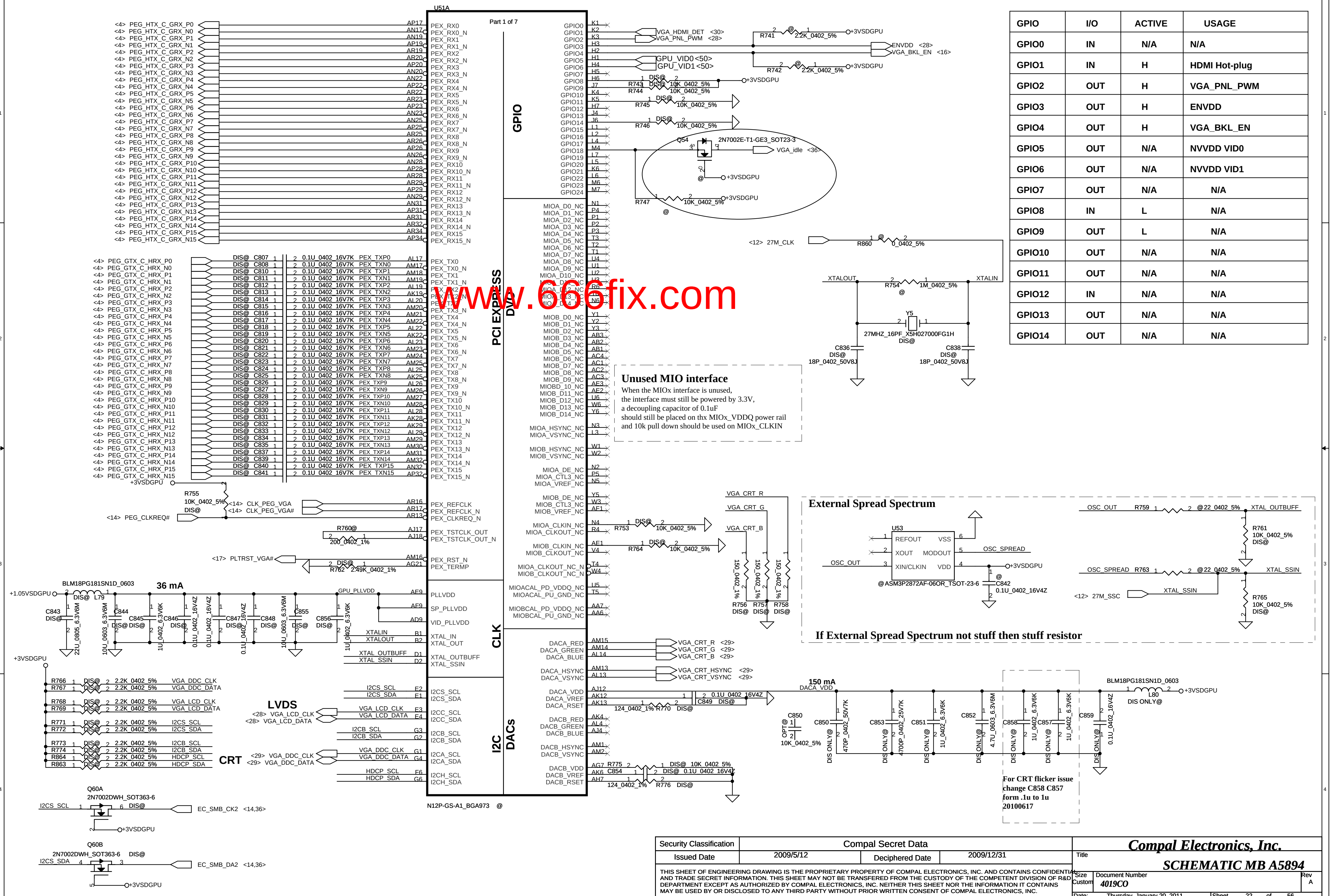

GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	N/A
GPIO1	IN	H	HDMI Hot-plug
GPIO2	OUT	H	VGA_PNL_PWM
GPIO3	OUT	H	ENVDD
GPIO4	OUT	H	VGA_BKL_EN
GPIO5	OUT	N/A	NVVDD VID0
GPIO6	OUT	N/A	NVVDD VID1
GPIO7	OUT	N/A	N/A
GPIO8	IN	L	N/A
GPIO9	OUT	L	N/A
GPIO10	OUT	N/A	N/A
GPIO11	OUT	N/A	N/A
GPIO12	IN	N/A	N/A
GPIO13	OUT	N/A	N/A
GPIO14	OUT	N/A	N/A

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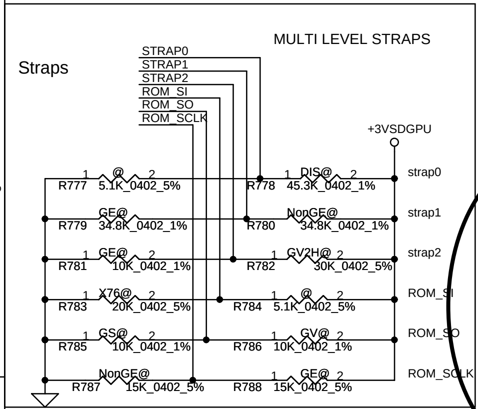

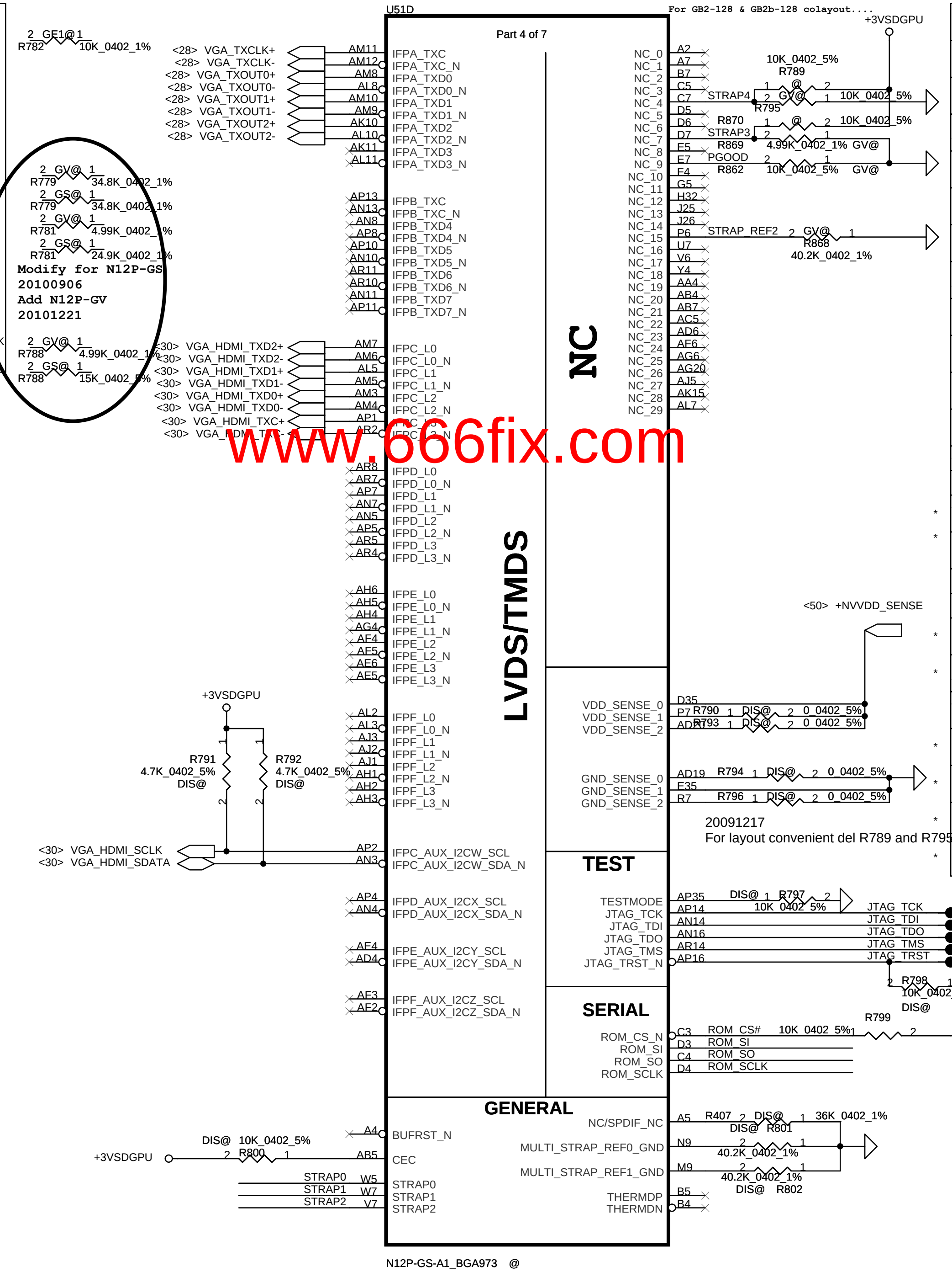

Mode E Command Mapping GB2-128 Package Femi	Mode C Command Mapping GB1-128 Package Data Bit	0..31	32..63
FBx_CMD3	FBx_CMD0	CKE_L	
FBx_CMD8	FBx_CMD1	A8	A8
FBx_CMD2	FBx_CMD2	CS0_L*	
FBx_CMD21	FBx_CMD3	A7	A6
FBx_CMD24	FBx_CMD4	A2	A1
FBx_CMD23	FBx_CMD5	A11	A9
FBx_CMD26	FBx_CMD6	A5	A4
FBx_CMD7	FBx_CMD7	A0	A12
FBx_CMD15	FBx_CMD8	CAS*	CAS*
FBx_CMD13	FBx_CMD9	BA1	A3
FBx_CMD4	FBx_CMD10	A9	A11
FBx_CMD18	FBx_CMD11		CS0_H
FBx_CMD29	FBx_CMD12	BA0	BA0
FBx_CMD27	FBx_CMD13	BA2	A15
FBx_CMD6	FBx_CMD14	A3	BA1
FBx_CMD17	FBx_CMD15		CS1_H
FBx_CMD19	FBx_CMD16		ODT_H
FBx_CMD22	FBx_CMD17	A4	A5
FBx_CMD12	FBx_CMD18	A13	A14
FBx_CMD28	FBx_CMD19	WE*	A10
FBx_CMD10	FBx_CMD20	A1	A2
FBx_CMD25	FBx_CMD21	A10	WE*
FBx_CMD9	FBx_CMD22	A12	A0
FBx_CMD1	FBx_CMD23	CS1_L*	
FBx_CMD11	FBx_CMD24	RAS*	RAS*
FBx_CMD0	FBx_CMD25	ODT_L	
FBx_CMD5	FBx_CMD26	A6	A7
FBx_CMD16	FBx_CMD27		CKE_H
FBx_CMD20	FBx_CMD28	RST	RST
FBx_CMD14	FBx_CMD29	A14	A13
FBx_CMD30	FBx_CMD30	A15	BA2
FBx_CMD31			

LOW HIGH

20091214 Modify For N11P-GV2H	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung :SA000035720	H 45K	H 35K	H 30K	L 20K	L 10K	L 15K
64MX16 Hynix:SA000032490	H 45K	H 35K	H 30K	L 15K	L 10K	L 15K

20100113 Modify For N11P-GE1	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung:SA000035720	H 45K	H 35K	H 10K	L 20K	L 10K	L 15K
64MX16 Hynix:SA000032490	H 45K	H 35K	H 10K	L 15K	L 10K	L 15K

20100601 Modify For N11P-GE	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung:SA000035720	H 45K	L 35K	L 10K	L 20K	L 10K	H 15K
64MX16 Hynix:SA000032490	H 45K	L 35K	L 10K	L 15K	L 10K	H 15K
128MX16 Samsung:SA00003MQ40	H 45K	L 35K	L 10K	L 45K	L 10K	H 15K
128MX16 Hynix:SA00003VS10	H 45K	L 35K	L 10K	L 35K	L 10K	H 15K

	20100909 Modify For N12P-GS VRAM: DDR3 900 down to 800	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
	64MX16 (800) Samsung:SA000035720	H 45K	H 35K	L 25K	NC	NC	L 10K	L 10K	H 15K
	64MX16 (800) Hynix:SA000032490	H 45K	H 35K	L 25K	NC	NC	L 5K	L 10K	H 15K
*	64MX16 (900) Samsung:K4W1G1646G-BC11 SA00004GS10	H 45K	L 35K	L 25K	NC	NC	L 20K	L 10K	H 15K
*	64MX16 (900) Hynix:H5TQ1G63DFR-11C SA000041S40	H 45K	L 35K	L 25K	NC	NC	L 15K	L 10K	H 15K
	128MX16 (800) Samsung:SA00003MQ40	H 45K	H 35K	L 25K	NC	NC	L 45K	L 10K	H 15K
	128MX16 (800) Hynix:SA00003VS10	H 45K	H 35K	L 25K	NC	NC	L 35K	L 10K	H 15K
*	128MX16 (900) Samsung:K4W2G1646C-HC11 SA000047Q20	H 45K	L 35K	L 25K	NC	NC	L 45K	L 10K	H 15K
*	128MX16 (900) Hynix:H5TQ2G63BFR-11C SA00003YO20	H 45K	L 35K	L 25K	NC	NC	L 35K	L 10K	H 15K

	20101220 Modify For N12P-GV-OP VRAM: DDR3 900 down to 800	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
*	64MX16 (900) Samsung:K4W1G1646G-BC11 SA00004GS10	H 45K	L 35K	L 5K	L 5K	L 10K	L 20K	H 10K	H 5K
*	64MX16 (900) Hynix:H5TQ1G63DFR-11C SA000041S40	H 45K	L 35K	L 5K	L 5K	L 10K	L 15K	H 10K	H 5K
*	128MX16 (900) Samsung:K4W2G1646C-HC11 SA000047Q20	H 45K	L 35K	L 5K	L 5K	L 10K	L 45K	H 10K	H 5K
*	128MX16 (900) Hynix:H5TQ2G63BFR-11C SA00003YO20	H 45K	L 35K	L 5K	L 5K	L 10K	L 35K	H 10K	H 5K

ROM_SI，爲Vram配打電阻

Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

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Title: SCHEMATIC MB A5894

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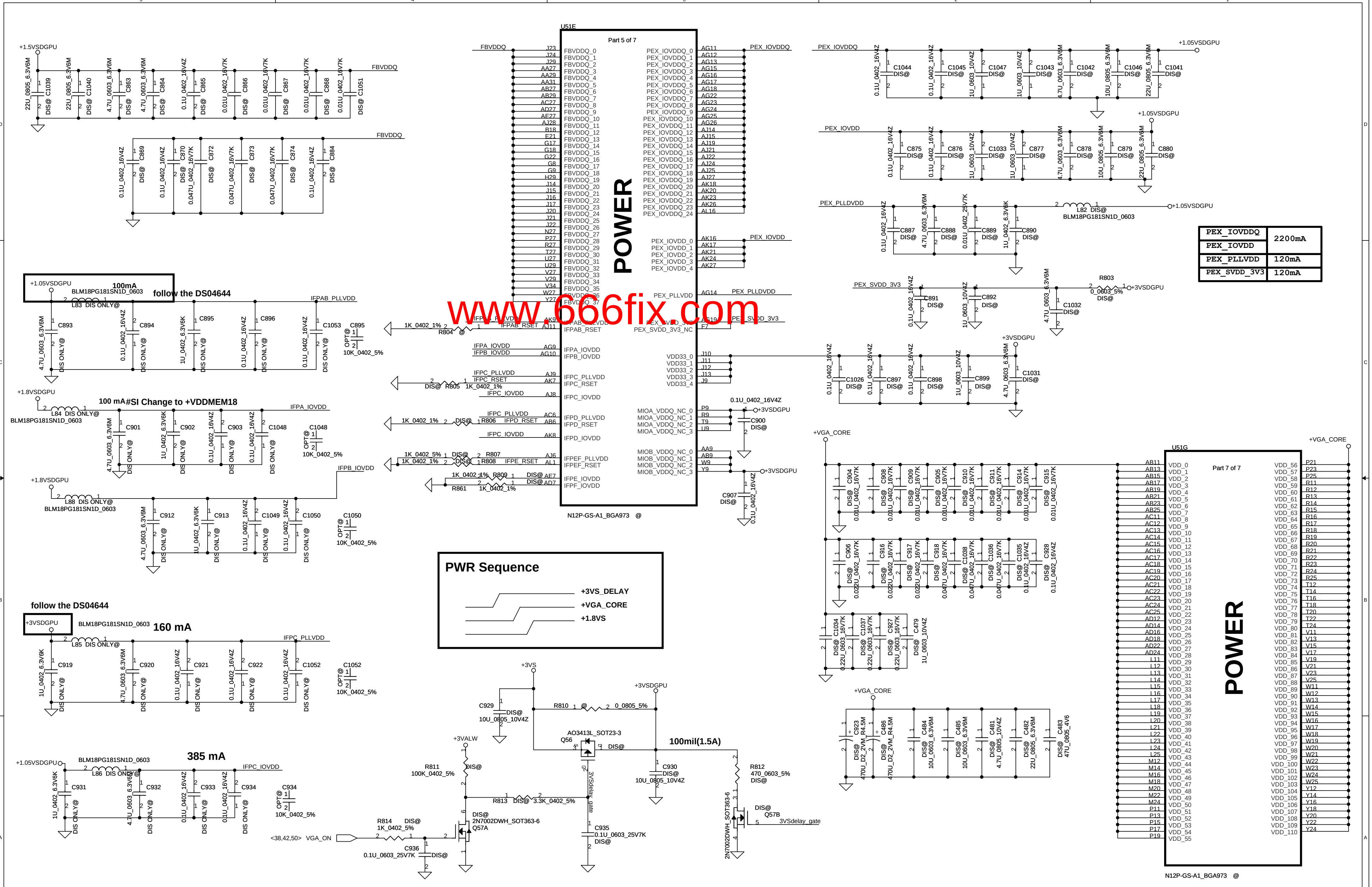

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Issued Date	2009/5/12	Deciphered Date	2009/12/31

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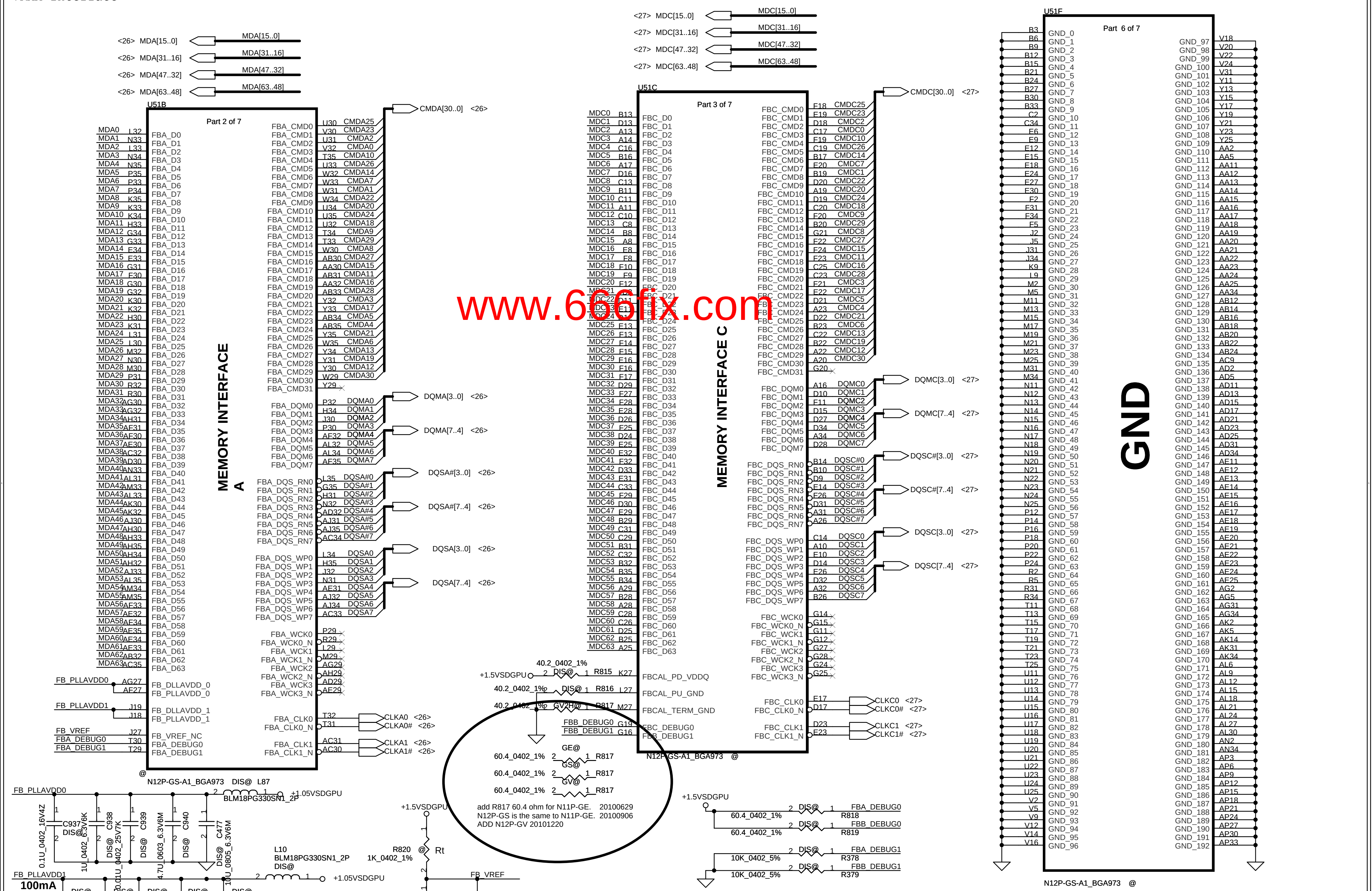
VRAM Interface



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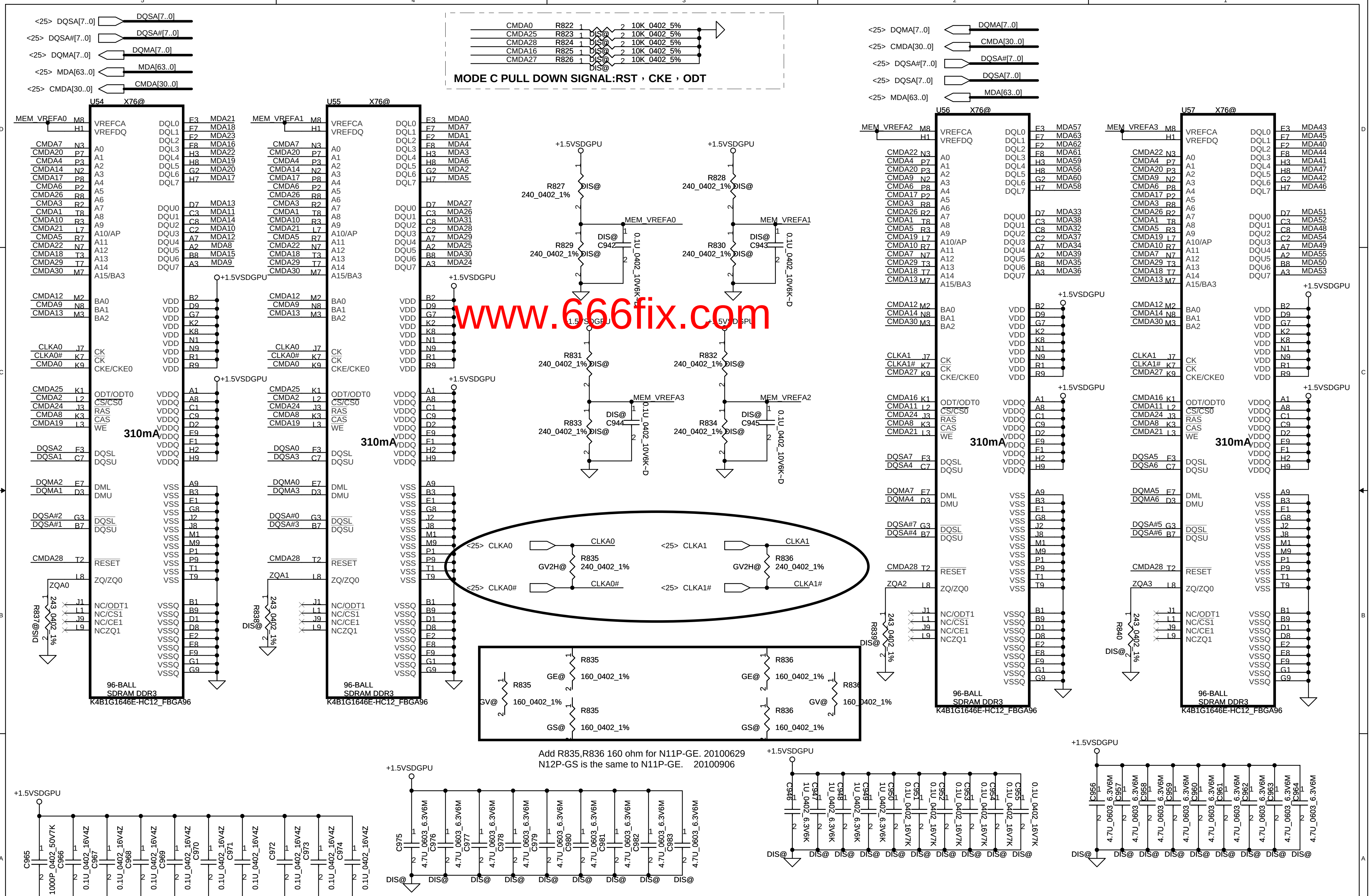
				Date: Thursday, January 20, 2011; Sheet 25 of 56



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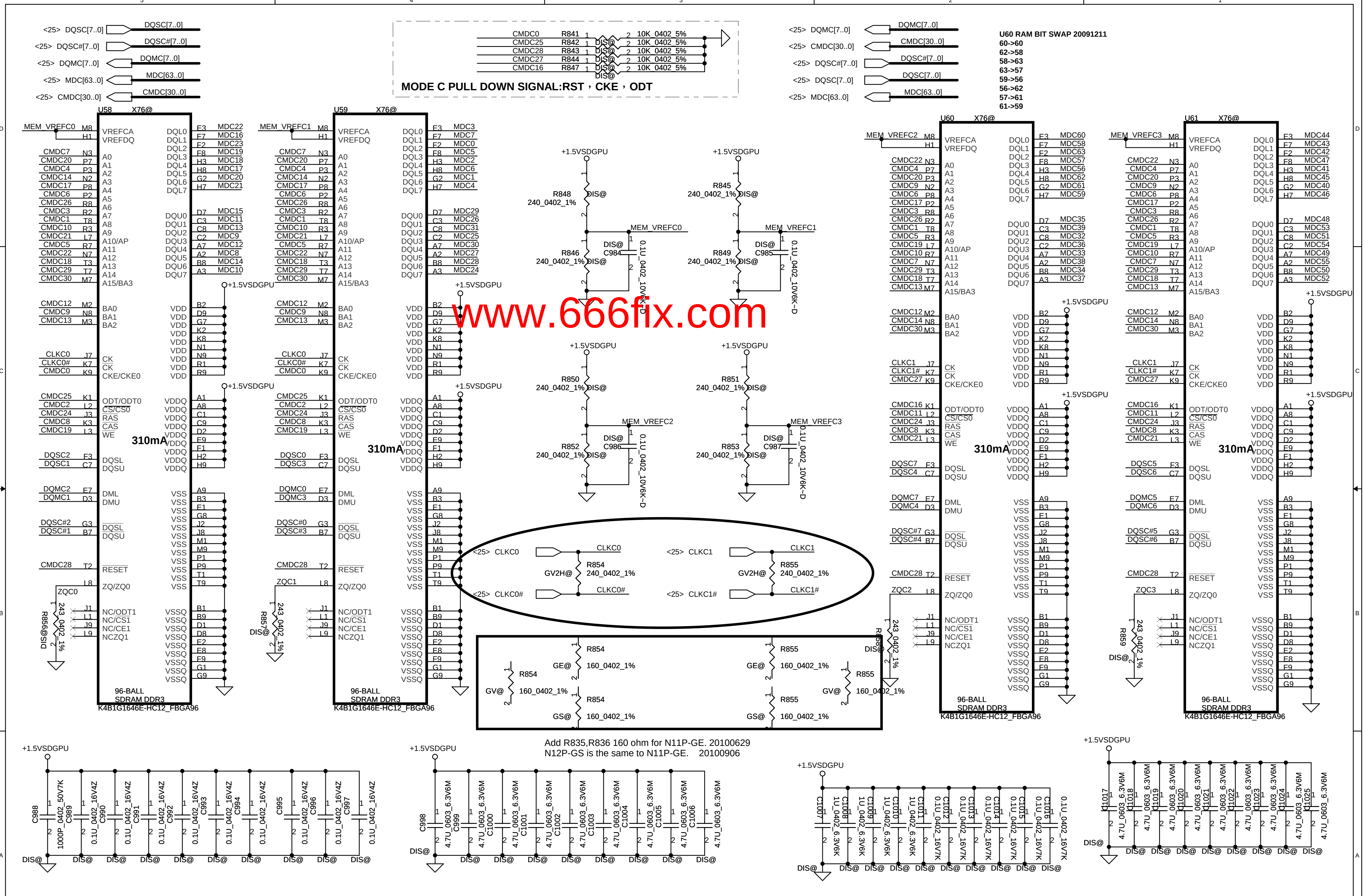
				Size: Custom; Document Number: 4019CO; Rev
				Date: Thursday, January 20, 2011; Sheet 26 of 56



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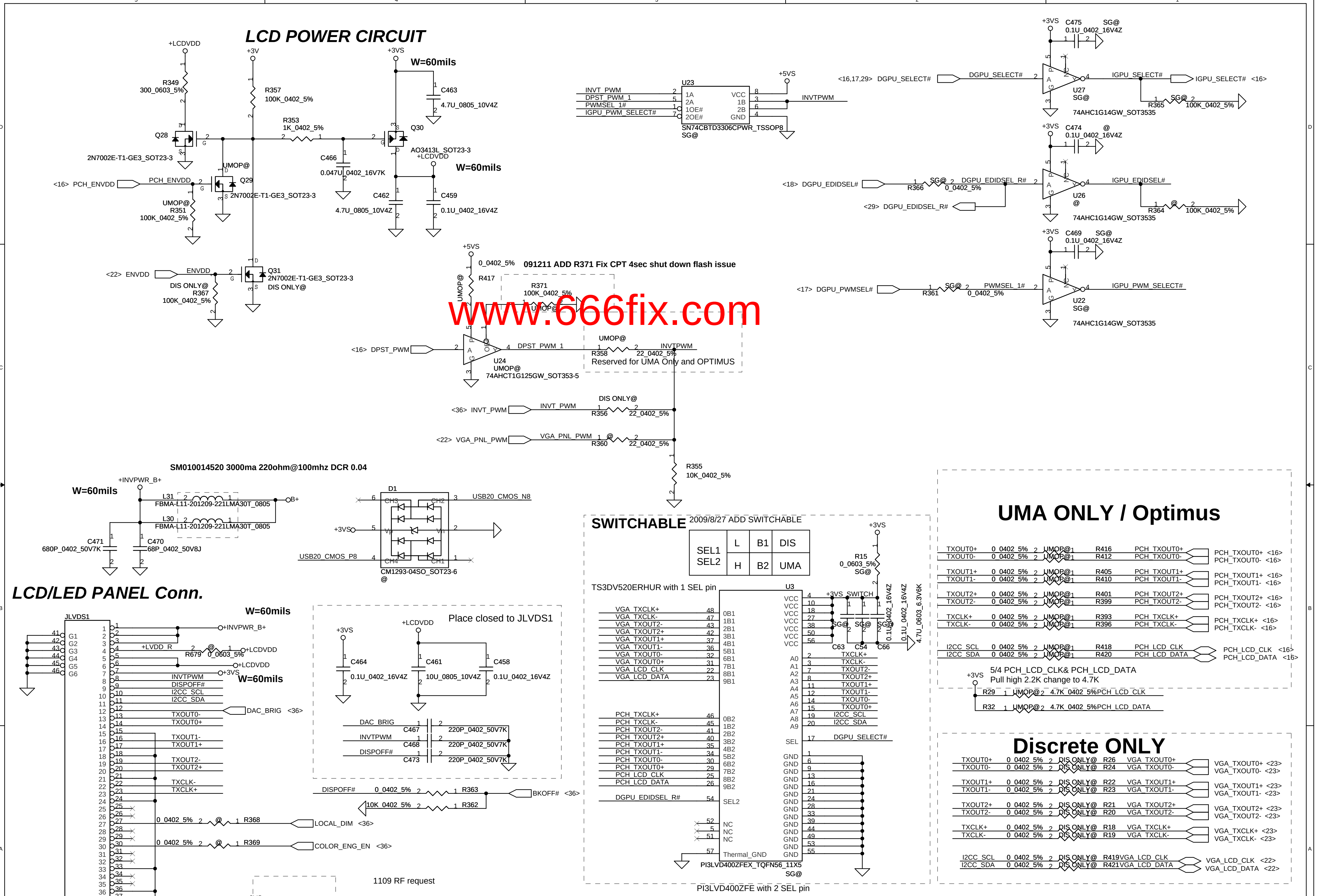
Size: Custom | Document Number: 4019CO | Rev: A

Date: Thursday, January 20, 2011 |



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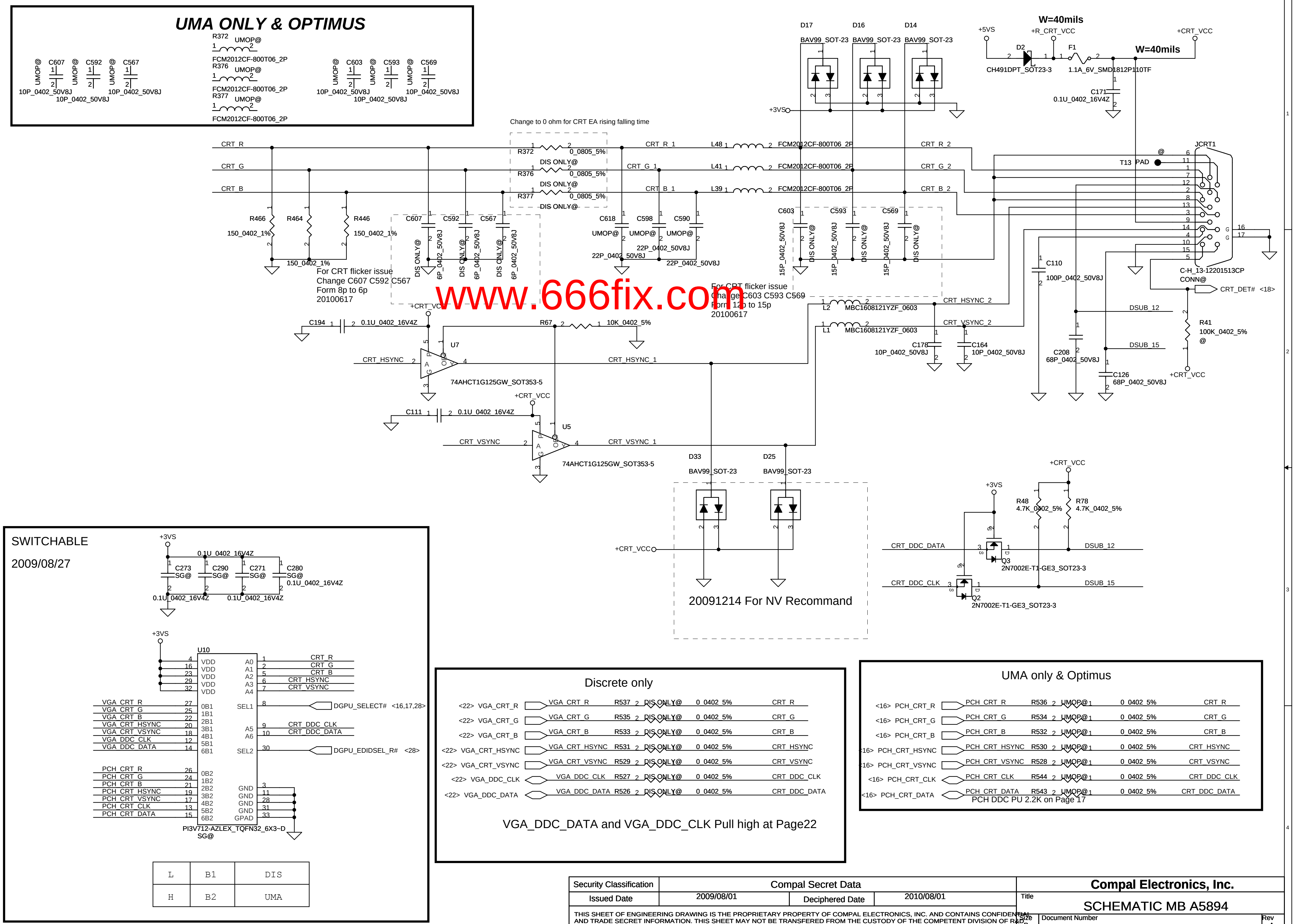
				Size: Custom; Document Number: 4019CO; Rev: A
				Date: Thursday, January 20, 2011; Sheet 28 of 56



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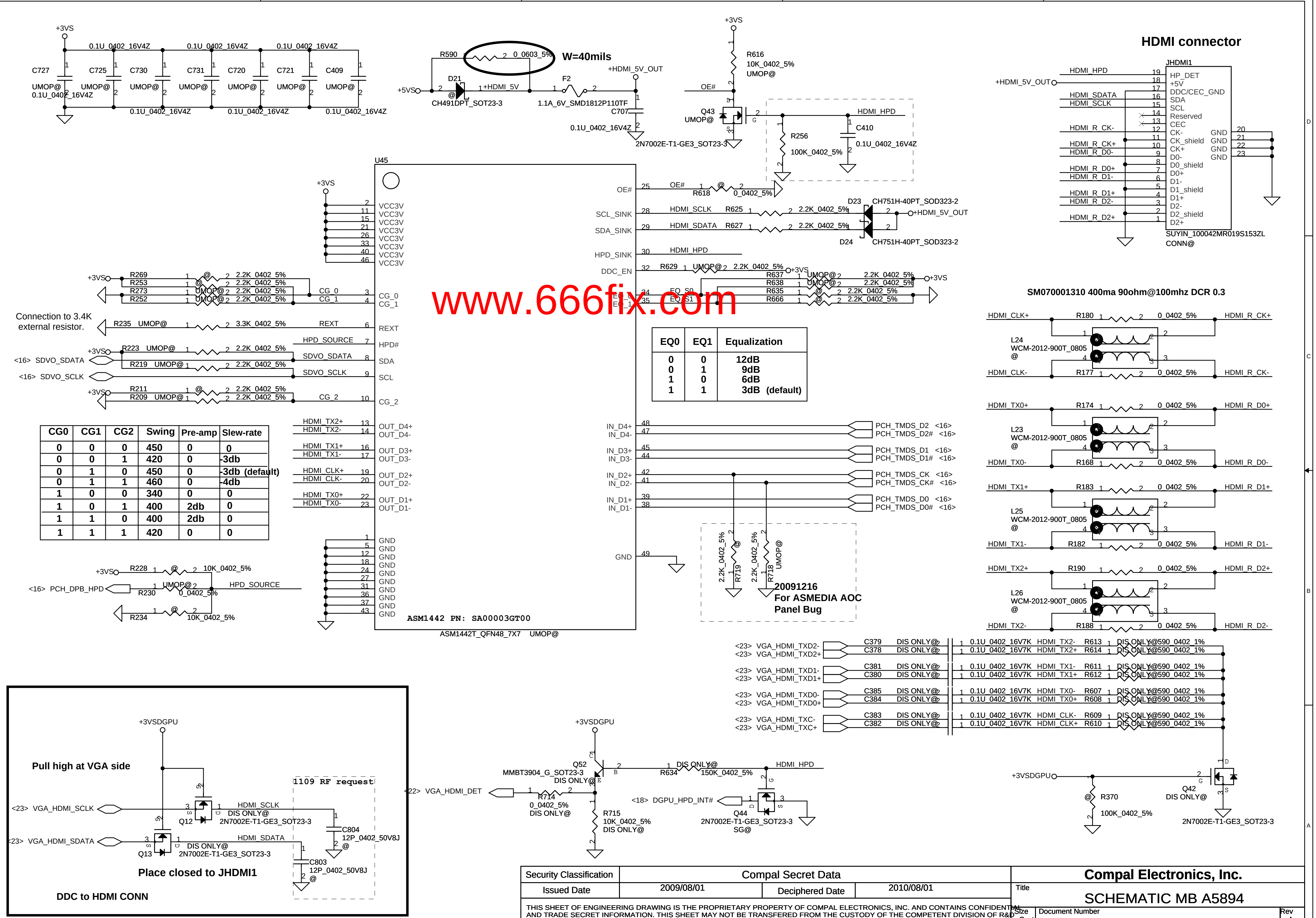
				Size: B; Document Number: 4019CO; Rev: A
				Date: Thursday, January 20, 2011; Sheet 29 of 56



EQ0	EQ1	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB (default)

CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0

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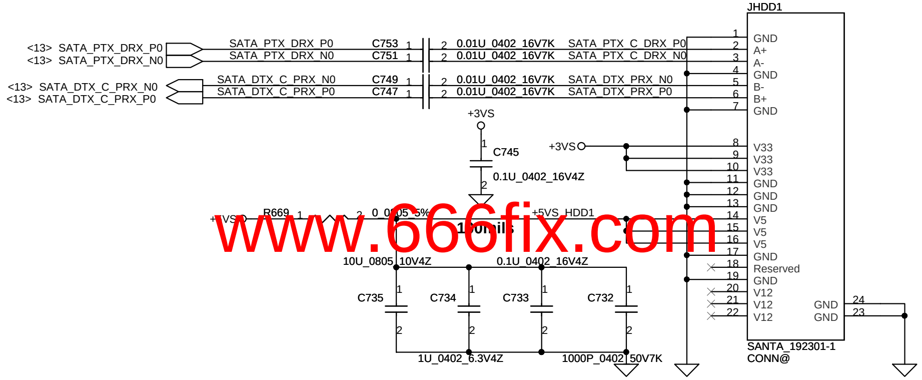
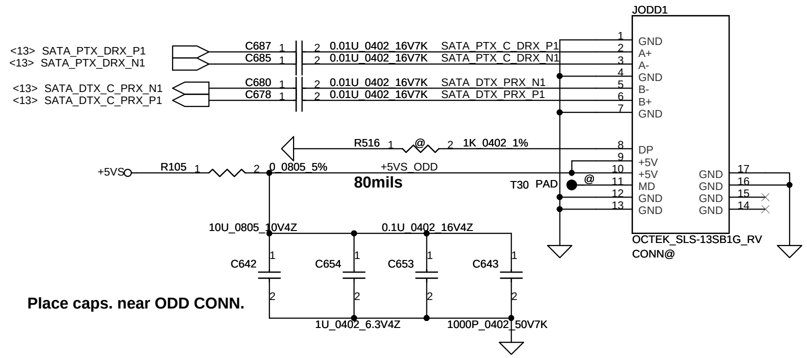
SATA HDD1 Conn.

CL 4.0 mm



SATA ODD Conn.



Place caps. near ODD CONN.

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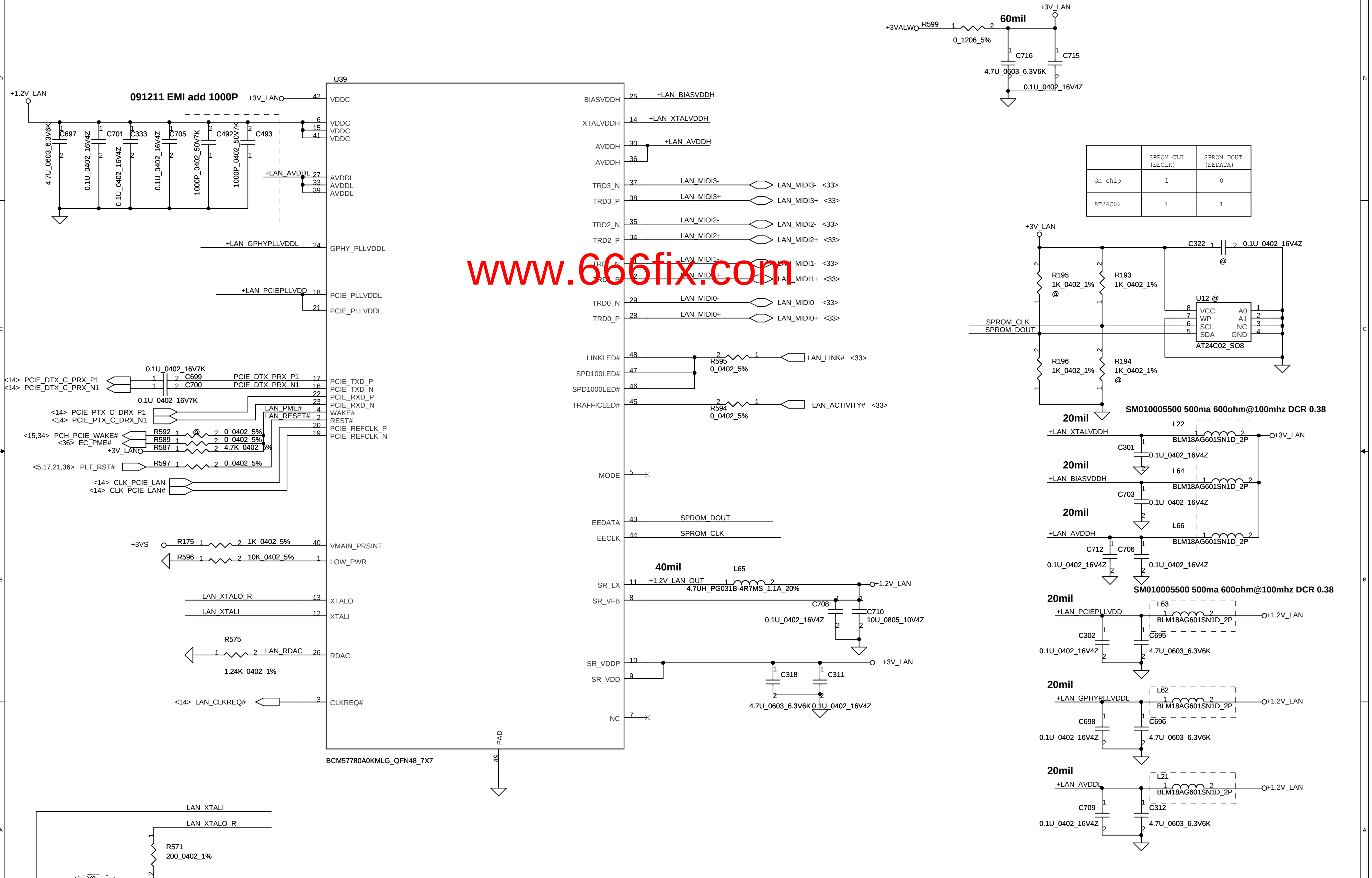
				Date: Thursday, January 20, 2011; Sheet 31 of 56



	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

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Issued Date	2008/08/10	Deciphered Date	2010/08/01

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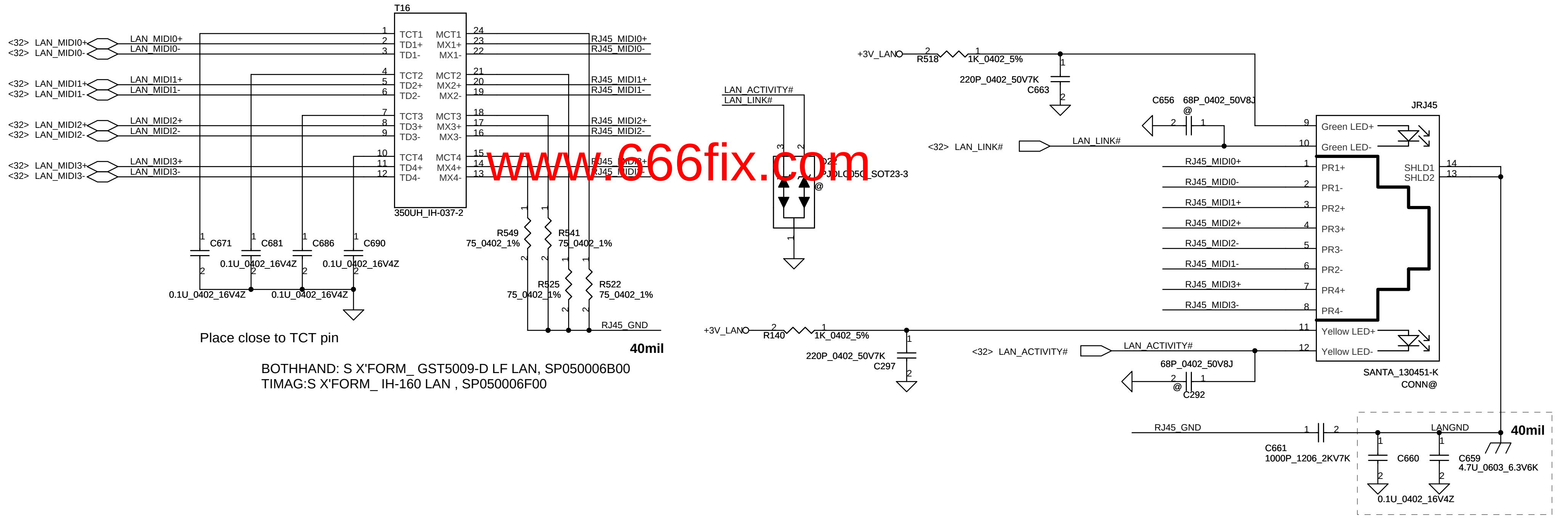
Date: Thursday, January 20, 2011 |

LAN Connector



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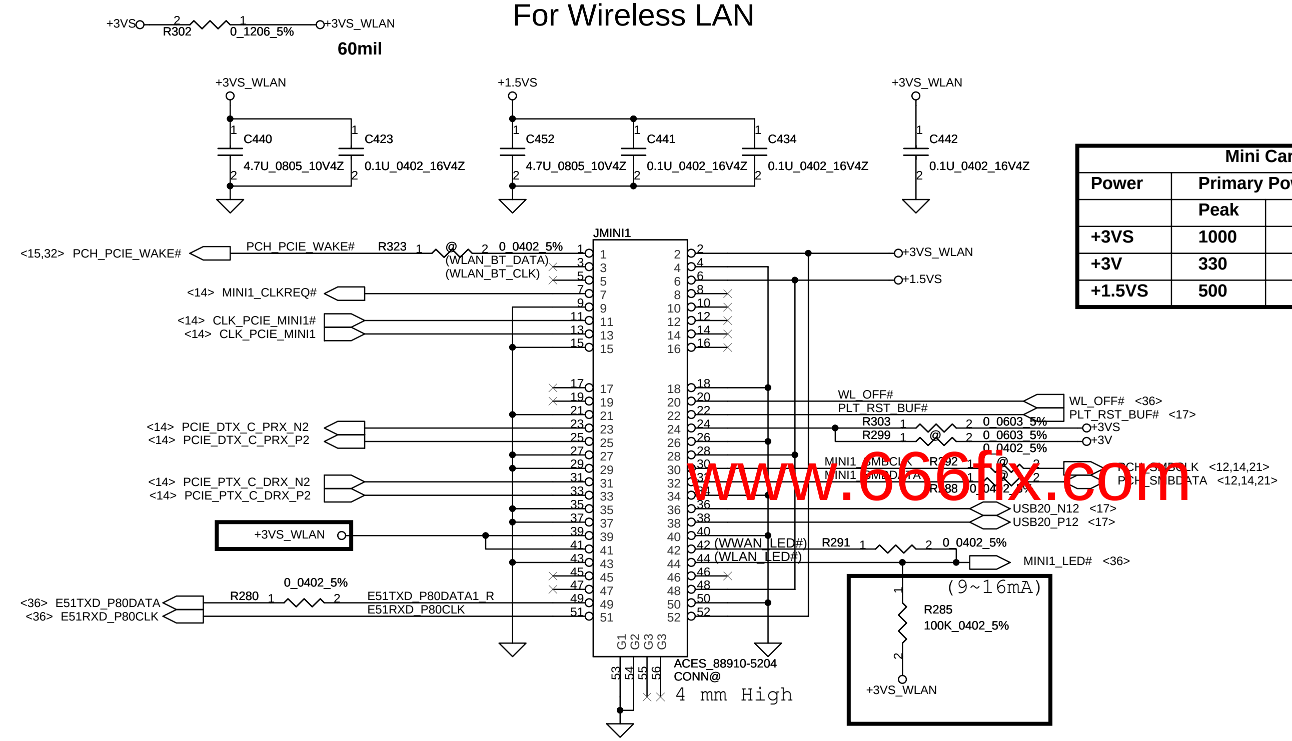
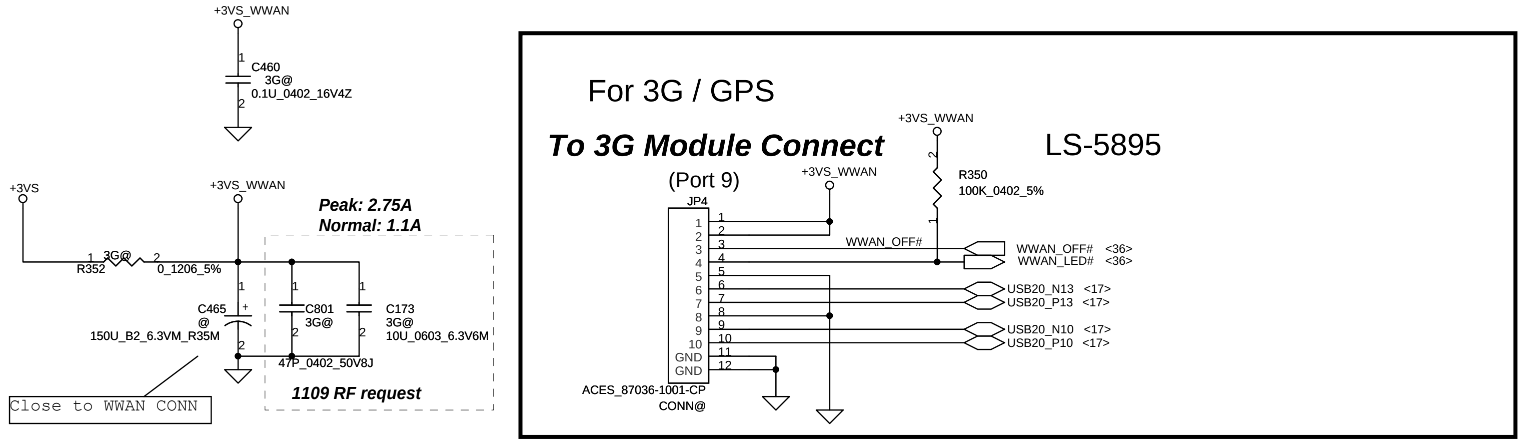
For Wireless LAN



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



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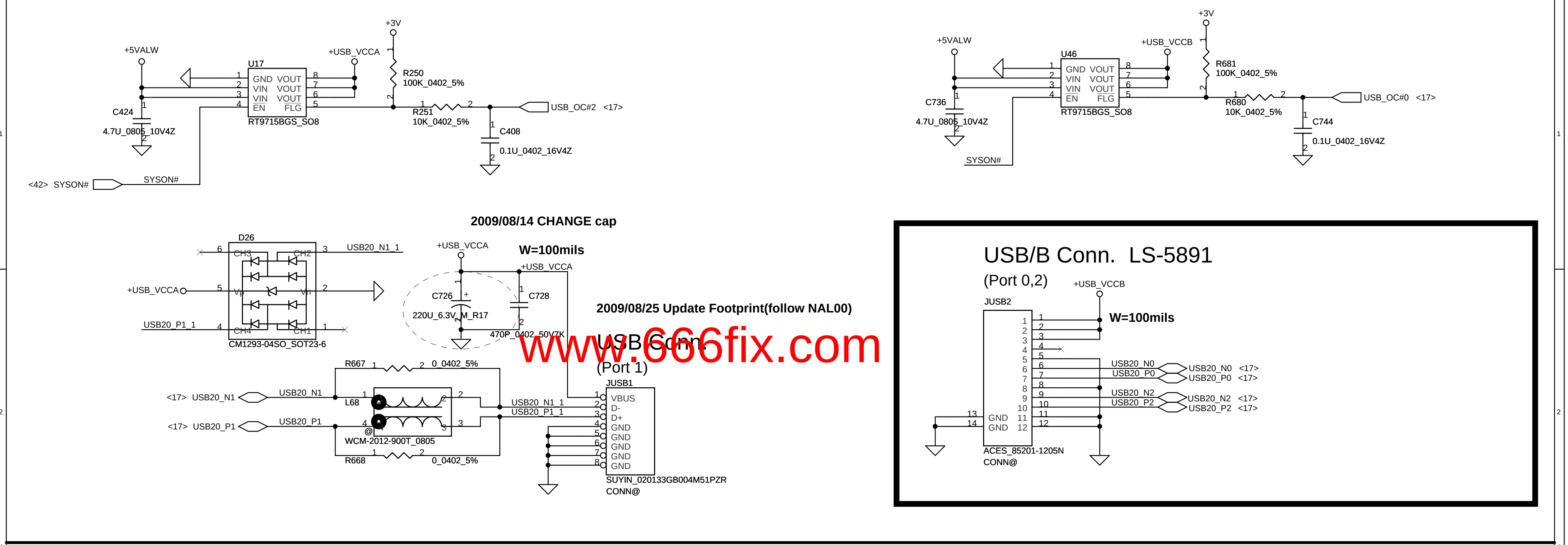
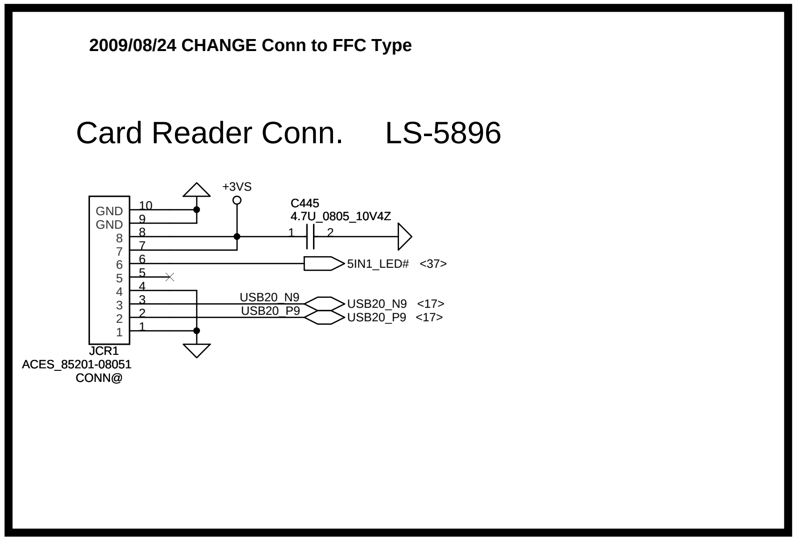
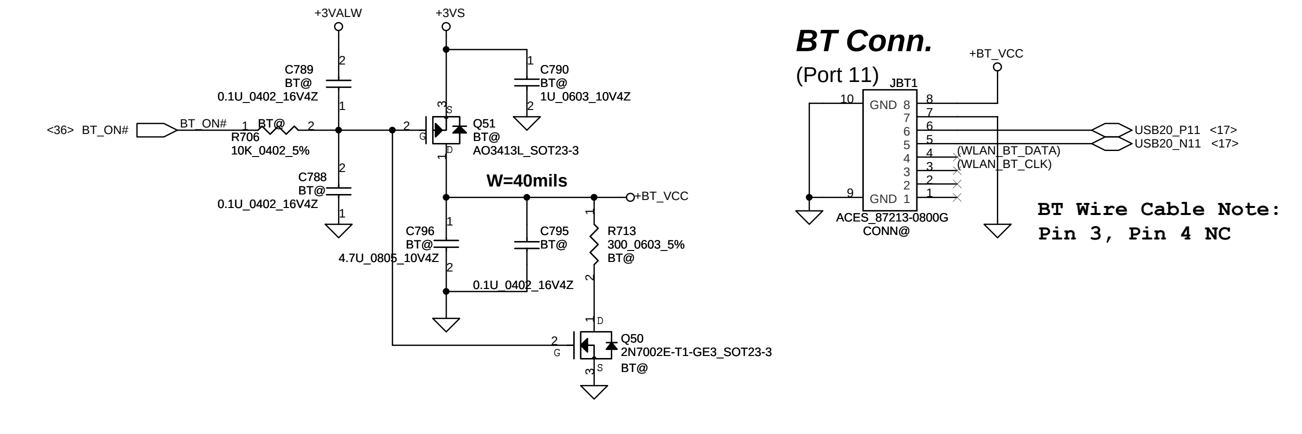
				Date: Thursday, January 20, 2011; Sheet 34 of 56







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Title: SCHEMATIC MB A5894		
Size: Custom	Document Number: 4019CO	Rev: A
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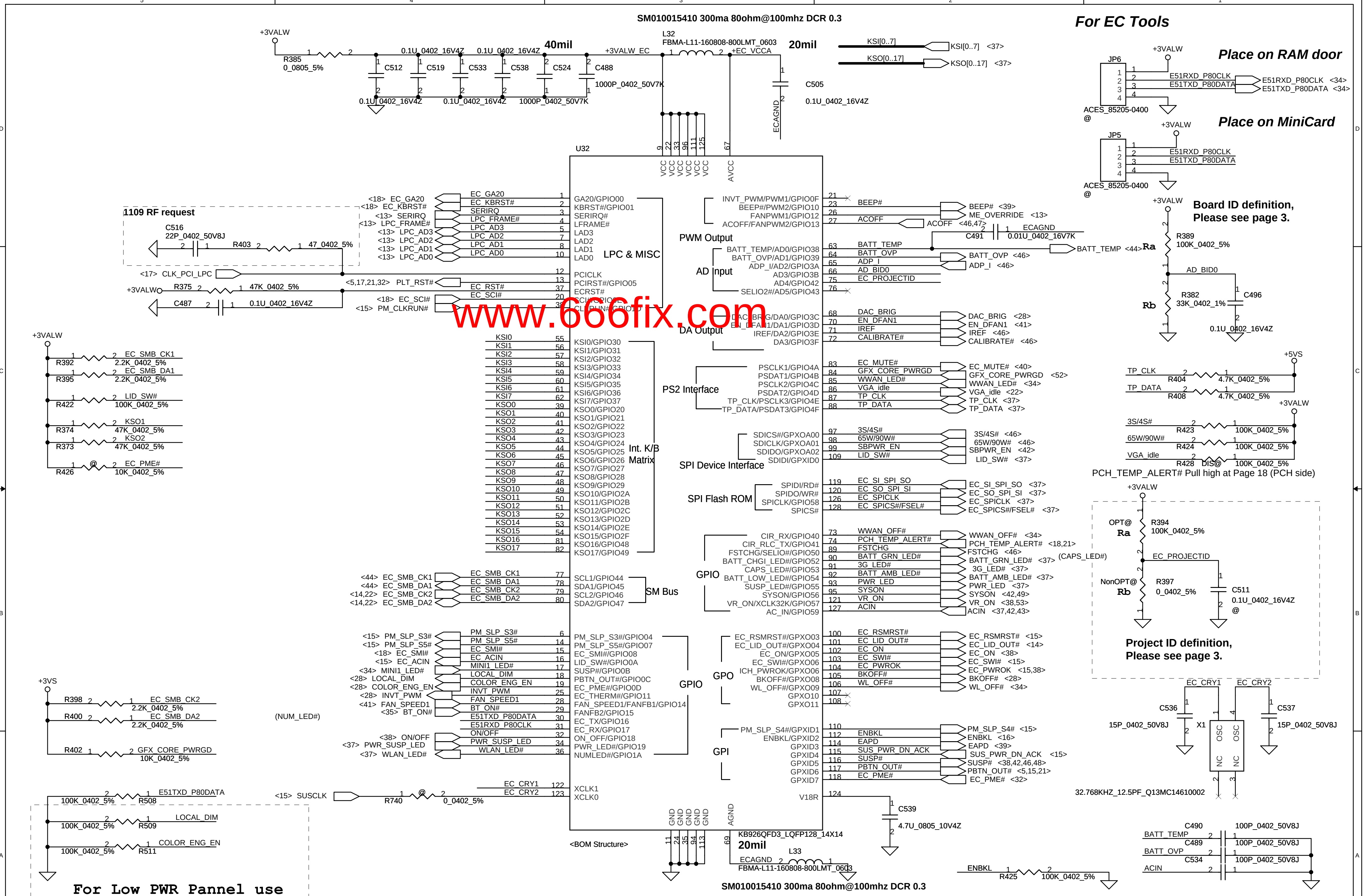

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Compal Electronics, Inc.

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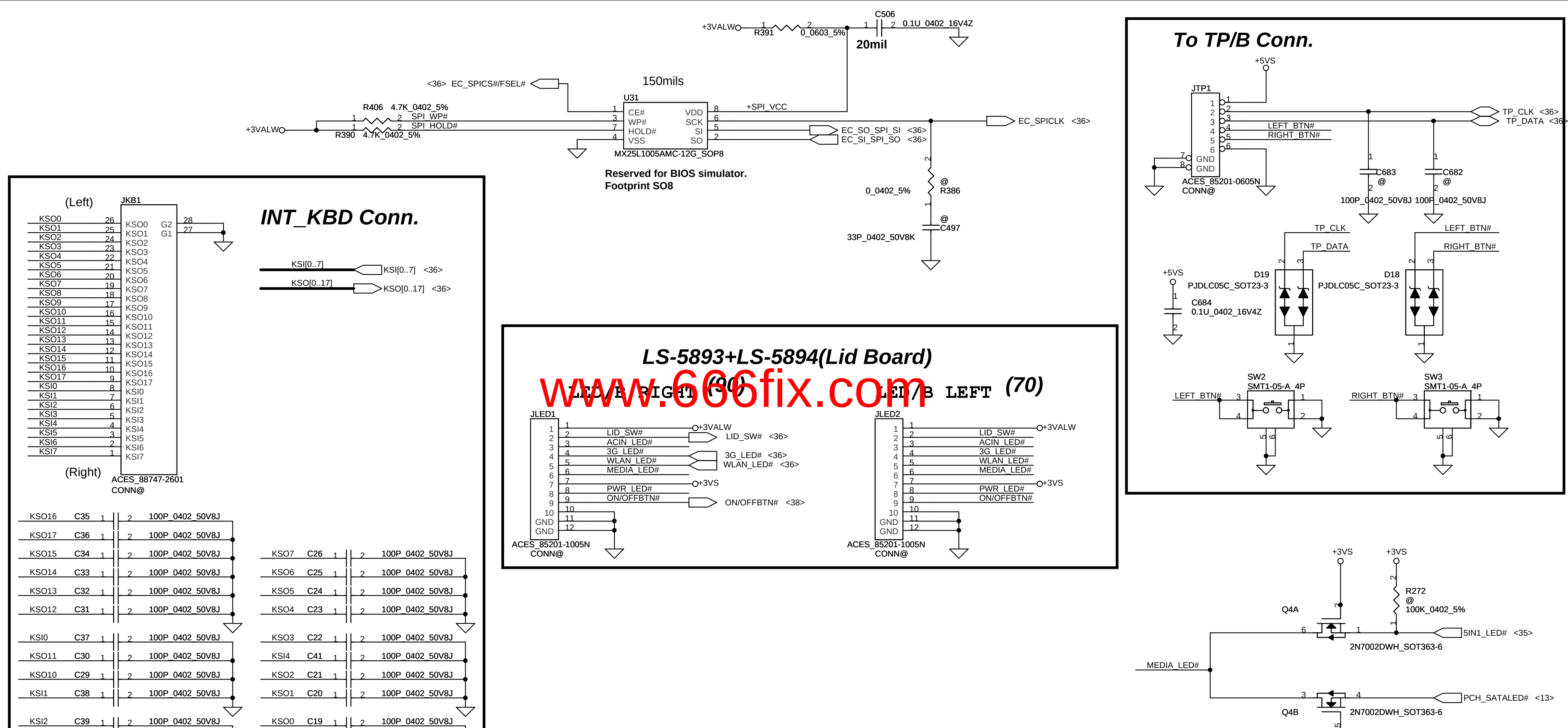
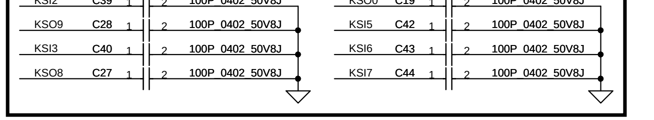
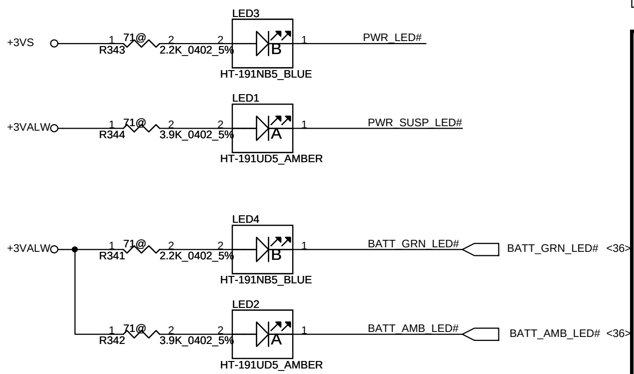
Size: B | Document Number: 4019CO | Rev: A

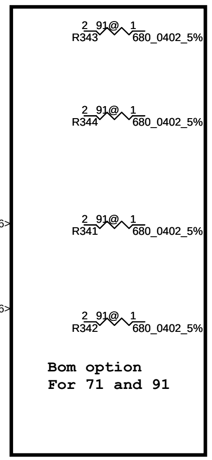
Date: Thursday, January 20, 2011 | Sheet 36 of 56

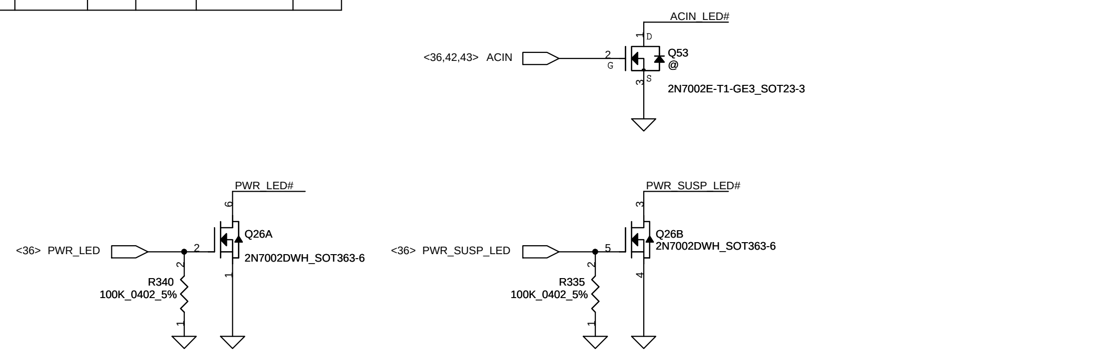




LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
NEW70/80/90	Blue	Amber	Blue	Amber	Blue	Amber		







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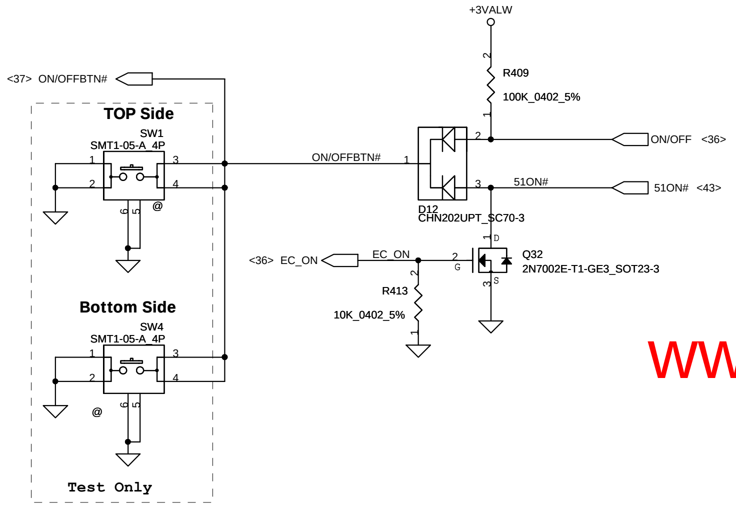
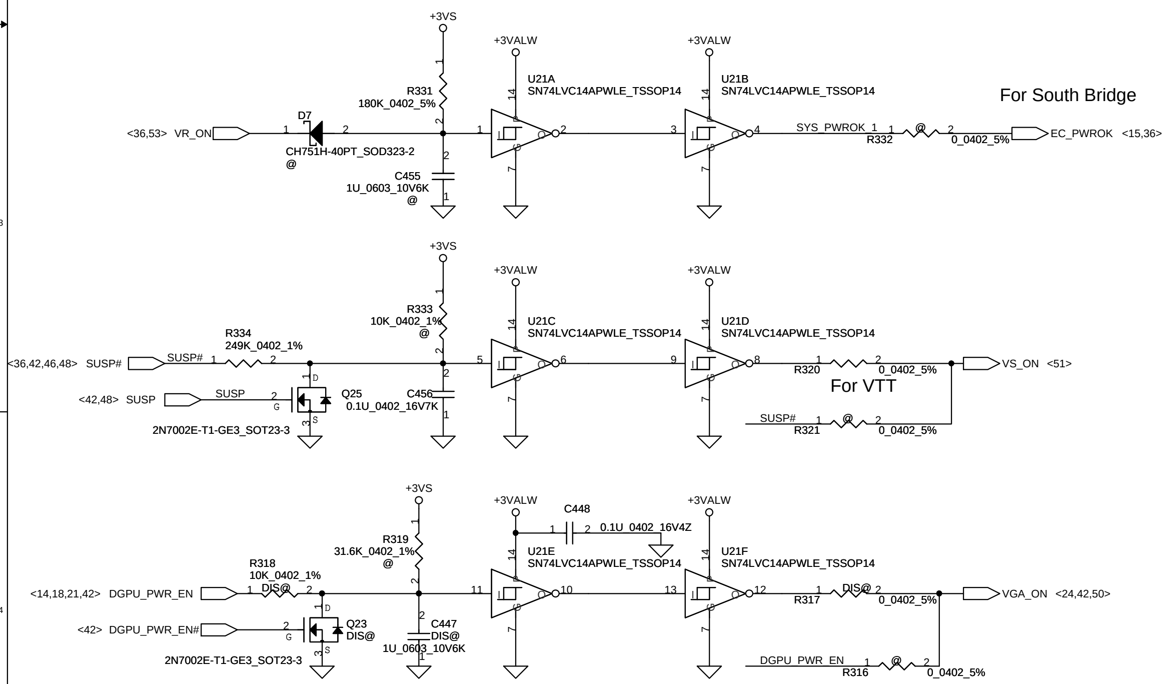
Power Button

ON/OFF switch



Power ON Circuit



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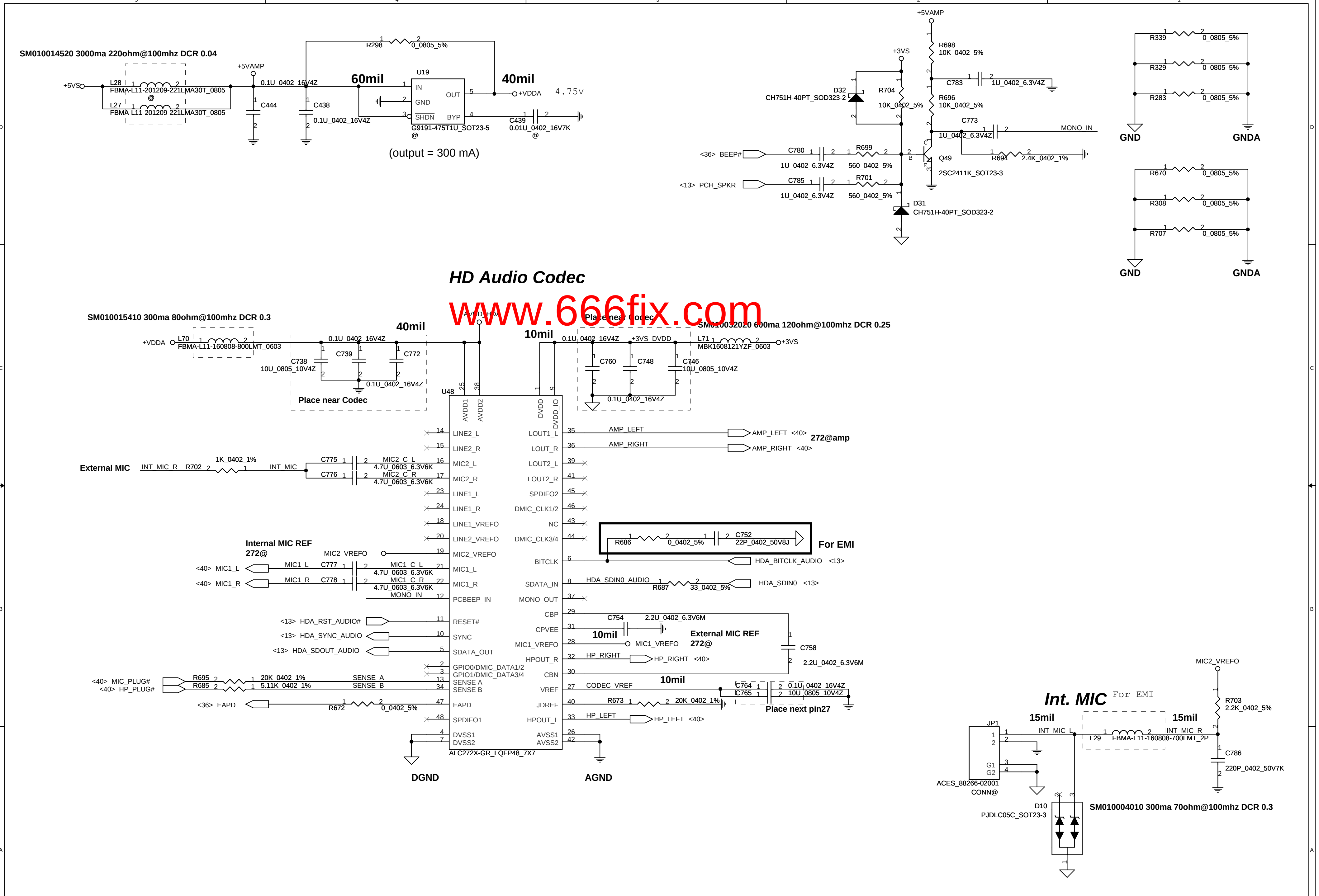
				Date: Thursday, January 20, 2011; Sheet 38 of 56



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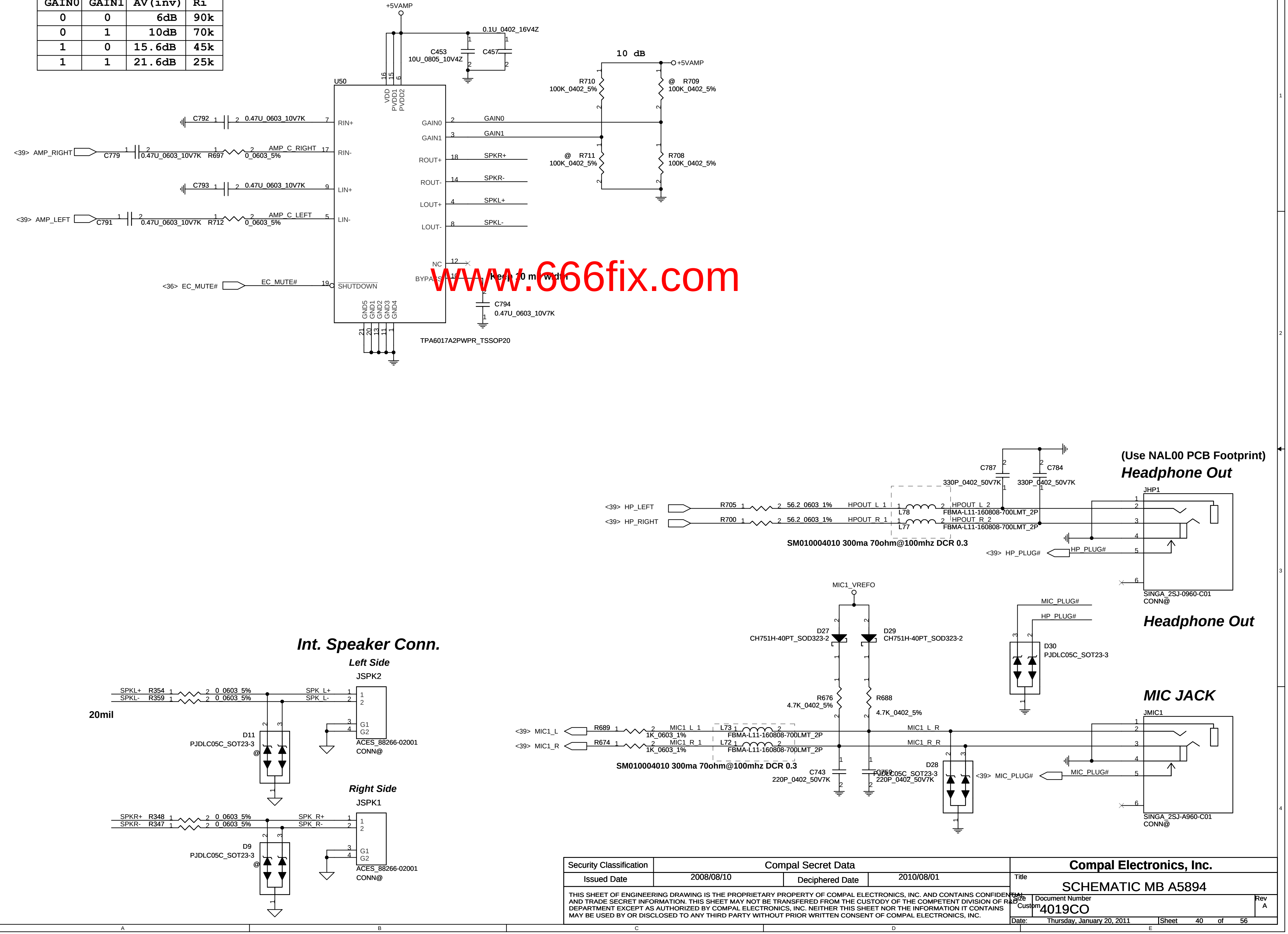
Date: Thursday, January 20, 2011 —

GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k



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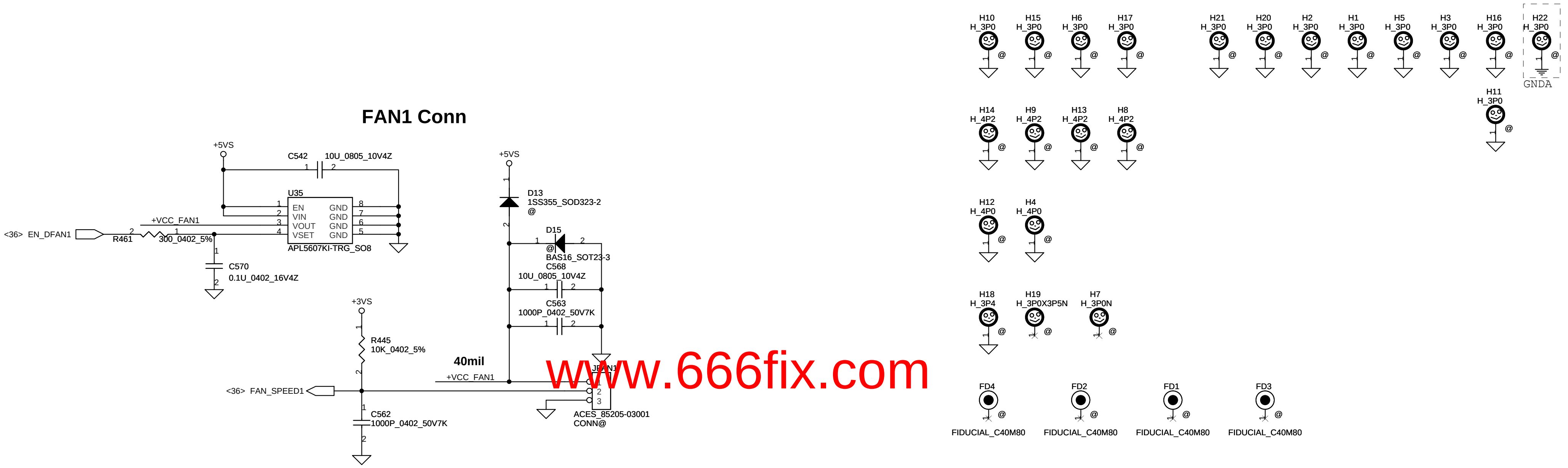

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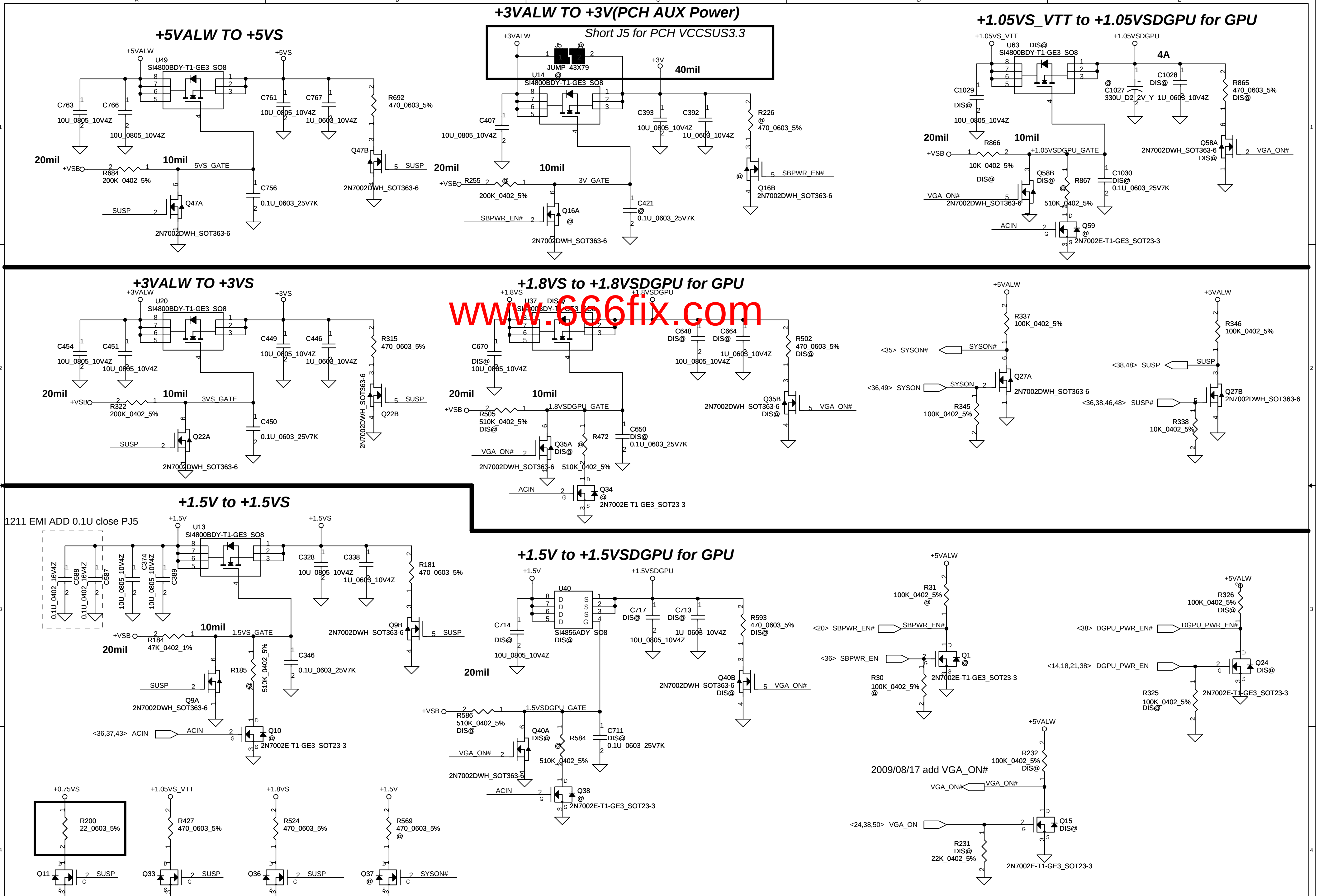
				Size: B; Document Number: 4019CO; Rev: A
				Date: Thursday, January 20, 2011; Sheet 41 of 56



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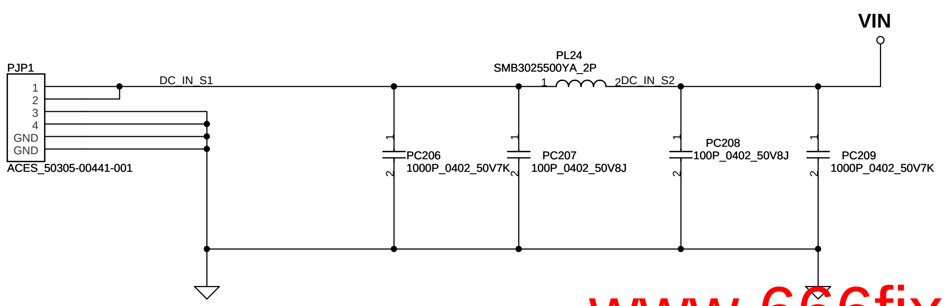
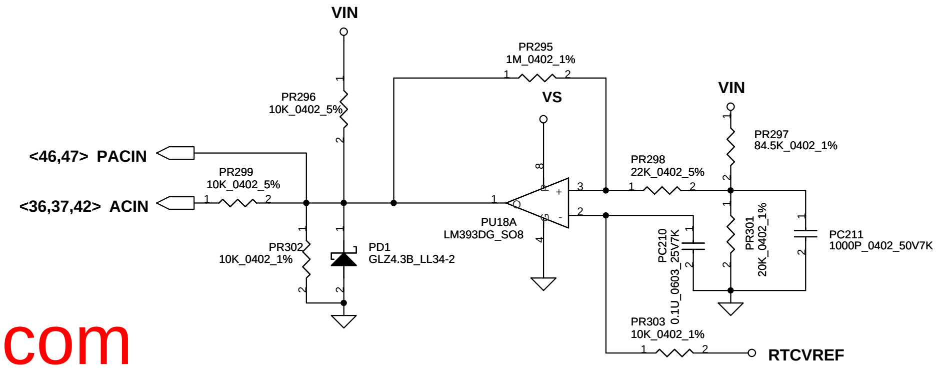
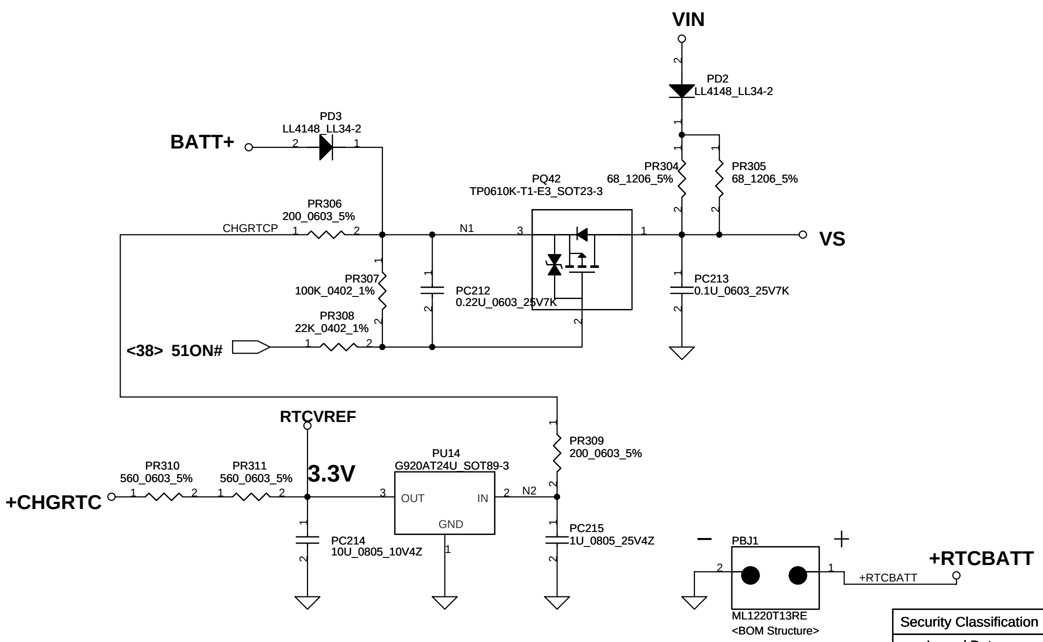
				Date: Thursday, January 20, 2011; Sheet 42 of 56

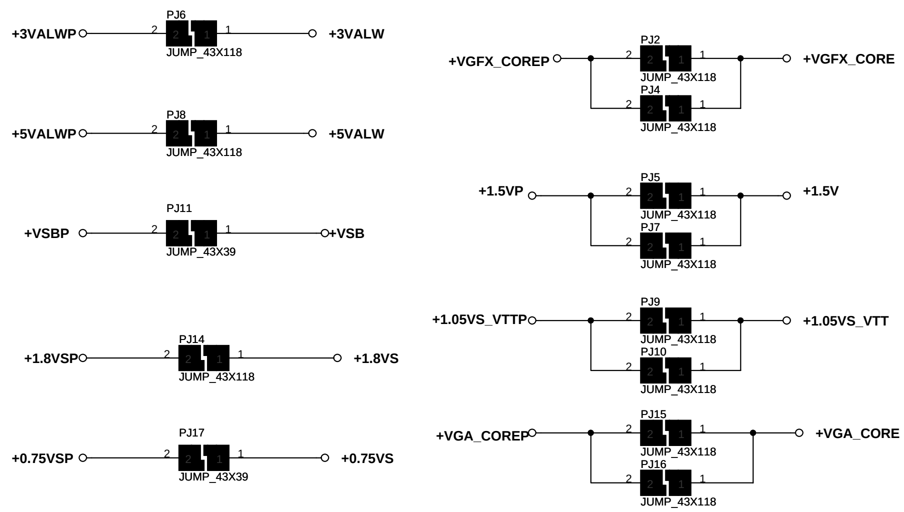




Vin Dectector

	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V





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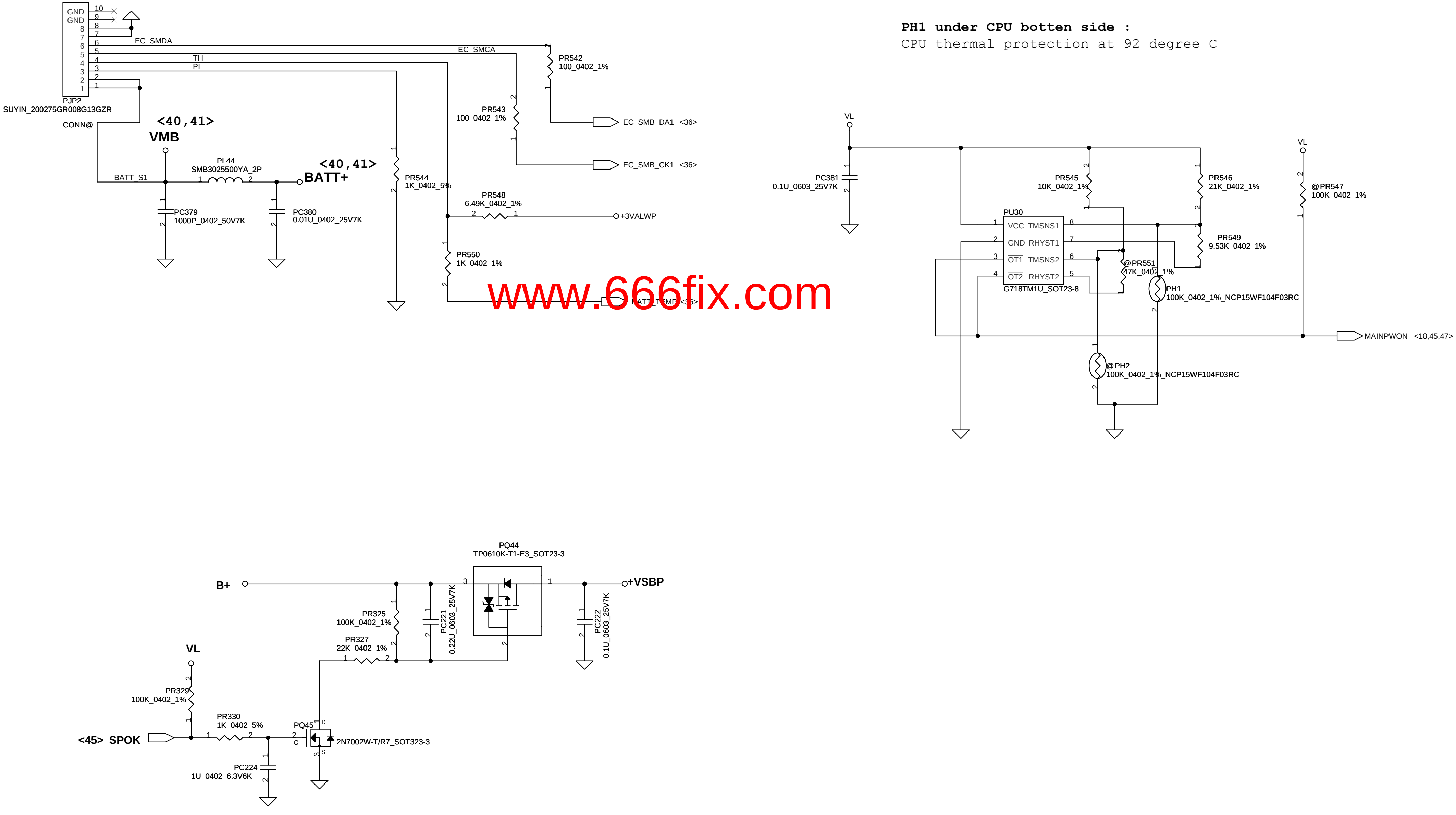

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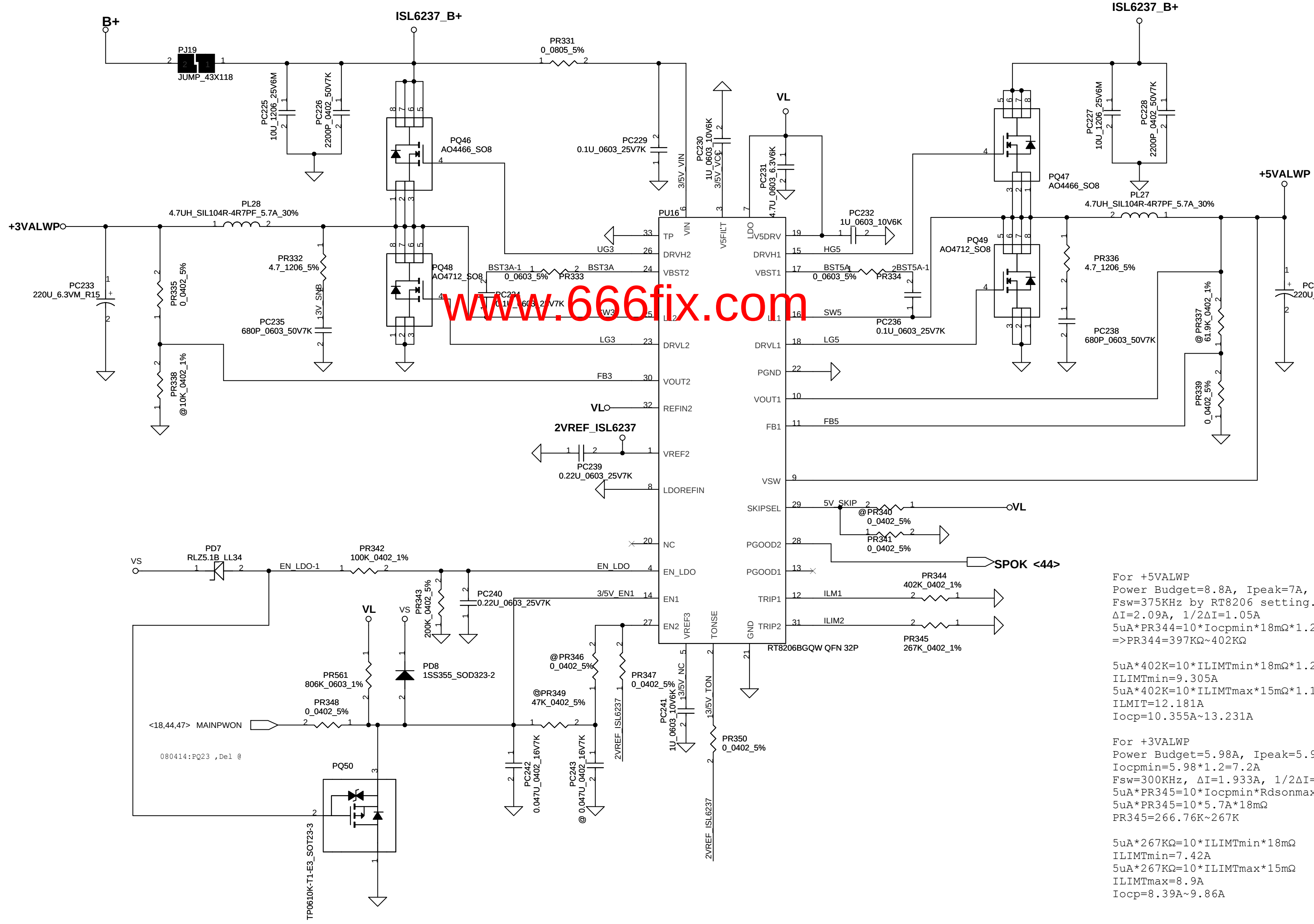

For +5VALWP
Power Budget=8.8A, Ipeak=7A, I max=4.9A
Fsw=375KHz by RT8206 setting.
ΔI=2.09A, 1/2ΔI=1.05A
5uA*PR344=10*Iocpmin*18mΩ*1.2
=>PR344=397KΩ~402KΩ

5uA*402K=10*ILIMTmin*18mΩ*1.2
ILIMTmin=9.305A
5uA*402K=10*ILIMTmax*15mΩ*1.1
ILMIT=12.181A
Iocp=10.355A~13.231A

For +3VALWP
Power Budget=5.98A, Ipeak=5.98A, Imax=4.2A
Iocpmin=5.98*1.2=7.2A
Fsw=300KHz, ΔI=1.933A, 1/2ΔI=0.966A
5uA*PR345=10*Iocpmin*Rdsonmax
5uA*PR345=10*5.7A*18mΩ
PR345=266.76K~267K

5uA*267KΩ=10*ILIMTmin*18mΩ
ILIMTmin=7.42A
5uA*267KΩ=10*ILIMTmax*15mΩ
ILIMTmax=8.9A
Iocp=8.39A~9.86A

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Issued Date	2009/02/04	Deciphered Date	2010/08/01

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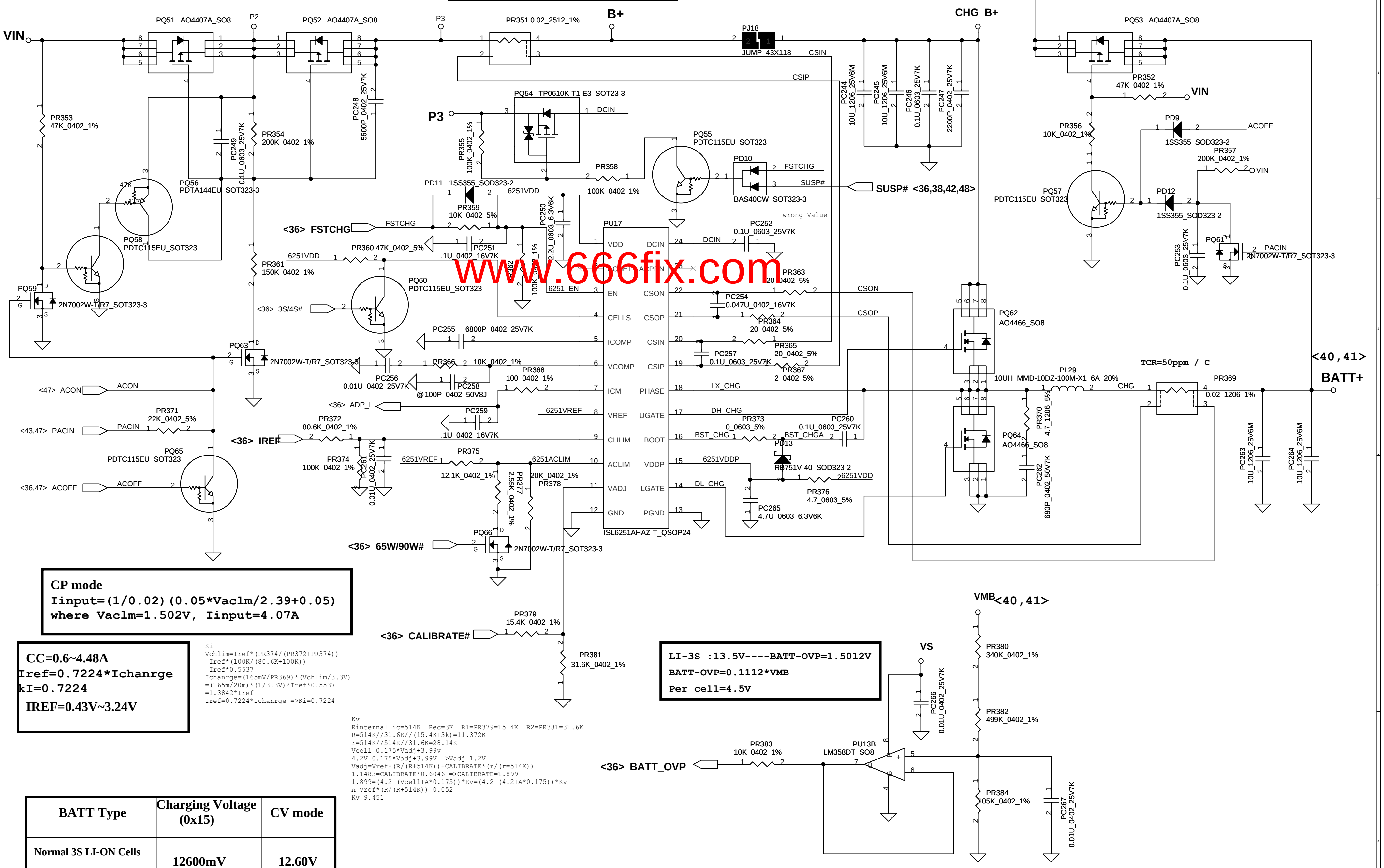
Iada=0~4.74A(90W/19V=4.736A)
Iada=0~3.42A(90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

CC=0.6~4.48A
Iref=0.7224*Ichanrge
kI=0.7224
IREF=0.43V~3.24V

Ki
Vchlim=Iref*(PR374/(PR372+PR374))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichanrge=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichanrge =>Ki=0.7224

Kv
Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
R=514K//31.6K//(15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451

LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=4.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

-

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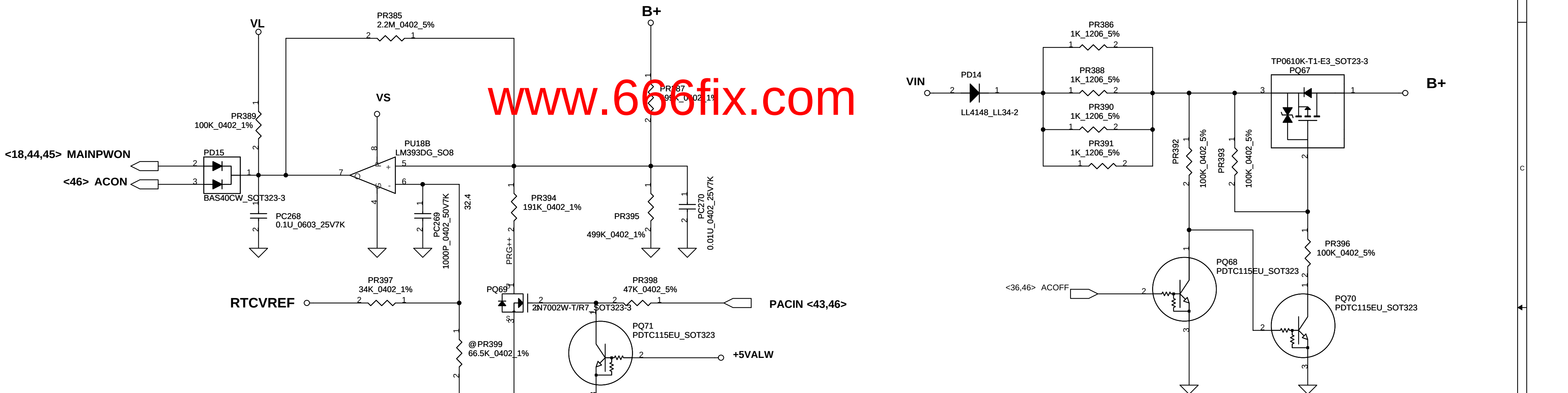

ACIN

Precharge detector	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

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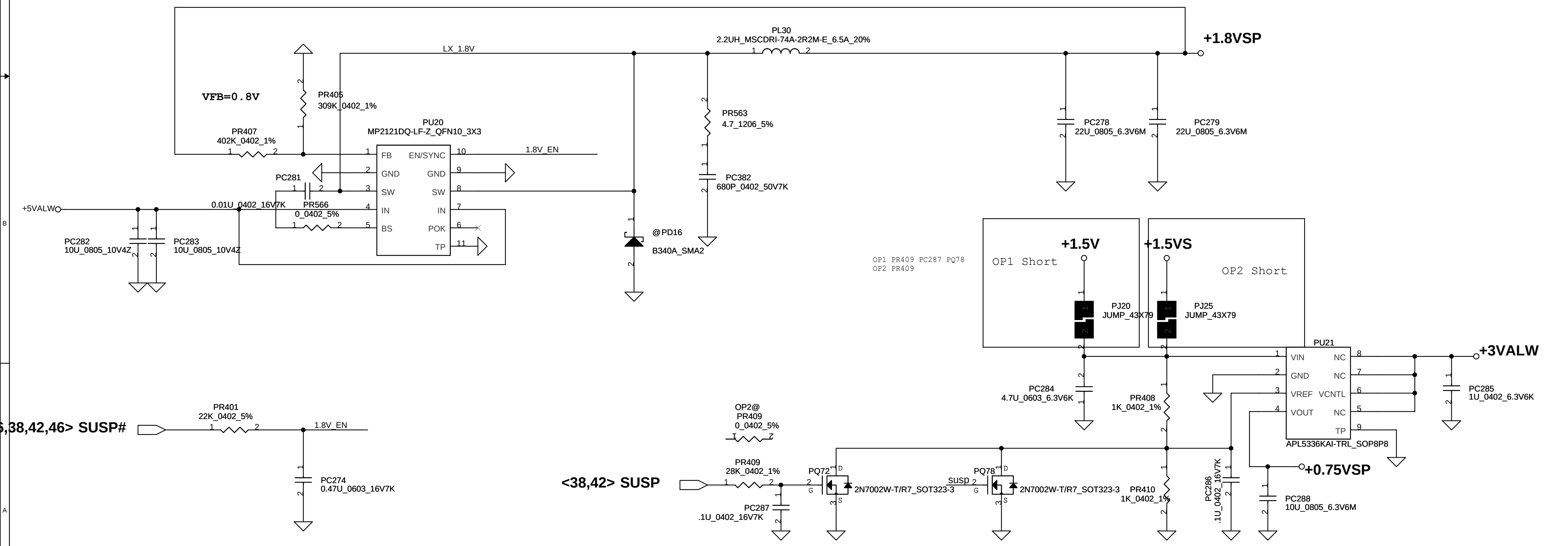

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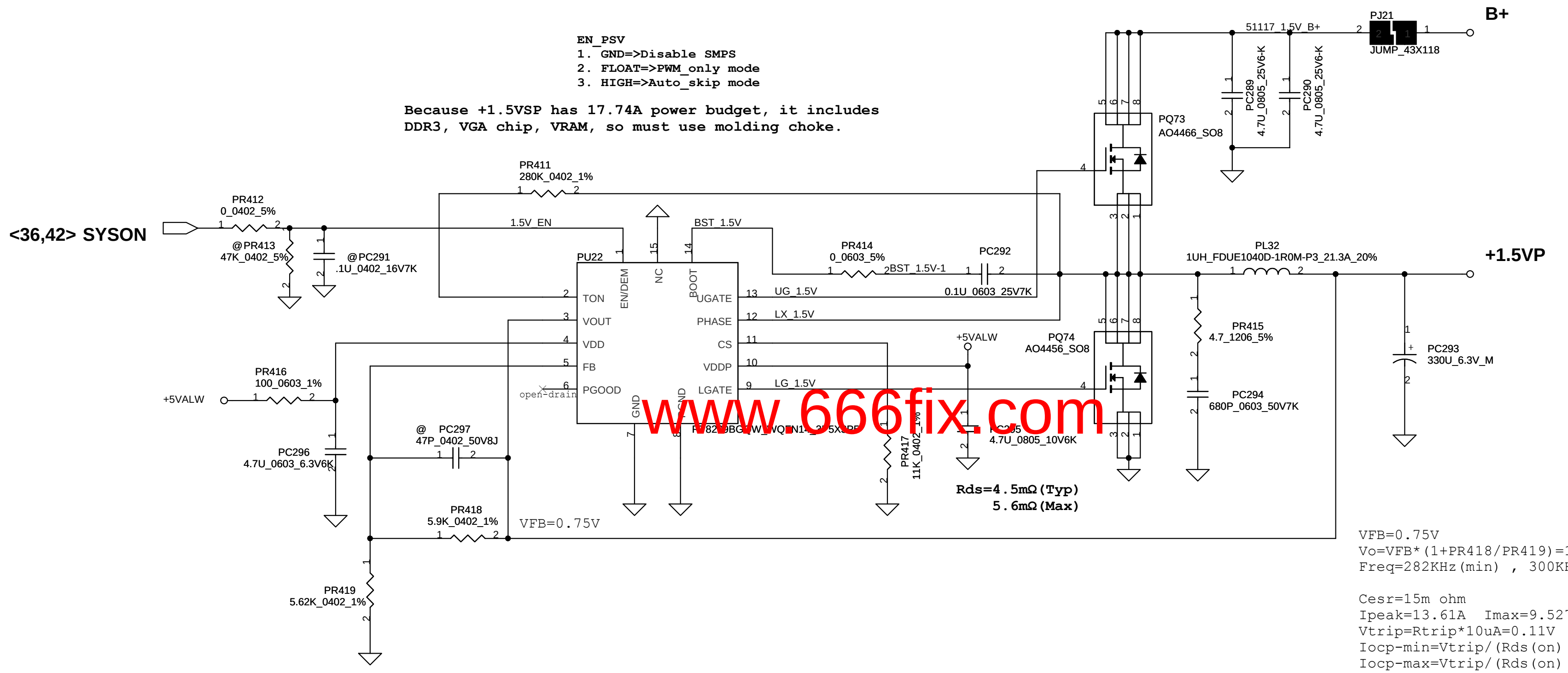

VFB=0.75V
Vo=VFB*(1+PR418/PR419)=1.52V
Freq=282KHz(min) , 300KHz(typ)

Cesr=15m ohm
Ipeak=13.61A Imax=9.527A
Vtrip=Rtrip*10uA=0.11V
Iocp-min=Vtrip/(Rds(on)(max)*1.2)+Delta I / 2= 18.67A
Iocp-max=Vtrip/(Rds(on)(typ)*1.2)+Delta I / 2=22.67A
Iocpmin=18.67A
ΔI=((19-1.5)*(1.5/19))/(L*Freq)=4.605A
1/2ΔI=2.3A

Iocp=18.67A~22.67A

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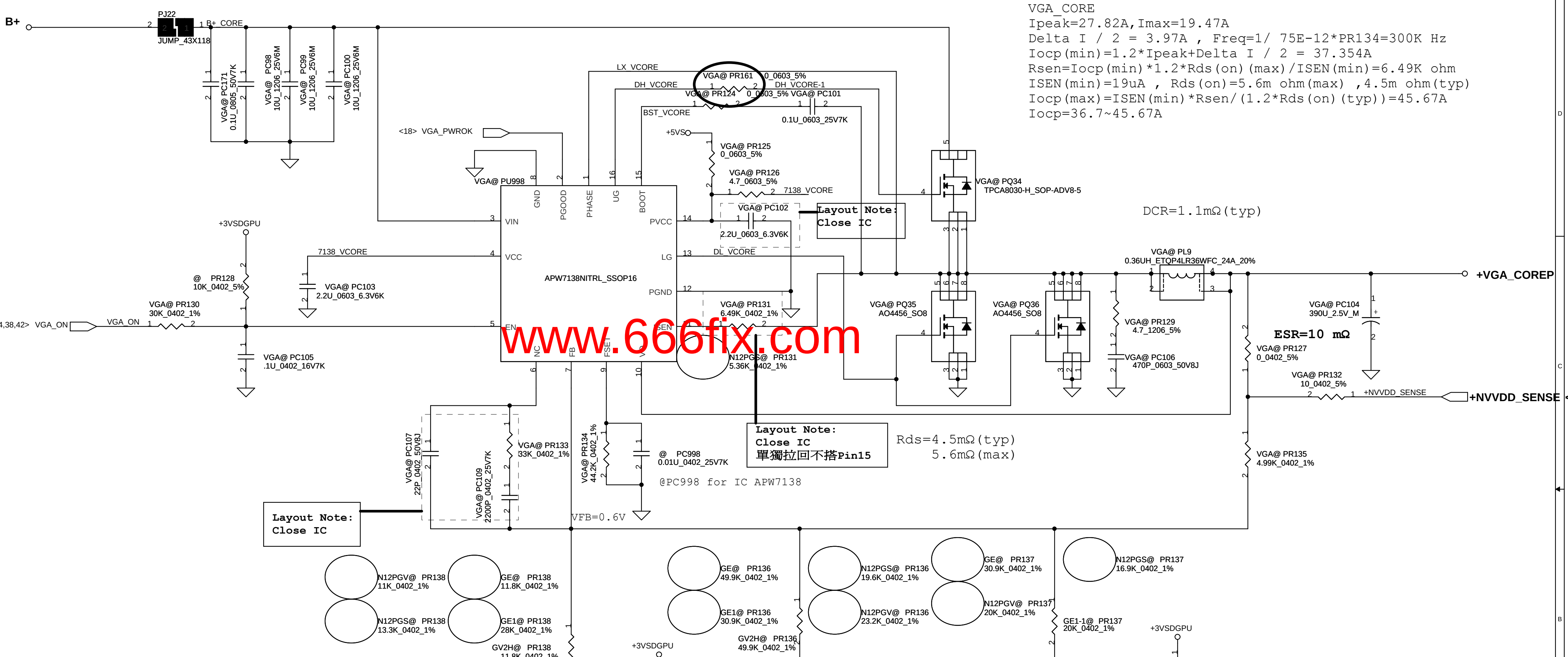
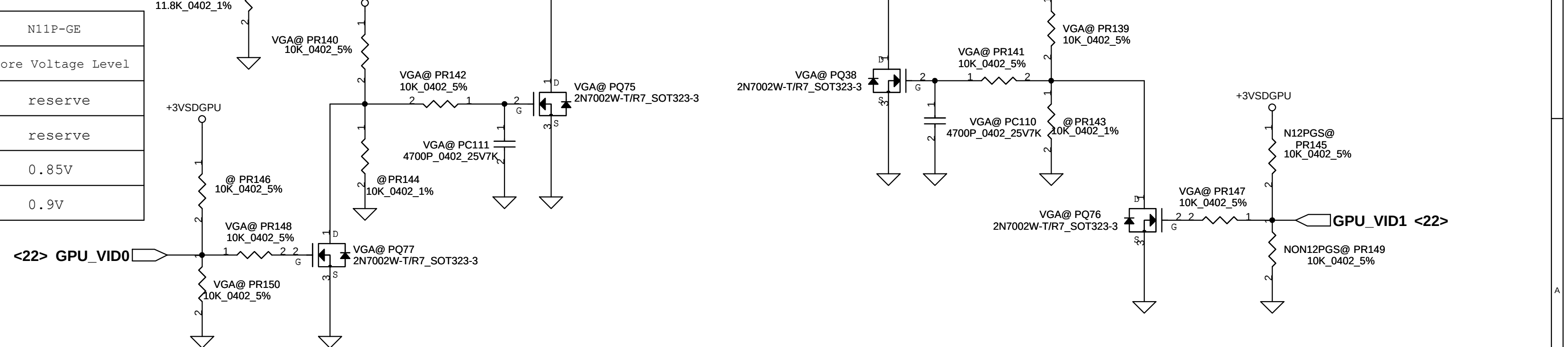
VGA_CORE
Ipeak=27.82A,Imax=19.47A
Delta I / 2 = 3.97A , Freq=1/ 75E-12*PR134=300K Hz
Iocp(min)=1.2*Ipeak+Delta I / 2 = 37.354A
Rsen=Iocp(min)*1.2*Rds(on)(max)/ISEN(min)=6.49K ohm
ISEN(min)=19uA , Rds(on)=5.6m ohm(max) ,4.5m ohm(typ)
Iocp(max)=ISEN(min)*Rsen/(1.2*Rds(on)(typ))=45.67A
Iocp=36.7~45.67A





		N11P-GV2H	N11P-GE1	N11P-GE
GPU_VID0	GPU_VID1	Core Voltage Level	Core Voltage Level	Core Voltage Level
1	1	reserve	reserve	reserve
0	1	reserve	0.8V	reserve
1	0	0.85V	0.85V	0.85V
0	0	0.9V	0.95V	0.9V

GPU_VID0	GPU_VID1	N12P-GS	N12P-GV
1	1	0.825V	0.875V
0	1	0.975V	1.006V
1	0	1.0V	1.025V
0	0	reserve	1.156V

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Issued Date	2009/08/25	Deciphered Date	2010/08/25

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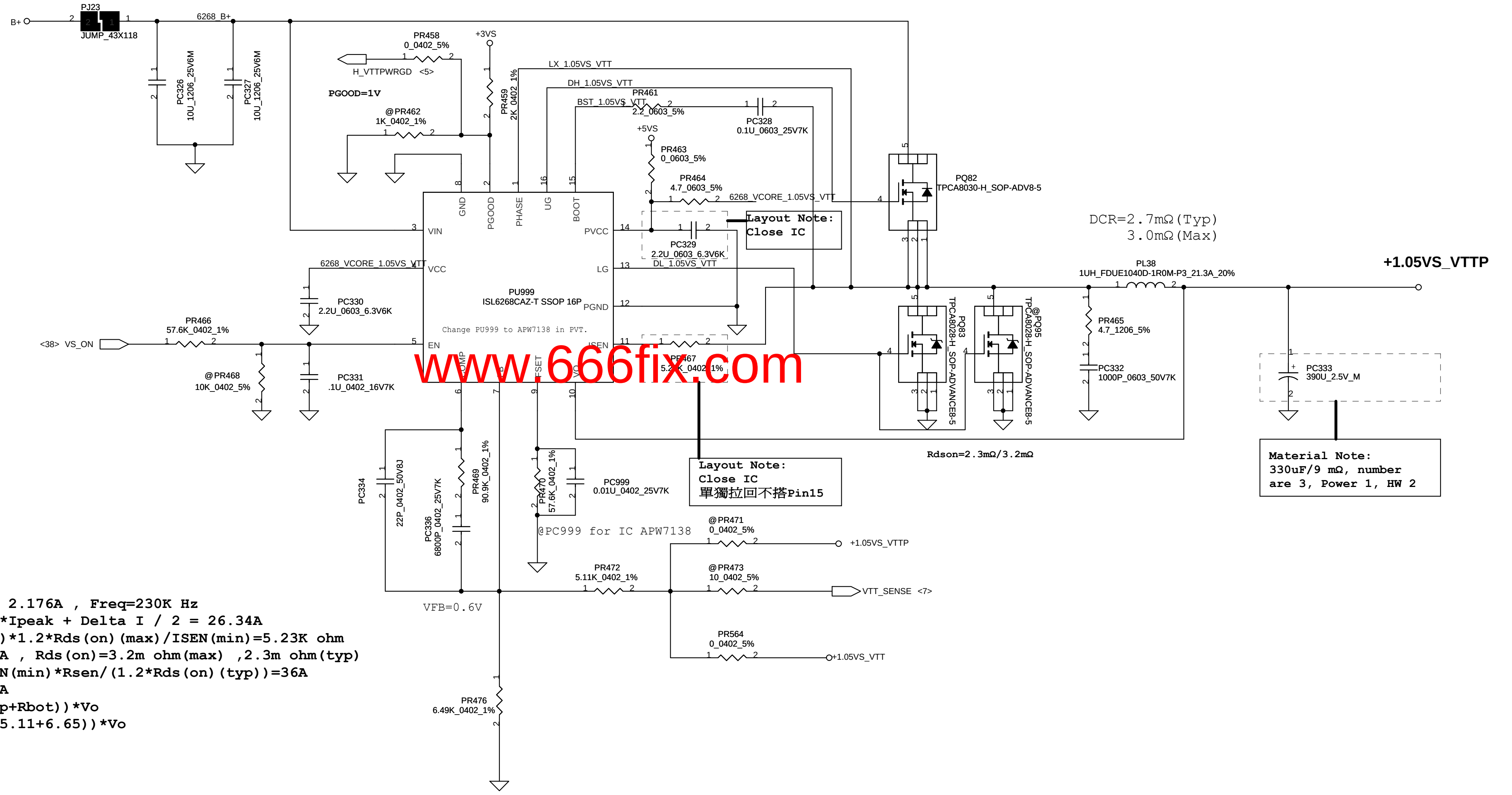

+1.05VS_VTT
Ipeak=20.14A
Imax=14.10A
Delta I / 2 = 2.176A , Freq=230K Hz
Iocp(min)=1.2*Ipeak + Delta I / 2 = 26.34A
Rsen=Iocp(min)*1.2*Rds(on)(max)/ISEN(min)=5.23K ohm
ISEN(min)=19uA , Rds(on)=3.2m ohm(max) ,2.3m ohm(typ)
Iocp(max)=ISEN(min)*Rsen/(1.2*Rds(on)(typ))=36A
Iocp=26.34~36A
Vref=(Rb/(Rtop+Rbot))*Vo
=>0.6=(6.65/(5.11+6.65))*Vo
Vo=1.061V

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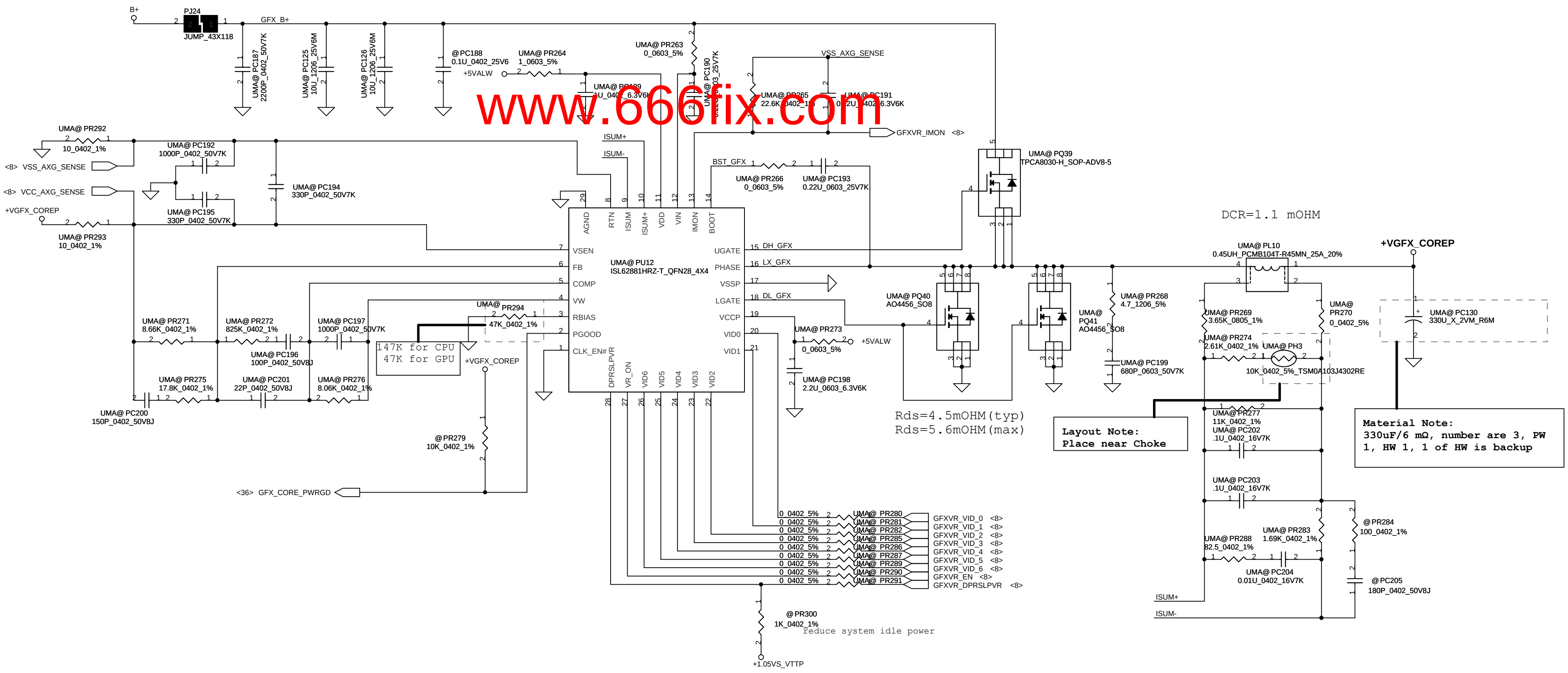
Intel Auburndale CPU(Integrate Graphics) Ipeak=22A Imax=15A
OCP calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum)=0.617
where Rn=PR277 // (PR274+PH3)=5.875k ohm
Rsum=PR269=3.65k ohm
LL=2*Rdroop*G1*DCR/Ri= 6.96m V/A
where Rdroop=PR271=8.66k ohm, Ri=PR283=1.69k ohm
Iocp=OCP Threshold*Rdroop/LL=24.89A



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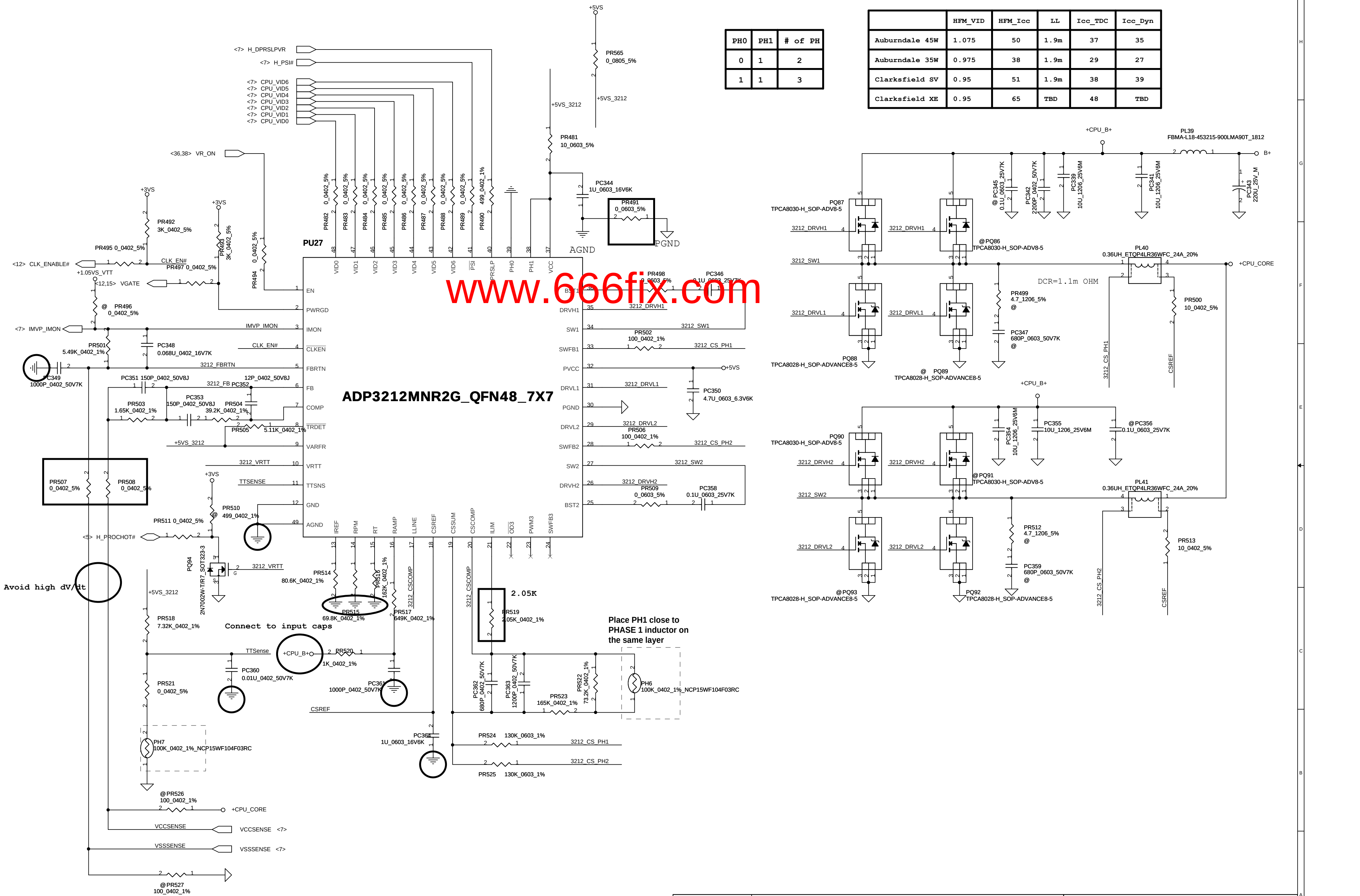
PH0	PH1	# of PH
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD



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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Modify VGA_COREP circuit	update VGA_COREP Vout by NV spec.	0.1	50	change PR136 from SD034604280 to SD034499280. Delete PR137 SD034309280. Change PR138 SD034147280 to SD034118280.	2010-0615	PVT
2							
3	Modify VGA_COREP circuit	Modify N12PGS to let Vboot=0.975V, that is VID0=0, VID1=1	0.2	50	Add PR145 SD028100280. delete PR149 SD028100280.	2010-1102	MP
4	Modify +1.5VP circuit	Because run 3Dmark has voltage too low, increase 1.5V.	0.2	49	Change PR419 from SD034576180 to SD034562180. Only for N12PGS.	2010-1102	MP
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							
19							
20							
21							
22							
23							

A -->Modify item

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20091214 Modify For N11P-GV2H	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung :SA000035720	H 45K	H 35K	H 30K	L 20K	L 10K	L 15K
64MX16 Hynix:SA000032490	H 45K	H 35K	H 30K	L 15K	L 10K	L 15K

20100113 Modify For N11P-GE1	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung:SA000035720	H 45K	H 35K	H 10K	L 20K	L 10K	L 15K
64MX16 Hynix:SA000032490	H 45K	H 35K	H 10K	L 15K	L 10K	L 15K

20100601 Modify For N11P-GE	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung:SA000035720	H 45K	L 35K	L 10K	L 20K	L 10K	H 15K
64MX16 Hynix:SA000032490	H 45K	L 35K	L 10K	L 15K	L 10K	H 15K
128MX16 Samsung:SA00003MQ40	H 45K	L 35K	L 10K	L 45K	L 10K	H 15K
128MX16 Hynix:SA00003VS10	H 45K	L 35K	L 10K	L 35K	L 10K	H 15K

20100909 Modify For N12P-GS VRAM: DDR3 900 down to 800	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
64MX16 (800) Samsung:SA000035720	H 45K	H 35K	L 25K	NC	NC	L 10K	L 10K	H 15K
64MX16 (800) Hynix:SA000032490	H 45K	H 35K	L 25K	NC	NC	L 5K	L 10K	H 15K
64MX16 (900) Samsung:K4W1G1646G-BC11 SA00004GS10	H 45K	L 35K	L 25K	NC	NC	L 20K	L 10K	H 15K
64MX16 (900) Hynix:H5TQ1G63DFR-11C SA000041S40	H 45K	L 35K	L 25K	NC	NC	L 15K	L 10K	H 15K
128MX16 (800) Samsung:SA00003MQ40	H 45K	H 35K	L 25K	NC	NC	L 45K	L 10K	H 15K
128MX16 (800) Hynix:SA00003VS10	H 45K	H 35K	L 25K	NC	NC	L 35K	L 10K	H 15K
128MX16 (900) Samsung:K4W2G1646C-HC11 SA000047Q20	H 45K	L 35K	L 25K	NC	NC	L 45K	L 10K	H 15K
128MX16 (900) Hynix:H5TQ2G63BFR-11C SA00003YO20	H 45K	L 35K	L 25K	NC	NC	L 35K	L 10K	H 15K

20101220 Modify For N12P-GV VRAM: DDR3 900 down to 800	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
64MX16 (900) Samsung:K4W1G1646G-BC11 SA00004GS10	H 45K	L 35K	L 5K	L 5K	L 10K	L 20K	H 10K	H 5K
64MX16 (900) Hynix:H5TQ1G63DFR-11C SA000041S40	H 45K	L 35K	L 5K	L 5K	L 10K	L 15K	H 10K	H 5K
128MX16 (900) Samsung:K4W2G1646C-HC11 SA000047Q20	H 45K	L 35K	L 5K	L 5K	L 10K	L 45K	H 10K	H 5K
128MX16 (900) Hynix:H5TQ2G63BFR-11C SA00003YO20	H 45K	L 35K	L 5K	L 5K	L 10K	L 35K	H 10K	H 5K

ROM_SI，爲Vram配打電阻

BOM Config		
PEW71 SKU N11P-GE 1G DISCRETE ONLY without 3G	BT@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,GE@,NonOPT@	431869BOL21
PEW71 SKU N11P-GV2H-A3 1G DISCRETE ONLY without 3G	BT@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,GV2H@,GV2HA3@,NonOPT@,NonGE@	431869BOL22
PEW51 SKU N11P-GV2H-A3 1G DISCRETE ONLY without 3G	BT@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,GV2H@,GV2HA3@,NonOPT@,NonGE@	431869BOL31
PEW51 SKU N11P-GE 1G DISCRETE ONLY without 3G	BT@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,GE@,NonOPT@	431869BOL32
PEW51 SKU N11P-GE 2G DISCRETE ONLY without 3G	BT@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,GE@,NonOPT@	431869BOL33
PEW71 SKU N11P-GE 1G Optimus without 3G	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,X7621@,GE@	431869BOL23
PEW71 SKU N11P-GE 2G Optimus without 3G	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,X7601@,GE@	431869BOL24
PEW71/91 SKU N12P-GS 1G Optimus without 3G	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,X7621@,GS@	431869BOL26
PEW71/91 SKU N12P-GS 2G Optimus without 3G	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,X7601@,GS@	431869BOL27
PEW51 SKU N12P-GS 1G DISCRETE ONLY without 3G	BT@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,GS@,NonOPT@	431869BOL34

*沒打 (431869BOL31)

*沒打 (431869BOL33)

以上爲LA5893PR10, Footprint:GB1-128

SMT MB A5894 PEW71 GS OPT 1G WHDMI	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,GS@	4319COBOL01
SMT MB A5894 PEW71 GS OPT 2G WHDMI	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,GS@	4319COBOL02
SMT MB A5894 PEW71 GV OPT 512M WHDMI	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,GV@	4319COBOL03
SMT MB A5894 PEW71 GV OPT 1G WHDMI	BT@,DIS@,SGOPT@,UMOP@,OPT@,71@,GV@	4319COBOL04

以上爲LA5894PR10, Footprint:GB2-128 Compability GB2B-128

PCB

ZZZ
LA-5894P REV0 M/B

GV2HA2@
U51
N11P-GV2H-A2_BGA969

GV2HA3@
U51
N11P-GV2H-A3_BGA969

GE1@
U51
N11P-GE1-A3 BGA 969P

GE@
U51
N11P-GE-A1 BGA 969P

GS@
U51
N12P-GS-A1 BGA 973P

GV@
U51
N12P-GV-OP-B-A1 BGA 973P

ZZZ3
X7601@
X76248BOL01

ALT. GROUP PARTS 2G HYN

ZZZ2
X7622@
X76198BOL22

ALT. GROUP PARTS 1G HYN

ZZZ1
X7621@
X76198BOL21

ALT. GROUP PARTS 1G SAM

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