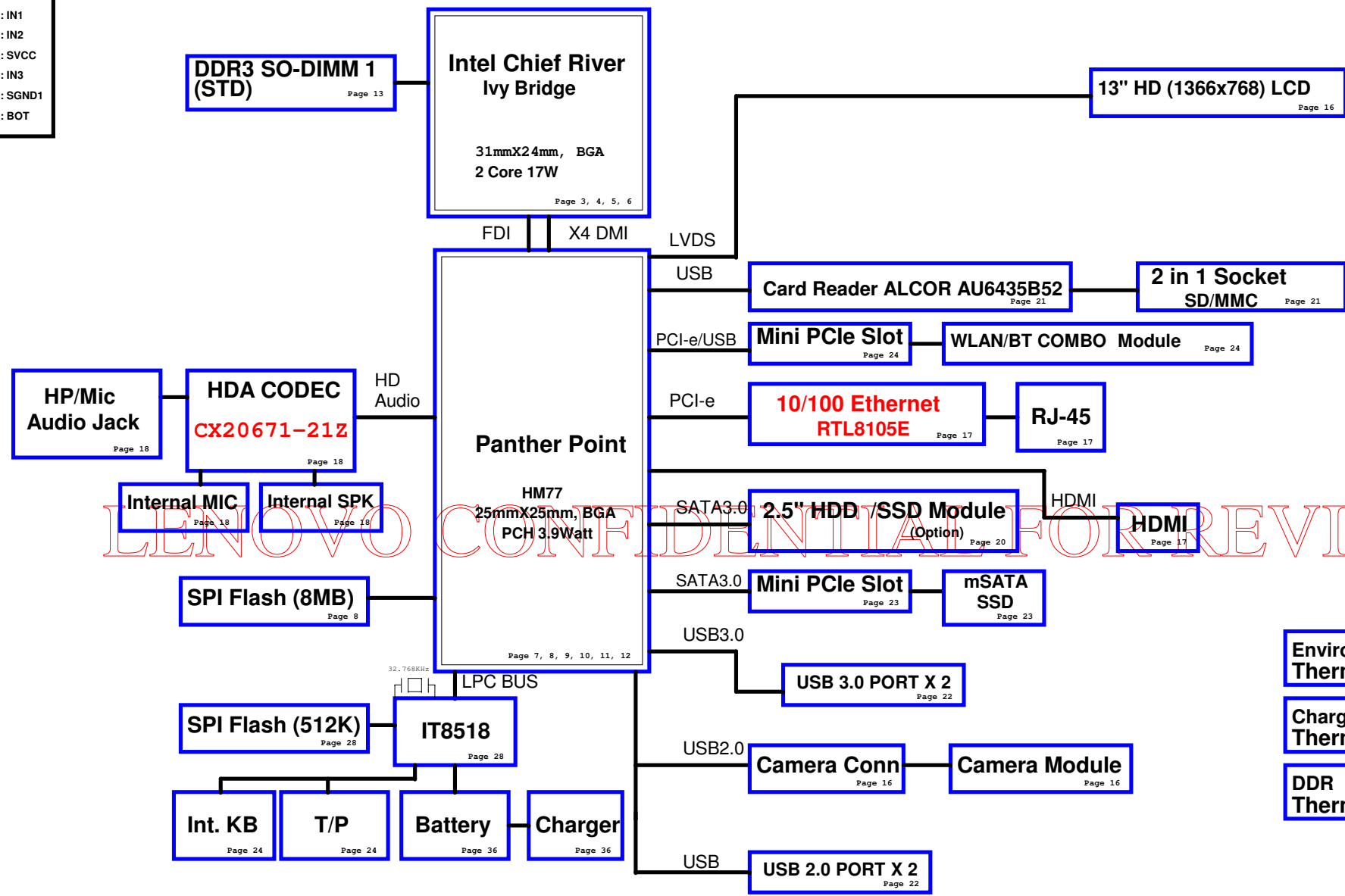


LZ7 13" Block Diagram -- Intel Chief River UMA

POWER

DC/DC 3V_PCU, 5V_PCU, +15V	Page 31
REGULATOR (DDR3) 1.5V_SUS, 0.75V_DDR_VTT	Page 32
REGULATOR 1.05V&1.8V	Page 33
REGULATOR VCCSA	Page 34
CPU Core	Page 35
Charger	Page 36
RUN POWER SW/Discharge 5V_SUS, 3V_S5, 5V_S5 +3V, +5V	Page 37

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : SVCC
- LAYER 6 : IN3
- LAYER 7 : SGND1
- LAYER 8 : BOT



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- Environment temperature Thermal Sensor** (Page 27)
- Charger temperature Thermal Sensor** (Page 27)
- DDR Thermal Sensor** (Page 27)

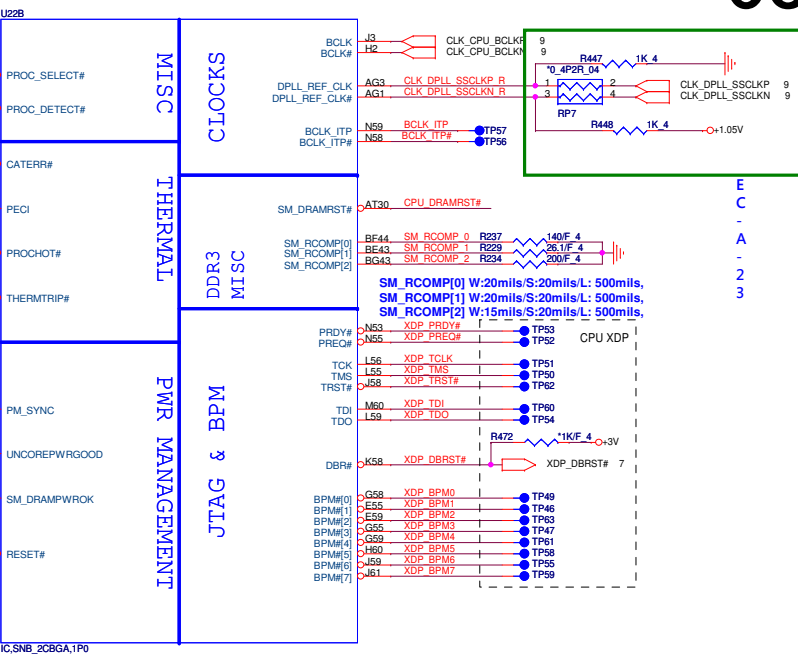
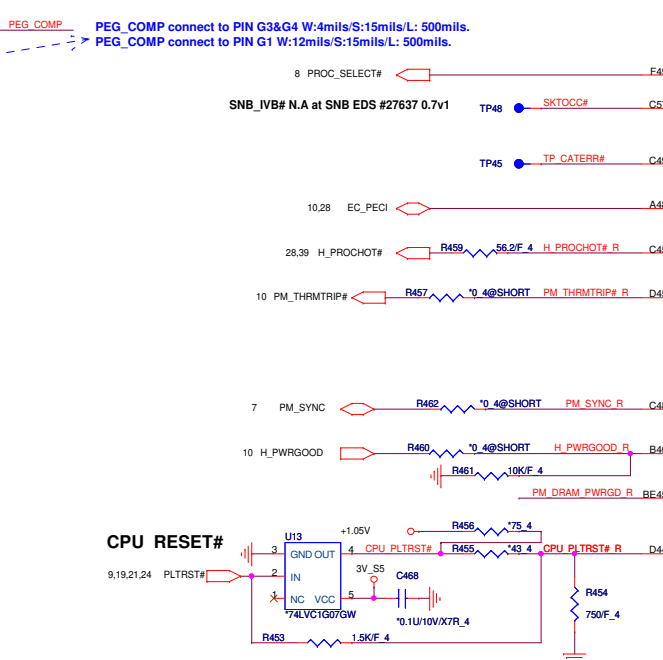
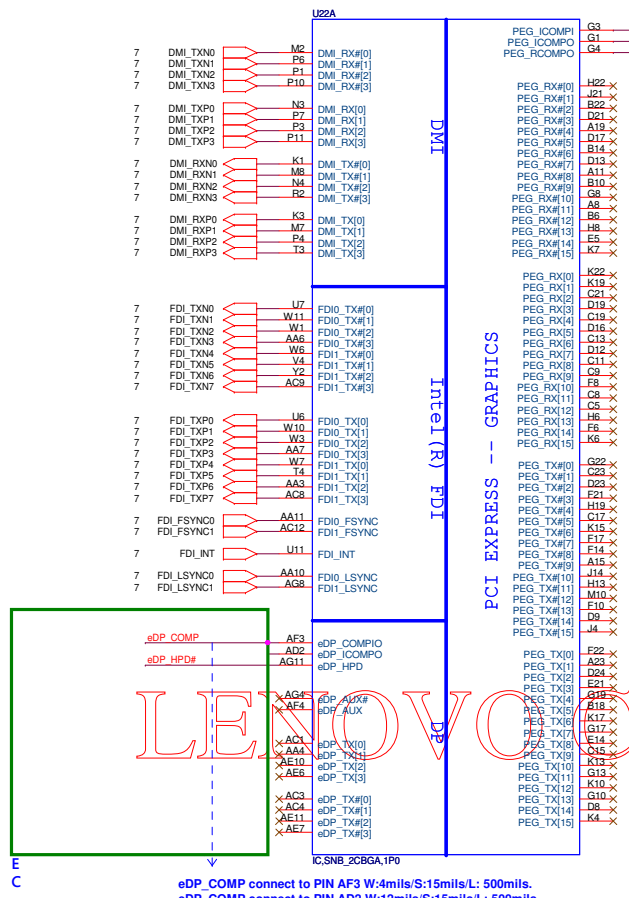
Table of Contents

PAGE	DESCRIPTION
01	LOCK DIAGRAM(UMA)
02	FRONT PAGE
03-06	Sandy Bridge
07-12	Cougar Point-PCH
13	DDRIII SO-DIMM
15	PS8622 LVDS converter
16	LCD/CAMERA
17	HDMI CONN
18	AUDIO (CX20671-21Z, SPK)
19	LAN[RTL8105E]
20	SATA
21	Card Reader-AU6435B52-GDL
22	USB2.0 X2/USB3.0 X2
23	MINI Card (SSD)
24	WLAN/BT
25	KB/TP/LID/AUDIO USB Conn
26	Blank
27	FAN/Thermal
28	KBC IT8518/19
29	SW/LED
30	Screw Hole/EMI/ESD
31	Power Block Diagram
32	3V/5V (TPS51123ARGERR)
33	Discharge
34	CHARGER (BQ24725)
35	DDR3/0.75V (TPS51216)
36	+1.05V(RT8240B)
37	VCCSA (RT8241A)
38	1.8V(TPS54318)
39	CPU(ISL95831)IMVP1+1
40	Power On Sequence
41	EC RECORD DV
42	Power EC RECORD DV
43	
44	
45	
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47	

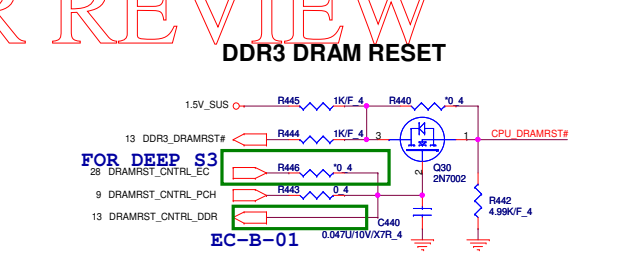
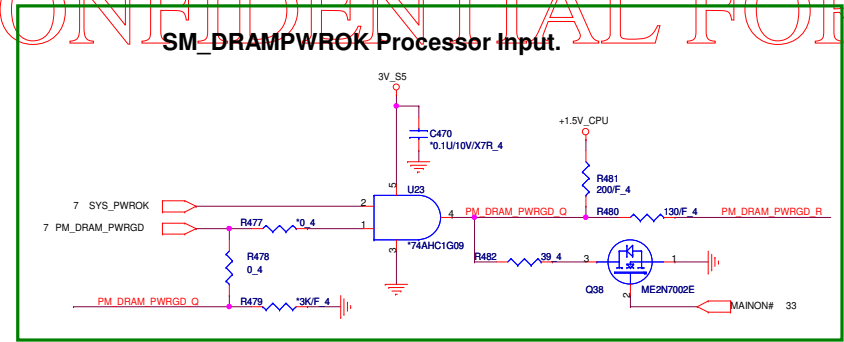
Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	16, 32, 34, 35, 36, 37, 39	MAIN POWER		S0~S5
+3V_RTC	+3.0V~+3.3V	7, 8, 11, 28	RTC		S0~S5
3VPCU	+3.3V	8, 16, 19, 25, 28, 29, 32, 33, 34, 38	IT8518/19 POWER	3V5V_EN	S0~S5
5VPCU	+5V	16, 32, 33, 35, 36, 37, 38, 39	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
15V	15V	16, 32, 33, 35	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	19, 33	LAN POWER	LAN_ON	
5V_S5	+5V	11, 22, 33	PCH SUS POWER	S5_ON	S0~S3
3V_S5	+3.3V	3, 7, 8, 9, 10, 11, 24, 33	Sys Management,PCH Resume Well, USB,WLAN,WiMAX POWER	S5_ON	S0~S3
5VSUS	+5V		SLP_S4# CTRLD POWER	SUSON	S0~S3
3VSUS	+3.3V		SLP_S4# CTRLD POWER	SUSON	S0~S3
1.5V_SUS	+1.5V	3, 11, 13, 33, 35	DDR3 SODIMM POWER	SUSON	S0~S3
+0.75V_DDR_VTT	+0.75V	7, 11, 16, 17, 18, 20, 27, 33, 34	DDR3 SODIMM REFERENCE POWER	MAINON	S0
+5V	+5V	16, 32, 34, 35, 36, 37, 39	SLP_S3# CTRLD POWER	MAINON	S0
+3V	+3.3V	8, 7, 8, 9, 10, 11, 13, 15, 16, 17, 18, 19, 20, 21, 23, 24, 25, 27, 28, 32, 33, 34, 35, 36, 37, 38, 39	SLP_S3# CTRLD POWER	MAINON	S0
+VCC_GFX		5, 39	VGA CORE POWER	MAINON	S0
VCCSA	+0.8V~+0.9V	5, 33, 37	Sandy Bridge Power	MAINON	S0
+1.8V	+1.8V	5, 8, 11, 33, 38	LVDS,NVM POWER	MAINON	S0
+1.05V	+1.05V	3, 5, 7, 8, 9, 11, 15, 33, 36	Sandy Bridge VTT POWER/PCH CORE POWER	MAINON	S0
+VCC_CORE		5, 6, 39	CPU CORE POWER	VRON	S0
+LCDVCC	+3.3V	16	LCD Power	ENVDD	S0
+3V_HDD	+3V	20	ODD Power	ODD_5V_ON	S0
+5V_HDD	+5V	20	HDD Power	MAINON#	S0
BAT-V	+10V~+17V	34	MAIN BATTERY	CHG_PBATT	S0~S5
+1.5V_CPU	+1.5V	3, 5, 35	DDR3 1.5V Rails	PS_S3CNTRL	S0

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eDP_COMP connect to PIN AF3 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN AD2 W:12mils/S:15mils/L: 500mils.



EC - A - 2 3

1.5V_SUS	11,13,33,35
+1.05V	5,7,8,9,11,33,36
+1.3V_CPU	5,35
3V_S5	7,8,9,10,11,18,24,29,33
+3V	7,8,9,10,11,13,16,17,18,19,20,21,23,24,25,27,28,32,33,34,35,36,37,38,39

DP & PEG Compensation

+1.05V R206 10K 4 eDP_HPDI#

+1.05V R448 24.9K 4 eDP_COMP

eDP_COMP and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

+1.05V R450 24.9K 4 PEG_COMP

PEG_ICOMPI and RCOMP0 signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

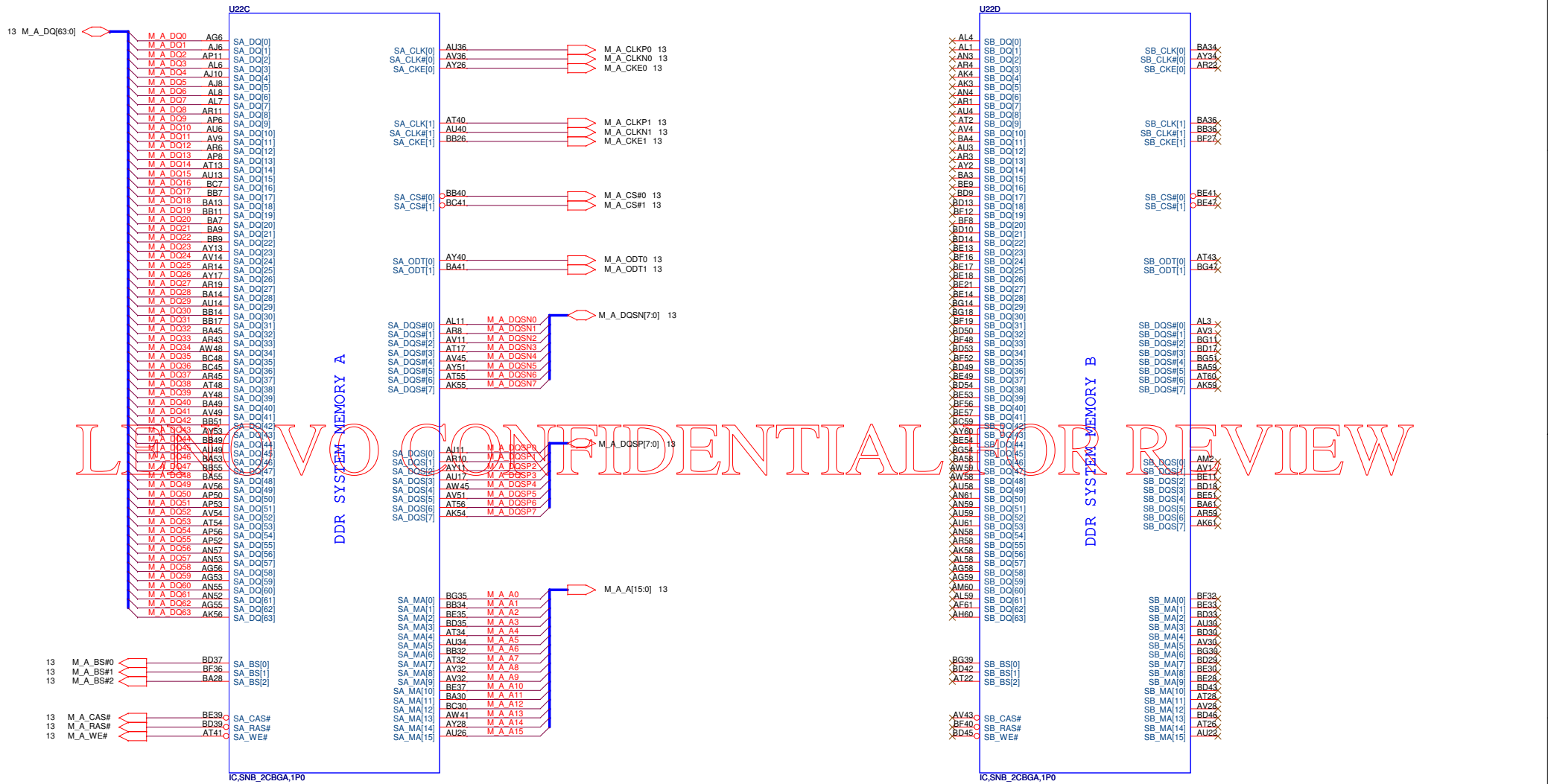
Processor pull-up (CPU)

+1.05V

- H_PROCHOT# R458 62 4
- XDP_TDO R473 51/F 4
- XDP_TMS R239 51/F 4
- XDP_TDI R471 51/F 4
- XDP_PRE# R242 51/F 4
- XDP_TCLK R240 51/F 4
- XDP_TRST# R474 51/F 4

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Ivy Bridge Processor (DDR3)

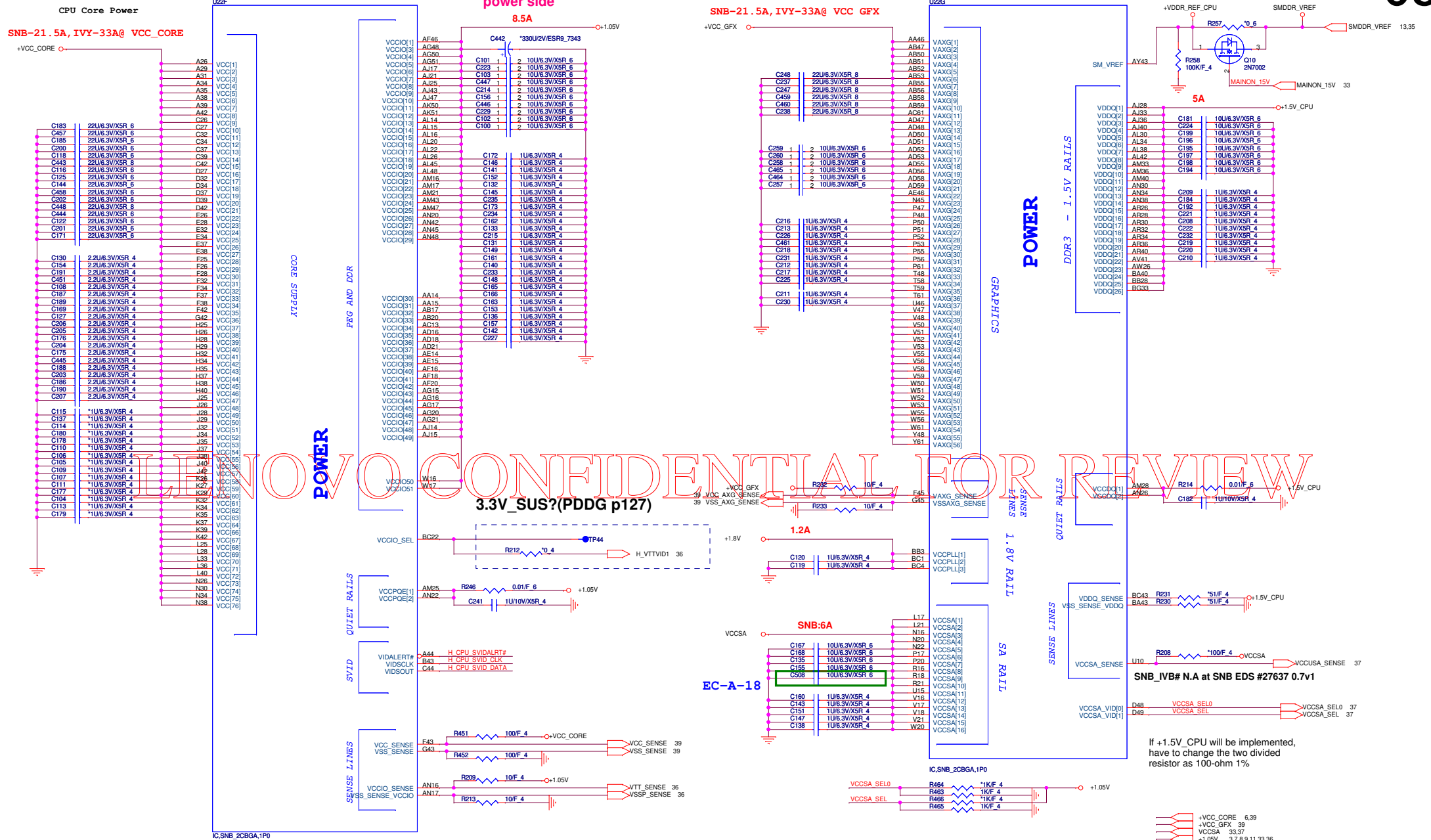


Ivy Bridge Processor (POWER)

Ivy Bridge Processor (GRAPHIC POWER)

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

05



POWER CONFIDENTIAL FOR REVIEW

3.3V_SUS?(PDDG p127)

If +1.5V_CPU will be implemented, have to change the two divided resistor as 100-ohm 1%

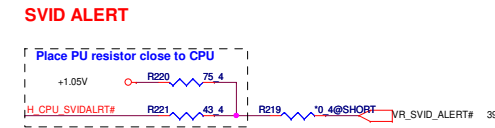
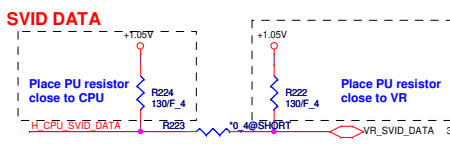
- +VCC_CORE 6,39
- +VCC_GFX 39
- VCCSA 33,37
- +1.05V 3,7,8,11,33,36
- +1.5V_CPU 3,35
- +1.8V 8,11,33,38
- SMDDR_VREF 13,35

SVID CLK

Layout note: need routing together and ALERT need between CLK and DATA.

Place PU resistor close to VR

R217 54.9F 4 +1.05V

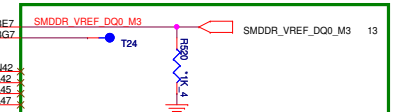
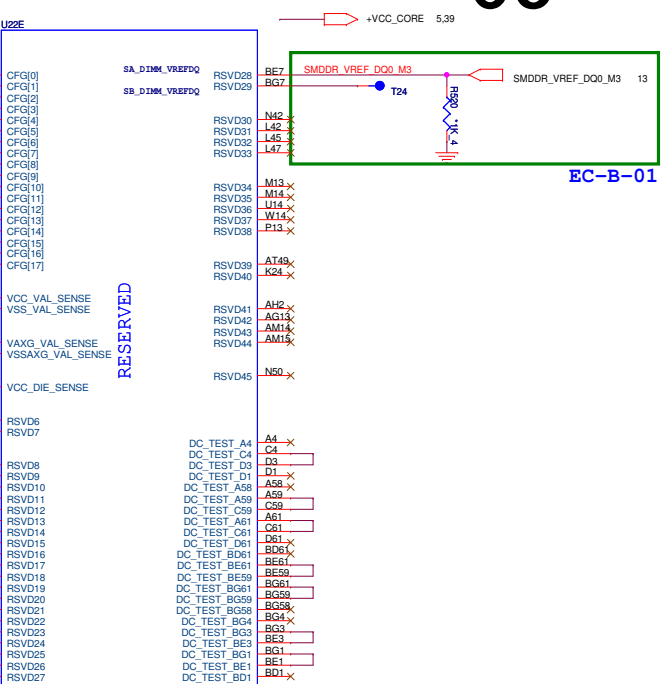
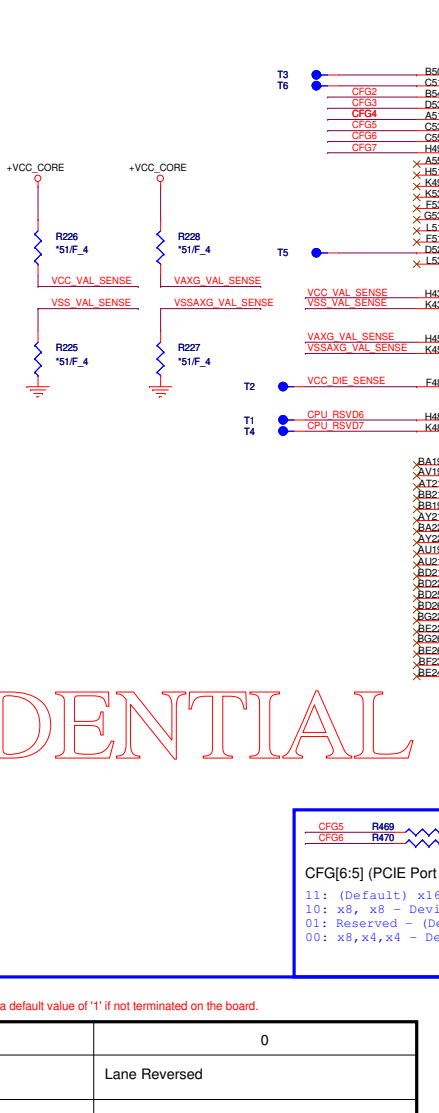
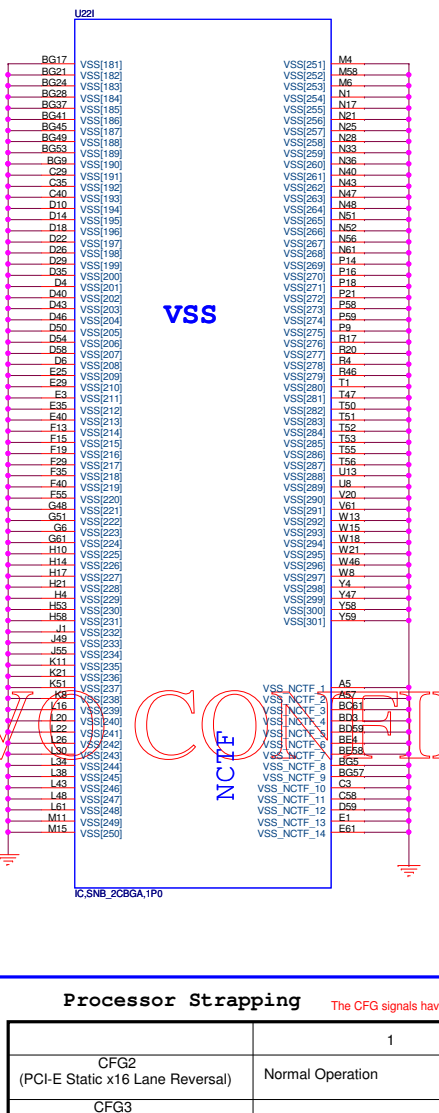
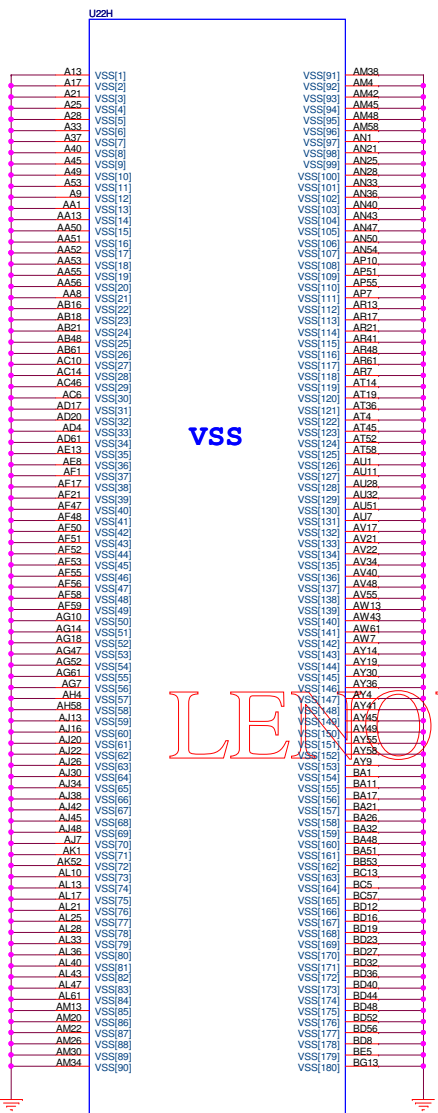


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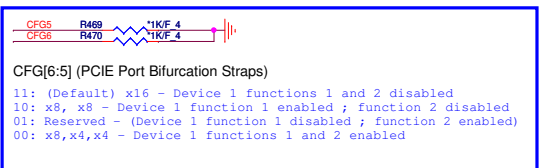
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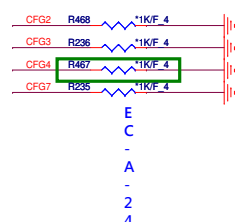
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CFG6(5) (PCIe Port Bifurcation Straps)
 11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled; function 2 enabled)
 00: x8, x4, x4 - Device 1 functions 1 and 2 enabled

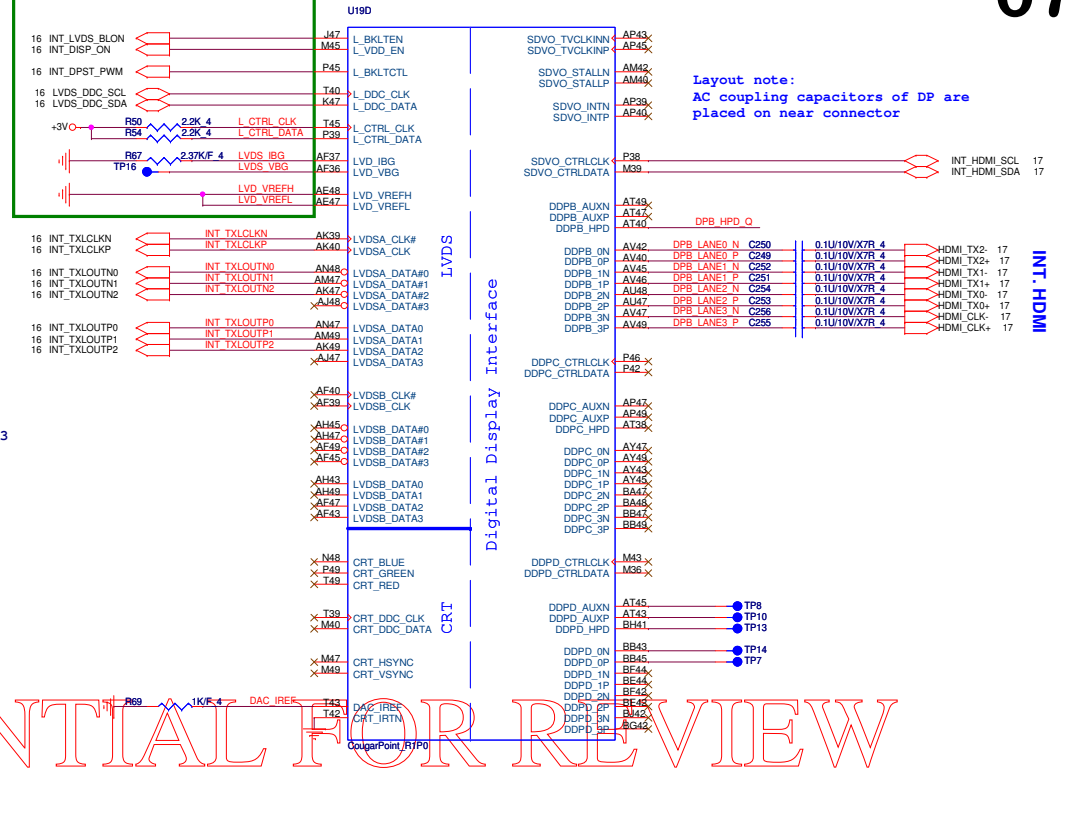
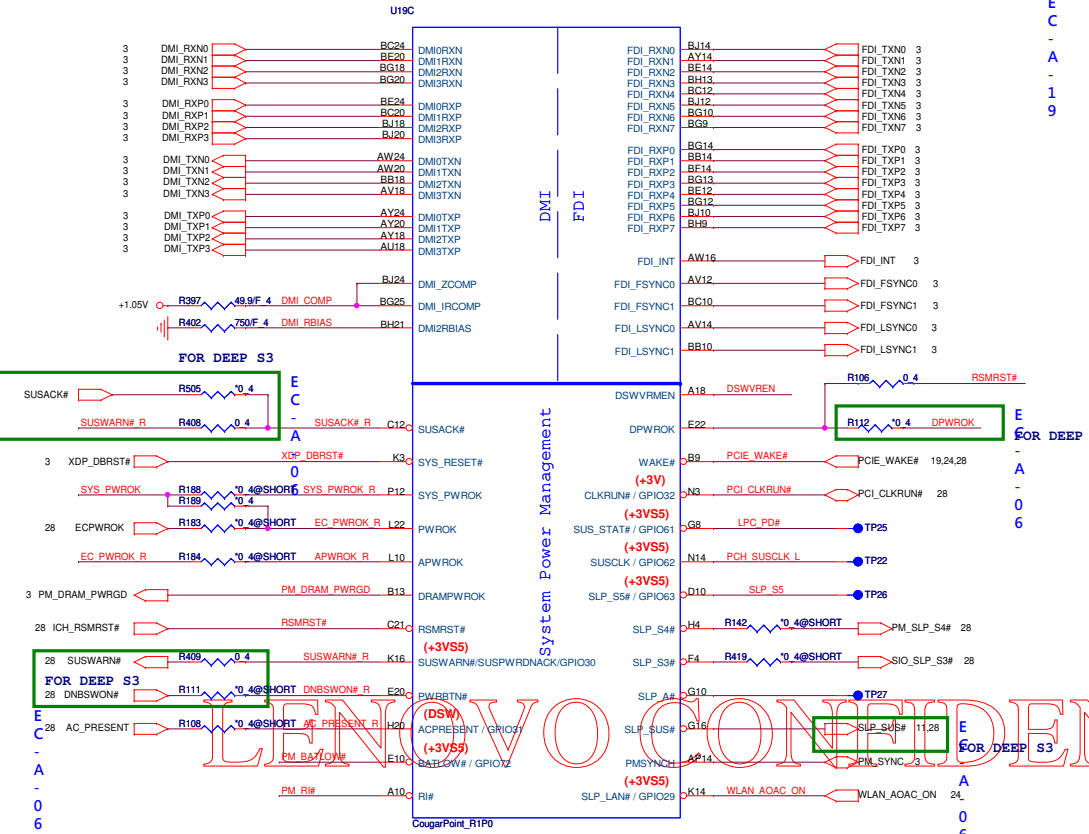
Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP



Cougar Point/Panther Point (DMI, FDI, PM)

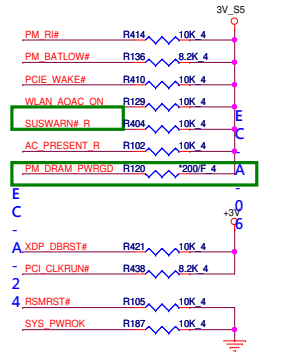
Cougar Point/Panther Point (LVDS, DDI)



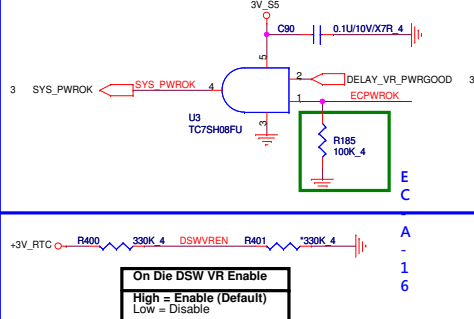
Layout note:
AC coupling capacitors of DP are placed on near connector

- +3V_DSW 8,11
- +1.05V 2,5,9,11,33,36
- +3V_RTC 8,11,28
- 3V_S5 3,8,9,10,11,18,24,29,33
- +3V 3,8,9,10,11,13,16,17,18,19,20,21,23,24,25,27,28,32,33,34,35,36,37,38,39
- +5V 8,11,17,18,20,27,33,34

PCH Pull-high/low(CLG)

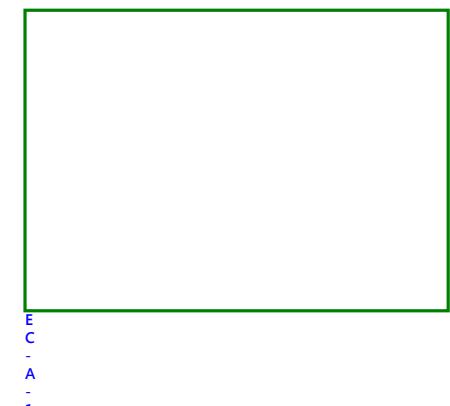
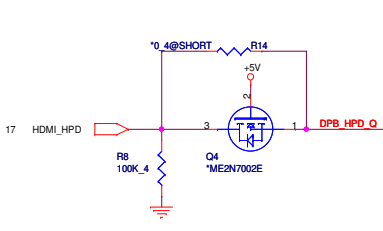


System PWR_OK(CLG)

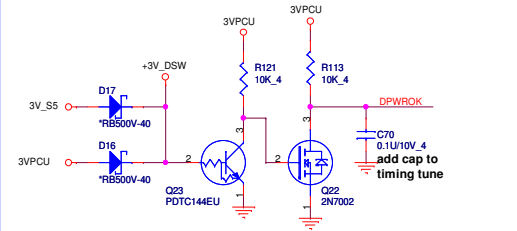


On Die DSW VR Enable
High = Enable (Default)
Low = Disable

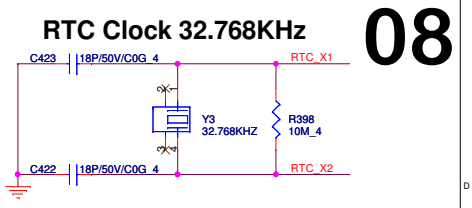
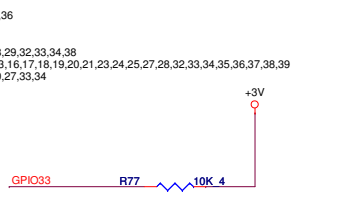
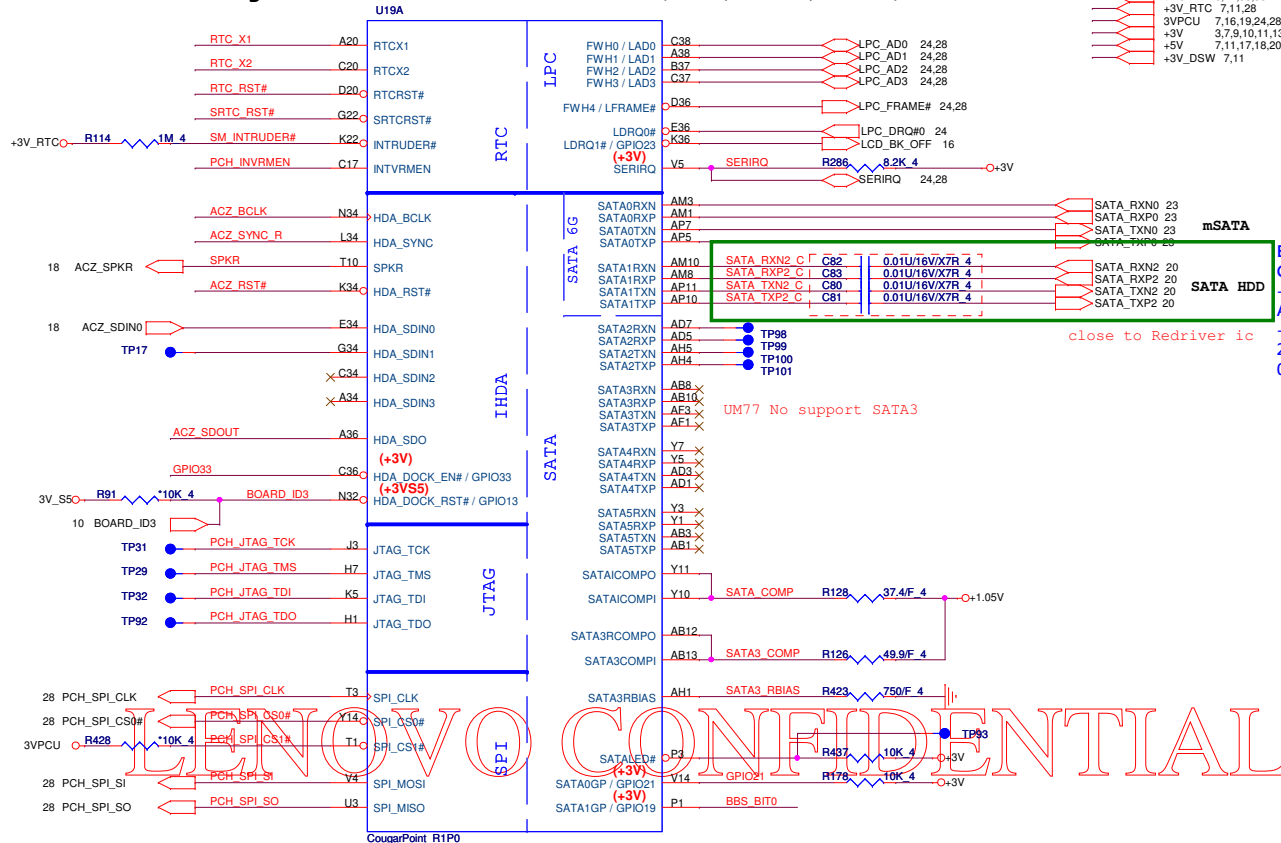
INT HDMI DETECT



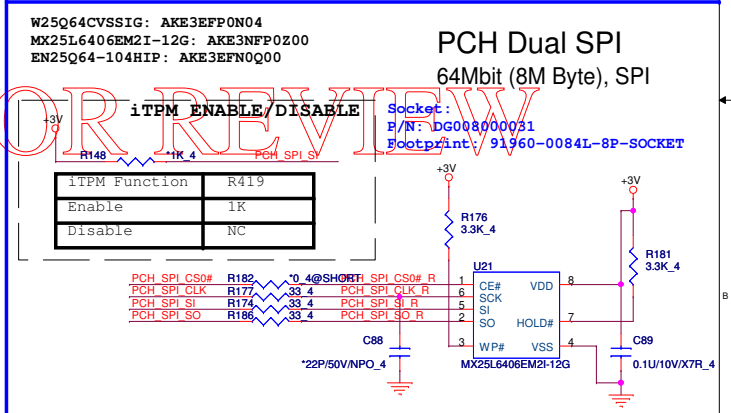
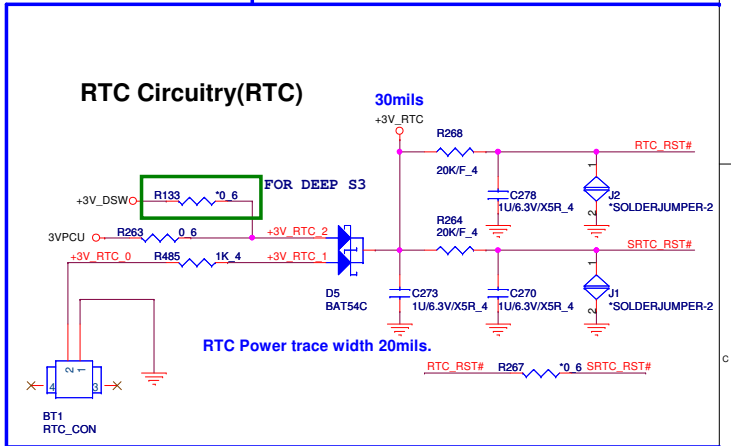
DPWROK FOR DSW (DEEP S3)



Cougar Point/Panther Point (HDA, JTAG, SATA)



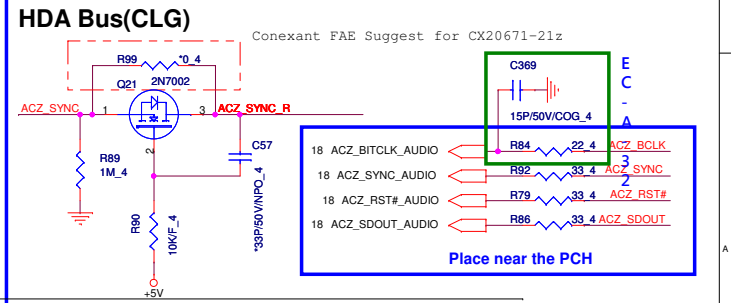
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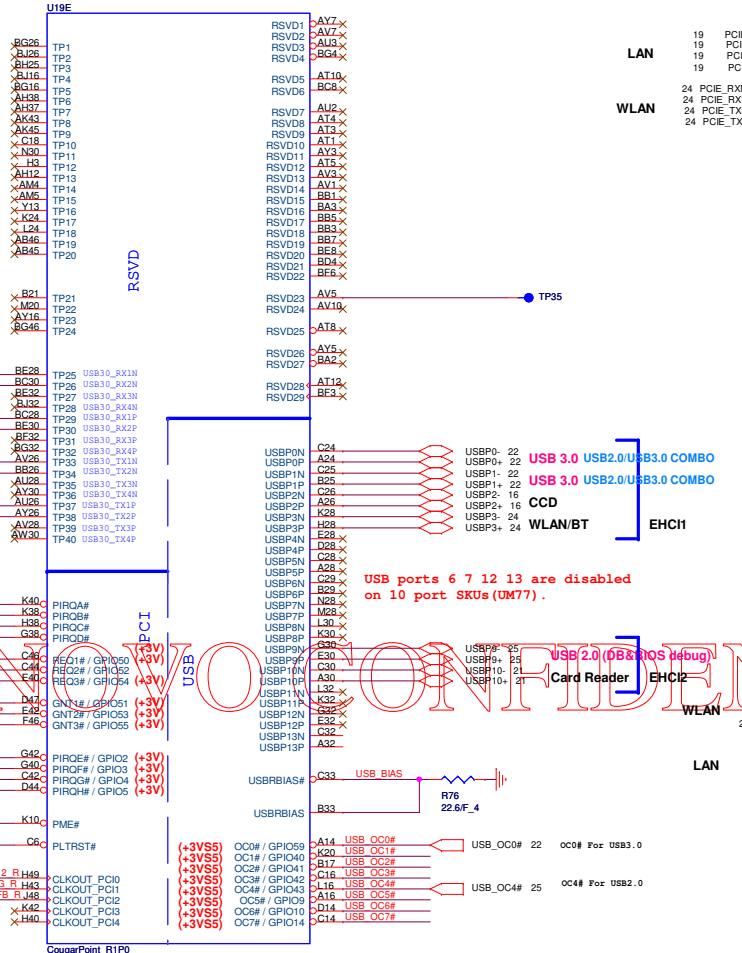
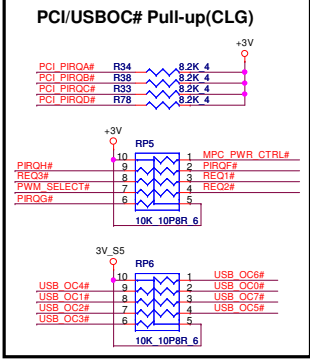
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit									
SPKR	Different from Calpella	No reboot mode setting	PWROK 0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode										
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)										
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up										
HDA_SDO	Flash Descriptor Security Only for Interposer	PWROK	0 = effective(Default: weak pull down) 1 = Override										
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>GNT1#</th> <th>GNT0#</th> <th>Boot Location</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>SPI</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </tbody> </table>	GNT1#	GNT0#	Boot Location	1	0	SPI	0	0	LPC	
GNT1#	GNT0#	Boot Location											
1	0	SPI											
0	0	LPC											
GPIO19	Different from Calpella	PWROK	0 = effective(Default: weak pull down) 1 = Override										
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN									
DF_TVS	DMI Termination voltage IVY:0 SANDY:1	PWROK	weak pull-down 20kohm										
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V										
GPIO15	Intel ME Crypto Transport Layer Security cipher suite		Low = Disable (Default) High = Enable										
GPIO28	Different from Calpella	On-die PLL Voltage Regulator	0 = Disable 1 = Enable (Default)										
DSWVREN		0: disable 1: enable											

if default boot destination is SPI, no external pull-up/-down resistors on the board are necessary

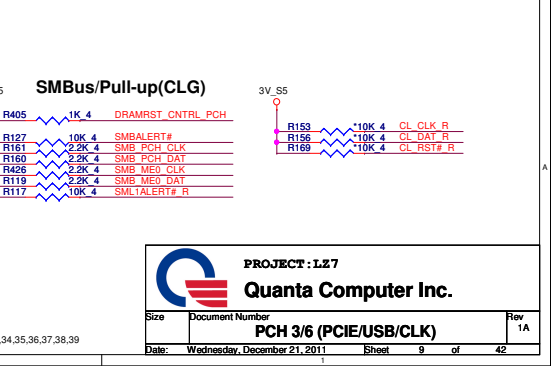
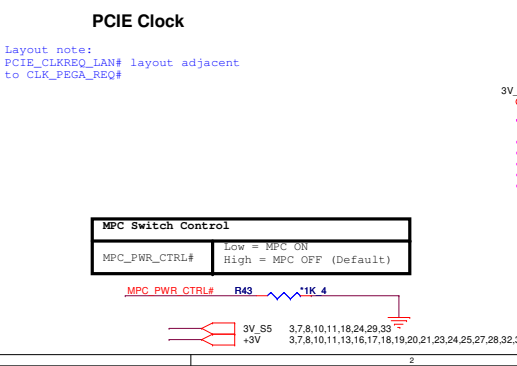
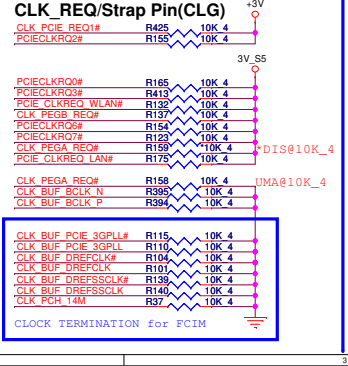
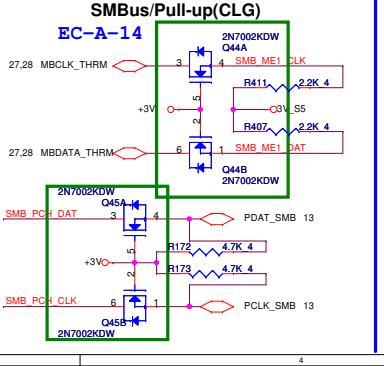
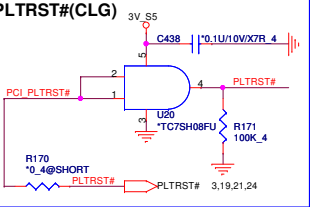
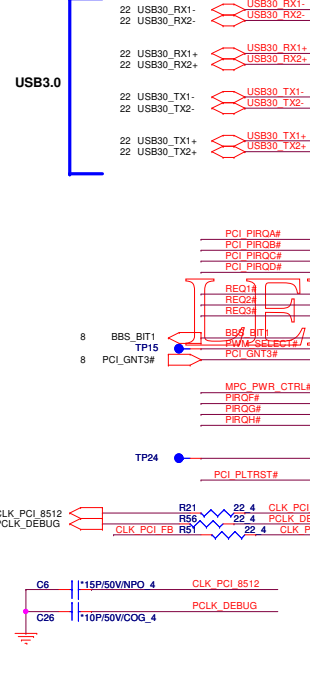
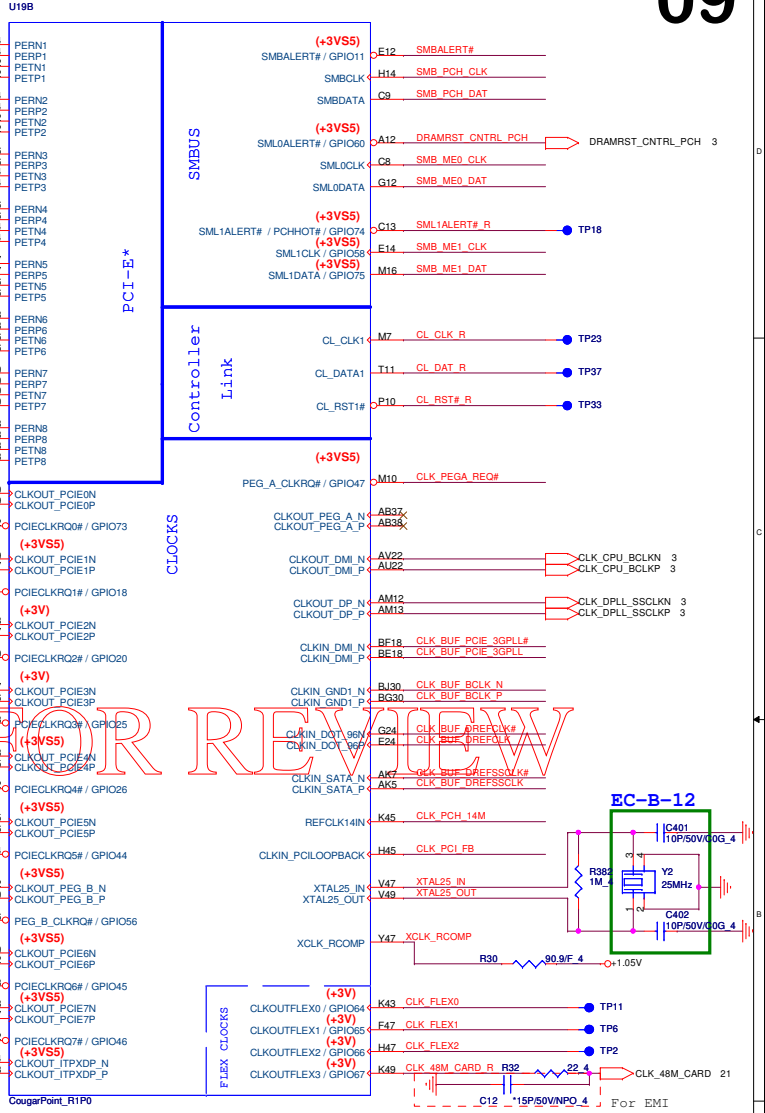


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PCH 2/6 (SATA/HDA/SPI)
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PCIe ports 4 5 6 7 are disabled on 10 port SKUs (UM77).

USB ports 6 7 12 13 are disabled on 10 port SKUs (UM77).

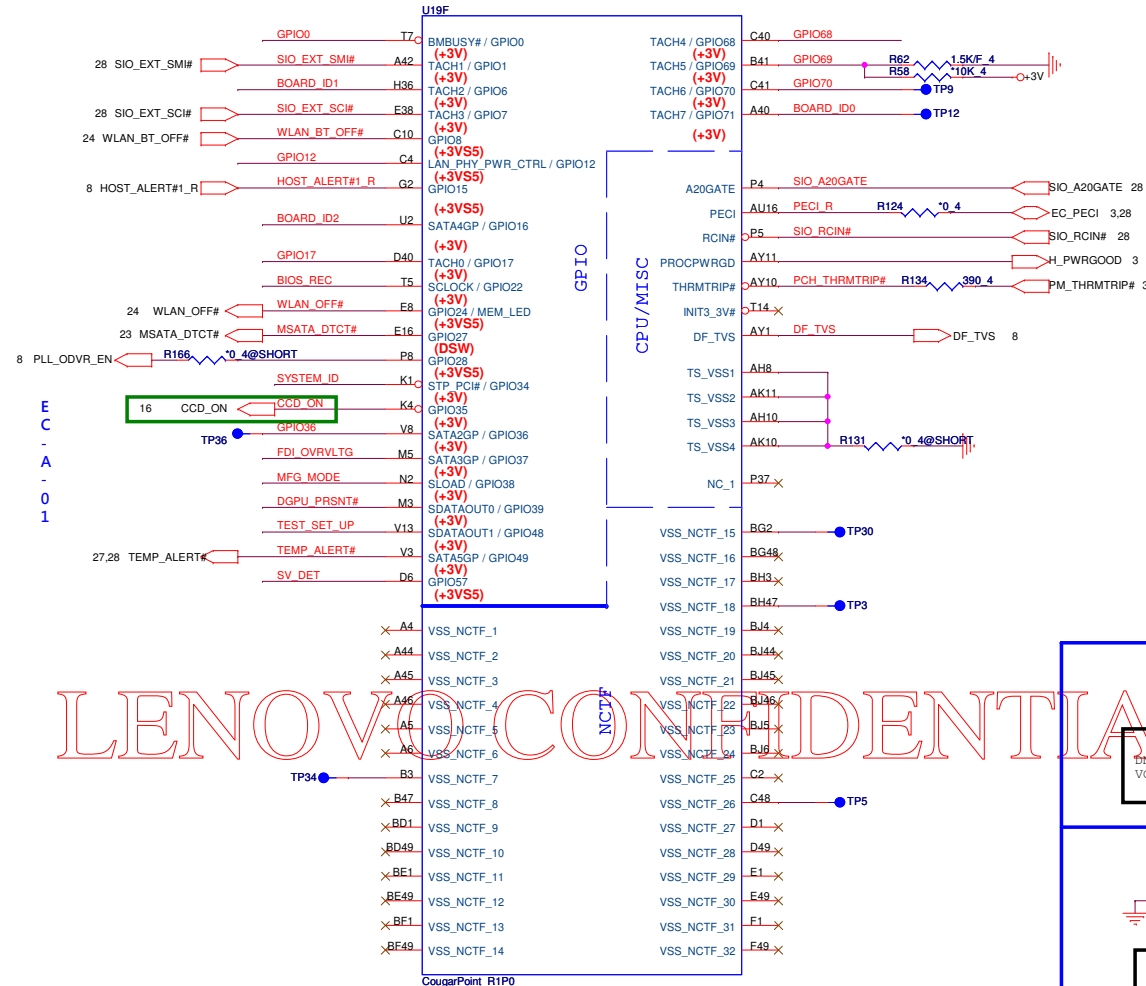


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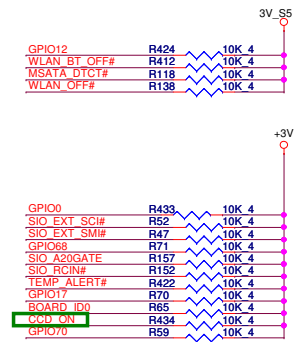
Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)

3V_S5 3.7,8,9,11,18,24,29,33
+3V 3.7,8,9,11,13,16,17,18,19,20,21,23,24,25,27,28,32,33,34,35,36,37,38,39

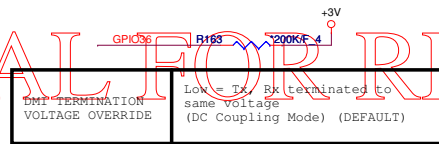
10



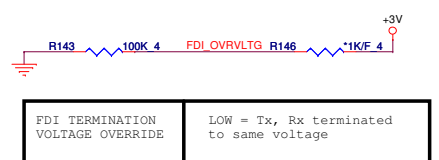
GPIO Pull-up/Pull-down(CLG)



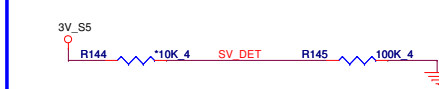
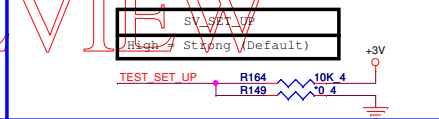
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DMI TERMINATION VOLTAGE OVERRIDE
Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)



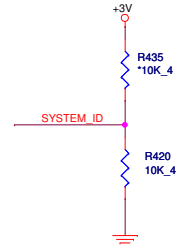
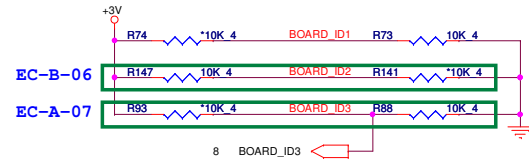
FDI TERMINATION VOLTAGE OVERRIDE
LOW = Tx, Rx terminated to same voltage



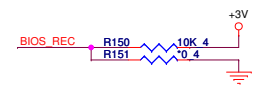
BOARD ID SETTING

Board ID For Function	ID1 GPIO6	ID2 GPIO16	ID3 GPIO13
SDV			
SIV			
SVI	0	1	0
SOVP			

	SYSTEM_ID
L27	0
L28	1

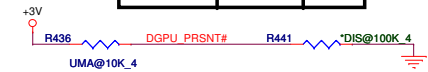


MFG-TEST



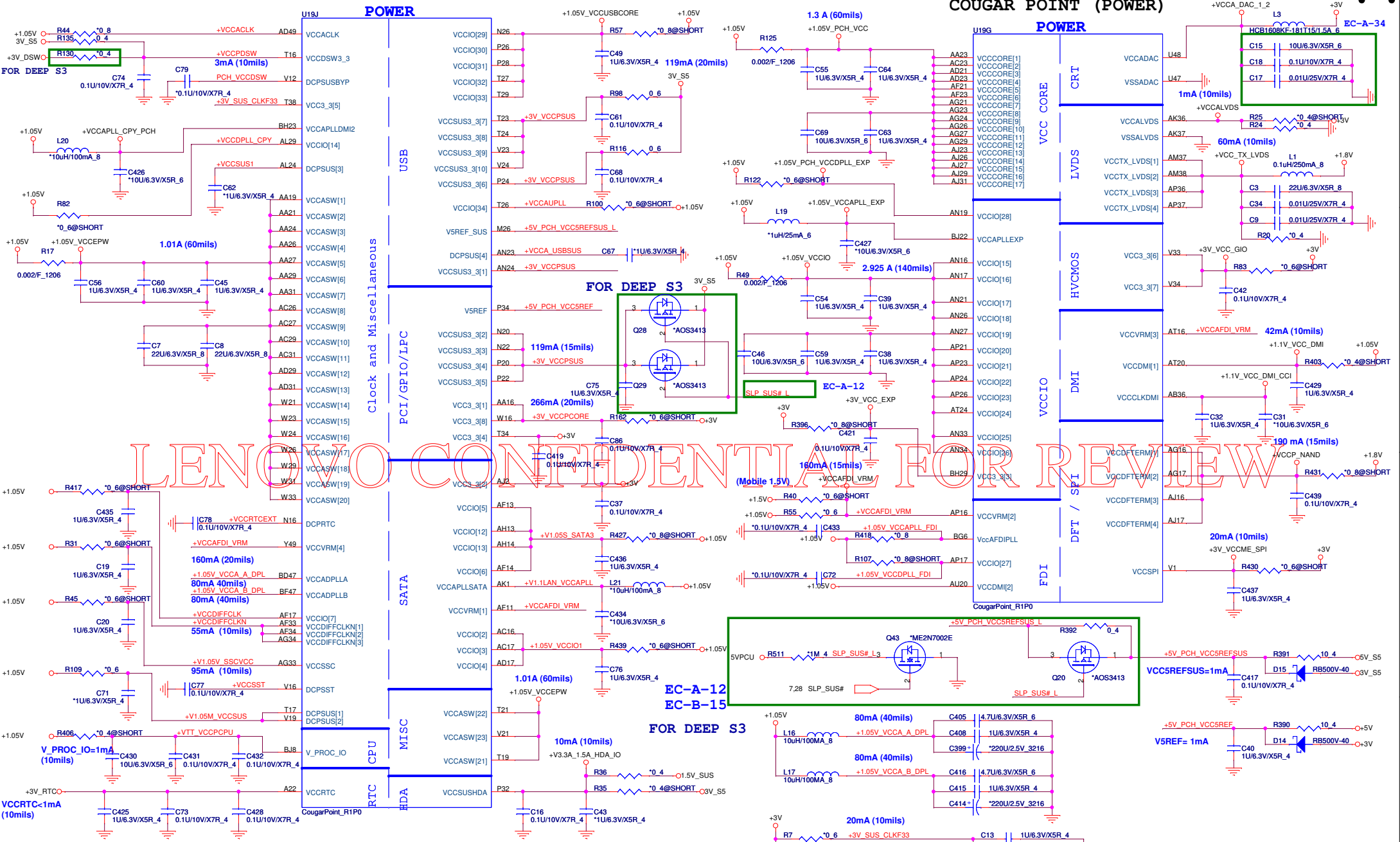
BIOS RECOVERY
High = Disable (Default)
Low = Enable

	Optimus	UMA
Stuff	R1566	R1565
No Stuff	R1565	R1566



PROJECT: L27
Quanta Computer Inc.

Cougar Point/Panther Point (POWER)

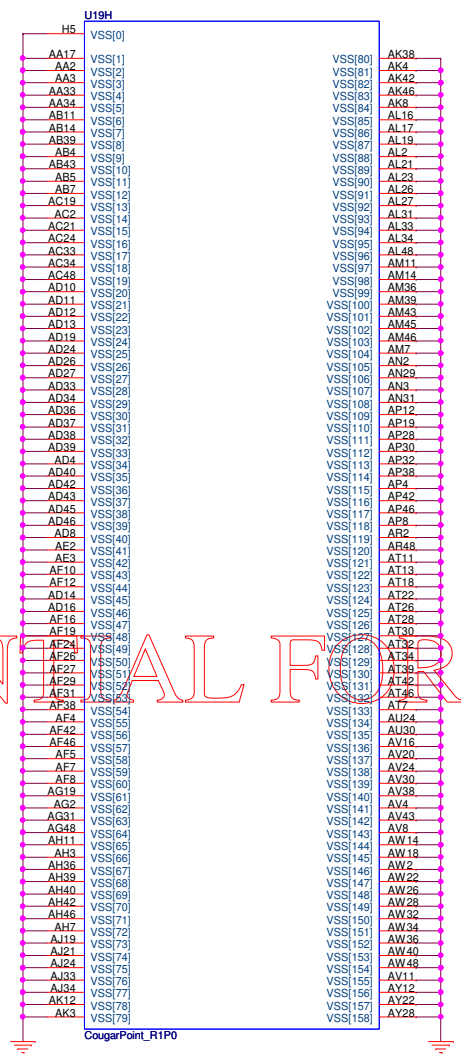
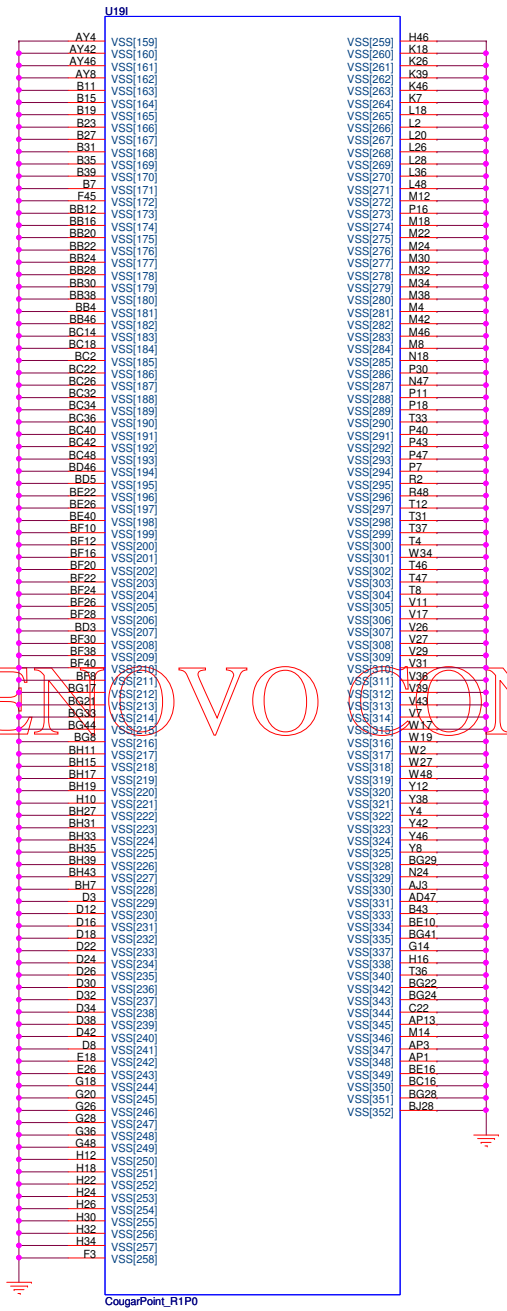


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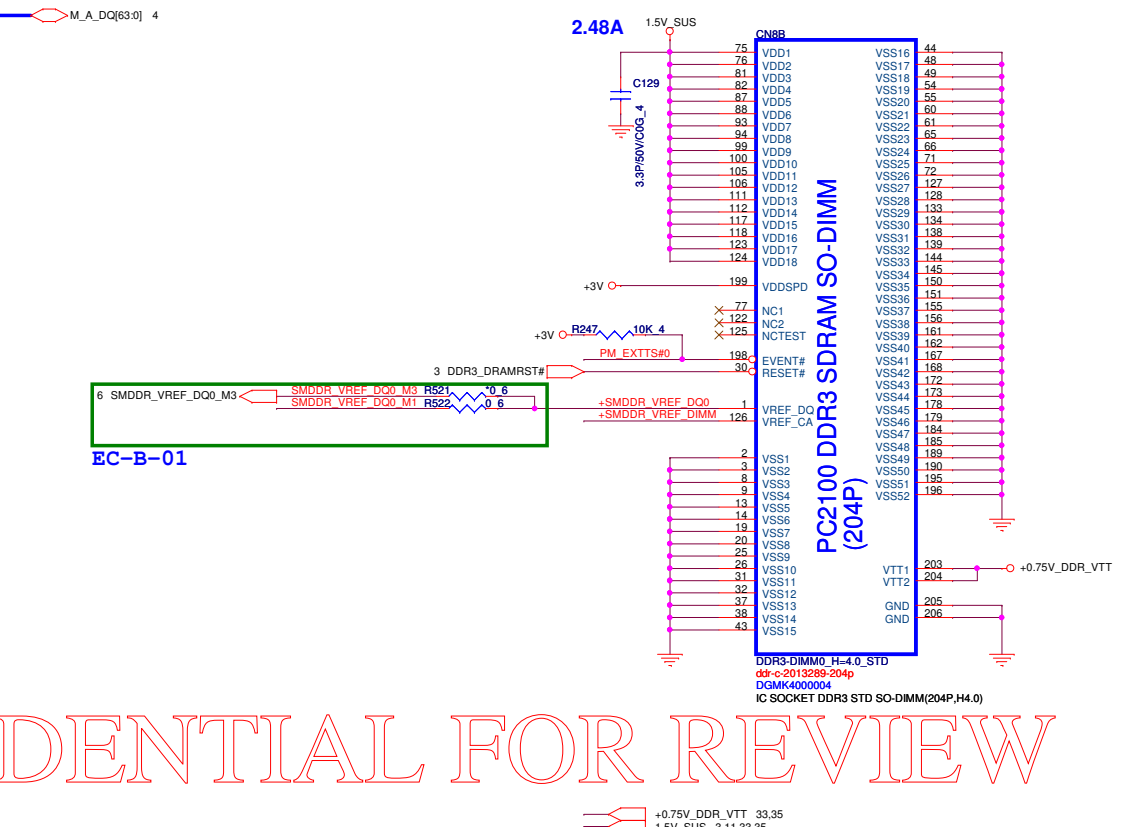
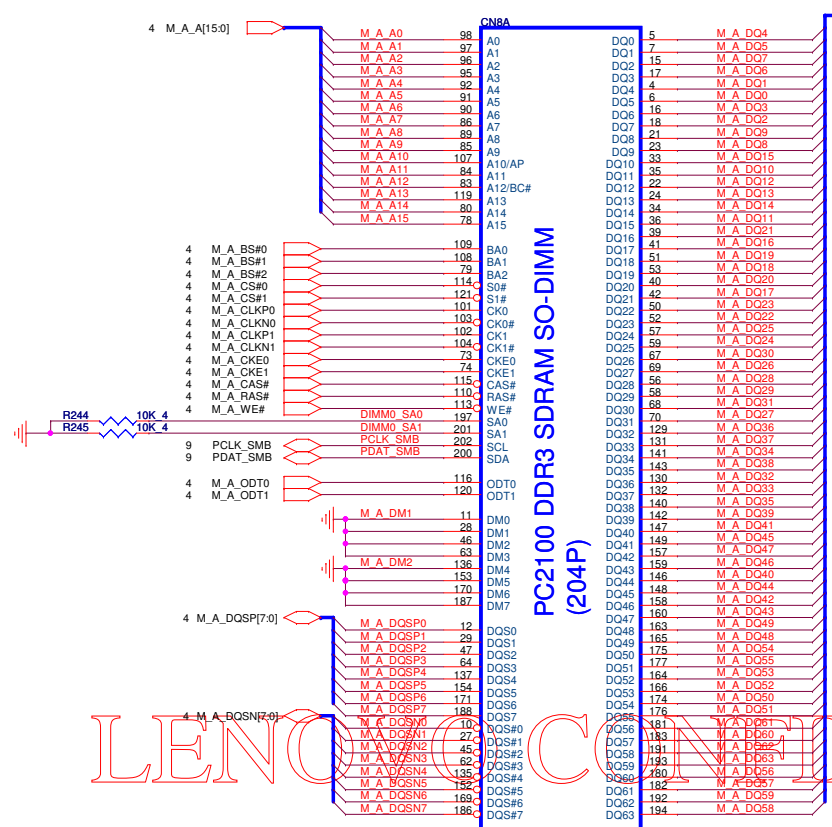
+3V_RTC	7,8,28
3V_S5	3,7,8,9,10,18,24,29,33
+3V	3,7,8,9,10,13,16,17,18,19,20,21,23,24,25,27,28,32,33,34,35,36,37,38,39
5V_S5	22,25,33
+5V	7,8,17,18,20,27,33,34
+1.05V	3,5,7,8,9,33,36
1.5V_SUS	3,13,33,35
+1.8V	5,8,33,38
+3V_DSVO	7,8

Cougar Point/Panther Point (GND)

Cougar Point/Panther Point (GND)



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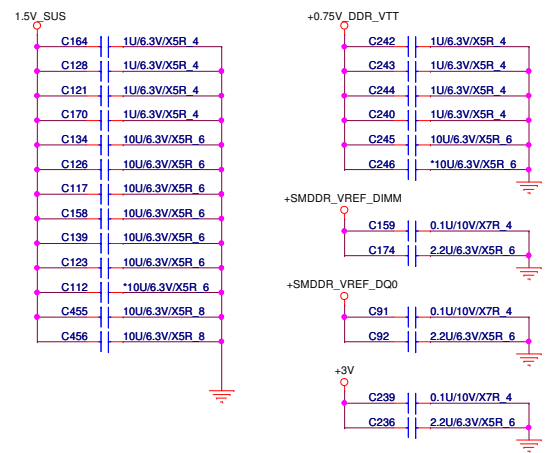


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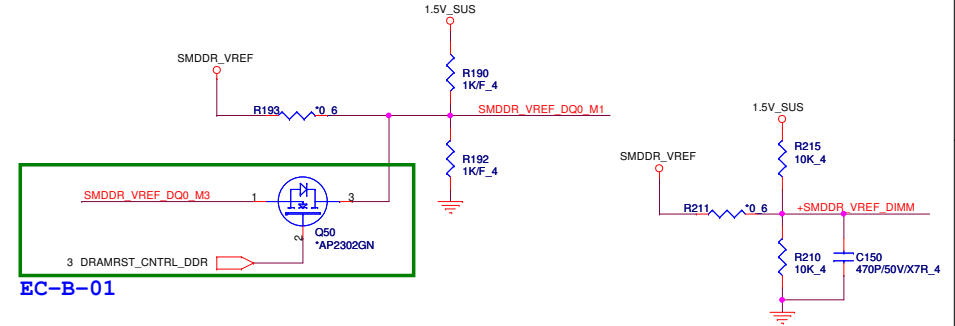
DDR3-DIMM0_H=4.0_STD
 ddr-c-2013289-204p
 DGMK4000004
 IC SOCKET DDR3 SODIMM(204P,H4.0,STD)

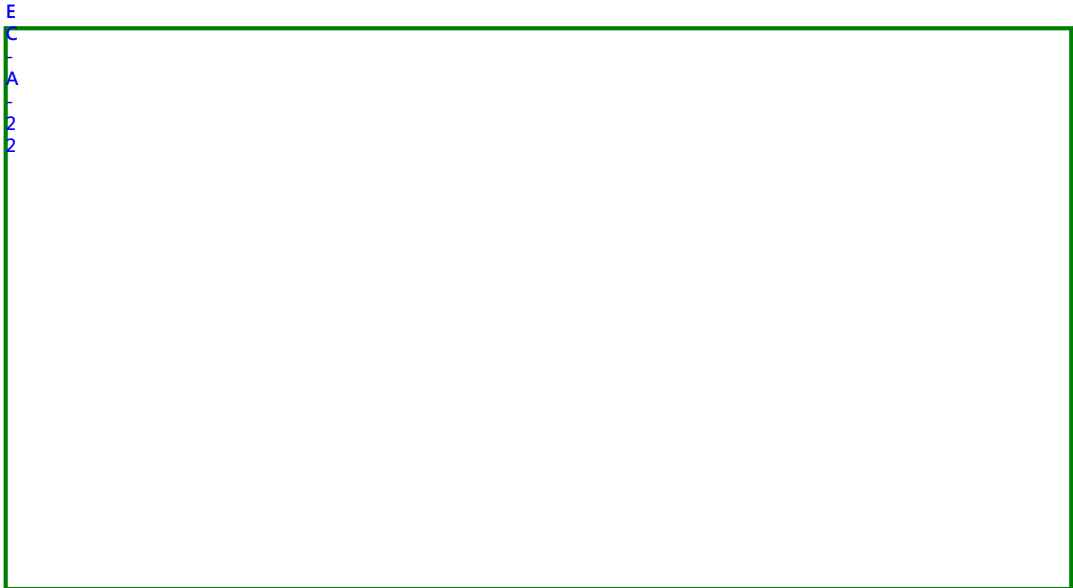
+0.75V_DDR_VTT 33.35
 1.5V_SUS 3.11,33,35
 +3V 3.7,8,9,10,11,16,17,18,19,20,21,23,24,25,27,28,32,33,34,35,36,37,38,39
 SMDDR_VREF 5.35

Place these Caps near So-Dimm0.



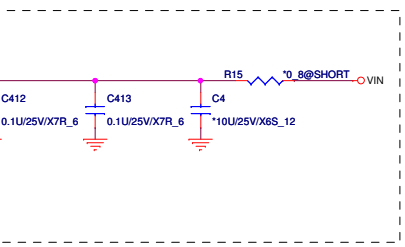
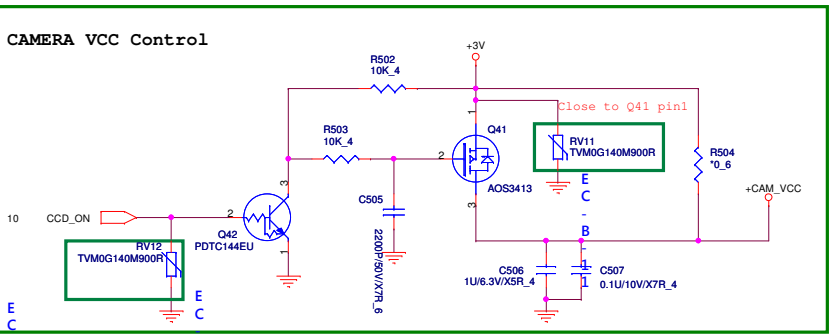
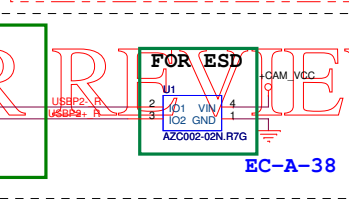
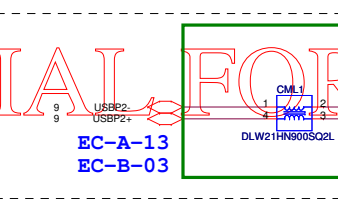
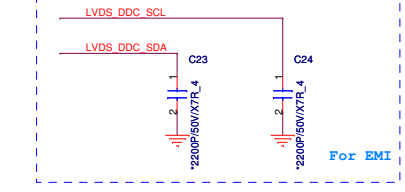
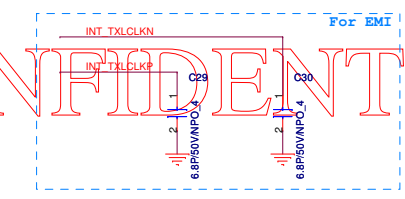
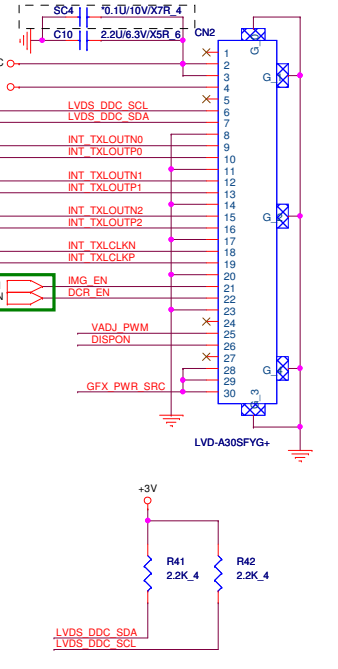
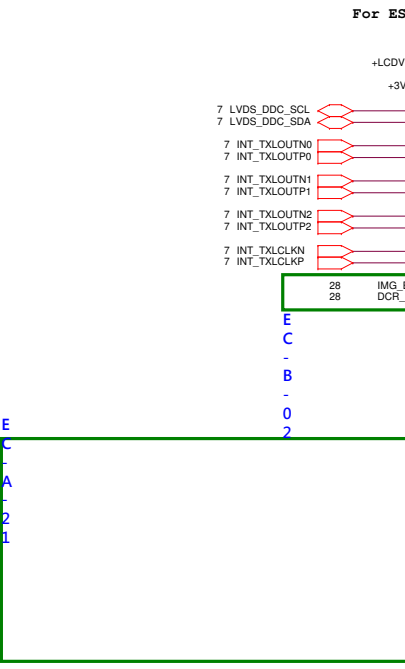
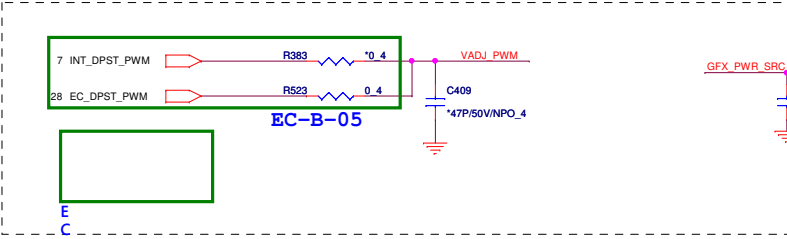
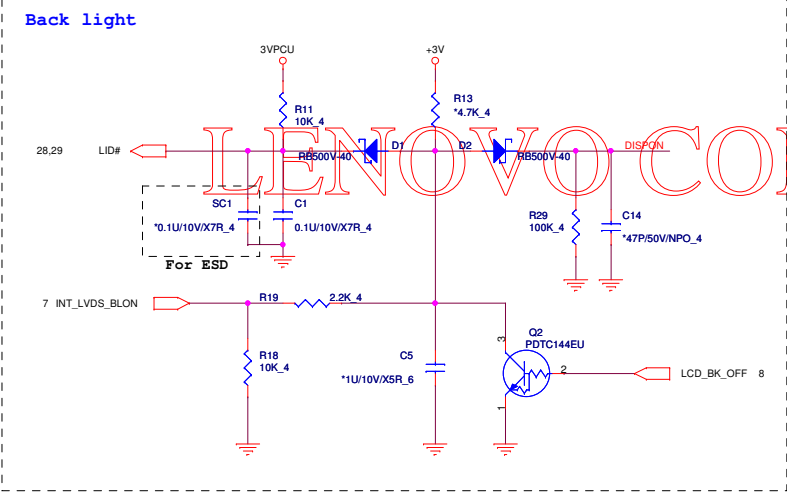
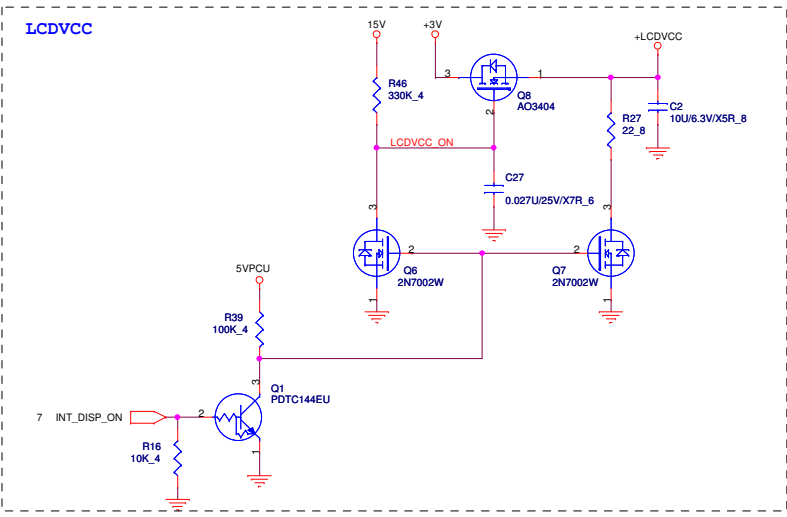
VREF DQ0 M1 Solution





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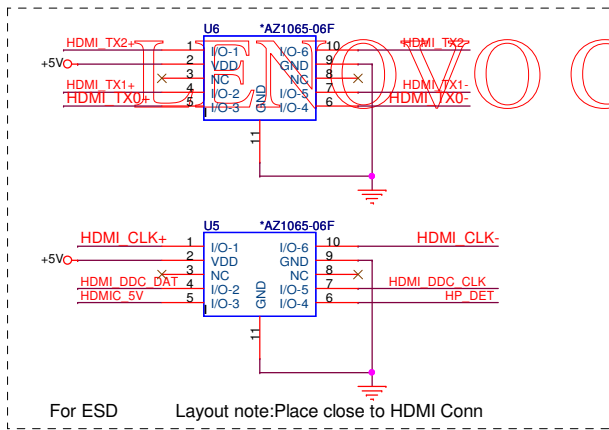
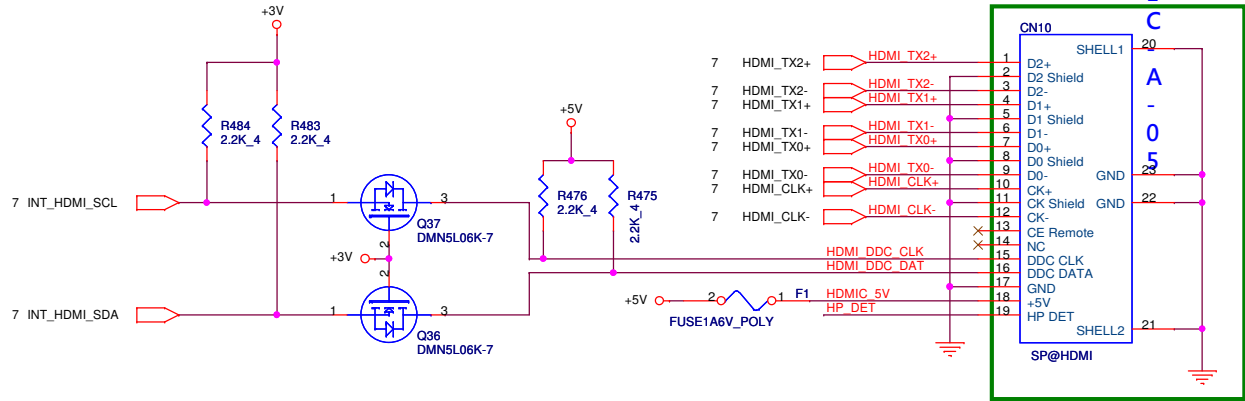
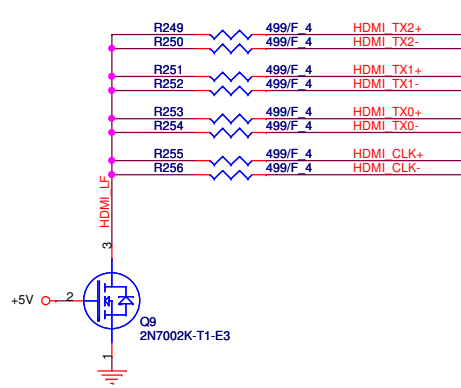
+3V	3,7,8,9,10,11,13,17,18,19,20,21,23,24,25,27,28,32,33,34,35,36,37,38,39
3VPCU	7,8,19,24,28,29,32,33,34,38
15V	32,33,35
+5V	7,8,11,17,18,20,27,33,34
VIN	32,34,35,36,37,39
5VPCU	32,33,35,36,37,38,39



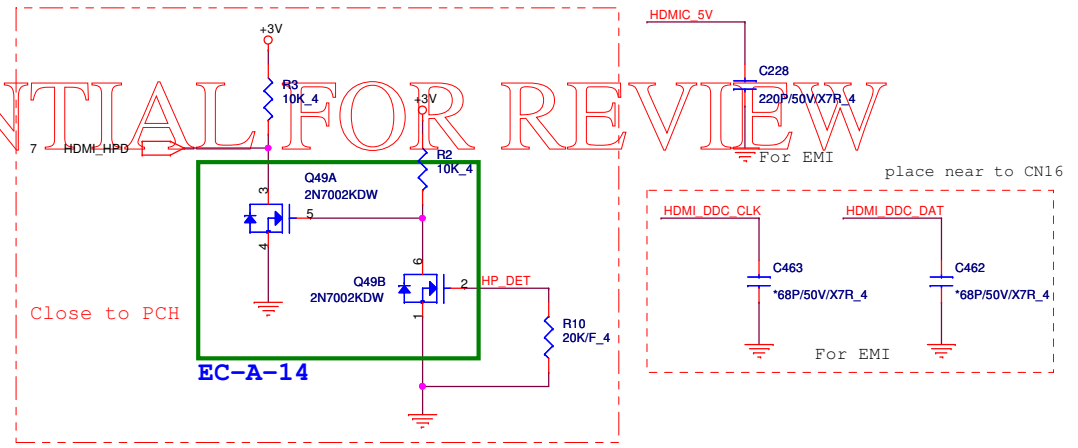
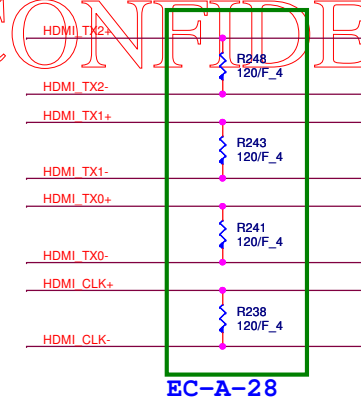
PROJECT : LZ7		
Quanta Computer Inc.		
Size	Document Number	Rev
	LCD/CAMERA	1A
Date:	Wednesday, December 21, 2011	Sheet 16 of 42

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EMI reserve for HDMI

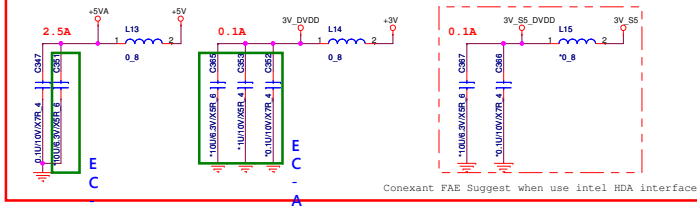
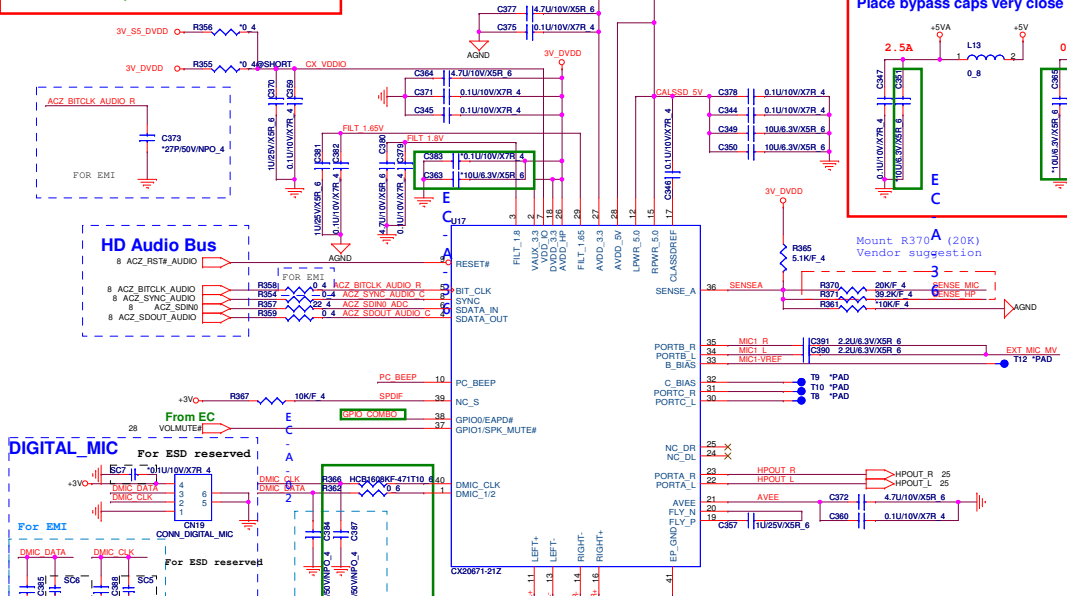


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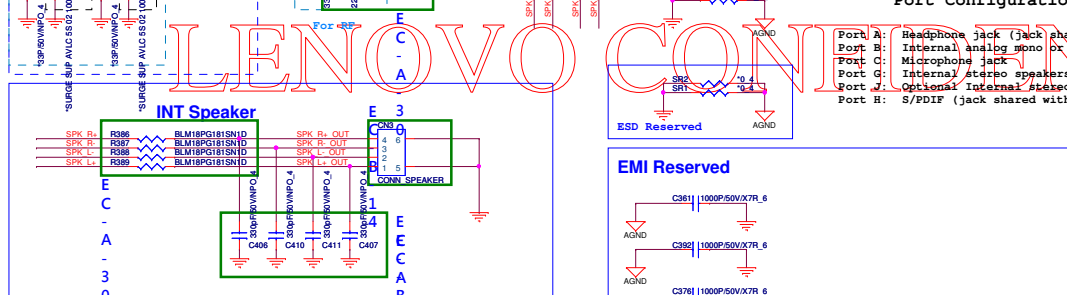
Note: To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX_3.3 pins must be powered by a rail that is not removed unless AC power is removed.

AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms). Place bypass caps very close to device.

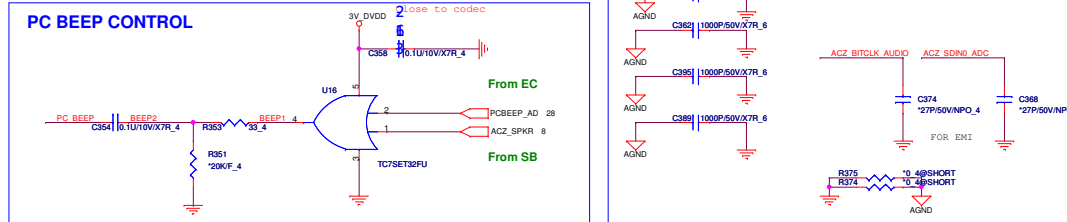
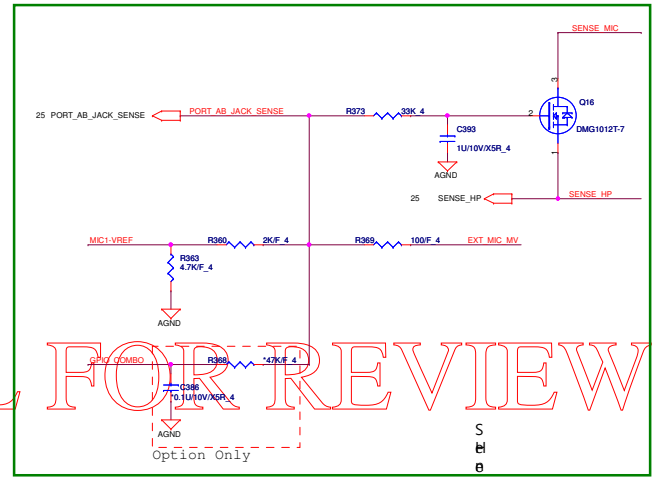


Conexant FAE Suggest when use intel HDA interface



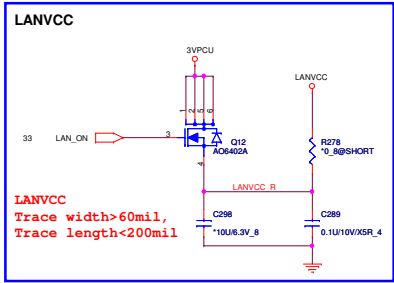
Port Configuration

- Port A: Headphone jack (jack shared with S/PDIF)
Port B: Internal analog mono or stereo MIC.
Port C: Microphone jack
Port D: Internal stereo speakers
Port E: Optional internal headset digital mic
Port H: S/PDIF (jack shared with headphone)

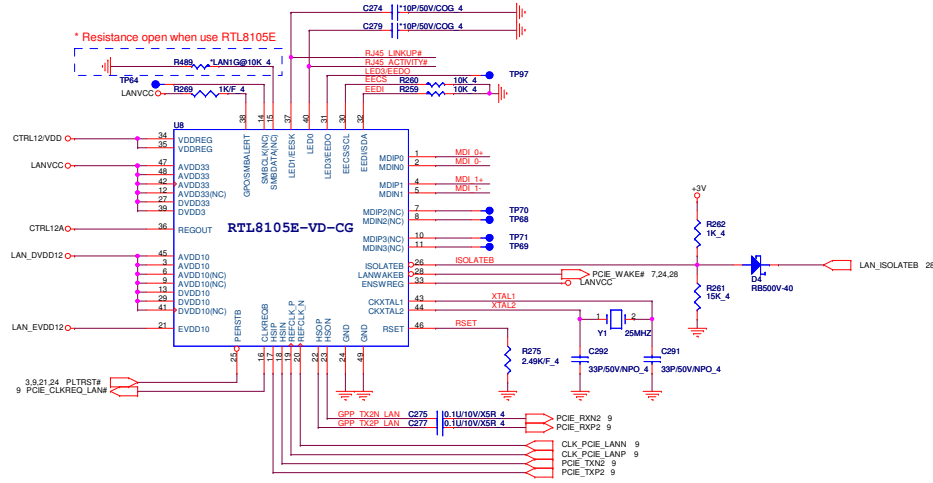


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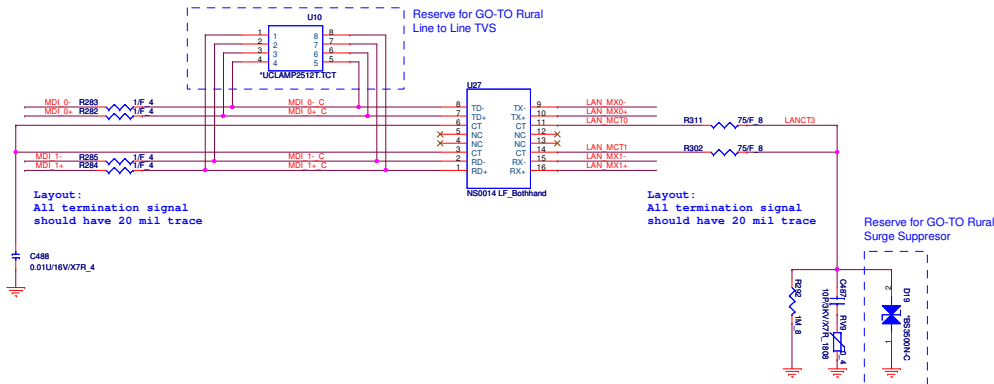
S
H
B
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h
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M
b
G
I
C
o
m
b
o



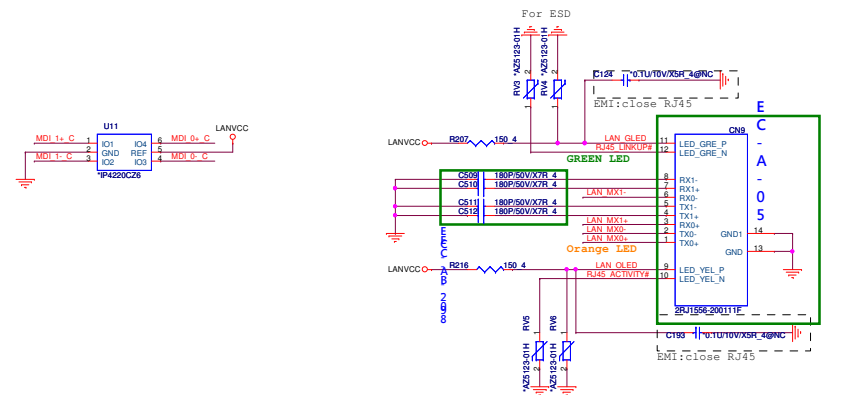
7,8,16,24,28,29,32,33,34,38 3VPCU
33 LANVCC
3V



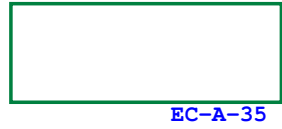
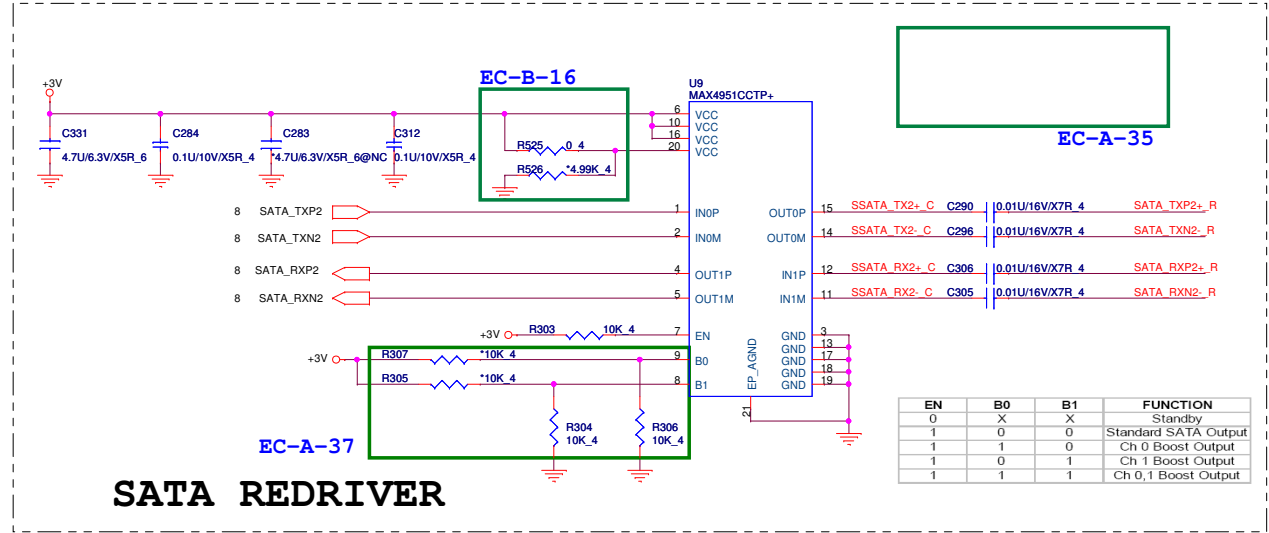
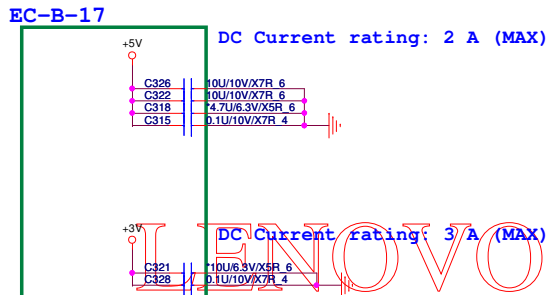
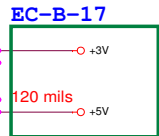
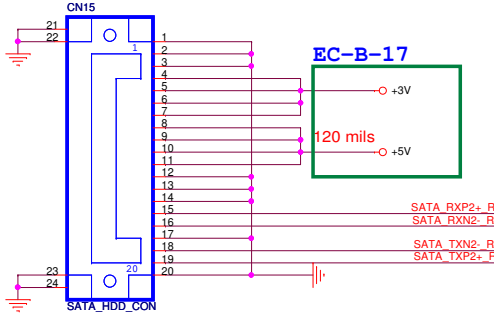
Transformer



RJ45 Connector



3,7,8,9,10,11,13,16,17,18,19,21,23,24,25,27,28,32,33,34,35,36,37,38,39
7,8,11,17,18,27,33,34

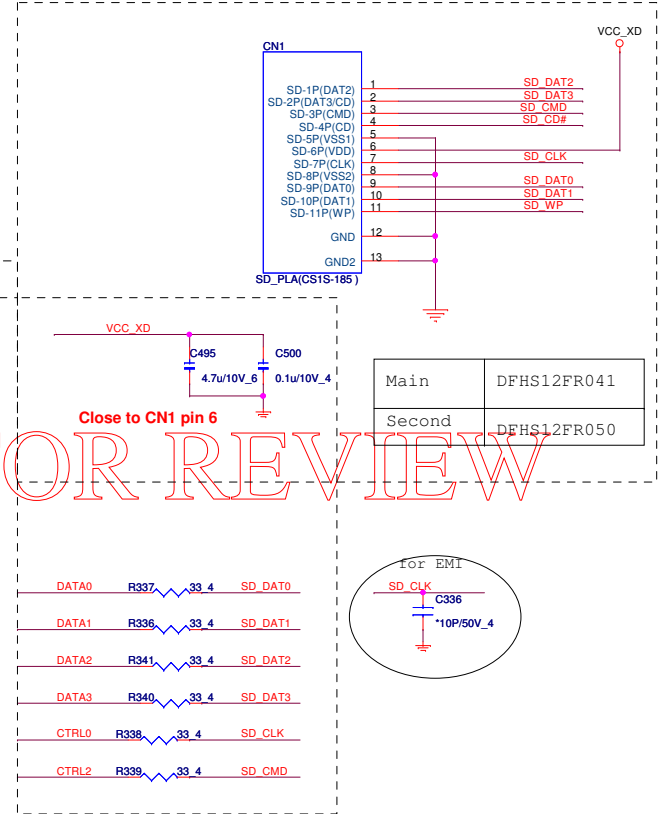
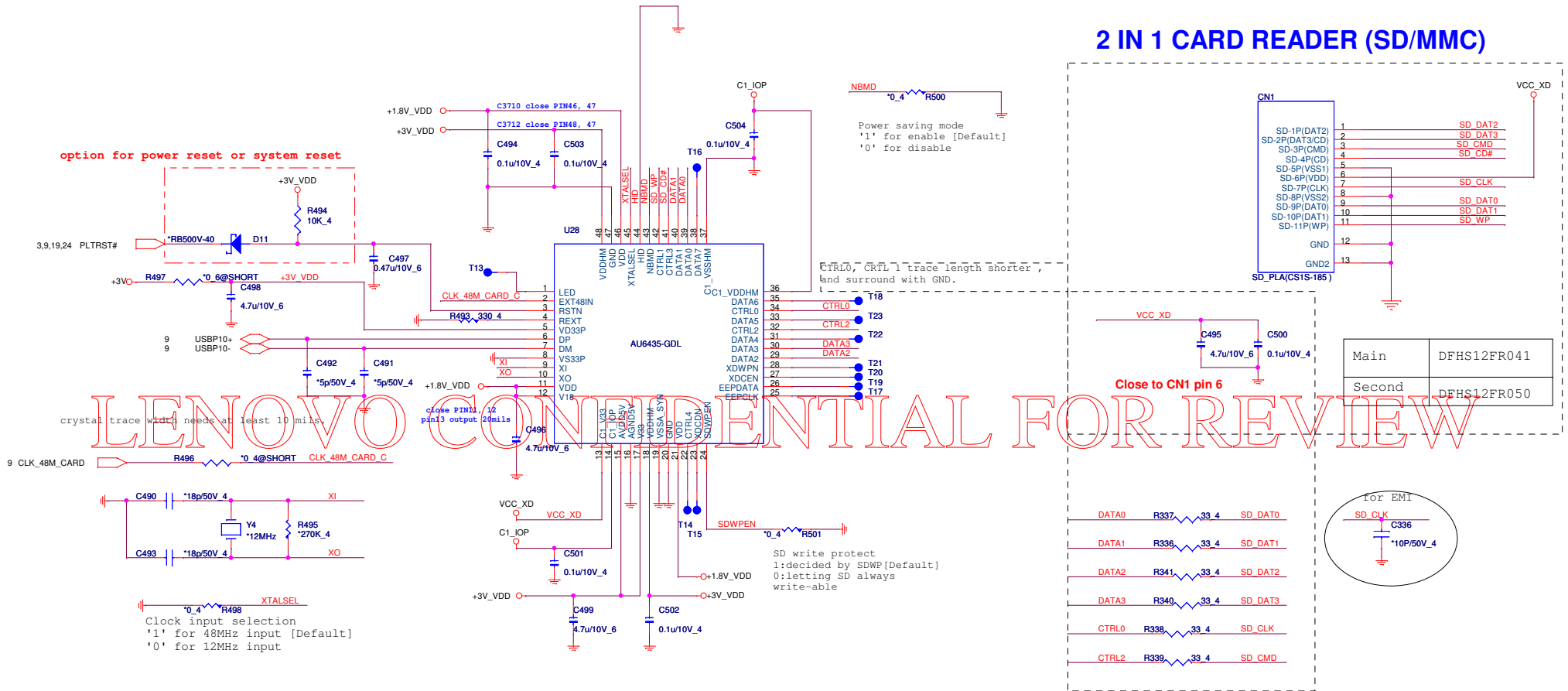


EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0,1 Boost Output

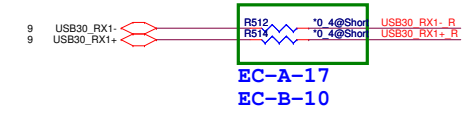
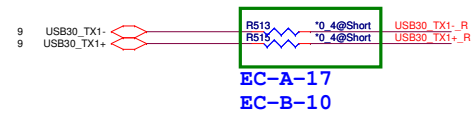
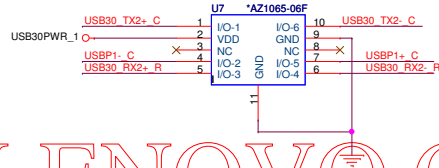
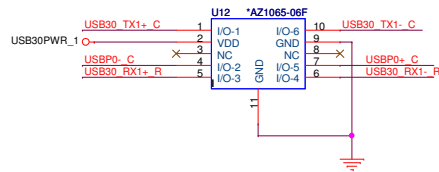
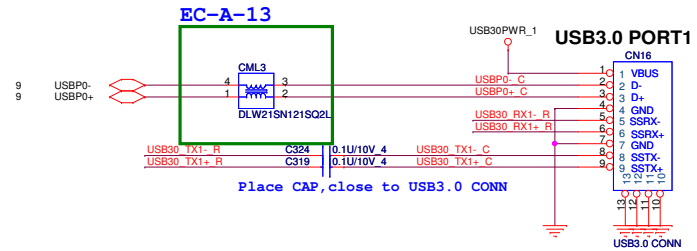
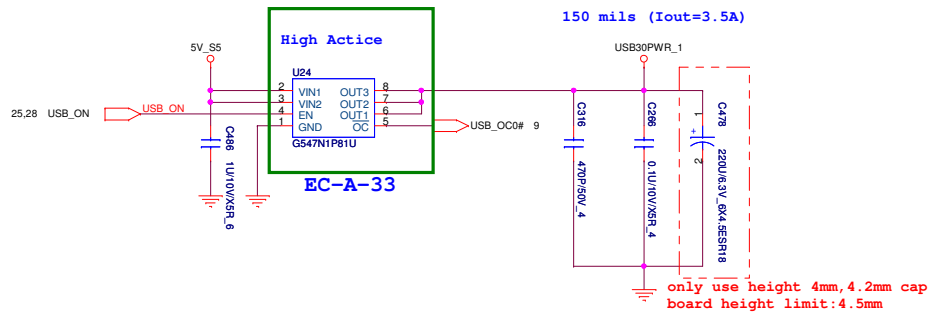
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 Quanta Computer Inc.
 Size: Document Number: SATA
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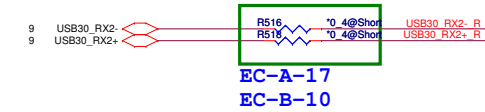
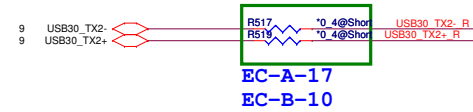
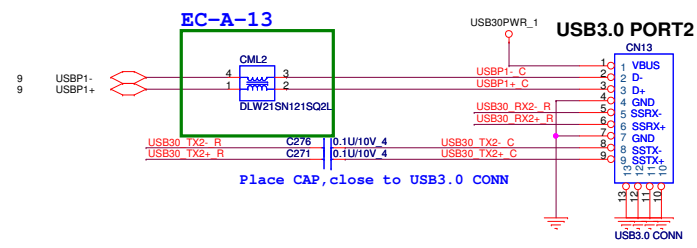
2 IN 1 CARD READER (SD/MMC)



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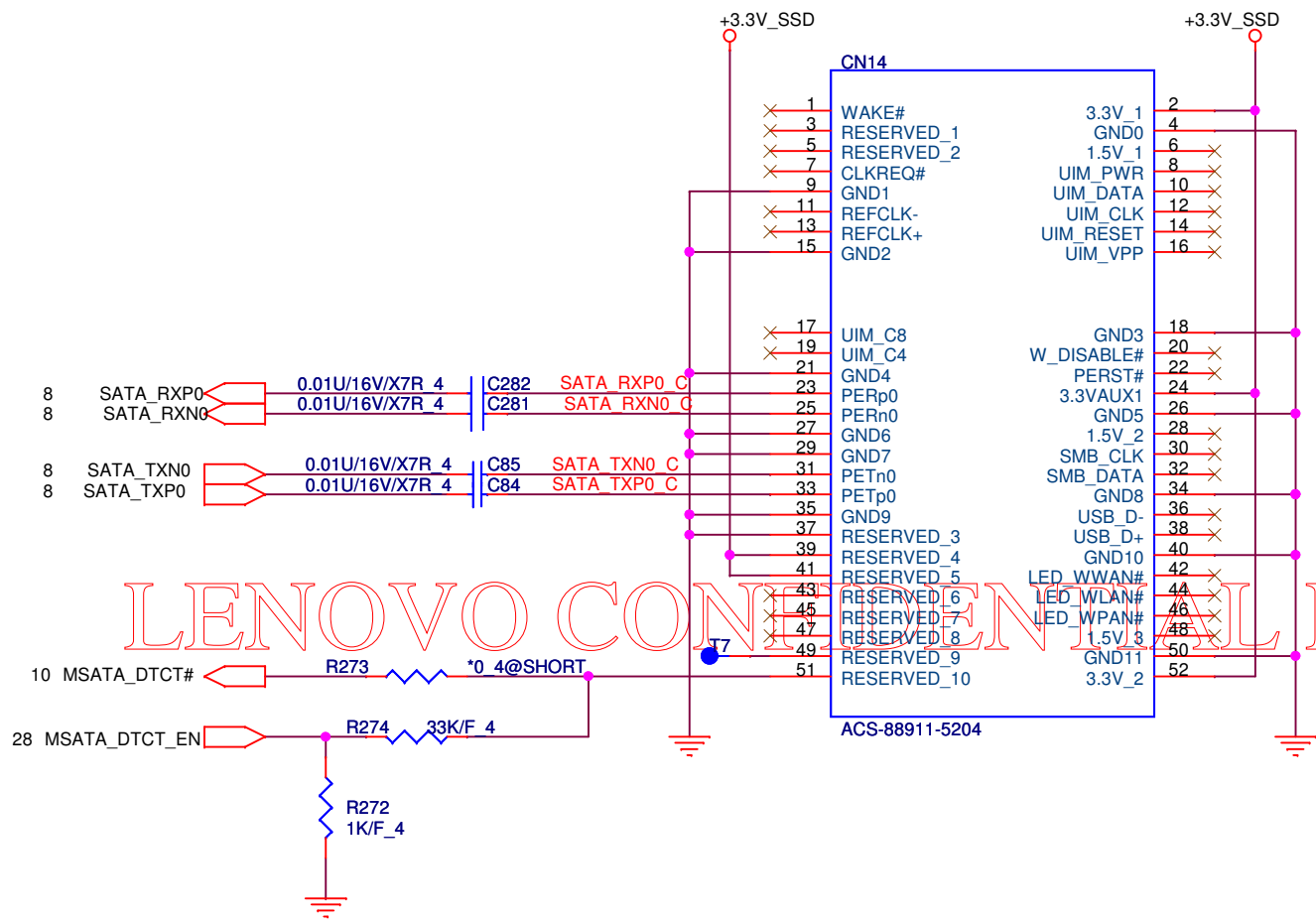


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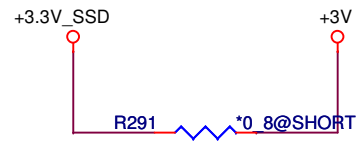
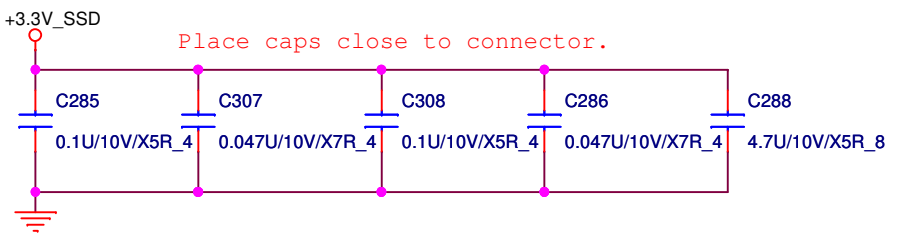


Mini PCI-E Card SSD

3,7,8,9,10,11,13,16,17,18,19,20,21,24,25,27,28,32,33,34,35,36,37,38,39
11,24,35



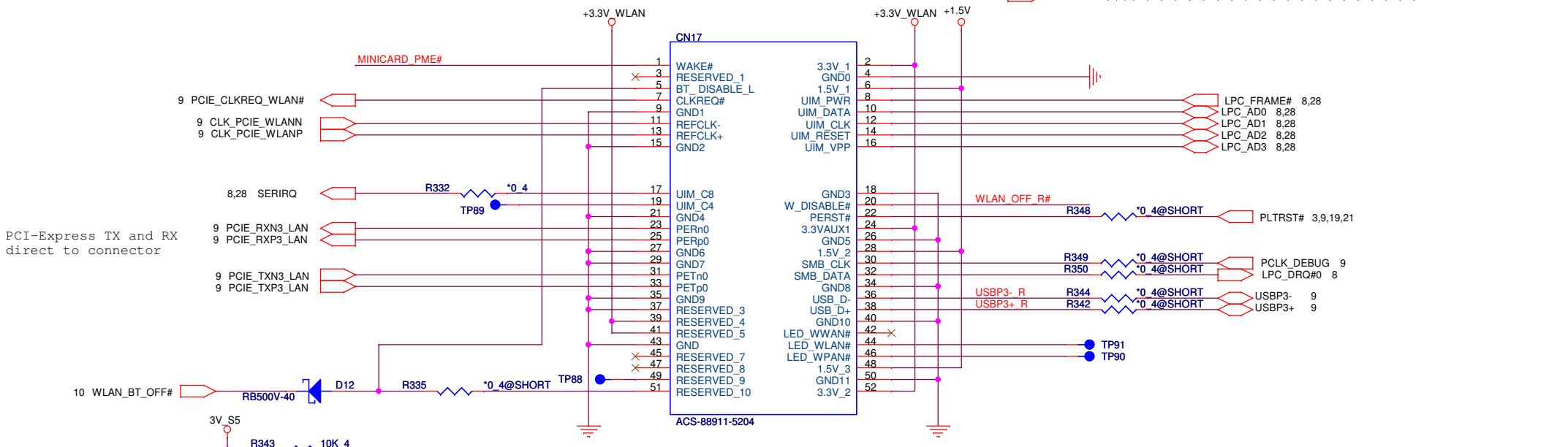
LENOVO CONFIDENTIAL FOR REVIEW



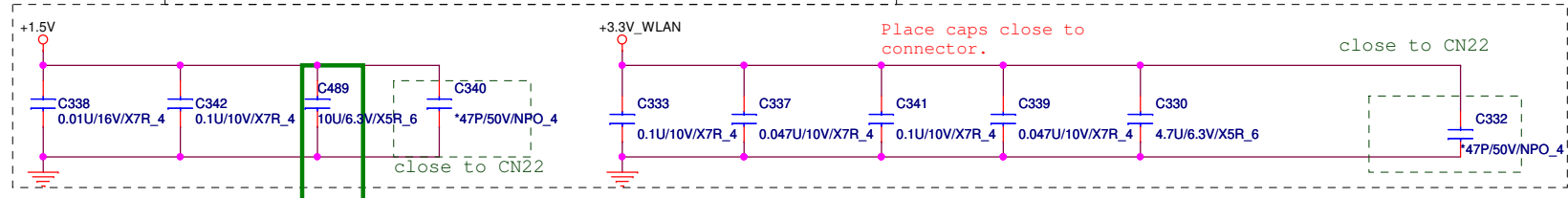
		PROJECT : LZ7	
		Quanta Computer Inc.	
Size Custom	Document Number	MINI Card (SSD)	
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			Rev 1E

MiniCard WLAN connector

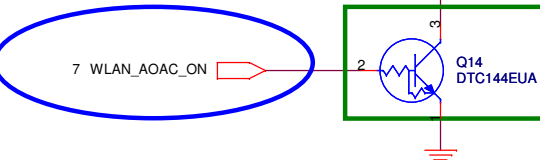
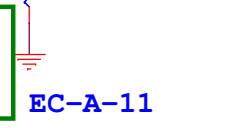
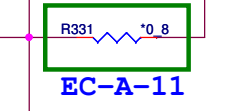
+1.5V	11,35
3V_S5	3,7,8,9,10,11,18,29,33
3VPCU	7,8,16,19,28,29,32,33,34,38
+3V	3,7,8,9,10,11,13,16,17,18,19,20,21,23,25,27,28,32,33,34,35,36,37,38,39



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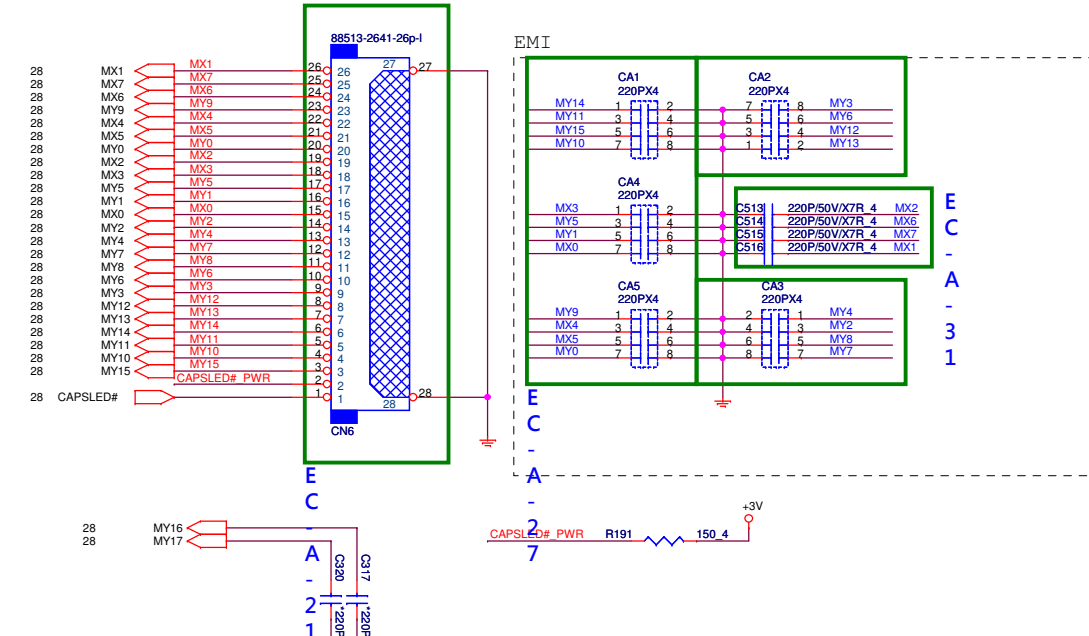
EC-A-15



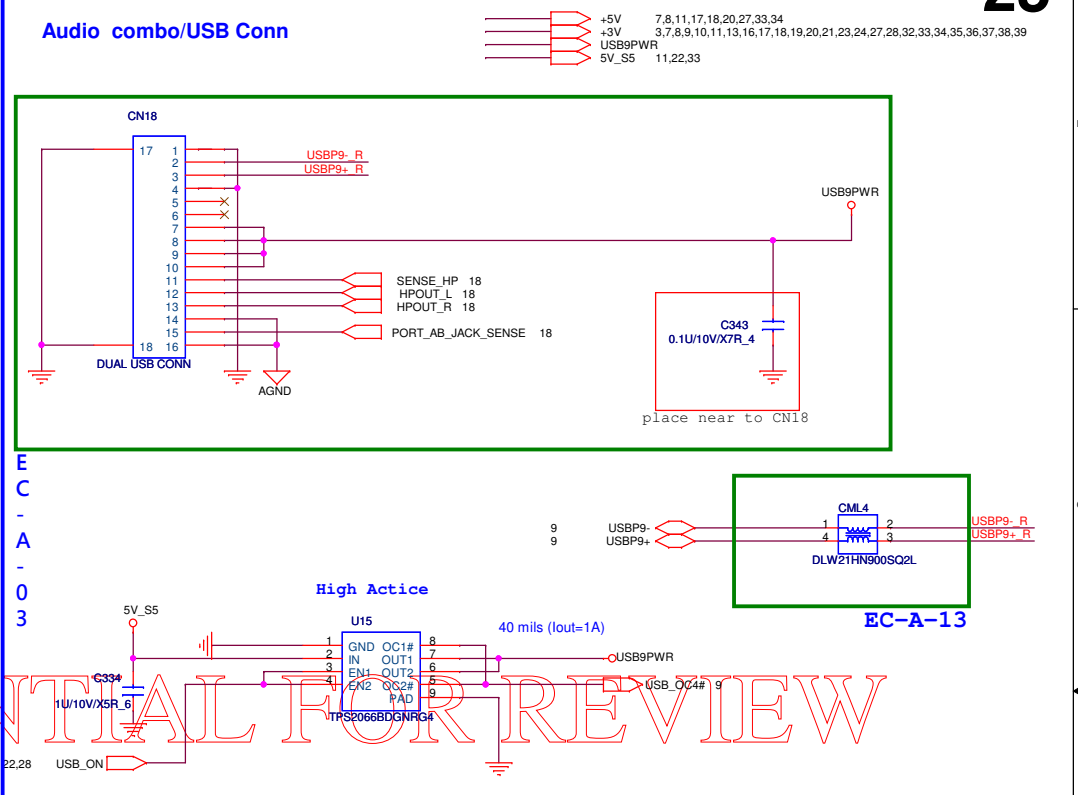
PROJECT: LZ7
Quanta Computer Inc.

Size	Document Number	Rev
	WLAN/BT	1A
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KEYBOARD

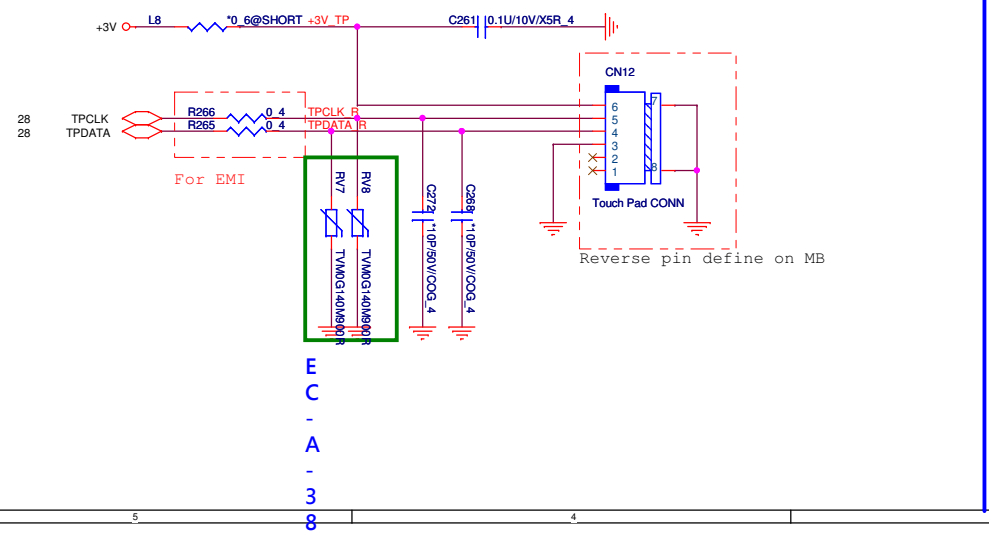


Audio combo/USB Conn



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Touch pad



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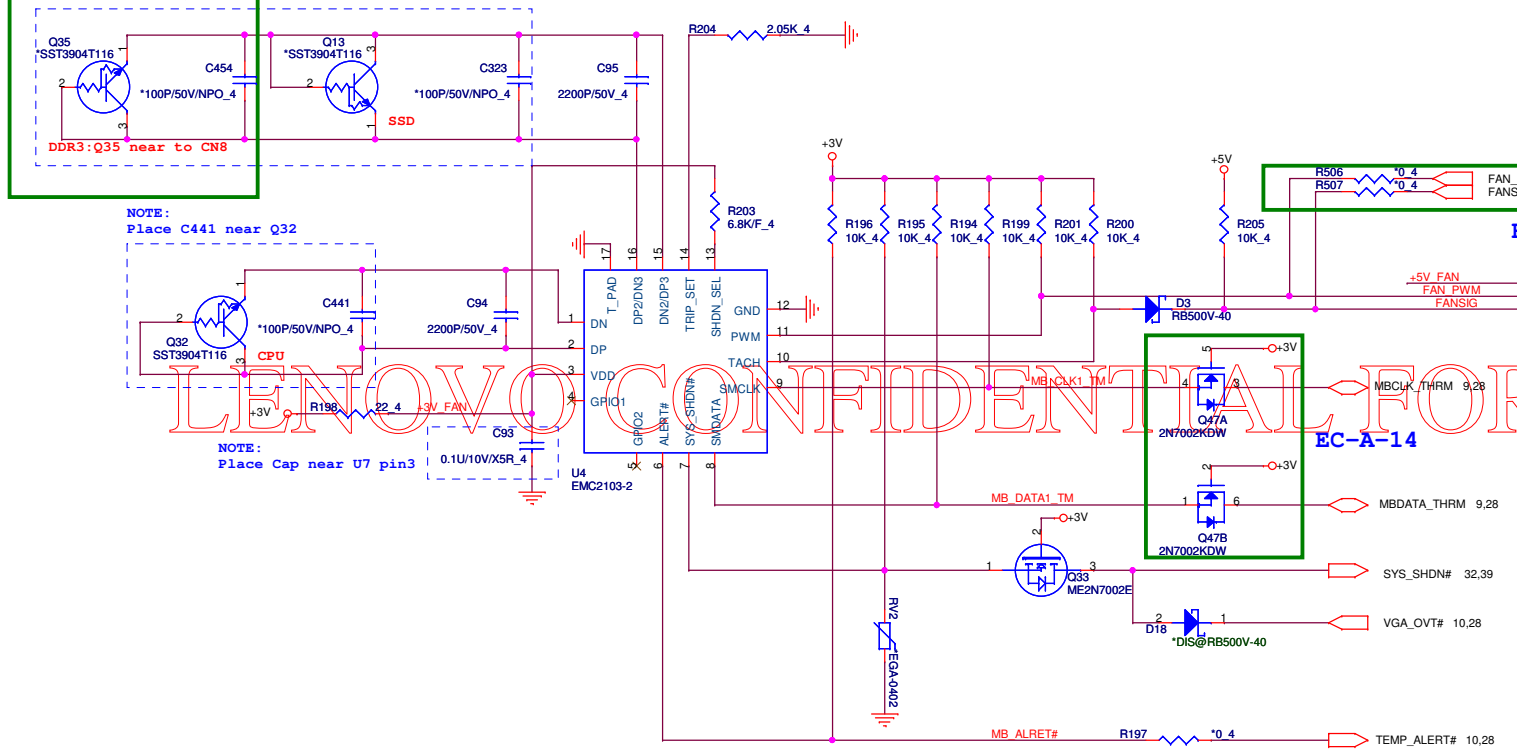
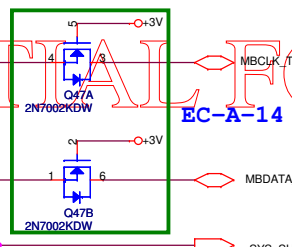
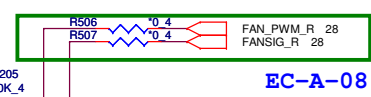
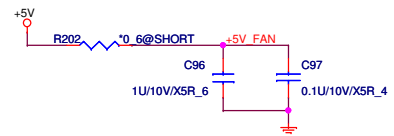
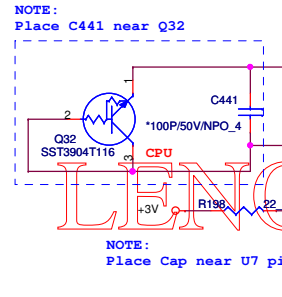
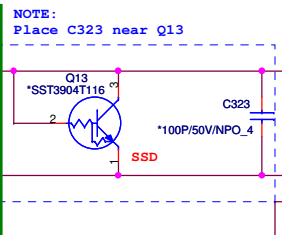
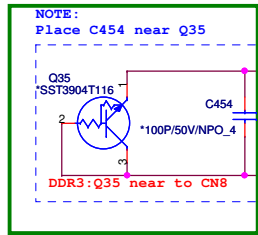
PROJECT : LZ7

Quanta Computer Inc.

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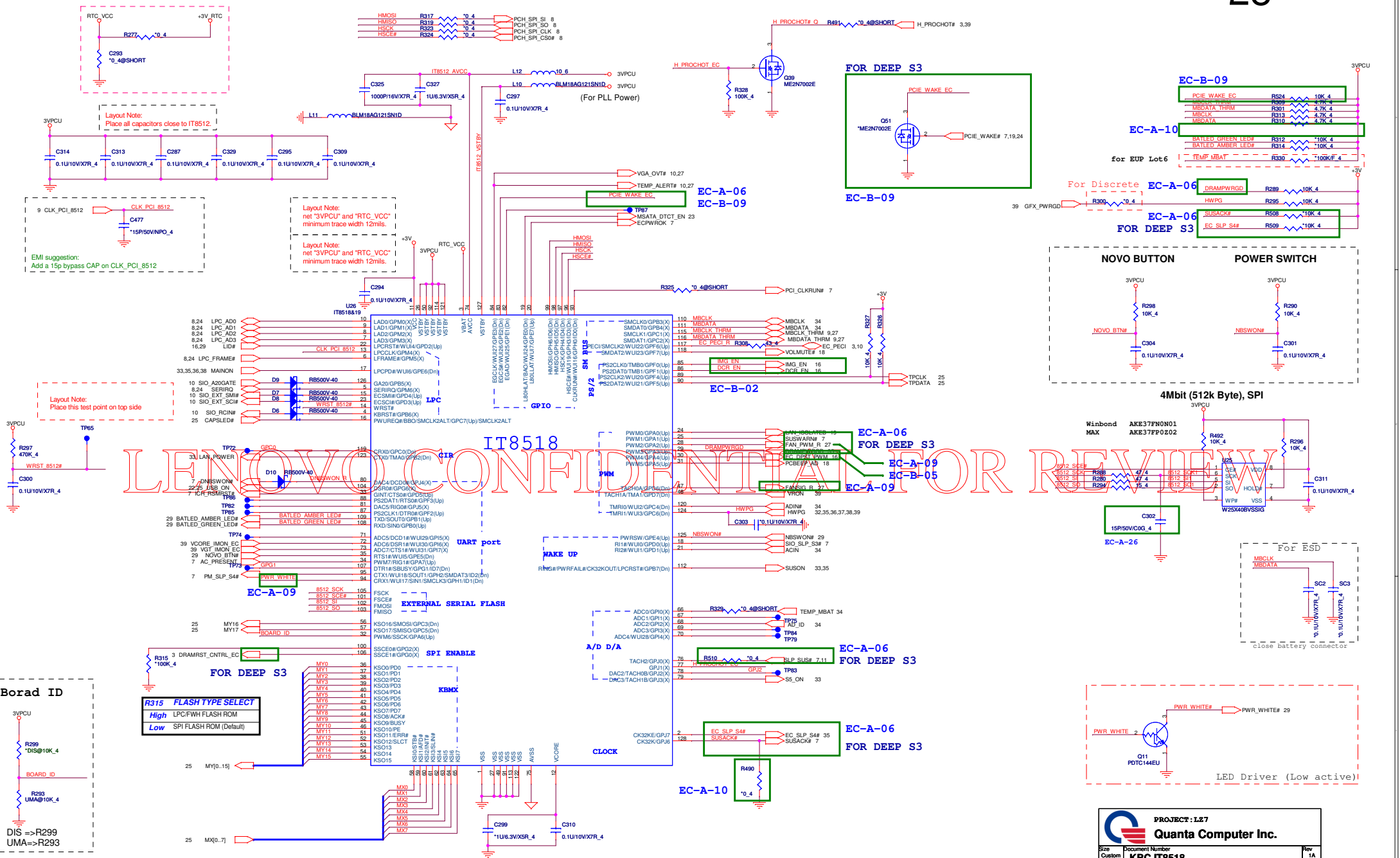


EC-B-07
EC-A-25



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Quanta Computer Inc.		
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	FAN/Thermal	1A
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Board ID

DIS => R299
UMA => R293

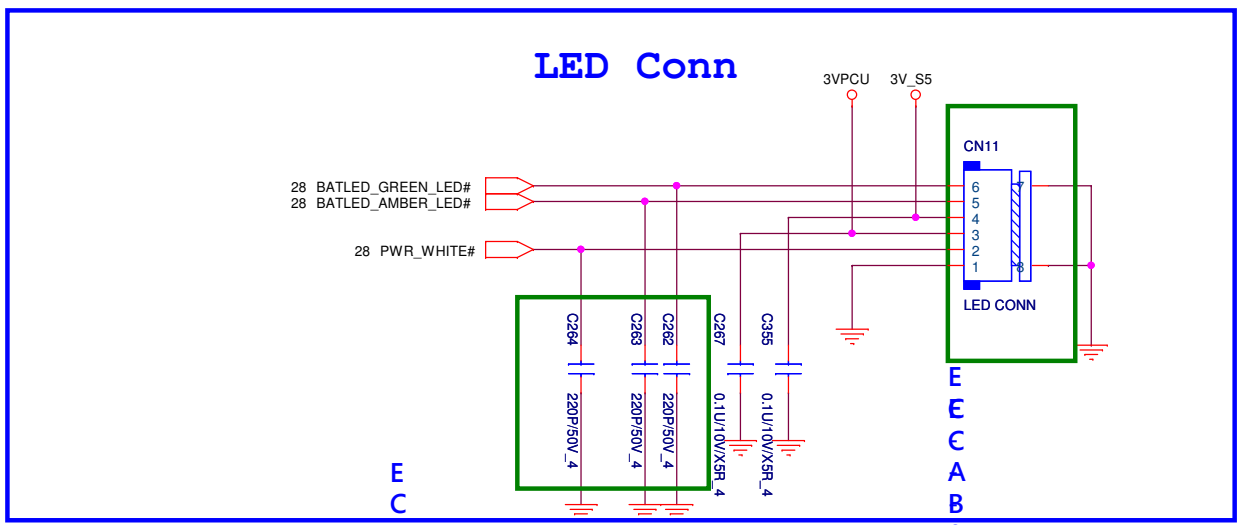
R315 FLASH TYPE SELECT

High	LPC/FWH FLASH ROM
Low	SPI FLASH ROM (Default)

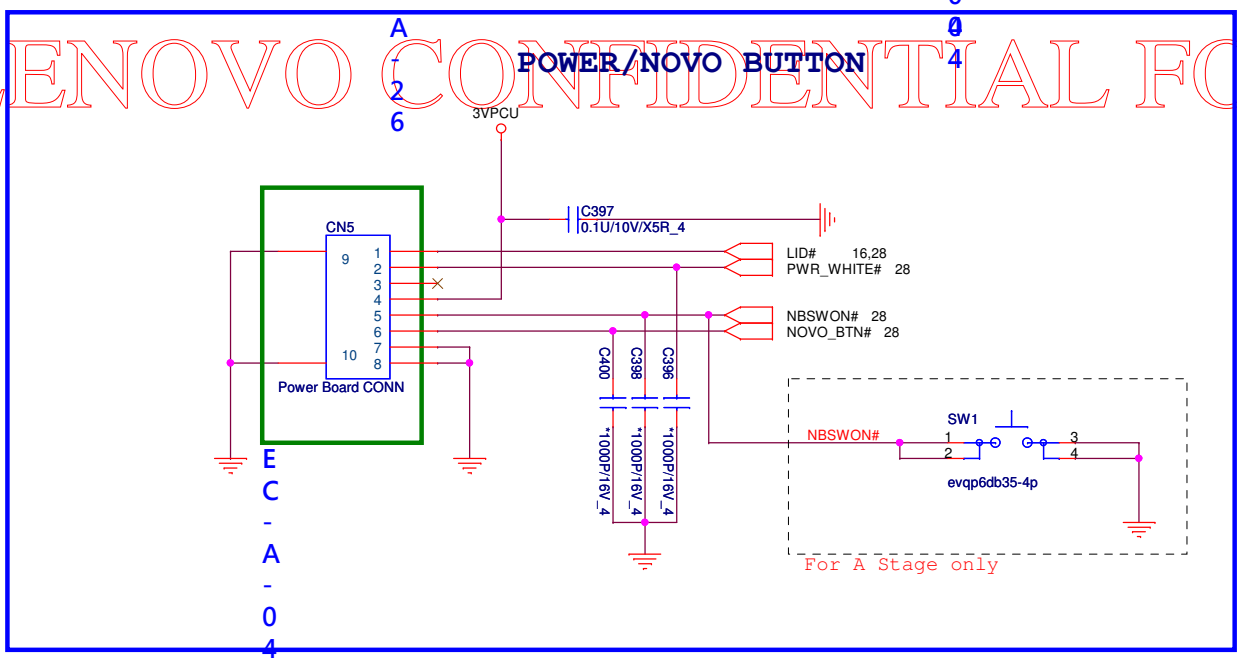
PROJECT : I27
Quanta Computer Inc.

Size: Custom	Document Number: KBC IT8518	Rev: 1A
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+3V	3,7,8,9,10,11,13,16,17,18,19,20,21,23,24,25,27,28,32,33,34,35,36,37,38,39
3VPCU	7,8,16,19,24,28,32,33,34,38
3V_S5	3,7,8,9,10,11,18,24,33

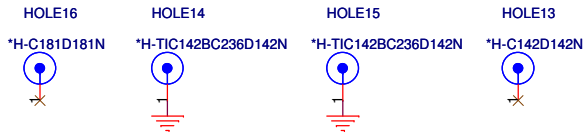


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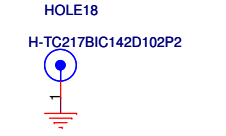


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	SW/LED		
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Hole for CPU support



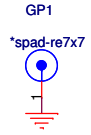
MiniCard SSD



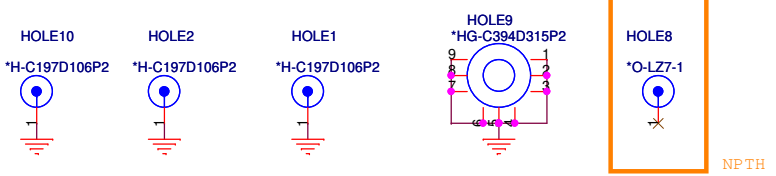
MiniCard WLAN



PAD

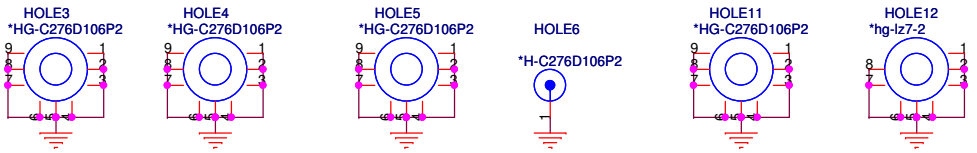


Boundary Hole

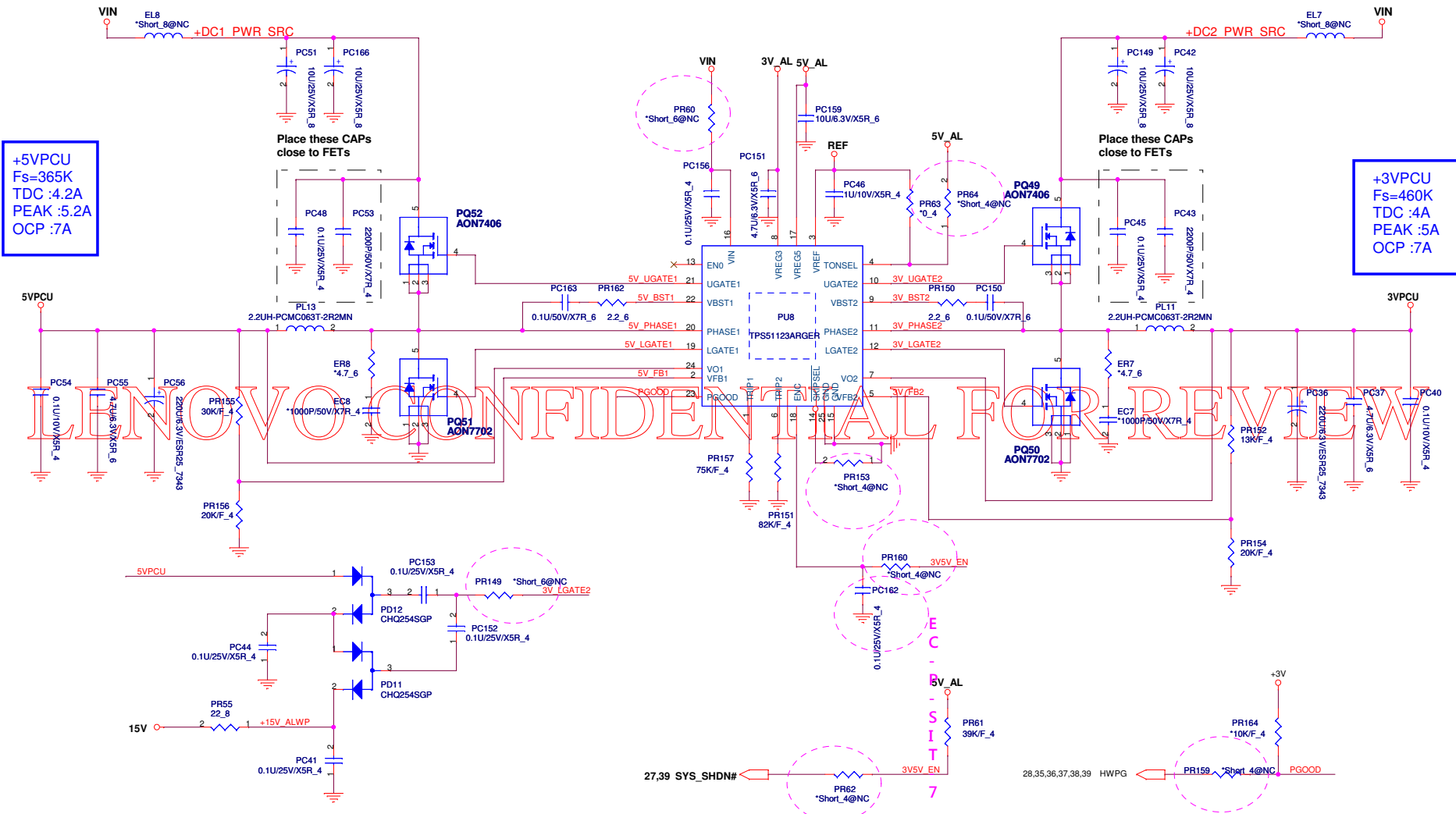


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Round screw hole



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+5VPCU
 Fs=365K
 TDC :4.2A
 PEAK :5.2A
 OCP :7A

+3VPCU
 Fs=460K
 TDC :4A
 PEAK :5A
 OCP :7A

Place these CAPs
 close to FETs

Place these CAPs
 close to FETs

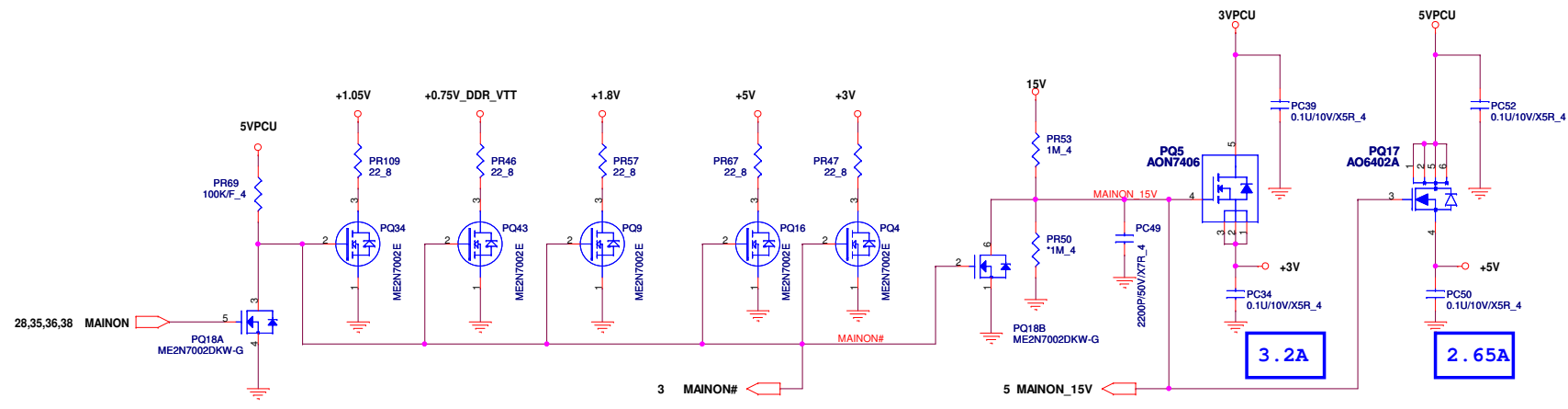
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E
C
P
I
S

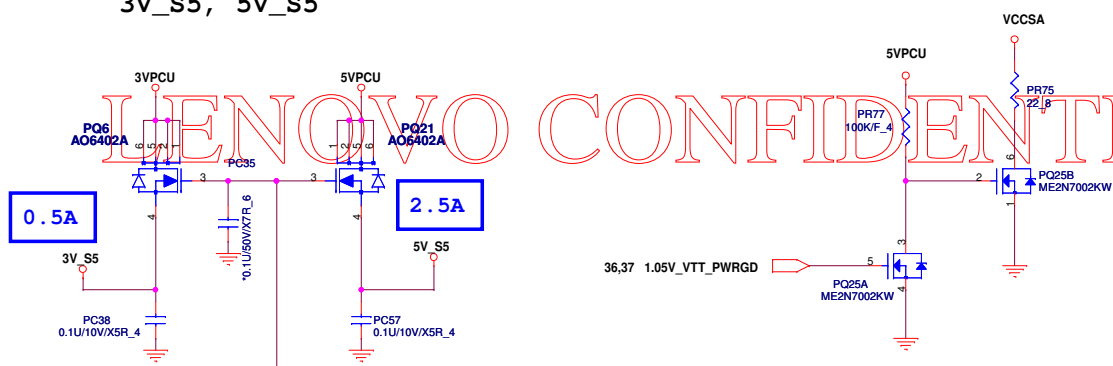
P
R
6
0

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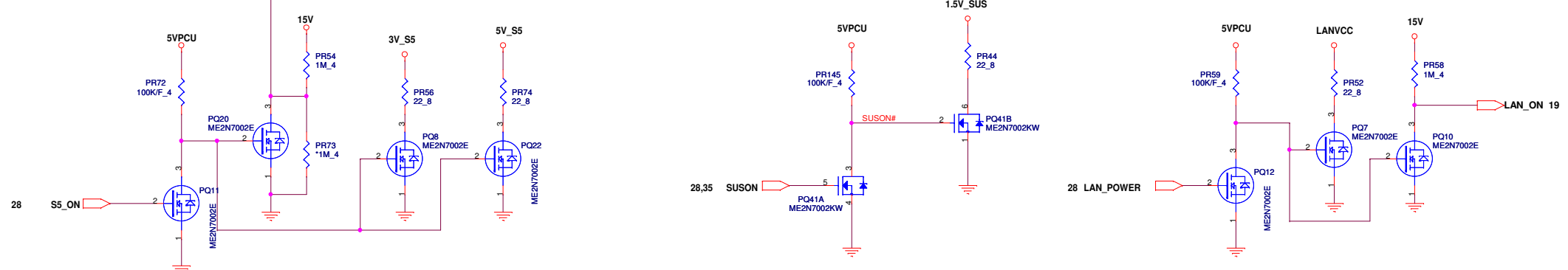
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	3V/5V (TPS51123ARGERR)	
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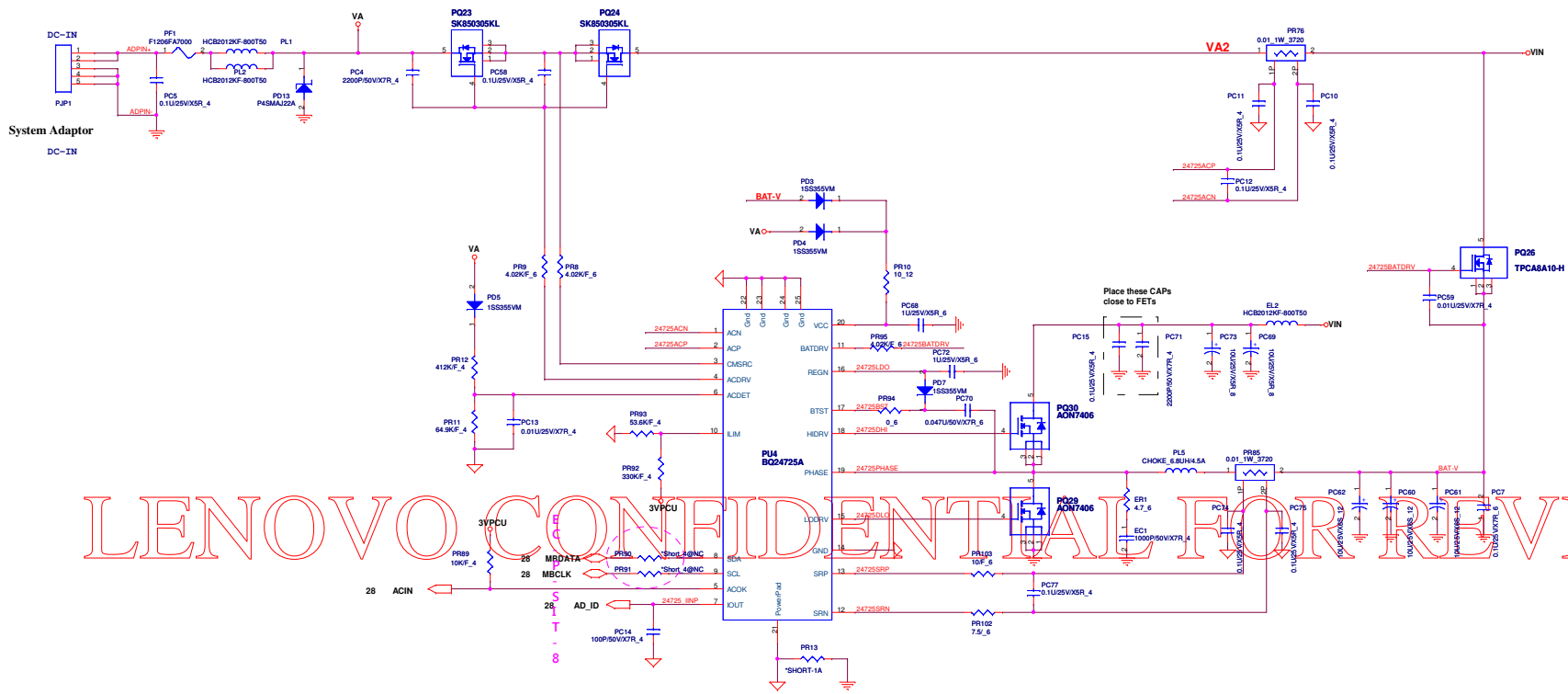


3V_S5, 5V_S5

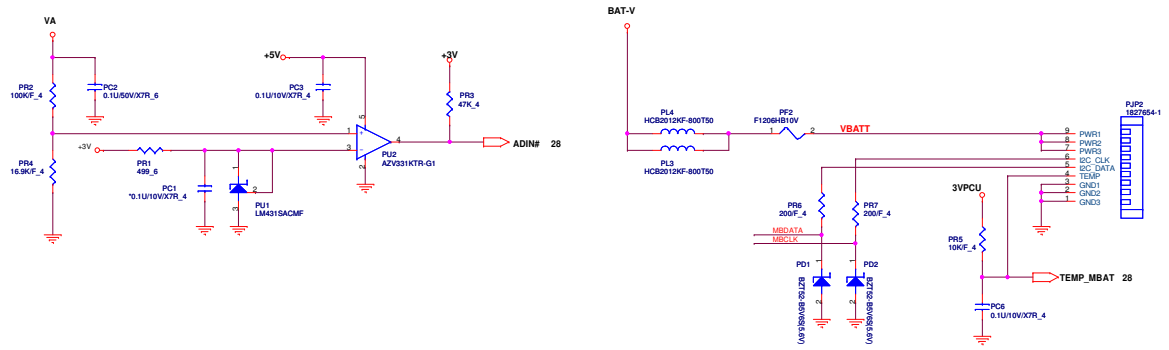


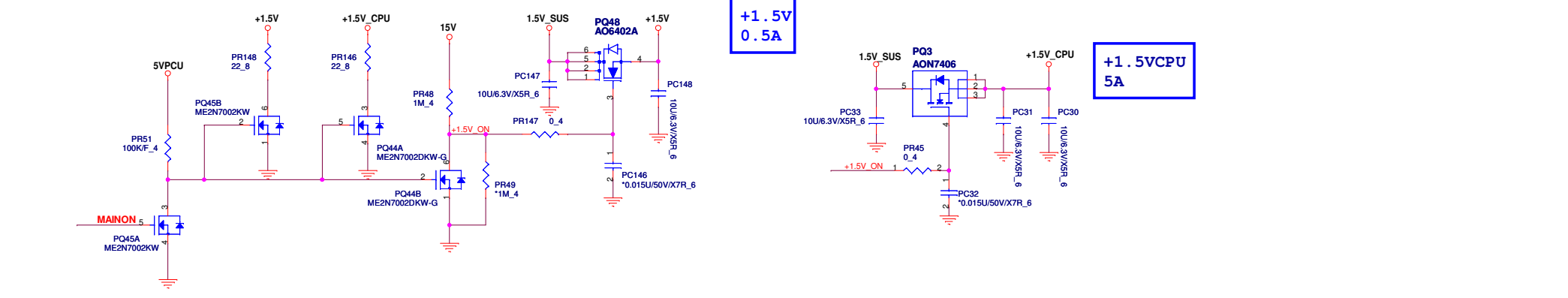
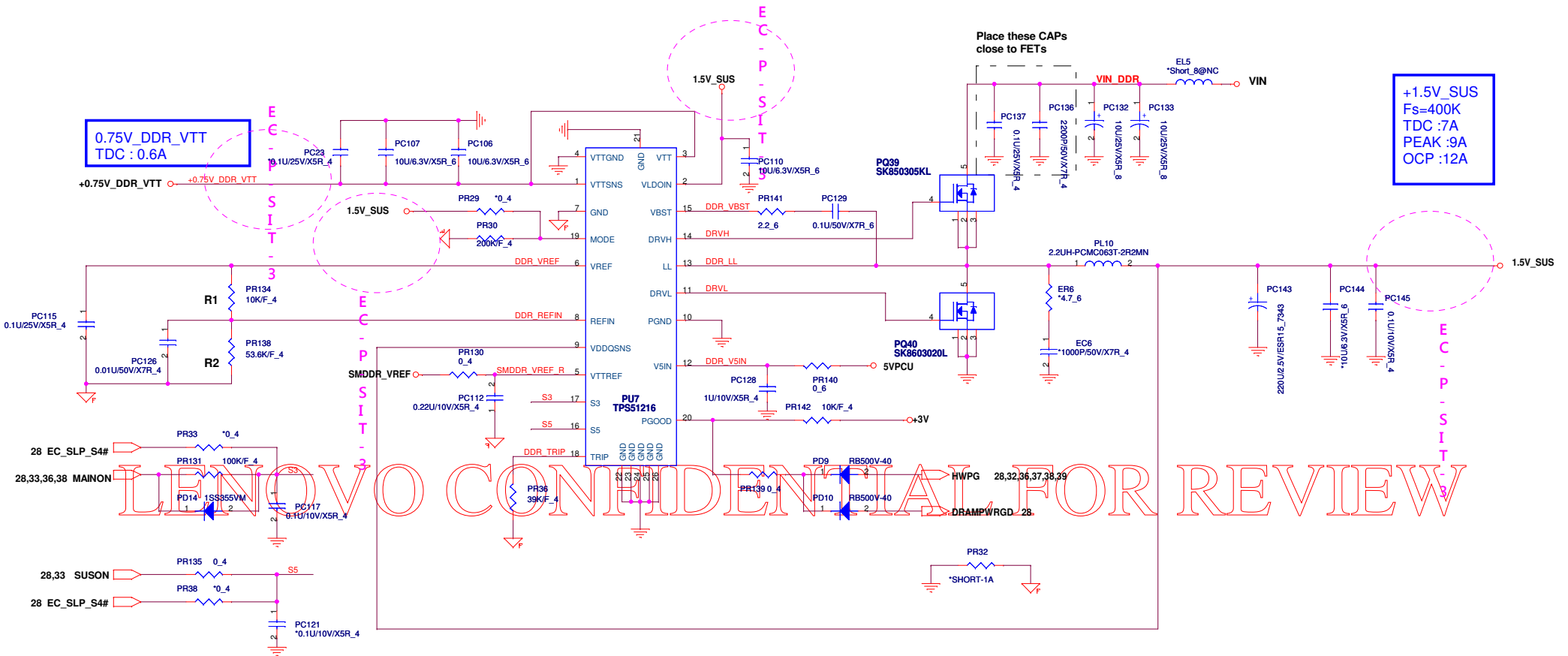
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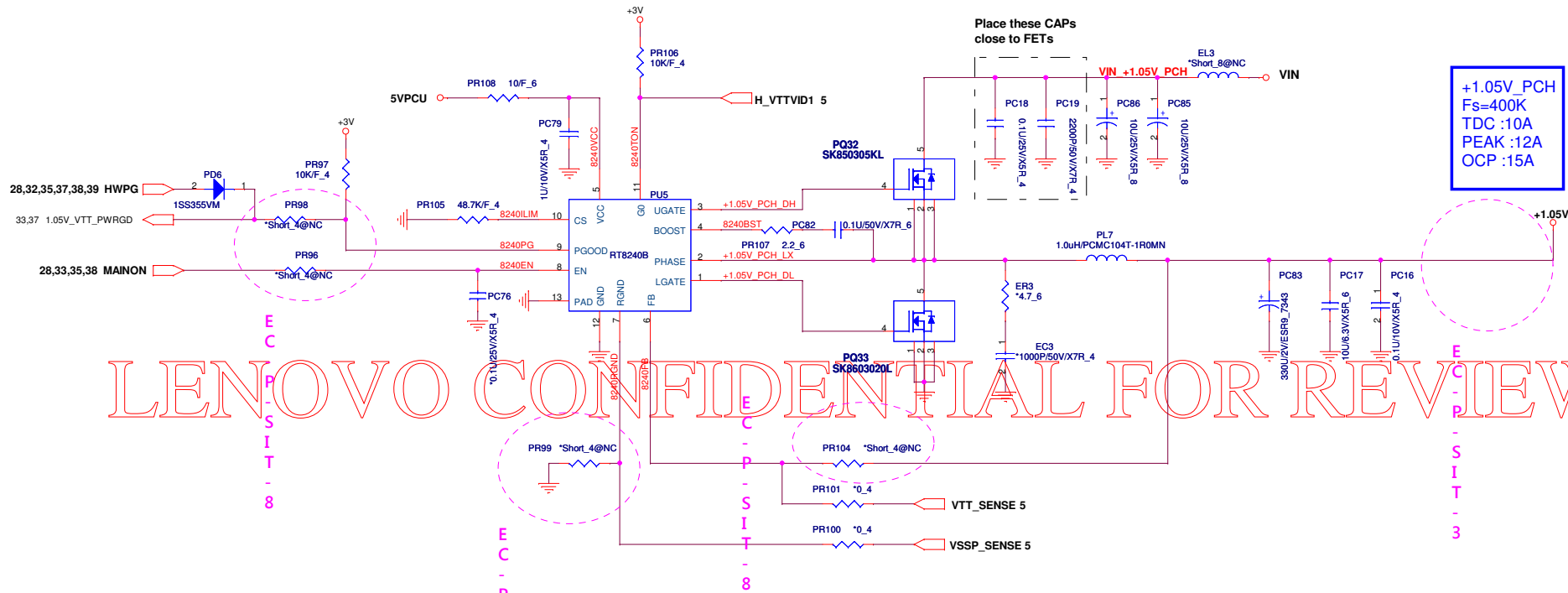


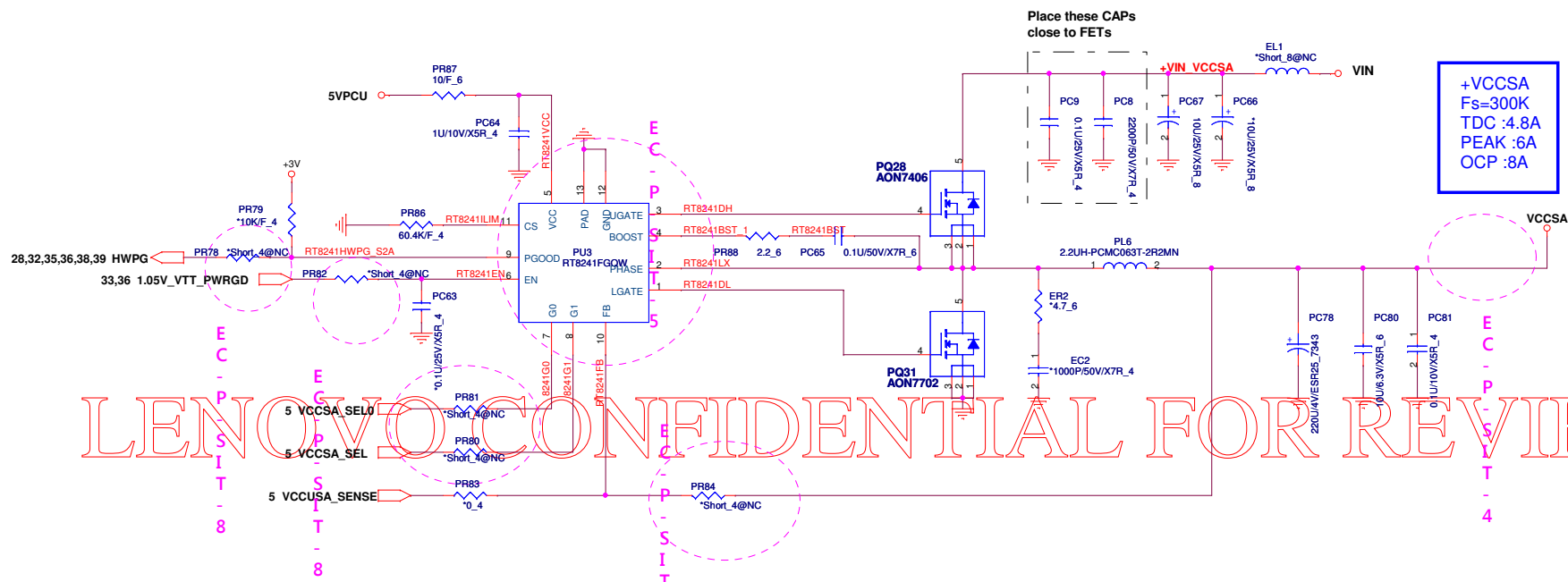
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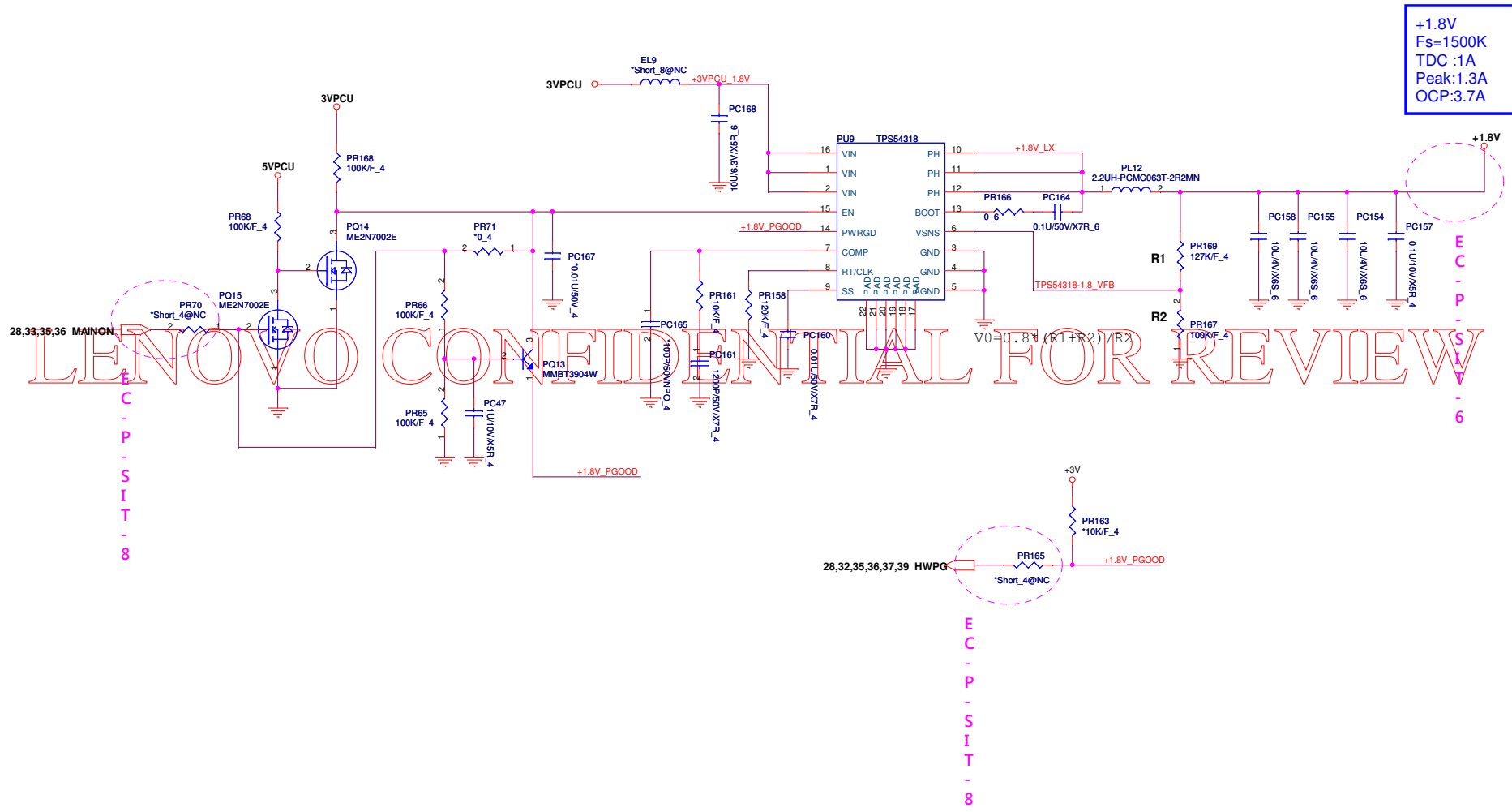
+VCCSA
 Fs=300K
 TDC :4.8A
 PEAK :6A
 OCP :8A

Place these CAPS close to FETs

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G0	G1	VCCSA
0	8	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

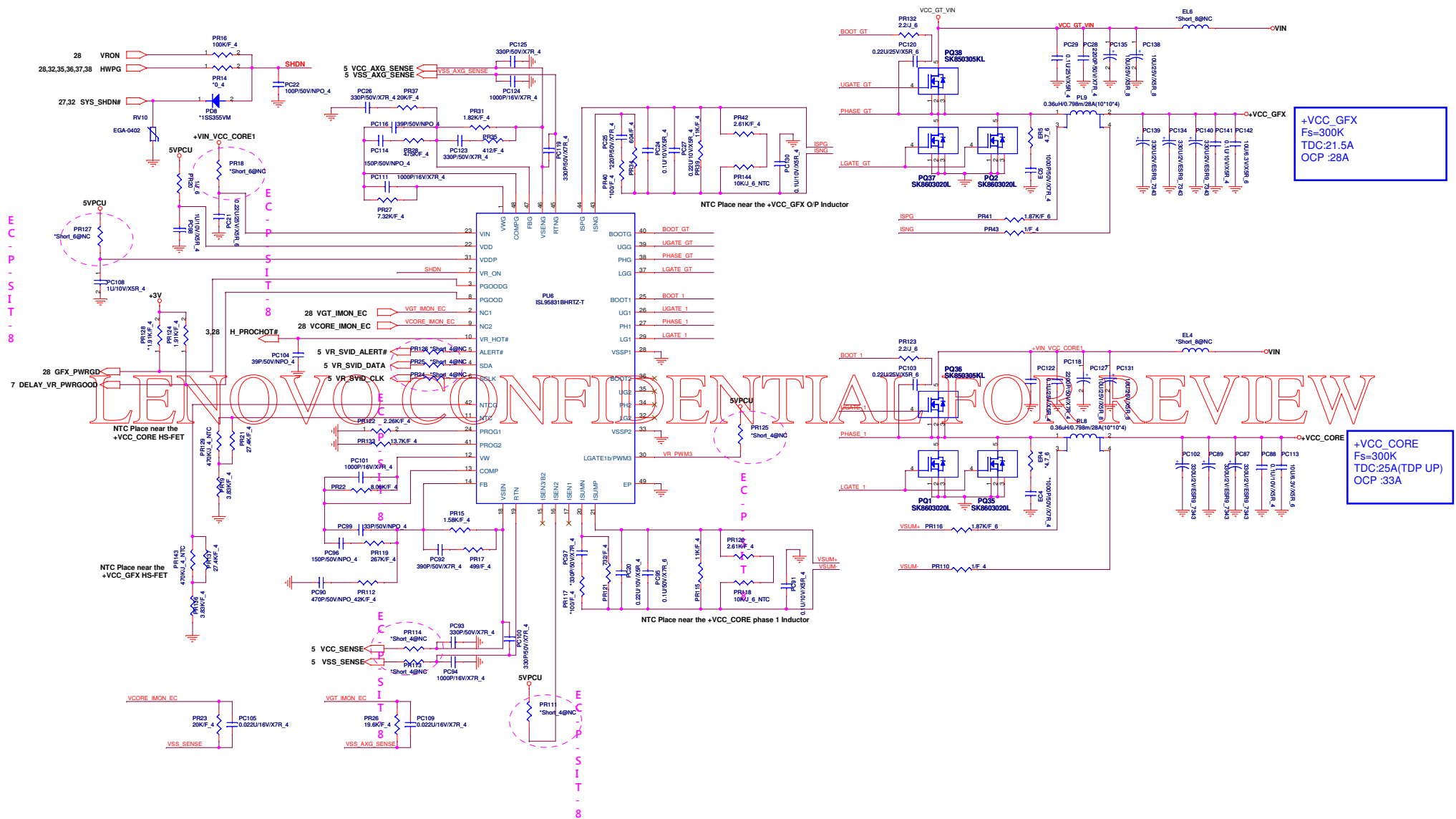
default 0.9V



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E C P S I T - 8

E C P S I T - 8



E C P S I T - 8

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+VCC_GFX
 Fs=300K
 TDC:21.5A
 OCP :28A

+VCC_CORE
 Fs=300K
 TDC:25A(TDP UP)
 OCP :33A

E C	P G	D A/mm/dd	P A	D E
EC-A-01	10,16	11/10/04	R505, C506, C507, Q41, Q42, R502, R503, R504	change GPIO35 to CCD_ON for bios request, Add camera control circuit
EC-A-02	18	11/10/11	Q16, R373, C393, R360, R369, R368, C386, U17	modify audio combo jack circuit for audio plug in/out nosie
EC-A-03	25	11/10/11	CN18, C348, C356, CR352	Delete C348, C356, R352 change CN18 Pin define
EC-A-04	29	11/10/12	CN5, CN11	Change CN5, CN11 footprint from pitch 1.0mm to 0.5mm
EC-A-05	17,19	11/10/12	CN10, CN9	Change CN9, CN10 footprint to correct one
EC-A-06	7,28	11/10/17	R608, R509, R112	Add DEEP S3 function
EC-A-07	10	11/10/17	R88, R93	R93 Asm, R88 noAsm for Change Board ID to SIV stage
EC-A-08	27	11/10/17		Add EC detect Fan speed circuit
EC-A-09	28	11/10/17		Change EC pin define, PIN94 connect to PWR_WHITE, PIN28 connect to FAN_PWM_R, PIN47 connect to FANSIG_R
EC-A-10	28	11/10/17	R316, R490	Del R316 for pin94 use PWR_WHITE signal No Asm R490 for EC use internal clock
EC-A-11	24	11/10/17	Q14, R331	Q14 Asm, R331 No Asm for input AOAC function
EC-A-12	11	11/10/17		Add DEEP S3 function
EC-A-13	16,22,25	11/10/17	CML1, CML2, CML3, CML4, R320, R318, R271, R270	CML2, CML3 CML4 asm R320, R318, R271, R270 R345, R346 noasm for EMI request Change common choke footprint from CHOKENCCM20C900-TR-4P to choke-dlw21s-4p for SMT request
EC-A-14	9,16,27	11/10/17	Q25, Q24, Q26, Q27, Q31, Q34, Q44, Q45, Q49, Q47, Q3, Q5	del Q25, Q24, Q26, Q27, Q31, Q34, Q3, Q5 Add Q44, Q45, Q47, Q49 change from mos to Dual mos (sot363)
EC-A-15	24	11/10/17	C489	Change footprint from CH6101K9A14 0805 to CH6101M1904 0603 for ME Height limit
EC-A-16	7	11/10/18	R185	R185 asm for System PWR_OK tune
EC-A-17	22	11/10/18	CML5, 6, 7, 8 R512, R513, R514, R515, R516, R517, R518, R519	Reserve CML5, 6, 7, 8 R512, R513, R514, R515, R516, R517, R518, R519 asm for EMI request
EC-A-18	5	11/10/19	C508	Add 10uF 6.3V Cap on VCCSA for INTEL DG request
EC-A-19	7	11/10/21	R4, R5, R6, R379, R380, R381	Delete Reserve LVDS signal from PCH
EC-A-20	8	11/10/21		Delete SATA2 for PCH Change to HM77
EC-A-21	25	11/10/21		Change CN6 footprint from GB1RF260-1253-8F to 88513-2641-26p-1-smt for SMT request
EC-A-22	15	11/10/21	C21, C22, C33, C35, C44, C48, C50, C51, C52, C58, C65, C66, C87, C418, C420, C424, L4, L6, L7, L18, Q19, Q48, Q48, R48, R53, R60, R61, R63, R64, R66, R68, R75, R81, R94, R95, R96, R97, R103, R385, R393, U2, U18	Delete eDP to LVDS IC Page
EC-A-23	3	11/10/21	RP7, R447, R448, R467, C449, C450, C453, C452	R467, RP7 no asm, R447, R448 asm for eDP function disable
EC-A-24	3	11/10/21	R478, U23, R482, Q38, R120, R477	R478, R482, Q38 asm, U23, R120, R477 Noasm Delete AND GATE for intel CRB Suggest
EC-A-25	27	11/10/21	Q35	Add Q35 for thermal request
EC-A-26	18,28,29	11/10/22	C406, C407, C410, C411, C302, C262, C263, C264	audio C406, C407, C410, C411 (CH4102K1B03) asm EC C302 (CH01506JBD9) asm LED C262, C263, C264 (CH12206JB00) asm for EMI request
EC-A-27	25	11/10/22	CA1, CA2, CA3, CA4, CA5	CA1, 2, 3, 4, 5 asm for KB EMI request
EC-A-28	17	11/10/22	R248, R243, R241, R238	R248, R243, R241, R238 asm for HDMI EMI request
EC-A-29	19	11/10/24	C509, C510, C511, C512	Reserve C509, C510, C511, C512 for LAN EMI request
EC-A-30	18	11/10/24	R386, R387, R388, R389, R366, C387	R386, R387, R388, R389 change to CX8PG181001 R366 Change to CX471110000 C387 Change to CH0226F0B05 for EMI request
EC-A-31	25	11/10/24	CA6, C513, C514, C515, C516	delete CA6 and change from cap array to cap 0402 C513, C514, C515, C516 asm for EMI request
EC-A-32	8	11/10/24	R84, C369	Change R84 to CS02202FB12 change C369 to CH01506JBD9 for EMI request
EC-A-33	22	11/10/24	U24	Change U24 from G547E2P81U to G547N1P81U for 3.7A usb3.0 2 port Current
EC-A-34	11	11/10/24	C15, C17, C18	C15, C17, C18 asm for VCCDAC ripple voltage issue
EC-A-35	20	11/10/27		Del R276, R279, R281, R287 for SATA TX RX Signal line Branch too long issue
EC-A-36	18	11/10/27	C383, C363, C351, C365, C353, C352	C383, C363, C351, C365, C353, C352 noasm for FAE Suggest
EC-A-37	20	11/10/27	R307, R305	R307, R305 No asm, for Boost mode change to Standard mode
EC-A-38	16,25	11/10/31	U1, RV7, RV8	U1, RV7, RV8 asm, for ESD request


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E C N	P G	D A/mm/dd	P A R	D E S C R I P T I O N
EC-B-01	06,13	11/12/05	R520,R521,R522,Q50	R522 Asm for DDR M3 mode
EC-B-02	16,28	11/12/05		Add DCR_IN,IMG_IN Signal for Lenovo request
EC-B-03	16	11/12/05	R9,R12,CML1	Delete R9,R12 CML1 asm for EMI request
EC-B-04	29	11/12/05	CN11	Change CN11 footprint from 88707-060n-6p-1 to 88501-0601-6P-L-smt for assembly line issue
EC-B-05	16,28	11/12/05	R383,R523	R383 No asm R523 asm Add LCD PWM Signal from EC for lenovo request
EC-B-06	10	11/12/06	R447,R141,R93,R88	R387,R88 asm R93,R141 no asm for board id SIT Stage
EC-B-07	27	11/12/08	Q35	Q35 no asm for thermal request
EC-B-08	19	11/12/09	C509,C510,C511,C512	C509,C510,C511,C512 CH11806JB09 asm for EMI request
EC-B-09	28	11/12/09	Q51,R524	Reserve Q51 R524(CS31002JB28) asm for DEEP S3 function
EC-B-10	22	11/12/09	CML5,CML6,CML7,CML8 R514,R513,R514,R515,R516,R517,R518,R519	CML5,CML6,CML7,CML8 delete change R512,R513,R514,R515,R516,R517,R518,R519 to short0402 for EMI request
EC-B-11	16	11/12/09	RV11,RV12	RV11,RV12 CY140M90B00 asm for ESD request
EC-B-12	09	11/12/13	C401,C402	Change footprint from XTAL-5X3_2-3_8 to xtI-3_2x2_5-2_2x1_7 C401,C402 Change to CH01006JB08 (10pf)
EC-B-13	18	11/12/13	C406,C410,C411,C407	Change CH4102K1B03 (0.1uF) to CH1336J0B01 (330pF) to meet Conexant spec <1000pf for Garbage screen issue
EC-B-14	18	11/12/14	CN3	Change DFHD04MR701 to DFHD04MR211(88266-040xx-xxx-4p-l) for speaker request
EC-B-15	11	11/12/15		R511 connect to 5VPCU for Deep S3 function
EC-B-16	20	11/12/16	R525,R526	R525 asm,R526 No asm for 2nd source parade sata redriver
EC-B-17	20	11/12/20	R322,R321	Delete R322,R321 for +3V,+5V HDD transfer layer via reduce

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EC NO.	PG.	DATE	DART REFERENCE	DESCRIPTION
EC-P-SIV-1	32		PR157,PR151	3VPCU,5VPCU OCP set
EC-P-SIV-2	34		PJP1	Change DC-IN CONN footprint
EC-P-SIV-3	34		PF1,PF2	Change Fuse footprint
EC-P-SIV-4	34		PQ26	Change N-MOSFET with built-in Schottky diode
EC-P-SIV-5	34		EL2	Add charger bead
EC-P-SIV-6	34		PR85	Change PR85 to 10mohm
EC-P-SIV-7	34		PR13	Change PR13 footprint
EC-P-SIV-8	34		PR11,PR12	Change ACDET voltage
EC-P-SIV-9	34		PR92,PR93	Change ILIM voltage
EC-P-SIV-10	34			Modify MBDATA,MBCLK
EC-P-SIV-11	35		PJP8,PJP9	Change to default short
EC-P-SIV-12	35		PC144	Change to NC
EC-P-SIV-13	35		PR32	Change PR32 footprint
EC-P-SIV-14	35			Change PU7 GND
EC-P-SIV-15	35		PR138	Change PR138 for 1.5V regulation
EC-P-SIV-16	35		PD14	Add PD14 for S3
EC-P-SIV-17	35		PJP6	Change to default short
EC-P-SIV-18	35			Change netname for EE request
EC-P-SIV-19	36		PJP3,PJP4	Change to default short
EC-P-SIV-20	36		PR105	Change PR105 to 48.7K for OCP set
EC-P-SIV-21	36		PR99,PR100 PR101,PR104	Change PR99 & PR100 to 0ohm,Change PR101 & PR104 to NC
EC-P-SIV-22	37		PJP5	Change to default short
EC-P-SIV-23	37		PR86	Change PR86 to 60.4K for OCP set
EC-P-SIV-24	37		PR83,PR84	Change PR84 to 0ohm,Change PR83 to NC
EC-P-SIV-25	37		PU3	Change PU3 to RT8241E for VCCS voltage level
EC-P-SIV-26	38		PJP9	Change to default short
EC-P-SIV-27	39		PL8,PL9	Change PL8,PL9 footprint
EC-P-SIV-28	39		ER5,EC5	Add ER5,EC5 for EMI request
EC-P-SIV-29	39		PC20	Change PC20 to 0.22uF for CPU transient
EC-P-SIV-30	39		RV10	Add RV10 for ESD request
EC-P-SIV-31	39		PR23	Change PR23 to 20K for CPU IMON
EC-P-SIV-32	39		PR34	Change PR34 to 604ohm for GFX OCP&loadline

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