


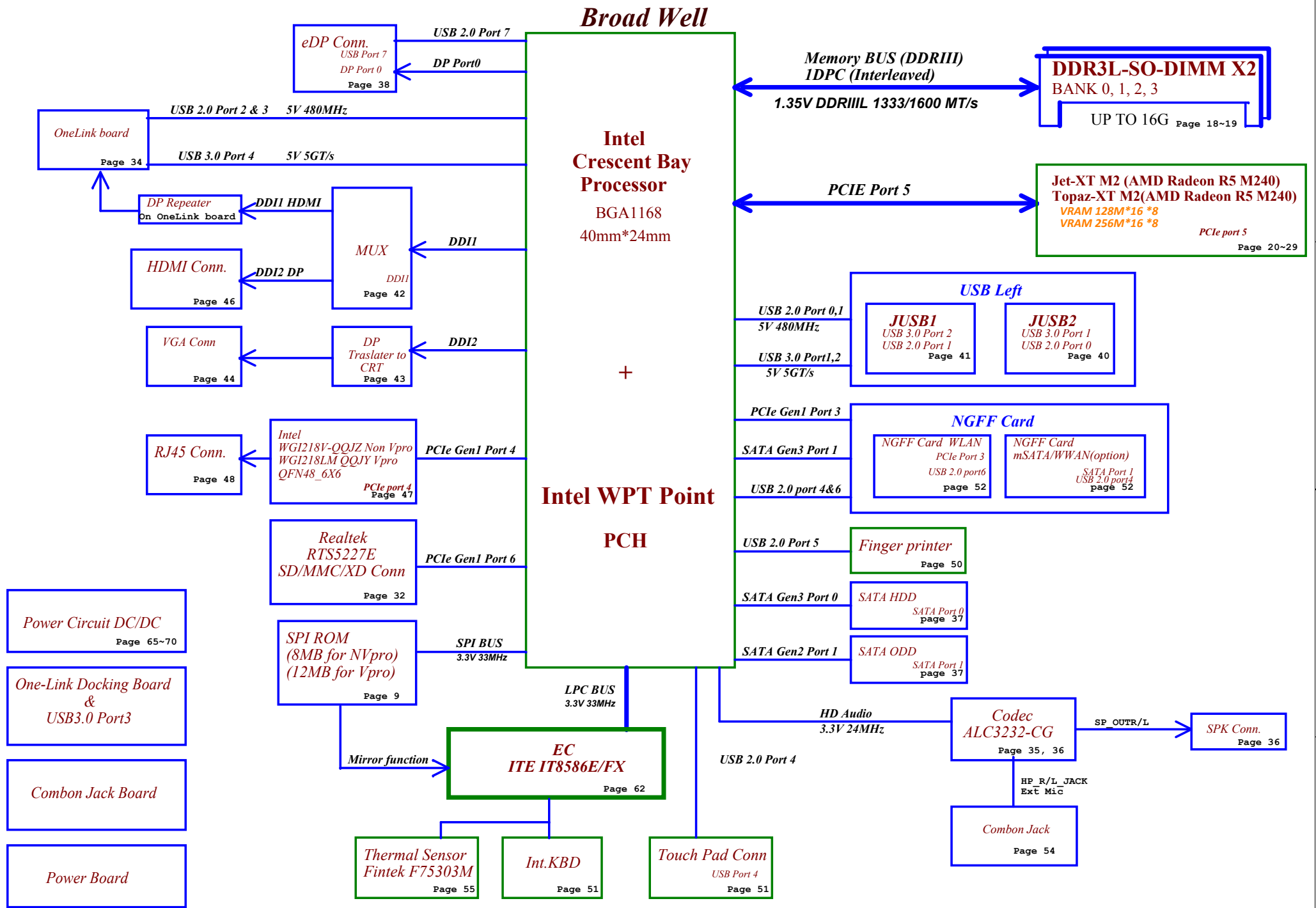
# *LCFC Confidential*

## *NM-A221 Rev1.0 Schematic*

*Intel Crescent Bay Processor with DDRIII + Wild Cat Point PCH  
AMD Opal-XT/ Jet-XT*

*2013-09-07 Rev1.0*

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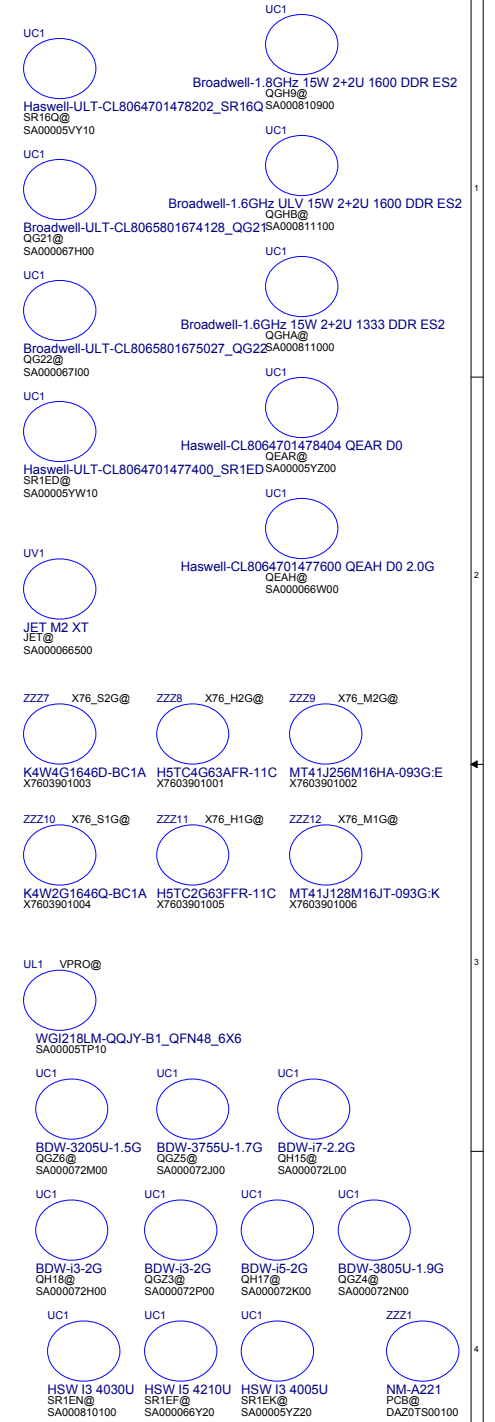
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**Voltage Rails ( O --> Means ON , X --> Means OFF )**

Power Plane	B+	+3VALW	+1.5V	+5VS
				+3VS
State	B+	+3VALW	+1.5V	+1.5VS
				+VCCSA
S0	O	O	O	+V1.5S_VCCP
				+CPU_CORE
S3	O	O	O	+VGA_CORE
				+GFX_CORE
S5 S4/AC Only	O	O	X	+1.8VS
				+1.05VS
S5 S4 Battery only	O	X	X	+0.75VS
				+3.3VS_VGA
S5 S4 AC & Battery don't exist	X	X	X	+1.5VS_VGA
				+1.05VS_VGA

**High Speed I/O port**

I/O	High Speed Signal	Configuration	Port assignment
1	USB3 1	USB3 1	On MB USB
2	USB3 2	USB3 2	On MB USB
3	PCIE 1 / USB3 3	NC	NC
4	PCIE 2 / USB3 4	USB3 4	Docking USB
5	PCIE 3	PCIE 3	WLAN
6	PCIE 4	PCIE 4	LAN
7	PCIE 5 L0	PCIE 5 L0	GPU
8	PCIE 5 L1	PCIE 5 L1	GPU
9	PCIE 5 L2	PCIE 5 L2	GPU
10	PCIE 5 L3	PCIE 5 L3	GPU
11	PCIE 6 L0 / SATA 3	PCIE 6	Cardreader
12	PCIE 6 L1 / SATA 2	SATA 2	mSATA
13	PCIE 6 L2 / SATA 1	SATA 1	ODD
14	PCIE 6 L3 / SATA 0	SATA 0	HDD



**BOM Structure Table**

BOM Structure	NOTE
PCB@	For PCB load BOM
3G@	3G function (Option with TS@)
TPM@	Trusted Platform Module (TPM)
NM14@	14" SKU ID
NM15@	15" SKU ID
UMA@	UMA SKU ID
DIS@	Optimus SKU ID
X76@	GPU VRAM Setting
M2G@	Micron 256Mx16 VRAM
M1G@	Micron 128Mx16 VRAM
S2G@	Samsung 256Mx16 VRAM
S1G@	Samsung 128Mx16 VRAM
ME@	ME Connector
TS@	Touch screen function
DEBUG@	For debug
BYPASS@	For bypass
MIRROR@	For mirror function
NVPRO@	For Non-VPRO function
VPRO@	For VPRO function
X76_S2G@	For Samsung 2G VRAM

**SMBUS Control Table**

	SOURCE	Main VGA	LAN	BATT	IT8586E	SODIMM	WLAN WIMAX	Thermal Sensor	PCH	CP Module	Charger
PCH_SML0_CLK PCH_SML0_DAT	PCH +3V_PCH	X	V +3V_PCH	X	X	X	X	X	X	X	X
PCH_SML1CLK PCH_SML1DATA	PCH +3V_PCH	V +3VS	X	X	V +3VS	X	X	V +3VS	X	X	X
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VL	X	X	V +3VL	X	X	X	X	X	X	V +3VL
PCH_SMBCLK PCH_SMBDATA	PCH +3V_PCH	X	X	X	X	V +3VS	X	X	V +3V_PCH	V +3VS	X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

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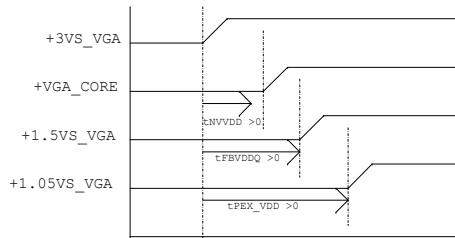
**NOTE LIST**

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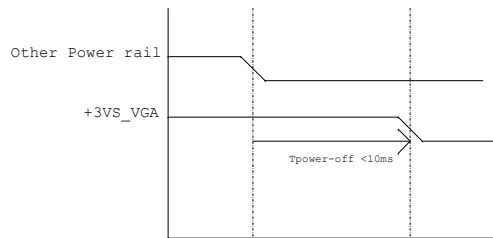
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### VGA and GDDR5 Voltage Rails (N13Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	-	VGA_BL_PWM
GPIO3	OUT	-	VGA_ENVDD
GPIO4	OUT	-	VGA_ENBKL
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	-	DPRSLPVR_VGA
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	GPIO9
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	-	FB_CLAMP_TOGGLE_REQ#
GPIO15	IN	N/A	(100K pull low)
GPIO16	OUT	-	FRMLCK#
GPIO17	IN	N/A	
GPIO18	IN	-	dGPU_HDMI_HPD
GPIO19	IN	-	HPD_IRQ



1. all power rail ramp up time should be larger than 40us



1. all GPU power rails should be turned off within 10ms  
2. Optimus system VDD33 avoids drop down earlier than NVVDD and FBVDDQ

### Performance Mode P0 TDP at Tj = 102 C\* (GDDR5)

Products	GPU (4)	Mem (1,5)	NVCLK /MCLK	NVVDD			FBVDD (1.35V)		FBVDDQ (GPU+Mem) (1.35V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N13X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Device ID	setting	I2C Slave address ID
N13P-GT (28nm)	0x0FDB	
	SMB_ALT_ADDR (ROM_SO Bit 1)	0 0x9E
		1 0x9C

GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N13P-GT1 28nm	PU 10K	PU 25K	PU 45K	PD 35K	PD 10K	PU 5K	PD 10K	Master
	PU 20K	PU 25K	PU 45K	PD 35K	PD 10K	PD 5K	PD 10K	Slave

GPU	N13P-GT		
FB Memory (GDDR5)	ROM_SI		
Samsung 2500MHz	K4G10325FG-HC04		
	32Mx32	PD 45K	
Hynix 2500MHz	H5GQ1H24BFR-T2C		
	32Mx32	PD 35K	
Samsung 2500MHz	K4G20325FD-FC04		
	64Mx32	PD 30K	
Hynix 2500MHz	H5GQ2H24MFR-T2C		
	64Mx32	PD 25K	

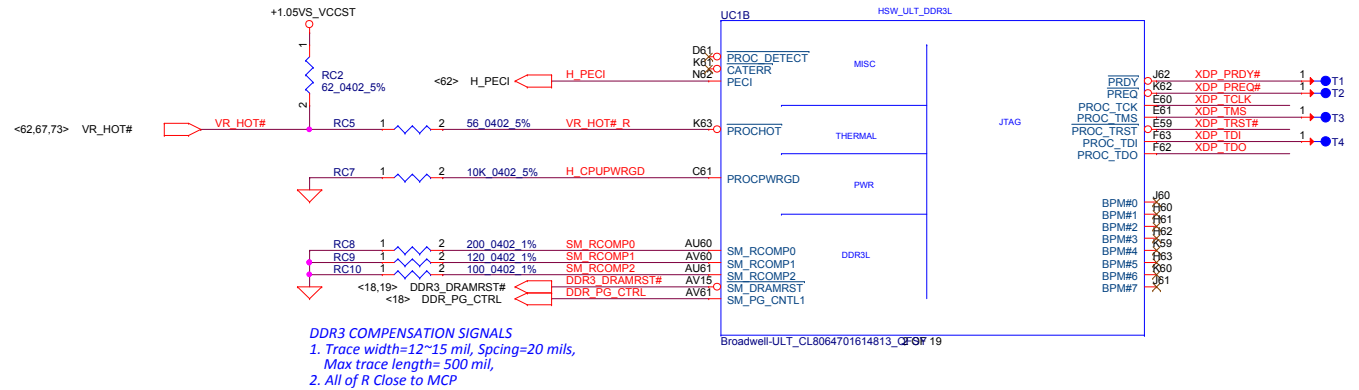
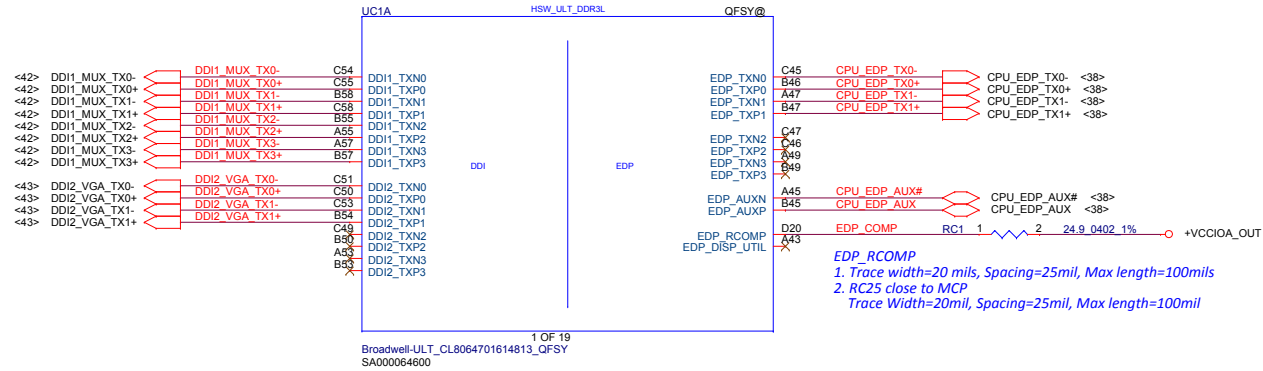
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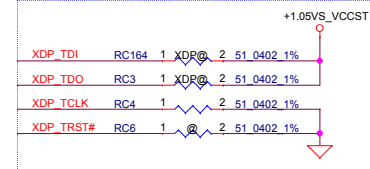


For 14" : DOCKING  
For 15" : HDMI & DOCKING

For 14" : HDMI  
For 15" : VGA



PU/PD Res. For CPU-XDP SIGNAL, Place R Closer to CPU



XDP PU/PD portion need to check again.

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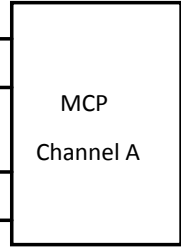
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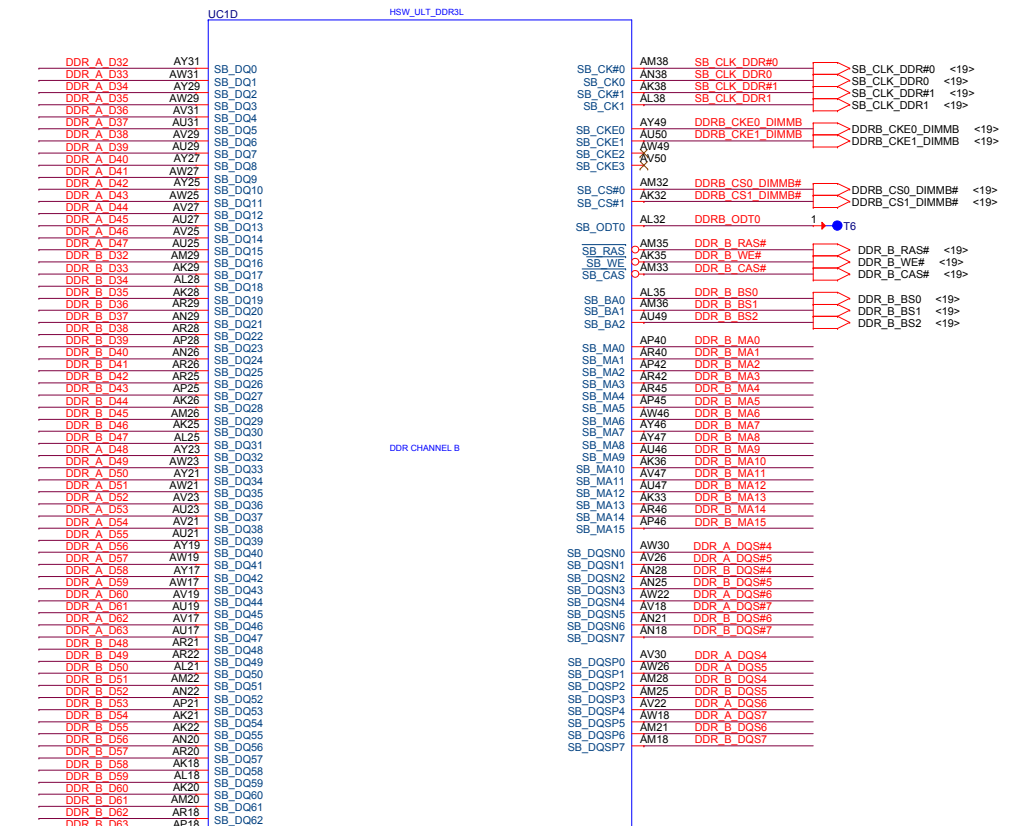
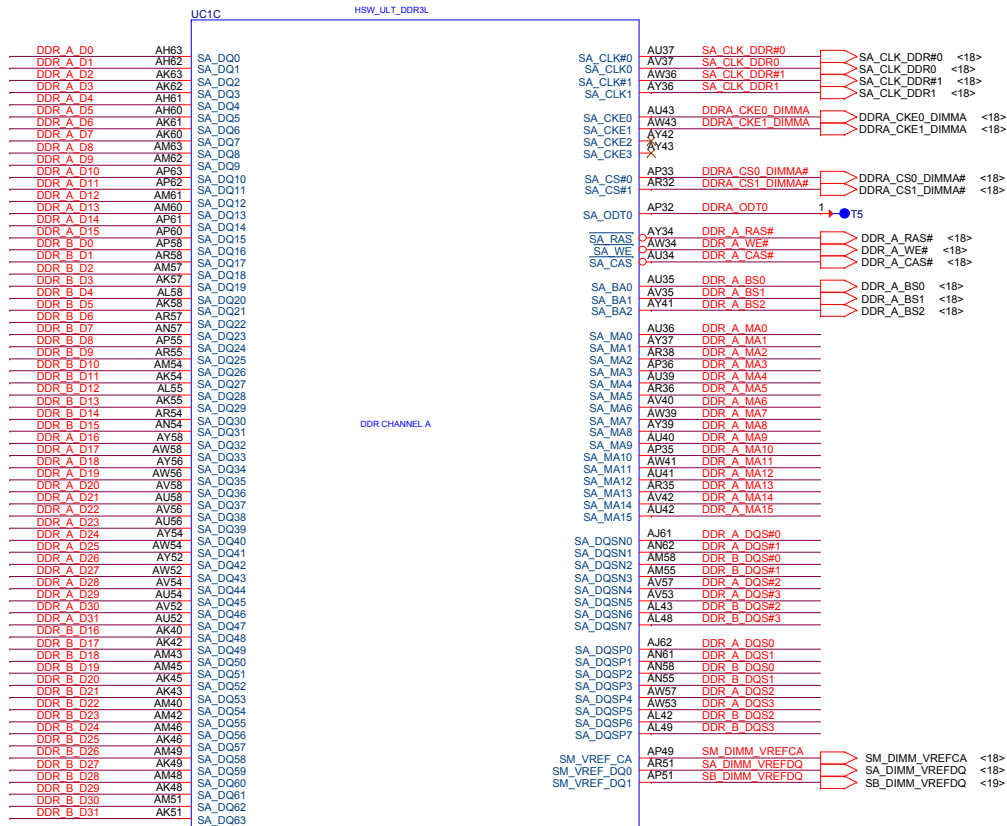
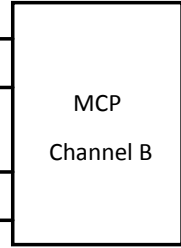
Rev 1.0

# Interleaved (Butterfly Topology) Broadwell Platform System Memory Interface Document Number: 528378 BDW U DDR3L/DDR3L-RS SO-DIMM Interleaved Recommendations

Channel A Byte 0 & 1  
Channel B Byte 0 & 1  
Channel A Byte 2 & 3  
Channel B Byte 2 & 3



Channel A Byte 4 & 5  
Channel B Byte 4 & 5  
Channel A Byte 6 & 7  
Channel B Byte 6 & 7

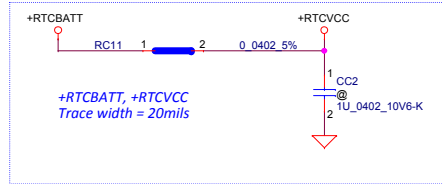


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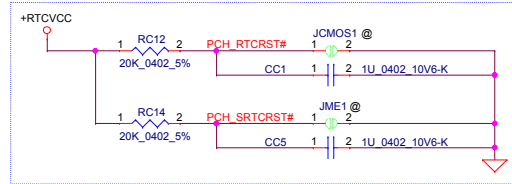
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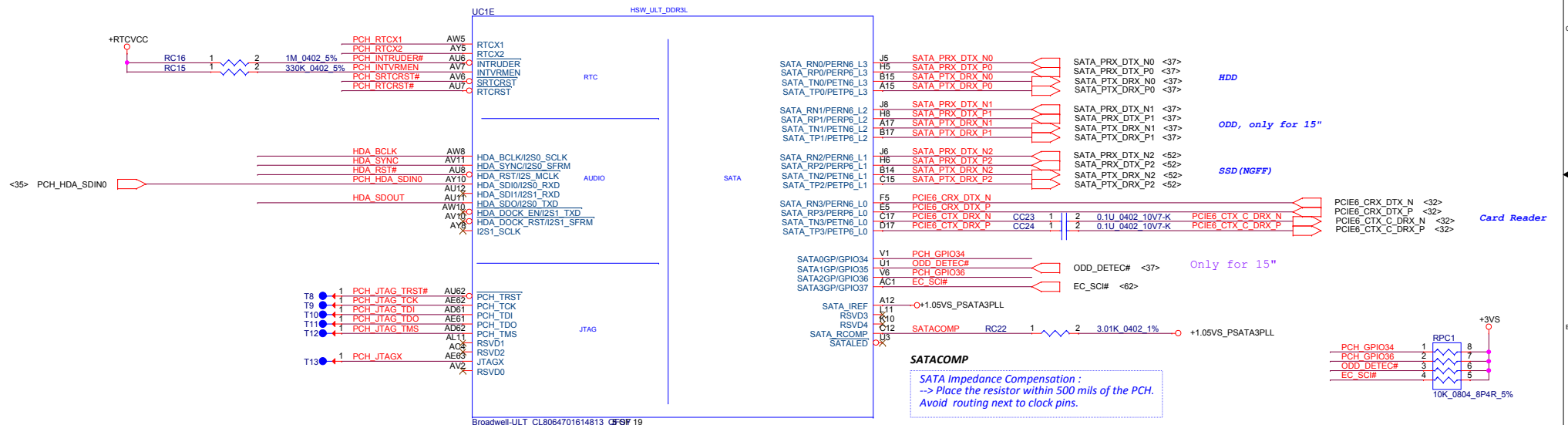
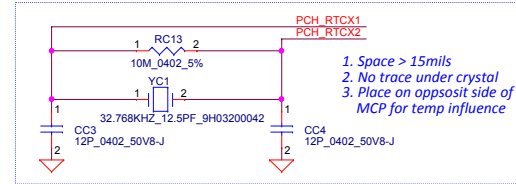
**RTC External Circuit**



**JCMOS, JME Setting, Need Under DDR Door**



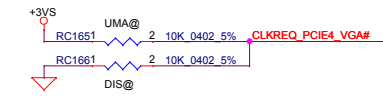
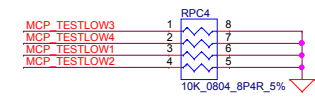
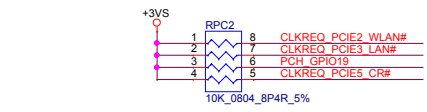
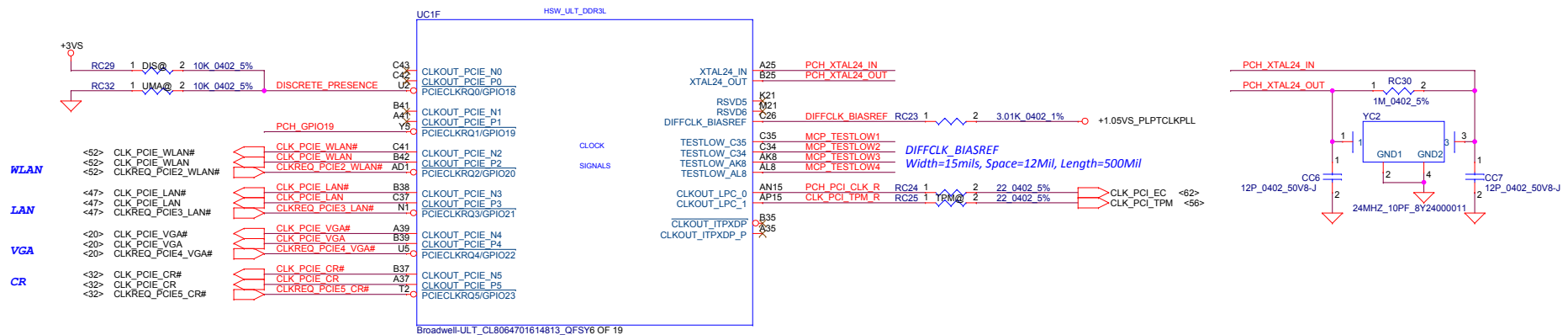
**RTC Crystal**



**INTVRMEN**

- INTVRMEN, should always be pull high
  - H Integrated VRM enable (Default)
  - L Integrated VRM disable
- Internal Voltage Regulator Enable:  
This signal enables the internal 1.05 V regulators.

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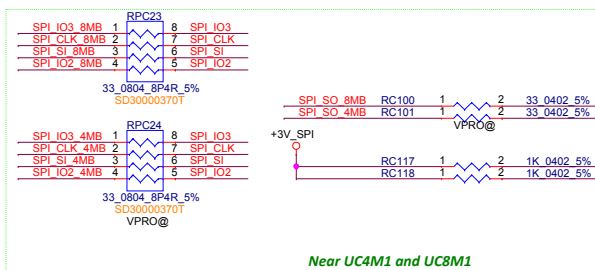
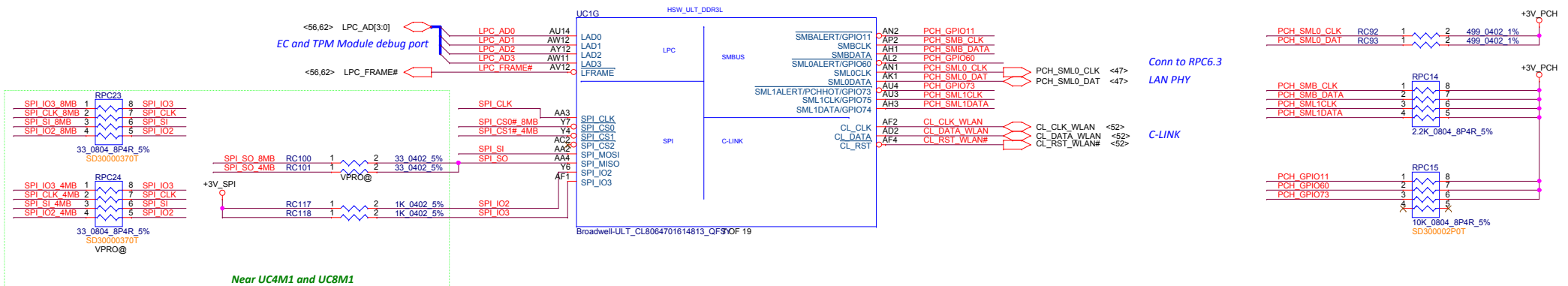


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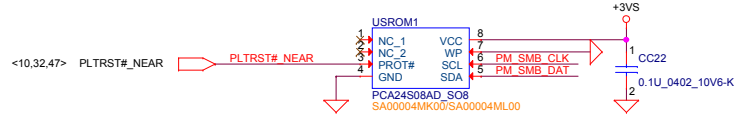


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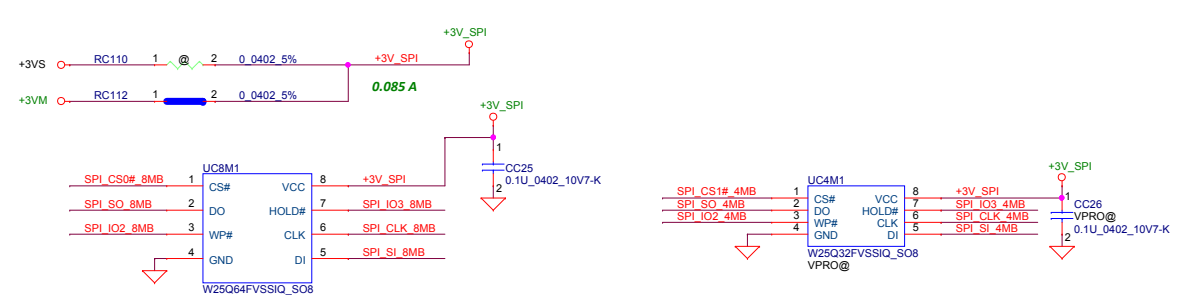




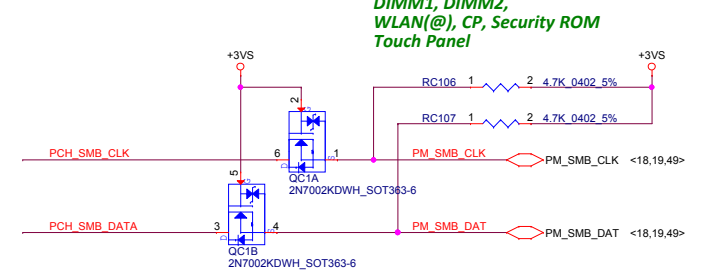
**Security ROM**



**M3 Support + Intel LAN PHY / Wireless LAN Solution**

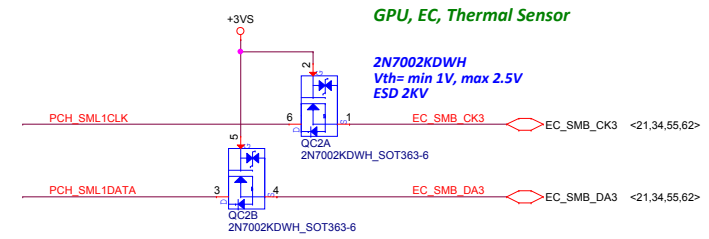


**SM Bus**



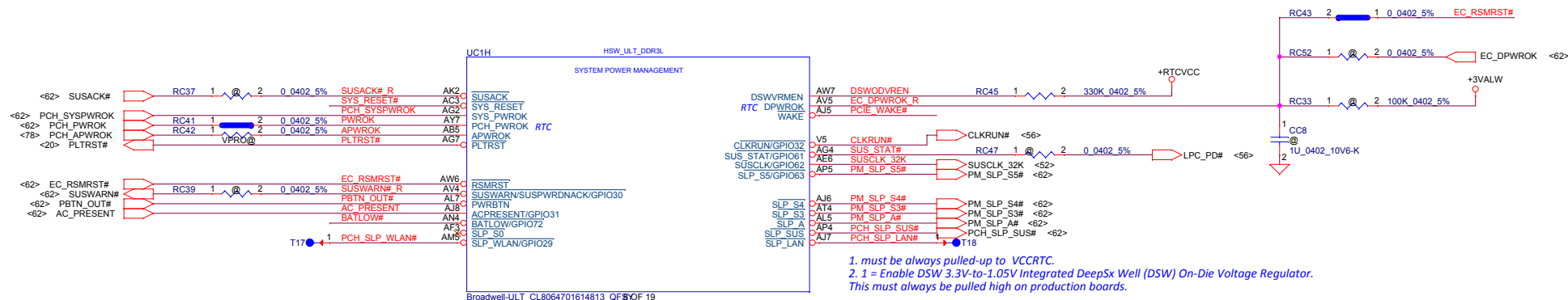
**DIMM1, DIMM2, WLAN(@), CP, Security ROM Touch Panel**

**GPU, EC, Thermal Sensor**

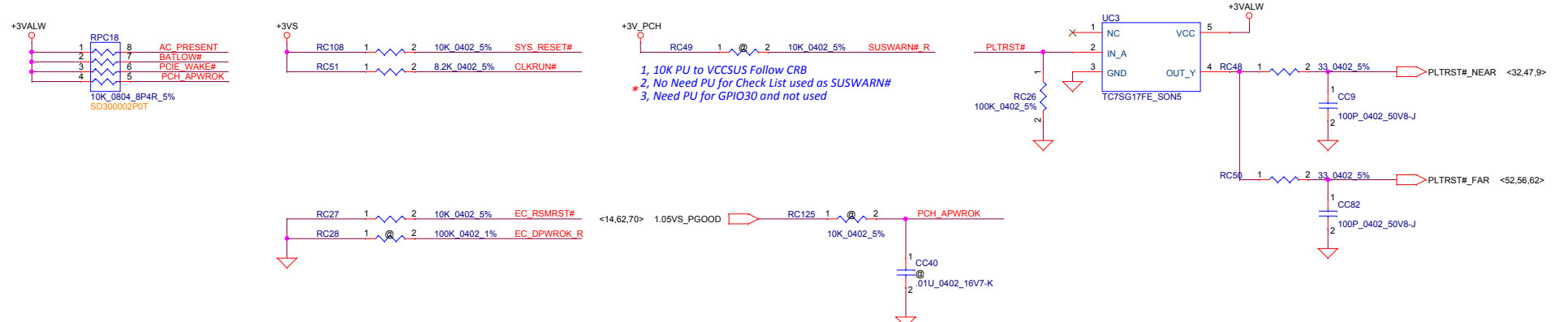


Close to SPI ROM (UC8M1).

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1. must be always pulled-up to VCCRTC.  
 2. 1 = Enable DSW 3.3V-to-1.05V Integrated DeepSx Well (DSW) On-Die Voltage Regulator.  
 This must always be pulled high on production boards.



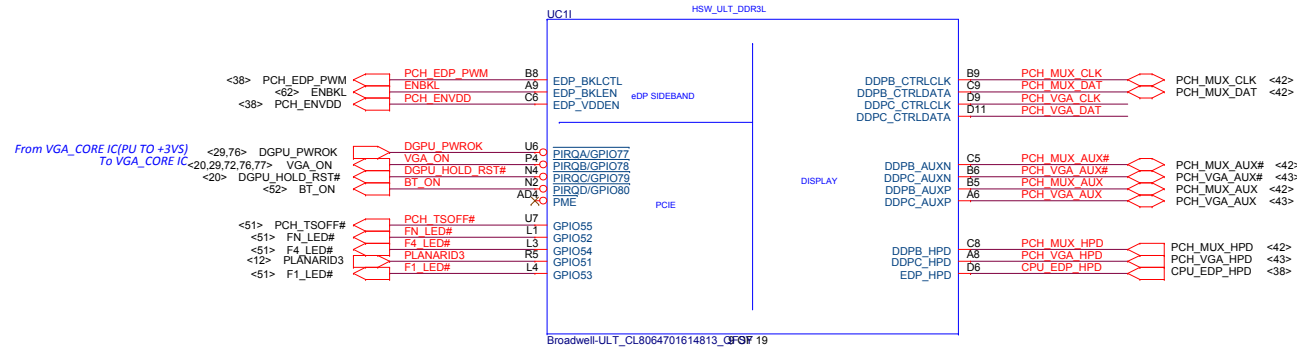
1, 10K PU to VCCSUS Follow CRB  
 2, No Need PU for Check List used as SUSWARN#  
 3, Need PU for GPIO30 and not used

SUSWARN#\_R 1 RC109 2 SUSACK#\_R 0\_0402\_5% SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit.

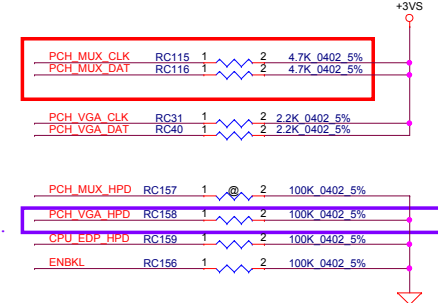
APWROK 1 RC111 2 PWRROK 0\_0402\_5% For platforms not supporting IntelR AMT it can be connected to PWRROK.

This signal can be tied to RSMRST# for platforms that do not support the Deep Sx state. RSMRST# <-> DPWROK

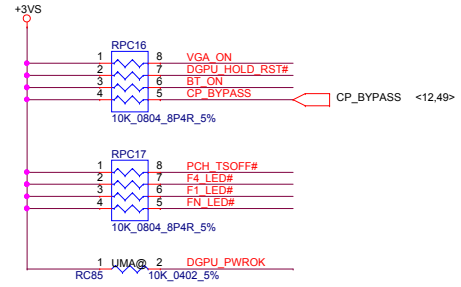
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Issued Date	2013/09/07	Deciphered Date	2014/09/07	BDW_SYS_PM			
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1. 鐵VENDOR 鐵板PU , 鐵板Vih anf Vil Tmeet SPEC value.
2. Vender fine tune recommend value.(Pass Through Mode)
3. Vendor recommend use PU 4.7K ohm. (10/1) Intel Spec is PU 2.2K ohm



After testing, check if can un-stuff.

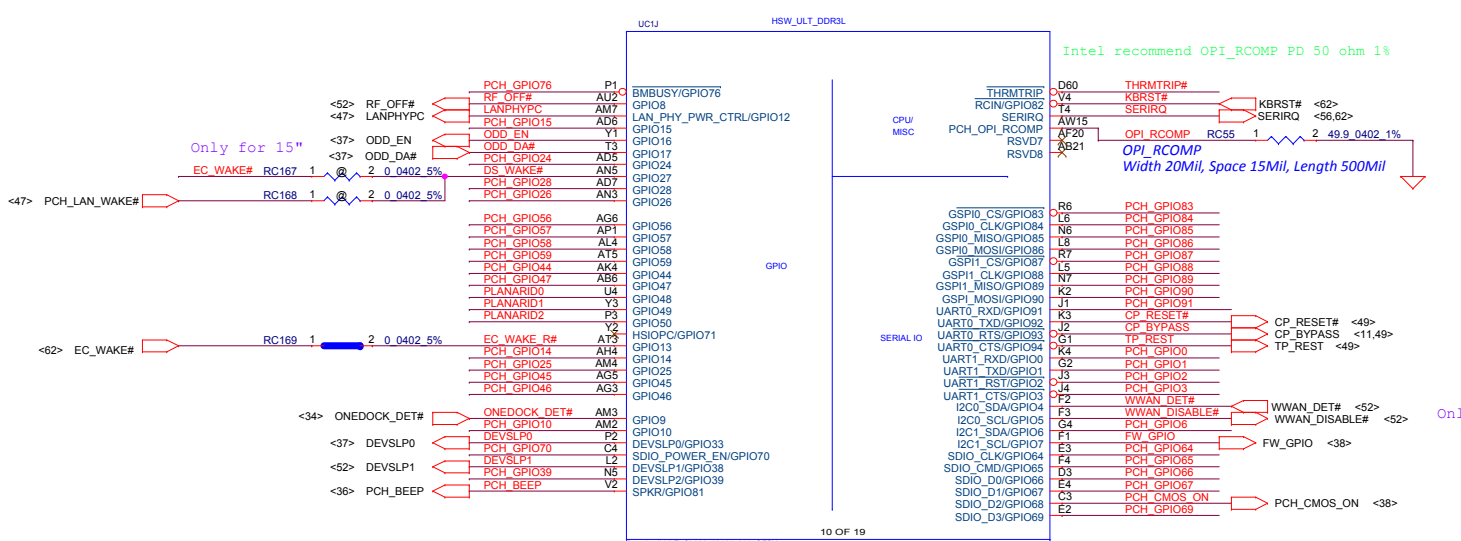


DDPB\_CTRLDATA: Port B Detected  
 DDPC\_CTRLDATA: Port C Detected

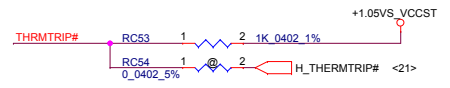
\* 1: Port B or C is detected  
 0: Port B or C is not detected

Internal PD 15K~40K, nominal 20K

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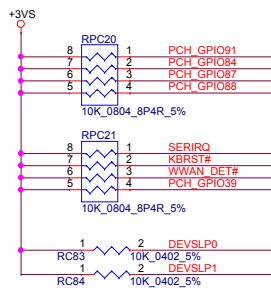
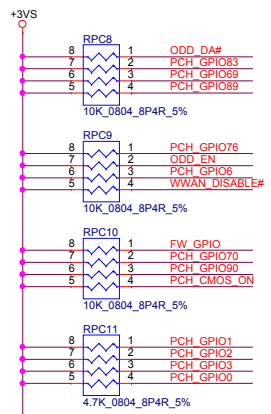
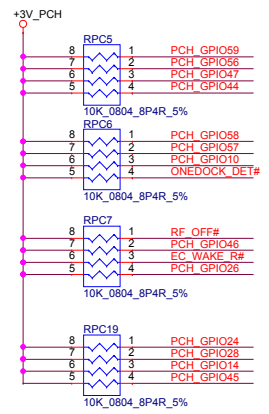
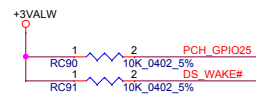
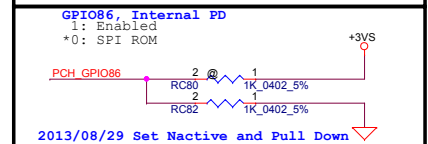
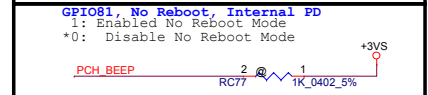
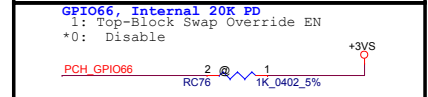
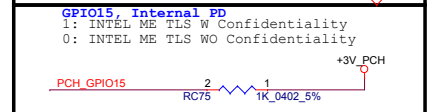
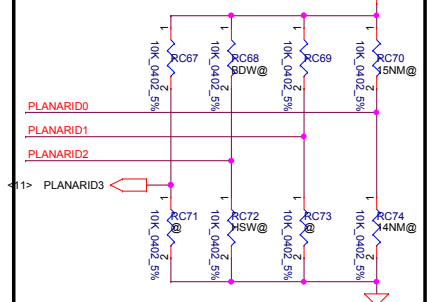


	SATA Port
DEVSLP0	SATA Port 0
DEVSLP1	SATA Port 1



Only for 15"

Planar ID			
PLANARID0 (GPIO48)	GPIO18	PLANARID2 (GPIO50)	PLANARID3 (GPIO51)
0	14"	UMA	HSW
1	15"	OPT	BDW



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		2014/09/07

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Title	<b>BDW_GPIO/SIO</b>
Document Number	<b>AIT1 NM-A221</b>
Rev	1.0
Date	Thursday, November 08, 2014 1 Sheet of 81

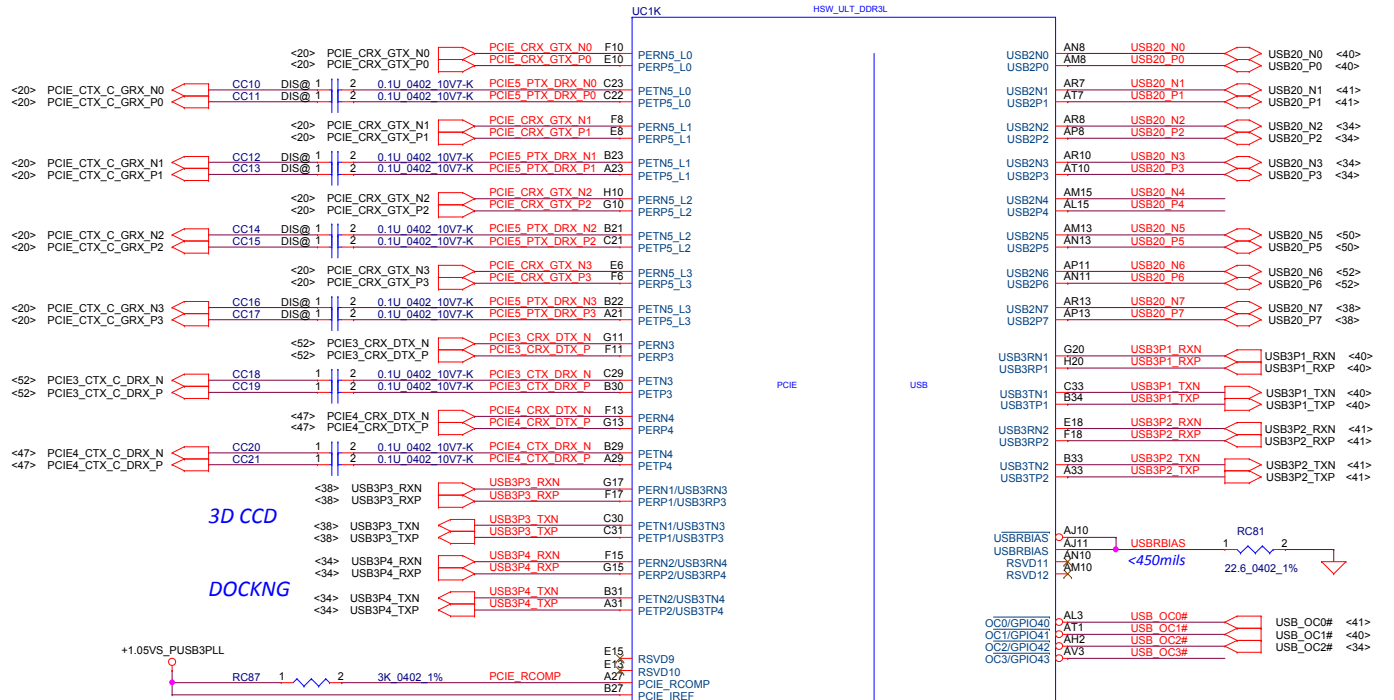
GPU

WLAN

LAN

3D CCD

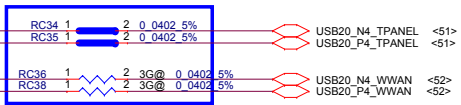
DOCKNG



+1.05VS\_PUSB3PLL

PCIE\_RCOMP&PCIE\_IREF (Shared with DMI)  
Width 20Mil, Space 15Mil, Length 500Mil

Broadwell-ULT\_CL8064701614813\_QF3Y OF 19



Close to device side

On Board (Back)

On Board /Charge Port (Front)

Sub/B

DOCKING

TOUCH PANEL/WWAN

FPR

BT

CAMERA

On Board (Back)

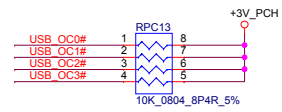
On Board (Front)

USBRBIAS/USBRBIAS#

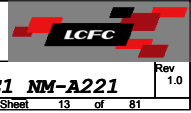
- 1. trace length and no longer than 450 mils to resistor.
- 2. Avoid routing next to clock pins or under stitching capacitors.
- Recommended minimum spacing to other signal traces is 15 mils (0.381 mm).

On Board Front (Charger Port)  
On Board Back  
Docking board (USB2)

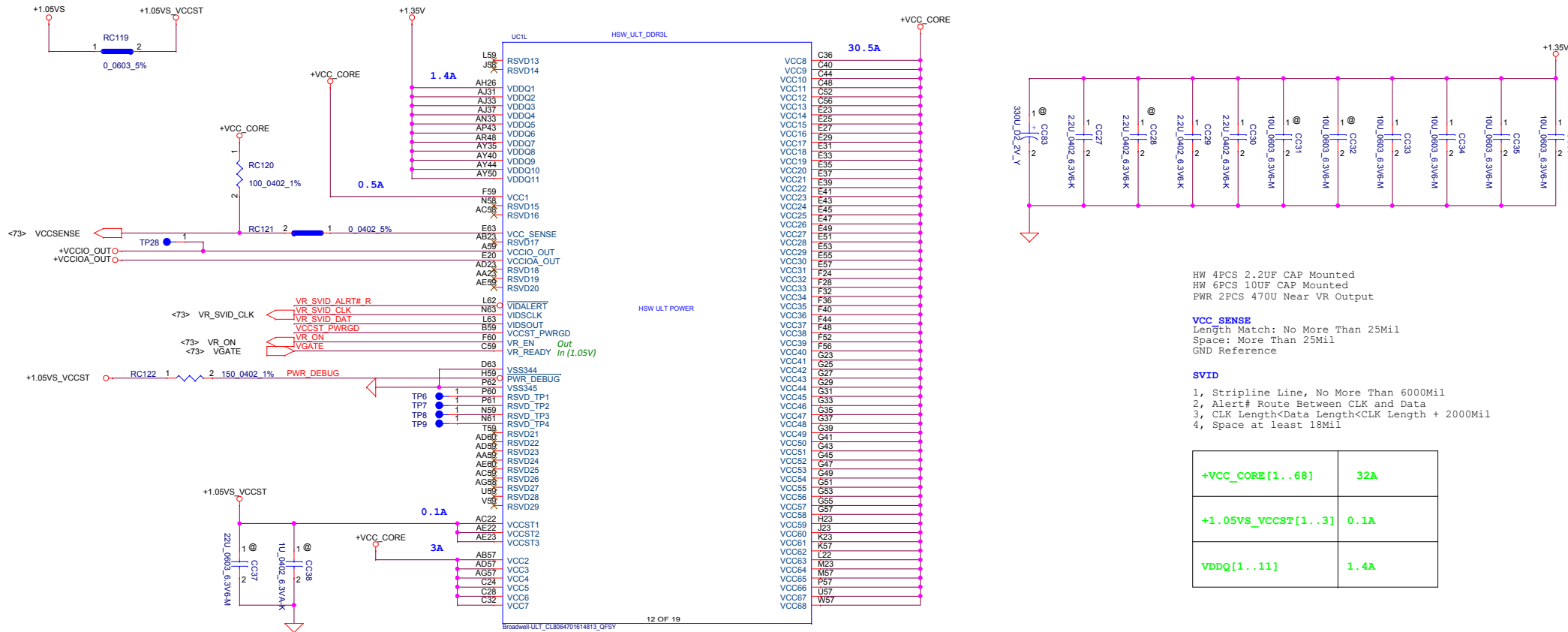
	USB3.0 Port NO.	USB2.0 Port NO.
USB_OC0#	Port 2	Port 1
USB_OC1#	Port 1	Port 0
USB_OC2#	Unused.	Port 2
USB_OC3#	Unused.	Unused.



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1	BDW_PCIE/USB BUS	Thursday, November 08, 2014	1.0



# Haswell MCP (Power)



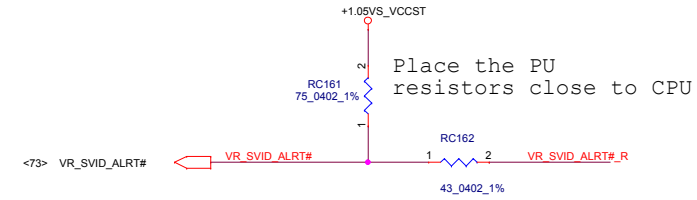
HW 4PCS 2.2UF CAP Mounted  
 HW 6PCS 10UF CAP Mounted  
 PWR 2PCS 470U Near VR Output

**VCC SENSE**  
 Length Match: No More Than 25Mil  
 Space: More Than 25Mil  
 GND Reference

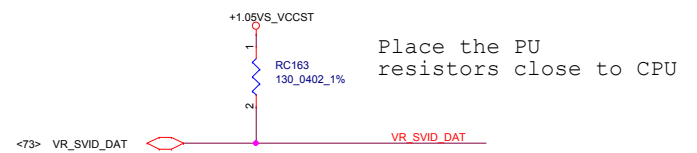
**SVID**  
 1, Stripline Line, No More Than 6000Mil  
 2, Alert# Route Between CLK and Data  
 3, CLK Length < Data Length < CLK Length + 2000Mil  
 4, Space at least 18Mil

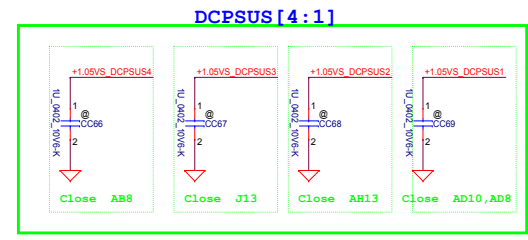
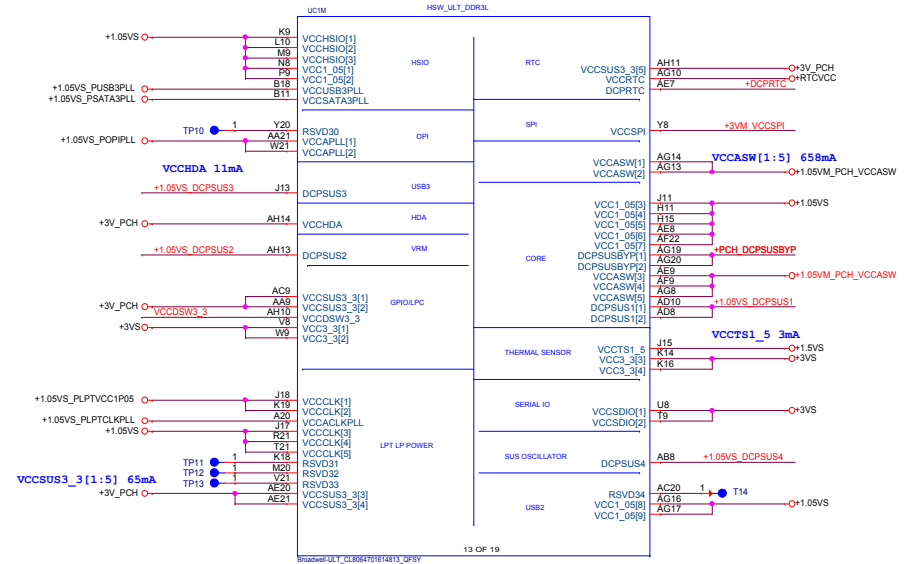
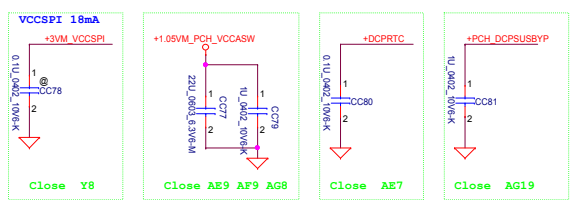
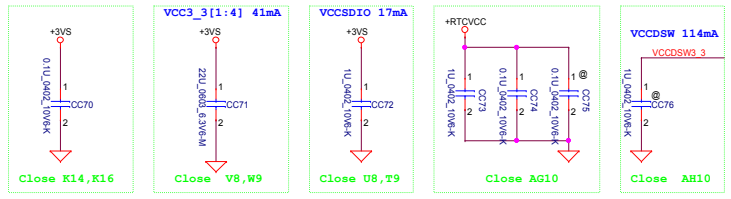
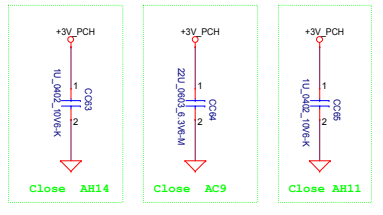
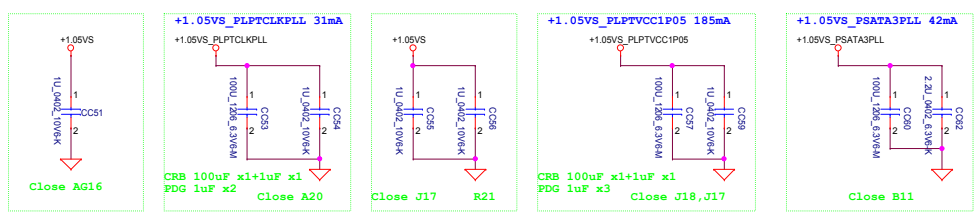
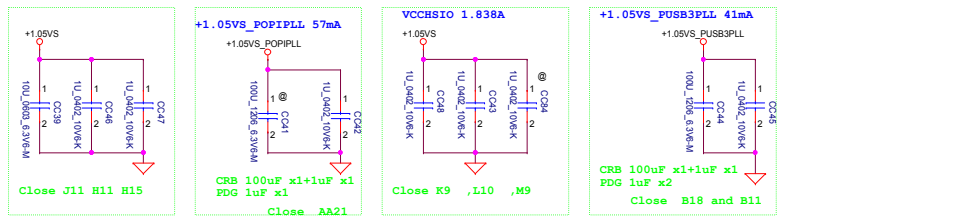
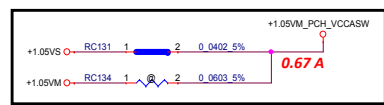
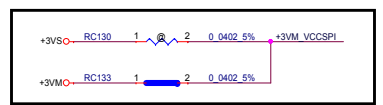
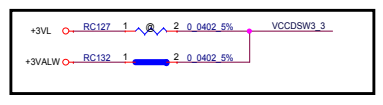
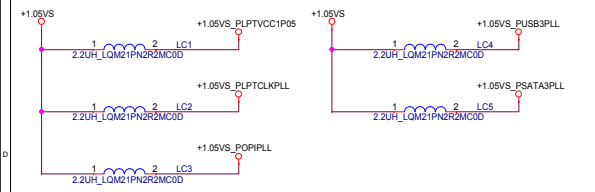
+VCC_CORE[1..68]	32A
+1.05VS_VCCST[1..3]	0.1A
VDDQ[1..11]	1.4A

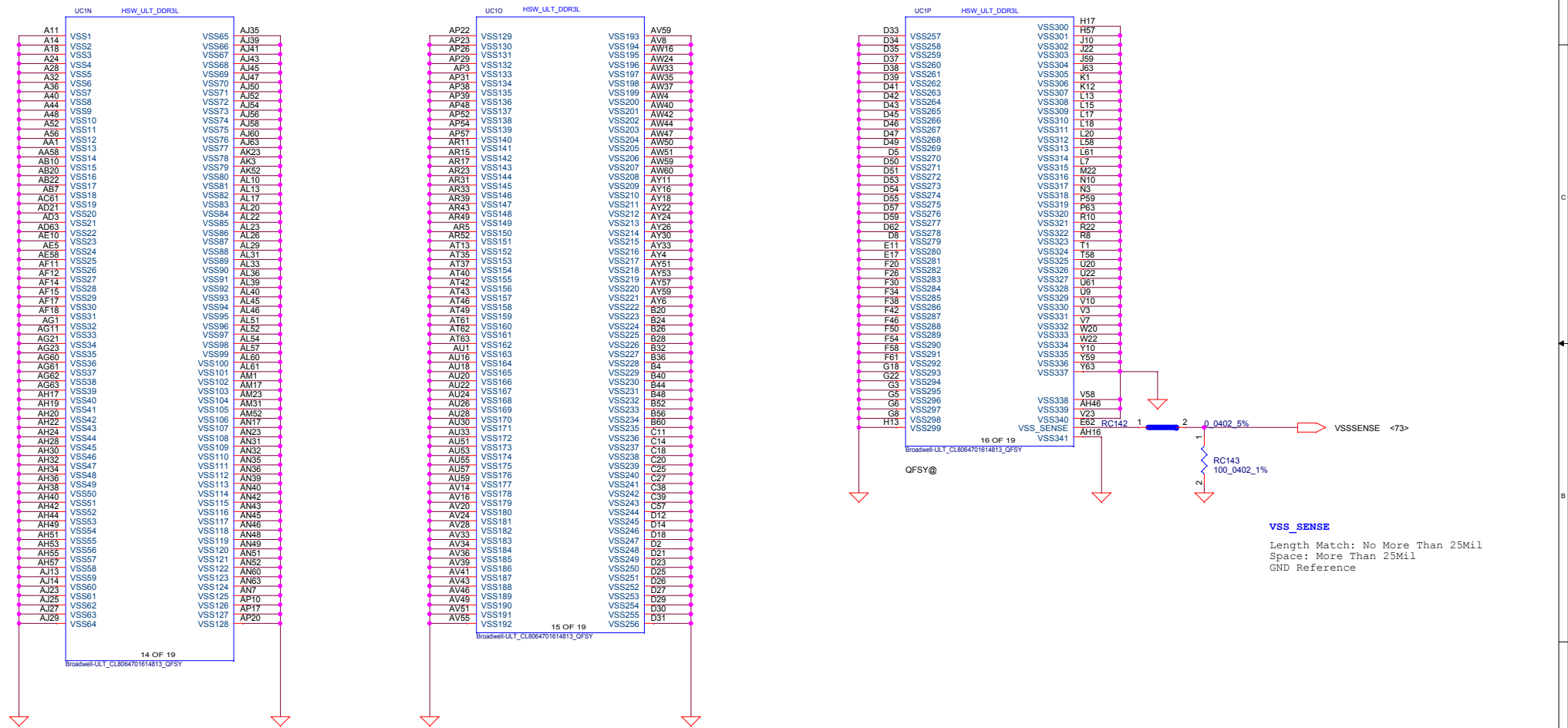
## SVID ALERT




## SVID DATA

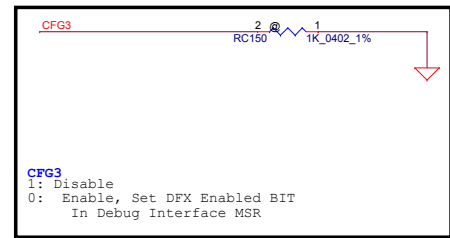
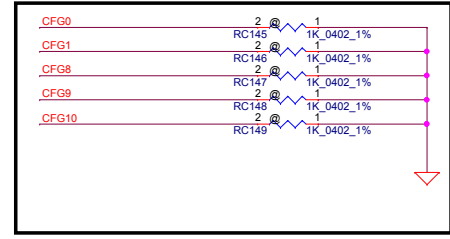
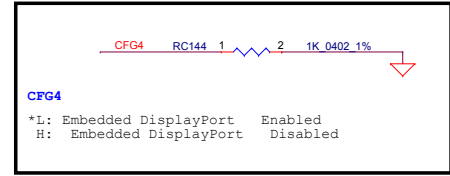
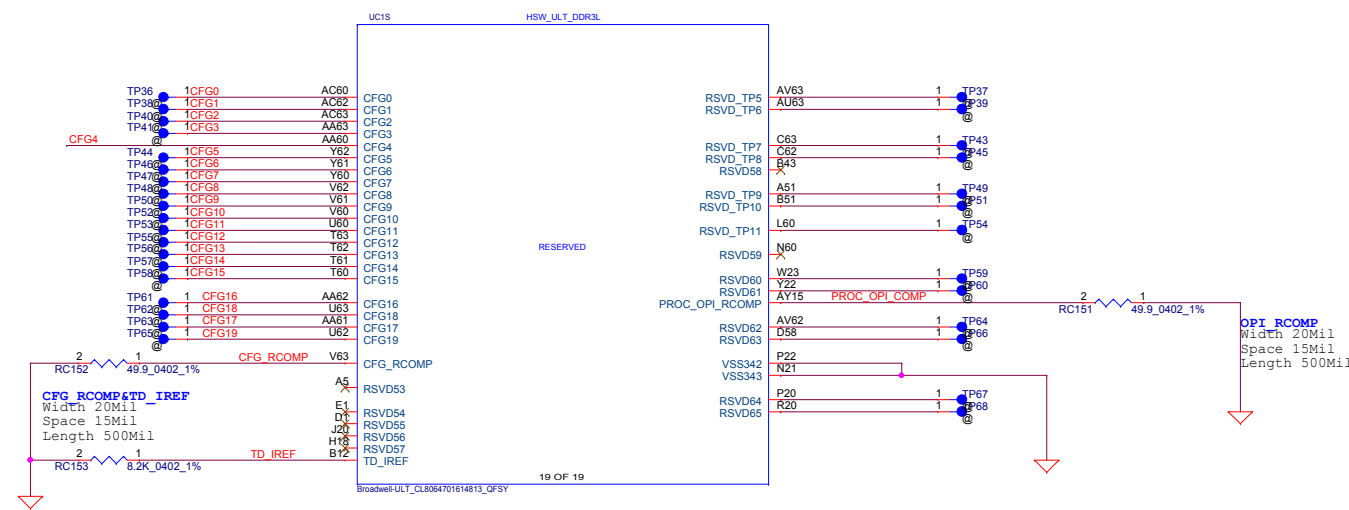
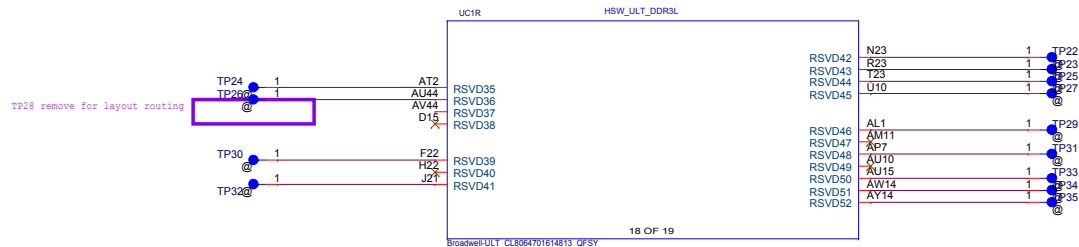
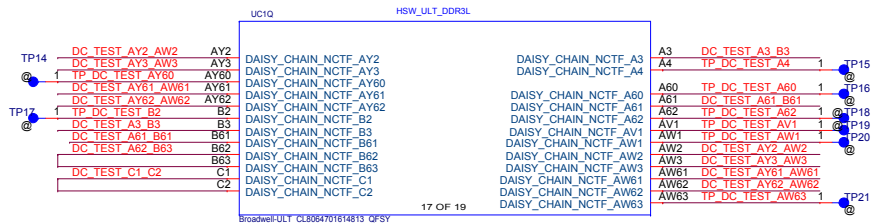




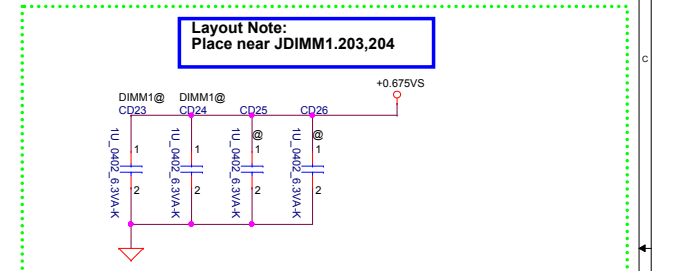
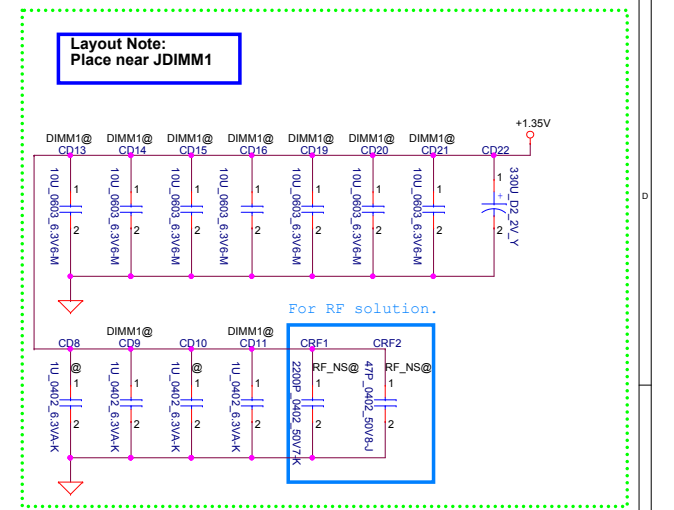
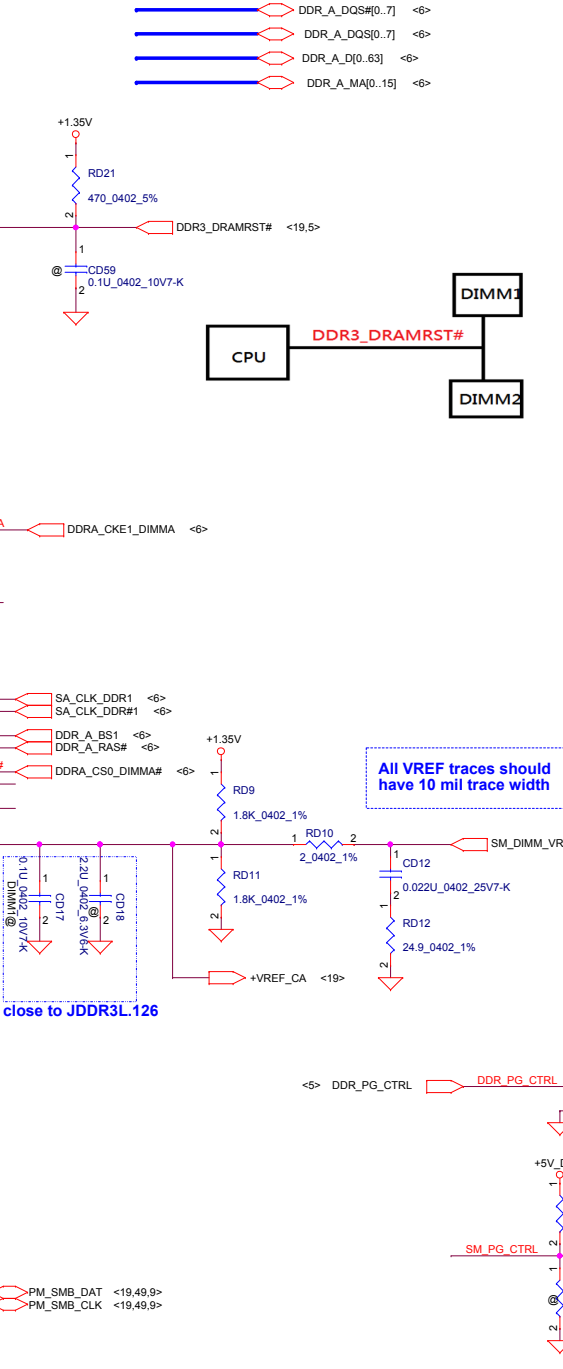
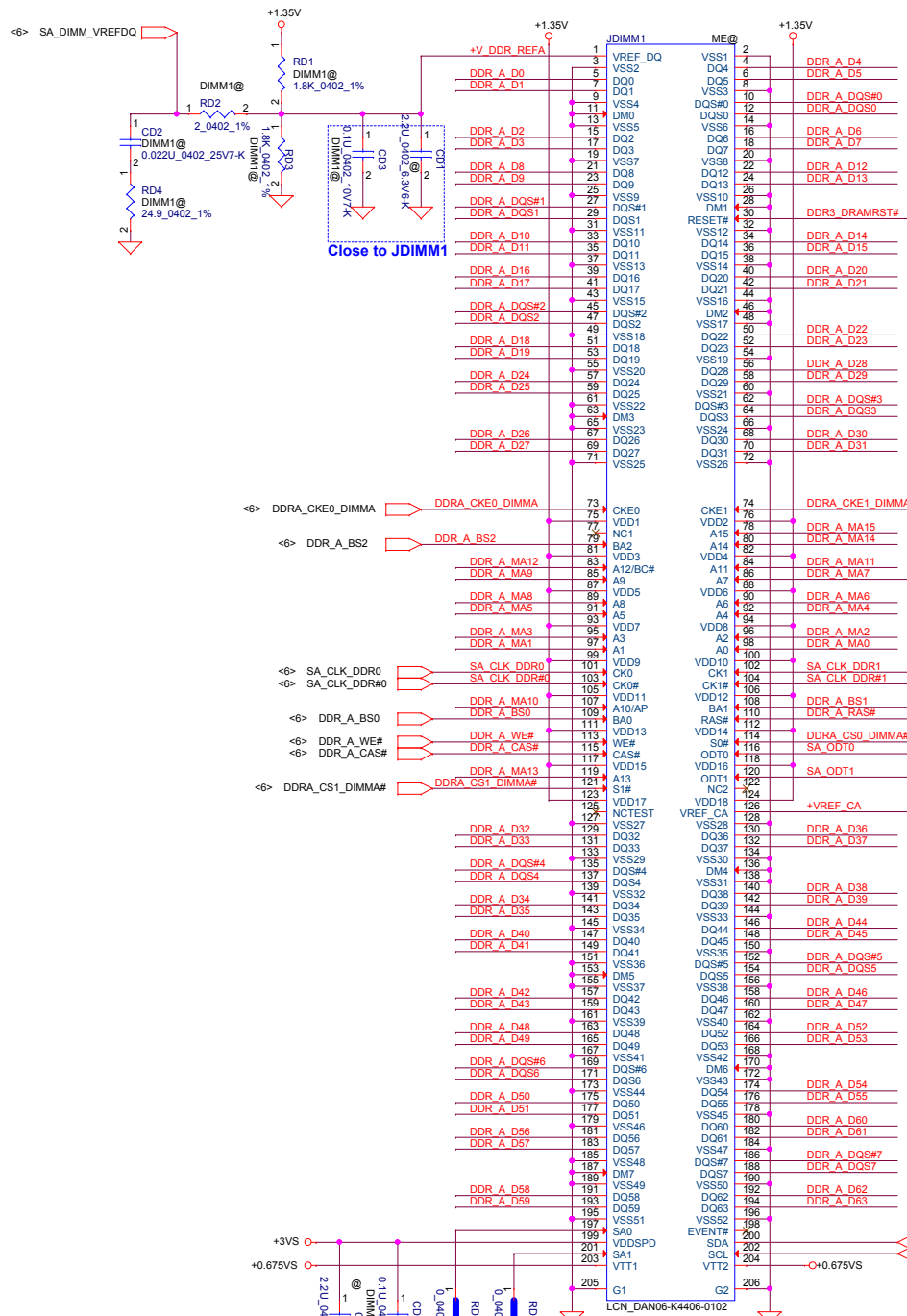


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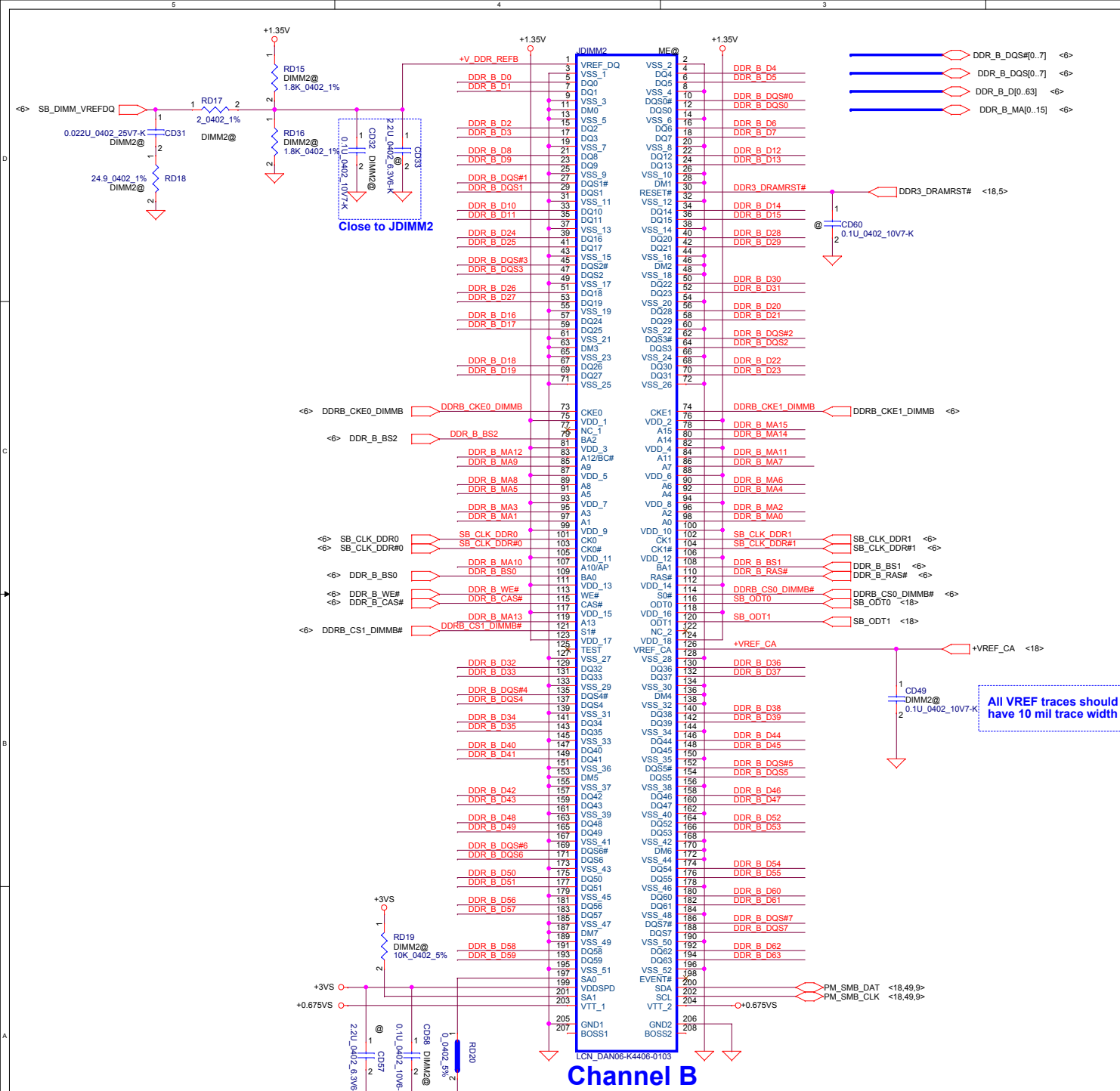
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All VREF traces should have 10 mil trace width

## Channel A

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<Address: SA1:SA0=10>  
DIMM\_2 STD H:4mm

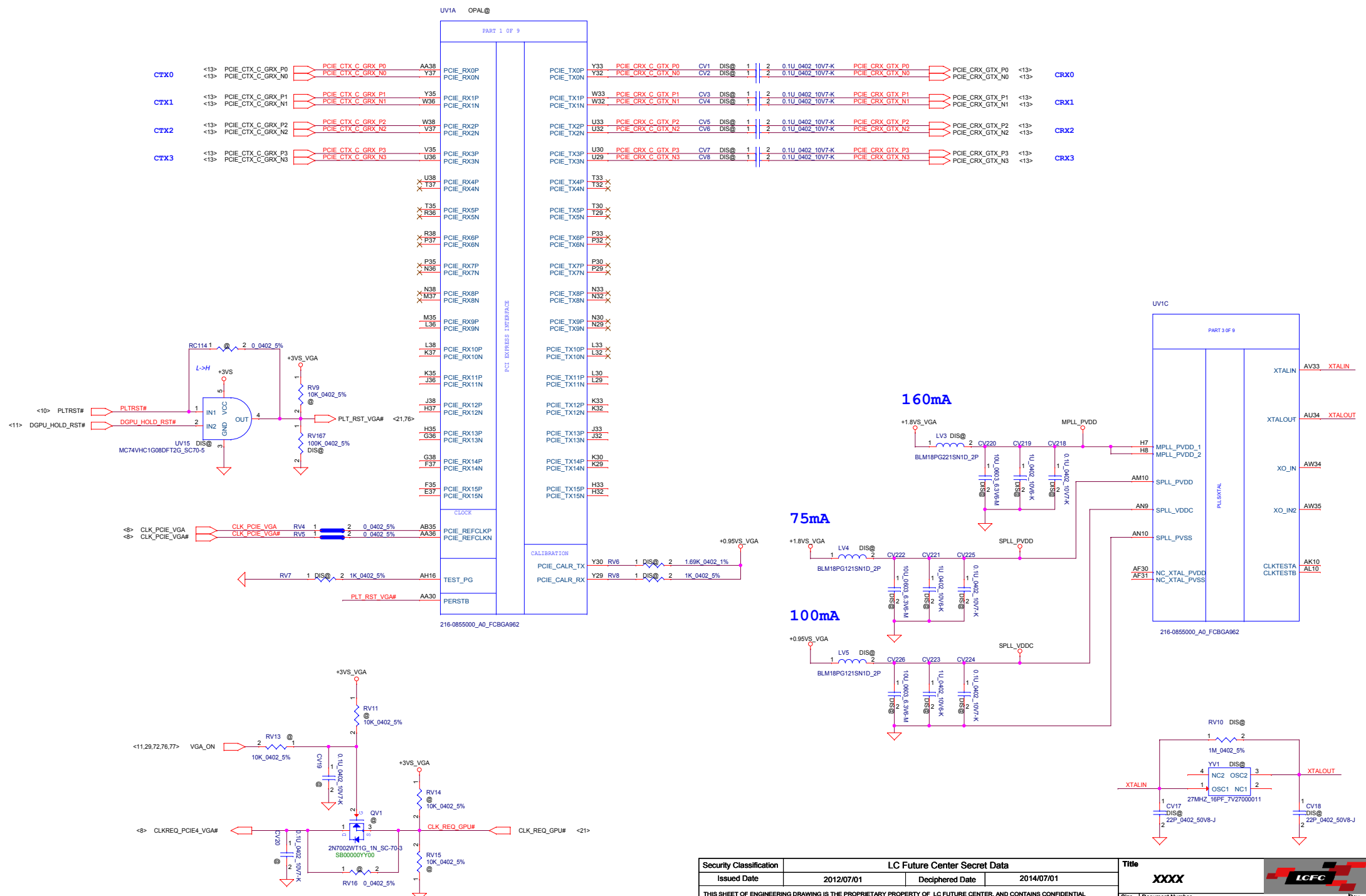
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**XXXX**

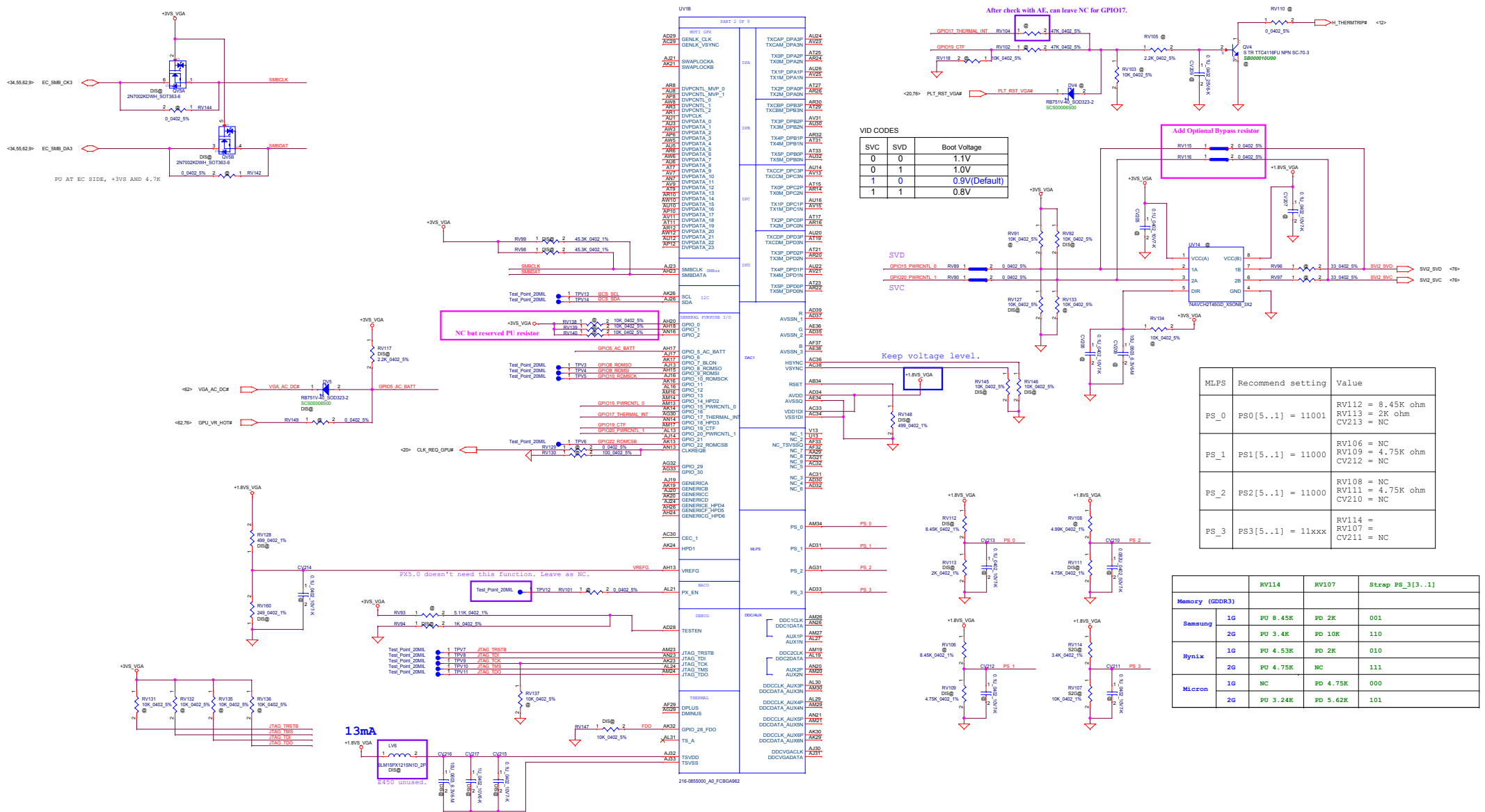
**LCFC**

**DATE1 NM-A221**

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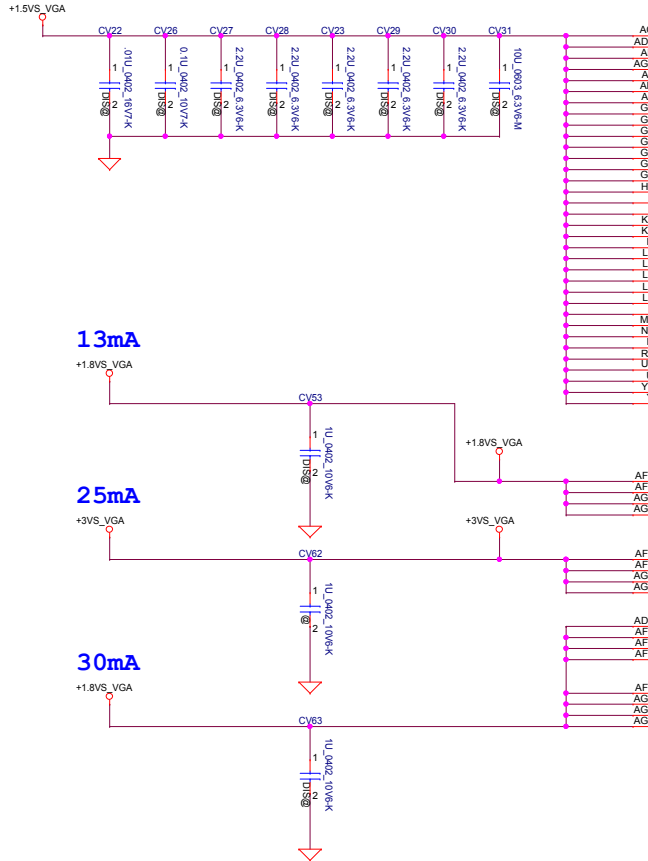
VID CODES

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V(Default)
1	1	0.8V

MLPS	Recommend setting	Value
PS_0	FS0[5..1] = 11001	RV112 = 8.45k ohm RV113 = 2K ohm CV213 = NC
PS_1	FS1[5..1] = 11000	RV106 = NC RV109 = 4.75K ohm CV212 = NC
PS_2	FS2[5..1] = 11000	RV108 = NC RV111 = 4.75K ohm CV210 = NC
PS_3	FS3[5..1] = 11xxx	RV114 = RV107 = CV211 = NC

	RV114	RV107	Strap_PS_3[3..1]
Memory (GDDR3)			
Samsung	1G	PU 8.45K PD 2K	001
	2G	PU 3.4K PD 10K	110
Hynix	1G	PU 4.53K PD 2K	010
	2G	PU 4.75K NC	111
Micron	1G	NC PD 4.75K	000
	2G	PU 3.24K PD 5.62K	101

1.5A



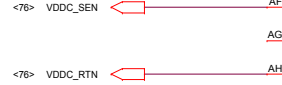
1.3mA



25mA



30mA



UV1E

MEM I/O PART 5 OF 9

AC7	VDDR1_1
AD11	VDDR1_2
AF7	VDDR1_3
AG10	VDDR1_4
AJ7	VDDR1_5
AK1	VDDR1_6
AL9	VDDR1_7
G11	VDDR1_8
G14	VDDR1_9
G17	VDDR1_10
G20	VDDR1_11
G23	VDDR1_12
G26	VDDR1_13
G29	VDDR1_14
H10	VDDR1_15
J9	VDDR1_16
K11	VDDR1_17
K13	VDDR1_18
K6	VDDR1_19
L12	VDDR1_20
L21	VDDR1_21
L23	VDDR1_22
L26	VDDR1_23
L7	VDDR1_24
M11	VDDR1_25
M12	VDDR1_26
N11	VDDR1_27
P7	VDDR1_28
R11	VDDR1_29
R12	VDDR1_30
U11	VDDR1_31
U7	VDDR1_32
Y11	VDDR1_33
Y7	VDDR1_34

LEVEL TRANSLATION

AF28	VDDCT_1
AG28	VDDCT_2
AG27	VDDCT_3
AG24	VDDCT_4

I/O

AF23	VDDR3_1
AF24	VDDR3_2
AG23	VDDR3_3
AG24	VDDR3_4

DIV

AD12	VDDR4_1
AF11	VDDR4_2
AF12	VDDR4_3
AF13	VDDR4_4
AF15	VDDR4_5
AG11	VDDR4_6
AG13	VDDR4_7
AG15	VDDR4_8

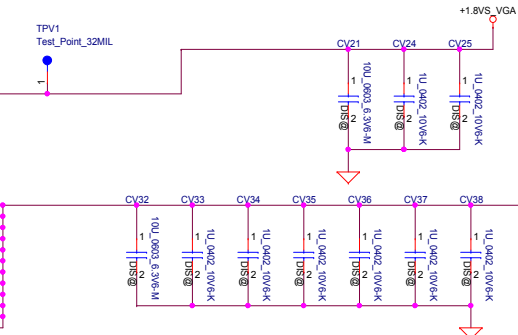
VOLTAGE SENSE

ISOLATED CORE I/O

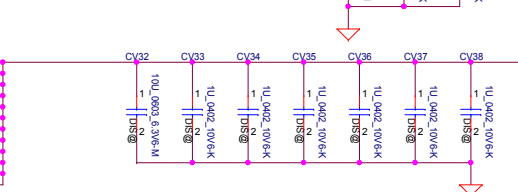
VDDCI_1	AA13
VDDCI_2	AB13
VDDCI_3	AC12
VDDCI_4	AC15
VDDCI_5	AD13
VDDCI_6	AD16
VDDCI_7	M15
VDDCI_8	M16
VDDCI_9	M18
VDDCI_10	M23
VDDCI_11	N13
VDDCI_12	N15
VDDCI_13	N17
VDDCI_14	N20
VDDCI_15	N22
VDDCI_16	R12
VDDCI_17	R13
VDDCI_18	R16
VDDCI_19	T12
VDDCI_20	T15
VDDCI_21	V15
VDDCI_22	Y13

216-0855000\_A0\_FCBGA962

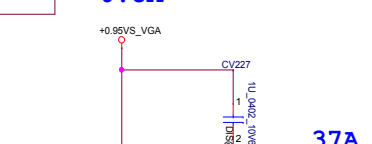
100mA



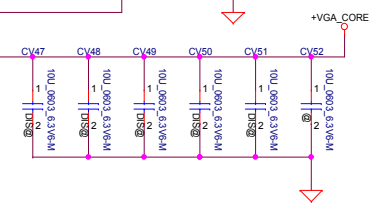
1A



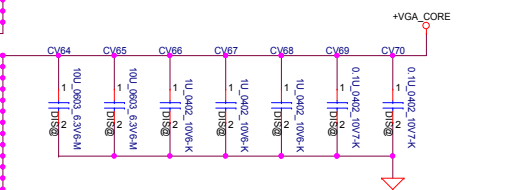
0.8A



37A

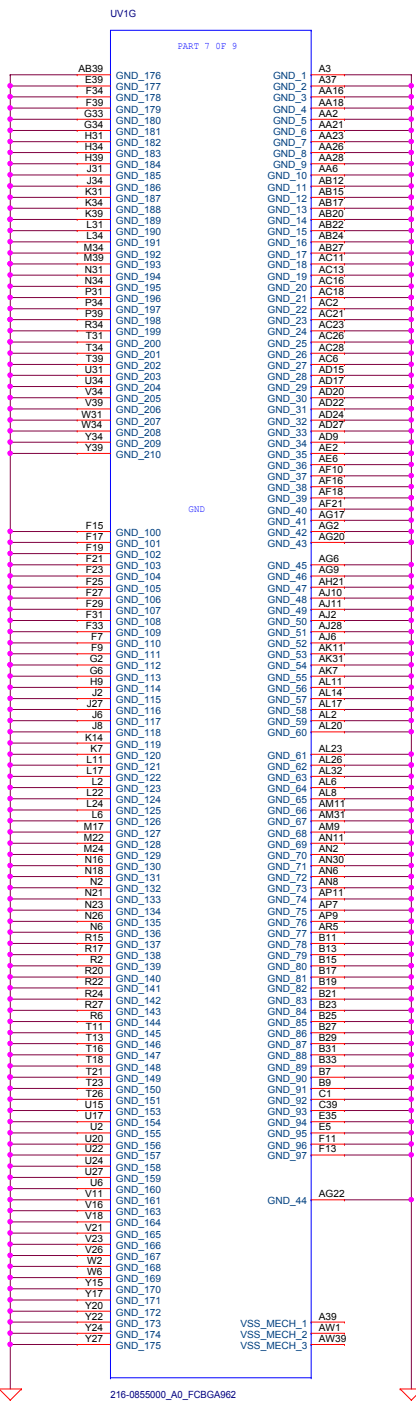


37A



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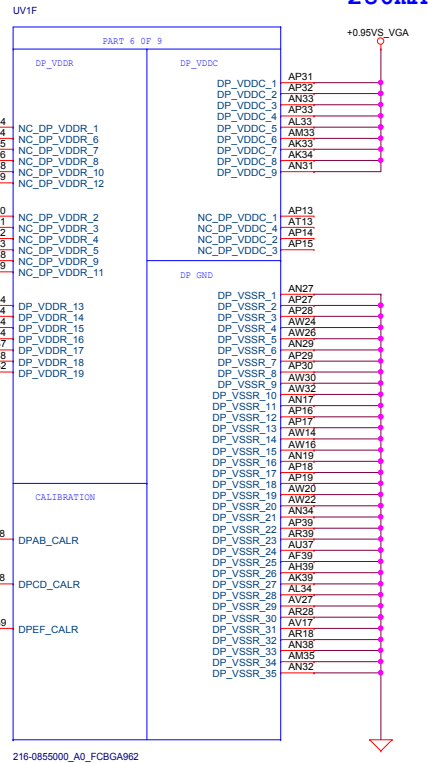
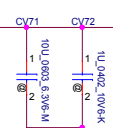
216-0855000\_A0\_FCBGA962

VSS\_MECH\_1  
VSS\_MECH\_2  
VSS\_MECH\_3

A39  
AW1  
AW39

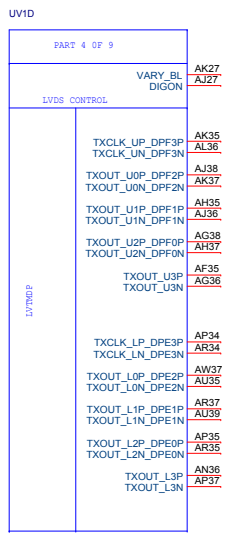
237mA

+1.8VS\_VGA



280mA

+0.85VS\_VGA



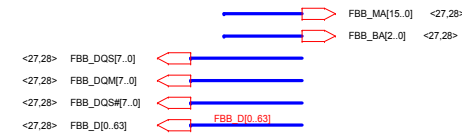
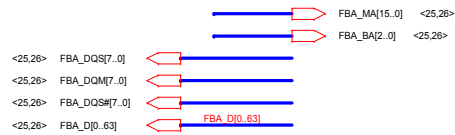
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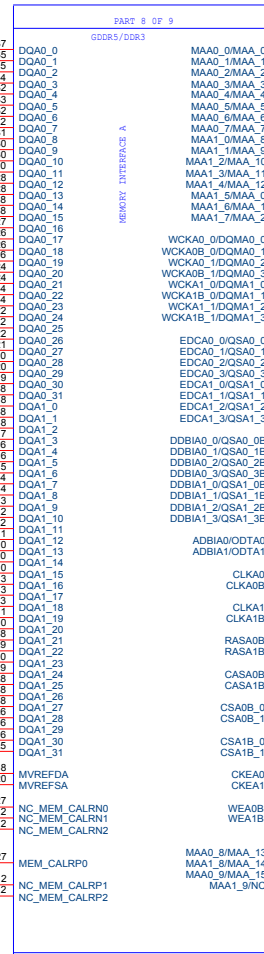


ATE1 NM-A221

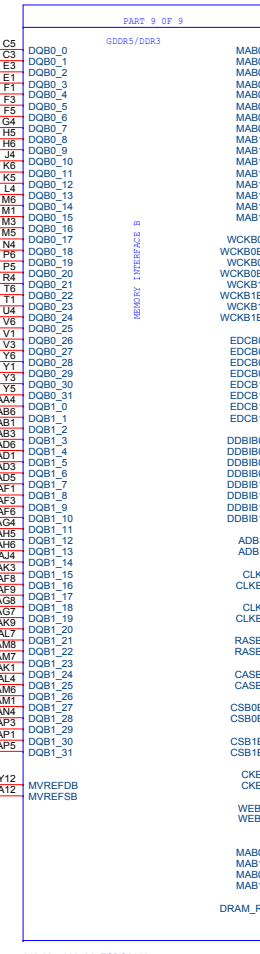




UV1H

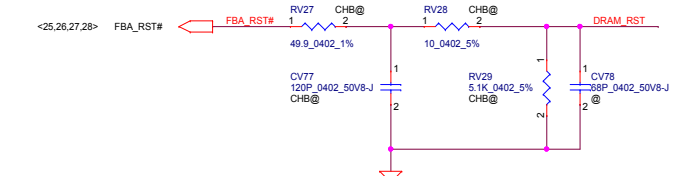
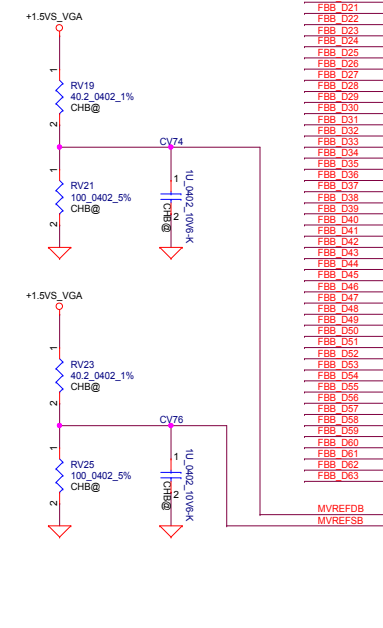
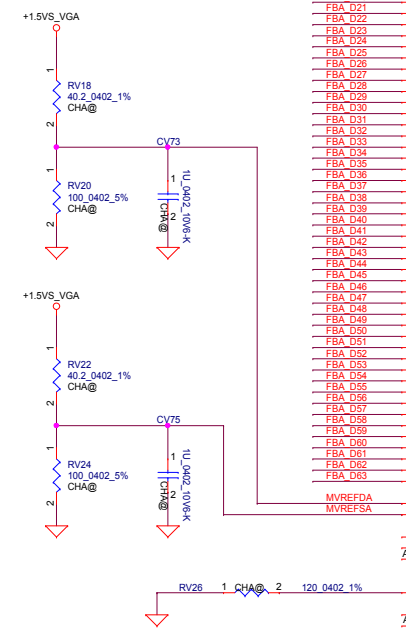


UV1I



216-0855000\_A0\_FCBGA962

216-0855000\_A0\_FCBGA962

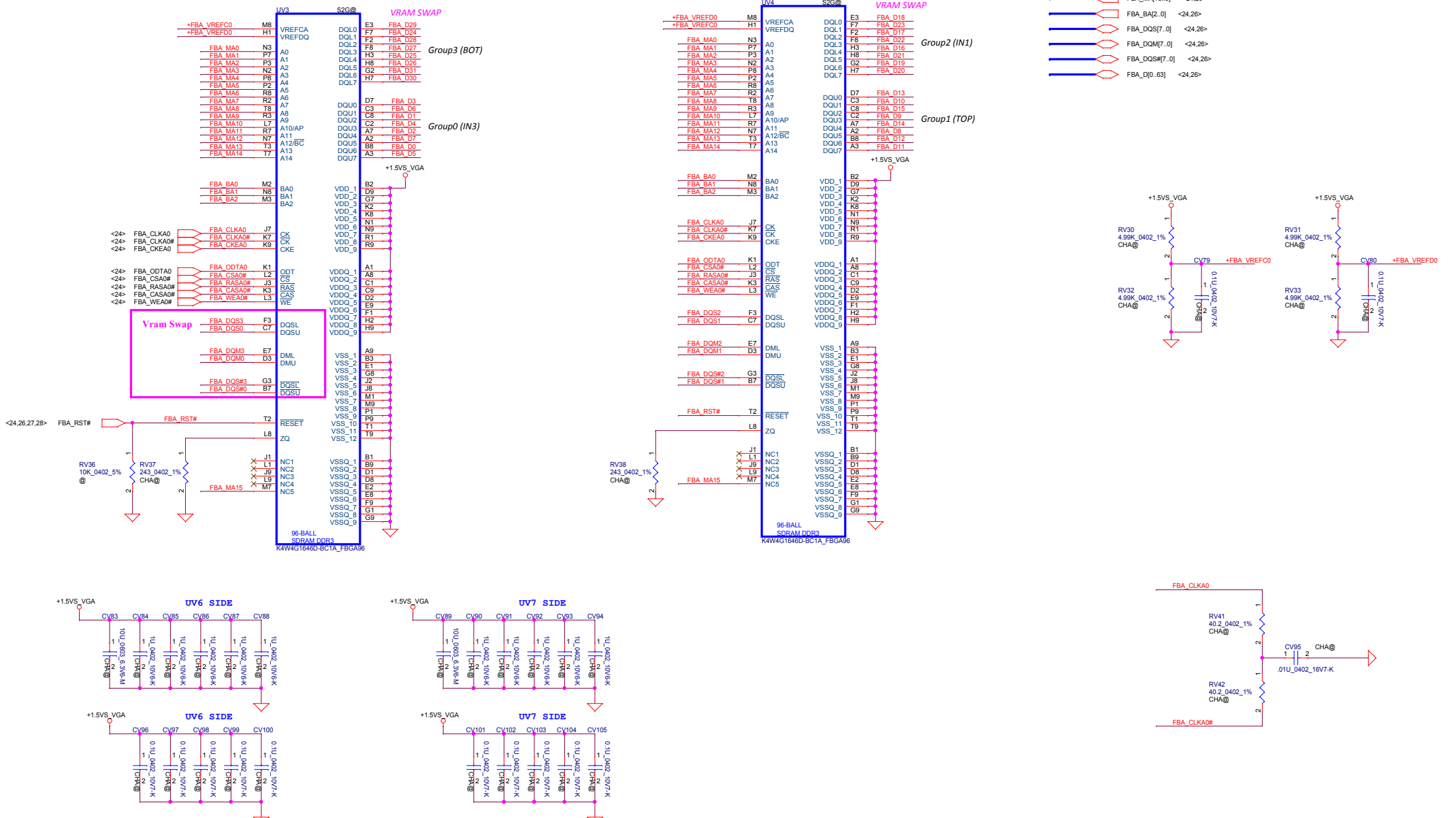


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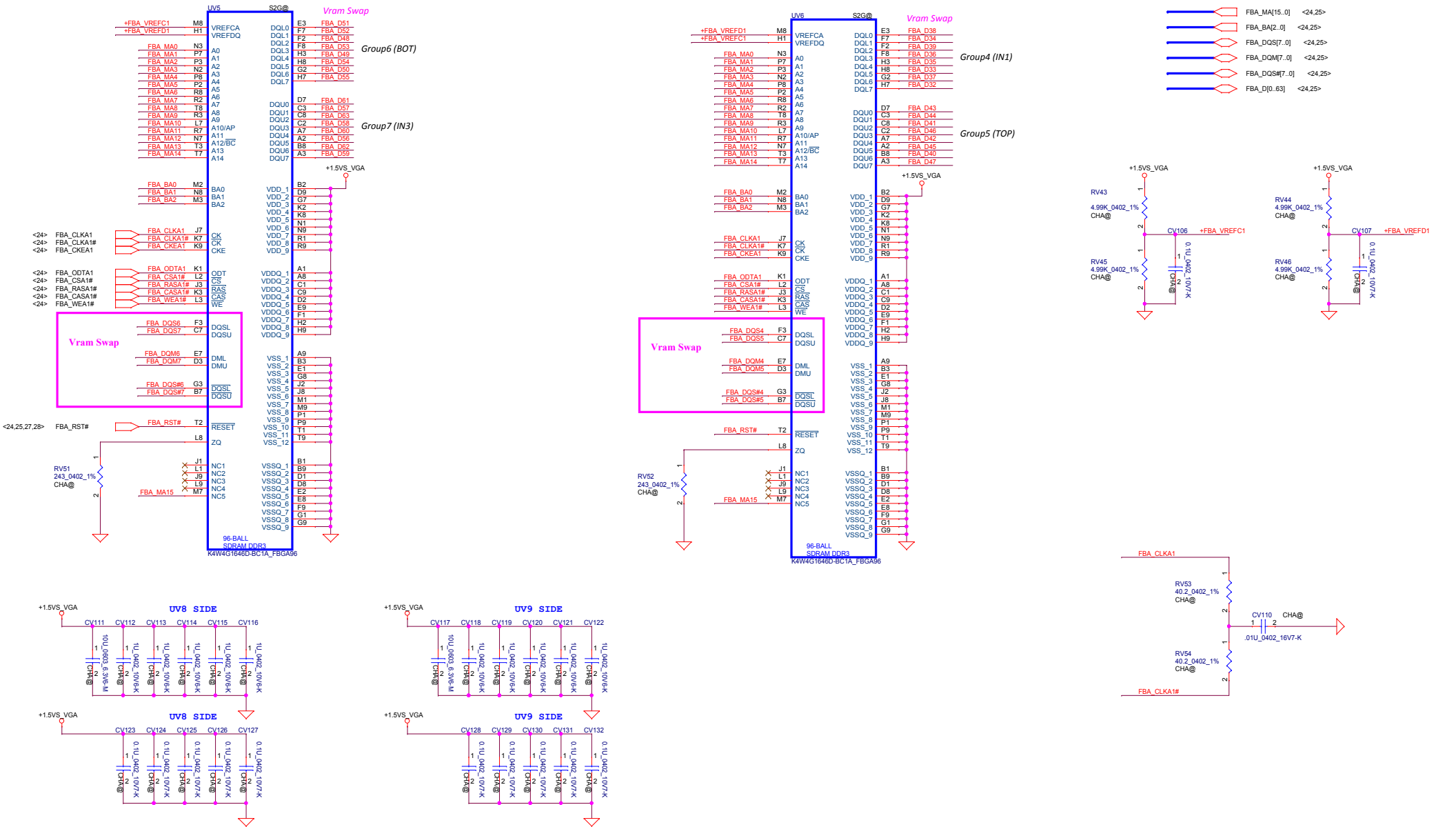


# Memory Partition A - Lower 32 bits

Change all VRAM footprint to MT41K256M16HA107\_FBGA96P-A39P

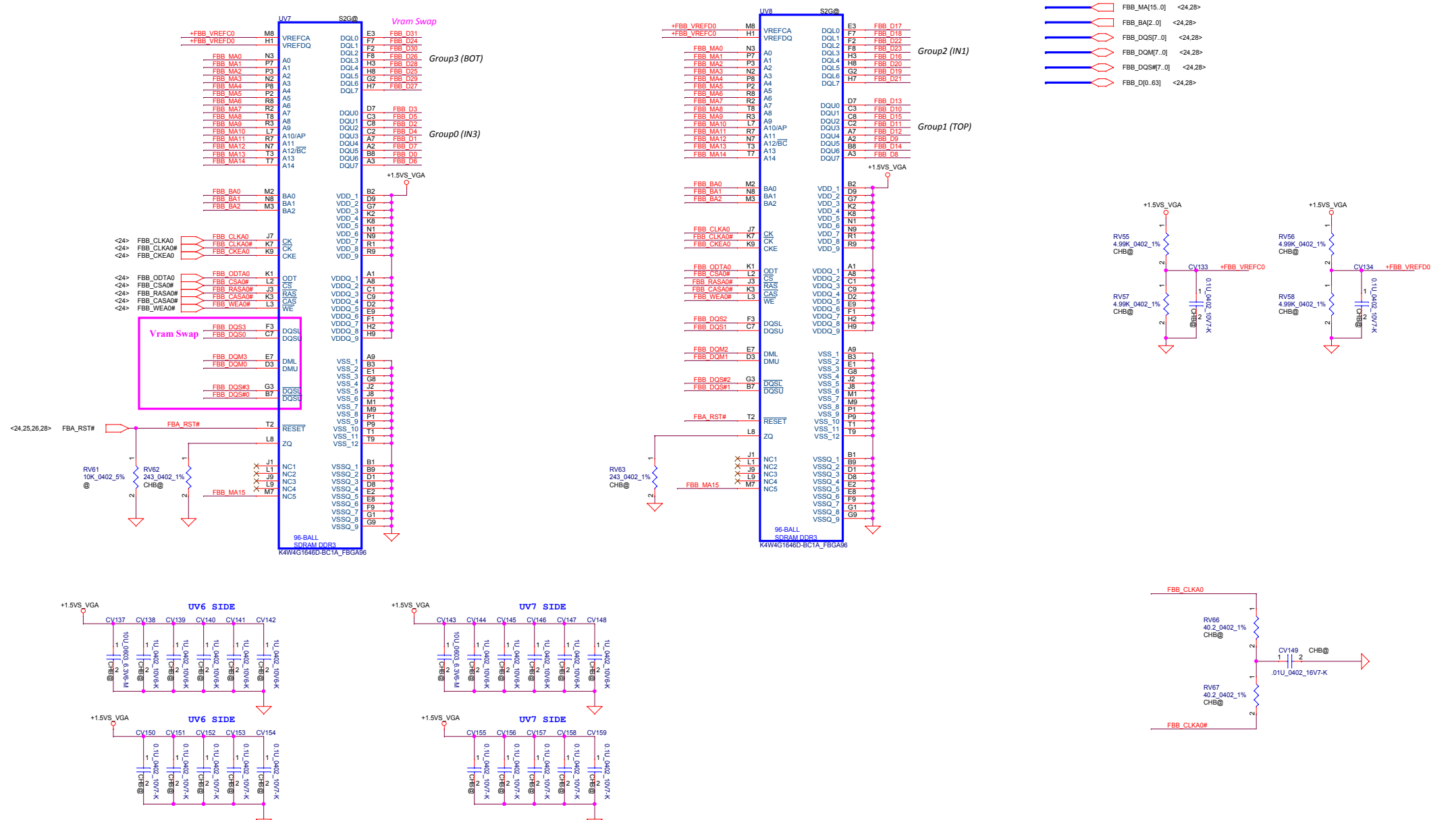


# Memory Partition A - Upper 32 bits



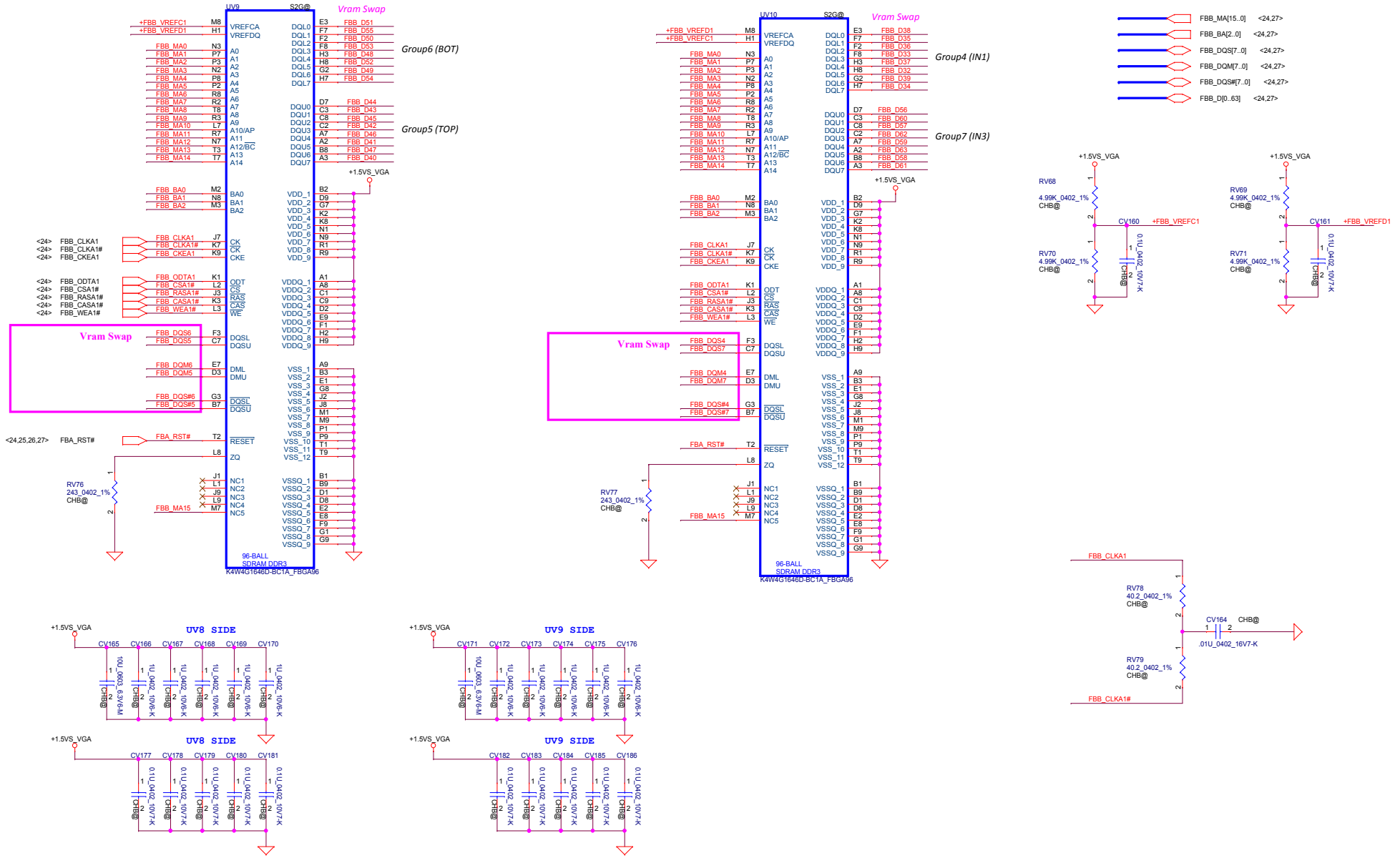
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# Memory Partition A - Lower 32 bits

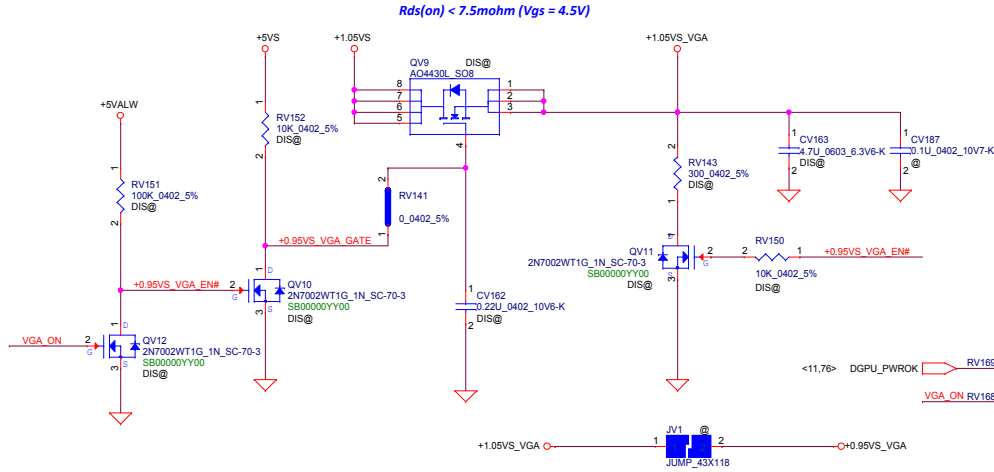


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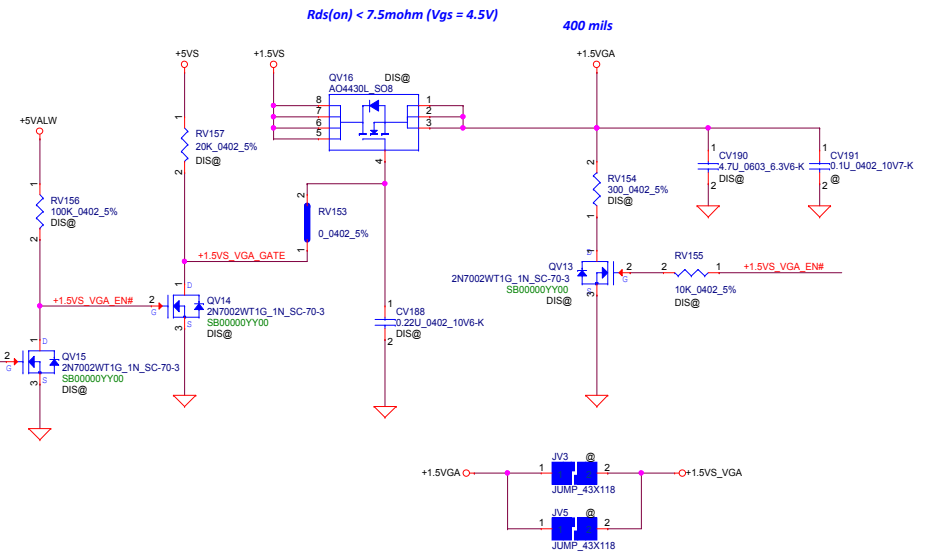
# Memory Partition A - Upper 32 bits



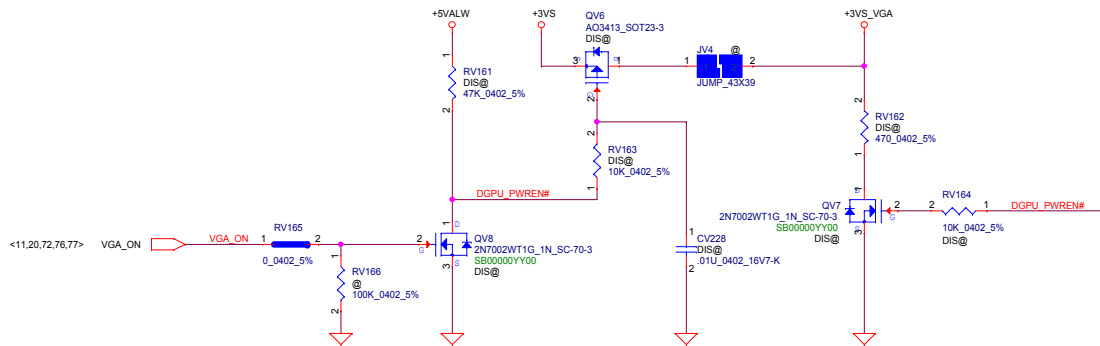
**+1.05VS to +0.95VS\_VGA**




**+1.5VS to +1.5VS\_VGA**




**+3VS to +3VS\_VGA**




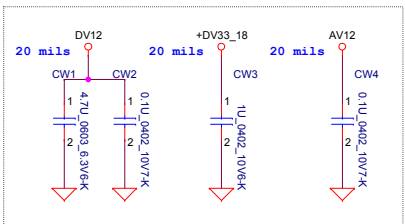
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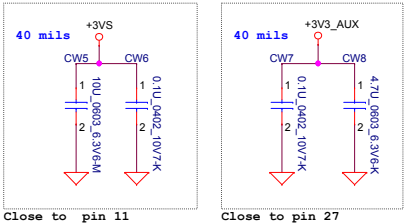
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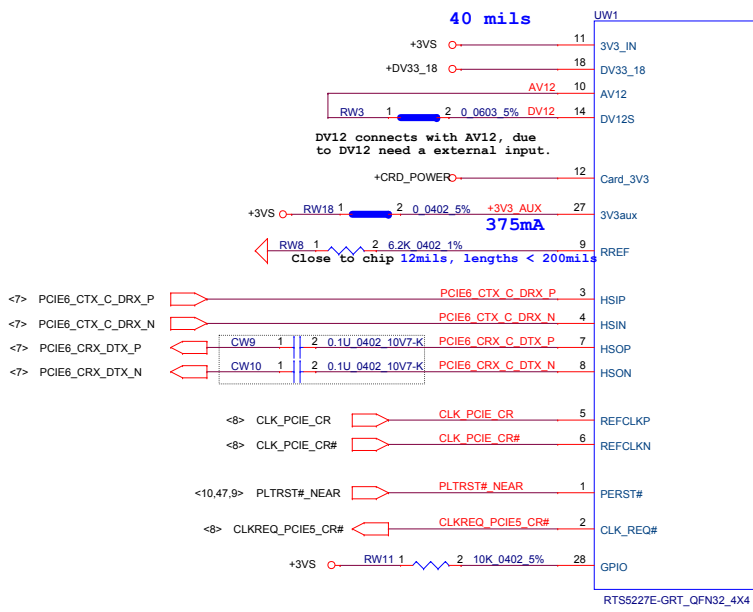


All of cap. close to chip



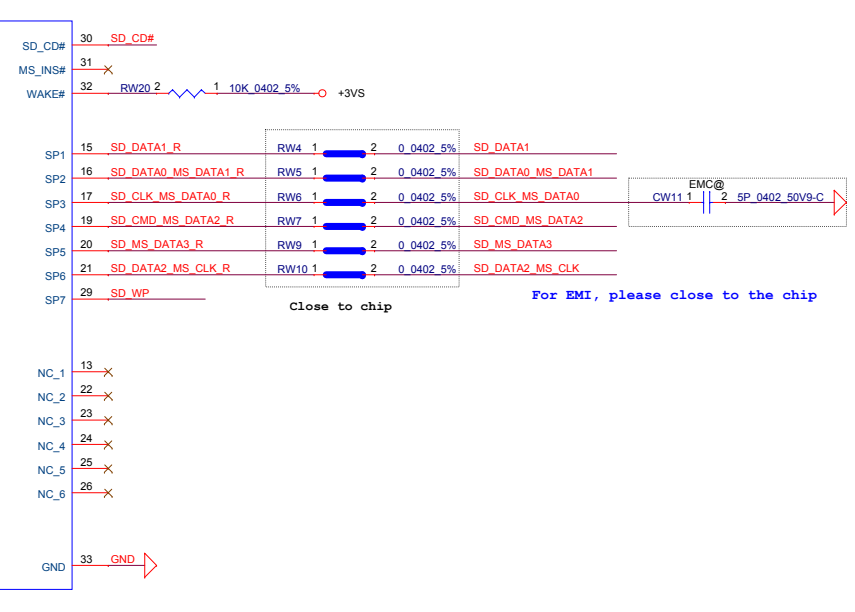
Close to pin 11

Close to pin 27



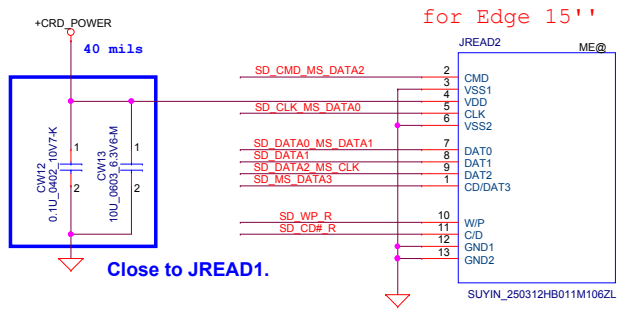
DV12 connects with AV12, due to DV12 need a external input.

375mA  
Close to chip 12mils, lengths < 200mils

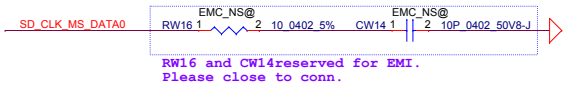


Close to chip

For EMI, please close to the chip




Close to JREAD1.

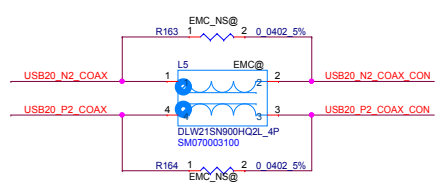


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**(Move to sub board)**

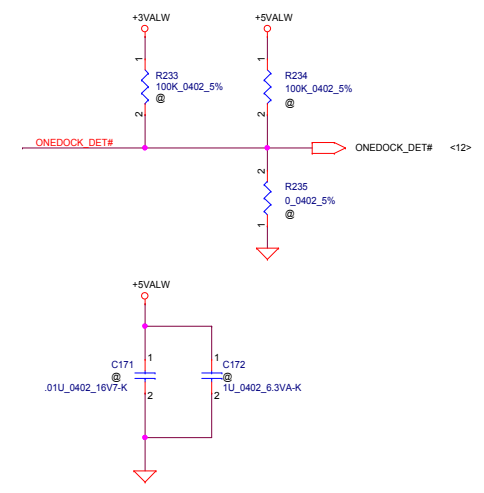
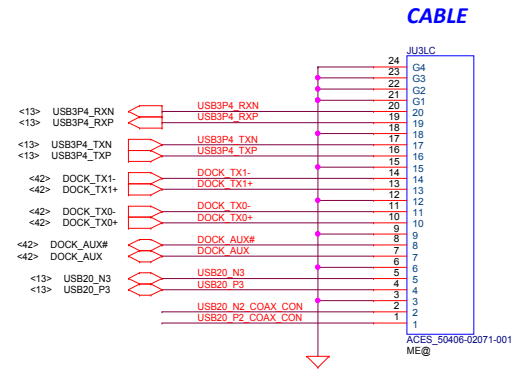
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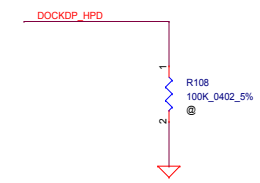
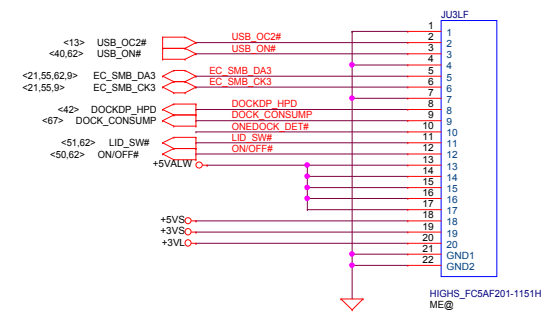
DOCKING

DOCKNG

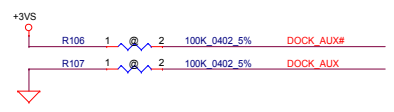
SUB/B



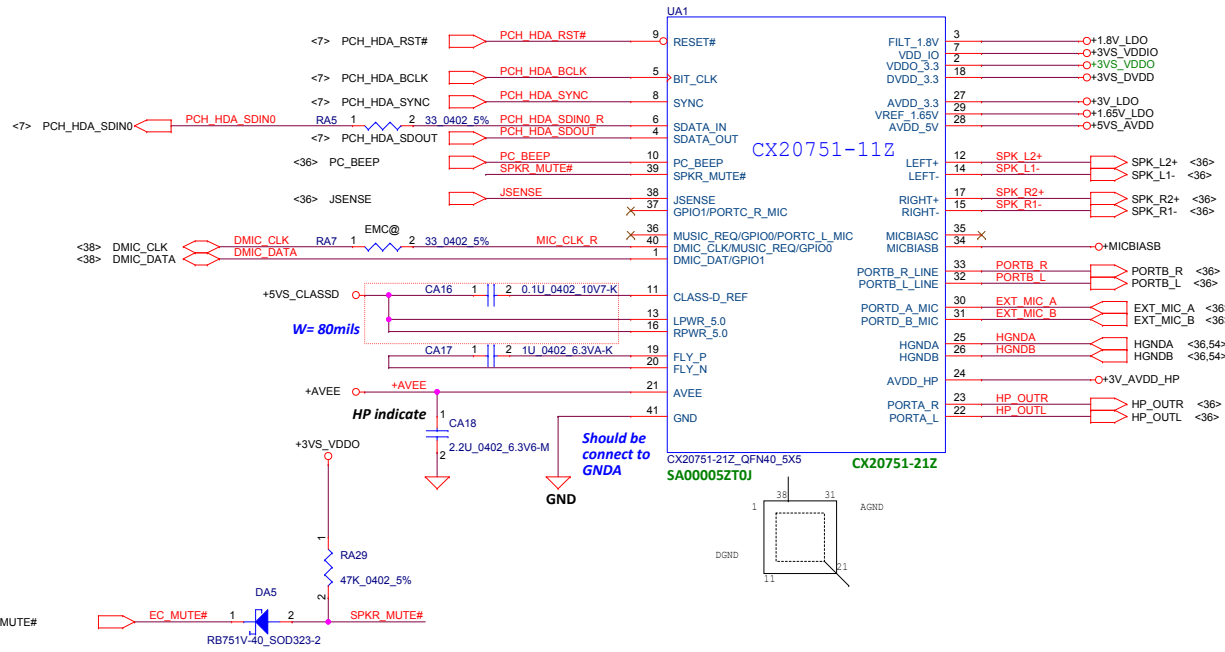
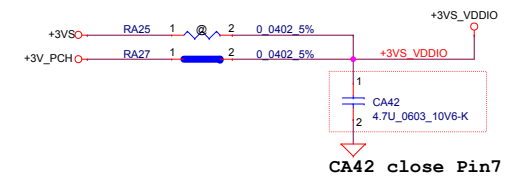
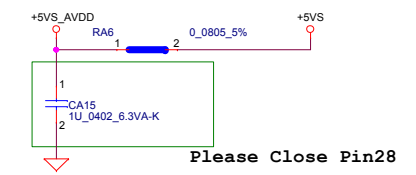
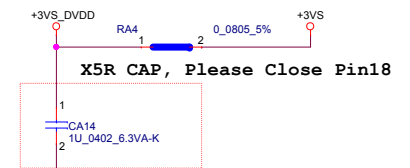
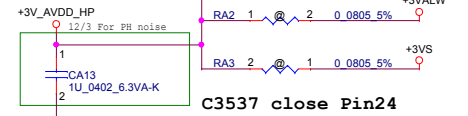
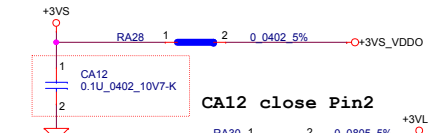
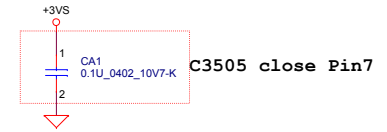
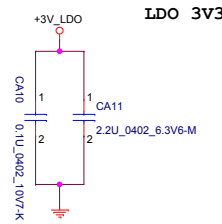
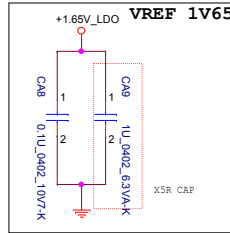
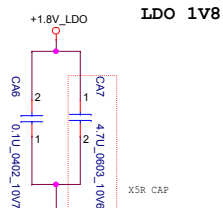
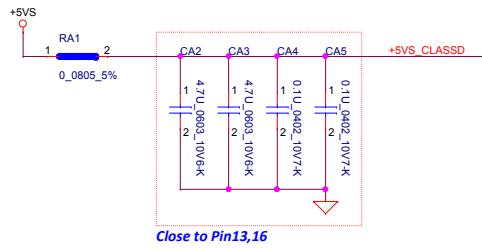
FFC



1. AC Capacitor place on Sub/B  
2. Need to check with MUX IC vendor whether still need AC cap between MUX IC and device.



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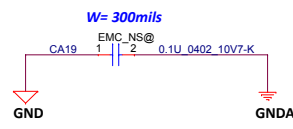
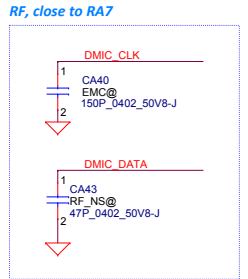
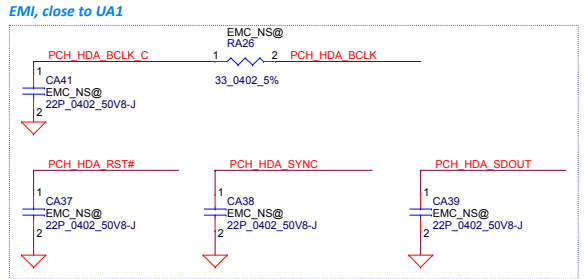


Apple --> EXT\_MIC\_A, HGND  
 Nokia --> EXT\_MIC\_B, HGND

W= 80mils

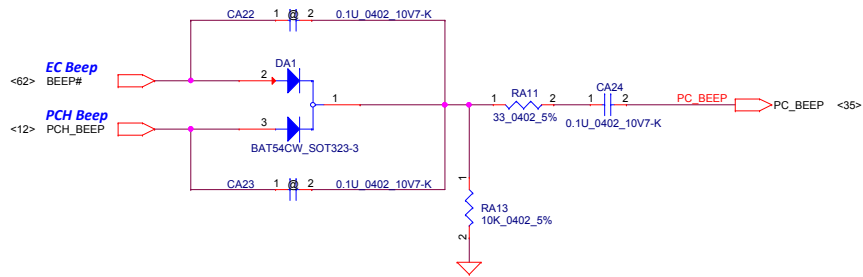
Should be connect to GND

W= 300mils

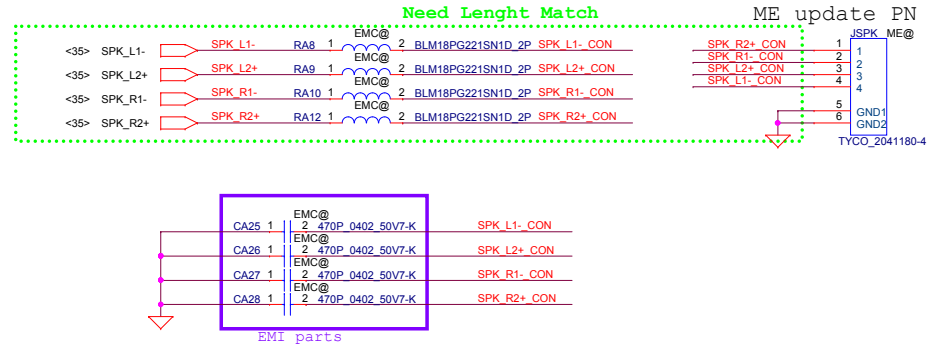


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### PC Beep

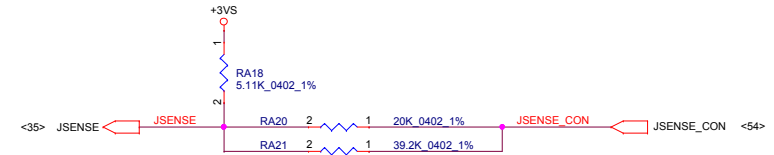
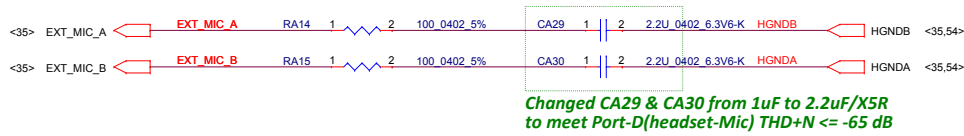


### Speaker OUT

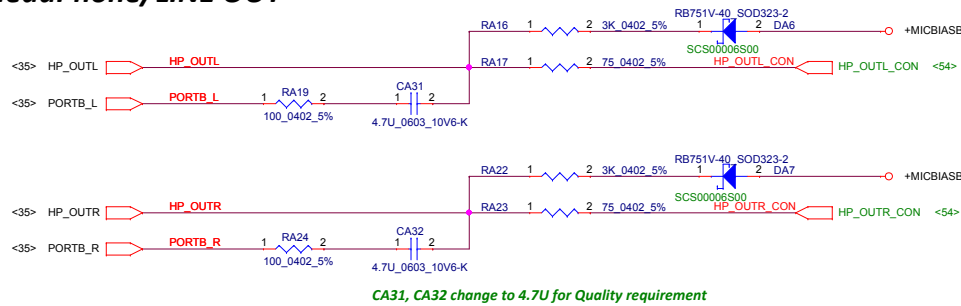


### EXT. MIC/LINE IN

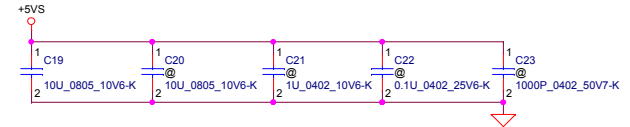
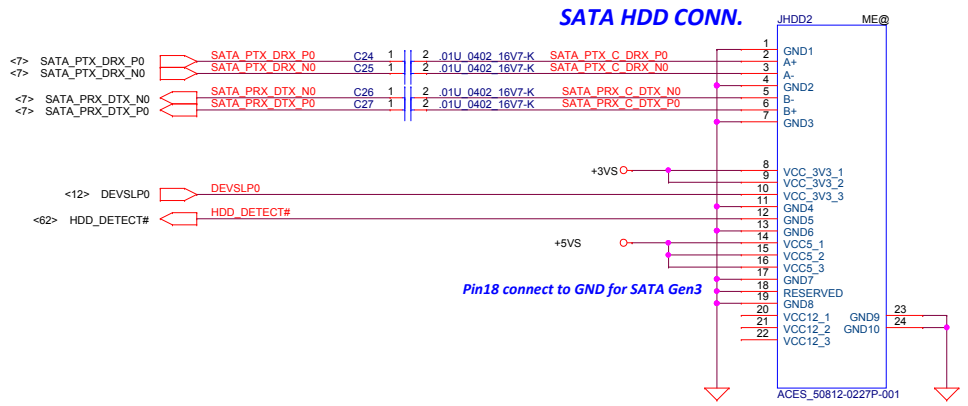
Apple --> EXT\_MIC\_A, HGND B  
 Nokia --> EXT\_MIC\_B, HGND A



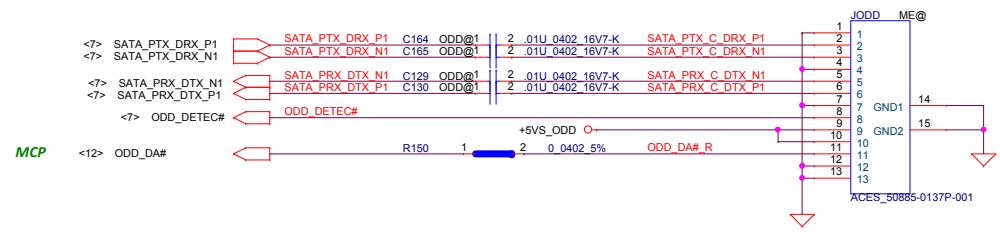
### HeadPhone/LINE OUT



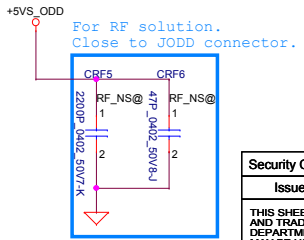
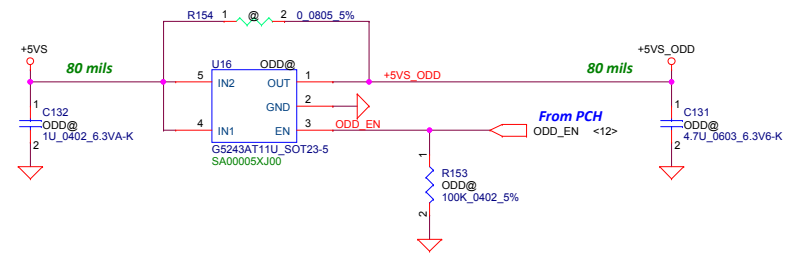
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### SATA ODD CONN

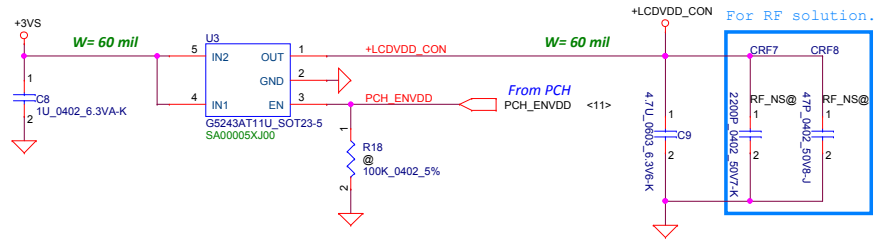


### +5VS TO +5VS\_ODD

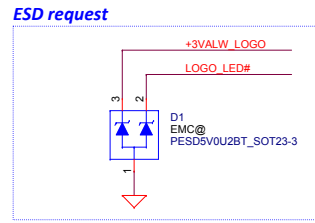
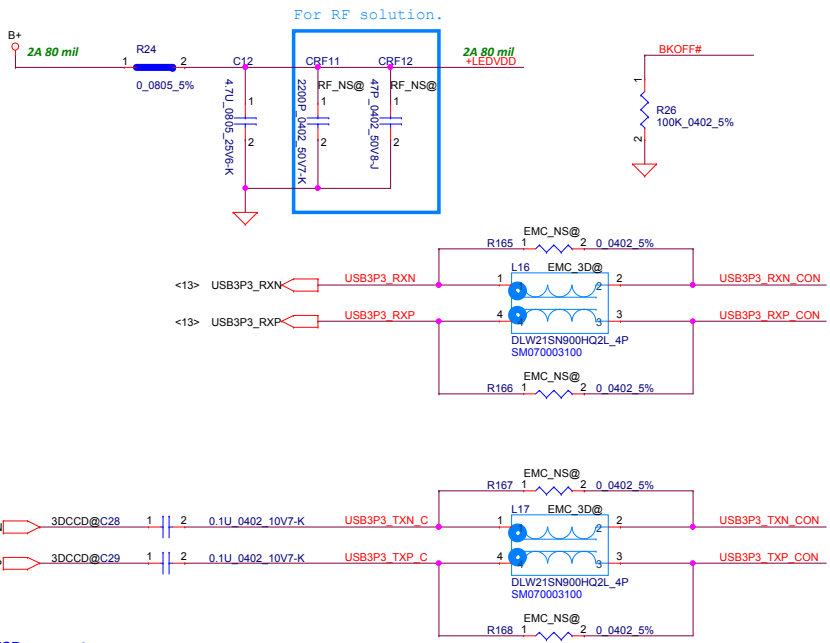
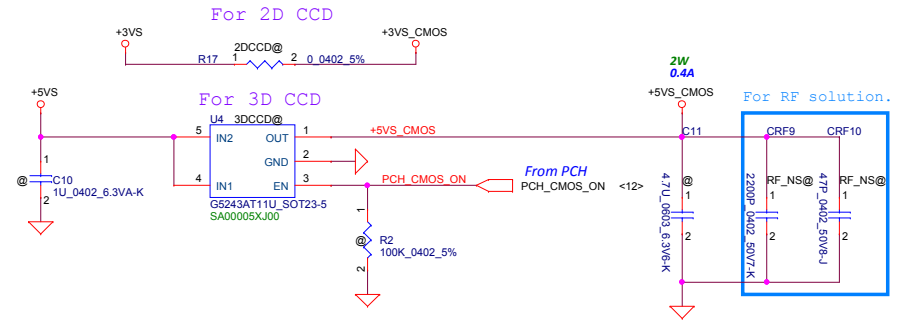


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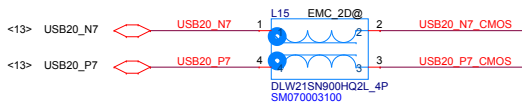
**LCDVDD Circuit**



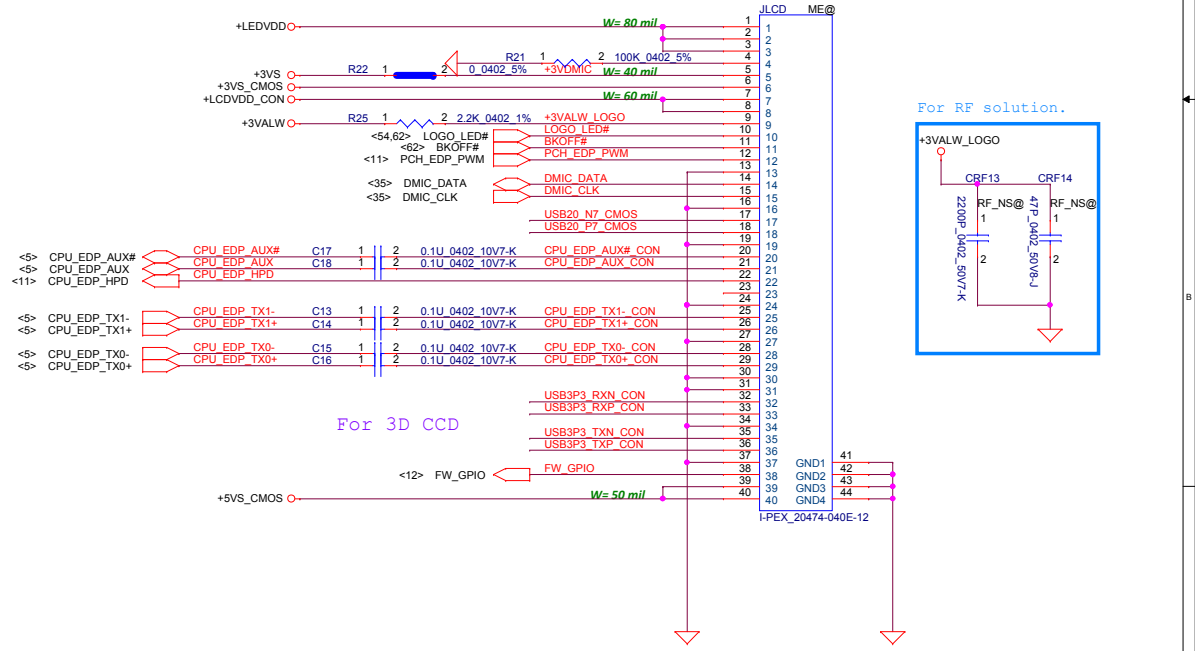
**CMOS Camera**



**CMOS USB Port 2**




**eDP CONN.**

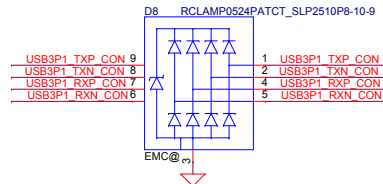
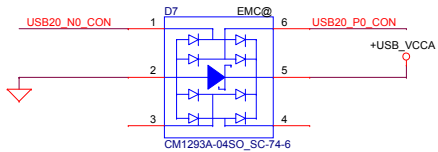
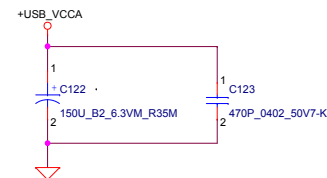
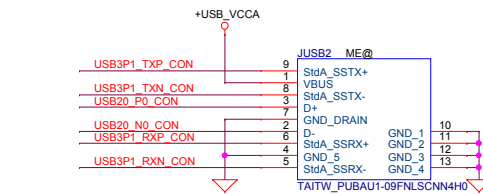
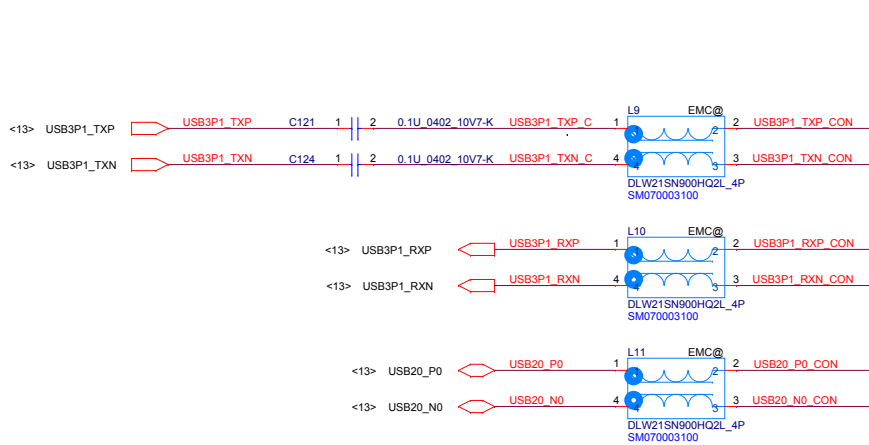
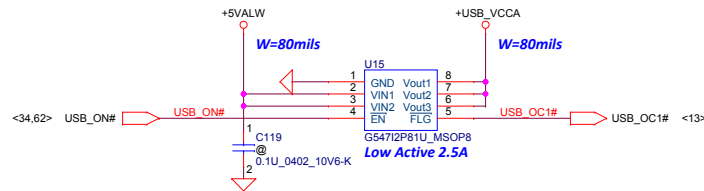



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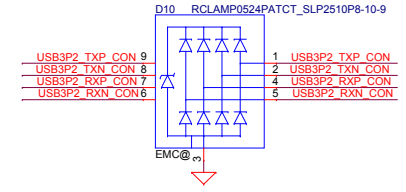
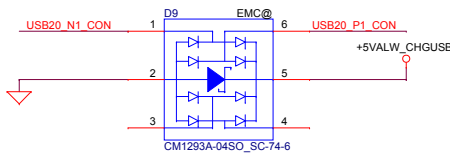
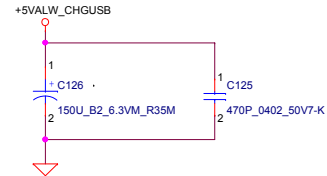
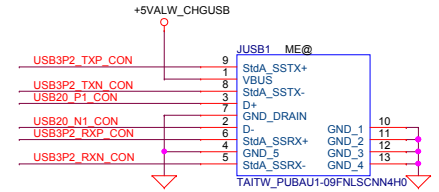
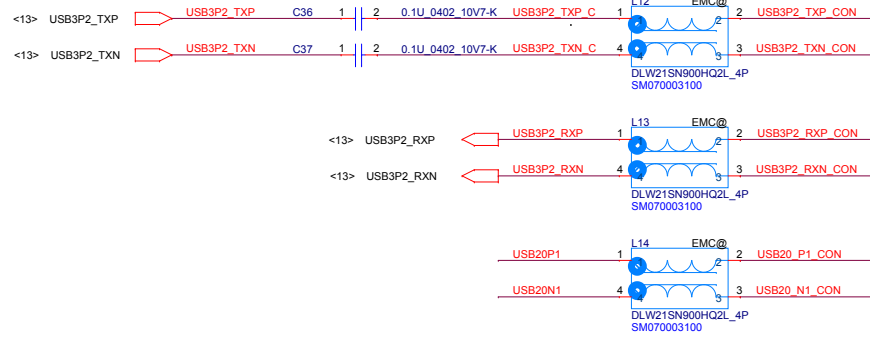
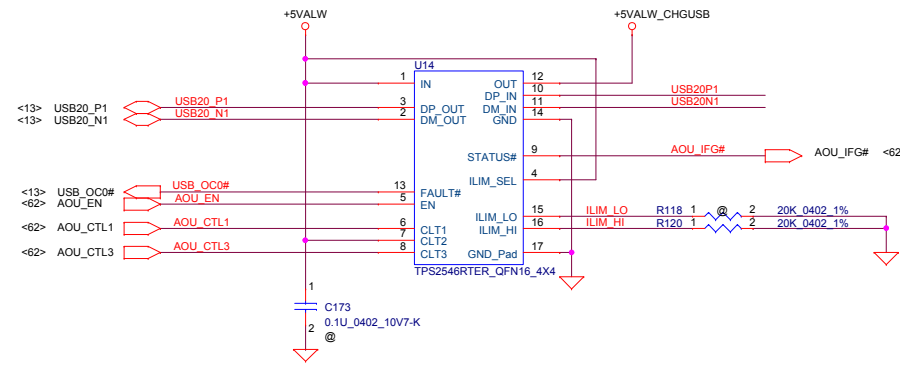
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### POWER SWITCH



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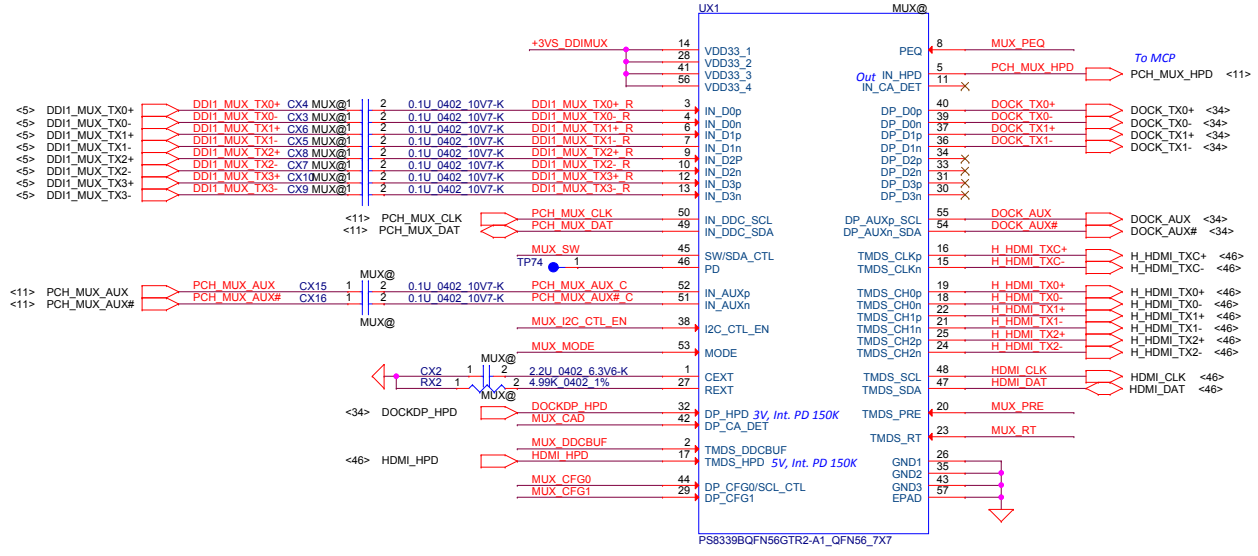
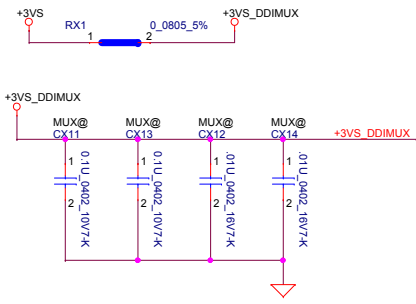




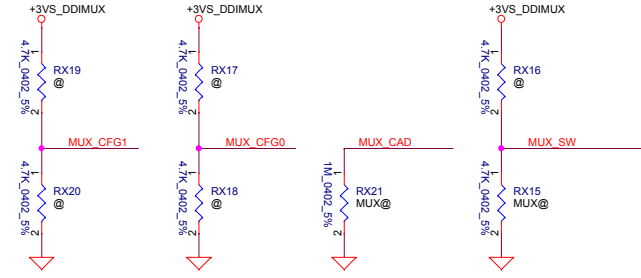
TI TPS2546

CLT1	CLT2	CLT3	ILIM_SEL	MOD	
0	0	0	X	DCH	OUT held low
* 1	1	1	1	CDP	Data Connected and Port Power Mgt. Function Active
* 1	1	1	0	SDP2	Data Connected
* 1	1	0	X	SDP1	Data Connected
* 0	1	0	X	SDP1	Data Connected
1	0	0	X	DCP_Short	Device Forced to stay in DCP BC 1.2 charging mode
1	0	1	X	DCP_Divider	Device Forced to stay in DCP Divider 1 Charging Mode
* 0	1	1	X	DCP_Auto	Data Disconnected and Port Power Mgt. Function Active
0	0	1	X	DCP_Auto	Data Disconnected and Power Wake Function Active

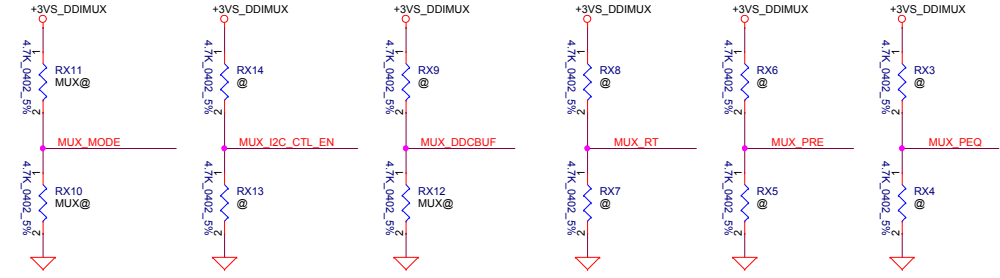
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**Auto Mode  
DP Higher Priority**

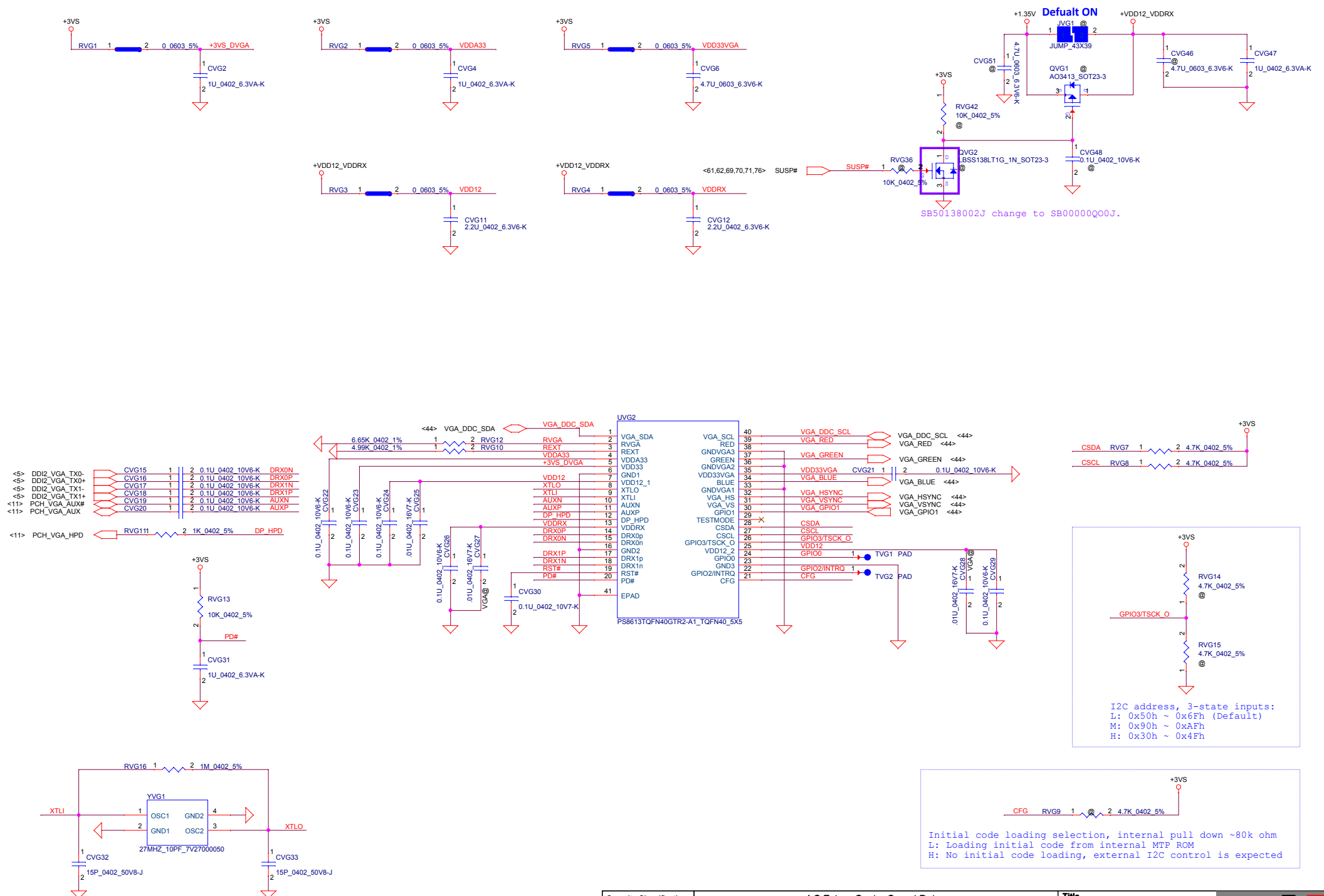


**Pass Through Mode**



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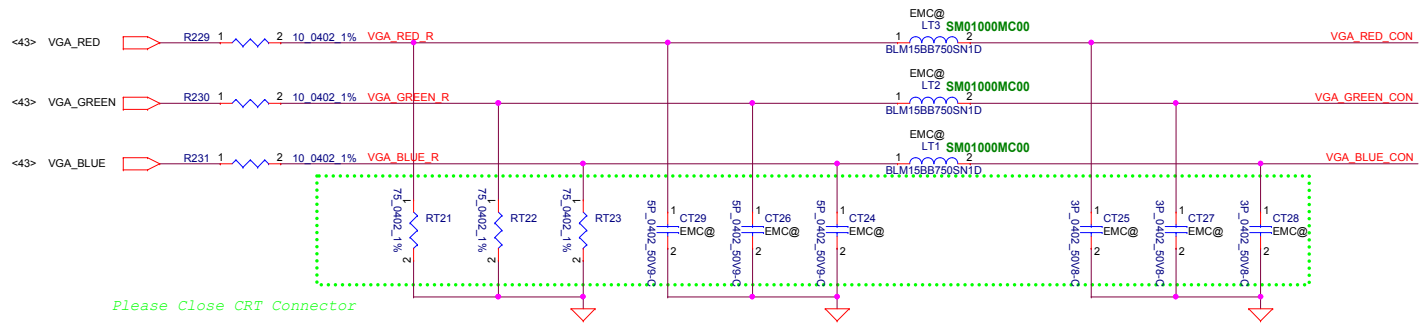
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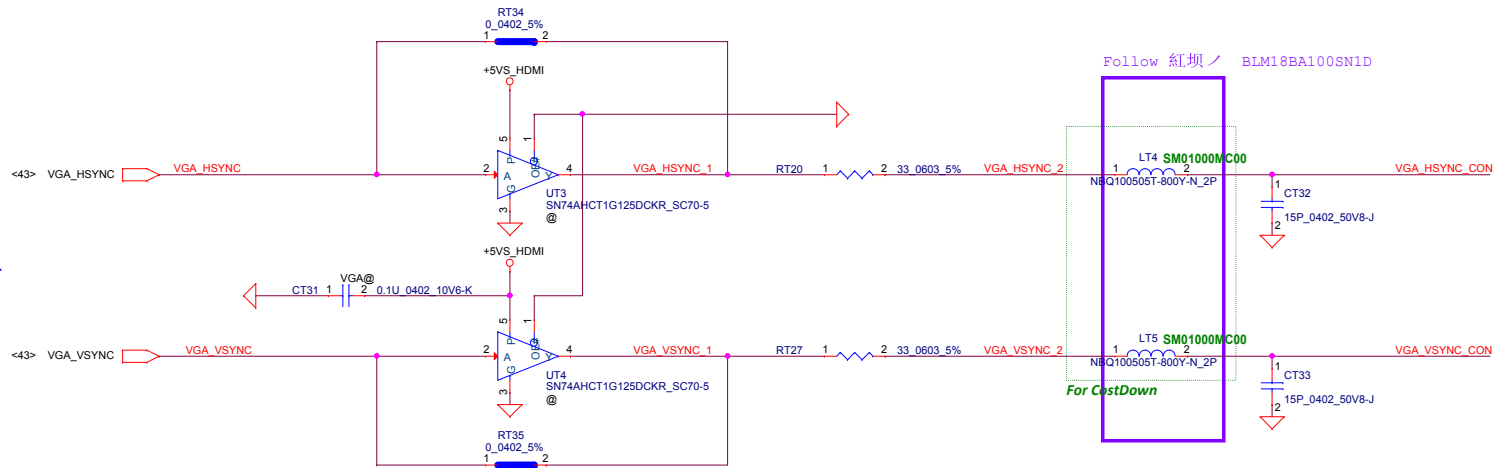
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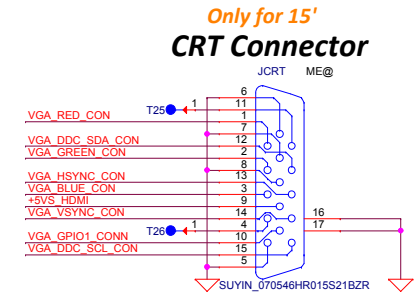


Please Close CRT Connector

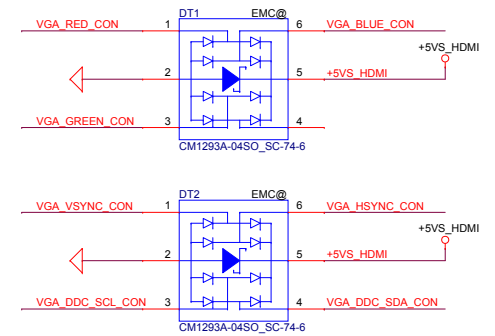
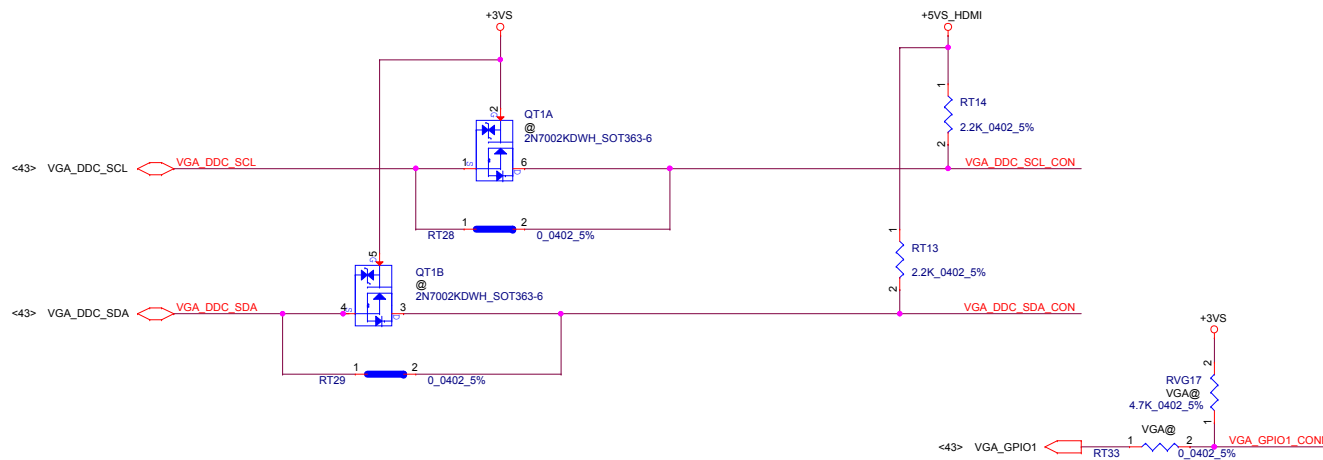


Follow 紅坝 / BLM18BA100SN1D

For CostDown



Traslater




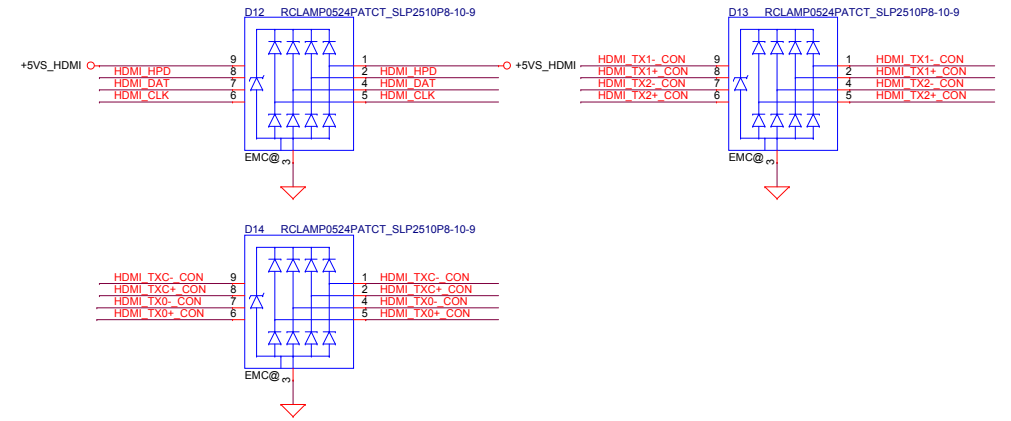
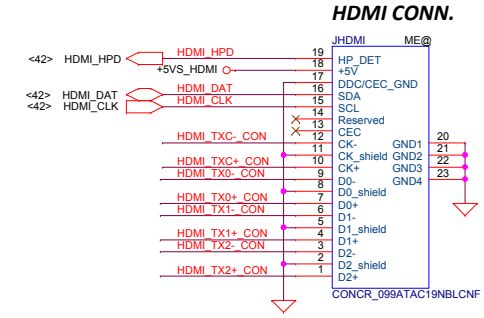
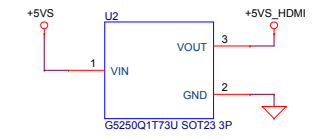
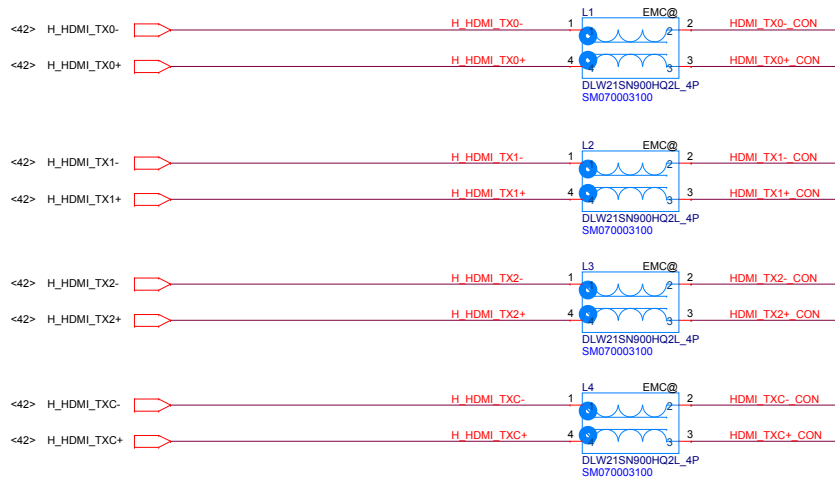
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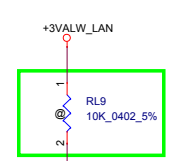
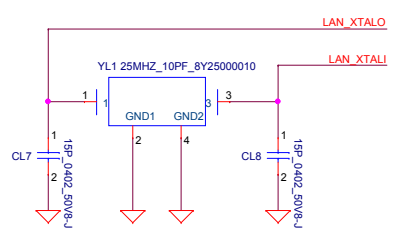
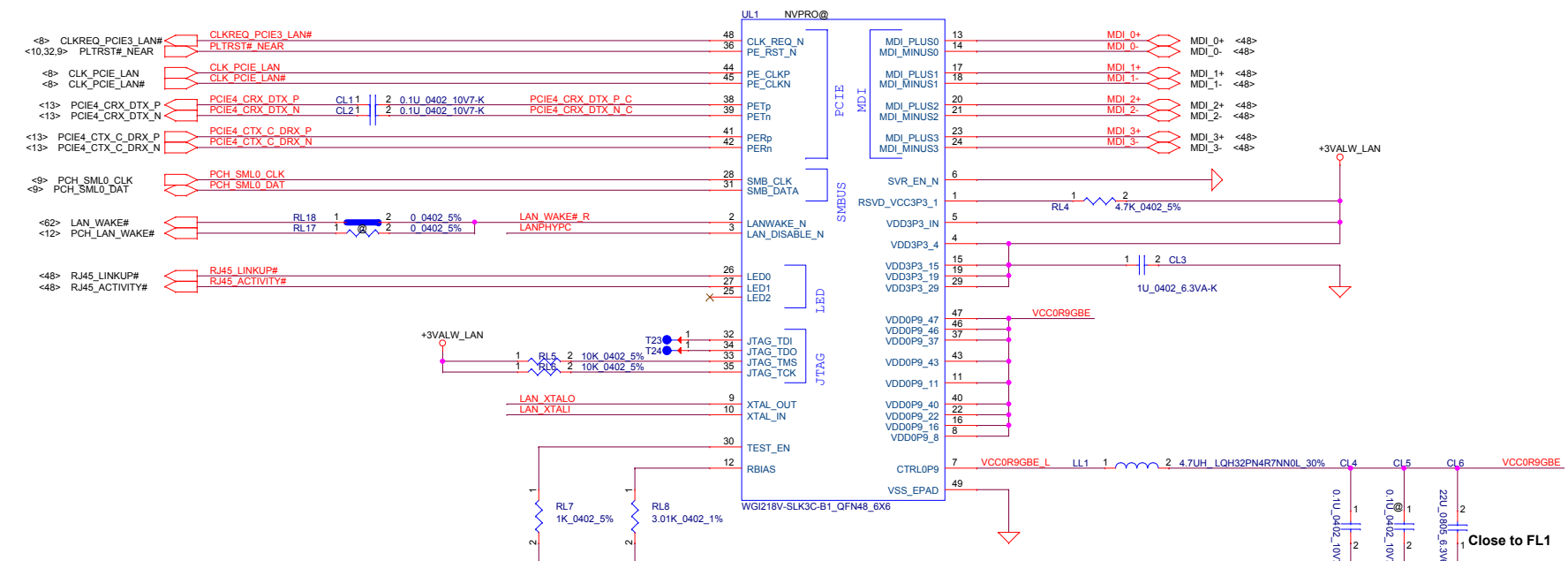
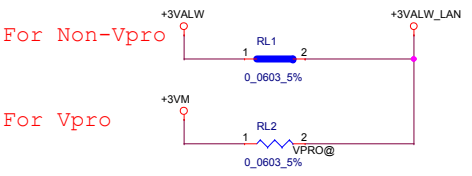
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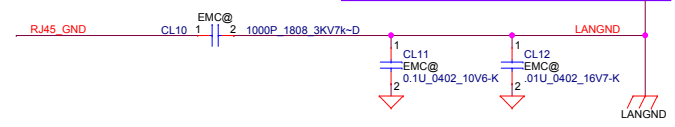
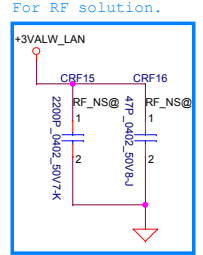
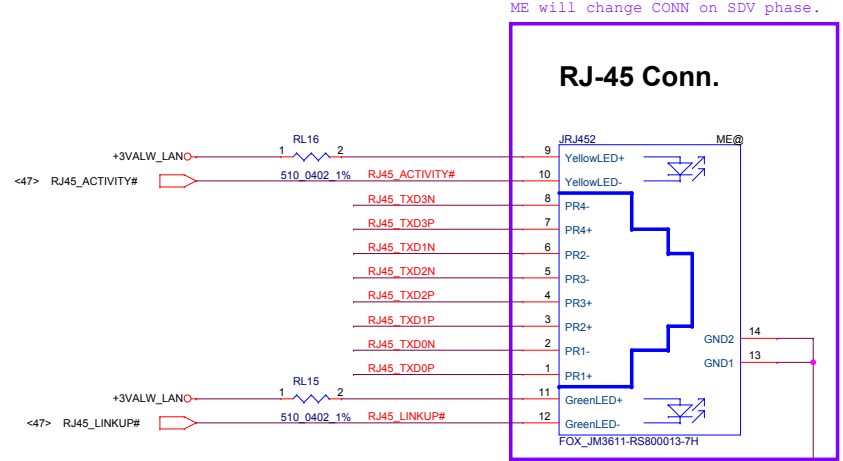
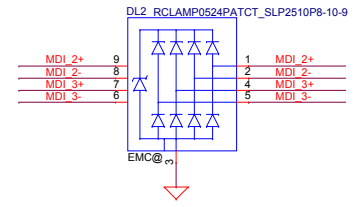
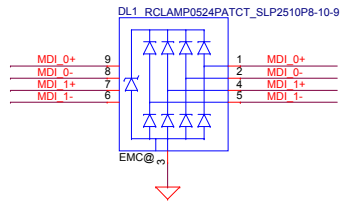
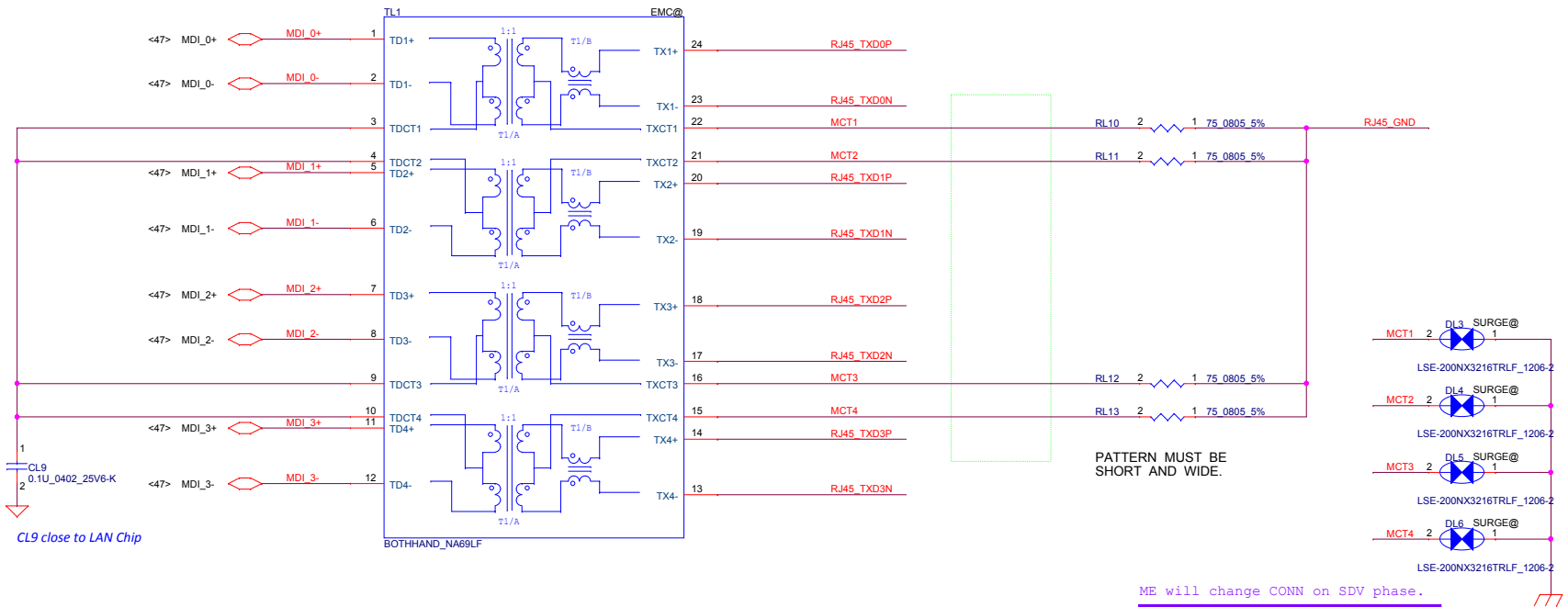


When use Native function, intel recommend pull high 10K ohm  
This part is un-mount in Sting.

**UL1 GBE PHY**

vPro Model	Non-vPro Model
I218LM	I218V

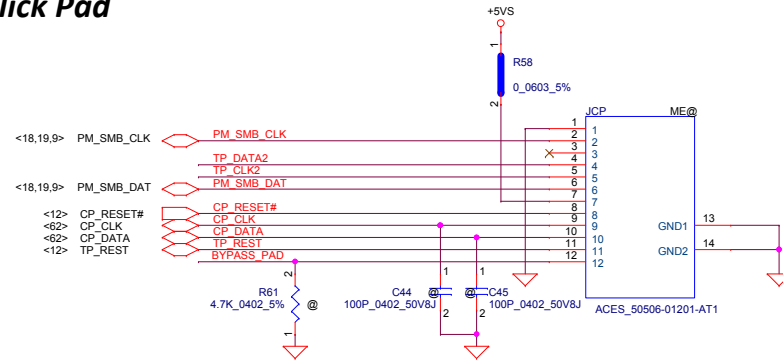
ST-1\_SWG\_SDV-SWG\_EC062  
Add vPro/Non-vPro table.



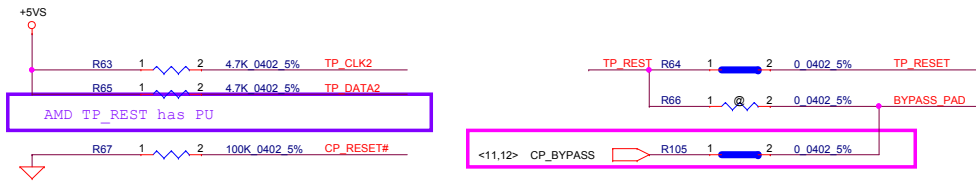
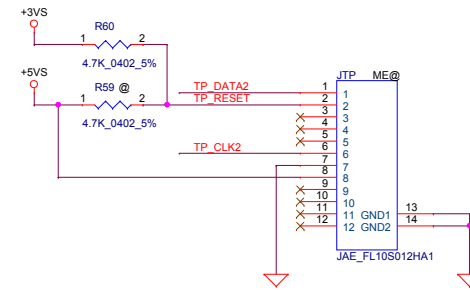
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### Click Pad

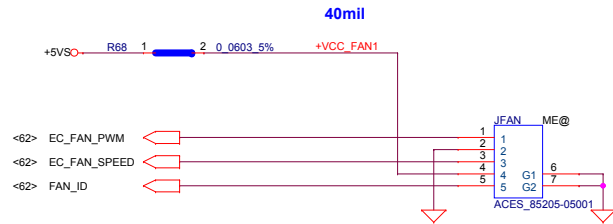


### Track point

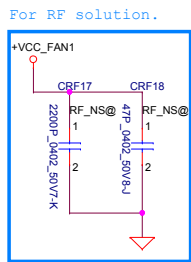


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**FAN CONN.**



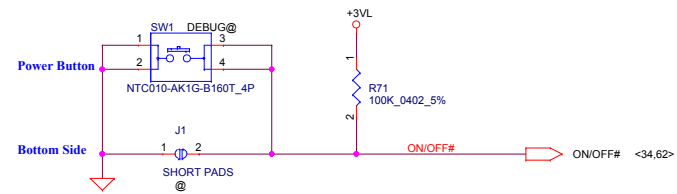
惠璣鐵AMD鐵THERMAL絨板PIN define



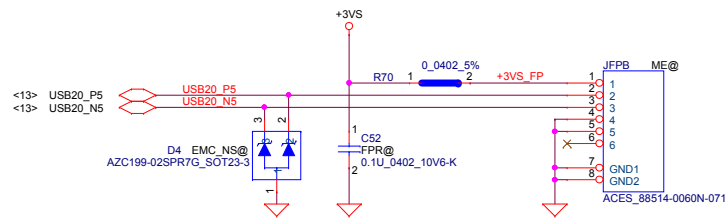
**PWR BTN/LID SW CONN.**

For 14" on board  
For 15" on Sub/B

ON/OFF Switch --> 簿 'Sub/B

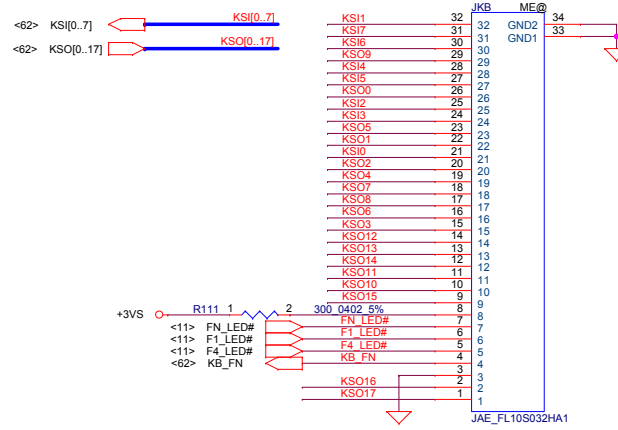


**FingerPrint CONN.**

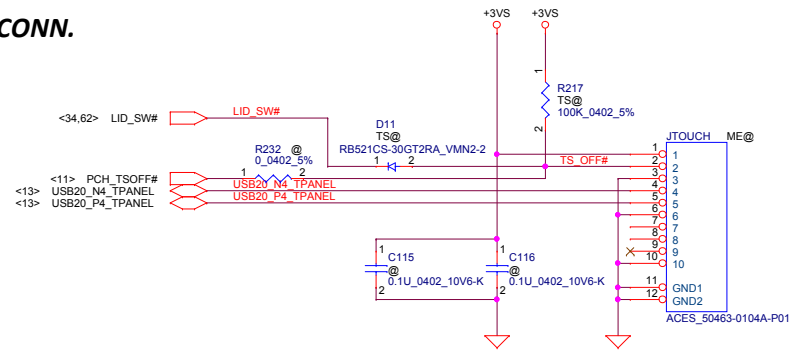


Lid Switch --> 簿 'Sub/B

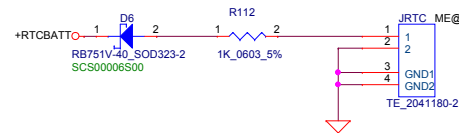
### KB CONN



### TOUCH PANEL CONN.

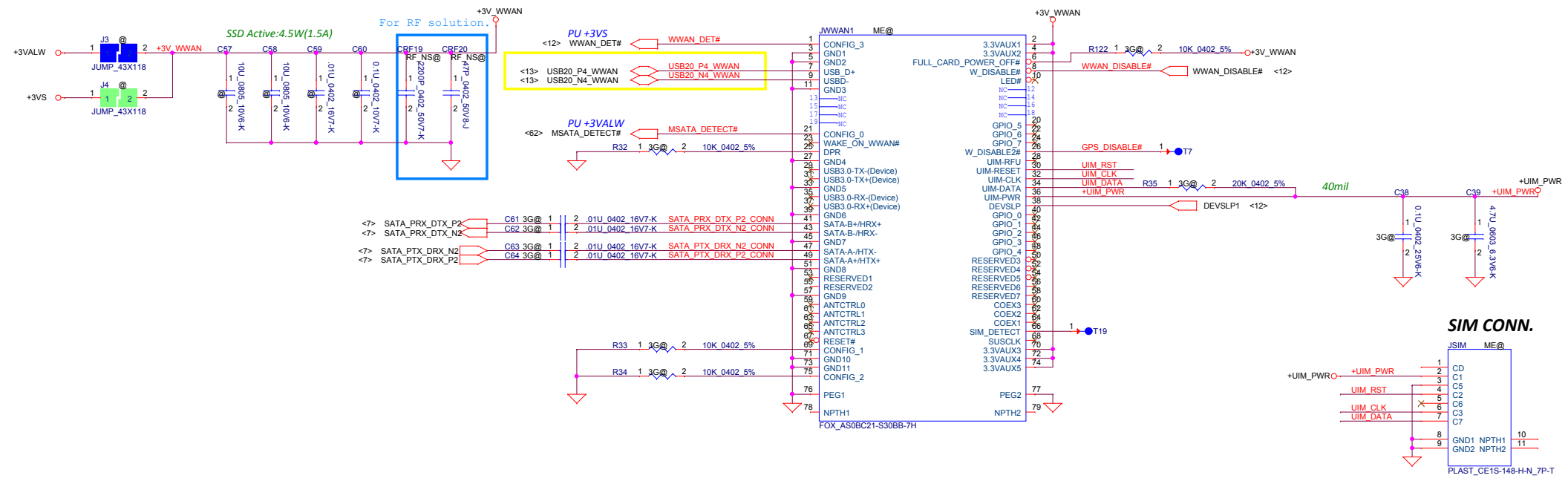


### RTC CONN.

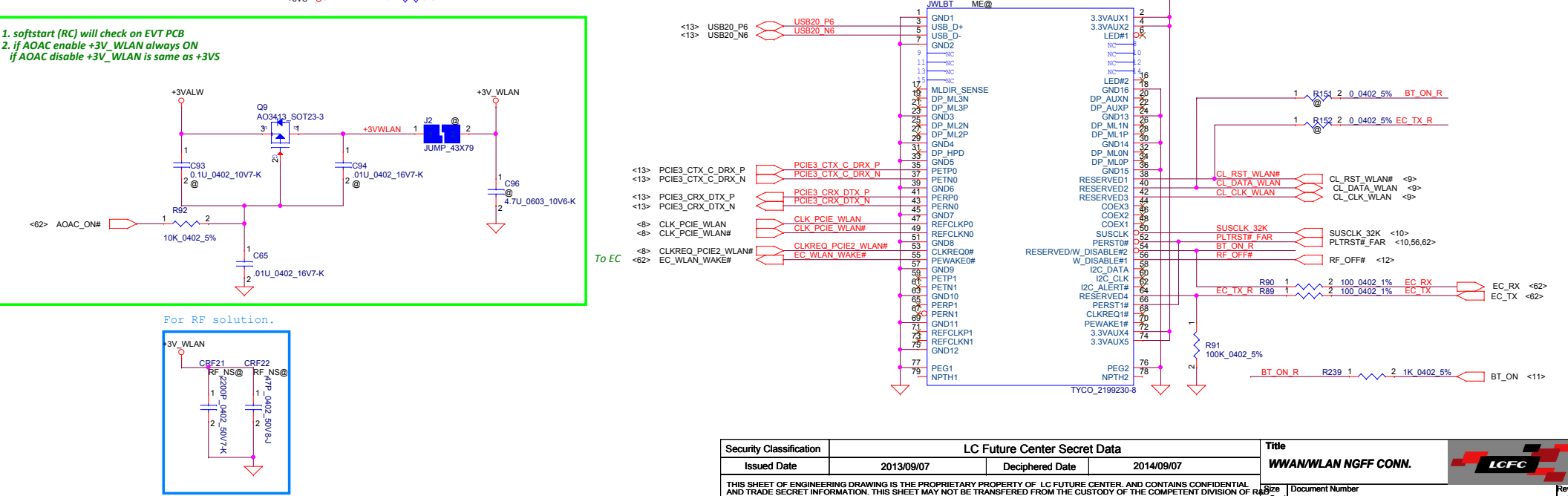


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# TYPE-B NGFF SLOT FOR WWAN/SSD 3.2H CONNECTOR




# TYPE-A NGFF SLOT FOR WLAN 3.2H CONNECTOR

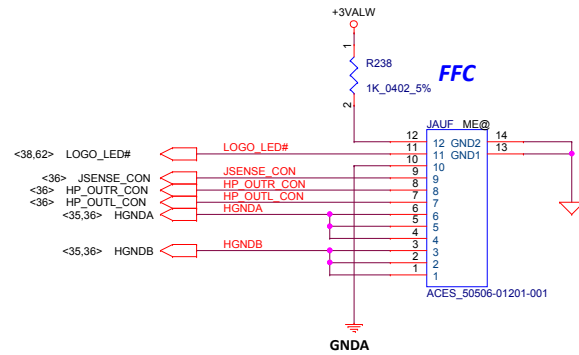



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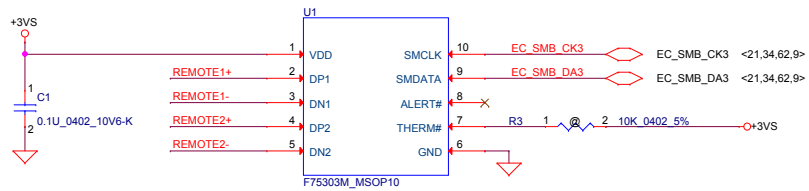
### For Edge 15" Audio board CONNECTOR



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				Rev 1.0
				Date: Thursday, November 08, 2014   Sheet 54 of 81

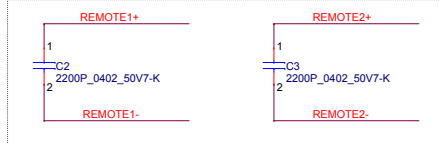
# Thermal Sensor

**Thermal Sensor  
placed near by VRAM**

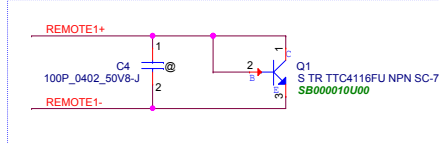


**Address 1001\_101xb**  
*Internal pull up 1.2K to 1.5V*  
*R for initial thermal shutdown temp*

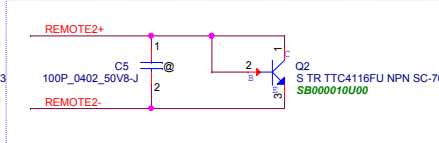
**Close to U1**



**Close to +VCC\_CORE**



**Close JDIMM1&JDIMM2**



**REMOTE2+/-:**  
*Trace width/space:10/10 mil*  
*Trace length:<8"*

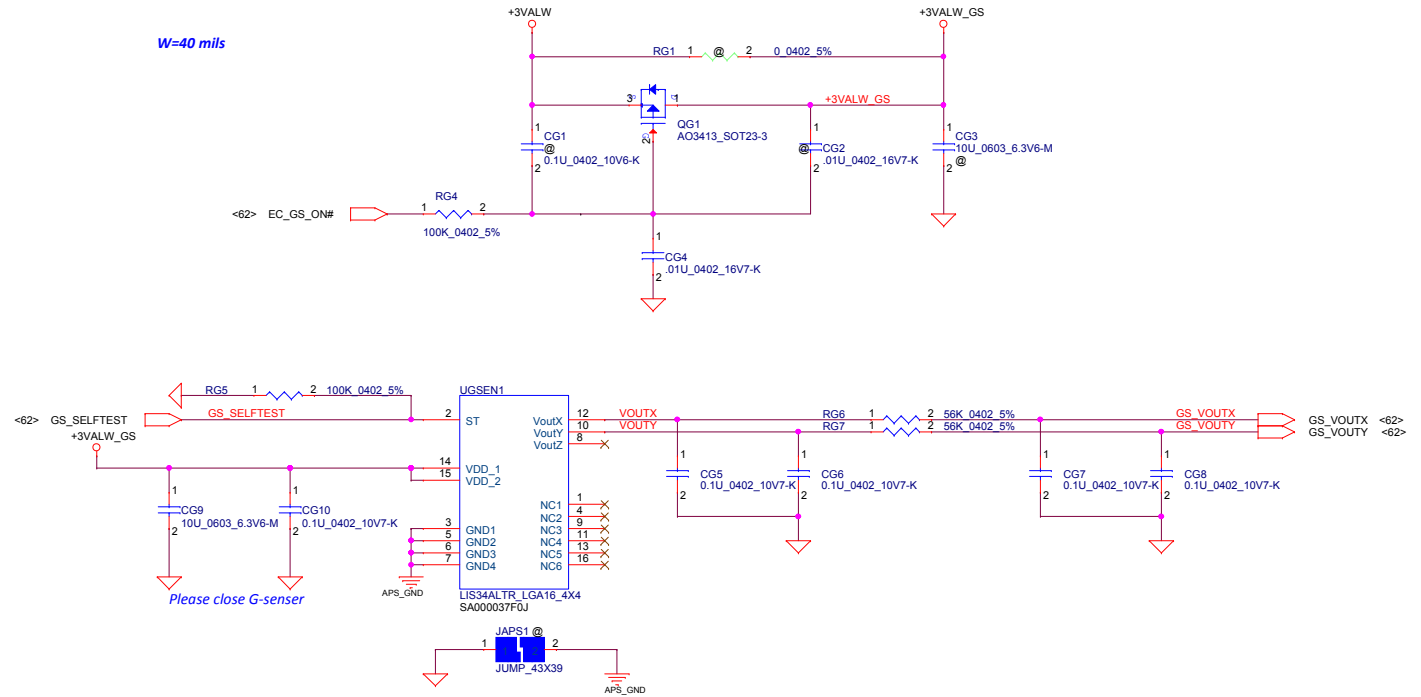
Security Classification	LC Future Center Secret Data			Title	XXXX
Issued Date	2013/09/07	Deciphered Date	2014/09/07	Size	
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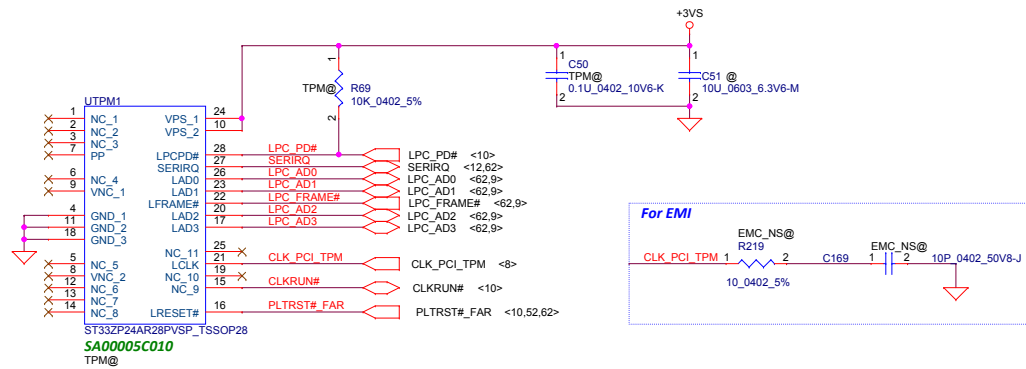
**AITE1 NM-A221**

# APS G-Sensor

W=40 mils



## TPM IC



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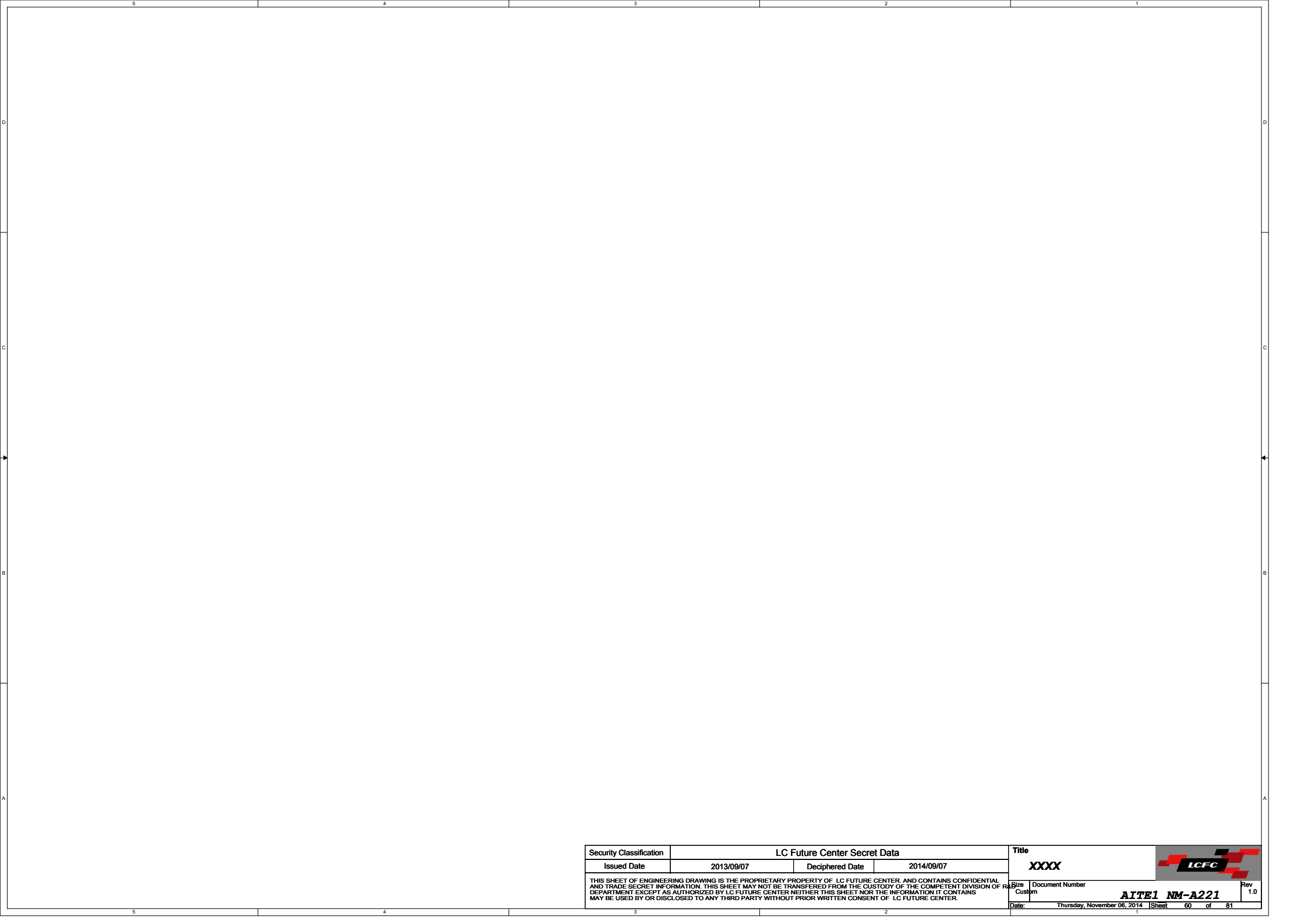
Security Classification	LC Future Center Secret Data		Title		
Issued Date	2013/09/07	Deciphered Date	2014/09/07		XXXX
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					Custom	<b>AITE1 NM-A221</b>	1.0
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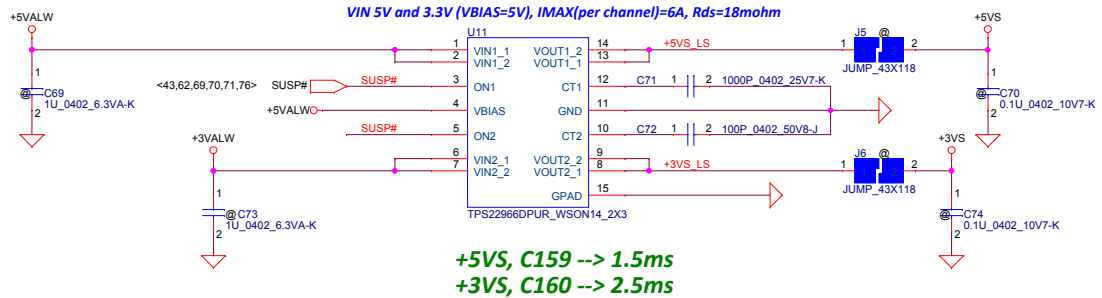
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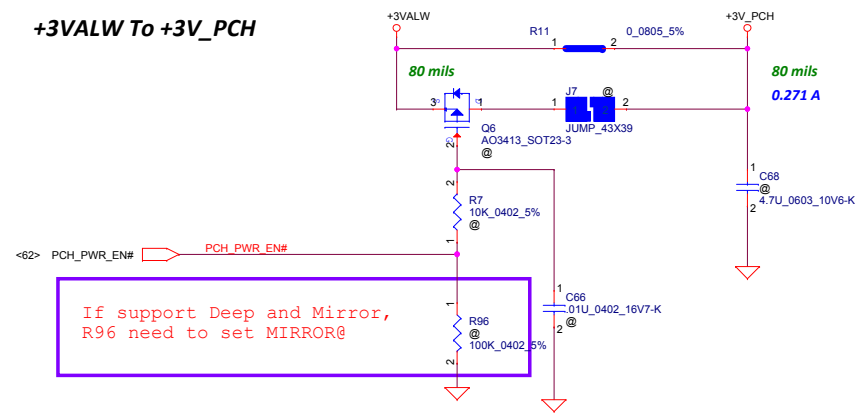
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Issued Date	2013/09/07	Deciphered Date	2014/09/07	
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**Load Switch**  
**+5VALW To +5VS**  
**+3VALW To +3VS**



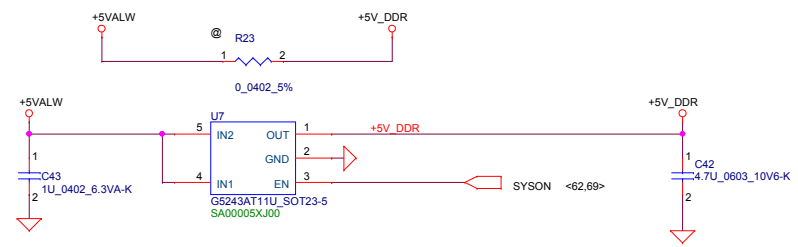
**+5VS, C159 --> 1.5ms**  
**+3VS, C160 --> 2.5ms**

**+3VALW To +3V\_PCH**

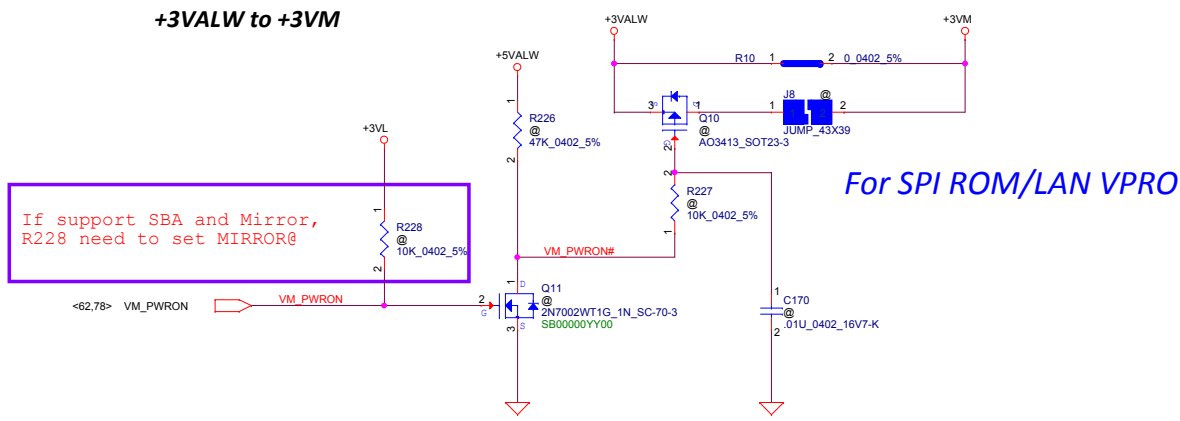


If support Deep and Mirror,  
R96 need to set MIRROR@

**+5VALW To +5V\_DDR**



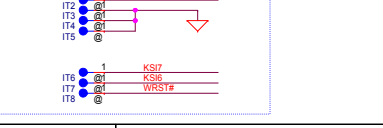
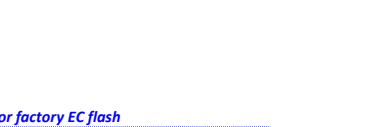
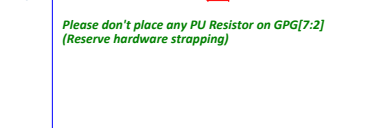
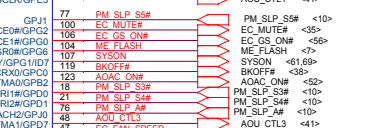
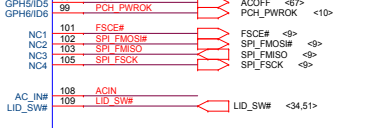
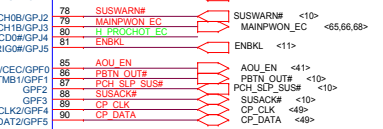
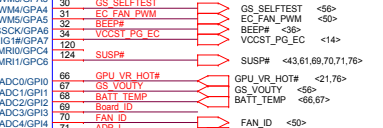
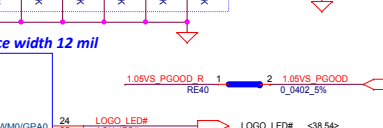
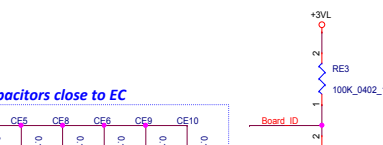
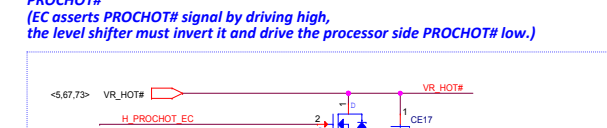
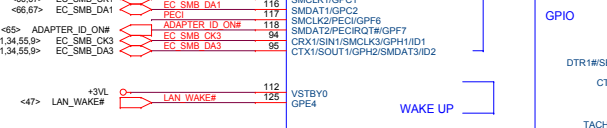
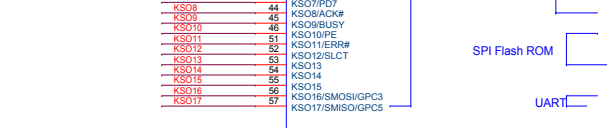
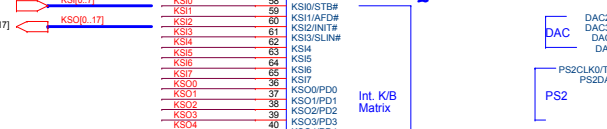
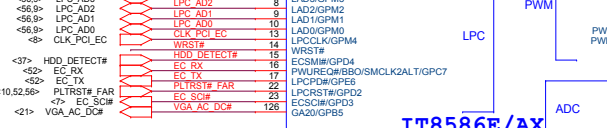
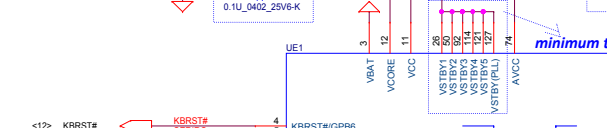
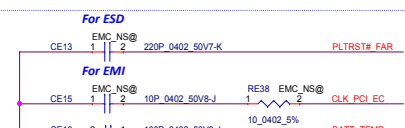
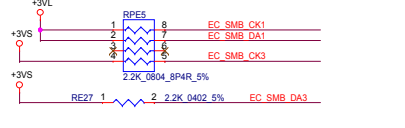
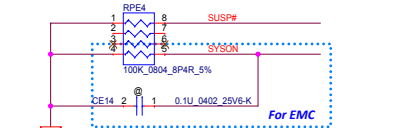
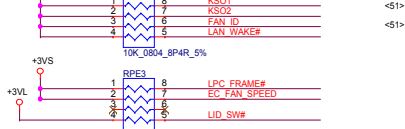
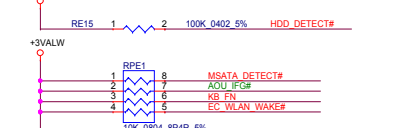
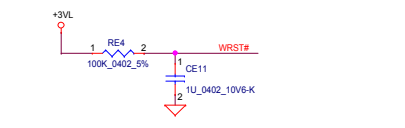
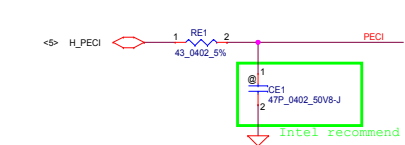
**+3VALW to +3VM**



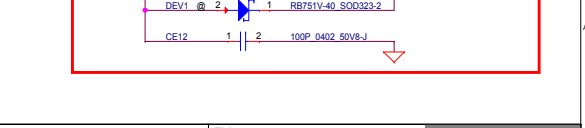
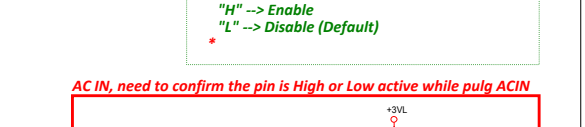
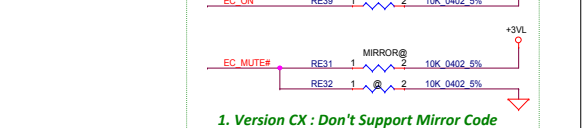
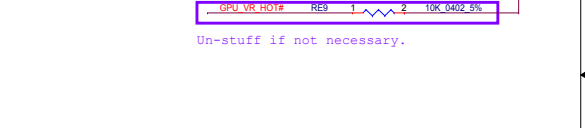
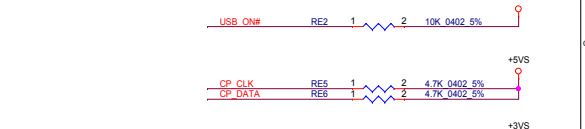
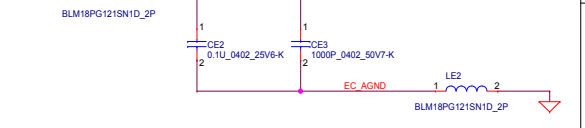
If support SBA and Mirror,  
R228 need to set MIRROR@

**For SPI ROM/LAN VPRO**

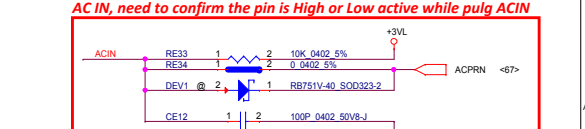
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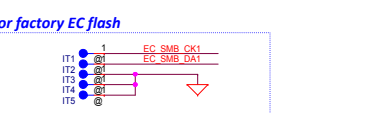
Board ID	RE7	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max	Phase
0	0K +/- 5%	0 V	0 V	0 V	Pre-SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	SDV
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	FVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SIT
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	SVT
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	



1. Version CX : Don't Support Mirror Code  
Version DX/EX/FX : Support Mirror Code  
"H" --> Enable  
"L" --> Disable (Default)



**PROCHOT#**  
(EC asserts PROCHOT# signal by driving high, the level shifter must invert it and drive the processor side PROCHOT# low.)

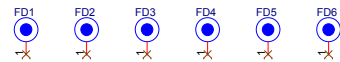



## Screw Hole




Center Zero

## PCB Fedcal Mark PAD

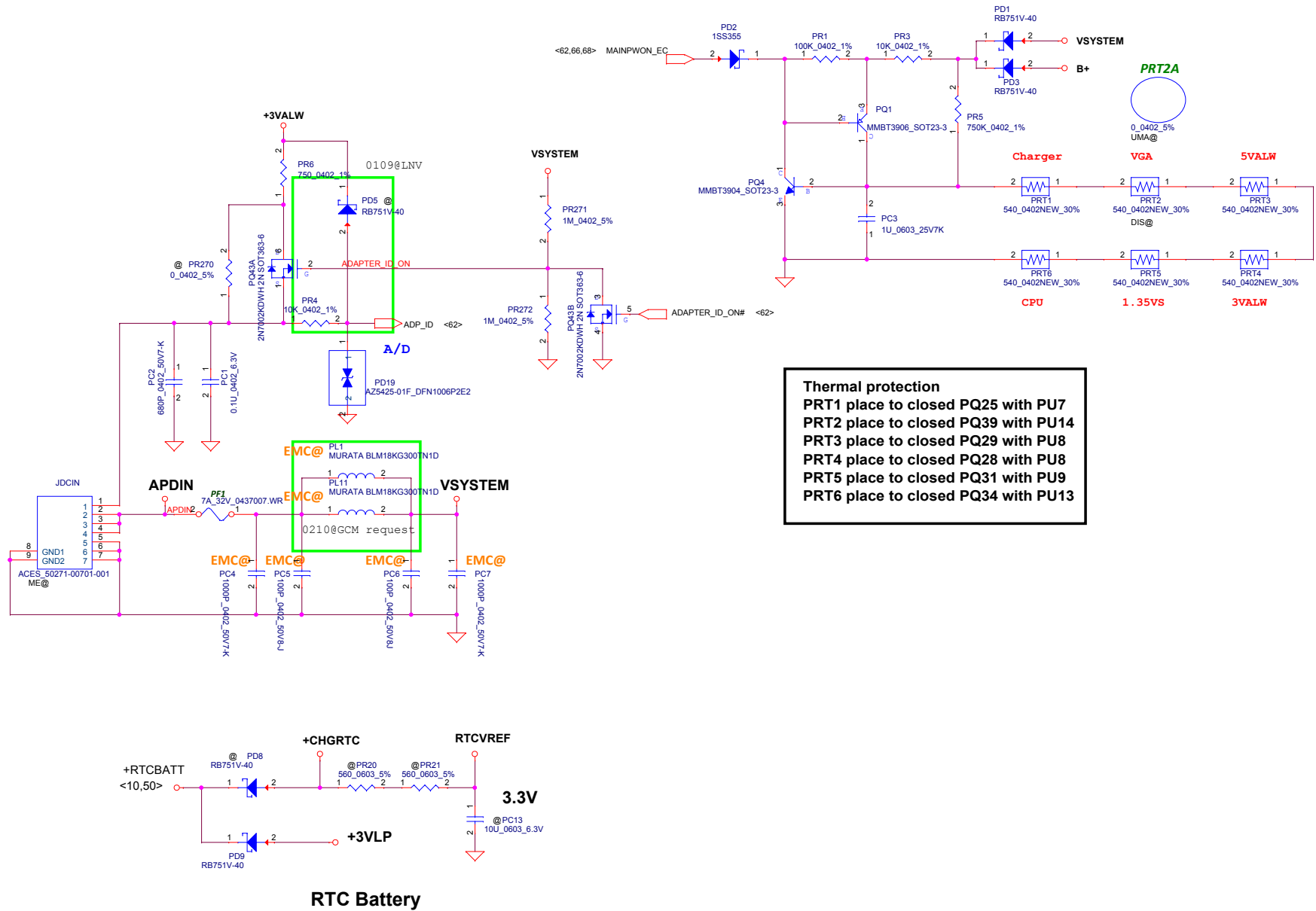


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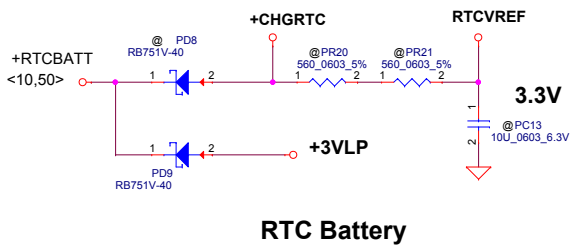
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Security Classification	LC Future Center Secret Data			Title	<b>XXXX</b>	
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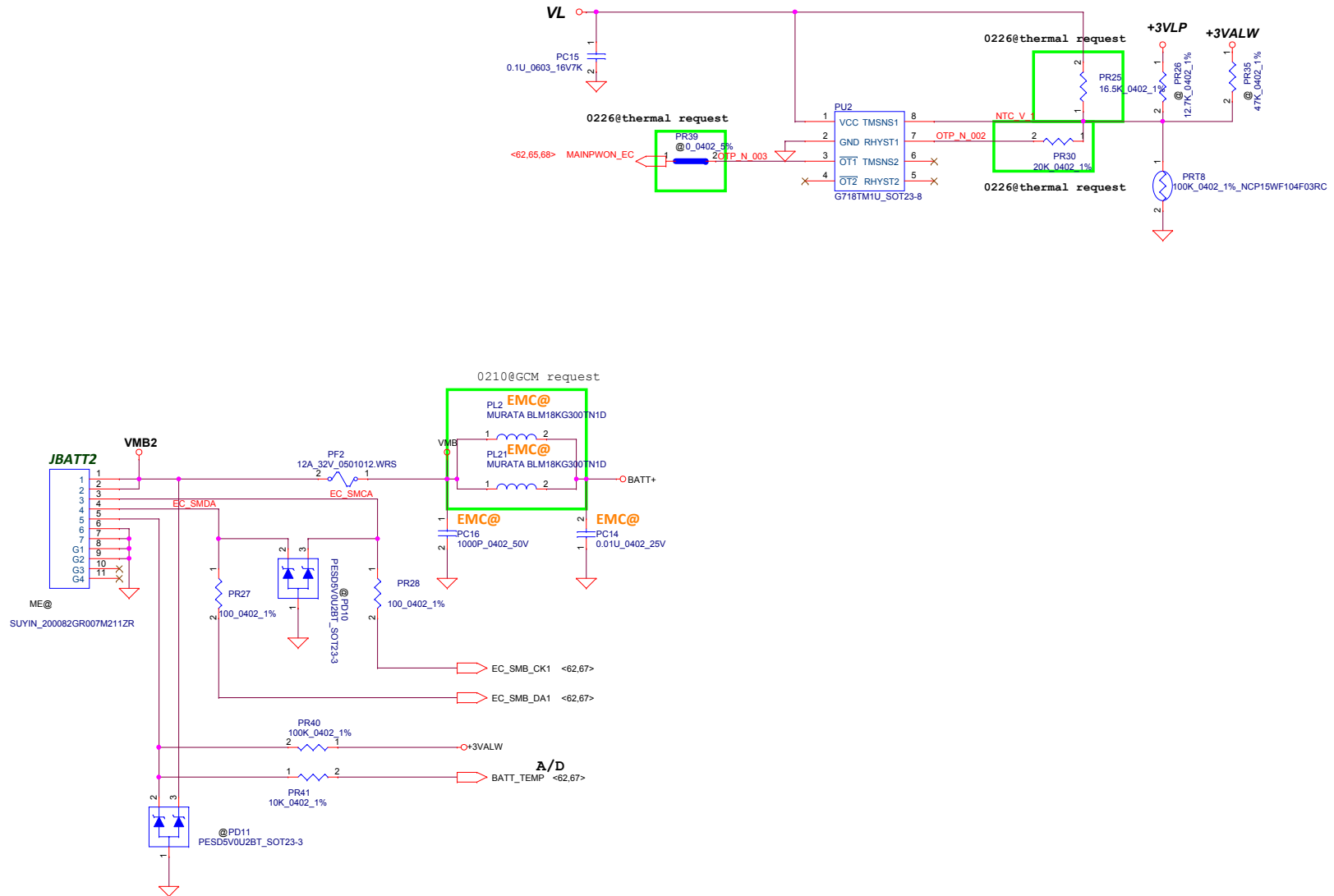


**Thermal protection**  
 PRT1 place to closed PQ25 with PU7  
 PRT2 place to closed PQ39 with PU14  
 PRT3 place to closed PQ29 with PU8  
 PRT4 place to closed PQ28 with PU8  
 PRT5 place to closed PQ31 with PU9  
 PRT6 place to closed PQ34 with PU13



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**PRT8 under CPU bottom side :**  
**CPU thermal protection at 93 +/-3 degree C**  
**Recovery at 56 +/-3 degree C**



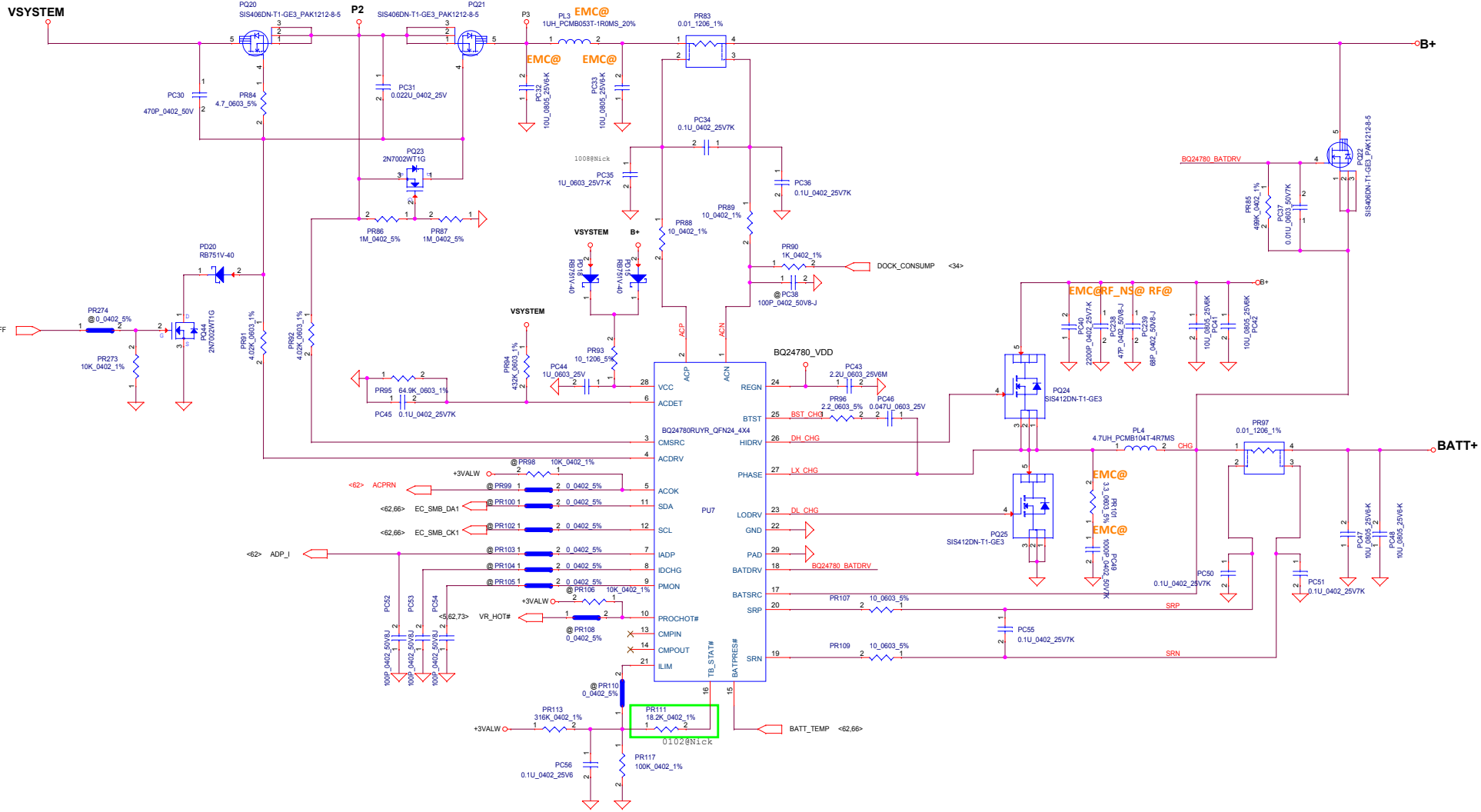
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Issued Date	2013/08/05	Deciphered Date 2014/12/31


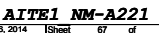
Title	BATTERY CONN/OTP
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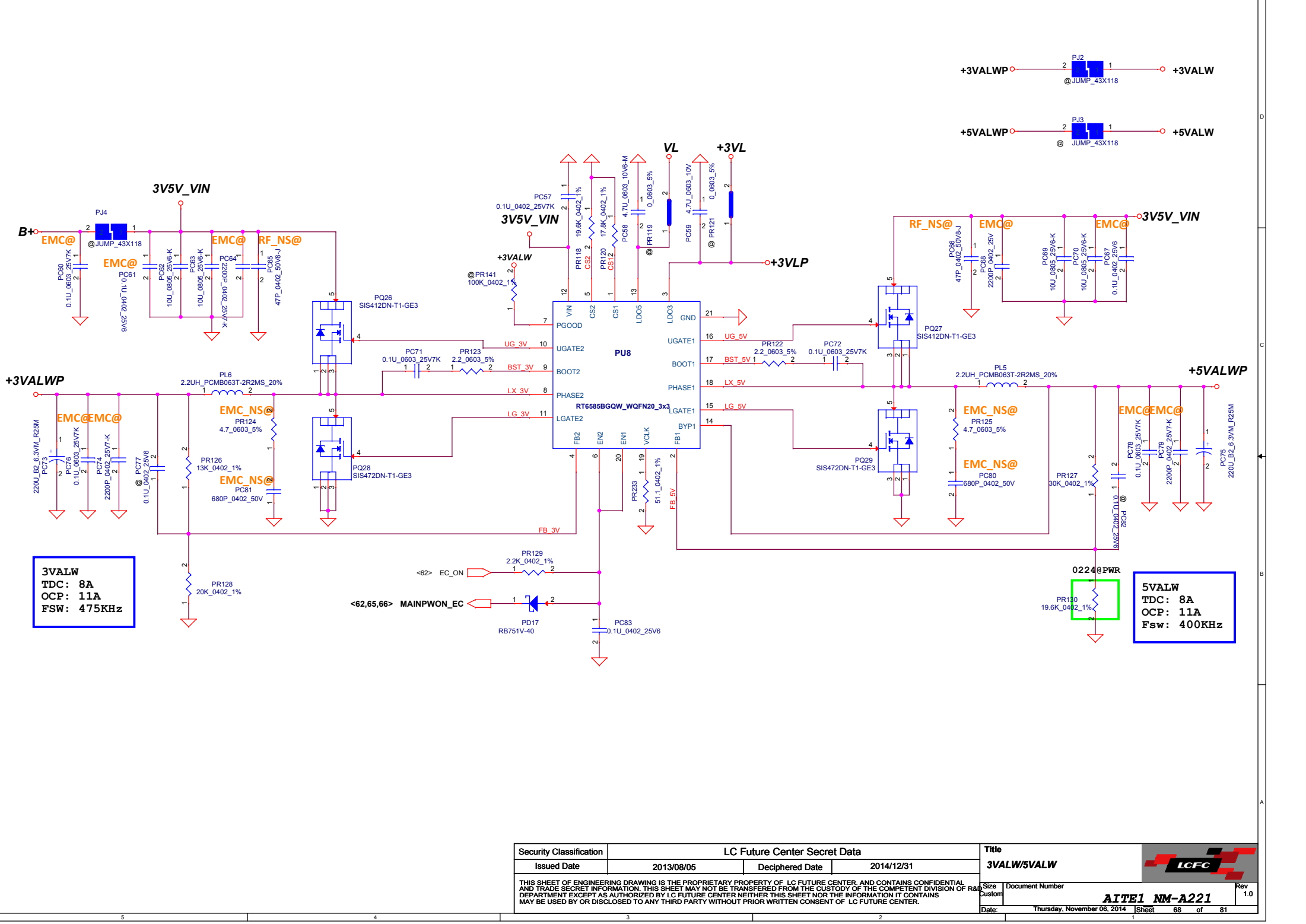
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Size	Document Number			Rev	
				1.0	
Date:	Thursday, November 06, 2014	Sheet	67	of	81

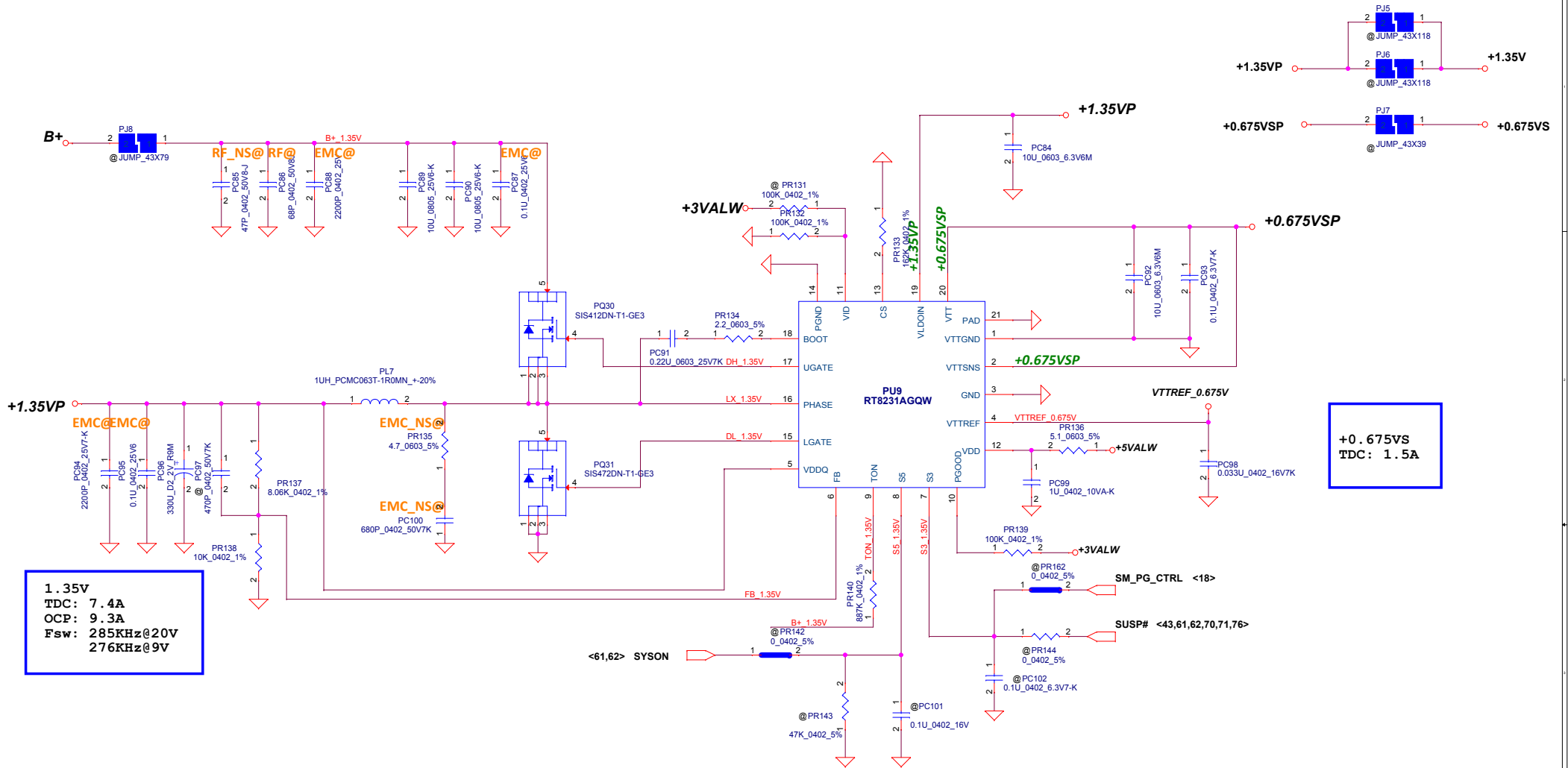


**3VALW**  
 TDC: 8A  
 OCP: 11A  
 FSW: 475KHz

**5VALW**  
 TDC: 8A  
 OCP: 11A  
 Fsw: 400KHz

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Title		
3VALW/5VALW		
Size	Document Number	<b>AITE1 NM-A221</b>
Custom		
Date:	Thursday, November 06, 2014	Sheet 68 of 81



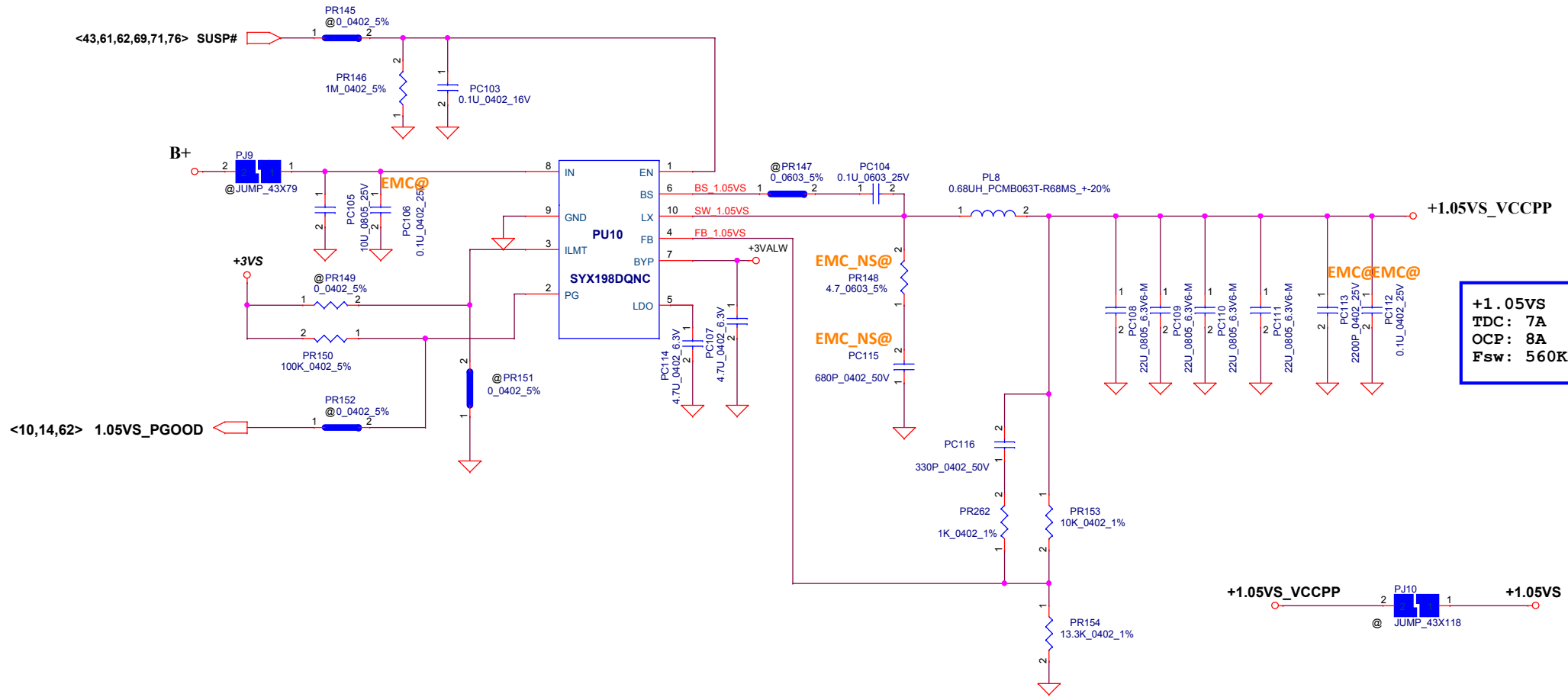
**1.35V**  
**TDC: 7.4A**  
**OCP: 9.3A**  
**Fsw: 285KHz@20V**  
**276KHz@9V**

**+0.675VS**  
**TDC: 1.5A**

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Date:	Thursday, November 06, 2014	

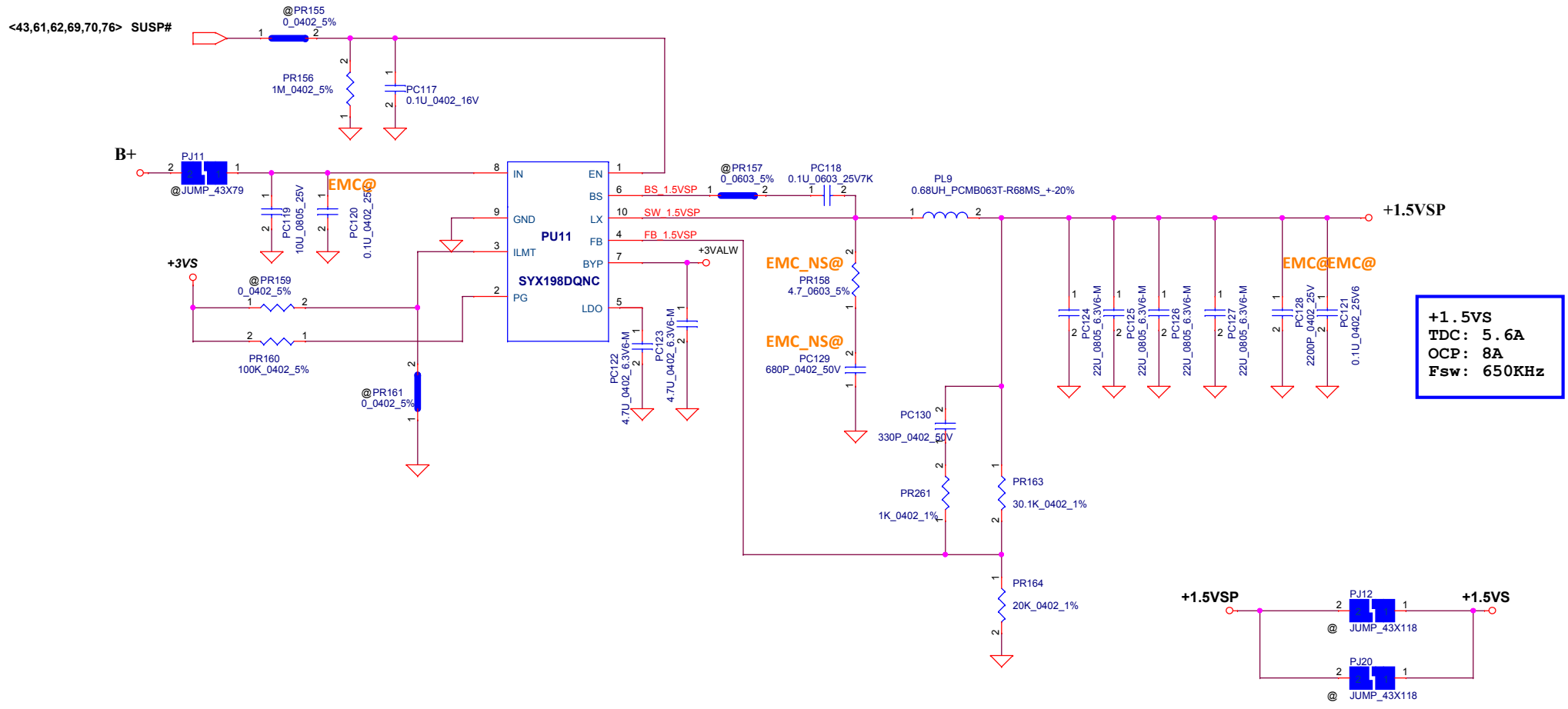




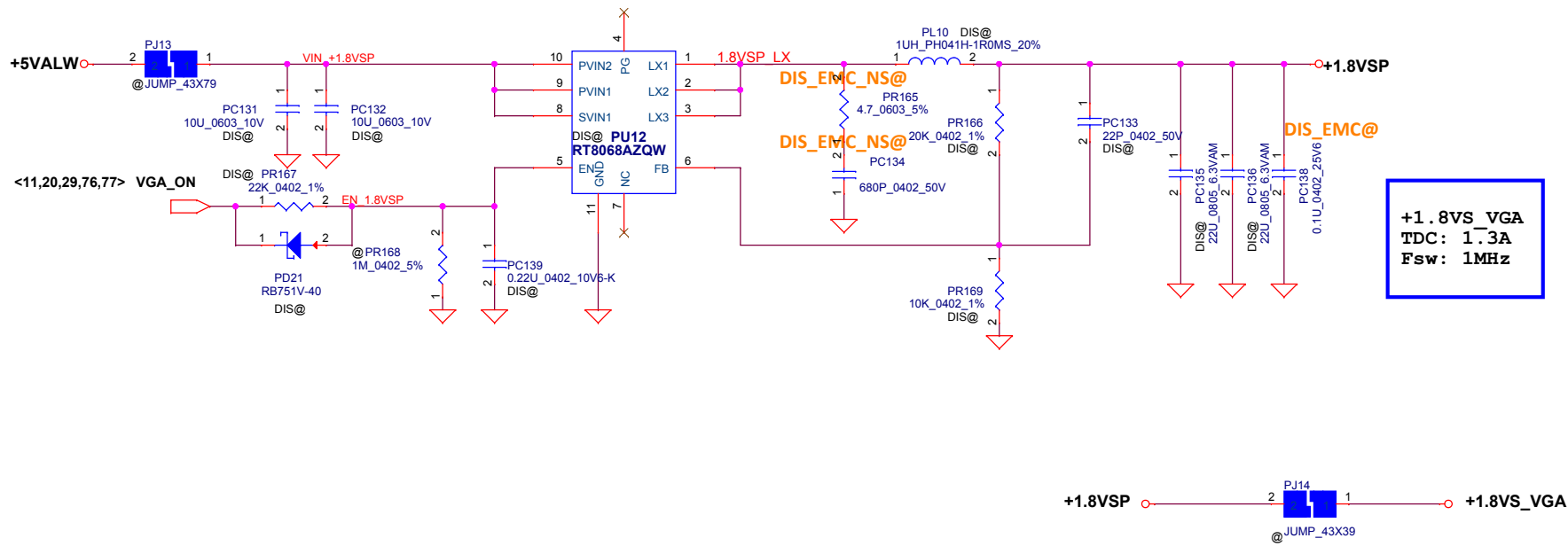
**+1.05VS**  
**TDC: 7A**  
**OCP: 8A**  
**Fsw: 560KHz**


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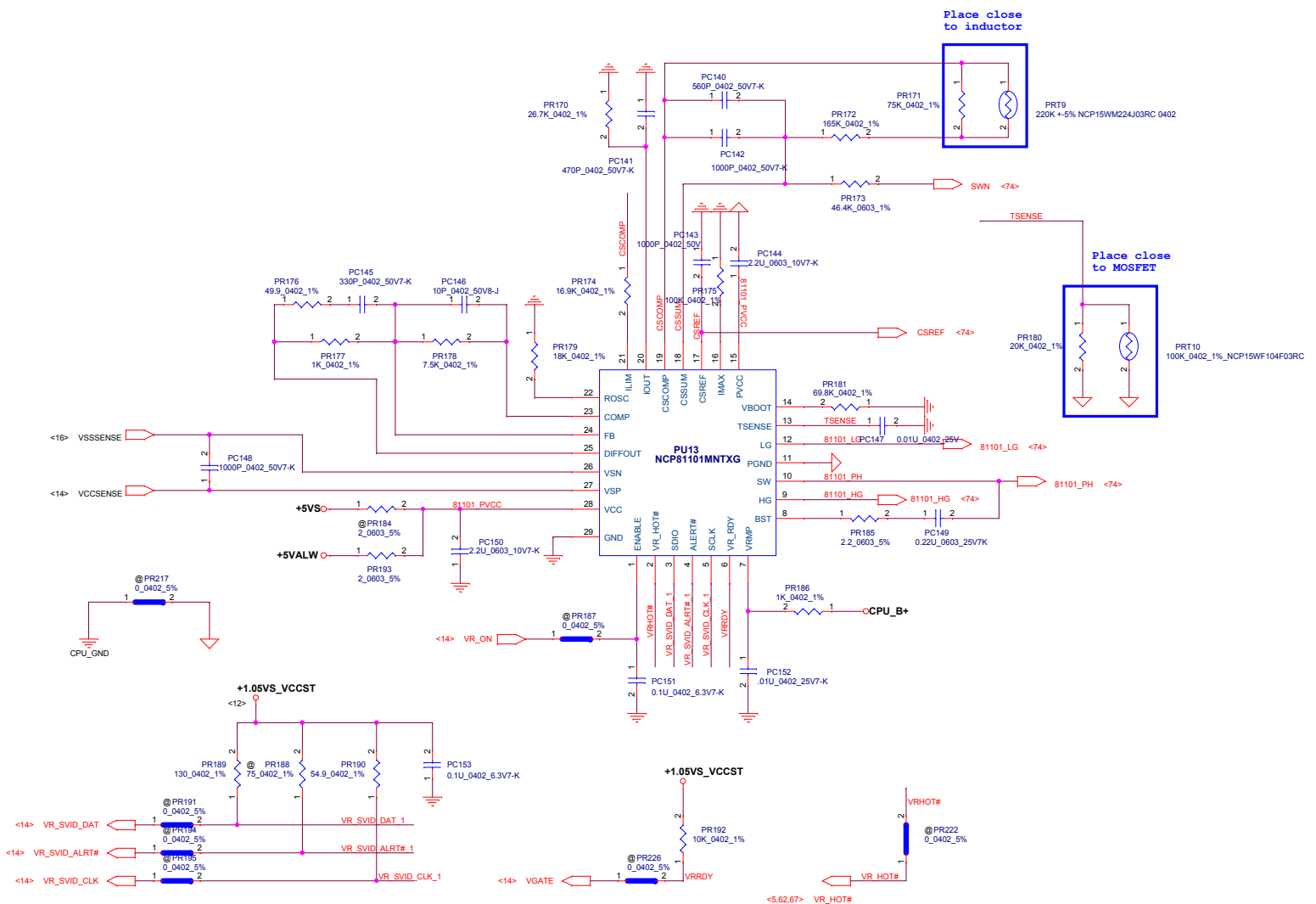


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			Sheet	71 of 81
			Rev	1.0

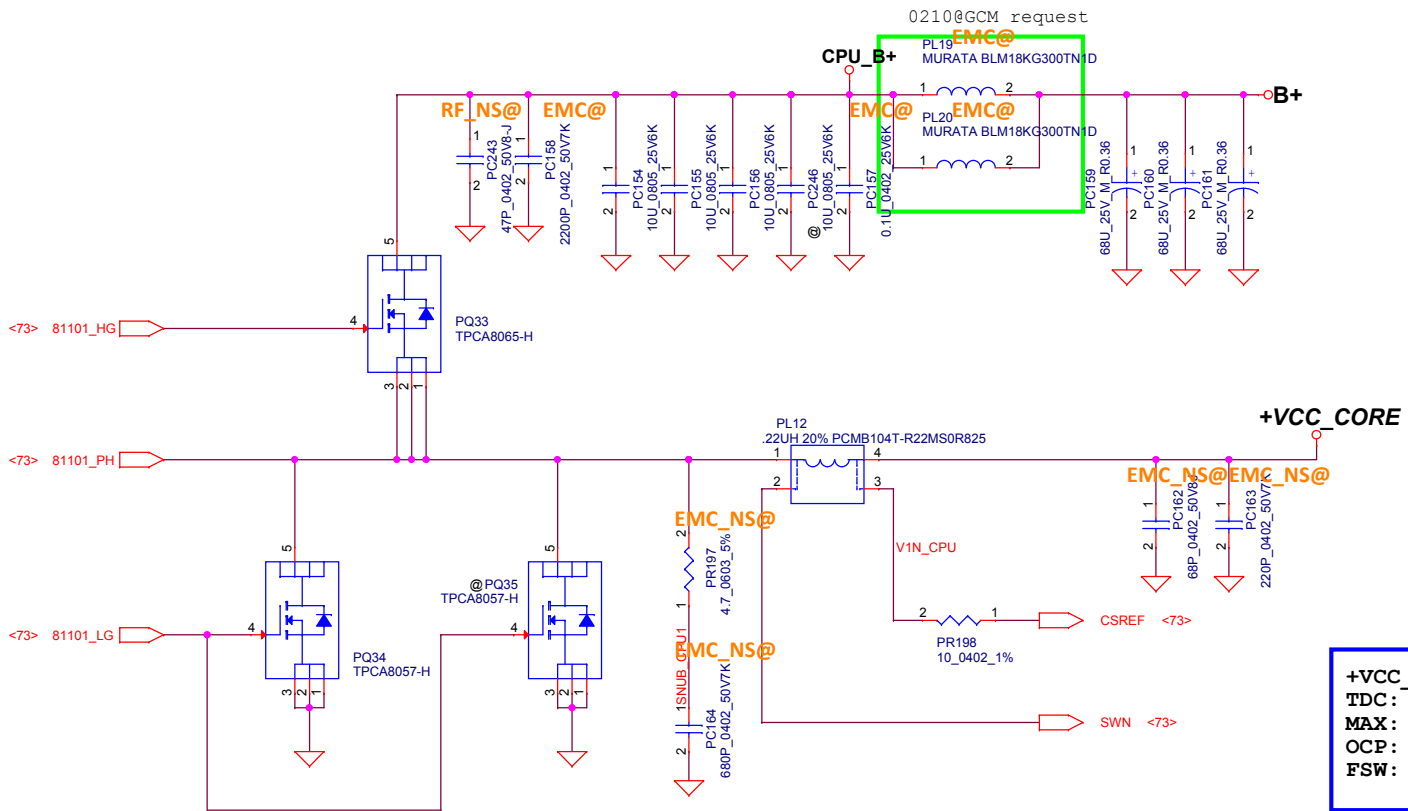


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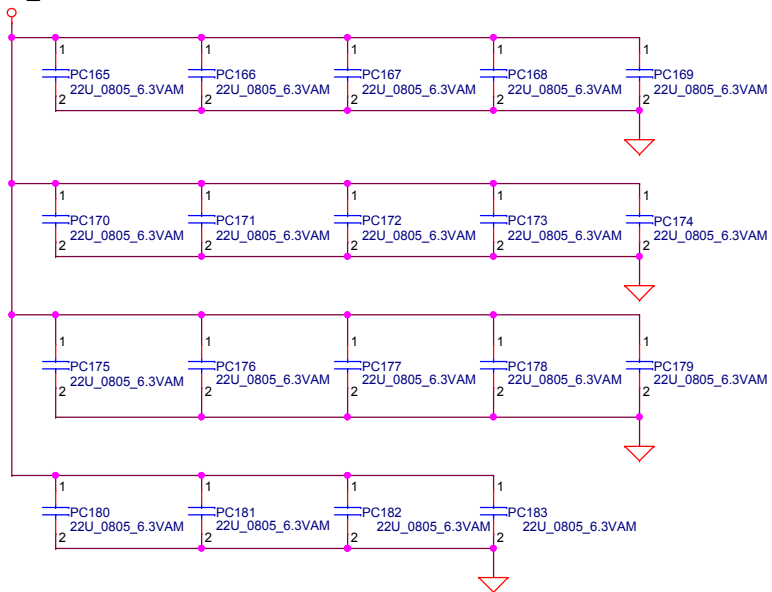
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Based on PDDG rev 0.7 Table 5-1.

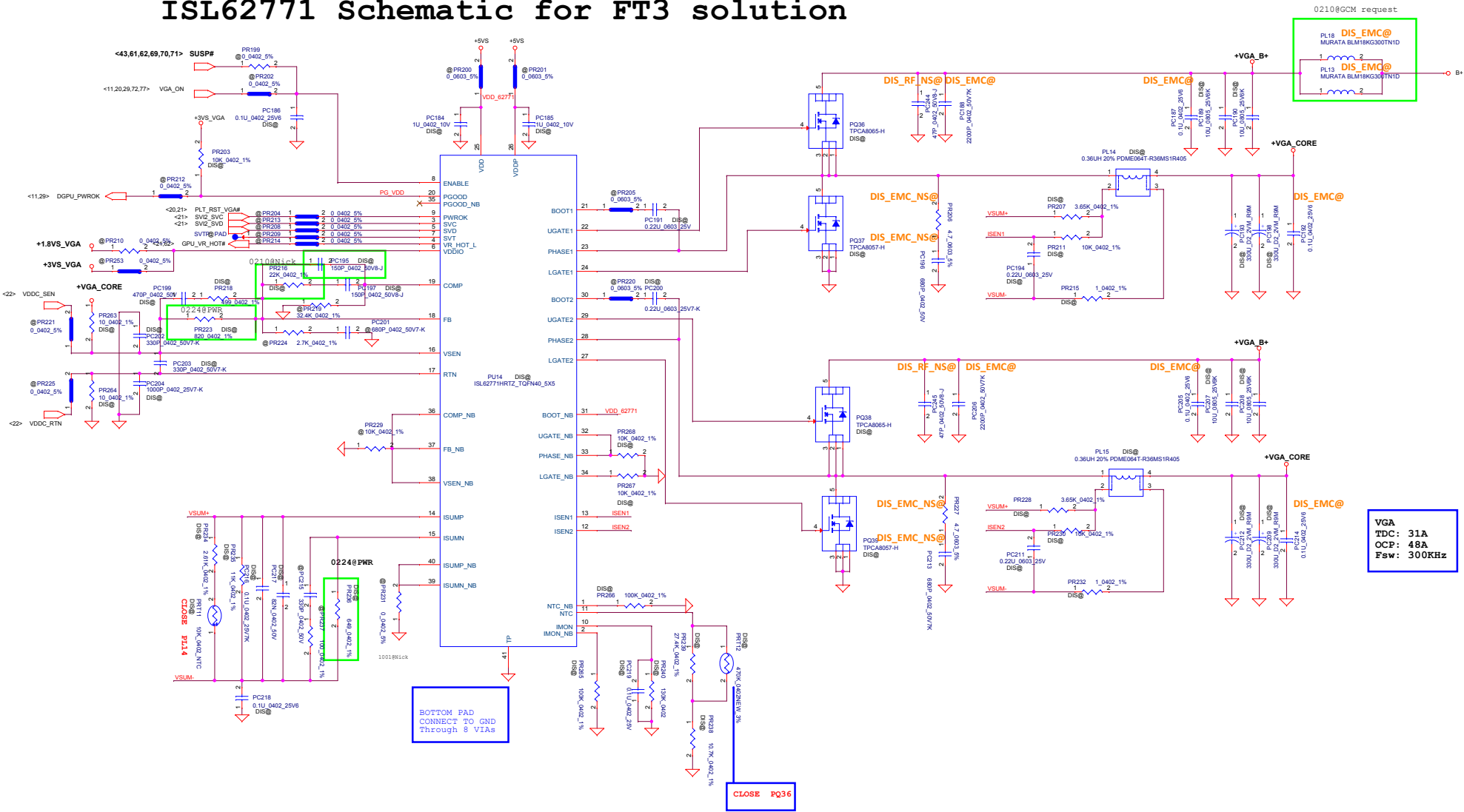
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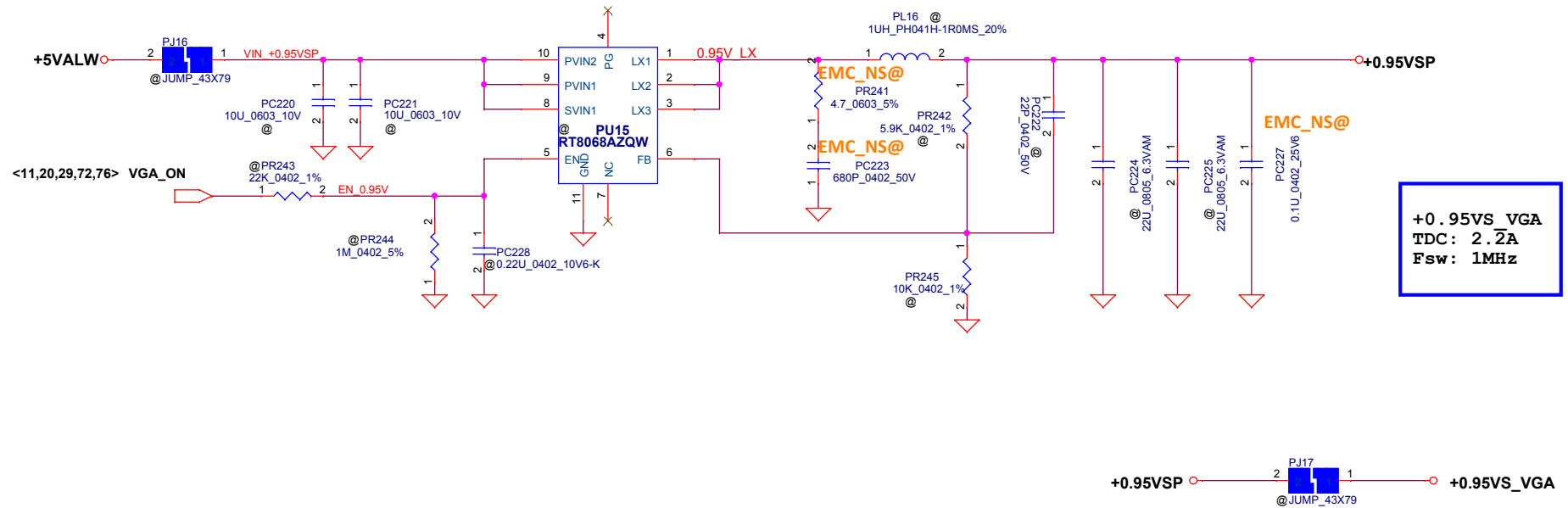
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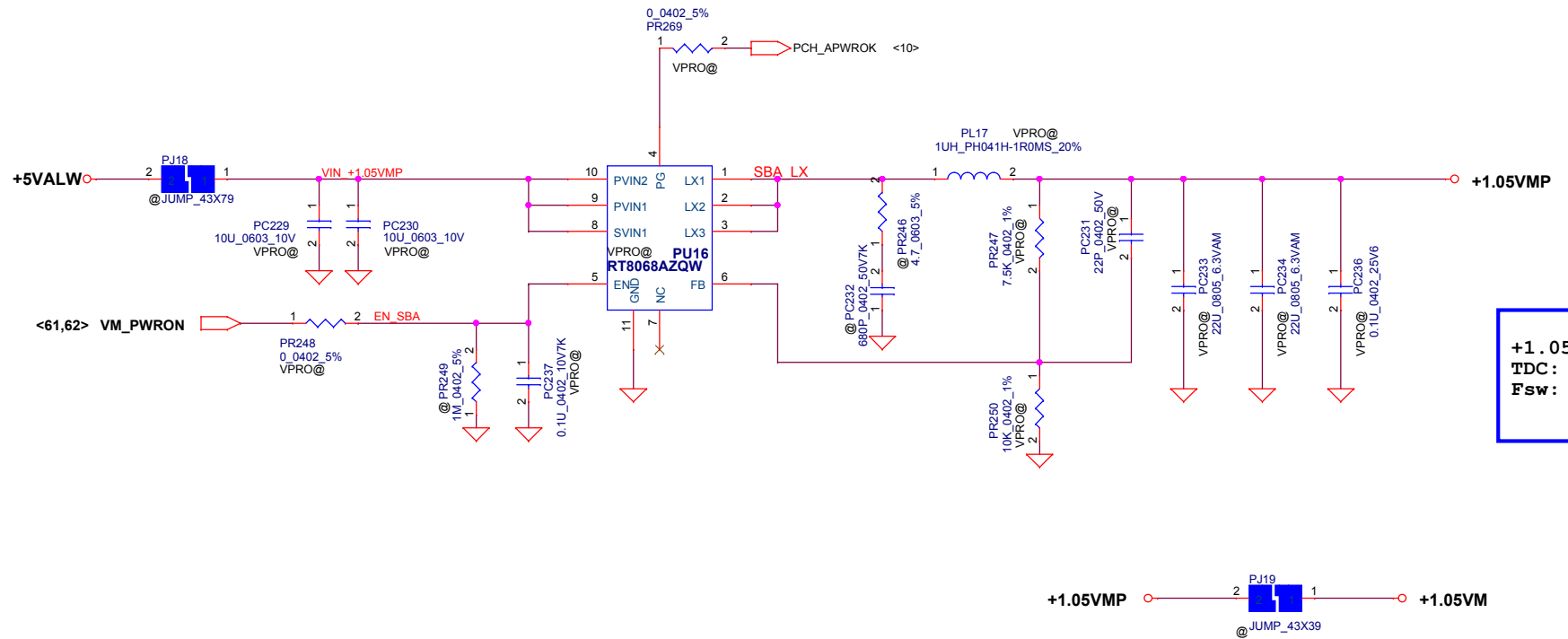
# ISL62771 Schematic for FT3 solution




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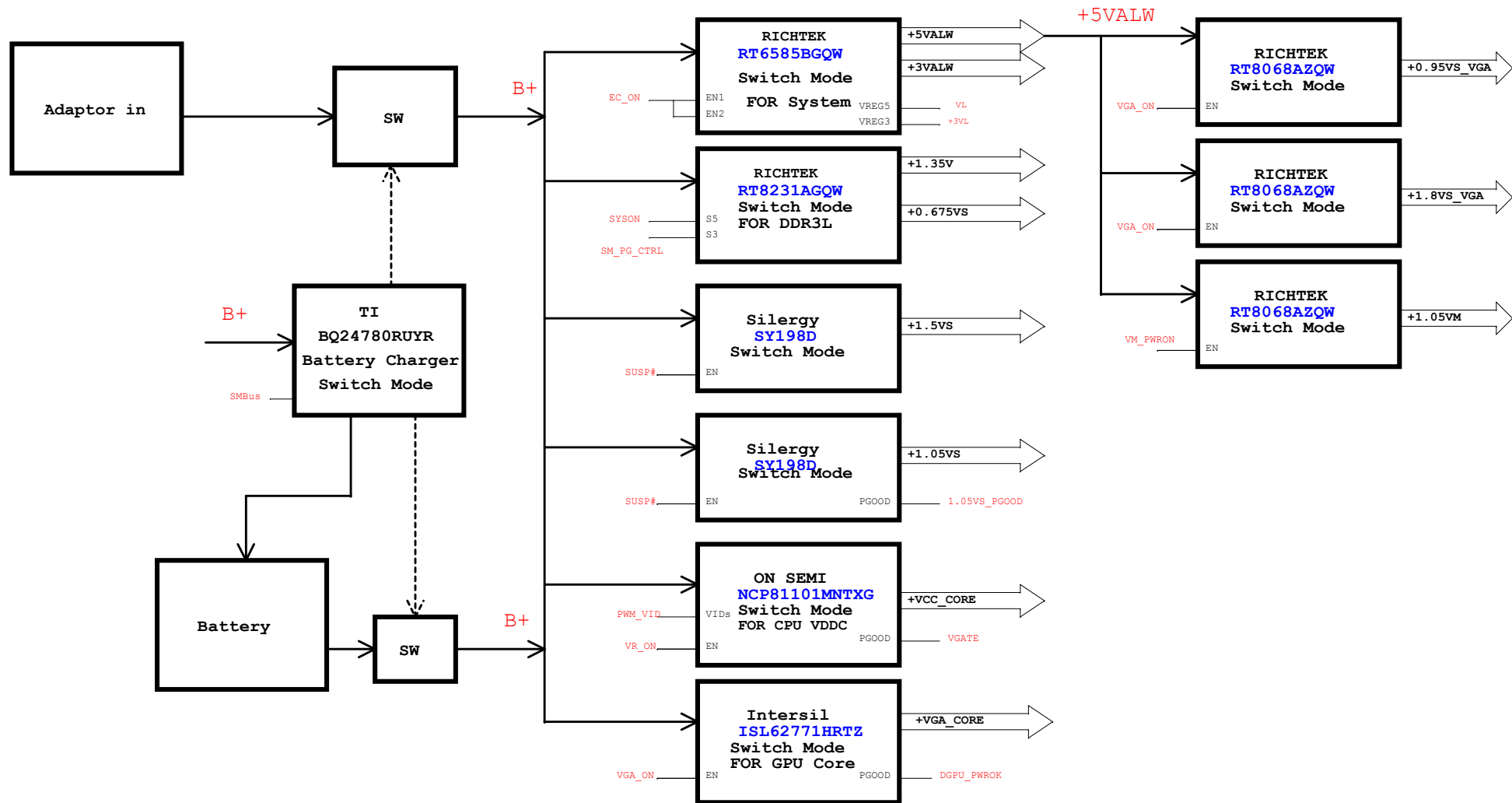
**+1.05VMP**  
**TDC: 1A**  
**Fsw: 1MHz**


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# POWER PIR (Product Improve Record)

AIIE1 NM-A151 SCHEMATIC CHANGE LIST  
 REVISION CHANGE: 0.1  
 GERBER-OUT DATE: 2013/01/16

NO DATE PAGE MODIFICATION LIST PURPOSE




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# HW PIR (Product Improve Record)

AIVE1 NM-XXXX SCHEMATIC CHANGE LIST  
 REVISION CHANGE: 0.1  
 GERBER-OUT DATE: 2013/10/15

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# Gordon SDV LOGIC SCHEMATICS

NMA-221  
VER 0.1  
Nov/13/2013

1.COVER PAGE  
2.BLOCK DIAGRAM  
3.NOTE LIST  
4.VGA NOTE  
5.BDW\_DDI/EDP/XDP  
6.BDW\_DDR3L INT  
7.BDW\_RTC/HDA/SATA/PCIe/JTAG  
8.BDW\_CLOCK/PM  
9.BDW\_LPC/SPI/SM BUS  
10.BDW\_SYS PM  
11.BDW\_eDP SBAND/DDPx  
12.BDW\_GPIO/SIO  
13.BDW\_PCIE/USB BUS  
14.BDW (Power)  
15.BDW (Power2)  
16.BDW (VSS)  
17.BDW (OTHER)  
18.DDR3L DIMM1  
19.DDR3L DIMM2  
20.Opal & Jet PCIE  
21.Opal & Jet GPIO  
22.Opal & Jet Core Power  
23.Opal & Jet DP Power/GND  
24.Opal & Jet MEM Interface  
25.Opal & Jet DDR3 VRAM U  
26.Opal & Jet DDR3 VRAM L  
27.Opal 22 TO 24 VRAM U2  
28.Opal 23 TO 25 VRAM L2  
29.Opal & Jet swich power  
30.BLANK  
31.BLANK  
32.CARDREADER IC/CONN.  
33.DP RP --> BLANK  
34.DOCKING/ DCIN CONN  
35.CX20751

36.HP/MIC JACK/Speaker  
37.SATA HDD/ODD CONN.  
38.eDP/CMOS CONN.  
39.USB30 RP --> BLANK  
40.USB3 PORT1-BACK  
41.USB3 PORT2-FRONT(AOU)  
42.MUX IC  
43.DP TO VGA  
44.VGA CONN.  
45.HDMI RP --> BLANK  
46.HDMI CONN.  
47.GBE LAN PHY  
48.RJ45 CONN.  
49.CP/TPOINTCONN.  
50.PBTN/LID/FP/FAN CONN.  
51.KB/RTC/TOUCH PAN CONN.  
52.WWAN/WLAN NGFF CONN.  
53.SUB CONN. --> BLANK  
54.SUB-AUDIO JACK CONN.  
55.THERMAL SENSOR  
56.G SENSOR/TPM  
57.BLANK  
58.BLANK  
59.BLANK  
60.BLANK  
61.DC V TO VS/ V-PCH/VM  
62.EC\_IT8586E/FX  
63.PLW/SCREW HOLE  
64.BLANK  
65.DCIN / Vin Detector  
66.BATTERY CONN/OTP  
67.CHARGER(BQ24780)  
68.3V/5VALW(RT6585B)  
69.+1.35V/+0.675V(RT8231A)  
70.+1.05VS(SYX198DQNC)

71.+1.5VS(SYX198DQNC)  
72.+1.8VS\_VGA(RT8068A)  
73.+VCC\_CORE(NCP81101MNTXG)  
74.+VCC\_CORE2  
75.PROCESSOR DECOUPLING  
76.+VGA\_CORE(ISL62771)  
77.+0.95VS\_VGA(RT8068A)  
78.+1.05VM(RT8068A)  
79.PWR-PIR  
80.HW PIR

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