LE4 BLOCK DIAGRAM

Yonah /Calistoga /ICH-7m

1

BOM MARK

E@ EXT VGA POPULATE
I@ INV VGA POPULATE
F@ FIR MODULE POPULATE
4@ 4401 10/100M POPULATE
5@ 5788 1G POPULATE

VGA NVIDA G72M (64 Bit B/W)
16M*16(128MB)
(Bank*4)
PG 18,19,20,21

CPU Yonah/Merom
31W/35W
(478 Micro-FCPGA)
PG 4,5

CPU THERMAL SENSOR
PG 5

14.318MHz

CLOCK GEN
IDTXXX/ ICSXXXX
56pins
PG 3

CPUCLK, CPUCLK#
SBLINKCLK, SBLINKCLK#
NBSRCCLK, NBSRCCLK#
HTREFCLK

HyperThansport I/O BUS
16X PCI-E
Link 16x16

NORTH BRIDGE Calistoga
945GM / 945PM / 940GML
INTEGRADED VGA FUNCTION
1466 BGA
PG 6,7,8,9,10,11

OSC14M

DDRII 266,333 MHz
DDRII 266,333 MHz

DDRII-SODIMM1
PG 16,17

DDRII-SODIMM2
PG 16,17

EXT_CRT
EXT_LVDS
EXT_TV-OUT

SWITCH CIRCUIT

INT_CRT
INT_LVDS
INT_TV-OUT

CRT port PG 23
LCD Panel PG 22
S-VIDEO PG 23

DMI LINK 2X PCI-E

32.768KHz

NBSRCCLK, NBSRCCLK#

33MHZ, 3.3V PCI

USB PORT 0,2,6 PG 31
USB 2.0

SATA-HDD PG 32

PATA-CDROM PG 32
ATA 66/100/133

ICH7-M
652 BGA
PG 12,13,14,15

Azalia

MIC IN
PG 28

Conexant Audio
CX20549-12
PG 28

LAN
BCM4401/5788
PG 33

25MHz

24.576MHz

CARDREADER / IEEE 1394 CONTROLLER/CF
TI 8412
PG 24,25

3 IN 1
CARD READER SD, SM, MS,
PG 25

CARDBUS SOCKET PG 25

1394 CONN PG 24

LPC
3.3V LPC, 33MHz
PCLK_E

32.768KHz

IO/B CON. SIO (87383) PG 26

PC87551L PG 30

Express Card x1 MINI PICE CARD
USB PORT 1
PG 27

AMP MAX9755 PG 29

MDC CONN PG 27

WIRE

SPEKER PG 29

INT_SPK PG 29

IO/B RJ11 JACK PG 24

RJ45 JACK PG 34

IR module PG 26
FAN PG 31
Touchpad PG 31
Keyboard PG 26
FLASH PG 30

SYSTEM POWER MAX1993 (1.2V/NB_CORE/1.25V) PG 41

CPU CORE MAX8771 POWER VCORE 1.2V /44A PG 38

SYSTEM MAX8734 POWER(3/5V) PG 39

SYSTEM POWER MAX8632 (1.8VSUS/0.9V SMDDR_VREF) PG 36

BATT CHARGER MAX8724 PG 35

DISCHARGE PG 40

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : VCC
LAYER 5 : IN2
LAYER 6 : IN3
LAYER 7 : GND
LAYER 8 : BOT

PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

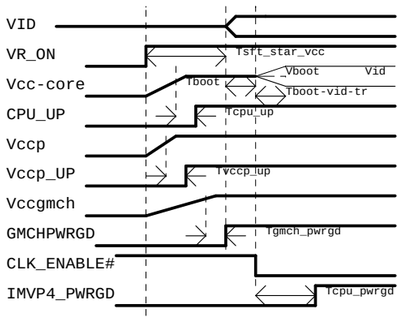
Date: Wednesday, November 16, 2005 Sheet 1 of 42

Board Stack up Description

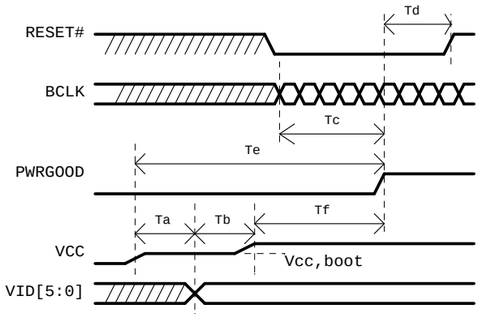
PCB Layers

Layer 1		TOP(Component,Other)
Layer 2		Ground Plane
Layer 3		IN1
Layer 4		Power Plane
Layer 5		IN2
Layer 6		IN3
Layer 7		Ground Plane
Layer 8		BOTTOM

Power On Sequencing Timing Diagram



Dothan Power-up Timing Specifications

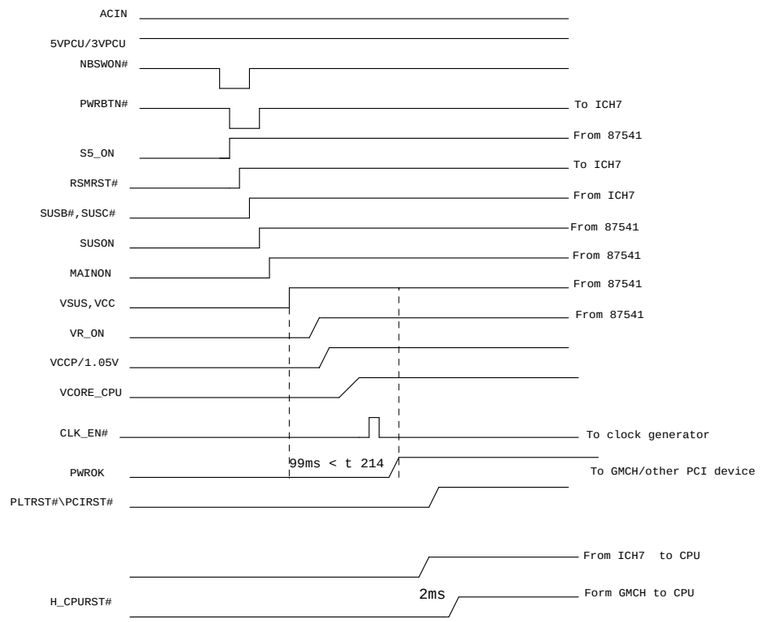


Ta=VCC and VCCP asseration to VID[5:0] vaild
Tb=VID[5:0] stable to VCC vaild
Tc=BCLK stable to PWRGOOD assertion
Td=PWRGOOD to RESET# de-assertion time
Te=Vcc,boot vaild to PWRGOOD assertion time

Voltage Rails

Voltage Rails		ON S0~S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE	Core voltage for Processor	X				VR_ON 0.726V~0.94V
VCCP	Core voltage for CPU / NB	X				VR_ON
SMDDR_VTERM	0.9V for DDR2 Termination voltage	X				MAINON
RVCC1.5		X	X	X		RVCC_ON
RVCC3		X	X	X		RVCCD
VCC1.5		X				MAIND
VCC2.5		X				MAINON
VCC3		X				MAIND
VCC5		X				MAIND
1.8VSUS		X	X			SUSON
3VSUS		X	X			SUSD
5VSUS		X	X			SUSD
3VPCU		X	X	X	X	VL
5VPCU		X	X	X	X	VL
9VPCU		X	X	X	X	5VPCU

ACIN POWER ON TIMING



Voltage Rails		ON S0~S1	ON S3	ON S4	ON S5	Control signal
VCC_CORE	Core voltage for Processor	X				VRON
GMCH_VTT	Core voltage for GMCH 1.05V	X				MAINON
SMDDR_VTERM	0.9V for DDR II Termination voltage	X				MAINON
SMDDR_VREF	0.9V for DDR II Reference Voltage	X				MAINON
GMCH_1.5V		X				MAINON
1.8VSUS	1.8V for DDR II voltage	X	X			SUSON
+2.5V		X				MAINON
3VPCU		X	X	X	X	VL
3VSUS		X	X			SUSON
+3V		X				MAINON
5VPCU		X	X	X	X	VL
5VSUS		X	X			SUSON
+5V		X				MAINON
VIN	POWER SOURCE	X	X	X	X	

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7402	AD25	REQ1# / GNT1#	PIRQ B/C/D

PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	System Information	1A

Date: Wednesday, November 16, 2005 Sheet 2 of 42

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

Place these termination to close CK410M. Cause those Pin-out is for Current-Mode.

R199 1 2 49.9/F_4
R200 1 2 49.9/F_4
R196 1 2 49.9/F_4
R197 1 2 49.9/F_4

C323 33P_4 2 1
C324 33P_4 2 1
Y2 14.318MHZ BG614318081
XIN <500mil
XOUT

U17

50 XTAL_IN
49 XTAL_OUT
37 VDDA
38 VSSA
52 REF 14M_REF
10 VTT_PWRGD#/PD#
55 PCI_STOP#
54 CPU_STOP#
46 SCLK
47 SDATA
12 FSA/USB_48
16 FSB/TEST_MODE
53 FSC/TEST_SEL
48 VDD_REF
42 VDD_CPU
1 VDD_PCI_1
7 VDD_PCI_2
21 VDD_SRC0
28 VDD_SRC1
34 VDD_SRC2
11 VDD_48
39 IREF
14 DOT96
15 DOT96#
13 GND_48
51 GND_REF
2 GND_PCI_1
6 GND_PCI_2
29 GND_SRC
45 GND_CPU

CK-410M

ICS954206AGLFT
250mA (MAX.)

CPU0 44 R_HCLK_CPU 43 R_HCLK_CPU# RP34 4P2R-S-33 → CLK_CPU_BCLK (4) CLK_CPU_BCLK# (4)
CPU1 41 R_HCLK_MCH 40 R_HCLK_MCH# RP39 4P2R-S-33 → CLK_MCH_BCLK (6) CLK_MCH_BCLK# (6)
CPU2_ITP/SRC7 36 R_PCIE_VGA 35 R_PCIE_VGA# RP43 4P2R-S-33 → CLK_PCIE_VGA (18) CLK_PCIE_VGA# (18)
SRC6 33 SRC6# 32
SRC5 31 R_MCH_3GPLL RP47 30 R_MCH_3GPLL# 4P2R-S-33 → CLK_PCIE_3GPLL (7) CLK_PCIE_3GPLL# (7)
SRC4 26 R_PCIE_SATA RP48 27 R_PCIE_SATA# 4P2R-S-33 → CLK_PCIE_SATA (12) CLK_PCIE_SATA# (12)
SRC3 24 R_PCIE_ICH RP44 25 R_PCIE_ICH# 4P2R-S-33 → CLK_PCIE_ICH (13) CLK_PCIE_ICH# (13)
SRC2 22 R_PCIE_MINI RP40 23 R_PCIE_MINI# 4P2R-S-33 → CLK_PCIE_MINI (27) CLK_PCIE_MINI# (27)
SRC1 19 SRC1# 20
SRC0 17 R_DREFSSCLK RP37 18 R_DREFSSCLK# I@4P2R-S-33 → DREFSSCLK (7) DREFSSCLK# (7)
PCI5 5 R_PCLK_LAN R186 33_4 → PCLK_LAN (33)
PCI4 4 R_PCLK_LPC R181 33_4 → PCLK_LPC (26)
PCI3 3 R_PCLK_LPC_DEBUG R178 33_4 → PCLK_LPC_DEBUG (27)
PCI2 56 R_PCLK_PCM R182 33_4 → PCLK_PCM (24)
PCIF1 9 R_PCLK_SIO R194 33_4 → PCLK_541 (30)
PCIF0/ITP_EN 8 PCIF0 R189 *10K_4 → +3VRUN; R183 10K_4; R185 33_4 → PCLK_ICH (13)

PCIF1 1:100 Mhz 0:96 Mhz

R192 1 2 33_4 → 14M_SIO (26)
R188 1 2 33_4 → 14M_ICH (14)
C366 *10P_4
C361 *10P_4

(14,37) CLK_EN# → 10
(14) PM_STPPCI# → 55
(14) PM_STPCPU# → 54
(25) TI_CLK48M R195 1 2 10_4
(14) CLKUSB_48 R190 1 2 10_4
CGCLK_SMB → 46
CGDAT_SMB → 47

SMbus address D2

(4,7) CPU_MCH_BSEL0 R193 1 2 8.2K/F_4 → FSA → 12
(4,7) CPU_MCH_BSEL1 → FSB → 16
(4,7) CPU_MCH_BSEL2 R184 1 2 8.2K/F_4 → FSC → 53

LE4 A:
Changed new function

Solved sometimes can't power on

VDDREF_CR → CLKVDD → 48, 42
CLKVDD1 → 1, 7
CLKVDD → 21, 28, 34
VDD48_CR → 11

R201 1 2 475/F_4 IREF → 39

Iref=5mA,
Ioh=4*Iref

+3VRUN

LE4 B:

Add R566 pull high with FSA

R566 10K_4
FSA
R567 *10K_4

(7) DOT96 → I@4P2R-S-33 RP35 → R_DOT96 → R_DOT96# → 14, 15
(7) DOT96#

0816a

CT_0505: Change footprint to TSSOP56-8_1-5 from TSSOP56-240

Connect ICH6 SMB

(14,33) PDAT_SMB → Q32 RHU002N06 → CGDAT_SMB → CGDAT_SMB (16,17,27)
(14,33) PCLK_SMB → Q33 RHU002N06 → CGCLK_SMB → CGCLK_SMB (16,17,27)

RP33 4P2R-S-10K

These are for backdrive issue

Connect DDR Module's SMB

CT_0229: Change MOS to RHU002N06 due to layout concern.

Bypass CAPs need to follow Bypass CAP. Routing Rule, no vias between CAP to CHIPSET VCC Pin or GND.

Tie to VCC (Logic 1) is for ITP using.
Tie to GND (Logic 0) is for PCIE using.

120 ohms@100Mhz L25 HB-1T2012-121JT_8 → CLKVDD1
C351 0.047U/10V_4
C565 0.047U/10V_4
C326 4.7U/10V_8

R177 2.2 → VDD48_CR
C374 0.047U/10V_4
C340 4.7U/10V_8

R191 1R_6 → VDDREF_CR
C564 0.047U/10V_4

120 ohms@100Mhz L31 HB-1T2012-121JT_8 → CLKVDD
C387 0.047U/10V_4
C573 0.047U/10V_4
C383 0.047U/10V_4
C579 0.047U/10V_4
C388 4.7U/10V_8

R204 2.2 → VDDA_CR
C578 0.047U/10V_4
C393 4.7U/10V_8

CLK_PCIE_VGA / CLK_PCIE_VGA# RP42 49.9_4P2R
CLK_PCIE_MINI / CLK_PCIE_MINI# RP41 49.9_4P2R
CLK_MCH_3GPLL / CLK_MCH_3GPLL# RP46 49.9_4P2R
CLK_PCIE_SATA / CLK_PCIE_SATA# RP49 49.9_4P2R
CLK_PCIE_ICH / CLK_PCIE_ICH# RP45 49.9_4P2R
DREFSSCLK / DREFSSCLK# RP38 I@49.9_4P2R
DOT96 / DOT96# RP36 I@49.9_4P2R

Place these termination to close CK410M. Cause those Pin-out is for Current-Mode.

PCLK_LAN C359 *10P_4
PCLK_PCM C432 *10P_4
PCLK_541 C566 *10P_4
PCLK_LPC_DEBUG C350 *10P_4
PCLK_LPC C355 *10P_4
PCLK_ICH C442 *10P_4

LE4 A:
Add Cap 10p reserve for EMI E-mail 093020051211

LE4 A:
Del this function desgin

PROJECT : LE4
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Size	Document Number	Rev
	CLOCK GENERATOR	1A
Date: Tuesday, March 14, 2006	Sheet 3 of 42	

U38A

ADDR GROUP 0
(6) H_A#[31:3]
H_A#3 J4 — A[3]#
H_A#4 L4 — A[4]#
H_A#5 M3 — A[5]#
H_A#6 K5 — A[6]#
H_A#7 M1 — A[7]#
H_A#8 N2 — A[8]#
H_A#9 J1 — A[9]#
H_A#10 N3 — A[10]#
H_A#11 P5 — A[11]#
H_A#12 P2 — A[12]#
H_A#13 L1 — A[13]#
H_A#14 P4 — A[14]#
H_A#15 P1 — A[15]#
H_A#16 R1 — A[16]#
(6) H_ADSTB#0 — L2 — ADSTB[0]#

REQ[0]#
REQ[1]#
REQ[2]#
REQ[3]#
REQ[4]#
(6) H_REQ#[4:0]
H_REQ#0 K3
H_REQ#1 H2
H_REQ#2 K2
H_REQ#3 J3
H_REQ#4 L5

ADDR GROUP 1
H_A#[31:3]
H_A#17 Y2 — A[17]#
H_A#18 U5 — A[18]#
H_A#19 R3 — A[19]#
H_A#20 W6 — A[20]#
H_A#21 U4 — A[21]#
H_A#22 Y5 — A[22]#
H_A#23 U2 — A[23]#
H_A#24 R4 — A[24]#
H_A#25 T5 — A[25]#
H_A#26 T3 — A[26]#
H_A#27 W3 — A[27]#
H_A#28 W5 — A[28]#
H_A#29 Y4 — A[29]#
H_A#30 W2 — A[30]#
H_A#31 Y1 — A[31]#
(6) H_ADSTB#1 — V4 — ADSTB[1]#

THERM
(12) H_A20M# — A6 — A20M#
(12) H_FERR# — A5 — FERR#
(12) H_IGNNE# — C4 — IGNNE#

H CLK
(12) H_STPCLK# — H_STPCLK# — D5 — STPCLK#
(12) H_INTR — C6 — LINT0
(12) H_NMI — B4 — LINT1
(12) H_SMI# — A3 — SMI#

LE4 A:
Modfiy circuit

RESERVED
T188 TP_A32# AA1
T187 TP_A33# AA4
T189 TP_A34# AB2
T186 TP_A35# AA3
T44 TP_A36# M4
T48 TP_A37# N5
T49 TP_A38# T2
T47 TP_A39# V3
T59 TP_APM0# B2
T51 TP_APM1# C3
T208 TP_HFPLL B25
RSVD[01]#
RSVD[02]#
RSVD[03]#
RSVD[04]#
RSVD[05]#
RSVD[06]#
RSVD[07]#
RSVD[08]#
RSVD[09]#
RSVD[10]#
RSVD[11]#
RSVD[12]#
RSVD[13]#
RSVD[14]#
RSVD[15]#
RSVD[16]#
RSVD[17]#
RSVD[18]#
RSVD[19]#
RSVD[20]#
D2 TP_SPARE0 — T57
F6 TP_SPARE1 — T61
D3 TP_SPARE2 — T53
C1 TP_SPARE3 — T190
AF1 TP_SPARE4 — T193
D22 TP_SPARE5 — T76
C23 TP_SPARE6 — T77
C24 TP_SPARE7 — T207
T22 TP_EXTBREF — T75

PZ47903-2741-01

CONTROL
ADS# H1 — H_ADS# (6) — T58
BNR# E2 — H_BNR# (6)
BPRI# G5 — H_BPRI# (6)
DEFER# H5 — H_DEFER# (6)
DRDY# F21 — H_DRDY# (6)
DBSY# F1 — H_DBSY# (6)
BR0# F1 — H_BREQ#0 (6)
IERR# D20
INIT# B3 — H_INIT# (12) — T195
LOCK# H4 — H_LOCK# (6)
H_CPURST# (6)
RESET# B1
RS[0]# E3 — H_RS#0
RS[1]# F4 — H_RS#1
RS[2]# G3 — H_RS#2
H_RS#[2:0] (6)
TRDY# G2 — H_TRDY# (6) — T56
HIT# G6 — H_HIT# (6)
HITM# E4 — H_HITM# (6)

XDP/ITP SIGNALS
BPM[0]# AD4 XDP_BPM#0 — T70
BPM[1]# AD3 XDP_BPM#1 — T67
BPM[2]# AD1 XDP_BPM#2 — T64
BPM[3]# AC4 XDP_BPM#3 — T65
PRDY# AC2 XDP_BPM#4 — T55
PREQ# AC1 XDP_BPM#5
TCK AC5 XDP_TCK
TDI AA6 XDP_TDI
TDO AB3 XDP_TDO — T191
TMS AB5 XDP_TMS
TRST# AB6 XDP_TRST#
DBR# C20 XDP_DBRESET#

LE4 A:
Modfiy circuit

THERM
PROCHOT D21 H_PROCHOT#
THERMDA A24 H_THERMDA — H_THERMDA (5)
THERMDC A25 H_THERMDC — H_THERMDC (5)
THERMTRIP# C7 PM_THRMTRIP# — PM_THRMTRIP# (7,12)

H CLK
BCLK[0] A22 — T228 — CLK_CPU_BCLK (3)
BCLK[1] A21 — T224 — CLK_CPU_BCLK# (3)

+1.05V
R458 56/F_4 — Near to MCH <500mils
+1.05V (5,6,7,9,10,12,15,38,40)
R198 75_4
XDP PU_R < 0.2"

U38B

DATA GRP 0
(6) H_D#[63:0]
H_D#0 F22 — D[0]#
H_D#1 F24 — D[1]#
H_D#2 E26 — D[2]#
H_D#3 H22 — D[3]#
H_D#4 F23 — D[4]#
H_D#5 G25 — D[5]#
H_D#6 E25 — D[6]#
H_D#7 E23 — D[7]#
H_D#8 K24 — D[8]#
H_D#9 G24 — D[9]#
H_D#10 J24 — D[10]
H_D#11 J23 — D[11]#
H_D#12 H26 — D[12]#
H_D#13 F26 — D[13]#
H_D#14 K22 — D[14]#
H_D#15 H25 — D[15]#
(6) H_DSTBN#0 — H23 — DSTBN[0]#
(6) H_DSTBP#0 — G22 — DSTBP[0]#
(6) H_DINV#0 — J26 — DINV[0]#

DATA GRP 2
H_D#[63:0]
D[32]# AA23 H_D#32
D[33]# AB24 H_D#33
D[34]# V24 H_D#34
D[35]# V26 H_D#35
D[36]# W25 H_D#36
D[37]# U23 H_D#37
D[38]# U25 H_D#38
D[39]# U22 H_D#39
D[40]# AB25 H_D#40
D[41]# W22 H_D#41
D[42]# Y23 H_D#42
D[43]# AA26 H_D#43
D[44]# Y26 H_D#44
D[45]# Y22 H_D#45
D[46]# AC26 H_D#46
D[47]# AA24 H_D#47
DSTBN[2]# W24 — H_DSTBN#2 (6)
DSTBP[2]# Y25 — H_DSTBP#2 (6)
DINV[2]# V23 — H_DINV#2 (6)

DATA GRP 1
H_D#[63:0]
H_D#16 N22 — D[16]#
H_D#17 K25 — D[17]#
H_D#18 P26 — D[18]#
H_D#19 R23 — D[19]#
H_D#20 L25 — D[20]#
H_D#21 L22 — D[21]#
H_D#22 L23 — D[22]#
H_D#23 M23 — D[23]#
H_D#24 P25 — D[24]#
H_D#25 P22 — D[25]#
H_D#26 P23 — D[26]#
H_D#27 T24 — D[27]#
H_D#28 R24 — D[28]#
H_D#29 L26 — D[29]#
H_D#30 T25 — D[30]#
H_D#31 N24 — D[31]#
(6) H_DSTBN#1 — M24 — DSTBN[1]#
(6) H_DSTBP#1 — N25 — DSTBP[1]#
(6) H_DINV#1 — M26 — DINV[1]#

DATA GRP 3
H_D#[63:0]
D[48]# AC22 H_D#48
D[49]# AC23 H_D#49
D[50]# AB22 H_D#50
D[51]# AA21 H_D#51
D[52]# AB21 H_D#52
D[53]# AC25 H_D#53
D[54]# AD20 H_D#54
D[55]# AE22 H_D#55
D[56]# AF23 H_D#56
D[57]# AD24 H_D#57
D[58]# AE21 H_D#58
D[59]# AD21 H_D#59
D[60]# AE25 H_D#60
D[61]# AF25 H_D#61
D[62]# AE22 H_D#62
D[63]# AF26 H_D#63
DSTBN[3]# AD23 — H_DSTBN#3 (6)
DSTBP[3]# AE24 — H_DSTBP#3 (6)
DINV[3]# AC20 — H_DINV#3 (6)

MISC
GTLREF AD26
TEST1 C26
TEST2 D25
BSEL[0] B22
BSEL[1] B23
BSEL[2] C21
COMP[0] R26 — R465
COMP[1] U26 — R464
COMP[2] U1 — R151
COMP[3] V1 — R150
DPRSTP# E5 — ICH_DPRSTP# (12,37)
DPSLP# B5 — H_DPSLP# (12)
DPWR# D24
PWRGOOD D6 — H_DPWR# (6)
SLP# D7 — H_PWRGD (12)
PSI# AE6 — H_CPUSLP# (6,12) — PSI# (37)

PZ47903-2741-01

+1.05V
R468 1K/F_4
H_GTLREF
R213 *1K_4
R212 51_4
20/15mils
R467 2K/F_4
(3,7) CPU_MCH_BSEL0
(3,7) CPU_MCH_BSEL1
(3,7) CPU_MCH_BSEL2
Use 1% R
Layout note: 0.5" max for GTLREF

LE4 A:
Modify circuit

Trcae width : ?
placement <0.5"
25/25mils
H_PWRGD is CMOS driving by ICH

TO VRD

LE4 A:
Modify circuit

XDP_TMS R147 54.9/F_4
XDP_TDI R149 54.9/F_4
XDP_BPM#5 R145 54.9/F_4
XDP_TCK R146 54.9/F_4
XDP_TRST# R148 54.9/F_4
+1.05V

XDP PU_R < 0.2"

Why BMP5 need PH ?

XDP_TCK PD 27.4/1% ?
XDP_TRST PD 510ohm /5% ?
XDP_TDI PU 150ohm /1.05V
XDP_TMS PU 39.2/1%?
XDP_TDO PU 54.9ohm?
For ITP700

XDP_DBRESET# R454 *54.9/F_4 R235 0/F_4 +1.05V — SYS_RST# (14)

LE4 B:
Add R235 in BOM

+1.05V
R455 *330_4
H_PROCHOT# — Q10 *MMBT3904 — PH_PROCHOT# (37)

LE4 B:
Change netname

+1.05V
+3V_S5
R223 *1K_4
R209 *10K_4
PM_THRMTRIP# — Q13 *MMBT3904 — THERM_CPUDIE_L# — R463 *0_4 — THERM_CPUDIE# (30)

LE4 B:
del R463 in BOM

+5VRUN
R456 100K_4
Q11 E@2N7002K
Q12 DTC144EUA
Q34 2N7002K
(30) FANLESS#
H_PROCHOT#
THERMATRIP_VGA# (19)

LE4 A:
Add new circuit with

PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	Yonah/Merom (Host)	1A
Date: Tuesday, March 14, 2006	Sheet 4 of 42	

+1.05V
C379 0.1U_4 C316 0.1U_4 C381 0.1U_4 C317 0.1U_4 C286 0.1U_4 C285 0.1U_4

VCC_CORE
CH6222M9A01
22UF/10V/X5R
C319 22U_8 C368 22U_8 C372 22U_8 C363 22U_8
C335 22U_8 C328 22U_8 C370 22U_8 C378 22U_8
C354 22U_8 C371 22U_8 C380 22U_8 C339 22U_8
C360 22U_8 C369 22U_8 C357 22U_8 C349 22U_8
C382 22U_8 C334 22U_8 C332 22U_8 C377 22U_8
C345 22U_8 C346 22U_8 C376 22U_8 C352 22U_8
C362 22U_8 C375 22U_8 C373 22U_8 C337 22U_8
C329 22U_8 C365 22U_8 C356 22U_8 C331 22U_8

U38C
VCC_CORE
VCC[001] A7, VCC[002] A9, VCC[003] A10, VCC[004] A12, VCC[005] A13, VCC[006] A15, VCC[007] A17, VCC[008] A18, VCC[009] A20, VCC[010] B7, VCC[011] B9, VCC[012] B10, VCC[013] B12, VCC[014] B14, VCC[015] B15, VCC[016] B17, VCC[017] B18, VCC[018] B20, VCC[019] C9, VCC[020] C10, VCC[021] C12, VCC[022] C13, VCC[023] C15, VCC[024] C17, VCC[025] C18, VCC[026] D9, VCC[027] D10, VCC[028] D12, VCC[029] D14, VCC[030] D15, VCC[031] D17, VCC[032] D18, VCC[033] E7, VCC[034] E9, VCC[035] E10, VCC[036] E12, VCC[037] E13, VCC[038] E15, VCC[039] E17, VCC[040] E18, VCC[041] E20, VCC[042] E7, VCC[043] F9, VCC[044] F10, VCC[045] F12, VCC[046] F14, VCC[047] F15, VCC[048] E17, VCC[049] F17, VCC[050] F18, VCC[051] E20, VCC[052] AA7, VCC[053] AA9, VCC[054] AA10, VCC[055] AA12, VCC[056] AA13, VCC[057] AA15, VCC[058] AA17, VCC[059] AA18, VCC[060] AA20, VCC[061] AB9, VCC[062] AC10, VCC[063] AB10, VCC[064] AB12, VCC[065] AB14, VCC[066] AB15, VCC[067] AB17, VSSSENSE AB18
VCC[068] AB20, VCC[069] AB7, VCC[070] AC7, VCC[071] AC9, VCC[072] AC12, VCC[073] AC13, VCC[074] AC15, VCC[075] AC17, VCC[076] AC18, VCC[077] AD7, VCC[078] AD9, VCC[079] AD10, VCC[080] AD12, VCC[081] AD14, VCC[082] AD15, VCC[083] AD17, VCC[084] AD18, VCC[085] AE9, VCC[086] AE10, VCC[087] AE12, VCC[088] AE13, VCC[089] AE15, VCC[090] AE17, VCC[091] AE18, VCC[092] AE20, VCC[093] AF9, VCC[094] AE10, VCC[095] AE12, VCC[096] AE14, VCC[097] AE15, VCC[098] AE17, VCC[099] AF18, VCC[100] AF20
VCCP[01] V6, VCCP[02] G21, VCCP[03] J6, VCCP[04] K6, VCCP[05] M6, VCCP[06] J21, VCCP[07] K21, VCCP[08] M21, VCCP[09] N21, VCCP[10] N6, VCCP[11] R21, VCCP[12] R6, VCCP[13] T21, VCCP[14] T6, VCCP[15] V21, VCCP[16] W21
VCCA B26
VID[0] AD6, VID[1] AE5, VID[2] AE5, VID[3] AF4, VID[4] AE3, VID[5] AE2, VID[6]
VCCSENSE AE7, VSSSENSE AE7
PZ47903-2741-01

H_VID0 (37), H_VID1 (37), H_VID2 (37), H_VID3 (37), H_VID4 (37), H_VID5 (37), H_VID6 (37)

+1.05V
VCC_CORE
+1.5V
+1.05V (4,6,7,9,10,12,15,38,40)
VCC_CORE (37,40)
+1.5V (7,9,10,13,15,27,38,40)

+1.05V
C289
330U/2.5V/ESR=9/POS
ESR :12m ohm

+1.5V
C401 0.01U_4
C402 10U/10V_8

VCC_CORE
R167 100_4
R162 100_4
VCCSENSE (37)
VSSSENSE (37)
Connect to PWM , special layout
Use 1% R

U38D
VSS[001] A4, VSS[002] A8, VSS[003] A11, VSS[004] A14, VSS[005] A16, VSS[006] A19, VSS[007] A23, VSS[008] A26, VSS[009] B6, VSS[010] B8, VSS[011] B11, VSS[012] B13, VSS[013] B16, VSS[014] B19, VSS[015] B21, VSS[016] B24, VSS[017] C5, VSS[018] C8, VSS[019] C11, VSS[020] C14, VSS[021] C16, VSS[022] C19, VSS[023] C2, VSS[024] C22, VSS[025] C25, VSS[026] D1, VSS[027] D4, VSS[028] D8, VSS[029] D11, VSS[030] D13, VSS[031] D16, VSS[032] D19, VSS[033] D23, VSS[034] D26, VSS[035] E3, VSS[036] E6, VSS[037] E8, VSS[038] E11, VSS[039] E14, VSS[040] E16, VSS[041] E19, VSS[042] E21, VSS[043] E24, VSS[044] F5, VSS[045] F8, VSS[046] F11, VSS[047] F13, VSS[048] F16, VSS[049] F19, VSS[050] F2, VSS[051] F22, VSS[052] F25, VSS[053] G4, VSS[054] G1, VSS[055] G23, VSS[056] G26, VSS[057] H3, VSS[058] H6, VSS[059] H21, VSS[060] H24, VSS[061] J2, VSS[062] J5, VSS[063] J22, VSS[064] J25, VSS[065] K1, VSS[066] K4, VSS[067] K23, VSS[068] K26, VSS[069] L3, VSS[070] L6, VSS[071] L21, VSS[072] L24, VSS[073] M2, VSS[074] M5, VSS[075] M22, VSS[076] M25, VSS[077] N1, VSS[078] N4, VSS[079] N23, VSS[080] N26, VSS[081] P3
VSS[082] P6, VSS[083] P21, VSS[084] P24, VSS[085] R2, VSS[086] R5, VSS[087] R22, VSS[088] R25, VSS[089] T1, VSS[090] T4, VSS[091] T23, VSS[092] T26, VSS[093] U3, VSS[094] U6, VSS[095] U21, VSS[096] U24, VSS[097] V2, VSS[098] V5, VSS[099] V22, VSS[100] V25, VSS[101] W1, VSS[102] W4, VSS[103] W23, VSS[104] W26, VSS[105] Y3, VSS[106] Y6, VSS[107] Y21, VSS[108] Y24, VSS[109] AA2, VSS[110] AA5, VSS[111] AA8, VSS[112] AA11, VSS[113] AA14, VSS[114] AA16, VSS[115] AA19, VSS[116] AA22, VSS[117] AA25, VSS[118] AB1, VSS[119] AB4, VSS[120] AB8, VSS[121] AB11, VSS[122] AB13, VSS[123] AB16, VSS[124] AB19, VSS[125] AB23, VSS[126] AB26, VSS[127] AC3, VSS[128] AC6, VSS[129] AC8, VSS[130] AC11, VSS[131] AC14, VSS[132] AC16, VSS[133] AC19, VSS[134] AC21, VSS[135] AC24, VSS[136] AD2, VSS[137] AD5, VSS[138] AD8, VSS[139] AD11, VSS[140] AD13, VSS[141] AD16, VSS[142] AD19, VSS[143] AD22, VSS[144] AD25, VSS[145] AE1, VSS[146] AE4, VSS[147] AE8, VSS[148] AE11, VSS[149] AE14, VSS[150] AE16, VSS[151] AE19, VSS[152] AE23, VSS[153] AE26, VSS[154] AE3, VSS[155] AE6, VSS[156] AE8, VSS[157] AE11, VSS[158] AE13, VSS[159] AE16, VSS[160] AE19, VSS[161] AE21, VSS[162] AE24
PZ47903-2741-01

LE4 C:

+3VRUN
Q16 2N7002K
(30,35) MBDATA — LM86_SMD — LM86_SMD (19)
+3VRUN
Q15 2N7002K
(30,35) MBCLK — LM86_SMC — LM86_SMC (19)

change to 0805

CRB use 8.2k PH

+3VRUN
R220 200_4
25mils
R211 10K_4
LM86VCC
C406 0.1U_4 10/20mils
R232 10K_4
R231 10K_4

LE4 B:

Solve can't power on isuue
So change R220 pull high and
R211 pull high to thermal
circuit.(12/12/2005)

U19
LM86_SMC — SCLK (8) — VCC (1)
LM86_SMD — SDA (7) — DXP (2) — H_THERMDA — C400 2200P/50V_4 — H_THERMDA (4)
(14) THERM_ALERT# — THERM_ALERT# — ALERT# (6) — DXN (3) — H_THERMDC — H_THERMDC (4)
OVERT# (4) — GND (5)
MAX6657/GMT-781
ADDRESS: 98H

LE4 C:

add hardware protect

+3VRUN
R214 *10K_4
R208 *0_6 — 1999_SHDN# (39)

LE4 C:

Del R208

+3VRUN
R224 *1M/F_4
C408 *0.1U_4
SYS_SHDN#
Q14 *2N7002K
Q17 *2N7002K

LE4 A:

Add new circuit
with H/W solution

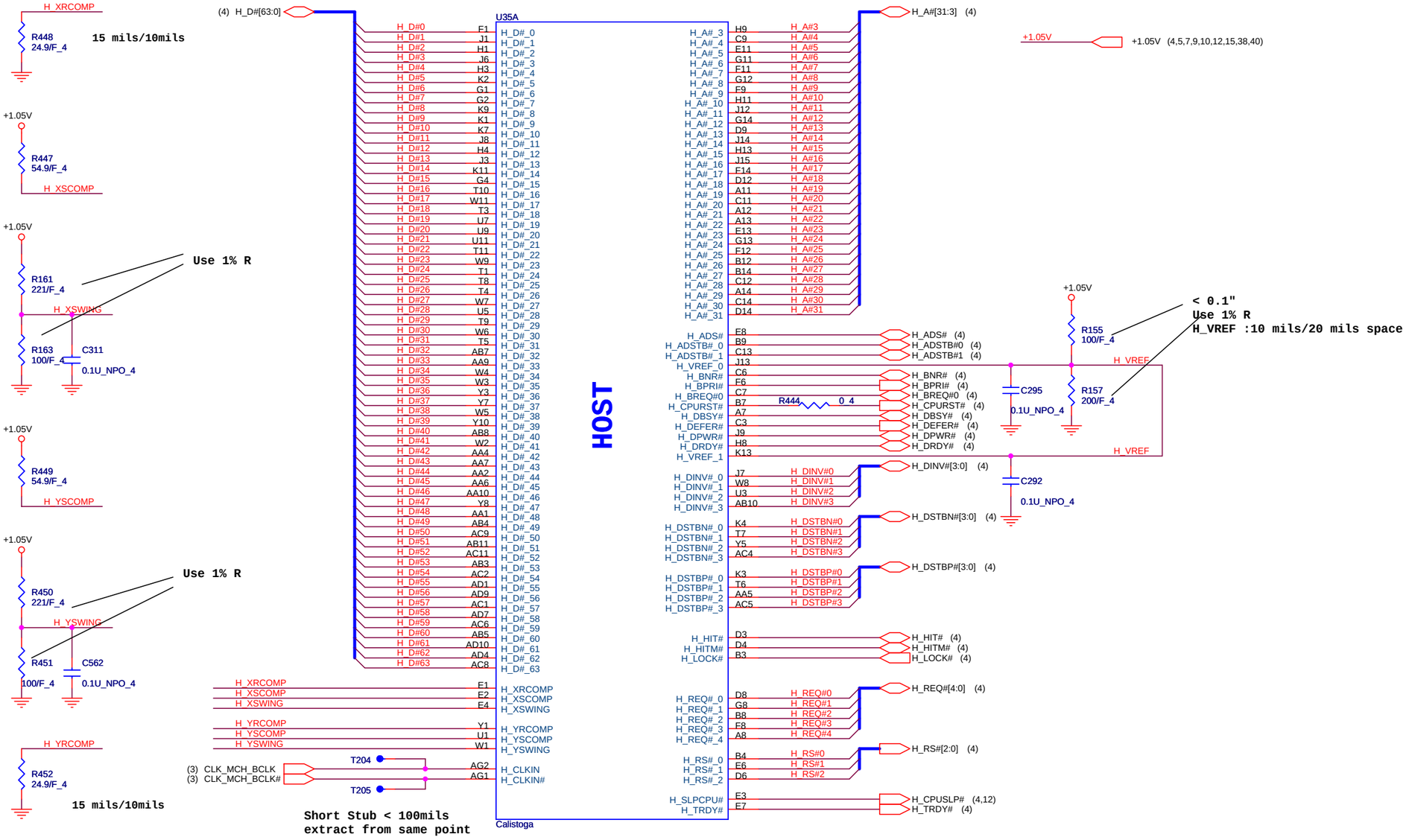
LE4 B:

Del R224, C408, Q14
and Q17 in BOM

Unstall R267 , Q28 , Q26 for Intel sighting -> CPU thermal die bug /0506

PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	Yonah/Merom (Power/NC)	1A
Date: Tuesday, March 14, 2006	Sheet 5 of 42	



PROJECT : LE4

Quanta Computer Inc.

Size	Document Number	Rev
	Calistoga_A (Host)	1A
Date: Tuesday, March 14, 2006	Sheet 6 of 42	

Check

U35B

RSVD
T21 MCH_RSVD_1 H32
T25 MCH_RSVD_2 T32
T24 MCH_RSVD_3 R32
T72 MCH_RSVD_4 F3
T68 MCH_RSVD_5 F7
T63 MCH_RSVD_6 AG11
T60 MCH_RSVD_7 AF11
T66 MCH_RSVD_8 H7
T42 TV_DCONSEL0 J19
T23 TV_DCONSEL1 K30
T31 MCH_RSVD_11 J29
T173 MCH_RSVD_12 A41
T183 MCH_RSVD_13 A35
T184 MCH_RSVD_14 A34
T36 MCH_RSVD_15 D28
T185 D27
RSVD_0 RSVD_1 RSVD_2 RSVD_3 RSVD_4 RSVD_5 RSVD_6 RSVD_7 RSVD_8 RSVD_9 RSVD_10 RSVD_11 RSVD_12 RSVD_13 RSVD_14 RSVD_15

CFG
(3,4) CPU_MCH_BSEL0 MCH_BSEL0 K16
(3,4) CPU_MCH_BSEL1 MCH_BSEL1 K18
(3,4) CPU_MCH_BSEL2 MCH_BSEL2 J18
MCH_CFG_3 F18
T43 MCH_CFG_4 E15
T62 MCH_CFG_5 F15
T50 MCH_CFG_6 E18
MCH_CFG_7 D19
MCH_CFG_8 D16
T46 MCH_CFG_9 G16
MCH_CFG_10 E16
MCH_CFG_11 D15
MCH_CFG_12 G15
(9) MCH_CFG_13 MCH_CFG_13 K15
T192 MCH_CFG_14 C15
T54 MCH_CFG_15 H16
MCH_CFG_16 G18
T194 MCH_CFG_17 H15
MCH_CFG_18 J25
MCH_CFG_19 K27
MCH_CFG_20 J26
CFG_0 CFG_1 CFG_2 CFG_3 CFG_4 CFG_5 CFG_6 CFG_7 CFG_8 CFG_9 CFG_10 CFG_11 CFG_12 CFG_13 CFG_14 CFG_15 CFG_16 CFG_17 CFG_18 CFG_19 CFG_20

PM
(14) PM_BMBUSY# G28
(16,17) PM_EXTTS#0 F25
(14,17) PM_EXTTS#1 H26
(4,12) PM_THRMTRIP# G6
(14,37) DELAY_VR_PWRGOOD AH33
AH34
PM_BMBUSY# PM_EXTTS#_0 PM_EXTTS#_1 PM_THRMTRIP# PWROK RSTIN#
(13) PLT_RST-R# R82 100/F_4 RST IN# MCH

MISC
T32 H28
T33 H27
+3VRUN K28
(13) MCH_ICH_SYNC R114 *10K/F_4
SDVO_CTRLCLK SDVO_CTRLDATA LT_RESET#

NC
T203 TP_MCH_NC0 D1
T178 TP_MCH_NC1 C41
T202 TP_MCH_NC2 C1
T179 TP_MCH_NC3 BA41
T181 TP_MCH_NC4 BA40
T182 TP_MCH_NC5 BA39
T71 TP_MCH_NC6 BA3
T73 TP_MCH_NC7 BA2
T201 TP_MCH_NC8 BA1
T177 TP_MCH_NC9 B41
T197 TP_MCH_NC10 B2
T176 TP_MCH_NC11 AY41
T200 TP_MCH_NC12 AY1
T175 TP_MCH_NC13 AW41
T199 TP_MCH_NC14 AW1
T174 TP_MCH_NC15 A40
T196 TP_MCH_NC16 A4
T180 TP_MCH_NC17 A39
T198 TP_MCH_NC18 A3
NC0 NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8 NC9 NC10 NC11 NC12 NC13 NC14 NC15 NC16 NC17 NC18

Calistoga

DDR MUXING
SM_CK_0 AY35 M_CLK_DDR0 (16)
SM_CK_1 AR1 M_CLK_DDR1 (16)
SM_CK_2 AW7 M_CLK_DDR2 (16)
SM_CK_3 AW40 M_CLK_DDR3 (16)
SM_CK#_0 AW35 M_CLK_DDR#0 (16)
SM_CK#_1 AT1 M_CLK_DDR#1 (16)
SM_CK#_2 AY7 M_CLK_DDR#2 (16)
SM_CK#_3 AY40 M_CLK_DDR#3 (16)
SM_CKE_0 AU20 M_CKE0 (16,17)
SM_CKE_1 AT20 M_CKE1 (16,17)
SM_CKE_2 BA29 M_CKE2 (16,17)
SM_CKE_3 AY29 M_CKE3 (16,17)
SM_CS#_0 AW13 M_CS#0 (16,17)
SM_CS#_1 AW12 M_CS#1 (16,17)
SM_CS#_2 AY21 M_CS#2 (16,17)
SM_CS#_3 AW21 M_CS#3 (16,17)
SM_OCDCOMP_0 AL20 M_OCDCOMP_0
SM_OCDCOMP_1 AF10 M_OCDCOMP_1
SM_ODT_0 BA13 M_ODT0 (16,17)
SM_ODT_1 BA12 M_ODT1 (16,17)
SM_ODT_2 AY20 M_ODT2 (16,17)
SM_ODT_3 AU21 M_ODT3 (16,17)
SM_RCOMP# AV9 M_RCOMP#
SM_RCOMP AT9 M_RCOMP
SM_VREF_0 AK1 SMDDR_VREF_MCH
SM_VREF_1 AK41

15mils/15mils
R156 *40.2/F_4
R120 *40.2/F_4
Layout as short as passable
NC from WW45

CLK
G_CLKIN# AF33
G_CLKIN AG33
D_REFCLKIN# A27 R_DOT96# R97 I@0_4 DOT96#
D_REFCLKIN A26 R_DOT96 R101 I@0_4 DOT96
D_REFSSCLKIN# C40 RDREFSSCLK# R96 I@0_4 DREFSSCLK#
D_REFSSCLKIN D41 RDREFSSCLK R94 I@0_4 DREFSSCLK
D_REFSSCLKIN
CLK_PCIE_3GPLL# (3)
CLK_PCIE_3GPLL (3)
DOT96# (3)
DOT96 (3)
DREFSSCLK# (3)
DREFSSCLK (3)

DMI
DMI_RXN_0 AE35 DMI_TXN0
DMI_RXN_1 AE39 DMI_TXN1
DMI_RXN_2 AG35 DMI_TXN2
DMI_RXN_3 AH39 DMI_TXN3
DMI_TXN[3:0] (13)
DMI_RXP_0 AC35 DMI_TXP0
DMI_RXP_1 AE39 DMI_TXP1
DMI_RXP_2 AE35 DMI_TXP2
DMI_RXP_3 AG39 DMI_TXP3
DMI_TXP[3:0] (13)
DMI_TXN_0 AE37 DMI_RXN0
DMI_TXN_1 AF41 DMI_RXN1
DMI_TXN_2 AG37 DMI_RXN2
DMI_TXN_3 AH41 DMI_RXN3
DMI_RXN[3:0] (13)
DMI_TXP_0 AC37 DMI_RXP0
DMI_TXP_1 AE41 DMI_RXP1
DMI_TXP_2 AE37 DMI_RXP2
DMI_TXP_3 AG41 DMI_RXP3
DMI_RXP[3:0] (13)

SMDDR_VREF_MCH
R568 *0_4 V_DDR_MCH_REF
R173 0_4 SMDDR_VREF
0402
R172 10K/F_6 1.8VSUS
R171 10K/F_6
(19,22,30) LCD_BLON_EC
0402
Change R172 AND R171 SIZE from 0402 to 0603
(22) LCD_BKLTCTL R391 I@0_4 D32
R89 I@0_4 J30
L_CLKCTLA H30
T38 L_CLKCTLB H29
T34 (22) EDIDCLK R119 I@0_4 G26
(22) EDIDDATA R115 I@0_4 G25
L_IBG B38
T22 L_VBG C35
(22) DISP_ON R81 I@0_4 VDDEN F32
R569 I@0_4 C33
C32

LE4 B: Use 1% R add R569

LE4 A: As below
Reserved for AV
R590 I@0_6 CRT_RGB#
R406 I@0_4 CRT_BLUE
R411 I@0_4 CRT_GREEN
R415 I@0_4 CRT_RED
R416 I@150/F_4
R412 I@150/F_4
R407 I@150/F_4
R105 I@0_4 CRT_DDC_CLK
R98 I@0_4 CRT_DDC_DAT
(23) DDCCLK
(23) DDCDAT
I@39/F_4
R116 HSYNC1
R126 I@255/F_4 CRTIREF
R112 I@39/F_4 VSYNC1
(23) HSYNC_COM
(23) VSYNC_COM
< 0.1" . 15mils/15mils space
use 1% R

LE4 A:
R428 I@0_4 TV_COMP1
R423 I@0_4 TV_Y/G1
R419 I@0_4 TV_C/R1
(23) TV_COMP
(23) TV_Y/G
(23) TV_C/R
R591 I@0_6 TV_IRTN
R421 I@150/F_4
R425 I@150/F_4
R430 I@150/F_4
R124 I@4.99K/F_4 TVIREF J20
< 0.1" . 15mils/15mils space

U35C

LVDS
L_BKLTCTL
L_BKLTEN
L_CLKCTLA
L_CLKCTLB
L_DDC_CLK
L_DDC_DATA
L_IBG
L_VBG
L_VDDEN
L_VREFH
L_VREFL
LA_CLK# A33
LA_CLK A32
LA_CLK#
LA_CLK
T37 LB_CLK# E27
T39 LB_CLK E26
LA_DATAN0 C37
LA_DATAN1 B35
LA_DATAN2 A37
LA_DATA#_0
LA_DATA#_1
LA_DATA#_2
LA_DATAP0 B37
LA_DATAP1 B34
LA_DATAP2 A36
LA_DATA_0
LA_DATA_1
LA_DATA_2
T30 G30
T28 LB_DATA#_0 D30
T26 LB_DATA#_1 F29
LB_DATA#_2
T29 F30
T27 LB_DATA_0 D29
T35 LB_DATA_1 F28
LB_DATA_2

TV
TV_DACA_OUT A16
TV_DACB_OUT C18
TV_DACC_OUT A19
TV_IREF
TV_IRTNA B16
TV_IRTNB B18
TV_IRTNC B19

VGA
CRT_BLUE
CRT_BLUE#
CRT_GREEN
CRT_GREEN#
CRT_RED
CRT_RED#
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_IREF
CRT_VSYNC

Calistoga

L_CLKCTLA R108 I@10K/F_4
L_CLKCTLB R102 I@10K/F_4
+3VRUN
20mils/20mils space
+V1.5_PCIE

PCI-EXPRESS GRAPHICS
EXP_A_COMPI D40 EXP_A_COMPX R67 24.9/F_4
EXP_A_COMPO D38
EXP_A_RXN_0 F34 PCIE_MRX_GTX_N0
EXP_A_RXN_1 G38 PCIE_MRX_GTX_N1
EXP_A_RXN_2 H34 PCIE_MRX_GTX_N2
EXP_A_RXN_3 J38 PCIE_MRX_GTX_N3
EXP_A_RXN_4 L34 PCIE_MRX_GTX_N4
EXP_A_RXN_5 M38 PCIE_MRX_GTX_N5
EXP_A_RXN_6 N34 PCIE_MRX_GTX_N6
EXP_A_RXN_7 P38 PCIE_MRX_GTX_N7
EXP_A_RXN_8 R34 PCIE_MRX_GTX_N8
EXP_A_RXN_9 T38 PCIE_MRX_GTX_N9
EXP_A_RXN_10 V34 PCIE_MRX_GTX_N10
EXP_A_RXN_11 W38 PCIE_MRX_GTX_N11
EXP_A_RXN_12 Y34 PCIE_MRX_GTX_N12
EXP_A_RXN_13 AA38 PCIE_MRX_GTX_N13
EXP_A_RXN_14 AB34 PCIE_MRX_GTX_N14
EXP_A_RXN_15 AC38 PCIE_MRX_GTX_N15
PCIE_MRX_GTX_N[0..15] (18)
EXP_A_RXP_0 D34 PCIE_MRX_GTX_P0
EXP_A_RXP_1 F38 PCIE_MRX_GTX_P1
EXP_A_RXP_2 G34 PCIE_MRX_GTX_P2
EXP_A_RXP_3 H38 PCIE_MRX_GTX_P3
EXP_A_RXP_4 J34 PCIE_MRX_GTX_P4
EXP_A_RXP_5 L38 PCIE_MRX_GTX_P5
EXP_A_RXP_6 M34 PCIE_MRX_GTX_P6
EXP_A_RXP_7 N38 PCIE_MRX_GTX_P7
EXP_A_RXP_8 P34 PCIE_MRX_GTX_P8
EXP_A_RXP_9 R38 PCIE_MRX_GTX_P9
EXP_A_RXP_10 T34 PCIE_MRX_GTX_P10
EXP_A_RXP_11 V38 PCIE_MRX_GTX_P11
EXP_A_RXP_12 W34 PCIE_MRX_GTX_P12
EXP_A_RXP_13 Y38 PCIE_MRX_GTX_P13
EXP_A_RXP_14 AA34 PCIE_MRX_GTX_P14
EXP_A_RXP_15 AB38 PCIE_MRX_GTX_P15
PCIE_MRX_GTX_P[0..15] (18)
EXP_A_TXN_0 F36 PCIE_MTX_GRX_C_N0
EXP_A_TXN_1 G40 PCIE_MTX_GRX_C_N1
EXP_A_TXN_2 H36 PCIE_MTX_GRX_C_N2
EXP_A_TXN_3 J40 PCIE_MTX_GRX_C_N3
EXP_A_TXN_4 L36 PCIE_MTX_GRX_C_N4
EXP_A_TXN_5 M40 PCIE_MTX_GRX_C_N5
EXP_A_TXN_6 N36 PCIE_MTX_GRX_C_N6
EXP_A_TXN_7 P40 PCIE_MTX_GRX_C_N7
EXP_A_TXN_8 R36 PCIE_MTX_GRX_C_N8
EXP_A_TXN_9 T40 PCIE_MTX_GRX_C_N9
EXP_A_TXN_10 V36 PCIE_MTX_GRX_C_N10
EXP_A_TXN_11 W40 PCIE_MTX_GRX_C_N11
EXP_A_TXN_12 Y36 PCIE_MTX_GRX_C_N12
EXP_A_TXN_13 AA40 PCIE_MTX_GRX_C_N13
EXP_A_TXN_14 AB36 PCIE_MTX_GRX_C_N14
EXP_A_TXN_15 AC40 PCIE_MTX_GRX_C_N15
EXP_A_TXP_0 D36 PCIE_MTX_GRX_C_P0
EXP_A_TXP_1 F40 PCIE_MTX_GRX_C_P1
EXP_A_TXP_2 G36 PCIE_MTX_GRX_C_P2
EXP_A_TXP_3 H40 PCIE_MTX_GRX_C_P3
EXP_A_TXP_4 J36 PCIE_MTX_GRX_C_P4
EXP_A_TXP_5 L40 PCIE_MTX_GRX_C_P5
EXP_A_TXP_6 M36 PCIE_MTX_GRX_C_P6
EXP_A_TXP_7 N40 PCIE_MTX_GRX_C_P7
EXP_A_TXP_8 P36 PCIE_MTX_GRX_C_P8
EXP_A_TXP_9 R40 PCIE_MTX_GRX_C_P9
EXP_A_TXP_10 T36 PCIE_MTX_GRX_C_P10
EXP_A_TXP_11 V40 PCIE_MTX_GRX_C_P11
EXP_A_TXP_12 W36 PCIE_MTX_GRX_C_P12
EXP_A_TXP_13 Y40 PCIE_MTX_GRX_C_P13
EXP_A_TXP_14 AA36 PCIE_MTX_GRX_C_P14
EXP_A_TXP_15 AB40 PCIE_MTX_GRX_C_P15

+1.5V
TV_COMP1 R576 E@0_4
TV_Y/G1 R577 E@0_4
TV_C/R1 R578 E@0_4
TVIREF R579 E@0_4
TV_IRTN R580 E@0_4
TV_IRTN R581 E@0_4
+1.05V
CRT_BLUE R582 E@0_4
CRT_GREEN R583 E@0_4
CRT_RED R584 E@0_4
CRT_RGB# R585 E@0_4
CRT_RGB# R586 E@0_4
CRTIREF R587 E@0_4
HSYNC1 R588 E@0_4
VSYNC1 R589 E@0_4

LE4 B:
945PM contact power and GND plane
945GM/940GML Contact GND plane

1.8VSUS
R160 80.6/F_4
M_RCOMP#
15mils/10mils
M_RCOMP
R159 80.6/F_4
+3VRUN
R106 10K/F_4 PM_EXTTS#0
R113 *10K/F_4 PM_EXTTS#1
MCH_CFG_9 R125 *10K/F_4 +3VRUN
+V1.5_PCIE
+3VRUN
SMDDR_VREF
1.8VSUS
+V1.5_PCIE (10)
+3VRUN (3,5,9,10,12,13,14,15,16,17,18,19,20,22,23,26,27,28,30,31,32,33,36,40,41)
SMDDR_VREF (16)
1.8VSUS (9,16,36,40,41)
(9) MCH_CFG_[12:5] MCH_CFG_[12:5]
(9) MCH_CFG_[20:16] MCH_CFG_[20:16]

L_IBG R74 I@1.5K_4
L_VDDEN R86 I@100K_4
RP32 I@4P2R-S-0 (19,22) LCD_ACLK- (19,22) LCD_ACLK+ LA_CLK# LA_CLK
RP29 I@4P2R-S-0 (19,22) LCD_A0- (19,22) LCD_A0+ LA_DATAN0 LA_DATAP0
RP31 I@4P2R-S-0 (19,22) LCD_A1- (19,22) LCD_A1+ LA_DATAN1 LA_DATAP1
RP30 I@4P2R-S-0 (19,22) LCD_A2- (19,22) LCD_A2+ LA_DATAN2 LA_DATAP2

C187 E@0.1U_P_4 PCIE_MTX_GRX_C_N0 PCIE_MTX_GRX_N0
C525 E@0.1U_P_4 PCIE_MTX_GRX_C_N1 PCIE_MTX_GRX_N1
C189 E@0.1U_P_4 PCIE_MTX_GRX_C_N2 PCIE_MTX_GRX_N2
C527 E@0.1U_P_4 PCIE_MTX_GRX_C_N3 PCIE_MTX_GRX_N3
C191 E@0.1U_P_4 PCIE_MTX_GRX_C_N4 PCIE_MTX_GRX_N4
C529 E@0.1U_P_4 PCIE_MTX_GRX_C_N5 PCIE_MTX_GRX_N5
C193 E@0.1U_P_4 PCIE_MTX_GRX_C_N6 PCIE_MTX_GRX_N6
C531 E@0.1U_P_4 PCIE_MTX_GRX_C_N7 PCIE_MTX_GRX_N7
C195 E@0.1U_P_4 PCIE_MTX_GRX_C_N8 PCIE_MTX_GRX_N8
C533 E@0.1U_P_4 PCIE_MTX_GRX_C_N9 PCIE_MTX_GRX_N9
C197 E@0.1U_P_4 PCIE_MTX_GRX_C_N10 PCIE_MTX_GRX_N10
C519 E@0.1U_P_4 PCIE_MTX_GRX_C_N11 PCIE_MTX_GRX_N11
C199 E@0.1U_P_4 PCIE_MTX_GRX_C_N12 PCIE_MTX_GRX_N12
C521 E@0.1U_P_4 PCIE_MTX_GRX_C_N13 PCIE_MTX_GRX_N13
C201 E@0.1U_P_4 PCIE_MTX_GRX_C_N14 PCIE_MTX_GRX_N14
C523 E@0.1U_P_4 PCIE_MTX_GRX_C_N15 PCIE_MTX_GRX_N15
PCIE_MTX_GRX_N[0..15] (18)

C186 E@0.1U_P_4 PCIE_MTX_GRX_C_P0 PCIE_MTX_GRX_P0
C524 E@0.1U_P_4 PCIE_MTX_GRX_C_P1 PCIE_MTX_GRX_P1
C188 E@0.1U_P_4 PCIE_MTX_GRX_C_P2 PCIE_MTX_GRX_P2
C526 E@0.1U_P_4 PCIE_MTX_GRX_C_P3 PCIE_MTX_GRX_P3
C190 E@0.1U_P_4 PCIE_MTX_GRX_C_P4 PCIE_MTX_GRX_P4
C528 E@0.1U_P_4 PCIE_MTX_GRX_C_P5 PCIE_MTX_GRX_P5
C192 E@0.1U_P_4 PCIE_MTX_GRX_C_P6 PCIE_MTX_GRX_P6
C530 E@0.1U_P_4 PCIE_MTX_GRX_C_P7 PCIE_MTX_GRX_P7
C194 E@0.1U_P_4 PCIE_MTX_GRX_C_P8 PCIE_MTX_GRX_P8
C532 E@0.1U_P_4 PCIE_MTX_GRX_C_P9 PCIE_MTX_GRX_P9
C196 E@0.1U_P_4 PCIE_MTX_GRX_C_P10 PCIE_MTX_GRX_P10
C518 E@0.1U_P_4 PCIE_MTX_GRX_C_P11 PCIE_MTX_GRX_P11
C198 E@0.1U_P_4 PCIE_MTX_GRX_C_P12 PCIE_MTX_GRX_P12
C520 E@0.1U_P_4 PCIE_MTX_GRX_C_P13 PCIE_MTX_GRX_P13
C200 E@0.1U_P_4 PCIE_MTX_GRX_C_P14 PCIE_MTX_GRX_P14
C522 E@0.1U_P_4 PCIE_MTX_GRX_C_P15 PCIE_MTX_GRX_P15
PCIE_MTX_GRX_P[0..15] (18)

DC Blocked Cap.
Near to North Bridge

+1.5V
R_DOT96# R95 E@0_4
R_DOT96 R107 E@0_4
RDREFSSCLK# R100 E@0_4
RDREFSSCLK R90 E@0_4
SMDDR_VREF_MCH
C333 0.1U_4
C536 0.1U_4

LE4 A:
940GML/945GM with clock signal
945PM with power and GND plan
LE4 B:
Change Netname

PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	Calistoga_B (VGA,DMI)	1A
Date: Tuesday, March 14, 2006	Sheet 7 of 42	

DDR SYSTEM MEMORY A

(16) M_A_DQ[63:0]

U35D

M_A_DQ0	AJ35	SA_DQ0	
M_A_DQ1	AJ34	SA_DQ1	
M_A_DQ2	AM31	SA_DQ2	
M_A_DQ3	AM33	SA_DQ3	
M_A_DQ4	AJ36	SA_DQ4	
M_A_DQ5	AK35	SA_DQ5	
M_A_DQ6	AJ32	SA_DQ6	
M_A_DQ7	AH31	SA_DQ7	
M_A_DQ8	AN35	SA_DQ8	
M_A_DQ9	AP33	SA_DQ9	
M_A_DQ10	AR31	SA_DQ10	
M_A_DQ11	AP31	SA_DQ11	
M_A_DQ12	AN38	SA_DQ12	
M_A_DQ13	AM36	SA_DQ13	
M_A_DQ14	AM34	SA_DQ14	
M_A_DQ15	AN33	SA_DQ15	
M_A_DQ16	AK26	SA_DQ16	
M_A_DQ17	AL27	SA_DQ17	
M_A_DQ18	AM26	SA_DQ18	
M_A_DQ19	AN24	SA_DQ19	
M_A_DQ20	AK28	SA_DQ20	
M_A_DQ21	AL28	SA_DQ21	
M_A_DQ22	AM24	SA_DQ22	
M_A_DQ23	AP26	SA_DQ23	
M_A_DQ24	AP23	SA_DQ24	
M_A_DQ25	AL22	SA_DQ25	
M_A_DQ26	AP21	SA_DQ26	
M_A_DQ27	AN20	SA_DQ27	
M_A_DQ28	AL23	SA_DQ28	
M_A_DQ29	AP24	SA_DQ29	
M_A_DQ30	AP20	SA_DQ30	
M_A_DQ31	AT21	SA_DQ31	
M_A_DQ32	AR12	SA_DQ32	
M_A_DQ33	AR14	SA_DQ33	
M_A_DQ34	AP13	SA_DQ34	
M_A_DQ35	AP12	SA_DQ35	
M_A_DQ36	AT13	SA_DQ36	
M_A_DQ37	AT12	SA_DQ37	
M_A_DQ38	AL14	SA_DQ38	
M_A_DQ39	AL12	SA_DQ39	
M_A_DQ40	AK9	SA_DQ40	
M_A_DQ41	AN7	SA_DQ41	
M_A_DQ42	AK8	SA_DQ42	
M_A_DQ43	AK7	SA_DQ43	
M_A_DQ44	AP9	SA_DQ44	
M_A_DQ45	AN9	SA_DQ45	
M_A_DQ46	AT5	SA_DQ46	
M_A_DQ47	AL5	SA_DQ47	
M_A_DQ48	AY2	SA_DQ48	
M_A_DQ49	AW2	SA_DQ49	
M_A_DQ50	AP1	SA_DQ50	
M_A_DQ51	AN2	SA_DQ51	
M_A_DQ52	AV2	SA_DQ52	
M_A_DQ53	AT3	SA_DQ53	
M_A_DQ54	AN1	SA_DQ54	
M_A_DQ55	AL2	SA_DQ55	
M_A_DQ56	AG7	SA_DQ56	
M_A_DQ57	AF9	SA_DQ57	
M_A_DQ58	AG4	SA_DQ58	
M_A_DQ59	AF6	SA_DQ59	
M_A_DQ60	AG9	SA_DQ60	
M_A_DQ61	AH6	SA_DQ61	
M_A_DQ62	AF4	SA_DQ62	
M_A_DQ63	AF8	SA_DQ63	

SA_BS_0	AU12	M_A_BS#0	M_A_BS#0 (16,17)
SA_BS_1	AV14	M_A_BS#1	M_A_BS#1 (16,17)
SA_BS_2	BA20	M_A_BS#2	M_A_BS#2 (16,17)
			M_A_CAS# (16,17)
SA_CAS#	AY13	M_A_CAS#	
SA_DM_0	AJ33	M_A_DM0	M_A_DM[7:0] (16)
SA_DM_1	AM35	M_A_DM1	
SA_DM_2	AL26	M_A_DM2	
SA_DM_3	AN22	M_A_DM3	
SA_DM_4	AM14	M_A_DM4	
SA_DM_5	AL9	M_A_DM5	
SA_DM_6	AR3	M_A_DM6	
SA_DM_7	AH4	M_A_DM7	
SA_DQS_0	AK33	M_A_DQS0	M_A_DQS[7:0] (16)
SA_DQS_1	AT33	M_A_DQS1	
SA_DQS_2	AN28	M_A_DQS2	
SA_DQS_3	AM22	M_A_DQS3	
SA_DQS_4	AN12	M_A_DQS4	
SA_DQS_5	AN8	M_A_DQS5	
SA_DQS_6	AP3	M_A_DQS6	
SA_DQS_7	AG5	M_A_DQS7	
SA_DQS#_0	AK32	M_A_DQS#0	M_A_DQS#[7:0] (16)
SA_DQS#_1	AU33	M_A_DQS#1	
SA_DQS#_2	AN27	M_A_DQS#2	
SA_DQS#_3	AM21	M_A_DQS#3	
SA_DQS#_4	AM12	M_A_DQS#4	
SA_DQS#_5	AL8	M_A_DQS#5	
SA_DQS#_6	AN3	M_A_DQS#6	
SA_DQS#_7	AH5	M_A_DQS#7	
SA_MA_0	AY16	M_A_A0	M_A_A[13:0] (16,17)
SA_MA_1	AU14	M_A_A1	
SA_MA_2	AW16	M_A_A2	
SA_MA_3	BA16	M_A_A3	
SA_MA_4	BA17	M_A_A4	
SA_MA_5	AU16	M_A_A5	
SA_MA_6	AV17	M_A_A6	
SA_MA_7	AU17	M_A_A7	
SA_MA_8	AW17	M_A_A8	
SA_MA_9	AT16	M_A_A9	
SA_MA_10	AU13	M_A_A10	
SA_MA_11	AT17	M_A_A11	
SA_MA_12	AV20	M_A_A12	
SA_MA_13	AV12	M_A_A13	
SA_RAS#	AW14	M_A_RAS#	M_A_RAS# (16,17)
SA_RCVENIN#	AK23	TP_MA_RCVENIN#	T41
SA_RCVENOUT#	AK24	TP_MA_RCVENOUT#	T40
SA_WE#	AY14	M_A_WE#	M_A_WE# (16,17)

Calistoga

DDR SYSTEM MEMORY B

(16) M_B_DQ[63:0]

U35E

M_B_DQ0	AK39	SB_DQ0	
M_B_DQ1	AJ37	SB_DQ1	
M_B_DQ2	AP39	SB_DQ2	
M_B_DQ3	AR41	SB_DQ3	
M_B_DQ4	AJ38	SB_DQ4	
M_B_DQ5	AK38	SB_DQ5	
M_B_DQ6	AN41	SB_DQ6	
M_B_DQ7	AP41	SB_DQ7	
M_B_DQ8	AT40	SB_DQ8	
M_B_DQ9	AV41	SB_DQ9	
M_B_DQ10	AU38	SB_DQ10	
M_B_DQ11	AV38	SB_DQ11	
M_B_DQ12	AP38	SB_DQ12	
M_B_DQ13	AR40	SB_DQ13	
M_B_DQ14	AW38	SB_DQ14	
M_B_DQ15	AY38	SB_DQ15	
M_B_DQ16	BA38	SB_DQ16	
M_B_DQ17	AV36	SB_DQ17	
M_B_DQ18	AR36	SB_DQ18	
M_B_DQ19	AP36	SB_DQ19	
M_B_DQ20	BA36	SB_DQ20	
M_B_DQ21	AU36	SB_DQ21	
M_B_DQ22	AP35	SB_DQ22	
M_B_DQ23	AP34	SB_DQ23	
M_B_DQ24	AY33	SB_DQ24	
M_B_DQ25	BA33	SB_DQ25	
M_B_DQ26	AT31	SB_DQ26	
M_B_DQ27	AU29	SB_DQ27	
M_B_DQ28	AU31	SB_DQ28	
M_B_DQ29	AW31	SB_DQ29	
M_B_DQ30	AV29	SB_DQ30	
M_B_DQ31	AW29	SB_DQ31	
M_B_DQ32	AM19	SB_DQ32	
M_B_DQ33	AL19	SB_DQ33	
M_B_DQ34	AP14	SB_DQ34	
M_B_DQ35	AN14	SB_DQ35	
M_B_DQ36	AN17	SB_DQ36	
M_B_DQ37	AM16	SB_DQ37	
M_B_DQ38	AP15	SB_DQ38	
M_B_DQ39	AL15	SB_DQ39	
M_B_DQ40	AJ11	SB_DQ40	
M_B_DQ41	AH10	SB_DQ41	
M_B_DQ42	AJ9	SB_DQ42	
M_B_DQ43	AN10	SB_DQ43	
M_B_DQ44	AK13	SB_DQ44	
M_B_DQ45	AH11	SB_DQ45	
M_B_DQ46	AK10	SB_DQ46	
M_B_DQ47	AJ8	SB_DQ47	
M_B_DQ48	BA10	SB_DQ48	
M_B_DQ49	AW10	SB_DQ49	
M_B_DQ50	BA4	SB_DQ50	
M_B_DQ51	AW4	SB_DQ51	
M_B_DQ52	AY10	SB_DQ52	
M_B_DQ53	AY9	SB_DQ53	
M_B_DQ54	AW5	SB_DQ54	
M_B_DQ55	AY5	SB_DQ55	
M_B_DQ56	AV4	SB_DQ56	
M_B_DQ57	AR5	SB_DQ57	
M_B_DQ58	AK4	SB_DQ58	
M_B_DQ59	AK3	SB_DQ59	
M_B_DQ60	AT4	SB_DQ60	
M_B_DQ61	AK5	SB_DQ61	
M_B_DQ62	AJ5	SB_DQ62	
M_B_DQ63	AJ3	SB_DQ63	

SB_BS_0	AT24	M_B_BS#0	M_B_BS#0 (16,17)
SB_BS_1	AV23	M_B_BS#1	M_B_BS#1 (16,17)
SB_BS_2	AY28	M_B_BS#2	M_B_BS#2 (16,17)
		M_B_CAS#	M_B_CAS# (16,17)
SB_CAS#	AR24		
SB_DM_0	AK36	M_B_DM0	M_B_DM[7:0] (16)
SB_DM_1	AR38	M_B_DM1	
SB_DM_2	AT36	M_B_DM2	
SB_DM_3	BA31	M_B_DM3	
SB_DM_4	AL17	M_B_DM4	
SB_DM_5	AH8	M_B_DM5	
SB_DM_6	BA5	M_B_DM6	
SB_DM_7	AN4	M_B_DM7	
SB_DQS_0	AM39	M_B_DQS0	M_B_DQS[7:0] (16)
SB_DQS_1	AT39	M_B_DQS1	
SB_DQS_2	AU35	M_B_DQS2	
SB_DQS_3	AR29	M_B_DQS3	
SB_DQS_4	AR16	M_B_DQS4	
SB_DQS_5	AR10	M_B_DQS5	
SB_DQS_6	AR7	M_B_DQS6	
SB_DQS_7	AN5	M_B_DQS7	
SB_DQS#_0	AM40	M_B_DQS#0	M_B_DQS#[7:0] (16)
SB_DQS#_1	AU39	M_B_DQS#1	
SB_DQS#_2	AT35	M_B_DQS#2	
SB_DQS#_3	AP29	M_B_DQS#3	
SB_DQS#_4	AP16	M_B_DQS#4	
SB_DQS#_5	AT10	M_B_DQS#5	
SB_DQS#_6	AT7	M_B_DQS#6	
SB_DQS#_7	AP5	M_B_DQS#7	
SB_MA_0	AY23	M_B_A0	M_B_A[13:0] (16,17)
SB_MA_1	AW24	M_B_A1	
SB_MA_2	AY24	M_B_A2	
SB_MA_3	AR28	M_B_A3	
SB_MA_4	AT27	M_B_A4	
SB_MA_5	AT28	M_B_A5	
SB_MA_6	AU27	M_B_A6	
SB_MA_7	AV28	M_B_A7	
SB_MA_8	AV27	M_B_A8	
SB_MA_9	AW27	M_B_A9	
SB_MA_10	AV24	M_B_A10	
SB_MA_11	BA27	M_B_A11	
SB_MA_12	AY27	M_B_A12	
SB_MA_13	AR23	M_B_A13	
SB_RAS#	AU23		M_B_RAS# (16,17)
SB_RCVENIN#	AK16	TP_MB_RCVENIN#	T52
SB_RCVENOUT#	AK18	TP_MB_RCVENOUT#	T45
SB_WE#	AR27	M_B_WE#	M_B_WE# (16,17)

Calistoga

PROJECT : LE4

Quanta Computer Inc.

Size	Document Number	Rev
	Calistoga_C (DDR)	1A
Date: Tuesday, March 14, 2006	Sheet 8 of 42	

U35G

+1.05V — C364 330U_2.5V_ESR12

VCC_0 … VCC_110 (AA33 … L16) — **VCC**

Calistoga

25mils

VCC_SM_0 … VCC_SM_107 (AU41 … AJ1)

VCC_SM1, VCC_SM2

C214 0.47U_6

C222 0.47U_6

VCC_SM106, VCC_SM107

C325 0.47U_6

C310 0.47U_6

25mils

C344 330U_2.5V_ESR12

+1.05V — C242 10U_8 — C273 10U_8 — C237 1U_4 — C272 0.1U_4 — C288 0.1U_4 — C294 0.1U_4

10U to 1U-Allen

1.8VSUS

120mils

PC6 330U_2.5V_ESR12 2.5

C274 10U_8 — C254 0.47U_6 — C282 0.1U_4 — C252 0.1U_4 — C302 0.1U_4

C253 0.47U_6

C255 0.47U_6

place C50 on BA23 Ball

place C49 on AJ23 Ball

LE4 B: del 1.5V_AUX power plane

(4,5,6,7,10,12,15,38,40) +1.05V → +1.05V

(7,16,36,40,41) 1.8VSUS → 1.8VSUS

Have to review again

ADD Matrix in silkscreen

place C51 on BA15 Ball

C269 0.47U_6

MCH_CFG_6 shall be PH !!
depopulate R2504 if use Calistoga

Depopulate R2504 for Calistoga-Allen

GMCH Strap pin

(7) MCH_CFG_5	R137	*2.2K_4	
(7) MCH_CFG_6	R136	*2.2K_4	
(7) MCH_CFG_7	R130	*2.2K_4	
(7) MCH_CFG_9	R129	*2.2K_4	
(7) MCH_CFG_10	R143	*2.2K_4	
(7) MCH_CFG_11	R141	2.2K_4	
(7) MCH_CFG_12	R144	*2.2K_4	
(7) MCH_CFG_13	R140	*2.2K_4	
(7) MCH_CFG_16	R142	*2.2K_4	+3VRUN
(7) MCH_CFG_18	R117	*1K/F_4	
(7) MCH_CFG_19	R110	*1K/F_4	+3VRUN
(7) MCH_CFG_20	R109	*1K/F_4	+3VRUN

intel WW51 recommand

25mils

U35F

NCTF

VCC_NCTF0 … VCC_NCTF72 (AD27 … T18)

VSS_NCTF0 … VSS_NCTF12 (AE27 … U17)

+1.5V

LE4 B: change +1.5V_AUX to +1.5V

100mils

VCCAUX_NCTF0 … VCCAUX_NCTF57 (AG27 … R15)

Calistoga

1.MCH_CFG_5 Low = DMI X2, High=DMIX4

2.MCH_CFG_6 DDR : Low =Moby Dick, High= Calistoga (Default)

3.MCH_CFG_7 CPU Strap Low=RSVD, High=Mobile CPU

4.MCH_CFG_9 PCI Exp Graphics Lane: Low =Reserved,High=Mobility

5.MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility

6.MCH_CFG_11: Low=Calistoga, High=Reserved

7.MCH_CFG_16 FSB Dynmic ODT: Low=Dynamic ODT Disabled,
High=Dynamic ODT Enabled.

8.MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V

9.MCH_CFG_19 DMI LANE Reversal:Low=Normal,High=LANES Reversed.

10.MCH_CFG_20 PCIE Backward interpoerability mode: Low= only SDVO or PCIE x1 is operational (defaults) ,High=SDVO and PCIE x1 are operation simultaneously via the PEG port.

PROJECT : LE4

Quanta Computer Inc.

Size	Document Number	Rev
	Calistoga_D (POWER)	1A
Date: Tuesday, March 14, 2006	Sheet 9 of 42	

+1.5V L53 10uH_8 +V1.5_DPLLA
C556 0.1U_4
+ C296 330U
L49 10uH_8 +V1.5_DPLLB
C537 0.1U_4
+ C184 330U
L27 FCM2012C-121_8 +V1.5_HPLL
C318 0.1U_4
C342 10U_8
L26 FCM2012C-121_8 +V1.5_MPLL
C309 0.1U_4
C341 10U_8

+V3.3_TVDAC L52 I@BLM18PG181SN1D_8 +V3.3_ATVBG
80mils
C267 10U_8 C555 0.1U_4 C293 0.022U_4
Oreginal FCM2012C-181 "CX000181008"
+V3.3_ATVBG C553 0.1U_4 C279 0.022U_4
+V3.3_ATVBG C554 0.1U_4 C287 0.022U_4
+1.5V L23 E@BLM18PG181SN1D-6_8 +V3.3_ATVBG

LE4 A:
Note:
940GML/945GM contact +V3.3_ATVBG
945PM contact +1.5V

+V1.5_PCIE L48 PCIE_L +1.5V
60mils
C513 10U_8 + C516 220U_6.3V BLM21PG220SN1D C515 10U_8
RC0805

LE4 C:
Solve black screen issue
to change L48 material
Del R389

+V1.5_3GPLL R93 0.5/F_6 3GPLL_FB_R L18 1uH_6 3GPLL_FB_L R103 0_8 +1.5V
60mils
RC0805
0.002ohm/1%

LE4 B: del R111,C246
change +1.5V_AUX to 1.5V

+2_5VRUN R396 I@0_8 R2_5VRUNA R401 E@0_8

LE4 A:
Note:
940GML/945GM contact Power plan
945PM contact GAN plan

+V2.5_CRTDAC +1.05V R118 I@0_8 R2.5VCRTDAC R127 E@0_8

LE4 A:
Note:
940GML/945GM contact +2.5_CRTDAC
945PM contact +1.05V

+V3.3_ATVBG +1.5V R131 I@0_8 V3.3_ATVBG R438 E@0_8

LE4 A:
Note:
940GML/945GM contact +V3.3_ATVBG
945PM contact +1.5V

+3VRUN +1.5V
C248 10U_8 C244 0.1U_4 C322 0.1U_4 C343 10U_8
+3.3S_TVDAC_LDO
30mils
+1.5V BAT54 D6 I@PDZ5.6B V1_5SFOLLOW 1 2
+V3.3_TVDAC R440 I@10_4
0.002 1% R154 I@0_8
RC0805

LE4 B:
Note:
940GML/945GM has circuit
945PM NA

+1.5V R397 I@0_8 VCCD_LVDS R398 E@0_8

LE4 A:
Note:
940GML/945GM contact Power plan
945PM contact GAN plan

+V1.5_TVDAC L20 V15_TVDAC_R R400 0_8 +1.5V
60mils
C257 0.022U_4 C250 0.1U_4
FCM2012C-121_8
RC0805
+V1.5_QTVDAC L22 FCM2012C-121_8
C259 0.022U_4 C251 0.1U_4
Oreginal FCM2012C-181 "CX000181008"
Oreginal FCM2012C-181 "CX000181008"

+2_5VRUN R392 I@0_8 R2_5VRUN
C205 0.1U_4 C240 10U_8

LE4 A:
Note:
940GML/945GM contact Power plan
945PM contact GAN plan

+2_5VRUN C234 0.1U_4 C207 4.7U_6
+V1.5_3GPLL C231 0.1U_4 C235 10U_8
+2_5VRUN C233 0.1U_4
R393 E@0_8 R2_5VRUN
R2_5VRUN
+V1.5_PCIE
R2.5VCRTDAC C256 0.1U_4 C258 0.022U_4
R2_5VRUNA C211 0.01U_4 C213 0.1U_4
RV3.3_ATVBG C270 0.1U_4 C271 0.022U_4
+V1.5_DPLLA +V1.5_DPLLB +V1.5_HPLL +V1.5_MPLL +V3.3_ATVBG +V3.3_ATVBG +1.5V VCCD_LVDS +V1.5_TVDAC +3VRUN +V1.5_QTVDAC 40mils +1.5V

LE4 B:

U35H — Calistoga — **POWER**

H22	VCCSYNC
C30	VCC_TXLVDS0
B30	VCC_TXLVDS1
A30	VCC_TXLVDS2
AJ41	VCC3G0
AB41	VCC3G1
Y41	VCC3G2
V41	VCC3G3
R41	VCC3G4
N41	VCC3G5
L41	VCC3G6
AC33	VCCA_3GPLL
G41	VCCA_3GBG
H41	VSSA_3GBG
F21	VCCA_CRTDAC0
E21	VCCA_CRTDAC1
G21	VSSA_CRTDAC
B26	VCCA_DPLLA
C39	VCCA_DPLLB
AF1	VCCA_HPLL
A38	VCCA_LVDS
B39	VSSA_LVDS
AF2	VCCA_MPLL
H20	VCCA_TVBG
G20	VSSA_TVBG
E19	VCCA_TVDACA0
F19	VCCA_TVDACA1
C20	VCCA_TVDACB0
D20	VCCA_TVDACB1
E20	VCCA_TVDACC0
F20	VCCA_TVDACC1
AH1	VCCD_HMPLL0
AH2	VCCD_HMPLL1
A28	VCCD_LVDS0
B28	VCCD_LVDS1
C28	VCCD_LVDS2
D21	VCCD_TVDAC
A23	VCC_HV0
B23	VCC_HV1
B25	VCC_HV2
H19	VCCD_QTVDAC
AK31	VCCAUX0
AE31	VCCAUX1
AE31	VCCAUX2
AC31	VCCAUX3
AL30	VCCAUX4
AK30	VCCAUX5
AJ30	VCCAUX6
AH30	VCCAUX7
AG30	VCCAUX8
AF30	VCCAUX9
AE30	VCCAUX10
AD30	VCCAUX11
AC30	VCCAUX12
AG29	VCCAUX13
AF29	VCCAUX14
AE29	VCCAUX15
AD29	VCCAUX16
AC29	VCCAUX17
AG28	VCCAUX18
AF28	VCCAUX19
AE28	VCCAUX20
AH22	VCCAUX21
AJ21	VCCAUX22
AH21	VCCAUX23
AJ20	VCCAUX24
AH20	VCCAUX25
AH19	VCCAUX26
P19	VCCAUX27
P16	VCCAUX28
AH15	VCCAUX29
P15	VCCAUX30
AH14	VCCAUX31
AG14	VCCAUX32
AF14	VCCAUX33
AE14	VCCAUX34
Y14	VCCAUX35
AE13	VCCAUX36
AE13	VCCAUX37
AE12	VCCAUX38
AE12	VCCAUX39
AD12	VCCAUX40

AC14	VTT_0
AB14	VTT_1
W14	VTT_2
V14	VTT_3
T14	VTT_4
R14	VTT_5
P14	VTT_6
N14	VTT_7
M14	VTT_8
L14	VTT_9
AD13	VTT_10
AC13	VTT_11
AB13	VTT_12
AA13	VTT_13
Y13	VTT_14
W13	VTT_15
V13	VTT_16
U13	VTT_17
T13	VTT_18
R13	VTT_19
N13	VTT_20
M13	VTT_21
L13	VTT_22
AB12	VTT_23
AA12	VTT_24
Y12	VTT_25
W12	VTT_26
V12	VTT_27
U12	VTT_28
T12	VTT_29
R12	VTT_30
P12	VTT_31
N12	VTT_32
M12	VTT_33
L12	VTT_34
R11	VTT_35
P11	VTT_36
N11	VTT_37
M11	VTT_38
R10	VTT_39
P10	VTT_40
N10	VTT_41
M10	VTT_42
P9	VTT_43
N9	VTT_44
M9	VTT_45
R8	VTT_46
P8	VTT_47
N8	VTT_48
M8	VTT_49
P7	VTT_50
N7	VTT_51
M7	VTT_52
R6	VTT_53
P6	VTT_54
M6	VTT_55
A6	VTT_56
R5	VTT_57
P5	VTT_58
N5	VTT_59
M5	VTT_60
P4	VTT_61
N4	VTT_62
M4	VTT_63
R3	VTT_64
P3	VTT_65
N3	VTT_66
M3	VTT_67
R2	VTT_68
P2	VTT_69
M2	VTT_70
D2	VTT_71
AB1	VTT_72
R1	VTT_73
P1	VTT_74
N1	VTT_75
M1	VTT_76

2005/07/14 VTTLF_CAP3 C303 0.47U_6

VTT_56 , VTT_71 and 72 are attached with 0.1u seperated .Checking

2005/07/14 VTTLF_CAP2 VTTLF_CAP1 C561 0.47U_6 C312 0.22U_4

+1.05V +1.5V +V1.5_PCIE +2_5VRUN +3VRUN

+1.05V (4,5,6,7,9,12,15,38,40)
+1.5V (5,7,9,13,15,27,38,40)
+V1.5_PCIE (7)
+2_5VRUN (19,22,40)
+3VRUN (3,5,7,9,12,13,14,15,16,17,18,19,20,22,23,26,27,28,30,31,32,33,36,40,41)

+1.05V C290 330U/2.5V/ESR-9/POS C245 4.7U/6.3v_8 C283 2.2U/6.3V_6 C249 0.1U_4 C261 10U_8
+1.05V C241 0.22U_4 C239 0.22U_4 C264 0.47U_6 C284 0.47U_6

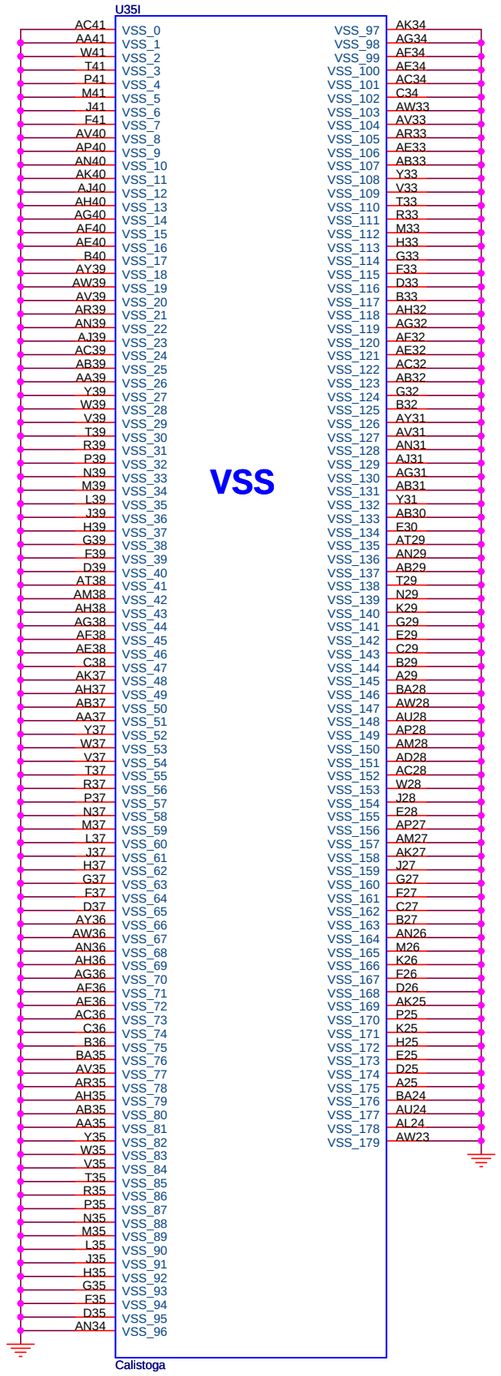
+2_5VRUN R91 10_4 VCCGFOLLOW BAT54 D1 PDZ5.6B +1.05V
L19 FCM2012C-121_8 +V2.5_CRTDAC
Within 3" of GMCH

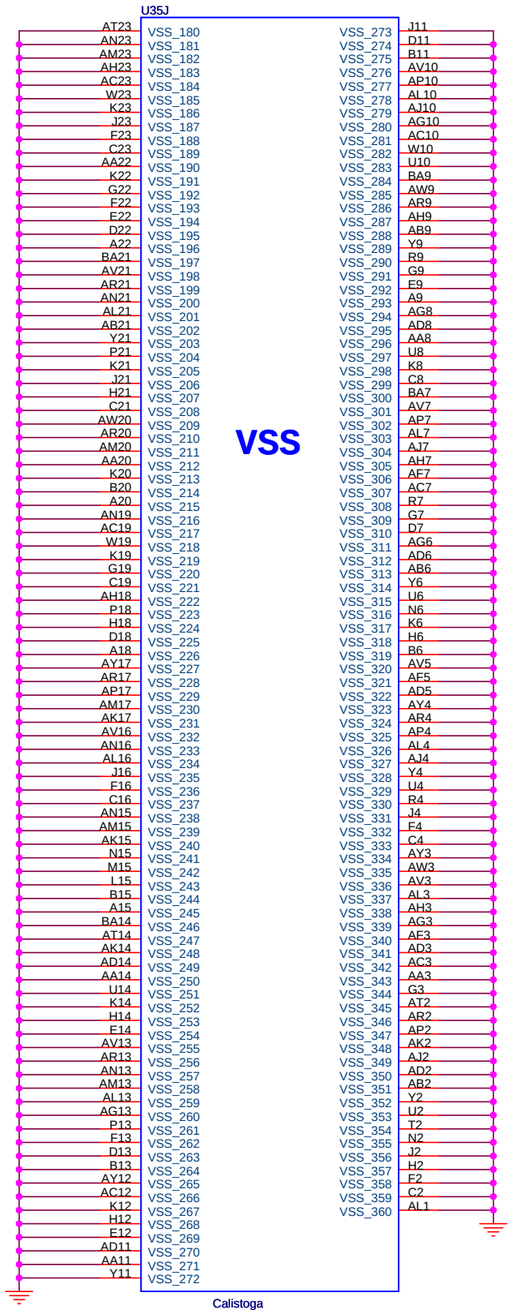
+3.3S_TVDAC_LDO
For TV-OUT
U16 I@AAT3218 OUT IN GND BYP EN
C300 I@10U_8 C299 I@0.01U_4 +5VRUN C306 I@1U_6

LE4 B:
Note:
940GML/945GM has circuit
945PM NA

PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	Calistoga_E (POWER2)	1A
Date: Tuesday, March 14, 2006	Sheet 10 of 42	





PROJECT : LE4

Quanta Computer Inc.

Size	Document Number	Rev
	Calistoga_F (VSS NCTF)	1A
Date: Wednesday, November 16, 2005	Sheet 11 of 42	

RTC

Place near to Mini-door

CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF

LE4 A:

LE4 B: Change C459 value from 18p to 15p

VCCRTC
C667 1U_4
3VPCU
D15 CH500H-40
VCCRTC_2
D14 CH500H-40
R312 1K/F_4
R546 1M_4
C684 1U/6.3V_4
R545 20K/F_4
G1 SHORT_ PAD1
C459 15P_4
CLK_32KX1
Y5 32.768KHZ BG332768909
C457 18P_4
CLK_32KX2
R315 10M_6
BT1 BAT_CONN
RTCRST#
SM_INTRUDER#
ICH_INTVRMEN
Internal PU

U23A

AB1 RTXC1
AB2 RTCX2
AA3 RTCRST#
Y5 INTRUDER#
W4 INTVRMEN

RTC

W1 EE_CS
Y1 EE_SHCLK
Y2 EE_DOUT
W3 EE_DIN

LPC

V3 LAN_CLK
U3 LAN_RSTSYNC
U5 LAN_RXD0
V4 LAN_RXD1
T5 LAN_RXD2
U7 LAN_TXD0
V6 LAN_TXD1
V7 LAN_TXD2

LAN

5VPCU
R316 1.2K/F_4
R317 1K/F_4
Q23 MMBT3904
R310 4.7K_4
R311 15K/F_4
20MIL
20MIL
VCCRTC_1
VCCRTC_3
add RTC Bat rechargeable circuit

CPU

ACZ_BCLK U1 ACZ_BIT_CLK
ACZ_SYNC R6 ACZ_SYNC
ACZ_RST# R5 ACZ_RST#
ACZ_SDIN0 T2 ACZ_SDIN0
ACZ_SDIN1 T3 ACZ_SDIN1
ACZ_SDIN2 T1 ACZ_SDIN2
ACZ_SDOUT T4 ACZ_SDOUT

AC-97/AZALIA

T254
T124

+3VRUN
R494 10K_4
Internal PU
(31) SATA_LED# → SATA_LED# → AF18 SATALED#
Review current rating

(32) SATA_RXN0_C → SATA_RXN0_C → AF3 SATA0RXN
(32) SATA_RXP0_C → SATA_RXP0_C → AE3 SATA0RXP
(32) SATA_TXN0 → C449 3900P_P_4 → SATA_TXN0_C → AG2 SATA0TXN
(32) SATA_TXP0 → C448 3900P_P_4 → SATA_TXP0_C → AH2 SATA0TXP
CKL:1n ~ 20nF

T245 SATA_RXN2_C AE7 SATA2RXN
T243 SATA_RXP2_C AE7 SATA2RXP
T249 SATA_TXN2_C AG6 SATA2TXN
T248 SATA_TXP2_C AH6 SATA2TXP

(3) CLK_PCIE_SATA# → CLK_PCIE_SATA# → AF1 SATA_CLKN
(3) CLK_PCIE_SATA → CLK_PCIE_SATA → AE1 SATA_CLKP

25mils/15mils

R289 24.9/F_4 SATA_BIAS → AH10 SATARBIASN, AG10 SATARBIASP
Place within 500 mils of ICH7

SATA

(32) PDIOR# → PDIOR# → AF15 DIOR#
(32) PDIOW# → PDIOW# → AH15 DIOW#
(32) PDDACK# → PDDACK# → AF16 DDACK#
(32) IRQ14 → IRQ14 → AH16 IDEIRQ
(32) PIORDY → PIORDY → AG16 IORDY
(32) PDDREQ → PDDREQ → AE15 DDREQ

IDE

ICH7-M

+3VRUN
R334 4.7K_4
R496 4.7K_4
Difference
IRQ14
PIORDY

LE4 B:
Change R496 and R334 from 8.2K to 4.7K

LAD0 AA6 LAD0 → LAD0 (26,27,30)
LAD1 AB5 LAD1 → LAD1 (26,27,30)
LAD2 AC4 LAD2 → LAD2 (26,27,30)
LAD3 Y6 LAD3 → LAD3 (26,27,30)
LDRQ0# AC3 LDRQ#0 → LDRQ#0 (26,27,30)
LDRQ1#/GPIO23 AA5 LDRQ#1 → T251
LFRAME# AB3 → LFRAME# (26,27,30)
A20GATE AE22 GATEA20 → GATEA20 (30)
A20M# AH28 → H_A20M# (4)
CPUSLP# AG27 TP_H_CPUSLP# → R222 *0_4 → H_CPUSLP# (4,6)
TP1/DPRSTP# AE24 H_DPRSTP# R → R477 0_4
TP2/DPSLP# AH25 H_DPSLP# R → R473 0_4 → ICH_DPRSTP# (4,37), H_DPSLP# (4)
FERR# AG26 → H_FERR# (4)
GPIO49/CPUPWRGD AG24 → R481 0/F_4 → H_PWRGD (4)
IGNNE# AG22 → H_IGNNE# (4)
INIT3_3V# AG21 → T97
INIT# AF22 → H_INIT# (4)
INTR AE25 → H_INTR (4)
RCIN# AG23 RCIN# → RCIN# (30)
NMI AH24 → H_NMI (4)
SMI# AF23 H_SMI# R → R479 0_4 → H_SMI# (4)
STPCLK# AH22 → H_STPCLK# (4)
THERMTRIP# AF26 H_THERMTRIP_R → R471 24.9_4 → PM_THRMTRIP# (4,7)

R5506 close to MCH

+3VRUN
R236 10K_4
R244 10K_4
RCIN#
GATEA20

+1.05V
R226 *56_4
R234 *56_4

+1.05V
R230 56_4
Should be 2" close ICH7

Difference

+1.05V
R472 56_4
Should be 2" close ICH7

DD0 AB15 PDD0
DD1 AE14 PDD1
DD2 AG13 PDD2
DD3 AE13 PDD3
DD4 AD14 PDD4
DD5 AC13 PDD5
DD6 AD12 PDD6
DD7 AC12 PDD7
DD8 AE12 PDD8
DD9 AE12 PDD9
DD10 AB13 PDD10
DD11 AC14 PDD11
DD12 AE14 PDD12
DD13 AH13 PDD13
DD14 AH14 PDD14
DD15 AC15 PDD15
→ PDD[15:0] (32)

DA0 AH17 PDA0
DA1 AE17 PDA1
DA2 AE17 PDA2
→ PDA[2:0] (32)

DCS1# AE16 → PDCS1# (32)
DCS3# AD16 → PDCS3# (32)

ICH7 internal VR enable strap

	INTVRMEN
Enable (default)	1
Disable	0

VCCRTC
R555 332K/F_6
ICH_INTVRMEN
R556 *0/F_4

0 ohm ?

ACZ_SDIN0 → ACZ_SDIN0 (28)
ACZ_SDOUT R552 39_4 → ACZ_SDOUT_AUDIO (28)
C689 *10P_4
ACZ_SYNC R553 39_4 → ACZ_SYNC_AUDIO (28)
C690 *10P_4
ACZ_BCLK R551 39_4 → BIT_CLK_AUDIO (28)
C688 *10P_4
ACZ_RST# R547 39_4 → ACZ_RST#_AUDIO (28)

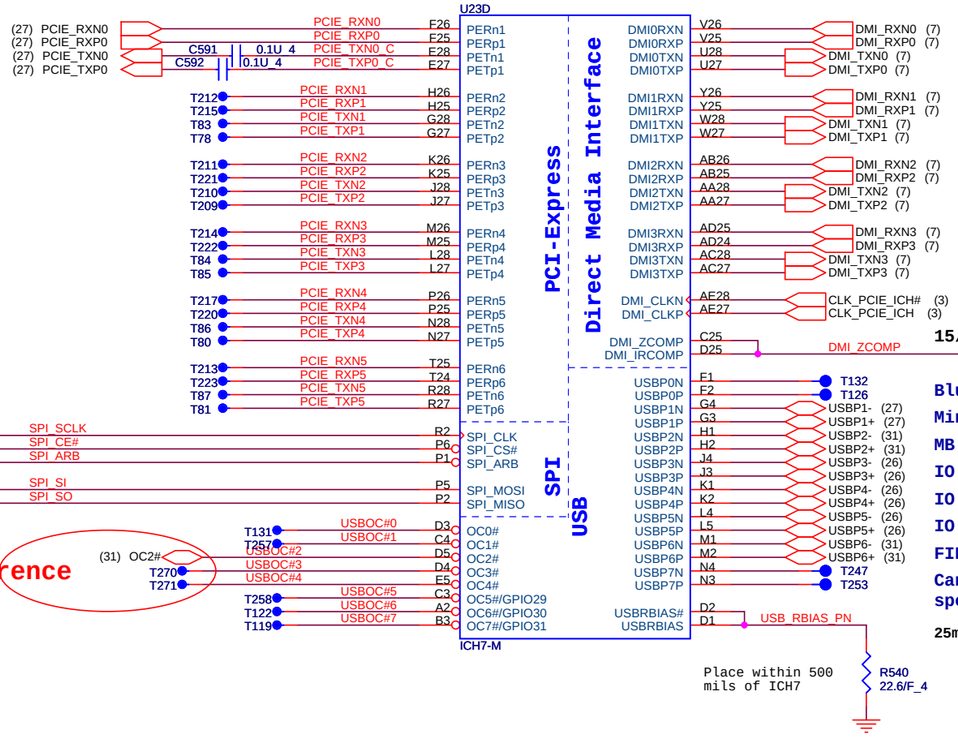
Near To ICH7-M

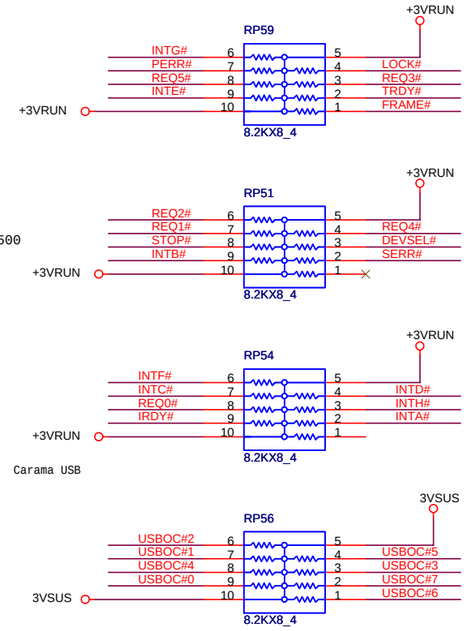
PROJECT : LE4
Quanta Computer Inc.

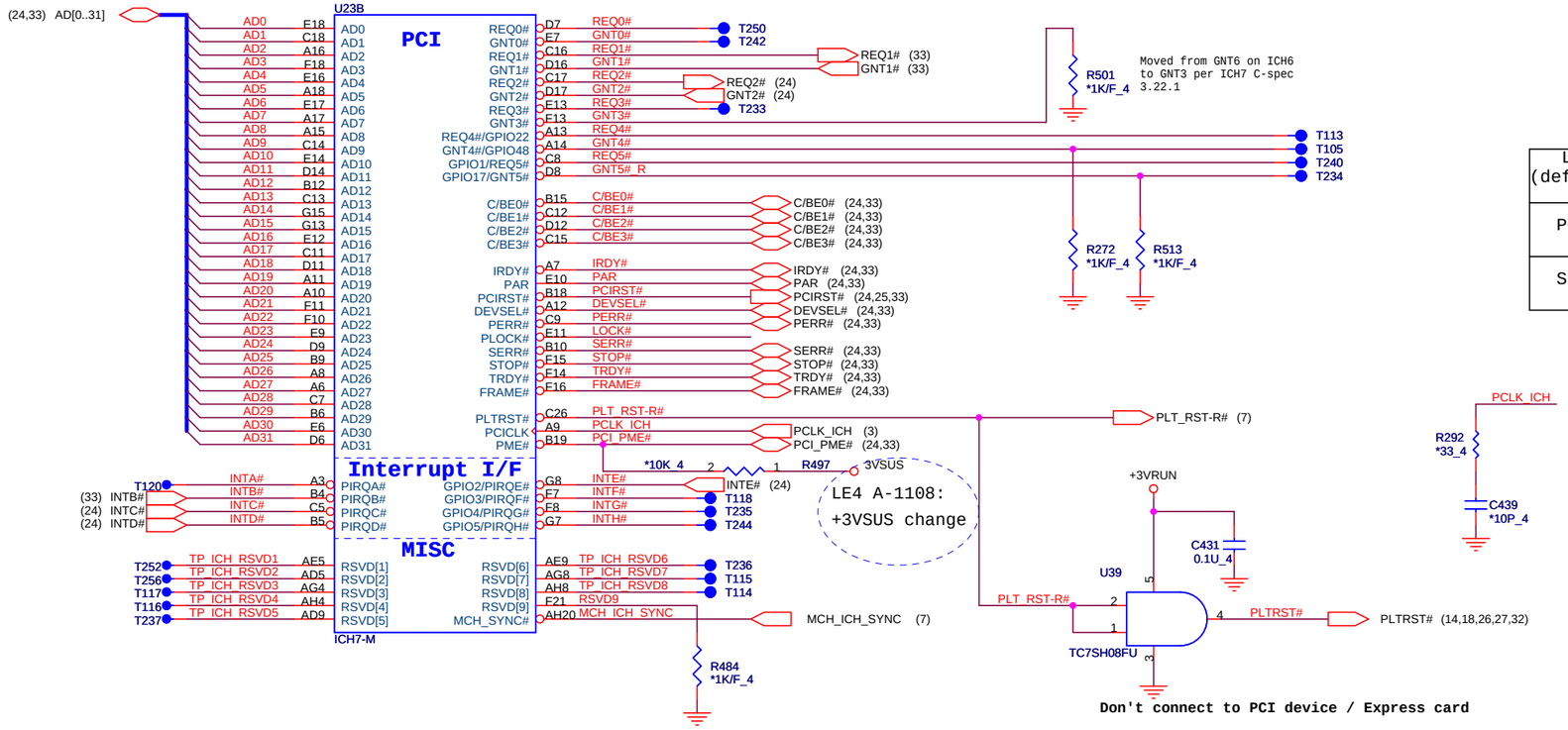
Size	Document Number	Rev
	ICH7-M HOST (1 of 4)	1A
Date: Tuesday, March 14, 2006	Sheet 12 of 42	

MINI CARD PCI-E

EXPRESS CARD (NEW CARD)







ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

PROJECT : LE4

Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M PCI E (2 of 4)	1A

Date: Tuesday, March 14, 2006 Sheet 13 of 42

R376

No stuff-->boot
Stuff-->No boot

LE4 B:
Change Value from 1K to 680

PCLK_SMB R482 2.2K_4
PDAT_SMB R485 2.2K_4
PCIE_WAKE# R498 680_4

RI# R207 10K_4
SMB_LINK_ALERT# R215 10K_4
SMLINK0 R218 10K_4
SMLINK1 R221 10K_4
EXTSMI# R R495 *10K_4
WAKE_SCI# R R459 10K_4
SMBALERT# R225 10K_4

DNBSWON# R478 10K_4
SYS_RST# R229 10K_6
PM_BATLOW# R247 8.2K/F_4
SWI# R270 10K_4

CLKRUN# R259 8.2K/F_4
SERIRQ R248 8.2K/F_4
LCDID0 R554 10K_4
LCDID1 R253 10K_4
RUNTIME_SCI# R R488 10K/F_4
SYS_RST# R238 *10K/F_4
RSMRST# R294 10K/F_4

to Clock Gen & DIMM

SYS_RST is suspend rail

+3VRUN R267 *1K_4

(28) ACZ_SPKR

(3,33) PCLK_SMB
(3,33) PDAT_SMB
T88
T92
T94
(24,26) RI#
(24,26,27) SUS_STAT#
(4) SYS_RST#
(7) PM_BMBUSY#
R499 0/F_4
SMBALERT#
No ASF support
(3) PM_STPPCI#
(3) PM_STPCPU#
R250 *10K_4
R246 *10K/F_4
R483 0_4
R486 0/F_4
PM_STPPCI_ICH#
PM_STPCPU_ICH#
T96
T99
T216
BIOS_REC_R
FWH_MFG_MODE_R
(24,26,27,30,33) CLKRUN#
T229
ICH_GPO33
BOARD_ID2
(27) PCIE_WAKE#
(24,26,27,30) SERIRQ
(5) THERM_ALERT#
R252 8.2K/F_4
VR_PWRGD_CK410
T225
R491 0_4
R492 0/F_4
RUNTIME_SCI# R
EXTSMI# R
(30) SCI#
(30) KBSMI#

Note: Connect to EC; Reserve PH/3V

U23C

SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SPKR
SUS_STAT#
SYS_RST#
GPIO0/BM_BUSY#
GPIO11/SMBALERT#
GPIO18/STPPCI#
GPIO20/STPCPU#
GPIO26
GPIO27
GPIO28
GPIO32/CLKRUN#
GPIO33/AZ_DOCK_EN#
GPIO34/AZ_DOCK_RST#
WAKE#
SERIRQ
THRM#
VRMPWRGD
GPIO6
GPIO7
GPIO8

SMB
SYS GPIO
Power MGT
GPIO

GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
PWROK
GPIO16/DPRSLPVR
TP0/BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
GPIO9
GPIO10
GPIO12
GPIO13
GPIO14
GPIO15
GPIO24
GPIO25
GPIO35
GPIO38
GPIO39

ICH7-M

BOARD_ID0
BOARD_ID1
BOARD_ID3
BOARD_ID4
14M_ICH
CLKUSB_48
ICH_SUSCLK
T231
R476 100/F_4
R480 100/F_4
SUSB# (30)
SUSC# (30)
T219
ICH_PWROK
R227 0_4
R233 *100K/F_4
PM_EXTTS#1 (7,17)
PM_DPRSLPVR (37)
PM_DPRSLPVR_R
R475 100/F_4
PM_BATLOW# (30)
PM_BATLOW#
R243 100/F_4
DNBSWON#
R500 100K/F_4
DNBSWON# (30)
R460 0/F_4
PLTRST# (13,18,26,27,32)
PM_RSMRST#_R
R295 100/F_4
RSMRST#
RSMRST# (30)
SWI#
SWI# (30)
T98
T226
T79
LCDID0
LCDID1
LCDID0 (22)
LCDID1 (22)
T261
GPIO24
GPIO25
T230
AMP_BEEP (28)
R_PLTRST_DELAY#
R255 *E@0_4
T218
PLTRST_DELAY#
PLTRST_DELAY# (18)

GPIO25 /Suspend rail is a HW strap , don't pull down .

CKL :100Kohm PD

MXM_ON#: 1 -> No MXM Module
0 -> MXM Module

MXM_THERM# R251 10K_4 +3V_S5

GPIO24 USBEN_LS# (26)
GPIO25 USBEN_RJ# (26)

+3VRUN R239 *10K_4
(3,37) CLK_EN#
U21
NL17SZ14DFT2G
VR_PWRGD_CK410

Note: External pull-up 3V

LE4 B:
del R487,R256,R469 and R462in BOM

LE4 C:
Add to select power on/off for USB function with R598 and R597

+3VRUN R487 *10K/F_6
R256 *0/F_4
BIOS_REC
BIOS_REC_R R597 0_4
USBEN_MB# (31)
R489 *0_4

3VPCU R462 *10K_4
R469 *0/F_4
FWH_MFG_MODE
FWH_MFG_MODE_R R598 0_4
(26) USBEN_LE3#
R470 *0_4

LE4 C:
Add to select power on/off for USB function

3VSUS
PWM require 6.9K
Change to 6.8K
R543 6.8K_4
C675 0.047U_4
+3VRUN
U41
(7,37) DELAY_VR_PWRGOOD
(22,30) PWROK
R542
100K_4
TC7SH08FU
ICH_PWROK
R541 10K_4

Level is incorrect !!

CLKUSB_48
14M_ICH
R314 *10_4
R550 *33_4
C458 *10P_4
C681 *10P_4

LE4 A:
Place close to ICH7

+3VRUN R265 *10K/F_4 BOARD_ID0 R512 10K_4
+3VRUN R493 *10K/F_4 BOARD_ID1 R490 10K/F_4
+3VRUN R466 *10K_4 BOARD_ID2 R461 10K/F_4

CHECK

PATA,SATA Select
PATA Mode: 1
SATA Mode: 0

+3VRUN R257 *10K_4 BOARD_ID3 R258 10K_4
+3VRUN R268 *10K_4 BOARD_ID4 R269 10K_4

BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	BOARD_ID4	
GPIO21	GPIO19	GPIO34	GPIO36	GPIO37	
L	L	L	L	L	LE3--L
L	L	L	L	H	LE4--H

PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M GPIO (3 of 4)	1A
Date: Tuesday, March 14, 2006	Sheet 14 of 42	

LE4 C:
Del C386

Add C718 and C719

Oreginal 270U P/N "CH7270LM885"

Check with Intel for power plan.

30mils

30mils

U23E — ICH7-M

A4	VSS[1]	VSS[98]	P28
A23	VSS[2]	VSS[99]	R1
B1	VSS[3]	VSS[100]	R11
B8	VSS[4]	VSS[101]	R12
B11	VSS[5]	VSS[102]	R13
B14	VSS[6]	VSS[103]	R14
B17	VSS[7]	VSS[104]	R15
B20	VSS[8]	VSS[105]	R16
B26	VSS[9]	VSS[106]	R17
B28	VSS[10]	VSS[107]	R18
C2	VSS[11]	VSS[108]	T6
C6	VSS[12]	VSS[109]	T12
C27	VSS[13]	VSS[110]	T13
D10	VSS[14]	VSS[111]	T14
D13	VSS[15]	VSS[112]	T15
D18	VSS[16]	VSS[113]	T16
D21	VSS[17]	VSS[114]	T17
D24	VSS[18]	VSS[115]	U4
E1	VSS[19]	VSS[116]	U12
E2	VSS[20]	VSS[117]	U13
E4	VSS[21]	VSS[118]	U14
E8	VSS[22]	VSS[119]	U15
E15	VSS[23]	VSS[120]	U16
E3	VSS[24]	VSS[121]	U17
F4	VSS[25]	VSS[122]	U24
F5	VSS[26]	VSS[123]	U25
F12	VSS[27]	VSS[124]	U26
F27	VSS[28]	VSS[125]	V2
F28	VSS[29]	VSS[126]	V13
G1	VSS[30]	VSS[127]	V15
G2	VSS[31]	VSS[128]	V24
G5	VSS[32]	VSS[129]	V27
G6	VSS[33]	VSS[130]	V28
G9	VSS[34]	VSS[131]	W6
G14	VSS[35]	VSS[132]	W24
G18	VSS[36]	VSS[133]	W25
G21	VSS[37]	VSS[134]	W26
G24	VSS[38]	VSS[135]	Y3
G25	VSS[39]	VSS[136]	Y24
G26	VSS[40]	VSS[137]	Y27
H3	VSS[41]	VSS[138]	Y28
H4	VSS[42]	VSS[139]	AA1
H5	VSS[43]	VSS[140]	AA24
H24	VSS[44]	VSS[141]	AA25
H27	VSS[45]	VSS[142]	AA26
H28	VSS[46]	VSS[143]	AB4
J1	VSS[47]	VSS[144]	AB6
J2	VSS[48]	VSS[145]	AB11
J5	VSS[49]	VSS[146]	AB14
J24	VSS[50]	VSS[147]	AB16
J25	VSS[51]	VSS[148]	AB19
J26	VSS[52]	VSS[149]	AB21
K24	VSS[53]	VSS[150]	AB24
K27	VSS[54]	VSS[151]	AB27
K28	VSS[55]	VSS[152]	AB28
L13	VSS[56]	VSS[153]	AC2
L15	VSS[57]	VSS[154]	AC5
L24	VSS[58]	VSS[155]	AC9
L25	VSS[59]	VSS[156]	AC11
L26	VSS[60]	VSS[157]	AD1
M3	VSS[61]	VSS[158]	AD3
M4	VSS[62]	VSS[159]	AD4
M5	VSS[63]	VSS[160]	AD7
M12	VSS[64]	VSS[161]	AD8
M13	VSS[65]	VSS[162]	AD11
M14	VSS[66]	VSS[163]	AD15
M15	VSS[67]	VSS[164]	AD19
M16	VSS[68]	VSS[165]	AD23
M17	VSS[69]	VSS[166]	AE2
M24	VSS[70]	VSS[167]	AE4
M27	VSS[71]	VSS[168]	AE8
M28	VSS[72]	VSS[169]	AE11
N1	VSS[73]	VSS[170]	AE13
N2	VSS[74]	VSS[171]	AE18
N5	VSS[75]	VSS[172]	AE21
N6	VSS[76]	VSS[173]	AE24
N11	VSS[77]	VSS[174]	AE25
N12	VSS[78]	VSS[175]	AF2
N13	VSS[79]	VSS[176]	AF4
N14	VSS[80]	VSS[177]	AF8
N15	VSS[81]	VSS[178]	AF11
N16	VSS[82]	VSS[179]	AF27
N17	VSS[83]	VSS[180]	AF28
N18	VSS[84]	VSS[181]	AG1
N24	VSS[85]	VSS[182]	AG3
N25	VSS[86]	VSS[183]	AG7
N26	VSS[87]	VSS[184]	AG11
P3	VSS[88]	VSS[185]	AG14
P4	VSS[89]	VSS[186]	AG17
P12	VSS[90]	VSS[187]	AG20
P13	VSS[91]	VSS[188]	AG25
P14	VSS[92]	VSS[189]	AH1
P15	VSS[93]	VSS[190]	AH3
P16	VSS[94]	VSS[191]	AH7
P17	VSS[95]	VSS[192]	AH12
P24	VSS[96]	VSS[193]	AH23
P27	VSS[97]	VSS[194]	AH27

U23F — ICH7-M

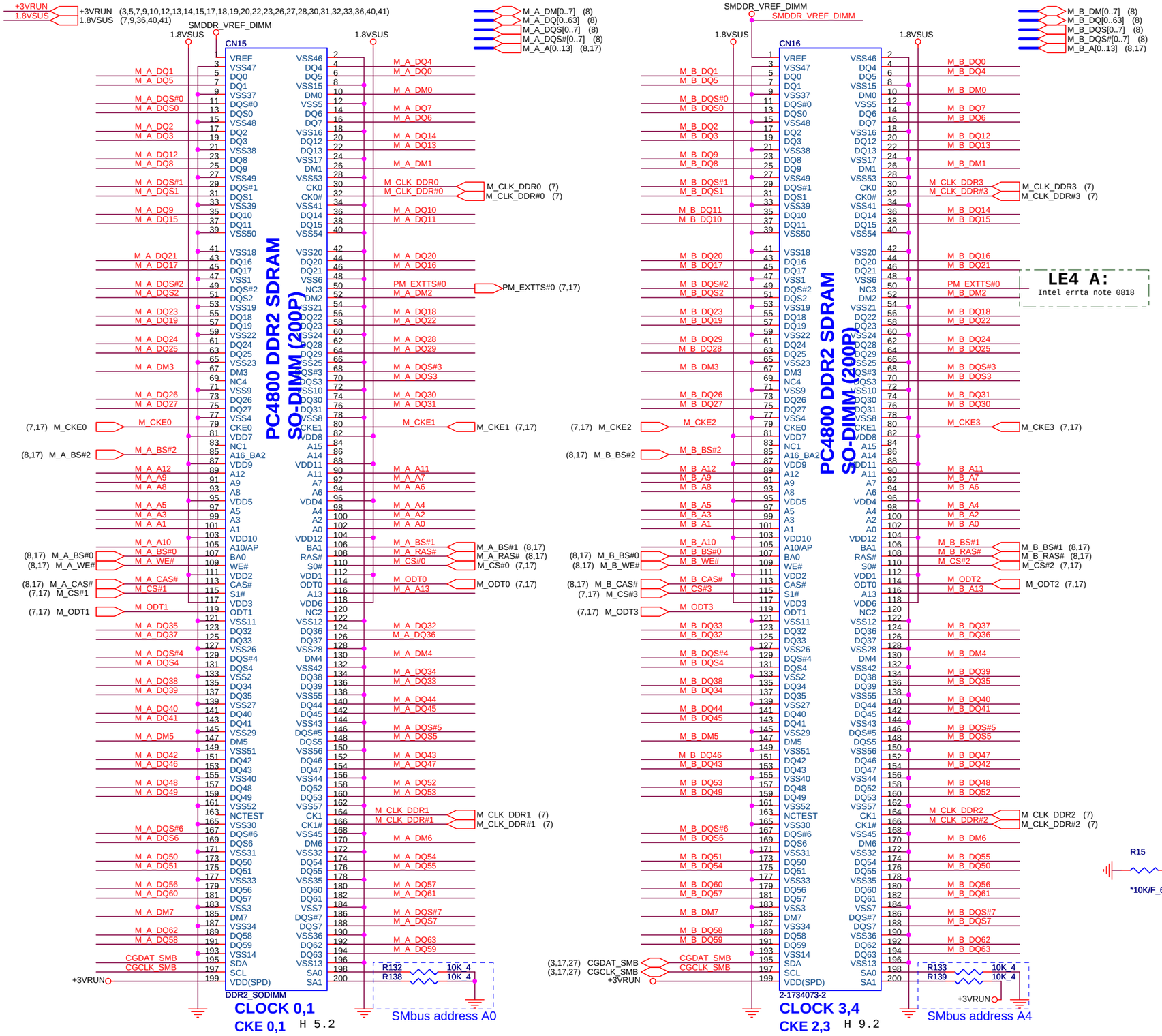
G10	V5REF[1]	Vcc1_05[1]	L11
AD17	V5REF[2]	Vcc1_05[2]	L12
F6	V5REF_Sus	Vcc1_05[3]	L14
AA22	Vcc1_5_B[1]	Vcc1_05[4]	L16
AA23	Vcc1_5_B[2]	Vcc1_05[5]	L17
AB22	Vcc1_5_B[3]	Vcc1_05[6]	L18
AB23	Vcc1_5_B[4]	Vcc1_05[7]	M11
AC23	Vcc1_5_B[5]	Vcc1_05[8]	M18
AC24	Vcc1_5_B[6]	Vcc1_05[9]	P11
AC25	Vcc1_5_B[7]	Vcc1_05[10]	P18
AC26	Vcc1_5_B[8]	Vcc1_05[11]	T11
AD26	Vcc1_5_B[9]	Vcc1_05[12]	T18
AD27	Vcc1_5_B[10]	Vcc1_05[13]	U11
AD28	Vcc1_5_B[11]	Vcc1_05[14]	U18
D26	Vcc1_5_B[12]	Vcc1_05[15]	V11
D27	Vcc1_5_B[13]	Vcc1_05[16]	V12
D28	Vcc1_5_B[14]	Vcc1_05[17]	V14
E24	Vcc1_5_B[15]	Vcc1_05[18]	V16
E25	Vcc1_5_B[16]	Vcc1_05[19]	V17
E26	Vcc1_5_B[17]	Vcc1_05[20]	V18
F23	Vcc1_5_B[18]	VCC_PAUX	
F24	Vcc1_5_B[19]	VccSus3_3/VccLAN3_3[1]	V5
G22	Vcc1_5_B[20]	VccSus3_3/VccLAN3_3[2]	V1
G23	Vcc1_5_B[21]	VccSus3_3/VccLAN3_3[3]	W2
H22	Vcc1_5_B[22]	VccSus3_3/VccLAN3_3[4]	W7
H23	Vcc1_5_B[23]	Vcc3_3/VccHDA	U6
J22	Vcc1_5_B[24]	VccSus3_3/VccSusHDA	R7
J23	Vcc1_5_B[25]	V_CPU_IO[1]	AE23
K22	Vcc1_5_B[26]	V_CPU_IO[2]	AE26
K23	Vcc1_5_B[27]	V_CPU_IO[3]	AH26
L22	Vcc1_5_B[28]	VCCA3GP	
L23	Vcc1_5_B[29]	Vcc3_3[3]	AA7
M22	Vcc1_5_B[30]	Vcc3_3[4]	AB12
M23	Vcc1_5_B[31]	Vcc3_3[5]	AB20
N22	Vcc1_5_B[32]	Vcc3_3[6]	AC16
N23	Vcc1_5_B[33]	Vcc3_3[7]	AD13
P22	Vcc1_5_B[34]	Vcc3_3[8]	AD18
P23	Vcc1_5_B[35]	Vcc3_3[9]	AG12
R22	Vcc1_5_B[36]	Vcc3_3[10]	AG15
R23	Vcc1_5_B[37]	Vcc3_3[11]	AG19
R24	Vcc1_5_B[38]	IDE	
R25	Vcc1_5_B[39]	Vcc3_3[12]	A5
R26	Vcc1_5_B[40]	Vcc3_3[13]	B13
T22	Vcc1_5_B[41]	Vcc3_3[14]	B16
T23	Vcc1_5_B[42]	Vcc3_3[15]	B7
T26	Vcc1_5_B[43]	Vcc3_3[16]	C10
T27	Vcc1_5_B[44]	Vcc3_3[17]	D15
T28	Vcc1_5_B[45]	Vcc3_3[18]	F9
U22	Vcc1_5_B[46]	Vcc3_3[19]	G11
U23	Vcc1_5_B[47]	Vcc3_3[20]	G12
V22	Vcc1_5_B[48]	Vcc3_3[21]	G16
V23	Vcc1_5_B[49]	PCI	
W22	Vcc1_5_B[50]	VccRTC	W5
W23	Vcc1_5_B[51]	VccSus3_3[1]	P7
Y22	Vcc1_5_B[52]	VccSus3_3[2]	A24
Y23	Vcc1_5_B[53]	VccSus3_3[3]	C24
B27	Vcc3_3[1]	VccSus3_3[4]	D19
AG28	VccDMIPLL	VccSus3_3[5]	D22
AB7	Vcc1_5_A[1]	VccSus3_3[6]	G19
AC6	Vcc1_5_A[2]	VccSus3_3[7]	K3
AC7	Vcc1_5_A[3]	VccSus3_3[8]	K4
AD6	Vcc1_5_A[4]	VccSus3_3[9]	K5
AE6	Vcc1_5_A[5]	VccSus3_3[10]	K6
AE5	Vcc1_5_A[6]	VccSus3_3[11]	L1
AE6	Vcc1_5_A[7]	VccSus3_3[12]	L2
AG5	Vcc1_5_A[8]	VccSus3_3[13]	L3
AH5	Vcc1_5_A[9]	VccSus3_3[14]	L6
AD2	VccSATAPLL	VccSus3_3[15]	L7
AH11	Vcc3_3[2]	VccSus3_3[16]	M6
AB10	Vcc1_5_A[10]	VccSus3_3[17]	M7
AB9	Vcc1_5_A[11]	VccSus3_3[18]	N7
AC10	Vcc1_5_A[12]	USB	
AD10	Vcc1_5_A[13]	Vcc1_5_A[19]	AB17
AE10	Vcc1_5_A[14]	Vcc1_5_A[20]	AC17
AF10	Vcc1_5_A[15]	Vcc1_5_A[21]	T7
AF9	Vcc1_5_A[16]	Vcc1_5_A[22]	F17
AG9	Vcc1_5_A[17]	Vcc1_5_A[23]	G17
AH9	Vcc1_5_A[18]	Vcc1_5_A[24]	AB8
E3	VccSus3_3[19]	Vcc1_5_A[25]	AC8
C1	VccUSBPLL	VccSus1_05[1]	K7
AA2	VccSus1_05/VccLAN1_05[1]	VccSus1_05[2]	C28
Y7	VccSus1_05/VccLAN1_05[2]	VccSus1_05[3]	G20
		Vcc1_5_A[26]	A1
		Vcc1_5_A[27]	H6
		Vcc1_5_A[28]	H7
		Vcc1_5_A[29]	J6
		Vcc1_5_A[30]	J7
		USB CORE	

ICH7-M

Size	Document Number	Rev
	ICH-M POWER (4 of 4)	1A
Date: Tuesday, February 07, 2006	Sheet 15 of 42	

PROJECT : LE4

Quanta Computer Inc.



PROJECT : LE4

Quanta Computer Inc.

Size	Document Number	Rev
	DDR II SO-DIMM (200P)	1A

Date: Tuesday, March 14, 2006 Sheet 16 of 42

DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL

M_A_A[13..0] → M_A_A[13..0] (8,16)
SMDDR_VTERM → SMDDR_VTERM (16,36,40)

SMDDR_VTERM

C127	C218	C128	C135	C220	C180	C209	C204	C182	C139	C157	C219	C212
0.1U_4	0.1U_4	0.1U_4	0.1U_4	0.1U_4	0.1U_4	0.1U_4	0.1U_4	0.1U_4	0.1U_4	0.1U_4	0.1U_4	0.1U_4

(7,16) M_ODT0	M_ODT0	RP25	1	2	56X2
	M_A_A13		3	4	
	M_A_A9	RP9	1	2	56X2
	M_A_A8		3	4	
	M_A_A5	RP15	1	2	56X2
	M_A_A3		3	4	
	M_A_A11	RP5	1	2	56X2
(7,16) M_CKE1	M_CKE1		3	4	
	M_A_A10	RP17	1	2	56X2
(8,16) M_A_WE#	M_A_WE#		3	4	
	M_A_A6	RP10	1	2	56X2
	M_A_A7		3	4	
	M_A_A2	RP13	1	2	56X2
	M_A_A4		3	4	
(8,16) M_A_BS#1	M_A_BS#1	RP18	1	2	56X2
	M_A_A0		3	4	
	M_A_A12	RP7	1	2	56X2
	M_A_A1		3	4	
(8,16) M_A_CAS#	M_A_CAS#	RP21	1	2	56X2
(8,16) M_A_BS#0	M_A_BS#0		3	4	

All → SMDDR_VTERM

DDRII B CHANNEL

M_B_A[13..0] → M_B_A[13..0] (8,16)
1.8VSUS → 1.8VSUS (7,9,16,36,40,41)
+3VRUN → +3VRUN (3,5,7,9,10,12,13,14,15,16,18,19,20,22,23,26,27,28,30,31,32,33,36,40,41)

SMDDR_VTERM

C181	C156	C137	C217	C206	C179	C134	C133	C129	C225	C223	C224	C221	
0.1U_4	0.1U_4	0.1U_4	0.1U_4	0.1U_4	0.1U_4	0.1U_4	0.1U_4	0.1U_4	0.1U_4	0.1U_4	0.1U_4	0.1U_4	0.1U_4

Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

(8,16) M_B_BS#1	M_B_BS#1	RP20	1	2	56X2
	M_B_A0		3	4	
	M_B_A3	RP16	1	2	56X2
	M_B_A1		3	4	
	M_B_A12	RP11	1	2	56X2
	M_B_A5		3	4	
	M_B_A2	RP14	1	2	56X2
	M_B_A4		3	4	
	M_B_A8	RP8	1	2	56X2
	M_B_A9		3	4	
	M_B_A6	RP12	1	2	56X2
	M_B_A7		3	4	
(7,16) M_CKE2	M_CKE2	RP3	1	2	56X2
(8,16) M_B_BS#2	M_B_BS#2		3	4	
(7,16) M_CS#2	M_CS#2	RP23	1	2	56X2
(8,16) M_B_RAS#	M_B_RAS#		3	4	
(8,16) M_B_WE#	M_B_WE#	RP24	1	2	56X2
(8,16) M_B_CAS#	M_B_CAS#		3	4	
	M_B_A10	RP19	1	2	56X2
(8,16) M_B_BS#0	M_B_BS#0		3	4	

All → SMDDR_VTERM

(7,16) M_CS#0	M_CS#0	RP22	1	2	56X2
(8,16) M_A_RAS#	M_A_RAS#		3	4	
(7,16) M_ODT2	M_ODT2	RP28	1	2	56X2
	M_B_A13		3	4	
(7,16) M_CS#3	M_CS#3	RP27	1	2	56X2
(7,16) M_ODT3	M_ODT3		3	4	
(7,16) M_ODT1	M_ODT1	RP26	1	2	56X2
(7,16) M_CS#1	M_CS#1		3	4	
	M_B_A11	RP6	1	2	56X2
(7,16) M_CKE3	M_CKE3		3	4	
(8,16) M_A_BS#2	M_A_BS#2	RP4	1	2	56X2
(7,16) M_CKE0	M_CKE0		3	4	

All → SMDDR_VTERM

Uninstall

+3VRUN
R62 *200_4
C185 *0.1U_4
LM86_3V
DDR_THERMDA
DDR_THERMDC
Q2 *PMST3904

U9 *LM86CIMM

(3,16,27) CGCLK_SMB	CGCLK_SMB	8	SCLK	VCC	1
(3,16,27) CGDAT_SMB	CGDAT_SMB	7	SDA	DXP	2
(7,16) PM_EXTTS#0	PM_EXTTS#0	6	ALERT#	DXN	3
(7,14) PM_EXTTS#1	PM_EXTTS#1 R58 *0_4	4	OVERT#	GND	5

Allen

PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	DDR II TERMINATION	1A
Date: Tuesday, March 14, 2006	Sheet 17 of 42	

(7) PCIE_MTX_GRX_P[0..15]
(7) PCIE_MTX_GRX_N[0..15]

(7) PCIE_MRX_GTX_P[0..15]

PCIE_MRX_GTX_P0	E@0.1U_4 C148	PCIE_MRX_GTX_C_P0
PCIE_MRX_GTX_P1	E@0.1U_4 C172	PCIE_MRX_GTX_C_P1
PCIE_MRX_GTX_P2	E@0.1U_4 C150	PCIE_MRX_GTX_C_P2
PCIE_MRX_GTX_P3	E@0.1U_4 C174	PCIE_MRX_GTX_C_P3
PCIE_MRX_GTX_P4	E@0.1U_4 C152	PCIE_MRX_GTX_C_P4
PCIE_MRX_GTX_P5	E@0.1U_4 C176	PCIE_MRX_GTX_C_P5
PCIE_MRX_GTX_P6	E@0.1U_4 C154	PCIE_MRX_GTX_C_P6
PCIE_MRX_GTX_P7	E@0.1U_4 C162	PCIE_MRX_GTX_C_P7
PCIE_MRX_GTX_P8	E@0.1U_4 C140	PCIE_MRX_GTX_C_P8
PCIE_MRX_GTX_P9	E@0.1U_4 C164	PCIE_MRX_GTX_C_P9
PCIE_MRX_GTX_P10	E@0.1U_4 C142	PCIE_MRX_GTX_C_P10
PCIE_MRX_GTX_P11	E@0.1U_4 C166	PCIE_MRX_GTX_C_P11
PCIE_MRX_GTX_P12	E@0.1U_4 C144	PCIE_MRX_GTX_C_P12
PCIE_MRX_GTX_P13	E@0.1U_4 C168	PCIE_MRX_GTX_C_P13
PCIE_MRX_GTX_P14	E@0.1U_4 C146	PCIE_MRX_GTX_C_P14
PCIE_MRX_GTX_P15	E@0.1U_4 C170	PCIE_MRX_GTX_C_P15

U33A

PART 1 OF 4

PCIE_MTX_GRX_P0	AF1	PEX_RX0P	
PCIE_MTX_GRX_N0	AG2	PEX_RX0N	
PCIE_MTX_GRX_P1	AG3	PEX_RX1P	
PCIE_MTX_GRX_N1	AG4	PEX_RX1N	
PCIE_MTX_GRX_P2	AF4	PEX_RX2P	
PCIE_MTX_GRX_N2	AF5	PEX_RX2N	
PCIE_MTX_GRX_P3	AG6	PEX_RX3P	
PCIE_MTX_GRX_N3	AG7	PEX_RX3N	
PCIE_MTX_GRX_P4	AF7	PEX_RX4P	
PCIE_MTX_GRX_N4	AF8	PEX_RX4N	
PCIE_MTX_GRX_P5	AG9	PEX_RX5P	
PCIE_MTX_GRX_N5	AG10	PEX_RX5N	
PCIE_MTX_GRX_P6	AF10	PEX_RX6P	
PCIE_MTX_GRX_N6	AF11	PEX_RX6N	
PCIE_MTX_GRX_P7	AG12	PEX_RX7P	
PCIE_MTX_GRX_N7	AG13	PEX_RX7N	
PCIE_MTX_GRX_P8	AG15	PEX_RX8P	
PCIE_MTX_GRX_N8	AG16	PEX_RX8N	
PCIE_MTX_GRX_P9	AF16	PEX_RX9P	
PCIE_MTX_GRX_N9	AF17	PEX_RX9N	
PCIE_MTX_GRX_P10	AG18	PEX_RX10P	
PCIE_MTX_GRX_N10	AG19	PEX_RX10N	
PCIE_MTX_GRX_P11	AF19	PEX_RX11P	
PCIE_MTX_GRX_N11	AF20	PEX_RX11N	
PCIE_MTX_GRX_P12	AG21	PEX_RX12P	
PCIE_MTX_GRX_N12	AG22	PEX_RX12N	
PCIE_MTX_GRX_P13	AF22	PEX_RX13P	
PCIE_MTX_GRX_N13	AF23	PEX_RX13N	
PCIE_MTX_GRX_P14	AG24	PEX_RX14P	
PCIE_MTX_GRX_N14	AG25	PEX_RX14N	
PCIE_MTX_GRX_P15	AG26	PEX_RX15P	
PCIE_MTX_GRX_N15	AF27	PEX_RX15N	

PCI-EXPRESS INTERFACE

		PEX_TX0P	AD5 PCIE_MRX_GTX_C_P0
		PEX_TX0N	AD6 PCIE_MRX_GTX_C_N0
		PEX_TX1P	AE6 PCIE_MRX_GTX_C_P1
		PEX_TX1N	AE7 PCIE_MRX_GTX_C_N1
		PEX_TX2P	AD7 PCIE_MRX_GTX_C_P2
		PEX_TX2N	AC7 PCIE_MRX_GTX_C_N2
		PEX_TX3P	AE9 PCIE_MRX_GTX_C_P3
		PEX_TX3N	AE10 PCIE_MRX_GTX_C_N3
		PEX_TX4P	AD10 PCIE_MRX_GTX_C_P4
		PEX_TX4N	AC10 PCIE_MRX_GTX_C_N4
		PEX_TX5P	AE12 PCIE_MRX_GTX_C_P5
		PEX_TX5N	AE13 PCIE_MRX_GTX_C_N5
		PEX_TX6P	AD13 PCIE_MRX_GTX_C_P6
		PEX_TX6N	AC13 PCIE_MRX_GTX_C_N6
		PEX_TX7P	AC15 PCIE_MRX_GTX_C_P7
		PEX_TX7N	AD15 PCIE_MRX_GTX_C_N7
		PEX_TX8P	AE15 PCIE_MRX_GTX_C_P8
		PEX_TX8N	AE16 PCIE_MRX_GTX_C_N8
		PEX_TX9P	AC18 PCIE_MRX_GTX_C_P9
		PEX_TX9N	AD18 PCIE_MRX_GTX_C_N9
		PEX_TX10P	AE18 PCIE_MRX_GTX_C_P10
		PEX_TX10N	AE19 PCIE_MRX_GTX_C_N10
		PEX_TX11P	AC21 PCIE_MRX_GTX_C_P11
		PEX_TX11N	AD21 PCIE_MRX_GTX_C_N11
		PEX_TX12P	AE21 PCIE_MRX_GTX_C_P12
		PEX_TX12N	AE22 PCIE_MRX_GTX_C_N12
		PEX_TX13P	AD22 PCIE_MRX_GTX_C_P13
		PEX_TX13N	AD23 PCIE_MRX_GTX_C_N13
		PEX_TX14P	AE25 PCIE_MRX_GTX_C_P14
		PEX_TX14N	AE25 PCIE_MRX_GTX_C_N14
		PEX_TX15P	AE24 PCIE_MRX_GTX_C_P15
		PEX_TX15N	AD24 PCIE_MRX_GTX_C_N15

Clock

(3) CLK_PCIE_VGA	AE3	PEX_REFCLK
(3) CLK_PCIE_VGA#	AE4	PEX_REFCLK#

PEX_TSTCLK_OUT	AF13	PEX_TSTCLK
PEX_TSTCLK_OUT#	AF14	PEX_TSTCLK#
PEX_RST#	AC6	R_PLTRST_DELAY#

PCIE Power

	J9	VDD_01
	M9	VDD_02
G72_PLLVDD	N9	VDD_03
	R9	VDD_04
	T9	VDD_05
	J10	VDD_06
	J11	VDD_07
	M11	VDD_08
	N11	VDD_09
	R11	VDD_10
	T11	VDD_11
	L12	VDD_12
	M12	VDD_13
	T12	VDD_14
	U12	VDD_15
	L13	VDD_16
	M13	VDD_17
	T13	VDD_18
	U13	VDD_19
	W13	VDD_20
	M14	VDD_21
	T14	VDD_22
	L15	VDD_23
	M15	VDD_24
	T15	VDD_25
	U15	VDD_26
	W15	VDD_27
	L16	VDD_28
	M16	VDD_29
	T16	VDD_30
	U16	VDD_31
	W16	VDD_32
	M17	VDD_33
	N17	VDD_34
	R17	VDD_35
	T17	VDD_36
PEX_PLL_AVDD	Y6	PEX_PLLAVDD
PEX_PLL_DVDD	AA5	PEX_PLLDVDD
	AA6	PEX_PLLGND

	AB10	PEX_IOVDD_01
	AB11	PEX_IOVDD_02
	AB14	PEX_IOVDD_03
	AB15	PEX_IOVDD_04
	W17	PEX_IOVDD_05
	W18	PEX_IOVDD_06
	AB20	PEX_IOVDD_07
	AB21	PEX_IOVDD_08
	AA4	PEX_IOVDDQ_01
	AB5	PEX_IOVDDQ_02
	AB6	PEX_IOVDDQ_03
	AB7	PEX_IOVDDQ_04
	AB8	PEX_IOVDDQ_05
	AB9	PEX_IOVDDQ_06
	AC9	PEX_IOVDDQ_07
	AC11	PEX_IOVDDQ_08
	AB12	PEX_IOVDDQ_09
	AC12	PEX_IOVDDQ_10
	AB13	PEX_IOVDDQ_11
	AB16	PEX_IOVDDQ_12
	AC16	PEX_IOVDDQ_13
	AB17	PEX_IOVDDQ_14
	AC17	PEX_IOVDDQ_15
	AB18	PEX_IOVDDQ_16
	AB19	PEX_IOVDDQ_17
	AC19	PEX_IOVDDQ_18
	AC20	PEX_IOVDDQ_19
	W9	VDD_LP_01
	W10	VDD_LP_02
	W11	VDD_LP_03
	W12	VDD_LP_04
	J12	VDD33_01
	F13	VDD33_02
	J13	VDD33_03
	F14	VDD33_04
	J15	VDD33_05
	J16	VDD33_06
	D12	NC_01
	E12	NC_02
	E12	NC_03
	C13	NC_04

G72M

(7) PCIE_MRX_GTX_N[0..15]

PCIE_MRX_GTX_N0	E@0.1U_4 C149	PCIE_MRX_GTX_C_N0
PCIE_MRX_GTX_N1	E@0.1U_4 C173	PCIE_MRX_GTX_C_N1
PCIE_MRX_GTX_N2	E@0.1U_4 C151	PCIE_MRX_GTX_C_N2
PCIE_MRX_GTX_N3	E@0.1U_4 C175	PCIE_MRX_GTX_C_N3
PCIE_MRX_GTX_N4	E@0.1U_4 C153	PCIE_MRX_GTX_C_N4
PCIE_MRX_GTX_N5	E@0.1U_4 C177	PCIE_MRX_GTX_C_N5
PCIE_MRX_GTX_N6	E@0.1U_4 C155	PCIE_MRX_GTX_C_N6
PCIE_MRX_GTX_N7	E@0.1U_4 C163	PCIE_MRX_GTX_C_N7
PCIE_MRX_GTX_N8	E@0.1U_4 C141	PCIE_MRX_GTX_C_N8
PCIE_MRX_GTX_N9	E@0.1U_4 C165	PCIE_MRX_GTX_C_N9
PCIE_MRX_GTX_N10	E@0.1U_4 C143	PCIE_MRX_GTX_C_N10
PCIE_MRX_GTX_N11	E@0.1U_4 C167	PCIE_MRX_GTX_C_N11
PCIE_MRX_GTX_N12	E@0.1U_4 C145	PCIE_MRX_GTX_C_N12
PCIE_MRX_GTX_N13	E@0.1U_4 C169	PCIE_MRX_GTX_C_N13
PCIE_MRX_GTX_N14	E@0.1U_4 C147	PCIE_MRX_GTX_C_N14
PCIE_MRX_GTX_N15	E@0.1U_4 C171	PCIE_MRX_GTX_C_N15

+3VRUN
U31
E@TC7SH08FU
C482 E@0.1U
PLTRST# (13,14,26,27,32)
R_PLTRST_DELAY#
R349 *E@0_4

LE4 B:
del U31, C482 in BOM

+1.22V_GFX_PCIE
L15 E@BLM11A121S_6
G72_PLLVDD
C120
C61 E@0.1U_4
E@4.7U_6.3V_6

R387 *E@200_4
R59 *E@0
PLTRST_DELAY# (14)

LE4 B:
del R387,R59 in BOM

+VCC_GFX_CORE
C40 E@100P_4
C45 E@0.01U_4
C58 E@0.01U_4
C42 E@100P_4
C96 E@0.01U_4
C56 E@220P_4
C71 E@100P_4
C84 E@220P_4
C95 E@100P_4
C68 E@1U_6.3V_4
C101 E@220P_4
C66 E@0.01U_4
C87 E@220P_4
C86 E@220P_4
C99 E@10U_6.3V_6
C60 E@10U_6.3V_6
C83 E@10U_6.3V_6
PLACE NEAR BALLS

+1.22V_GFX_PCIE
C106 E@0.1U_4
C121 E@0.022U_4
C118 E@0.022U_4
C114 E@0.022U_4
PLACE NEAR BALLS
C112 E@10U_6.3V_6
C122 E@1U_6.3V_4
C510 E@4.7U_6.3V_6
PLACE NEAR GPU

+1.22V_GFX_PCIE
C111 E@10U_6.3V_6
C117 E@0.022U_4
C116 E@0.1U_4
C108 E@0.1U_4
C123 E@1U_6.3V_4
C508 E@4.7U_6.3V_6
PLACE NEAR BALLS

+1.22V_GFX_PCIE
L44 E@BLM11A121S_6
C504 E@4.7U_6.3V_6
C501 E@1U_6.3V_4
C503 E@1U_6.3V_4
C107 E@0.1U_4
C97 E@0.01U_4

+VCC_GFX_CORE
C74 E@220P_4
C85 E@0.01U_4
C65 E@0.1U_4
+3VRUN
C39 E@0.1U_4
C54 E@4700P_4
C31 E@0.022U_4
C43 E@1U_6.3V_4
PLACE NEAR BALLS

LE4 B:
Update correct power plane

+1.22V_GFX_PCIE
C100 330U/2.5V-12m
+VCC_GFX_CORE
C17 330U/2.5V-12m
Place near VGA chipset

LE4 A:

PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	VGA G72M (PCIe POWER)	1A
Date: Tuesday, March 14, 2006	Sheet 18 of 42	

LE4 B:
Cancel R355,R367 in BOM

LE4 B:
Cancel parts in BOM

LE4 B:
Cancel parts in BOM

LE4 B:
Cancel parts in BOM

	CFG3	CFG2	CFG1	CFG0
128MB(16M*16)	0	0	1	0
	DEV3	DEV2	DEV1	DEV0
G72M	1	0	0	0

LE4 B:
Update correct power plane

LE4 B:
Cancel R21 in BOM

LE4 B:
Update correct power plane

LE4 B:
Del R361, C481 in BOM

LE4 B:
Cancel R57 in BOM

LE4 B:
Cancel R362 in BOM

LE4 C:
Add U46,R599,C711

Thermal Sensor for Graphic

SLAVE ADDRESS: 9A

LE4 B:
Del R13, R14 in BOM

LE4 C:

B:Change U9 from G781-1 to MAX6649 for thermal issue

D:Change U9 footprint from SOIC8 to MSOP8

Place close to VGA Chip

PROJECT :	LE4
Quanta Computer Inc.	
Size:	Document Number: VGA-G72M (VIDEO) Rev: 1A
Date:	Tuesday, March 14, 2006 Sheet 19 of 42

FB_CMD[0..26] (21)
FBD[0..63] (21)
FBDQM[0..7] (21)
FBDQS[0..7] (21)
FBDQS#[0..7] (21)

U33C

Part 3 of 4

MEMORY INTERFACE

FBD0	A26	FB_DQ0	FB_CMD0	G27	FB_CMD0
FBD1	C24	FB_DQ1	FB_CMD1	D25	FB_CMD1
FBD2	B24	FB_DQ2	FB_CMD2	F26	FB_CMD2
FBD3	A24	FB_DQ3	FB_CMD3	F25	FB_CMD3
FBD4	C22	FB_DQ4	FB_CMD4	G25	FB_CMD4
FBD5	A25	FB_DQ5	FB_CMD5	J25	FB_CMD5
FBD6	B25	FB_DQ6	FB_CMD6	J27	FB_CMD6
FBD7	D23	FB_DQ7	FB_CMD7	M26	FB_CMD7
FBD8	G22	FB_DQ8	FB_CMD8	C27	FB_CMD8
FBD9	J23	FB_DQ9	FB_CMD9	C25	FB_CMD9
FBD10	E24	FB_DQ10	FB_CMD10	D24	FB_CMD10
FBD11	F23	FB_DQ11	FB_CMD11	N27	FB_CMD11
FBD12	J24	FB_DQ12	FB_CMD12	G24	FB_CMD12
FBD13	F24	FB_DQ13	FB_CMD13	J26	FB_CMD13
FBD14	G23	FB_DQ14	FB_CMD14	M27	FB_CMD14
FBD15	H24	FB_DQ15	FB_CMD15	C26	FB_CMD15
FBD16	D16	FB_DQ16	FB_CMD16	M25	FB_CMD16
FBD17	E16	FB_DQ17	FB_CMD17	D26	FB_CMD17
FBD18	D17	FB_DQ18	FB_CMD18	D27	FB_CMD18
FBD19	F18	FB_DQ19	FB_CMD19	K26	FB_CMD19
FBD20	E19	FB_DQ20	FB_CMD20	K25	FB_CMD20
FBD21	E18	FB_DQ21	FB_CMD21	K24	FB_CMD21
FBD22	D20	FB_DQ22	FB_CMD22	F27	FB_CMD22
FBD23	D19	FB_DQ23	FB_CMD23	K27	FB_CMD23
FBD24	A18	FB_DQ24	FB_CMD24	G26	FB_CMD24
FBD25	B18	FB_DQ25	FB_CMD25	B27	FB_CMD25
FBD26	A19	FB_DQ26	FB_CMD26	N24	FB_CMD26
FBD27	B19	FB_DQ27			
FBD28	D18	FB_DQ28			
FBD29	C19	FB_DQ29			
FBD30	C16	FB_DQ30	FB_DQM0	D21	FBDQM0
FBD31	C18	FB_DQ31	FB_DQM1	F22	FBDQM1
FBD32	N26	FB_DQ32	FB_DQM2	F20	FBDQM2
FBD33	N25	FB_DQ33	FB_DQM3	A21	FBDQM3
FBD34	R25	FB_DQ34	FB_DQM4	V27	FBDQM4
FBD35	R26	FB_DQ35	FB_DQM5	W22	FBDQM5
FBD36	R27	FB_DQ36	FB_DQM6	V22	FBDQM6
FBD37	T25	FB_DQ37	FB_DQM7	V24	FBDQM7
FBD38	T27	FB_DQ38			
FBD39	T26	FB_DQ39	FB_DQS_RN0	A22	FBDQS#0
FBD40	AB23	FB_DQ40	FB_DQS_RN1	E22	FBDQS#1
FBD41	Y24	FB_DQ41	FB_DQS_RN2	F21	FBDQS#2
FBD42	AB24	FB_DQ42	FB_DQS_RN3	B21	FBDQS#3
FBD43	AB22	FB_DQ43	FB_DQS_RN4	V26	FBDQS#4
FBD44	AC24	FB_DQ44	FB_DQS_RN5	W23	FBDQS#5
FBD45	AC22	FB_DQ45	FB_DQS_RN6	V23	FBDQS#6
FBD46	AA23	FB_DQ46	FB_DQS_RN7	W27	FBDQS#7
FBD47	AA22	FB_DQ47			
FBD48	T24	FB_DQ48	FB_DQS_WP0	B22	FBDQS0
FBD49	T23	FB_DQ49	FB_DQS_WP1	D22	FBDQS1
FBD50	R24	FB_DQ50	FB_DQS_WP2	E21	FBDQS2
FBD51	R23	FB_DQ51	FB_DQS_WP3	C21	FBDQS3
FBD52	R22	FB_DQ52	FB_DQS_WP4	V25	FBDQS4
FBD53	T22	FB_DQ53	FB_DQS_WP5	W24	FBDQS5
FBD54	N23	FB_DQ54	FB_DQS_WP6	U24	FBDQS6
FBD55	P24	FB_DQ55	FB_DQS_WP7	W26	FBDQS7
FBD56	AA24	FB_DQ56			
FBD57	AA27	FB_DQ57			
FBD58	AA26	FB_DQ58			
FBD59	AB25	FB_DQ59			
FBD60	AB26	FB_DQ60			
FBD61	AB27	FB_DQ61			
FBD62	AA25	FB_DQ62			
FBD63	W25	FB_DQ63			

read strobe

write strobe

FBVTT_01	E15	FBVDDQ_01	F17
FBVTT_02	F15	FBVDDQ_02	F19
FBVTT_03	F16	FBVDDQ_03	J19
FBVTT_04	J17	FBVDDQ_04	M19
FBVTT_05	J18	FBVDDQ_05	T19
FBVTT_06	L19	FBVDDQ_06	J22
FBVTT_07	N19	FBVDDQ_07	L22
FBVTT_08	R19	FBVDDQ_08	P22
FBVTT_09	U19	FBVDDQ_09	U22
FBVTT_10	W19	FBVDDQ_10	Y22

(21) FB_CLK0	L24	FB_CLK0	
(21) FB_CLK0#	K23	FB_CLK0#	
(21) FB_CLK1	M22	FB_CLK1	
(21) FB_CLK1#	N22	FB_CLK1#	
	M23	FB_REFCLK	
	M24	FB_REFCLK#	
T4	FB_DEBUG	K22	FB_DEBUG
	FBVREF	A16	FB_VREF
+3VRUN	FBA_PLLVDD	D14	FB_PLLVDD
+1.22V_GFX_PCIE	FB_PLLAVDD	D13	FB_PLLAVDD
		C15	FB_PLLAGND
FBCAL_PD_VDDQ	D15	FBCAL_PD_VDDQ	
FBCAL_PU_GND	E13	FBCAL_PU_GND	
FBCAL_TERM_GND	H22	FBCAL_TERM_GND	

G72M

T6

T5

+1.8VRUN

R34 E@40.2/F_4

R40 E@0_4

R32 E@30/F_4

LE4 B: del R40 in BOM

LE4 B: del L5 in BOM

L5 *E@BLM11A121S_6

L7 E@BLM11A121S_6

C21 E@4.7U_6.3V_6

C23 E@1U_6.3V_4

C26 E@0.01U_4

U33D

Part 4 of 4

GND

B2	GND_01	GND_48	P14
E2	GND_02	GND_49	R14
H2	GND_03	GND_50	U14
L2	GND_04	GND_51	W14
P2	GND_05	GND_52	AC14
U2	GND_06	GND_53	AD14
Y2	GND_07	GND_54	N15
AC2	GND_08	GND_55	P15
AE2	GND_09	GND_56	R15
AF3	GND_10	GND_57	AF15
B5	GND_11	GND_58	N16
E5	GND_12	GND_59	P16
L5	GND_13	GND_60	R16
P5	GND_14	GND_61	AD16
U5	GND_15	GND_62	B17
Y5	GND_16	GND_63	E17
AC5	GND_17	GND_64	L17
H6	GND_18	GND_65	P17
AF6	GND_19	GND_66	U17
B8	GND_20	GND_67	AD17
E8	GND_21	GND_68	AF18
AD8	GND_22	GND_69	K19
K9	GND_23	GND_70	P19
P9	GND_24	GND_71	V19
V9	GND_25	GND_72	AD19
AD9	GND_26	GND_73	B20
AF9	GND_27	GND_74	E20
B11	GND_28	GND_75	AD20
E11	GND_29	GND_76	AF21
F11	GND_30	GND_77	B23
L11	GND_31	GND_78	E23
P11	GND_32	GND_79	H23
U11	GND_33	GND_80	L23
AD11	GND_34	GND_81	P23
N12	GND_35	GND_82	U23
P12	GND_36	GND_83	Y23
R12	GND_37	GND_84	AC23
AD12	GND_38	GND_85	AF24
AF12	GND_39	GND_86	B26
N13	GND_40	GND_87	E26
P13	GND_41	GND_88	H26
R13	GND_42	GND_89	L26
B14	GND_43	GND_90	P26
E14	GND_44	GND_91	U26
J14	GND_45	GND_92	Y26
L14	GND_46	GND_93	AC26
N14	GND_47	GND_94	AF26

G72M

PLACE BELOW GPU

+1.8VRUN

C104 E@4700P_4
C103 E@0.022U_4
C15 E@0.1U_4
C14 E@4700P_4
C160 E@0.1U_4
C93 E@4.7U_6.3V_6
C161 E@1U_6.3V_4

C47 E@4700P_4
C48 E@0.022U_4
C63 E@0.1U_4
C62 E@4700P_4
C76 E@0.022U_4
C77 E@0.1U_4
C88 E@4.7U_6.3V_6

C44 E@4700P_4
C35 E@0.022U_4
C36 E@0.1U_4
C50 E@0.022U_4
C37 E@0.1U_4
C82 E@1U_6.3V_4

+1.8VRUN

C16 330U/2.5V-12m

LE4 A:
Place near VGA chipset

R365 E@1K/F_4

R364 E@1K/F_4

C489 E@0.1U_4

FBVREF

FBVREF = FBVDDQ * Rb/(Rt + Rb).
VREF = 0.5 * FBVDDQ.
DDR: 0.9V = 1.8V * 1K/(1K + 1K).

PROJECT : LE4			
Quanta Computer Inc.			
Size	Document Number		Rev
	VGA-G72M (MENORY, GND)		1A
Date: Tuesday, March 14, 2006	Sheet 20	of 42	

FB_CMD[0..26] (20)
FBD[0..63] (20)
FBDQM[0..7] (20)
FBDQS[0..7] (20)
FBDQS#[0..7] (20)

R48 E@10K_4 FB_CMD12
R384 E@10K_4 FB_CMD11
R358 E@120_4 FB_CLK0 FB_CLK0#
R52 E@120_4 FB_CLK1 FB_CLK1#

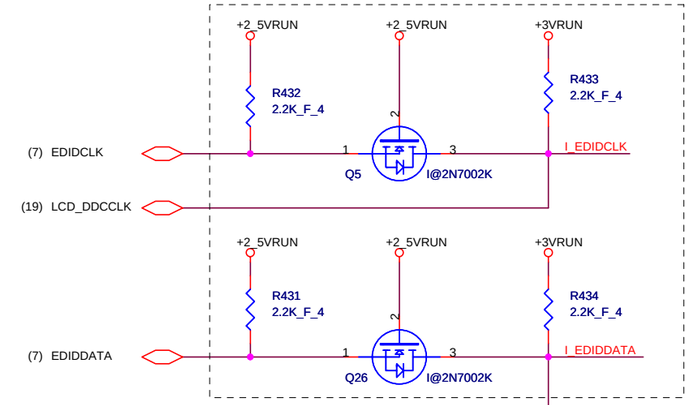
U32 VRAM
U4 VRAM
U7 VRAM
U34 VRAM

R47 E@1K/F_4
R383 E@1K/F_4
C81 E@0.1U_P_4
R50 E@1K/F_4
R385 E@1K/F_4
C91 E@0.1U_P_4

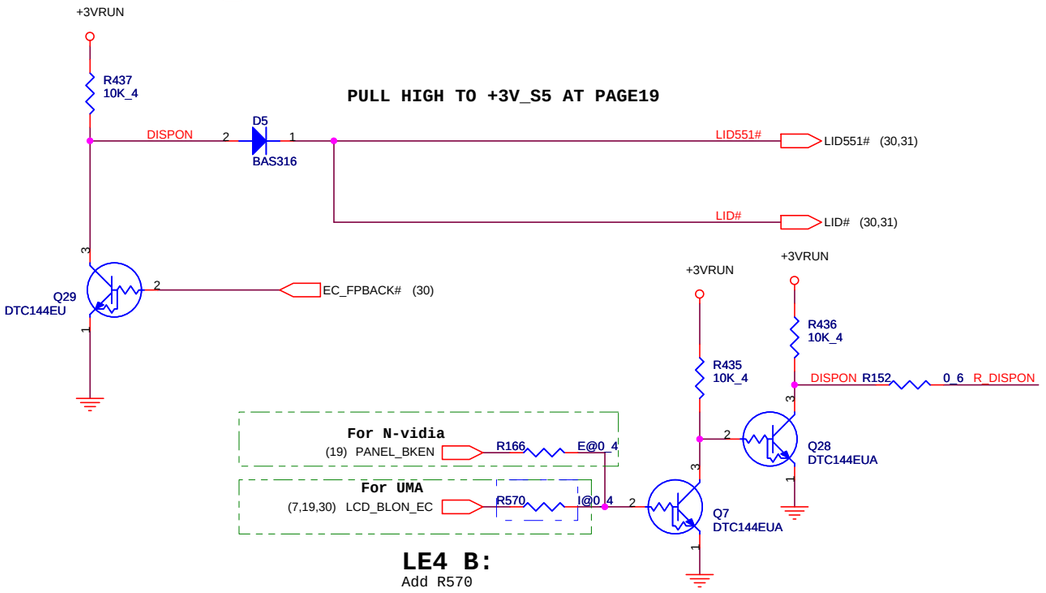
C485 C494 E@0.1U_4 C493 E@0.01U_4 E@4.7U_6.3V_6
C483 E@0.1U_4 C492 E@0.1U_4 C484 E@0.01U_4 E@0.1U_10V_4
C8 C79 E@0.1U_4 C9 E@0.01U_4 E@4.7U_6.3V_6
C10 E@0.1U_4 C80 E@0.1U_4 C78 E@0.01U_4
C496 C41 E@0.1U_4 C486 E@0.01U_4 E@4.7U_6.3V_6
C90 E@0.1U_4 C92 E@0.1U_4 C89 E@0.01U_4
C495 C498 E@0.1U_4 C11 E@0.01U_4 E@4.7U_6.3V_6
C499 E@0.1U_4 C49 E@0.1U_4 C497 E@0.01U_4

PROJECT : LE4
Quanta Computer Inc.

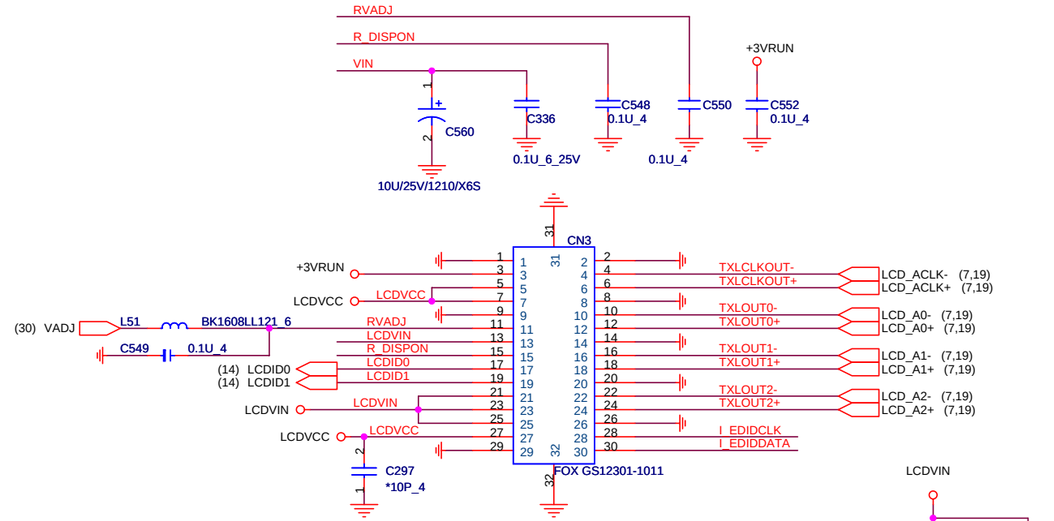
Size	Document Number	Rev
	VGA-G72M (VRAM)	1A
Date: Tuesday, March 14, 2006	Sheet 21 of 42	



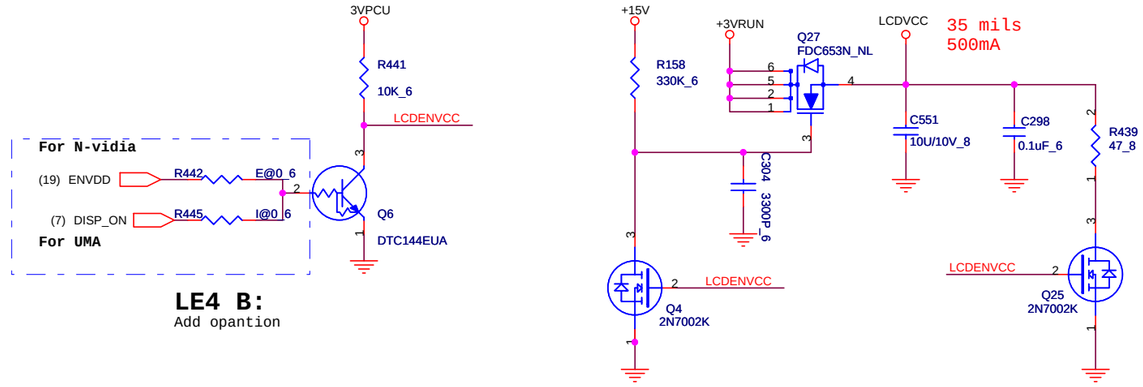
ADD LEVEL SHIFT FOR EDID



LE4 B:
Add R570

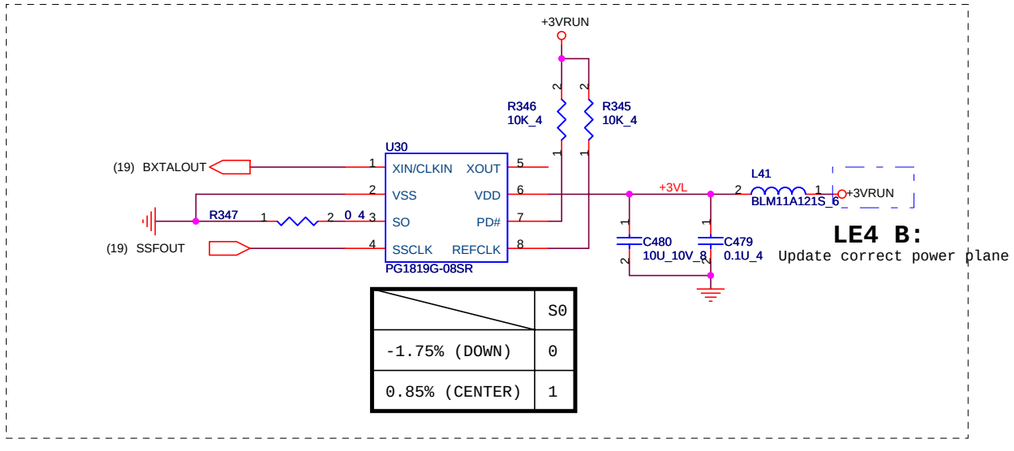


LCD CONNECTOR



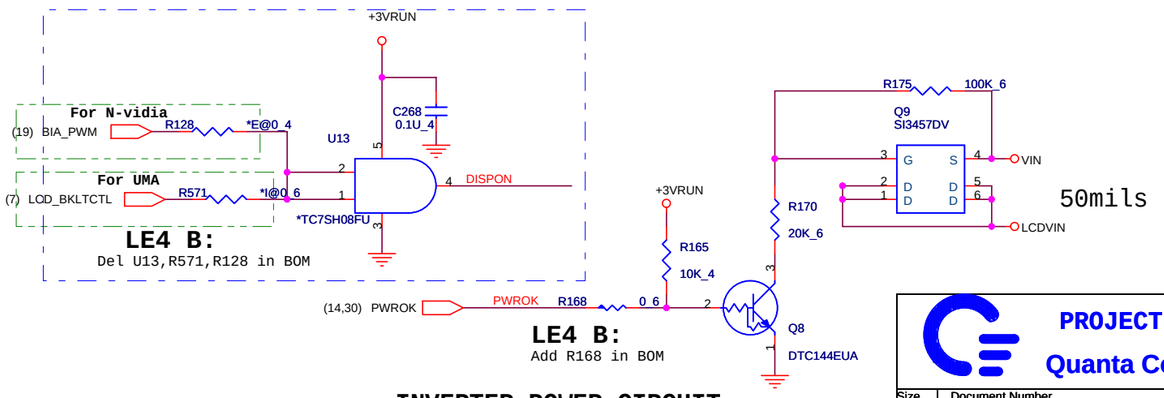
LE4 B:
Add opantion

LCD VCC



LE4 B:
Update correct power plane

	S0
-1.75% (DOWN)	0
0.85% (CENTER)	1



LE4 B:
Del U13,R571,R128 in BOM

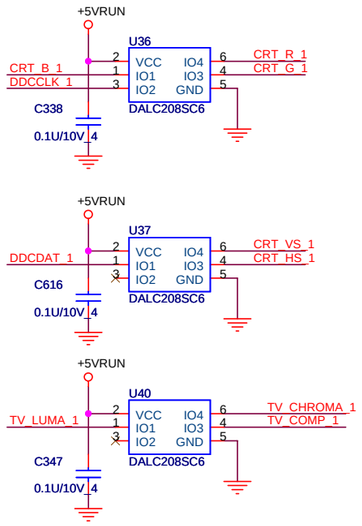
LE4 B:
Add R168 in BOM

INVERTER POWER CIRCUIT

PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	LCD CON. & LCD POWER	1A
Date: Tuesday, March 14, 2006	Sheet 22 of 42	

ESD PORTECTION

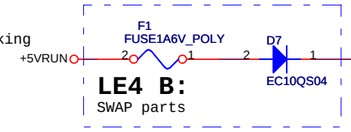


LE4 C:

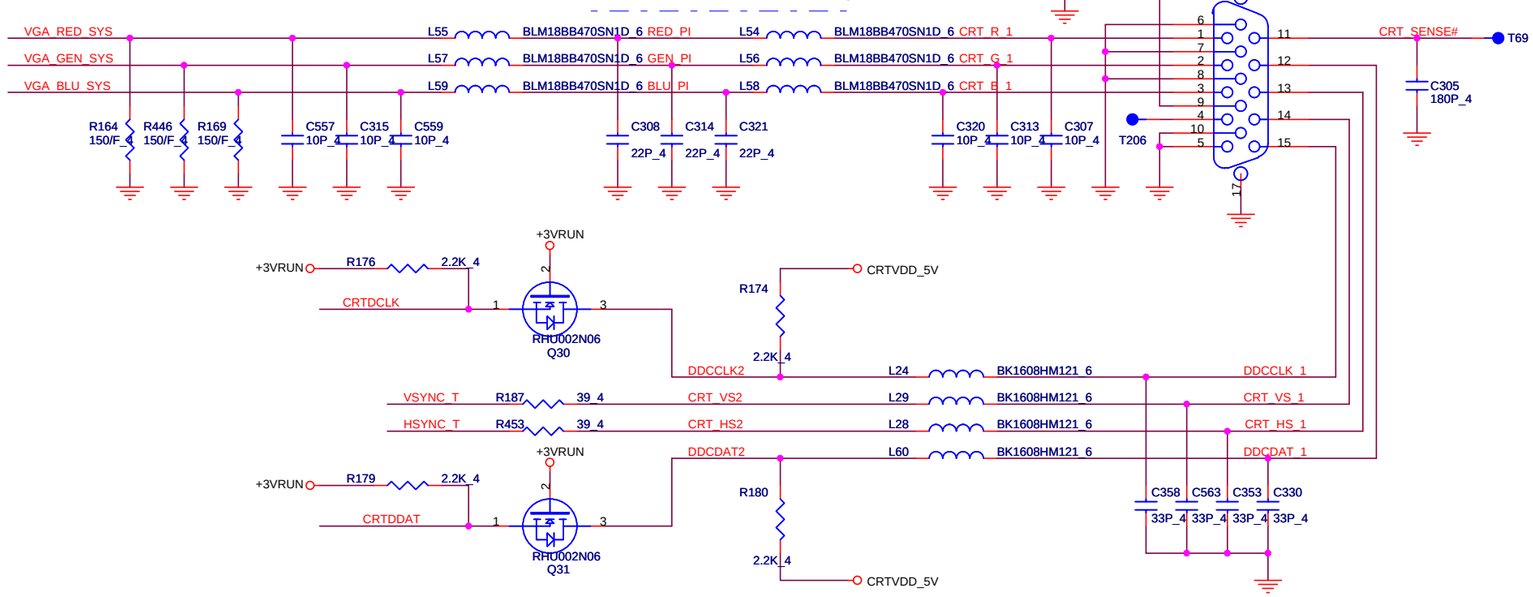
Change D7 packing

LE4 B:

SWAP parts



CRT PORT



TV-OUT

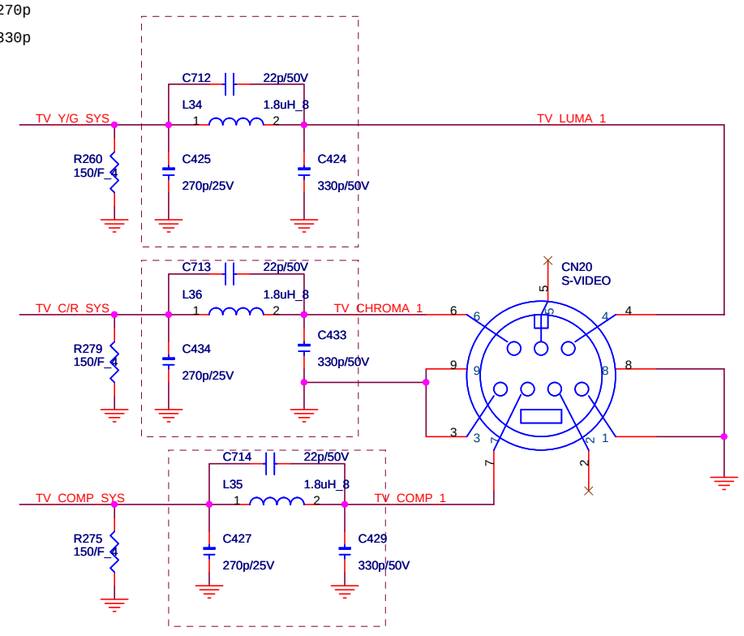
LE4 C:

Change C425,C434 and C427 from 6p to 270p

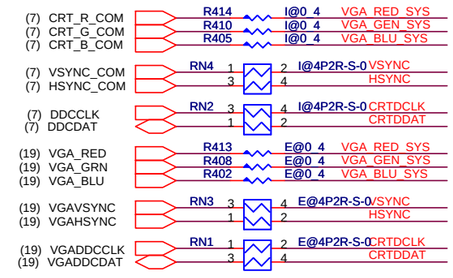
Change C424,C433 and C429 from 6p to 330p

ChangeL35 size from 0603 to 0805

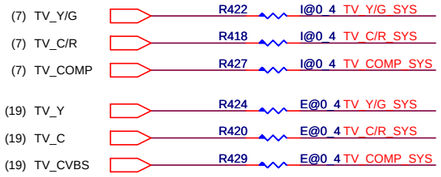
Add C712 ,C713 and C714

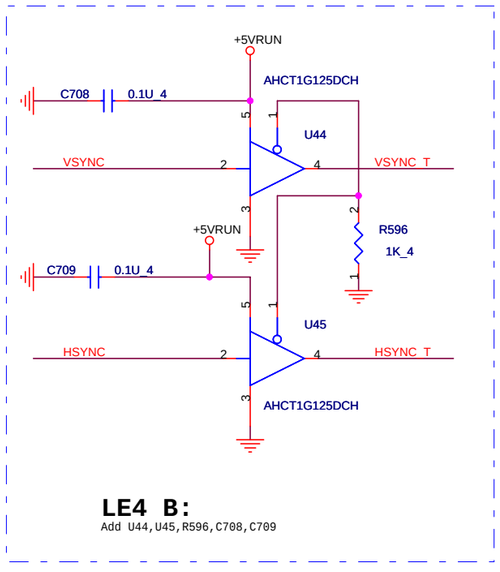


(7) CRT_R_COM
(7) CRT_G_COM
(7) CRT_B_COM
(7) VSYNC_COM
(7) HSYNC_COM
(7) DDCCLK
(7) DDCDAT
(19) VGA_RED
(19) VGA_GRN
(19) VGA_BLU
(19) VGAVSYNC
(19) VGAHSYNC
(19) VGADDCCLK
(19) VGADDCDAT



(7) TV_Y/G
(7) TV_C/R
(7) TV_COMP
(19) TV_Y
(19) TV_C
(19) TV_CVBS





LE4 B:

Add U44,U45,R596,C708,C709

Intel CRB

150 ohm@ 100MHZ
(100mA)

6pf 16V 6pf 16V

CX8PG181001 (180 ohm ,1.5A)

CH00606TB04 CH00606TB04

PROJECT : LE4

Quanta Computer Inc.

Size	Document Number	Rev
	CRT & TV-OUT CONN	1A
Date: Tuesday, March 14, 2006	Sheet 23 of 42	

LE4 B:
SAWP GNT2# AND REQ2#

U22A

(13) GNT2# — GNT2# — L2 — GNT#
(13) ~~REQ2#~~ — REQ2# — L3 — REQ#
AD25 R280 150_4 — N5 — IDSEL
(13,33) FRAME# — FRAME# — R6 — FRAME#
(13,33) IRDY# — IRDY# — V5 — IRDY#
(13,33) DEVSEL# — DEVSEL# — U6 — DEVSEL#
(13,33) TRDY# — TRDY# — W5 — TRDY#
(13,33) SERR# — SERR# — W6 — SERR#
(13,33) STOP# — STOP# — V6 — STOP#
(13,33) PERR# — PERR# — R7 — PERR#
(13,33) PAR — PAR — U7 — PAR

(13,33) C/BE3# — P2 — CBE3
(13,33) C/BE2# — U5 — CBE2
(13,33) C/BE1# — V7 — CBE1
(13,33) C/BE0# — C/BE0# — W10 — CBE0

(3) PCLK_PCM — PCLK_PCM — L1 — PCLK

(13,25,33) PCIRST# — PCIRST# — K3 — PRST#
GRST# — K5 — GRST#

(13,33) AD[0..31] — AD0 R11 — AD00
AD1 P11 — AD01
AD2 U11 — AD02
AD3 V11 — AD03
AD4 W11 — AD04
AD5 R10 — AD05
AD6 U10 — AD06
AD7 V10 — AD07
AD8 R9 — AD08
AD9 U9 — AD09
AD10 V9 — AD10
AD11 W9 — AD11
AD12 V8 — AD12
AD13 U8 — AD13
AD14 R8 — AD14
AD15 W7 — AD15
AD16 W4 — AD16
AD17 T2 — AD17
AD18 T1 — AD18
AD19 R3 — AD19
AD20 P5 — AD20
AD21 R2 — AD21
AD22 R1 — AD22
AD23 P3 — AD23
AD24 N3 — AD24
AD25 N2 — AD25
AD26 N1 — AD26
AD27 M5 — AD27
AD28 M6 — AD28
AD29 M3 — AD29
AD30 M2 — AD30
AD31 M1 — AD31

PCI7412

PCI Interface

1394 Interface

Miscellaneous

PN

1394_XIN — C391 12P-50V_4
Y3 FW@24.576MHZ B6624576473
1394_XOUT — C389 12P-50V_4

XI — R19
XO — R18

R0 — T18 — R0 R205 FW@6.34K/F_4
R1 — T19 — R1
CPS — R12 — CPS R237 FW@0_4
TEST0 — P12 — R241 FW@0_4
VSSPLL — R17

LE4 C:
Change R237 and R241 from 390K and 330 to 0 ohm

TPA0P — V14 — TPA0P
TPA0N — W14 — TPA0N
TPBIAS0 — R13 — TPBIAS0
TPB0P — V13 — TPB0P
TPB0N — W13 — TPB0N

TPA1P — V16 — 1394_TPA1+ — T91
TPA1N — W16 — 1394_TPA1- — T90
TPBIAS1 — W17 — TPBIAS1 — T89
TPB1P — V15 — 1394_TPB1+ — T93
TPB1N — W15 — 1394_TPB1- — T95

VDDPLL15 — P15
PHY_TEST_MA — P17 — R219 1394_AVDD FW@4.7K_4
C394 1U-16V_6

PC0_RSVD — U12
PC1_RSVD — V12
PC2_RSVD — W12

3VSUS
AGND_00 — U13
AGND_01 — U14
AGND_02 — R14
R283 10K_4

SUSPEND# — J5
RI_OUT# — L5 — R281 0_4 — PCMSPK — PCI_PME# (13,33)
SPKROUT — H3 — R282 *0_4 — PCMSPK (28)
RI# (14,26)
VR_EN# — K2
USB_EN — E10

D2 *1SS355_NC
SUS_STAT# (14,26,27)

SCL — G2 — SCL_CARD
SDA — G3 — SDA_CARD

MFUNC0 — G1 — INTC# — INTC# (13)
MFUNC1 — H5 — INTD# — INTD# (13)
MFUNC2 — H2 — INTE# — INTE# (13)
MFUNC3 — H1 — SERIRQ (14,26,27,30)
MFUNC4 — J1 — R284 10K_4 — 3VSUS
MFUNC5 — J2 — T111
MFUNC6 — J3 — CLKRUN# (14,26,27,30,33)

LATCH/VD3/VPPD0 — C9 — R249 0_4 — TPS_LATCH (25)
CLOCK/VD1/VCCD0# — A9 — R245 0_4 — TPS_CLOCK (25)
DATA/VD2/VPPD1 — B9 — R240 0_4 — TPS_DATA (25)
RSVD_03/VD0/VCCD1#/PS_MODE — C4 — R278 10K_4 — 3VSUS
LE4 A-1108;

LE4 C:
Add C?, solve 1394 hang up and busy on system.

LE4 B:

TPBIAS0 — C715 270P-25V_4
R38 FW@56.2/F_4
R39 FW@56.2/F_4
C34 1U-16V_6

TPA0P — R24 FW@0_4 — L1394_TPA0+
TPA0N — R23 FW@0_4 — L1394_TPA0-
TPB0P — L1394_TPB0+
TPB0N — L1394_TPB0-
R37 FW@56.2/F_4
R36 FW@56.2/F_4
R26 0_4 — L1394_TPA0+
R25 0_4 — L1394_TPA0-
R42 FW@5.1K/F_6
C28 270P-25V_4

No Struff

L9 *PLW3216S900SQ2T1 <PN>
TPA0P — 2 — L1394_TPA0+
TPA0N — 3 — L1394_TPA0-

L10 *PLW3216S900SQ2T1 <PN>
TPB0P — 3 — L1394_TPB0+
TPB0N — 2 — L1394_TPB0-

J1
L1394_TPB0- — 1
L1394_TPA0- — 3
L1394_TPA0+ — 4
L1394_TPB0+ — 2
5
6
FOX_UV31413-K1

LE4 B:

1394_TPA1+
1394_TPA1-
TPBIAS1
1394_TPB1+
1394_TPB1-
PCMSPK

R600 0_4
R601 0_4
R602 0_4
R603 0_4
R604 47K_4
C716 1U-16V_6

LE4 C:
Solve to hang up and busy on system

3VSUS
R286 100K_4
GRST# — C436 0.22U/10V_4

LE4 C:
Modify PCIRST# circuit method

D3 *1SS355_NC — GRST# — GRST#_7402 (30)
D18 *1SS355_NC — PCIRST# — R285 *0_4

LE4 B:
Add L71

3VSUS
R261 2.2K_4
R264 2.2K_4
R262 *220_4
R263 *220_4
SCL_CARD
SDA_CARD
U24 24LC02BT
VCC A0 NC A1 SCL A3 SDA GND
C422 0.1U-10V_4

1394_AVDD
L71 FW@BK1608HS800_6
L32 FW@BK1608HS800_6
C398 0.1U-10V_4
C392 1U-16V_6

PCLK_PCM
R290 *33_4
C440 *10P_4

PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	PC7412 - IEEE1394	1A
Date: Tuesday, March 14, 2006	Sheet 24 of 42	

DO NOT INSERT SD/MMC, MEMORYSTICK AND XD SIMULTANEOUSLY.

3 IN1 CARD READER (push-push)

FlashMedia Interface

U22C

SC_OC# F2
SC_PWR_CTRL G5
SC_VCC5 G6
SD_CMD/SM_ALE/SC_GPIO2 C5
SD_CLK/SM_RE#/SC_GPIO1 A4
SM_CLE/SC_GPIO0 B4
SM_R/B#/SC_RFU D1
SM_PHYS_WP#/SC_FCB E3
SC_CLK E2
SC_RST F5
SC_DATA E1

CLK_48 F1 — TI_CLK48M — TI_CLK48M (3)

SC_CD# E3
SD_CD# E9 — SD_CDZ
MS_CD# A8 — MS_CDZ
SM_CD# B8

XD_CD#/SM_PHYS_WP# A3

MC_PWR_CTRL_0 C8 — MC_PWR_CTRL_0#
MC_PWR_CTRL_1/SM_R/B# E8 — SM_R/B# — R266 CR@10K_4 — VCC_FM
MS_BS/SD_CMD/SM_WE# E8 — MS_BS_SD_CMD_SM_WEZ — R271 CR@10K_4 — VCC_FM
MS_CLK/SD_CLK/SM_EL_WP# A7 — MS_CLK_SD_CLK_SM_ELWPZ_R — R254 47_6 — MS_CLK_SD_CLK_SM_ELWPZ

MS_SDIO(DATA0)/SD_DATA0/SM_D0 B7 — MS_DATA0_SD_DAT0_SM_D0
MS_DATA1/SD_DATA1_SM_D1 C7 — MS_DATA1_SD_DAT1_SM_D1
MS_DATA2/SD_DATA2_SM_D2 A6 — MS_DATA2_SD_DAT2_SM_D2
MS_DATA3/SD_DATA3_SM_D3 B6 — MS_DATA3_SD_DAT3_SM_D3

SD_WP/SM_CE# E7 — SD_WP_SM_CEZ — R277 CR@10K_4 — VCC_FM

SD_DAT0/SM_D4/SC_GPIO6 C6
SD_DAT1/SM_D5/SC_GPIO5 A5
SD_DAT2/SM_D6/SC_GPIO4 B5
SD_DAT3/SM_D7/SC_GPIO3 E6

PCI7412

CardBus Interface

U22B

CAD31 C10 A_CAD31
CAD30 A10 A_CAD30
CAD29 F11 A_CAD29
CAD28 E11 A_CAD28
CAD27 C11 A_CAD27
CAD26 B13 A_CAD26
CAD25 C13 A_CAD25
CAD24 A14 A_CAD24
CAD23 B14 A_CAD23
CAD22 B15 A_CAD22
CAD21 E14 A_CAD21
CAD20 A16 A_CAD20
CAD19 D19 A_CAD19
CAD18 E17 A_CAD18
CAD17 F15 A_CAD17
CAD16 H19 A_CAD16
CAD15 J17 A_CAD15
CAD14 J15 A_CAD14
CAD13 J18 A_CAD13
CAD12 K15 A_CAD12
CAD11 K17 A_CAD11
CAD10 K18 A_CAD10
CAD09 L15 A_CAD9
CAD08 L18 A_CAD8
CAD07 L19 A_CAD7
CAD06 M17 A_CAD6
CAD05 M18 A_CAD5
CAD04 N19 A_CAD4
CAD03 M15 A_CAD3
CAD02 N17 A_CAD2
CAD01 N18 A_CAD1
CAD00 P19 A_CAD0

CCBE3 E13 A_CC/BE3#
CCBE2 E18 A_CC/BE2#
CCBE1 H18 A_CC/BE1#
CCBE0 L17 A_CC/BE0#

RSVD_04/D2 B10 A_CRSVD/D2
CCD1#/CD1# N15 A_CCD1#
CCD2#/CD2# B11 A_CCD2#

CVS1/VS1# A13 A_CVS1#
CRST# C15 A_CRST#
CBLOCK# H15 A_CBLOCK#
CREQ#/INPACK# C14 A_CREQ#
CSERR#/WAIT# C12 A_CSERR#
CDEVSEL# F19 A_CDEVSEL#
CFRAME# E19 A_CFRAME#
CGRANT# G17 A_CGNT#
CINT# F12 A_CINT#
CVS2/VS2# B16 A_CVS2#
CPERR# G19 A_CPERR#
CSTOP# G18 A_CSTOP#
CIRDY F17 A_CIRDY#
CTRDY# G15 A_CTRDY#

RSVD_02/A18 H17 A_CRSVD/A18
RSVD_01/D14 M19 A_RSVD/D14

CCLKRUN# A11 A_CCLKRUN#
CPAR H14 A_CPAR
VCCCA_01 A15
VCCCA_00 J19 — A_VCC
CSTSCHG A12 A_CSTSCHG
CAUDIO B12 A_CAUDIO
CCLK F18 A_CCLK — R443 47_6 — A_CCLK1

PCI7412

CN4

A_CAD0	1	GND1	
A_CAD1	2	SKTAAD0/D3	
A_CAD3	3	SKTAAD1/D4	
A_CAD5	4	SKTAD3/D5	
A_CAD7	5	SKTAD5/D6	
A_CC/BE0#	6	SKTAAD7/D7	
A_CAD9	7	-SKTACBE0/CE1#	
A_CAD11	8	SKTAAD9/A10	
A_CAD12	9	SKTABAD11/OE#	
A_CAD14	10	SKTAAD12/A11	
A_CC/BE1#	11	SKTAAD14/A9	
A_CPAR	12	-SKTACBE1/A8	
A_CPERR#	13	SKTAPAR/A13	
A_CGNT#	14	-SKTAPERR/A14	
A_CINT#	15	-SKTAGNT/WE#	
	16	-SKTAINT/RDY	
		UPPER PIN	
A_CCLK1	19	SKTAPCLK/A16	
A_CIRDY#	20	-SKTAIRDY/A15	
A_CC/BE2#	21	-SKTACBE2/A12	
A_CAD18	22	SKTAAD18/A7	
A_CAD20	23	SKTAAD20/A6	
A_CAD21	24	SKTAAD21/A5	
A_CAD22	25	SKTAAD22/A4	
A_CAD23	26	SKTAAD23/A3	
A_CAD24	27	SKTAAD24/A2	
A_CAD25	28	SKTAAD25/A1	
A_CAD26	29	SKTAAD26/A0	
A_CAD27	30	SKTAAD27/D0	
A_CAD29	31	SKTAAD29/D1	
A_CRSVD/D2	32	SKTARSVD/D2	
A_CCLKRUN#	33	-SKTACLKRUN/WP	
	34	GND2	
	35	GND3	
A_CCD1#	36	-SKTACD1/CD1#	
A_CAD2	37	SKTAAD2/D11	
A_CAD4	38	SKTAD4/D12	
A_CAD6	39	SKTAAD6/D13	
A_RSVD/D14	40	SKTARSVD/D14	
A_CAD8	41	SKTAAD8/D15	
A_CAD10	42	SKTAAD10/CE2#	
A_CVS1#	43	-SKTAVS1/VS1#	
A_CAD13	44	SKTAAD13/IORD#	
A_CAD15	45	SKTAAD15/IOWR#	
A_CAD16	46	SKTAAD16/A17	
A_CRSVD/A18	47	-SKTRSVD/A18	
A_CBLOCK#	48	-SKTALOCK/A19	
A_CSTOP#	49	-SKTASTOP/A20	
A_CDEVSEL#	50	-SKTADEVSEL/A21	
		LOWER PIN	
A_CTRDY#	53	-SKTATRDY/A22	
A_CFRAME#	54	-SKTAFRAME/A23	
A_CAD17	55	SKTAAD17/A24	
A_CAD19	56	SKTAAD19/A25	
A_CVS2#	57	-SKTAVS2VS2#	
A_CRST#	58	-SKTARST/RESET	
A_CSERR#	59	0SKTASERR/WAIT#	
A_CREQ#	60	-SKTAREQ/INPACK#	
A_CC/BE3#	61	-SKTACBE3/REG#	
A_CAUDIO	62	SKTAAUDIO/BVD2	
A_CSTSCHG	63	-SKTASTSCHG/BVD1	
A_CAD28	64	SKTAAD28/D8	
A_CAD30	65	SKTAAD30/D9	
A_CAD31	66	SKTAAD31/D10	
A_CCD2#	67	-SKTACD2/CD2#	
	68	GND4	

SKTA/VCC1 17 — A_VCC
SKTA/VCC2 51 — A_VCC
SKTA/VPP1 18 — A_VPP
SKTA/VPP2 52 — A_VPP
GND5 69
GND6 70
GND7 71
GND8 72

CARDBUS SLOT
FOX_1CA4C5G2-TC_CARD BUS

CARD BUS

CN8

MS_DATA3_SD_DAT3_SM_D3	18	SD-1(DAT3)	(VSS)MS-1 5
MS_BS_SD_CMD_SM_WEZ	15	SD-2(CMD)	(BS)MS-2 6 — MS_BS_SD_CMD_SM_WEZ
	12	SD-3(VSS)	(DAT1)MS-3 8 — MS_DATA1_SD_DAT1_SM_D1
	10	SD-4(VCC)	(DAT0)MS-4 9 — MS_DATA0_SD_DAT0_SM_D0
MS_CLK_SD_CLK_SM_ELWPZ	7	SD-5(CLK)	(DAT2)MS-5 11 — MS_DATA2_SD_DAT2_SM_D2
MS_DATA0_SD_DAT0_SM_D0	4	SD-6(VSS)	(INS)MS-6 13 — MS_CDZ
MS_DATA1_SD_DAT1_SM_D1	3	SD-7(DAT0)	(DAT3)MS-7 14 — MS_DATA3_SD_DAT3_SM_D3
MS_DATA2_SD_DAT2_SM_D2	2	SD-8(DAT1)	(SCLK)MS-8 16 — MS_CLK_SD_CLK_SM_ELWPZ
SD_CDZ	20	SD-9(DAT2)	(VCC)MS-9 17
	21	SD-CD1	(VSS)MS-10 19
SD_WP_SM_CEZ	23	SD-CD2(G)	
	1	SD-WP1	
	22	SD-WP-COM	
	24	NAIL1	
	25	NAIL2	
	26	NAIL3	

3@3IN1_DFHD23MS069

VCC_FM

LE4 D:
change footprint form
3IN1-R009-020-XX-21P to
3IN1-R009-020-XX-21P-LE4

VCC_FM
C451 0.1U-10V_4 — C410 0.1U-10V_4 — C409 CR@.1U-10V_4 — C443 CR@.1U-10V_4

3VSUS
R242 CR@10K_4 — MC_PWR_CTRL_0#
Q35 TPS2061DGNR
IN1 2, IN2 3, EN# 4, GND 1, GND-C 9, OUT3 8, OUT2 7, OUT1 6, OC# 5
VCC_FM
C598 10U-10V_8
C411 0.1U-10V_4

Supporting MMC/SD/MS Cards
Foxconn P/N:DFHS19FR012

3VSUS
C415 0.1U-10V_4 — C412 10U-10V_8
C418 0.1U-10V_4 — C396 0.1U-10V_4 — C435 10U-10V_8 — C416 0.01U-16V_4 — C397 0.01U-16V_4

3VSUS
C421 0.1U-10V_4 — C423 1U-16V_6 — C437 1U-16V_6
1394_AVDD
C403 0.1U-10V_4 — C399 1U-16V_6

VCC_FM
C441 2.2U-6.3V_6
R302 CR@150K_6
CLOSE CONN

C395 0.1U-10V_4
1394_AVDD

U22D

		1.5V_00	K1
		1.5V_01	K19
		VDDPLL33	U19
H6		GND_00	
K6		GND_01	
N6		GND_02	
P7		GND_03	
P9		GND_04	
M14		GND_05	
K14		GND_06	
G14		GND_07	
F13		GND_08	
F10		GND_09	
F7		GND_10	
		VCC33_00	J6
		VCC33_01	L6
		VCC33_02	P6
		VCC33_03	P8
		VCC33_04	P10
		VCC33_05	L14
		VCC33_06	J14
		VCC33_07	F14
		VCC33_08	F12
		VCC33_09	F9
		VCC33_10	F6
		AVDD33_00	P13 — 1394_AVDD
		AVDD33_01	P14
		AVDD33_02	U15
		VCCP_00	P1 — 3VSUS
		VCCP_01	W8

Power/GND

PCI7412

5VSUS
U18
5V_0 1, 5V_1 2, DATA 3, CLOCK 4, LATCH 5, NC_0 6, 12V_0 7, AVPP/AVCORE 8, AVCC0 9, AVCC1 10, GND 11, RESET# 12
5V_2 24, NC_3 23, NC_2 22, SHDN# 21, 12V_1 20, BVPP/BVCORE 19, BVCC1 18, BVCC0 17, NC_1 16, OC# 15, 3.3VIN0 14, 3.3VIN1 13
NC 25
TPS2220APWP

(24) TPS_DATA — TPS_DATA
(24) TPS_CLOCK — TPS_CLOCK
(24) TPS_LATCH — TPS_LATCH
T74
A_VPP
A_VCC
(13,24,33) PCIRST#
3VSUS

TPS_CLOCK
R457 *47K_4

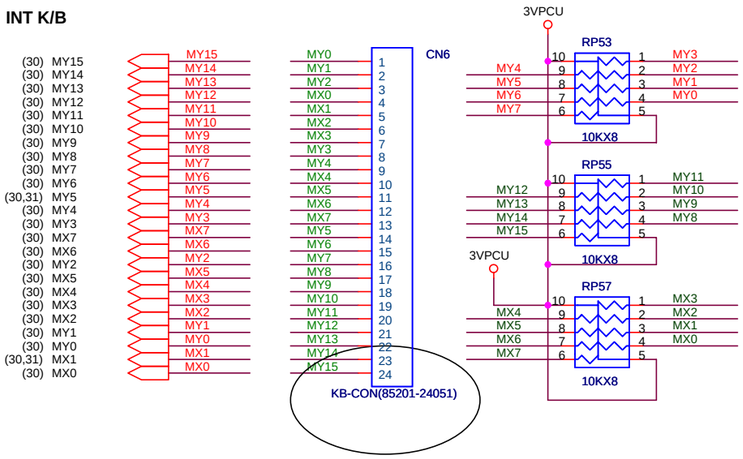
A_VPP
5VSUS
3VSUS
C571 0.1U-10V_4 — C570 0.01U-16V_4
C581 0.1U-10V_4 — C575 10U-10V_8
C583 0.1U-10V_4 — C584 0.1U-10V_4 — C580 10U-10V_8 — C588 0.01U-16V_4 — C582 0.01U-16V_4

A_VCC
C568 0.01U-16V_4 — C567 0.01U-16V_4 — C572 0.1U-10V_4 — C574 0.1U-10V_4 — C576 10U-10V_8
A_VCC
C569 0.01U-16V_4 — C577 10U-10V_8
3VSUS
C587 0.1U-10V_4 — C586 1U-16V_6 — C585 1U-16V_6

PROJECT : LE4
Quanta Computer Inc.

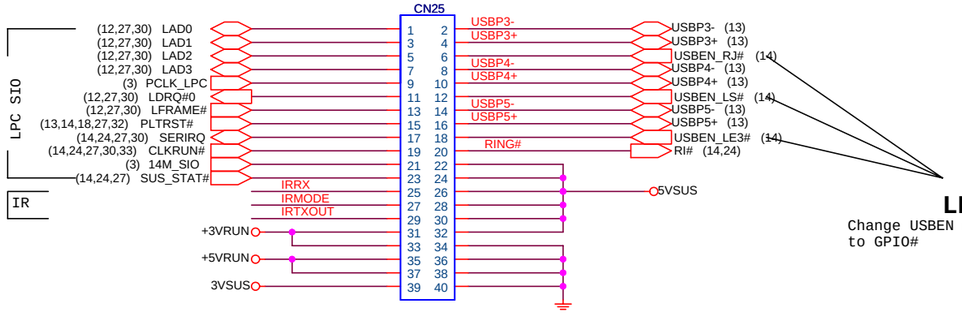
Size	Document Number	Rev
	PCI7412 - 3 IN 1 / CARD BUS	1A
Date: Tuesday, March 14, 2006	Sheet 25 of 42	

INT K/B



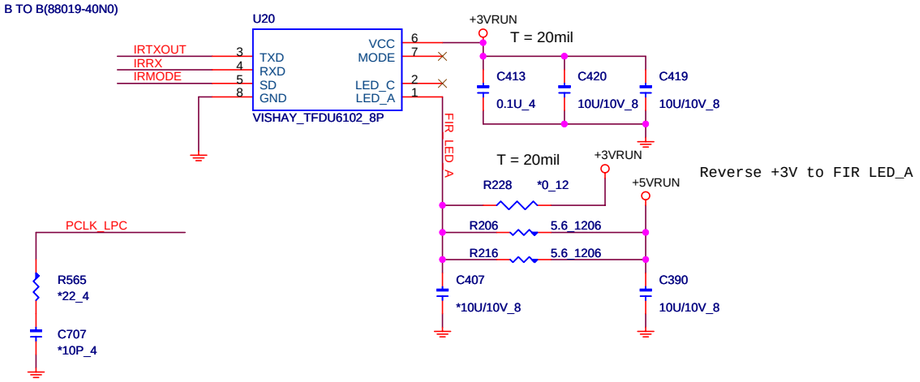
1/27 update keymatrix as same as le1

M/B TO MODEM/B



LE4 C:
Change USBEN meaning from OC# to GPIO#

MODEM B TO B(88019-40N0)



HOLE6 *H-C354D106P2 — **CRT and SV between**

HOLE13 *H-C354D106P2 — **LAN and LID between**

HOLE11 *H-C354D106P2 — **ODD-R**

HOLE15 H-C354D106P2 — **VGA-RU**

HOLE12 *H-C236BC354D106P2 — **ODD-L+screw**

HOLE1 *H-C354D106P2 — **Audio Jack**

HOLE14 *H-C354D106P2 — **Power/B**

HOLE2 *H-TC236BC354D106P2 — **PCMCIA-L-M**

HOLE4 *H-C354D106P2 — **CRAD BUS R-DOWN**

HOLE5 *H-C354D106P2 — **PCMCIA-R-M**

HOLE7 *H-C354D106P2 — **N.B and BIOS between**

HOLE3 *H-C354D106P2 — **1394**

VGA+N.B. NUT

HOLE20 H-C238D150P2

HOLE16 *H-C2380150P2

HOLE19 H-C238D150P2

IO Module NUT

HOLE24 H-C236D150P2

HOLE23 H-C236D106P2

CPU NUT

HOLE22 H-C238D150P2

HOLE18 H-C238D150P2

HOLE17 H-C238D150P2

HOLE21 H-C238D150P2

HDD NUT

HOLE9 H-C238D150P2

Modem NUT

HOLE10 H-C236D142P2

HOLE8 H-C236D142P2

P29 P24 P23 P27 P11 P12 P28 P8 P26 — EMIPAD158X87

P7 P9 P10 P14 P25 P16 P1 P15 P30 — EMIPAD158X87

P1 — AGND

HOLE25 H-C236D142P2

HOLE26 H-C236D142P2

PCIe-NUT

BOTTON

E@EMI P21 P22 P20 — EMIPAD158X87

P18 P17 P19 — EMIPAD158X87

E@EMI E@EMI E@EMI

TOP

E@EMI P4 P5 P6 — EMIPAD158X87

P2 P3 — EMIPAD158X87

E@EMI E@EMI

P13 EMIPAD158X87

MIC

P31 S8-90

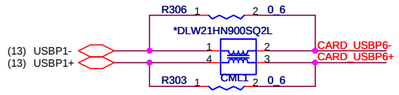
LE4 C:
Arrange modem cable

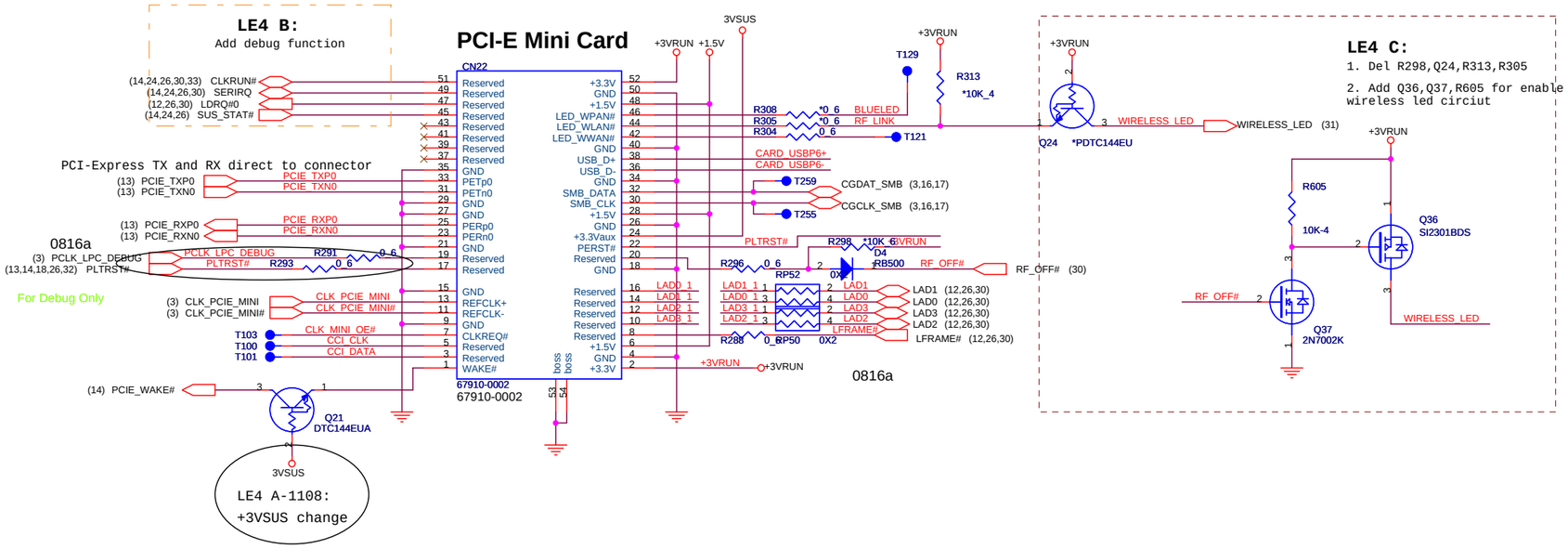
PROJECT : LE4

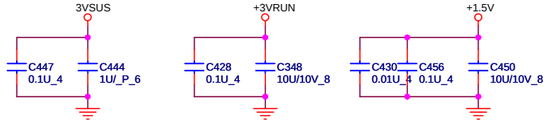
Quanta Computer Inc.

Size	Document Number	Rev
	SCREW hole EMI pad	1A
Date: Tuesday, March 14, 2006	Sheet 26 of 42	

Need one more wireless LED /mini card on MB ?
currently , No LED here







PROJECT : LE4		
Quanta Computer Inc.		
Size	Document Number: MIMI PCI e	Rev: 1A
Date: Tuesday, March 14, 2006	Sheet 27 of 42	

LE4 A-1108:

3VSUS

L50 BK2125HS330-T

For associated Line Side Device portion of this design see Conexant RD02-D450 reference schematic

C247 10U/10V_8 C243 0.1U_4 C238 0.1U_4

3V_DVDD

VDDIO is used in determining which HD Audio bus voltage is present on the system. When VDDIO is +1.5V, the device will use 1.5v signaling on the HDA interface pins; when VDDIO is +3.3v, the device will use 3.3v signaling on the HDA interface pins.

AVDD

L21 *BK2125HS330-T +3VRUN

U10 GMT_G910T21U Vout Vin GND +5VRUN

C543 0.1U_4 C230 0.1U_4 C260 0.1U_4 C202 10U/10V_8 AGND

C69 1U_4 C75 0.1U_4 C59 10U/10V_8

U11 CX20549-12

VDDIO DVDD DVDDM AVDD_20 AVDD_31 AVDDHP

(12) ACZ_RST#_AUDIO ACZ_RST#_AUDIO 10 RESET#

(12) BIT_CLK_AUDIO BIT_CLK_AUDIO R104 33_4 BITCLK 5 BIT_CLK

(12) ACZ_SYNC_AUDIO ACZ_SYNC_AUDIO 9 SYNC

(12) ACZ_SDIN0 R99 0_4 SDI 7 SDI

(12) ACZ_SDOUT_AUDIO ACZ_SDOUT_AUDIO 4 SDO

MIC_BIAS_L MIC_BIAS_R MIC_L MIC_R 29 30 21 22 MICBIAS_INT INT_MIC

LINEOUT_L LINEOUT_R 35 36 LINEOUT_L (29) LINEOUT_R (29) Speaker

PORT-A_BIAS_L PORT-A_BIAS_R PORT-A_L PORT-A_R 33 34 38 39 LINEIN_L_1 C263 1U_6 HPOUT_L C262 1U_6 HPOUT_R HPOUT_L (29) HPOUT_R (29)

(29) DIBP_HS DIBP_HS R122 0_4 DIBP 44 DIBP

(29) DIBN_HS DIBN_HS R123 0_4 DIBN 43 DIBN

Near To Codec

PORT-B_BIAS_L PORT-B_BIAS_R PORT-B_L PORT-B_R 14 15 23 24 EXT_MICBIAS_L EXT_MICBIAS_R EXT_MIC_L EXT_MIC_R MIC IN

BEEP 11 PCBEEP

CD_L CD_GND CD_R 17 18 19 CDAUDL C229 1U/16V_6 CDGND C215 1U/16V_6 CDAUDR C216 1U_6 AGND AVDD

48 SPDIF

(29) EAPD EAPD 47 EAPD

SENSE 13 SENSE R75 5.11K/F_6 SENSE_PORT_A T20 R71 5.11K/F_6 SENSE_PORT_B R68 10K/F_4 R69 39.2K_4 SENSE_MIC T19 R70 20K_4 SENSE_LINEOUT (29)

1 2 16 NC_1 NC_2 NC_16

VREF_HI VREF_LO VC_REFA 26 27 28 VREF_HI VREF_LO VC_REFA C540 1U_4 AGND C541 1U_4

3V_DVDD R403 237K/F_8 RCOSC 41 RCOSC

RC0805

VSSIO_42 VSSIO_46 DVSS AVSS_12 AVSS_25 AVSS_32 AVSSHP

42 46 6 12 25 33 40 AGND

BIT_CLK_AUDIO ACZ_SYNC_AUDIO ACZ_SDIN0

R399 *22_4

C544 *10P_4 C236 *10P_4 C542 *10P_4

DIGITAL ANALOG

+5VRUN U15 74AHCT1G86GW C201 0.1U/10V_4 04/9

+5VRUN C291 0.1U/10V_4 E200505-0166 5/6 update

(24) PCMSPK (14) ACZ_SPKR (29,30) MUTE# (14) AMP_BEEP R153 *0_4 U14 74AHCT1G08GW PCBEEP R80 10K_4 R84 10K_4 C232 0.47U/10V_6 BEEP

BEEP MIC

R572 *0_4

LE4 B: add R572

LE4 C: Cancel R572
ADD R80,R84,U15,U14,C301,C291

EXT_MICBIAS_R EXT_MICBIAS_L R77 *10K_4 R76 *10K_4 AVDD AVDD

R64 2.2K_4 R65 2.2K_4

EXT_MIC_R C227 10U_8 EXT_MIC_L C226 10U_8 R_SYS_MIC_1 L1 BK1608LL121_6 SYS_MIC_1 R_SYS_MIC_2 L3 BK1608LL121_6 SYS_MIC_2 SENSE_PORT_B R6 0_6

R63 *1K_4 R66 *1K_4 AGND AGND

C2 100P_4 C5 100P_4 AGND AGND

MIC JACK

CN13 JACK_MIC(010178FR006G101JL) AGND AGND

Fox : JA6333L-1S0-TR => AC97
JA6333L-3S0-TR => Azalia

LE4 B:
SWAP CN13,CN14
position and Change
Footprint

C: Change to 0_4

R343 0_4 MICGND

CN12 INT_MIC1 R344 0_4 R_INT_MIC L40 BK1608LL121_6 L_INT_MIC INT_MIC MICGND

R342 *1K_4 C478 100P_4 MICGND

MICBIAS_INT R394 *10K_4 AVDD

R395 2.2K_4

C539 10U_8 INT_MIC

R390 *1K_4 AGND

LE4 C:
Modidy bias voltage type from C539 before

PROJECT : LE4

Quanta Computer Inc.

Size	Document Number	Rev
	Azalia Codec / Audio Jack	1A
Date: Tuesday, March 14, 2006	Sheet 28 of 42	

0816a

EAPD
low:mute

LE4 C:
slove power on systrm
when the sound had
bob

LE4 C:
Support Vista function

LE4 B: add D17 and R573

AUDIO POWER

LE4 A:
Place near Audio port with CN26

AUDIO POWER

LE4 C:
Del R350

LE4 A:
Place near Audio port with CN14

LE4 C:
Support Vista function

LE4 A:
Place near audio codec

08/04:Change CN5 Left/right pin define and P/N

LE4 B:
Change GND plane from
AUDGND to AGND

LE4 B:
SWAP CN13,CN14
position and Change
Footprint

When Docking insert , disable BTL

GAIN	SPKR MODE	HP MODE
0	10.5	3
1	9	0

Modem connector

2/16 swap audio conn
pin define

PROJECT : LE4		
Quanta Computer Inc.		
Size	Document Number: Audio Amp.	Rev: 1A
Date: Tuesday, March 14, 2006	Sheet 29 of 42	

Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

LE4 B: Pull high, Add R593, R592

BT1#	R593	4.7K_4
BT4#	R592	4.7K_4
ENV1	R332	10K_4
BADDR0	R331	*10K_4
BADDR1	R330	*10K_4
SHBM	R329	10K_4

BADDR1-0	I/O Address	
	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

LE4 B: Pull high, add R594, R595

LE4 B: Change BT4# from pin 43 to pin176

Power LED controll

LE4 B: pin 175 EC_FPBACK# change to pin 41

LE4 B: Chnage pin 176 form 551_LPCPD# to BT4#

LE4 B: pin 24 add 591_PME#

LE4 A: for EC Debug

IOSEL# is NC now

LE4 B:

LE4 A: Change Power plan

LE4 B: Add R273 in BOM

FLASH 8Mbit (1M Byte),NO PLCC TYPE

AMD :Pin 10 is RESET# ; Pin12 is RY/BY#
SST :Pin10,12 are NC

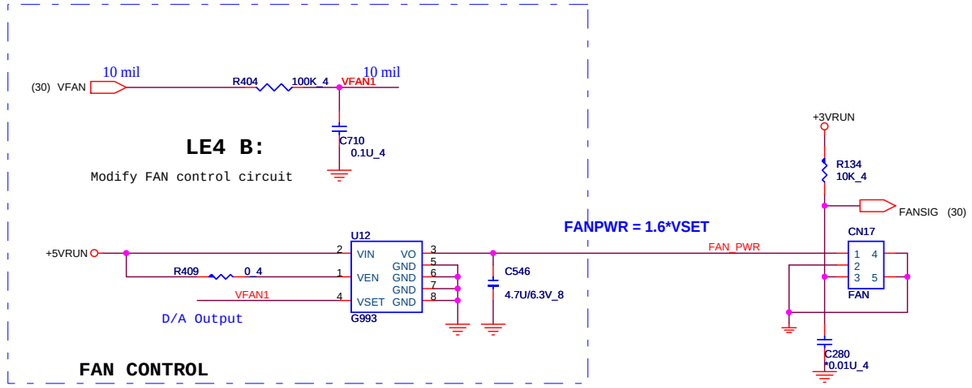
AKE358AKZ61 IC EEPROM(40P)MX29LV008BTTC-70G(1M*8)LF
AKE358AKZ87 IC EEPROM(40P)MX29LV008CTTC-70G(1M*8)LF

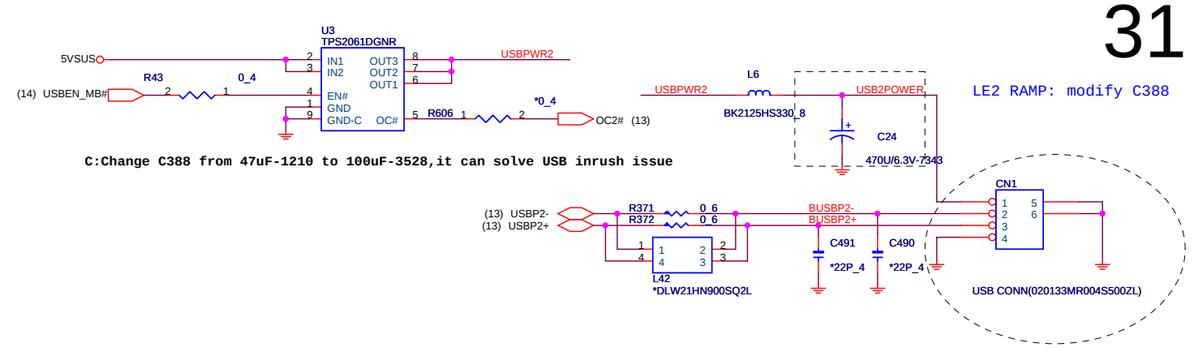
1.AMD-29LV081B require MAX 500nS Tready for it's hardware reset.And MAX6326_UR29 has >100mS reset timing.So we can tie it's reset# pin to +3VALW directly.
2.SIO has internal 20 mS delay of VCC1_PWROK

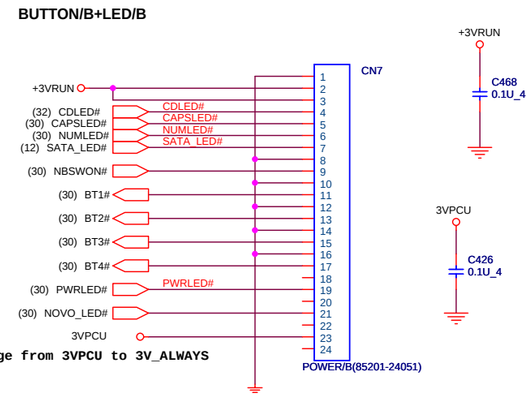
Battery LED BLUE and AMBER

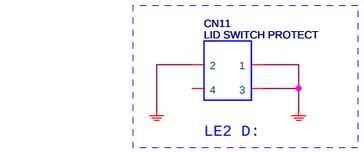
PS/2 to Port Replicator

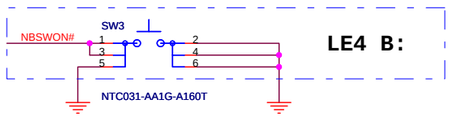
Project	PROJECT : LE4	
Quanta Computer Inc.		
Size	Document Number	Rev
	PC87541 & FLASH	1A
Date: Tuesday, March 14, 2006	Sheet 30 of 42	

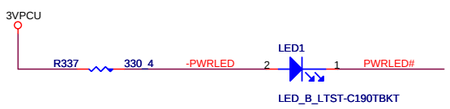


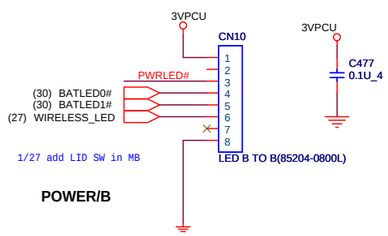


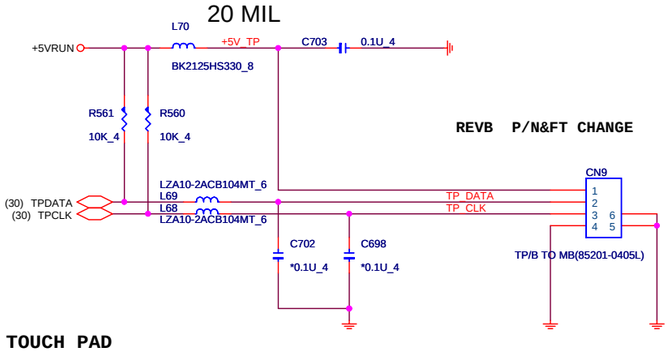


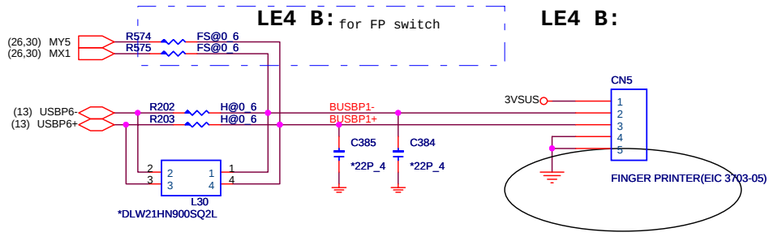












Finger Printer

PROJECT : LE4

Quanta Computer Inc.

Size	Document Number	Rev
	USB BT FP TP PB BD FAN	1A
Date: Tuesday, March 14, 2006	Sheet 31 of 42	

SATA HDD

CN19

ALLTOP-C16647-122A4-L

SATA_RXP0_C (12)
SATA_RXN0_C (12)
SATA_TXN0 (12)
SATA_TXP0 (12)

1.5A

LE4 B:
Add L73

BLM18PG181SN1_6

LE4 B:
Add L74

BLM18PG121SN_6
BLM18PG121SN_6
BLM18PG181SN1_6

BLM18PG121SN_6

Near To SATA connector

LE4 A:
Place near SATA connector

LE4 A:
Place near POWER source

PDD[0..15] PDD[0..15] (12)
PDCS1# PDCS1# (12)
PDCS3# PDCS3# (12)
PDA0 PDA0 (12)
PDA1 PDA1 (12)
PDA2 PDA2 (12)
PDIOR# PDIOR# (12)
PDIOW# PDIOW# (12)
PIORDY PIORDY (12)
IRQ14 IRQ14 (12)
PDDREQ PDDREQ (12)
PDDACK# PDDACK# (12)

ODD

LE4 B:
CN24 change back to LE2 footprint

ALLTOP-C1242B-150B1
DFHD50MRA75

LE4 C:
Del R328 in BOM

LE4 B:
Add parts in BOM
R335 set to Master

2.0A

LE4 B:
Add L72

BLM18PG121SN_6
BLM18PG121SN_6

Q22
DTC144EU

PROJECT : LE4			
Quanta Computer Inc.			
Size	Document Number		Rev
	SATA HDD & PATA ODD		1A
Date: Tuesday, March 14, 2006	Sheet 32 of 42		

FOR 10/100 +3V_S5 R562 4@0_8
FOR GIGA +3VRUN R563 5@0_8

VDDIO_LAN

C706 10U/10V_8 | C686 0.1U_4 | C672 0.1U_4 | C668 0.1U_4 | C696 0.01U/16V_4 | C660 0.01U/16V_4 | C680 0.01U/16V_4 | C654 0.01U/16V_4

+1.8V_1.2V_LAN

U26

Voltage Rail	4401	5702	5705M
VDDIO_PCI	3V_S5	+3V	+3V
+3V_2.5V_LAN	3.3V	2.5V	2.5V
+1.8V_1.2V_LAN	1.8V	1.2V	1.2V

(13,24) AD[31..0] — AD[31..0] — AD0 N7 … AD31 B8

C/BE0# M4 CBE_0#
C/BE1# L3 CBE_1#
C/BE2# F3 CBE_2#
C/BE3# C4 CBE_3#

+3V_S5 R321 4.7K_4 J12 VAUXPRSNT
REQ1# C3 REQ#
GNT1# J3 GNT#
FRAME# F2 FRAME#
IRDY# F1 IRDY#
DEVSEL# H3 DEVSEL#
STOP# H1 STOP#
TRDY# G3 TRDY#
PAR J1 PAR
PERR# J2 PERR#
SERR# A2 SERR#
INTB# H2 INTA#
PCIRST# C2 PCI_RST#
PCLK_LAN A3 PCI_CLK
AD23 R523 0_4 A4 IDSEL
LAN_PME# R522 0_4 A6 PME#

4401,5788 support CLKRUN

CLKRUN# R525 0_4 C8 CSTSCHG
PCLK_SMB R520 *0_4 H4 CLKRUN#
PDAT_SMB R521 *0_4 A10 SMB_CLK
R322 5@4.7K_4 C9 SMB_DATA
M11 LOW_PWR

4401 and 5788M don't support SMBus

F4 M66EN

+3V_2.5V_LAN
C685 0.1U_4 | C670 0.1U_4 | C694 0.01U/16V_4
C466 27P_4 | C465 27P_4 | Y6 25MHZ BG625000737 | R319 200_6
CLK_LAN_X1 J14 XTALVDD
N11 XTALI
CLK_LAN_X2 N10 XTALO

+1.8V_1.2V_LAN L67 BK1608HS330_6
10mils
LAN_PLLVDD2 T264 P7 NC/PLLVDD3
C682 0.1U_4 | C683 4.7U/6.3V_8
H14 PLLVDD2

L8 NC
M9 NC
N8 NC

@BCM4401/5788

15mm x 15mm BGA196

BIASVDD A14 — BIASVDD — L64 — +3V_2.5V_LAN
VDDIO A11, F11, K12, L12 — +3V_S5 — C651 1000P_4 — PBY201209T-300Y-S_8
VESD1 P1, VESD2 G2, VESD3 A1 — +3V_S5
NC/VDDP K14, NC/VDDP L13, VDDP P11 — +3V_2.5V_LAN
NC/AVDD A13, NC/AVDD F14 — LAN_AVDD — L65 — +3V_2.5V_LAN — C652 0.1U_4 — BK1608HS330_6
EPHY_AVDD/AVDDL F12, EPHY_AVDD/AVDDL F13 — LAN_AVDDL

C671 5@0.1U_4 | C665 5@0.1U_4 | C662 0.1U_4 | C659 0.1U_4

NC/TRD[3]- E14 — R537 5@49.9/F_4 — TX3N — TX3N (34)
NC/TRD[3]+ E13 — R534 5@49.9/F_4 — TX3P — TX3P (34)
NC/TRD[2]- D14 — R533 5@49.9/F_4 — TX2N — TX2N (34)
NC/TRD[2]+ D13 — R531 5@49.9/F_4 — TX2P — TX2P (34)
RDN/TRD[1]- C14 — R530 49.9/F_4 — TX1N — TX1N (34)
RDP/TRD[1]+ C13 — R529 49.9/F_4 — TX1P — TX1P (34)
TDN/TRD[0]- B14 — R527 49.9/F_4 — TX0N — TX0N (34)
TDP/TRD[0]+ B13 — R526 49.9/F_4 — TX0P — TX0P (34)

LINK_LED10#/LINKLEDB G13 — 10MBPS# — 100MBPS# (34)
LINK_LED100#/SPD100LEDB H13 — -100MBPS R538 0_4
COL_LED#/SPD1000LEDB G12 — 1GBPS#
ACT_LED#/TRAFFICLEDB G14 — ACT# — ACT# (34)

ALWAYS USE -100MBPS
1.27Kohm+-1% for 4401
1.24Kohm+-1% for 5788M

RDAC D10 — LAN_RDAC — R519 5@1.24K/F_4/4@1.27K/F_4

GPIO0 H12, GPIO1 K13, GPIO2 J13 — EEWP# — R320 1K_4 — +3V_S5
SPROM_CLK/EECLK M10 — EECLK — R323 5@1K_4
SPROM_CS/EEDATA P10 — EEDATA — R324 5@1K_4

U29
+3V_S5 — C697 5@0.1U_4
EEWP# 7, EECLK 6, EEDATA 5
VCC 8, WP# 7, SCL 6, SDA 5, A0 1, A1 2, A3 3, GND 4
5@24C128

LAN_AVDDL — L66 — +1.8V_1.2V_LAN — C673 0.1U_4 — BK1608HS330_6

U28
EEDATA 1, EECLK 2, BCM_DI 3, BCM_DO 4
CS 1, SK 2, DI 3, DO 8, VCC 8, NC 7, ORG 6, GND 5
4@93LC46
+3V_S5 — C679 4@0.1U_4

SPROMDOUT/NC N9, SPROMDIN/NC P9 — BCM_DI, BCM_DO

TRST# D11 — BCM_TRST# — R518 1K_4 — +3V_S5
TDI D12, TCK C12, TMS A12, TDO B12
REGIN33/REGSUP25 B11 — Q18 5@BCP69T1 — 1G — C633 10U/10V_8 | C625 0.01U/16V_4
NC/REGCTL25 C11
OUT33/REGSEN25 C10 — 40mils — 2.5V@88mA 0.564W — +3V_2.5V_LAN
NC/REGSUP12 B9 — Q19 5@BCP69T1 — 1G — C634 10U/10V_8 | C626 0.01U/16V_4 | C620 0.01U/16V_4 | C618 0.01U/16V_4
NC/REGCTL12 B10
REGOUT18/REGSEN12 A9 — 40mils — 1.2V@618mA 0.803W — +1.8V_1.2V_LAN
C635 10U/10V_8 | C621 0.01U_4 | C619 0.01U_4 | C627 0.01U_4

NC L7, NC K11, NC K4, NC J11, NC J4, NC H10, NC M8, NC L14, VSS/NC L11
NC/CS# H11, EECLK_PXE/SCLK E11, EEDATA_PXE/SI E10, NC/SO G11

1.5" AWAY FROM CHIP
Use Philips BCP69-16, hfe=75~275

VSS B7, D4, D5, D6, D7, D8, D9, NC/VSS E2, E5, E6, E7, E8, E9, F5, F6, F7, F8, F9, F10, G4, G5, G6, G7, G8, G9, G10, H9, K2, L6, L9, M6, M12, M13, N1, N12, N13, ND/VSS

BCM4401 is for 10/100(1.8)
BCM5702 is for giga
BCM5705M is for giga cost-down(12)

LE4 C:
Select enable or disable LAN function

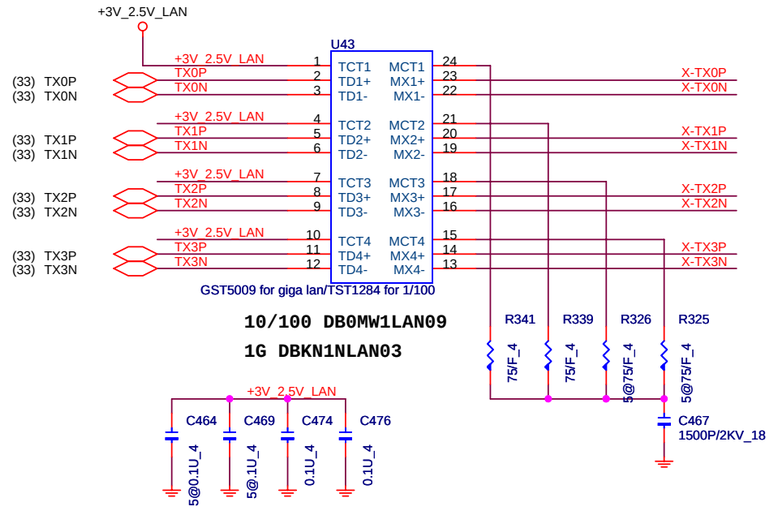
PCLK_LAN — R524 *22_4 — C655 *10P_4

+3V_2.5V_LAN: C704 10U/10V_8 | C691 0.1U_4 | C666 0.1U_4 | C701 0.1U_4
+1.8V_1.2V_LAN: C705 10U/10V_8 | C695 0.1U_4 | C700 0.1U_4 | C699 0.1U_4 | C677 0.01U/16V_4 | C676 0.01U/16V_4 | C678 0.01U/16V_4 | C653 0.01U/16V_4

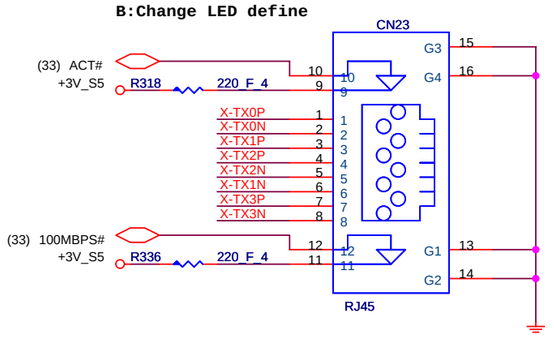
PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	BCM4401/5705M LAN	A
Date: Tuesday, March 14, 2006	Sheet 33 of 42	

B:Change 10/100 LAN transform U23 to ST1284A(DB0MW1LAN09)



B:Change LED define



PROJECT : LE4

Quanta Computer Inc.

Size	Document Number	Rev
	DVO CH7011A & RJ45-11 CON	A
Date: Tuesday, March 14, 2006	Sheet 34 of 42	

LE4 B: add PL27 change PL18 same as PL27

PL27 HI0805R800R-10

PL18 HI0805R800R-10

LE4 C: VA-1

PJ1 2DC-S726B201

PJ1.1

PC168 0.1U_50V_6

PC169 1000P_X7_6

LE4 B: del PL4

PC171 0.1U_50V_6

LE4 B: change size 0805 to 0603

PD17 SSM24PT

PD18 SSM24PT

VA

PC173 10U_25V_1206

PR183 0.01

VA2

R3

PL5 FBJ3216HS800-T

VIN

300mil

PR192 10K_F_6

PQ55 DTA124EU

PC88 10U_25V_1206

PC89 0.1U_50V_6

8724_3D3_LDO

PC170 1U_X7_8

LE4 C: VA-1

PC167 0.1U_50V_6

PQ56 SI4425BDY-T1-E3

PR86 100K_F_6

8724_3D3_LDO

PR87 100K_F_6

CELL-SET
0 = 4 CELL
1 = 3 CELL

LE4 C: VA-1

PD16 RB500

LE4 B: del PR80

LE4 A:

PR81 75K_6

PR88 825_F_6

PR182

PR90 1.33K_F_6

8724LDO

CELL_SET

CELL_SET (30)

PQ35 2N7002K

PC90 0.1U_50V_6

PR94 200K_F_6

PR82 10K_F_6

PC78 0.01U_50V_6

PR84 0_6

PC172 1U_X7_8

27 CSSP

26 CSSN

DCIN CELLS

LDO

DLOV 8724DLOV

BST 8724BST

PR91 0_6

33_6

PC85 1U_10V_X5_6

PC86 1U_10V_X5_6

PD8 SW1010C

PQ38 SI4425BDY-T1-E3

PR186 100K_F_6

LE4 B: change c from 0.015ohm to 0.01ohm

PQ40 DTA124EU

ACOK

8724LDO

PR96 10K_F_6

8724_3D3_LDO

(30) CC-SET

CC-SET_R

(30) ACIN

PR95 15K_6

ACIN

VCTL

ICTL

REFIN

ACOK

ICHG

IINP

SHDN

DHI 8724DH

LX 8724LX

DLO 8724DL

PGND

CSIP

CSIN

BATT V_CHG

REF

CLS

PC87 0.1U_50V_6

PC82 1000P_X7_6

PC80 1000P_X7_6

PC79 0.1U_50V_6

ACOK#

PQ37 SI4914DY-T1-E3

PL6 10uH 30% 4.4A(SIL104R-100PF)L-F

8724LXR

PR97 0.01

V_CHG

PC92 0.1U_50V_6

PC94 10U_25V_1206

PC93 10U_25V_1206

8724_3D3_LDO

VA2

PC91

PR202 *0_6

PR180 100K_F_6

PR83 1K_6

PR181 20K_6

PR85 20K_6

CCV

CCI

CCS

GND GND

PU5 MAX8724

R1

R2

PR89 13.3K_F_6

PC84 1U_10V_X5_6

PC77 0.1U_50V_6

PC81 0.01U_50V_6

PC83 0.01U_50V_6

PQ39 2N7002K

PD9 SW1010C

PR93 1M_F_6

1U_X7_8

ACOK#

3VPCU

PR179 *0_6

LE4 C:

Iinput =(V CLS / V REF)*(0.075/ RS1)

ICHG =(V ICTL / V REFIN)*(0.075/ RS2)

5VPCU

(12,15,36,38,39,40) 5VPCU

VAD-5

3VPCU

(12,14,15,22,26,30,31,39,40) 3VPCU

PR191 100K_F_6

ACOK

PD19 RB500

PQ61 2N7002K

VIN

(22,36,37,38,39,41) VIN

3VPCU

PR190 100K_F_6

ACOK-2

D/C#

D/C# (30)

PQ58 2N7002K

PD20 SW1010

PR187 475K_F_6

P331

P332

PU9 LMV331

PR188 332K_F_4

PR189 100K_F_6

PQ62 2N7002K

BL/C# (30)

4A

PR195 100K_4

MBATV

MBATV (30)

PL8 HI0805R800R-10

PR193 14K_F_4

PC176 0.01U_25V_4

V_CHG

PF1 TR2/6125FA10A

PL7 HI0805R800R-10

PJ2 SUYIN_200275MR005G118ZL

3VPCU

PR196 330_4

PR197 330_4

PR194

(5,30) MBCLK

(5,30) MBDATA

10K_F_4

(30) TEMP_MBAT

PD22 ZD5.6V

PD21 ZD5.6V

10V

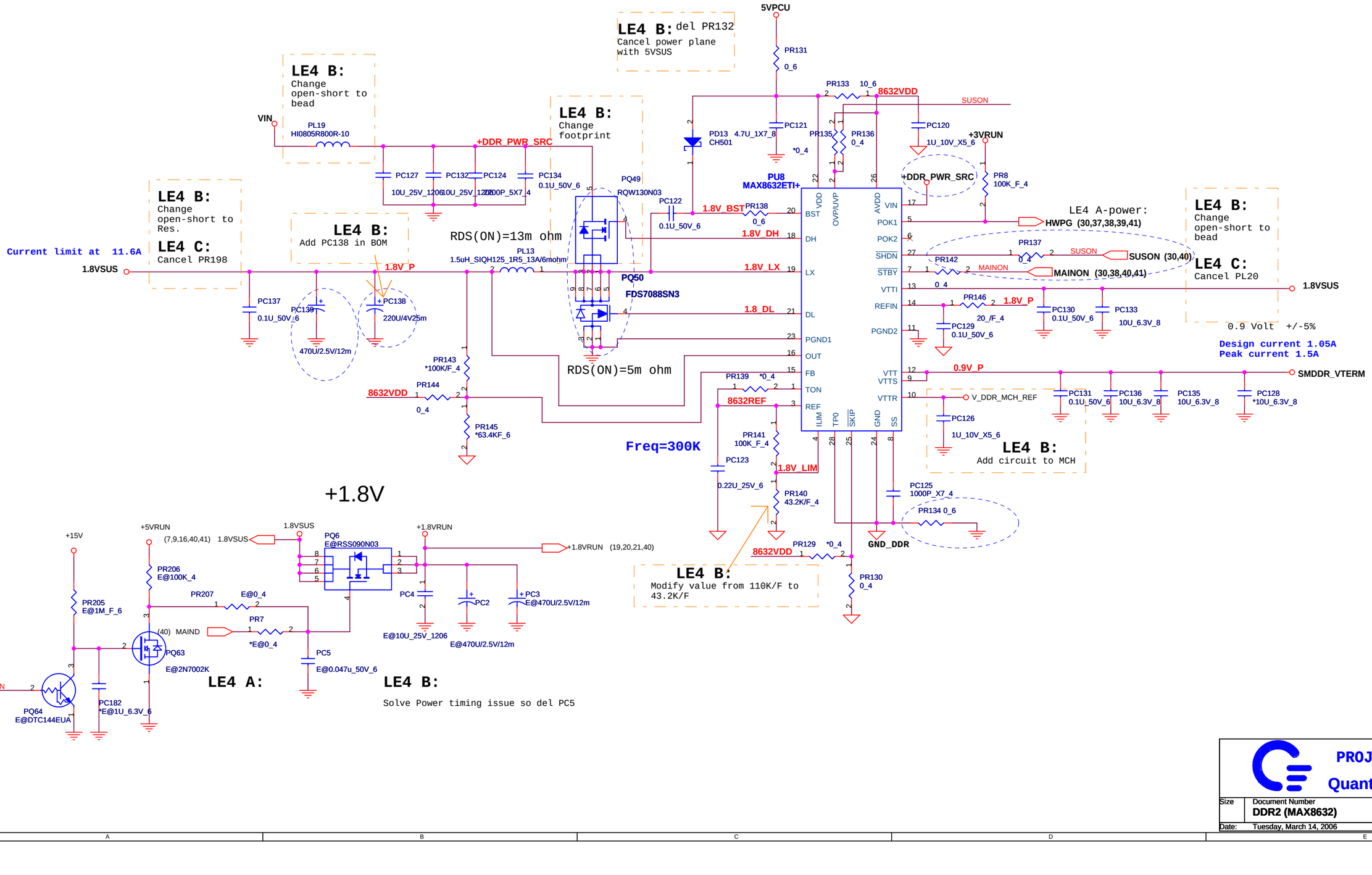
PC177 0.1U_10V_4

LE4 C:

PROJECT : LE4

Quanta Computer Inc.

Size	Document Number	Rev
	Charger --MAX8724	1A
Date: Tuesday, March 14, 2006	Sheet 35 of 42	



PROJECT : LE4		
Quanta Computer Inc.		
Size	Document Number: DDR2 (MAX8632)	Rev: 1A
Date: Tuesday, March 14, 2006	Sheet 36 of 42	

LE4 B:
Change netname from
VR_PWRGD_CK410# to CLK_EN#

CLK_EN# PQ34 2N7002K PR79 1K_F_4 VRON PR78 *0_4 PC76 0.1U_4 CLKEN

5VSUS

LE4 B: change PC68
10u 25V_1206 to 4.7u_0805

PR33 0_6 8771VDD PR66 10_4 PC68 4.7U_1X7_8 PD6 SDM10K45-7-F

8771VCC PC63 2.2U_10V_X5_6 8771BST1 PC67 0.22U_25V_6

+CPU_PWR_SRC PR70 0_6 PR43 200K_F_4

PR36 0_6 PR38 10K_F_4 PR39 1.91K_F_4 PR171 10K_F_4

VCC VDD

T272 PR62 *0_6

(7,14) DELAY_VR_PWRGOOD

(3,14) CLK_EN#

CLKEN

(5) H_VID0 PR64 0_4
(5) H_VID1 PR63 0_4
(5) H_VID2 PR58 0_4
(5) H_VID3 PR54 0_4
(5) H_VID4 PR49 0_4
(5) H_VID5 PR47 0_4
(5) H_VID6 PR45 0_4

(4) PSI# PR40 0_4

(30) VRON PR173 100K_F_4

(4,12) ICH_DPRSTP# PR37 0_4

(30,36,38,39,41) HWPG PR172 0_4

(14) PM_DPRSLPVR PR44 0_4

LE4 A:

PC161 100P_50V_4

PC49 470P_X7_4

PR42 71.5K_F_4

PC59 0.22U_10V_6

8771REF

PR168 10K_F_4

8771VCC

PR169 *NTC 10K_6-B4.25K_6

5VSUS

PR41 56_4

(4) PH_PROCHOT#

LE4 B:
Change nename

PR167 10K_F_4

PC159 0.1U_10V_4

PR175 0_6

PHASEGD PWRGD CLKEN D0 D1 D2 D3 D4 D5 D6 PSI SHDN DPRSTP DPRSLPVR CCV TIME REF GND EP THRM VRHOT POUT

TON BST1 LX1 DH1 DL1 PGND1 FB CCI GNDS CSP1 CSN12 CSP2 DH2 DL2 LX2 BST2 PGND2

PU3
MAX8771

8771BST1_R
8771LX1
8771DH1
8771DL1

PR165 *3.48K/F_4 PC158 *4700P_4

PR164 3.48K_F_4 PR166 100_4 PC50 4700P_X7_4 PR46

PC56 470P_X7_4 20K_4 PR170 100_4

PC160 1000P_X7_6

VCCSENSE (5)

PR48 *100_4

VCC_CORE

VSSSENSE (5)

8/11 change

PR53 *100_4

LE4 B:
Enable Value

8771CSP1
8771CSN12
8771CSP2
8771DH2
8771DL2
8771LX2
BST2_R

PR65 0_6 PC65 0.22U_25V_6 PC31 *1nF_50V_4

8771BST2

PD4 SDM10K45-7-F

8771VDD

PQ32 FDS7088SN3 PQ28 FDS7088SN3 PC58 *1nF_50V_4 *1.5n_50V_6 PC41

PQ20 FDS7088SN3 PQ21 FDS7088SN3 *1.5n_50V_6 PC40

LE4 B:
Change
footprint

PQ33 RQW130N03

PQ29 RQW130N03

LE4 B:
del PC165,PC166,PC55

PR30 *0_6 PR28 *0_6

PL17 0.45_25A_20%_ETQP4LR45XFC

PL15 0.45_25A_20%_ETQP4LR45XFC

PR176 2.1K_F_4 PR177 4.02K_F_4 PR174 NTC 10K_6-B4.25K

PC163 0.22U_10V_6 PR56 0_4

8771CSP1
8771CSN12

Use differential routing away from switch nodes
8771LX1 and 8771LX2

PR32 2.1K_F_4 PR34 4.02K_F_4 PR29 NTC 10K_6-B4.25K

PC47 0.22U_10V_6 PR52

8771CSP2
8771CSN12

Use differential routing away from switch nodes
8771LX1 and 8771LX2

LE4 B:
Change
open-short to
bead

PL21 HI0805R800R-10 PL22 HI0805R800R-10

VIN

+CPU_PWR_SRC

PC157 100U/25V+ PC53 2200P_5X7_4 PC60 10U_25V_1206 X6S_1206 PC72 10U_25V_1206 X6S_1206

LE4 B:
Add PC20 in BOM

VCC_CORE

PC20 PC143 330UF_2V_7mohm PC142 330UF_2V_7mohm 330UF_2V_7mohm_7343 PC12 0.01U_25V_4

distribute evenly between N side and S side, preferably on secondary side.

LE4 B:
Add PC20 in BOM

LE4 B:
Del PC26 parts in BOM

PC141 330UF_2V_7mohm PC19 330UF_2V_7mohm PC26 330UF_2V_7mohm 330UF_2V_7mohm_7343 PC140 0.01U_25V_4

distribute evenly between N side and S side, preferably on secondary side.

LE4 B:
Change
Footprint

PC57 0.1U_50V_6

LE4 B:
del PC48

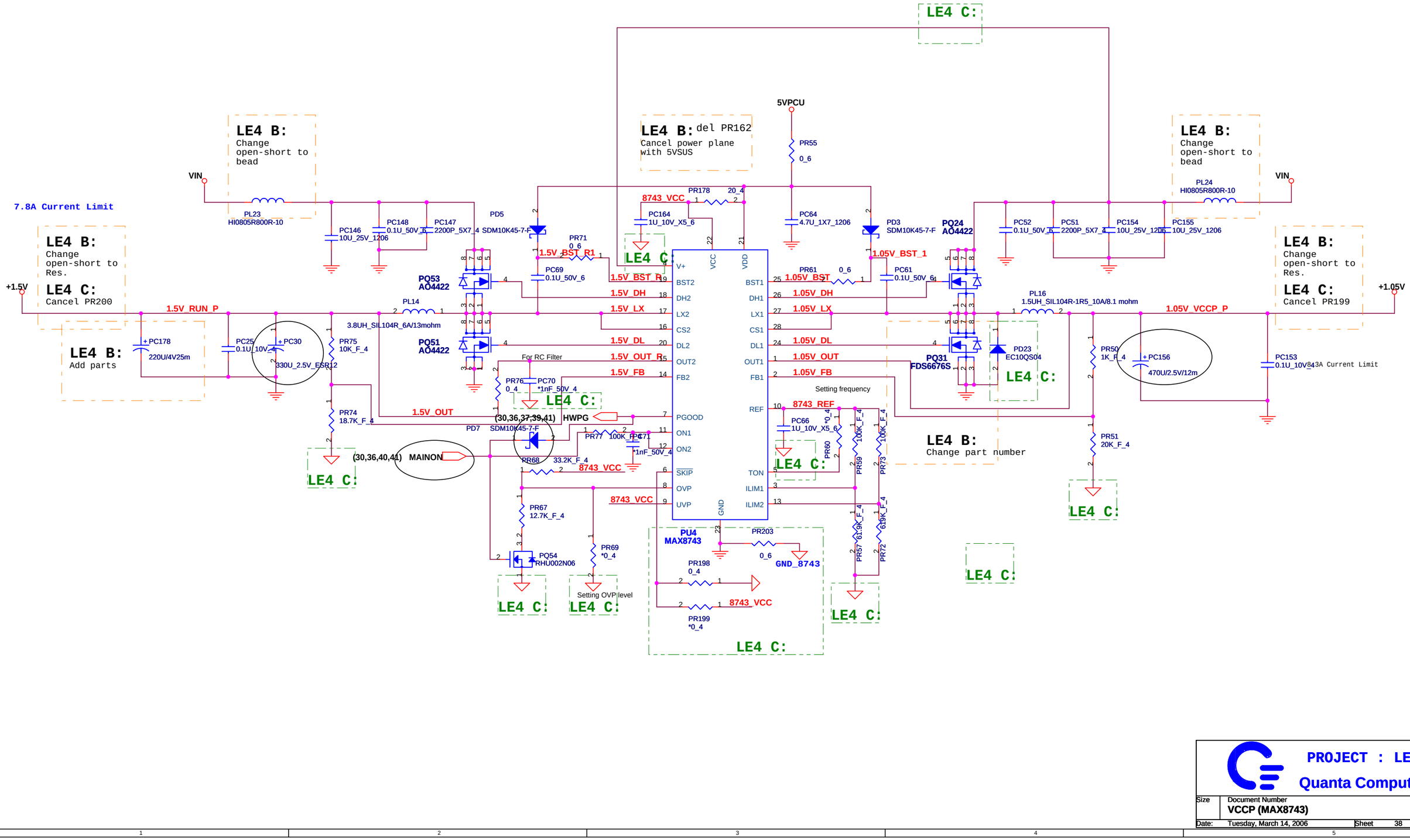
PC74 0.1U_50V_6 PC162 100U/25V+ PC75 2200P_5X7_4 PC73 10U_25V_1206 X6S_1206 PC62 10U_25V_1206 X6S_1206

+CPU_PWR_SRC

Add layout note on pins 22 and 28 of MAX8771 controller. These nets have large voltage swings. Need to route them away from the sensitive areas that are trying to detect small changes in voltage, such as the voltage sense VccSense VssSense lines.

Sense lines are 18 mil wide, Z0=27.4 Ohm.
Use differential routing with 7 mil spacing.
Route external layer with solid GND reference (no split planes).
Use 25 mil separation from any other signal.

PROJECT : LE4		
Quanta Computer Inc.		
Size	Document Number: CPU power MAX8771	Rev: 1A
Date: Tuesday, March 14, 2006	Sheet 37 of 42	



PROJECT : LE4		
Quanta Computer Inc.		
Size	Document Number: VCCP (MAX8743)	Rev: 1A
Date: Tuesday, March 14, 2006	Sheet 38 of 42	

LE4 B: Change open-short to bead

LE4 A-power:

VIN — PL25 HI0805R800R-10 — +DC1_PWR_SRC2

PC43 0.1U_50V_6 — PC33 *10U_25V_1206 — PC34 10U_25V_1206 — PC36 0.1U_50V_6 — PC32 2200P_5X7_4

8734VCC — PR31 47_6 — PC46 1U_10V_X5_6 — PD2 CH501 — PD1 CH501

5V_AL — PC45 4.7U_1X7_8

Place PC78, PC79 as close as possible to PQ25 drain and PQ24 source

LE4 B: Change open-short to bead

LE4 A-power:

VIN — PL26 — PC7 HI0805R800R-10 — 10U_25V_1206 — +DC1_PWR_SRC1

PC9 0.1U_50V_6 — PC8 2200P_5X7_4

PQ10 RSS090N03 — PQ11 RSS090N03

BST_3_1 — BST_5_1

Current Limit at 6.7A

3VPCU

Place PC81, PC82 as close as possible to PQ27 drain and PQ26 source

LE4 B: Change Vaule from 2.5UH to 3.3UH

IND SMD 3.3UH 30% 6.6A — PL2

+3.3V_SUSP — PC14 220U/4V/25m — PC13 0.1U_50V_6 — PR153 *0_4 — PR152 0_4

PQ19 RSS090N03 — PQ15 RSS090N03

PC37 0.1U_50V_6 — PR27 0_6

PR22 0_6 — PC38 0.1U_50V_6

LE4 B: Change Vaule from 2.5UH to 3.3UH

IND SMD 3.3UH 30% 6.6A(PLC-1045-3R3)L-F — PL3

Current Limit at 5.7A

5VPCU — +5V_SUSP — PC16 0.1U_50V_6 — PC10 220U/6.3V/ESR25 — PR160 *0_4 — PR156 0_4

RDS(ON)=20m ohm

RDS(ON)=20m ohm

PU2 MAX8734AEEI+

V+	20	LDO5	18
VCC	17	BST5	14
N.C.	1	DH5	16
BST3	28	LX5	15
DH3	26	DL5	19
LX3	27	OUT5	21
DL3	24	FB5	9
OUT3	22	PRO	10
FB3	7	ILIM5	11
ON3	3	ILIM3	5
ON5	4	REF	8
LDO3	25	TON	13
SKIP	12	GND	23
SHDN	6	PGOOD	2

BST3 DH3 LX3 DL3 FB3 ON5 — BST5 DH5 LX5 DL5 FB5 PRO# ILIM5 ILIM3 8734REF TON

8734REF — PC144 1U_10V_X5_6 — PR163 0_6 — GND_DC/DC

3V_AL — PC44 4.7U_1X7_8 — PR18 *100K_F_4 — HWPG (30,36,37,38,41)

5V_AL — PR23 2K_F_4 — PR21 240K_4 — PC35 *1000P_50V_4

PR148 0_4

LE4 A-power:

PR157 200K_4 — +DC1_PWR_SRC2 — 1999_SHDN# (5)

PC145 0.1U_50V_6 — PR161 100K_F_4

8734VCC — PR159 *0_4

8734VCC — PR158 *0_4

8734REF — REF=2V — PR147 63.4K_F_4 — PR151 63.4K_F_4 — ILIM5 — ILIM3 — PRO# — TON

PR155 0_4 — PR154 0_4 — PR150 91K_F_4 — PR149 63.4K_F_4

LE4 B: add PC150.PC149

Add parts in BOM

Change PC149,PC152 size and Value from 0603 to 0805 and from 0.1 and 4.7u

DL3 — PR162 0_4

PC150 0.01U_50V_6 — PC151 0.01U_50V_6

PD14 BAT54S — PD15 BAT54S

+15V — PC180 0.1U_50V_6 — PC149 4.7U_1X7_8 — PC181 0.1U_50V_6 — PC152 4.7U_1X7_8 — 5VPCU

10V

PROJECT : LE4

Quanta Computer Inc.

Size	Document Number	Rev
	D/D (MAX8734)	1A
Date: Tuesday, March 14, 2006	Sheet 39 of 42	

DISCHARGE

LE4 A:
S5_ON a:

LE4 B:
Cancel Circuit

LE4 A:
S5_ON b:

LE4 B:
Modify discharge circuit
with +3V_S5

LE4 C:
Change power plane from
10V to +15V

LE4 B:
Change Power plane

LE4 A:
modify PQ40

LE4 B:
Change Power plane

LE4 B: add PL28

+15V
+5VRUN
+3VRUN
+2_5VRUN
+1.8VRUN
+VCC_GFX_CORE
+1.22V_GFX_PCIE
PR26 1M_F_6
PR16 22_8
PR100 22_8
PR14 22_8
PR6 22_8
PR98 22_8
PR1 22_8
(30,36,38,41) MAINON
MAINON
PQ23 PDTC144EU
PQ17 2N7002K
PQ44 2N7002K
PQ15 2N7002K
PQ5 2N7002K
PQ42 2N7002K
PQ1 2N7002K
(36) MAIND
PR4 1M_F_6
PQ2 2N7002K
MAIND
PC1 *2200P_5X7_6
5VPCU
PC23 0.1U_10V_4 10V
PQ18 AO4422
+5VRUN (4,10,15,23,26,28,29,30,31,32,36)
3A
+5VRUN
PC24 0.1U_10V_4 10V
3VPCU
PC15 0.1U_10V_4 10V
AO4422 PQ13
+3VRUN (3,5,7,9,10,12,13,14,15,16,17,18,19,20,22,23,26,27,28,30,31,32,33,36,41)
4.5A
+3VRUN
PC17 0.1U_10V_4 10V
PR3 *1M_6

+15V
+1.5V
VCC_CORE
SMDDR_VTERM
+1.05V
PR20 1M_F_6
PR92 22_8
PR13 22_8
PR9 22_8
PR11 22_8
MAINON
PQ52 PDTC144EU
PQ36 2N7002K
PQ12 2N7002K
PQ7 2N7002K
PQ9 2N7002K

200mils
S0-S5
3VPCU
PQ60 SI3456DV
+3V_S5
0.5A
+3V_S5 (4,14,15,30,33,34)
PC175 10U_6.3V_8
PC174 0.1U_25V_6

PL28 HI0805R800R-00
PL1 HI0805R800R-00
+3VRUN
+5VRUN
PR12 0_4
VCNTL 2.5VA
PC29 10U_6.3V_8
PC11 1U_X5_6
PR19 6.34K_F_4
PR17 20K_F_4
VIN VOUT VCNTL NC VREF AGND GND NC GND1 NC
PU1 APL5331
+2.5VA
PC27 1000P_X7_6
PC18 10U_6.3V_8
PC28 10U_6.3V_8
2.5V/ 1A
+2_5VRUN

+15V
+3V_S5
5VPCU
PR5 100K_4
PR99 10K_F_4
PQ3 FDS6676S
PR184 22_8
(30) S5_ON
S5_ON
PQ41 RHU002N06
PQ59 2N7002K

+15V
5VSUS
3VSUS
1.8VSUS
+15V
PR25 1M_F_6
PR35 22_8
PR15 22_8
PR10 22_8
PR24 1M_F_6
SUSON_G
SUSD
(30,36) SUSON
PQ22 PDTC144EU
PQ30 2N7002K
PQ25 2N7002K
PQ8 2N7002K
PQ27 2N7002K
PC39 *2200P_50V_6

3VPCU
PQ14 SI3456DV
3VPCU (12,14,15,22,26,30,31,35,39)
PC21 0.1U_10V_4 10V
3VSUS
1A
3VSUS (13,14,24,25,26,27,28,31)
PC22 0.1U_10V_4 10V
5VPCU
5VPCU
5VPCU (12,15,35,36,38,39)
PC42 0.1U_10V_4 10V
AO4422 PQ26
5VSUS (25,26,31,37,41)
2A
5VSUS
PC54 0.1U_10V_4 10V

PROJECT : LE4
Quanta Computer Inc.

Size	Document Number	Rev
	Discharge Circuit	1A
Date: Tuesday, March 14, 2006	Sheet 40 of 42	

LE4 B: Cancel dot

LE4 B: Change footprint

LE4 C: Change enable type from mainon to +3VRUN

Because it had been fist up with +3VRUN to +VCC_GFX_CORE and 1.8VRUN

1.2V/1.0V 12A

+VCC_GFX_CORE

250 mils

LE4 C: Cancel PR201

LE4 C: Portest diode with ?? reserve.

VIN — PL12 E@HI0805R800R-00 — PL11 E@HI0805R800R-00 — 1993_VIN

PC115 E@10U_25V_1206 — PC104 E@0.1U_50V_6 — PC110 E@10U_25V_1206 — PC108 E@10U_25V_1206

PC111 E@0.1U_50V_6 — PC113 E@2200P_5X7_4

5VSUS — PR117 E@0_6 — PR121 E@20_4 — VGA_P_VCC — PC106 E@1U_X5_6

PD12 E@SDM10K45-7-F — PC105 E@4.7U_1X7_8

PR114 E@0_6 — VGA_BST

PL10 0.56uH/ 1.6m ohm — PL9 *E@2.2UH-HILP-2525CZRZ-2R2-14A/20m ohm — VGA_CORE

PQ47 E@SI7392DP — PC103 E@0.1U_50V_6 — 1993_DH — 1993_LX

PD24 E@EC10QS04 — PC95 E@0.1U_50V_6 — PD10 E@2.4V — PC97 E@330U_2.5V_ESR12 — PC96 E@330U_2.5V_ESR12 — PC98 E@330U_2.5V_ESR12 — PR105 1.62K/F — PD11 E@EC10QS04 — PC99 E@0.22U_10V_6 — 1993_DL

PQ46 E@SI7336ADP — PR109 *E@0_4 — PR103 *E@0_4

VGA_CSP — PR104 1.62K/F

PU6 E@MAX1993ETG

VDD, BST, DH, LX, DL, GND, CSP, CSN, OUT, FB, OVP/UVP, VCC, V+, POK, LSAT, SHDN, GATE, REFIN, OD, GND, GND, GND, GND, GND, TON, REF, SKIP, FBLANK, ILIM

1993_VIN — PR112 *E@10K_4 — PR113 E@0_4 — 1993PG — PR115 *E@0_4 — HWPG (30,36,37,38,39)

+3VRUN — *E@0_4 PR204 — PD26 E@SDM10K45-7-F — PR118 E@100K_4 — MAINON

PR119 E@0_4 — VGA_REFIN — VGA_P_REF — GFX_CORE_CNTRL(19)

PR108 E@75K_F_4 — PR107 E@75K_F_4 — PC100 E@470P_X7_4

PC107 E@0.022u_50V_6

LE4 A: V_PWRCNTL: High(3.3V) = 1.0V Low(0V) = 1.1V

PR106 E@16.9K_F_4 — *0_4 PR116 — VGA_P_REF

PC101 E@1U_10V_X5_6

LE4 A: Add GND pin

PR110 E@100K_F_4 — PR111 E@43.2K_F_4

PC102 E@0.1U_50V_6

LE4 B: Modify value from 127K/F to 43.2K/F

PR120 E@0_6

LE4 B: Change to LF part number

LE4 C: Slove +VCC_GFX_CORE of rippe

VIN — PR101 *E@1M_F_4 — PR125 *E@0_4

LE4 B: Del PR125 in BOM

PQ43 *E@2N7002K — PR102 *E@1M_F_4

MAINON — PQ45 *E@PDTC144EU

PD25 E@SDM10K45-7-F

PU7 E@SC4215

NC0, EN, VIN, NC1, NC2, VO, GND0, GND1, ADJ

(30,36,38,40) MAINON — MAINON — PR200 E@0_4 — PR127 E@120K_4 — EN_4215

+3VRUN — PR201 *E@0_4

PR124 *E@0_4 — PR123 *E@100K_4 — PQ48 *E@MMBT3904 — PR122 *E@43K_F_4 — PC112 *E@0.1U_50V_6

LE4 C: Add +3VRUN and MAINON selector function and fixed circiut for C-test

1.8VSUS — PC114 E@0.22U_50V_6 — PC116 — PC117 E@0.1U_50V_6 — E@10U/X6S_8

4215FB — R1 PR128 E@5.1K_F_4 — R2 PR126 E@10K_F_4

Vo=0.8(R1+R2)/R2

PC119 — PC118 — PC109 E@0.1U_50V_6 — E@10U/X6S_8 — E@10U/X6S_8

LE4 B: 1.22V/ 2A — +1.22V_GFX_PCIE

PROJECT : LE4

Quanta Computer Inc.

Size	Document Number	Rev
	VGA --- MAX1993	1A
Date: Tuesday, March 14, 2006	Sheet 41 of 42	

MODEL	REV	CHANGE LIST		CW3 M/B	
				FROM	TO
CW3 M/B	1A	**0316~0317**	**1. ADD EMI Solution (Per EMI Team suggestion)**	A1A	

PROJECT : LE4

Quanta Computer Inc.

Size	Document Number	Rev
	Change History	1A
Date: Wednesday, November 16, 2005	Sheet 42 of 42	