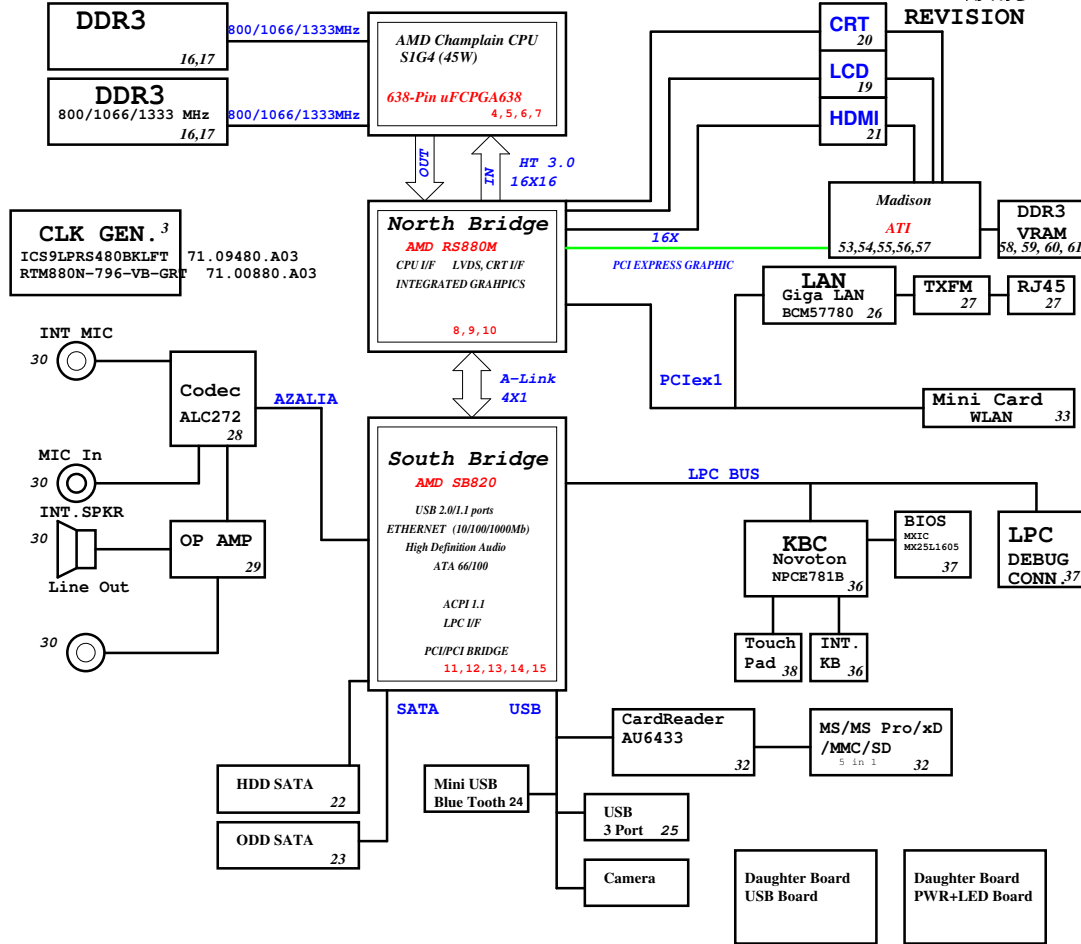


# JV42-DN Block Diagram

Project code: 91.4HD01.001  
 PCB P/N : 48.4GX01.0SA  
 PCB 版號 : 09919 SA  
 REVISION : PCB STACKUP



TOP  
 VCC  
 S  
 S  
 GND  
 BOTTOM

SYSTEM DC/DC RT8223		46
INPUTS	OUTPUTS	
DCBATOUT	5V_S5 (5.5A)	
	3D3V_S5 (5A)	
SYSTEM DC/DC RT8209E		47
5V_S5	1D5V_S3 (1.4A)	
RT9026		47
5V_S5	0D75_S3 (1.2A)	
SYSTEM DC/DC RT8209E		48
DCBATOUT	1D1V_S0 (11A)	
RT9025		48
3D3V_S5	1D1V_S5 (1.4A)	
RT9025		49
3D3V_S0	2D5V_S0 (200mA)	
RT9025		49
1D5V_S3	1D05V_S0 (1.4A)	
CHARGER BQ24745		50
INPUTS	OUTPUTS	
DCBATOUT	CHG_PWR	
	18V 6.0A	
	UP+5V	
	5V 100mA	
CPU DC/DC ISL6265AHR		45
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE_S0	
	0~1.55V 18A	
	VDDNB	
	0~1.55V 4A	

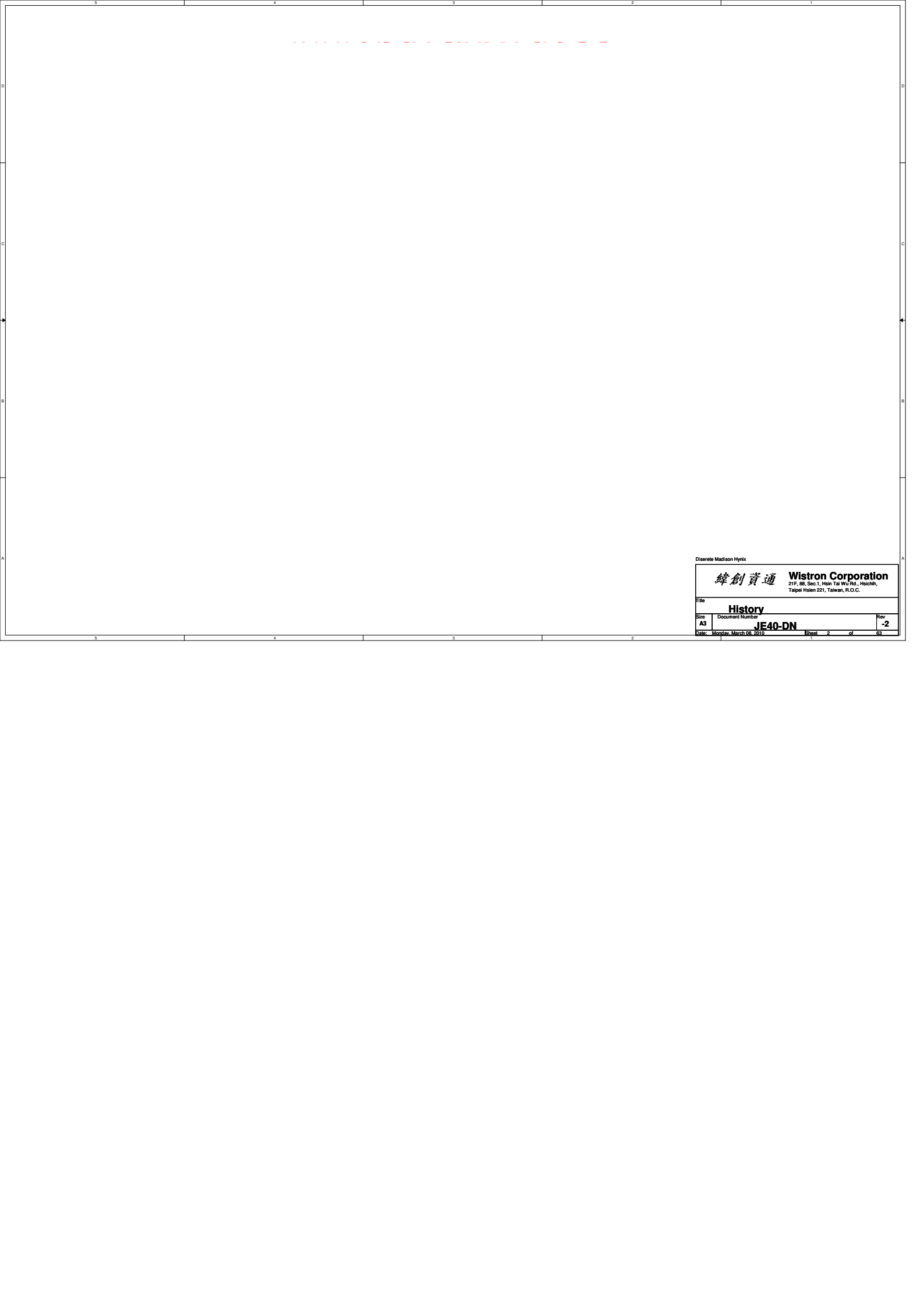
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Title: **BLOCK DIAGRAM**

Size: A3 Document Number: **JE40-DN** Rev: -2

Date: Monday, March 08, 2010 Sheet 1 of 83



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**History**

Size

Document Number

A3

**JE40-DN**

Rev

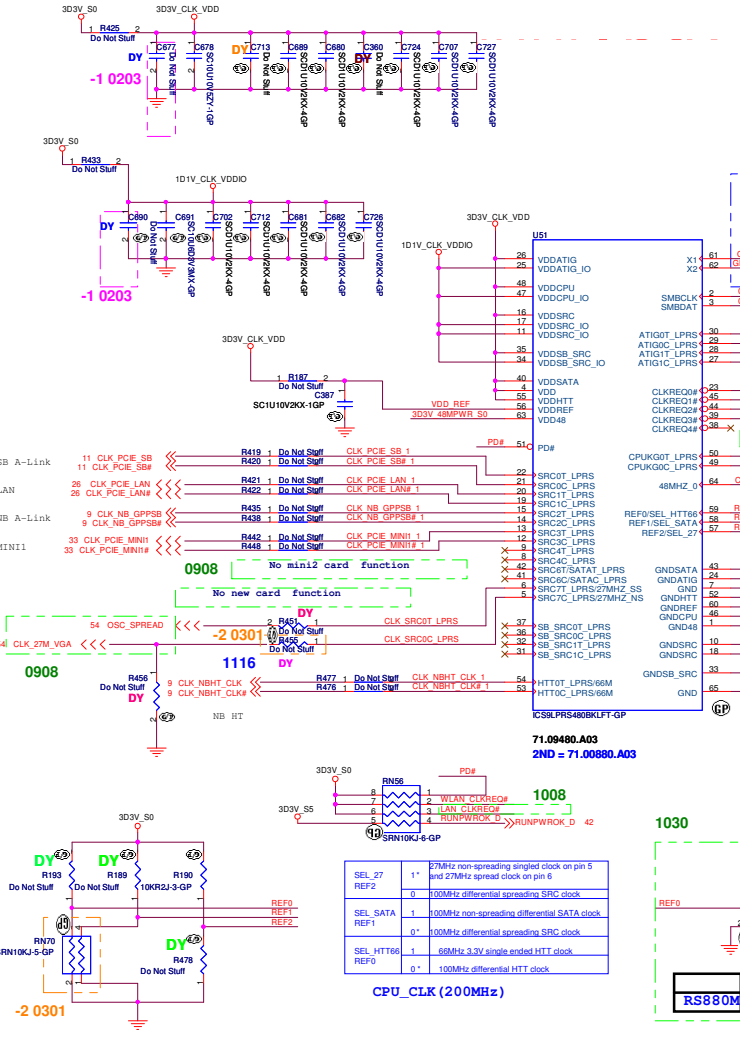
**-2**

Date: Monday, March 08, 2010

Sheet 2 of 93

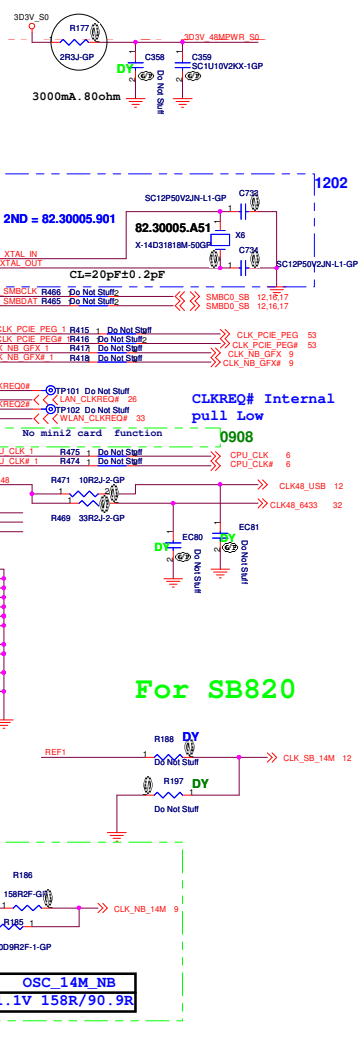
Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



**CPU\_CLK (200MHz)**

SEL_REF2	1*	7MHz non-spreading single clock on pin 5 and 27MHz spread clock on pin 6
SEL_SATA_REF1	0	100MHz differential spreading SRC clock
SEL_HT706_REF0	1	100MHz differential spreading SRC clock
SEL_HT706_REF0	1	68MHz 3.3V single ended HTT clock
SEL_HT706_REF0	0*	100MHz differential HTT clock



**NB CLOCK INPUT TABLE**

NB CLOCKS	RS880M
HT_REFCLKP	100M DFF
HT_REFCLKN	100M DFF
REFCLK_P	14M SE (1.1V)
REFCLK_N	VREF
GFx_REFCLK	100M DFF(IN/OUT)*
GPx_REFCLK	NC or 100M DFF OUTPUT
GPSSB_REFCLK	100M DFF

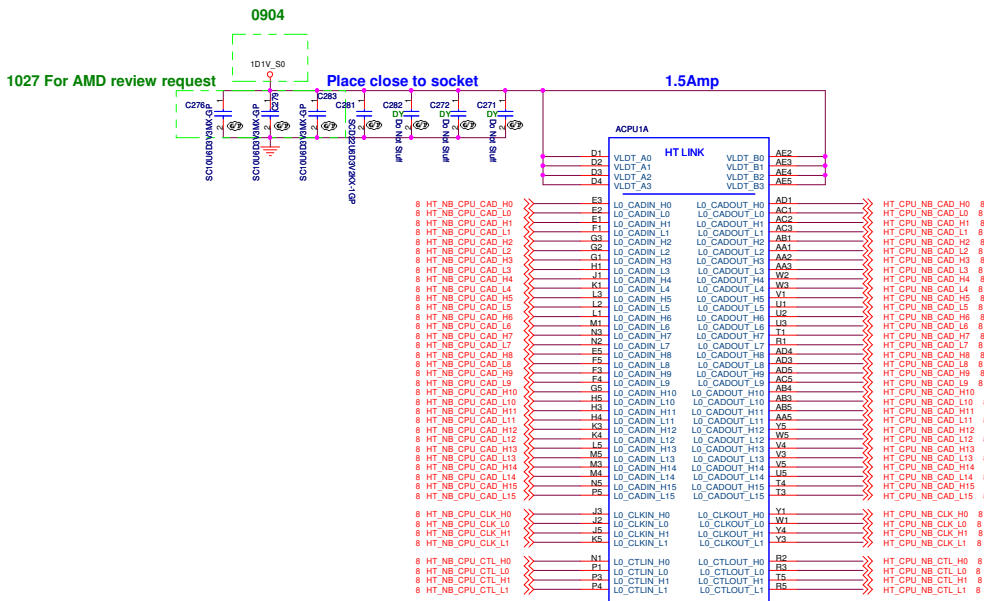
\* RS880M can be used as clock buffer to output two PCIe reference clocks. By default, chip will configured as input mode, BIOS can program it to output mode.

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File	<b>CLKGEN ICS9LPRS480</b>		
Size	A3	Document Number	<b>JE40-DN</b>
Date	Monday, March 08, 2010	Sheet	3 of 83

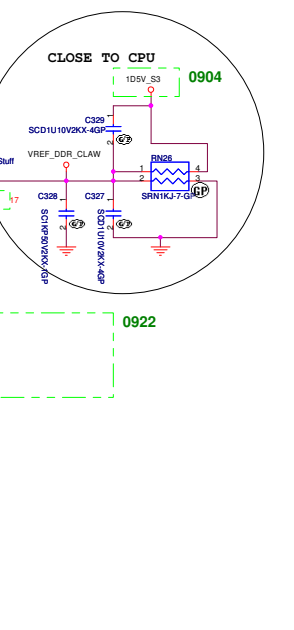
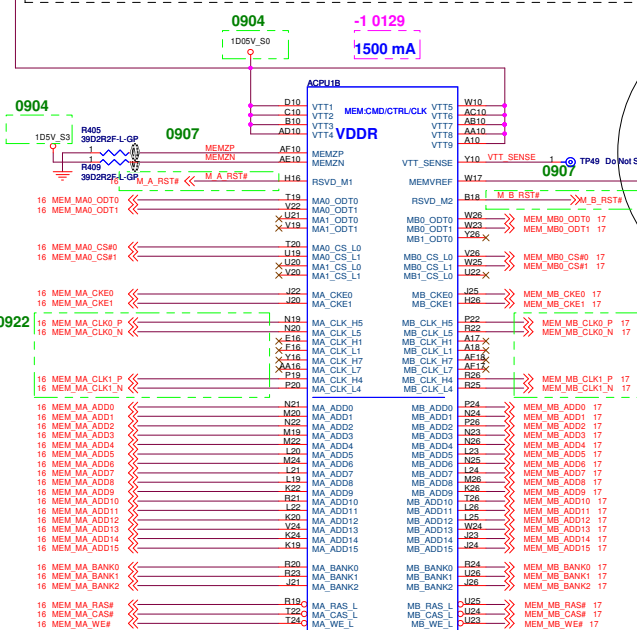
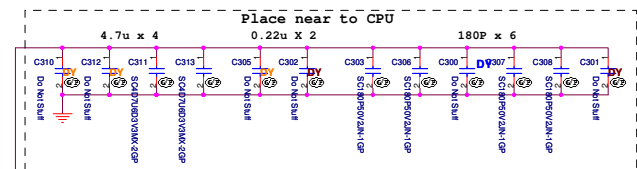
Rev -2



SKT-CPU638P-GP-U2  
**62-10055.111**  
 2ND = 62.10055.181(ENG 未上)  
**SKT-BGA638H176**

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<b>CPU HT LINK I/F (1/4)</b>	
Size	Rev
A3	-2
<b>JE40-DN</b>	
Date: Monday, March 08, 2010	Sheet 4 of 83



MEMDATA	MEMDATA	MEMDATA
MB_DATA0	G11	MEM_MB_DATA0 17
MB_DATA1	A14	MEM_MB_DATA1 17
MB_DATA2	B14	MEM_MB_DATA2 17
MB_DATA3	G11	MEM_MB_DATA3 17
MB_DATA4	B11	MEM_MB_DATA4 17
MB_DATA5	E11	MEM_MB_DATA5 17
MB_DATA6	A13	MEM_MB_DATA6 17
MB_DATA7	A13	MEM_MB_DATA7 17
MB_DATA8	A16	MEM_MB_DATA8 17
MB_DATA9	A16	MEM_MB_DATA9 17
MB_DATA10	A20	MEM_MB_DATA10 17
MB_DATA11	A20	MEM_MB_DATA11 17
MB_DATA12	C14	MEM_MB_DATA12 17
MB_DATA13	C18	MEM_MB_DATA13 17
MB_DATA14	C18	MEM_MB_DATA14 17
MB_DATA15	A23	MEM_MB_DATA15 17
MB_DATA16	A23	MEM_MB_DATA16 17
MB_DATA17	D21	MEM_MB_DATA17 17
MB_DATA18	D21	MEM_MB_DATA18 17
MB_DATA19	C25	MEM_MB_DATA19 17
MB_DATA20	C25	MEM_MB_DATA20 17
MB_DATA21	C29	MEM_MB_DATA21 17
MB_DATA22	C29	MEM_MB_DATA22 17
MB_DATA23	D24	MEM_MB_DATA23 17
MB_DATA24	D24	MEM_MB_DATA24 17
MB_DATA25	G25	MEM_MB_DATA25 17
MB_DATA26	G25	MEM_MB_DATA26 17
MB_DATA27	C28	MEM_MB_DATA27 17
MB_DATA28	C28	MEM_MB_DATA28 17
MB_DATA29	C26	MEM_MB_DATA29 17
MB_DATA30	C26	MEM_MB_DATA30 17
MB_DATA31	A24	MEM_MB_DATA31 17
MB_DATA32	A24	MEM_MB_DATA32 17
MB_DATA33	A23	MEM_MB_DATA33 17
MB_DATA34	A23	MEM_MB_DATA34 17
MB_DATA35	A26	MEM_MB_DATA35 17
MB_DATA36	A26	MEM_MB_DATA36 17
MB_DATA37	A26	MEM_MB_DATA37 17
MB_DATA38	A26	MEM_MB_DATA38 17
MB_DATA39	A22	MEM_MB_DATA39 17
MB_DATA40	A22	MEM_MB_DATA40 17
MB_DATA41	A20	MEM_MB_DATA41 17
MB_DATA42	A20	MEM_MB_DATA42 17
MB_DATA43	A20	MEM_MB_DATA43 17
MB_DATA44	A23	MEM_MB_DATA44 17
MB_DATA45	A23	MEM_MB_DATA45 17
MB_DATA46	A20	MEM_MB_DATA46 17
MB_DATA47	A20	MEM_MB_DATA47 17
MB_DATA48	A23	MEM_MB_DATA48 17
MB_DATA49	A23	MEM_MB_DATA49 17
MB_DATA50	A23	MEM_MB_DATA50 17
MB_DATA51	A23	MEM_MB_DATA51 17
MB_DATA52	A23	MEM_MB_DATA52 17
MB_DATA53	A23	MEM_MB_DATA53 17
MB_DATA54	A23	MEM_MB_DATA54 17
MB_DATA55	A23	MEM_MB_DATA55 17
MB_DATA56	A23	MEM_MB_DATA56 17
MB_DATA57	A23	MEM_MB_DATA57 17
MB_DATA58	A23	MEM_MB_DATA58 17
MB_DATA59	A23	MEM_MB_DATA59 17
MB_DATA60	A23	MEM_MB_DATA60 17
MB_DATA61	A23	MEM_MB_DATA61 17
MB_DATA62	A23	MEM_MB_DATA62 17
MB_DATA63	A23	MEM_MB_DATA63 17
MB_DATA64	A23	MEM_MB_DATA64 17
MB_DATA65	A23	MEM_MB_DATA65 17
MB_DATA66	A23	MEM_MB_DATA66 17
MB_DATA67	A23	MEM_MB_DATA67 17
MB_DATA68	A23	MEM_MB_DATA68 17
MB_DATA69	A23	MEM_MB_DATA69 17
MB_DATA70	A23	MEM_MB_DATA70 17
MB_DATA71	A23	MEM_MB_DATA71 17
MB_DATA72	A23	MEM_MB_DATA72 17
MB_DATA73	A23	MEM_MB_DATA73 17
MB_DATA74	A23	MEM_MB_DATA74 17
MB_DATA75	A23	MEM_MB_DATA75 17
MB_DATA76	A23	MEM_MB_DATA76 17
MB_DATA77	A23	MEM_MB_DATA77 17
MB_DATA78	A23	MEM_MB_DATA78 17
MB_DATA79	A23	MEM_MB_DATA79 17
MB_DATA80	A23	MEM_MB_DATA80 17
MB_DATA81	A23	MEM_MB_DATA81 17
MB_DATA82	A23	MEM_MB_DATA82 17
MB_DATA83	A23	MEM_MB_DATA83 17
MB_DATA84	A23	MEM_MB_DATA84 17
MB_DATA85	A23	MEM_MB_DATA85 17
MB_DATA86	A23	MEM_MB_DATA86 17
MB_DATA87	A23	MEM_MB_DATA87 17
MB_DATA88	A23	MEM_MB_DATA88 17
MB_DATA89	A23	MEM_MB_DATA89 17
MB_DATA90	A23	MEM_MB_DATA90 17
MB_DATA91	A23	MEM_MB_DATA91 17
MB_DATA92	A23	MEM_MB_DATA92 17
MB_DATA93	A23	MEM_MB_DATA93 17
MB_DATA94	A23	MEM_MB_DATA94 17
MB_DATA95	A23	MEM_MB_DATA95 17
MB_DATA96	A23	MEM_MB_DATA96 17
MB_DATA97	A23	MEM_MB_DATA97 17
MB_DATA98	A23	MEM_MB_DATA98 17
MB_DATA99	A23	MEM_MB_DATA99 17
MB_DATA100	A23	MEM_MB_DATA100 17

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 2ND = 62.10055.181

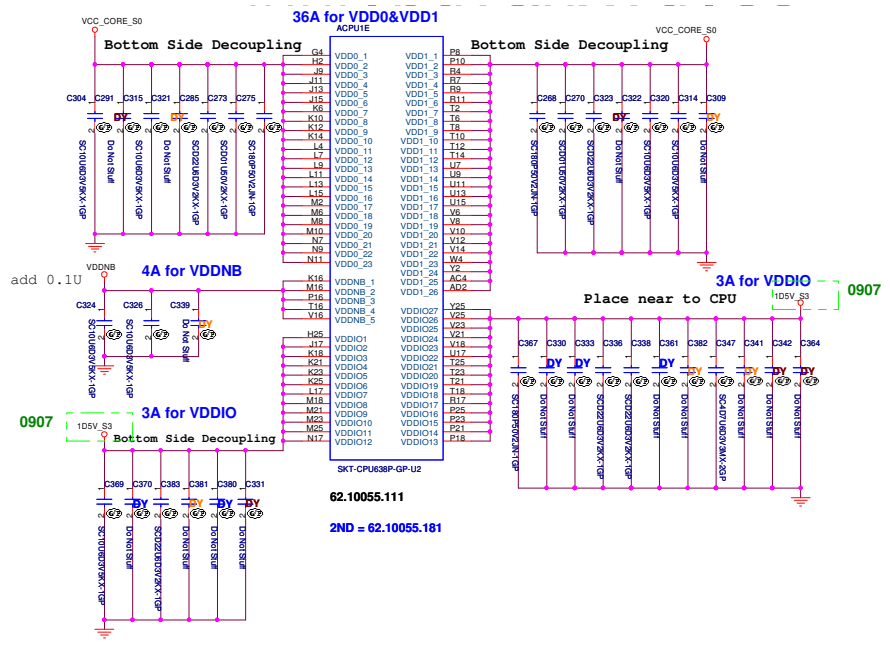
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 Discrete Madison Hynix  
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File	CPU DDR (2/4)	
Size	Document Number	Rev
A3	JE4Q-DN	-2
Date:	Monday, March 08, 2010	Sheet 5 of 83



ACPUHF		
AA4	VSS1	VSS66
AA11	VSS2	VSS67
AA12	VSS3	VSS68
AA15	VSS4	VSS69
AA17	VSS5	VSS70
AA19	VSS6	VSS71
AB0	VSS7	VSS72
AB7	VSS8	VSS73
AB9	VSS9	VSS74
AB23	VSS10	VSS75
AC11	VSS11	VSS76
AC12	VSS12	VSS77
AC13	VSS13	VSS78
AC17	VSS14	VSS79
AC19	VSS15	VSS80
AC21	VSS16	VSS81
AD0	VSS17	VSS82
AD8	VSS18	VSS83
AD9	VSS19	VSS84
AD25	VSS20	VSS85
AE13	VSS21	VSS86
AE15	VSS22	VSS87
AE19	VSS23	VSS88
AE19	VSS24	VSS89
AE19	VSS25	VSS90
AE23	VSS26	VSS91
AE23	VSS27	VSS92
BE	VSS28	VSS93
BE	VSS29	VSS94
BE	VSS30	VSS95
BE	VSS31	VSS96
BE	VSS32	VSS97
BE	VSS33	VSS98
BE	VSS34	VSS99
BE	VSS35	VSS100
BE	VSS36	VSS101
BE	VSS37	VSS102
BE	VSS38	VSS103
BE	VSS39	VSS104
BE	VSS40	VSS105
BE	VSS41	VSS106
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BE	VSS55	VSS120
BE	VSS56	VSS121
BE	VSS57	VSS122
BE	VSS58	VSS123
BE	VSS59	VSS124
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BE	VSS65	VSS130



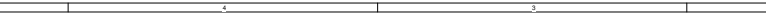
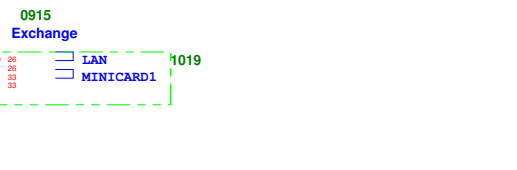
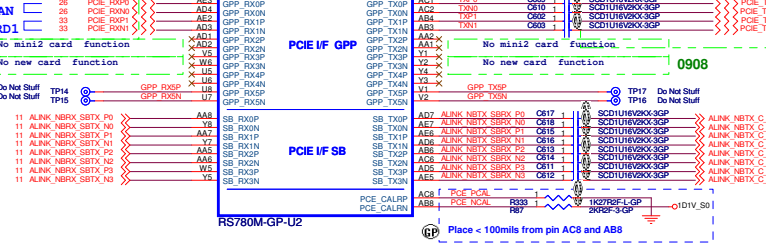
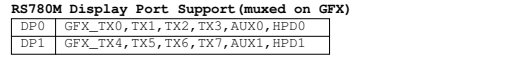
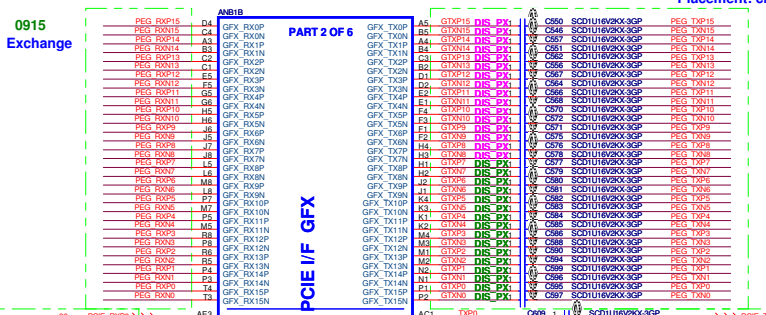
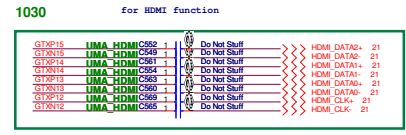
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Taipei Hsien 221, Taiwan, R.O.C.

File: **CPU\_Power\_(4/4)**

Size: A3 Document Number: **JE40-DN** Rev: **-2**

Date: Monday, March 08, 2010 Sheet 7 of 83



Discrete Media System

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei 30001, Taiwan, R.O.C.

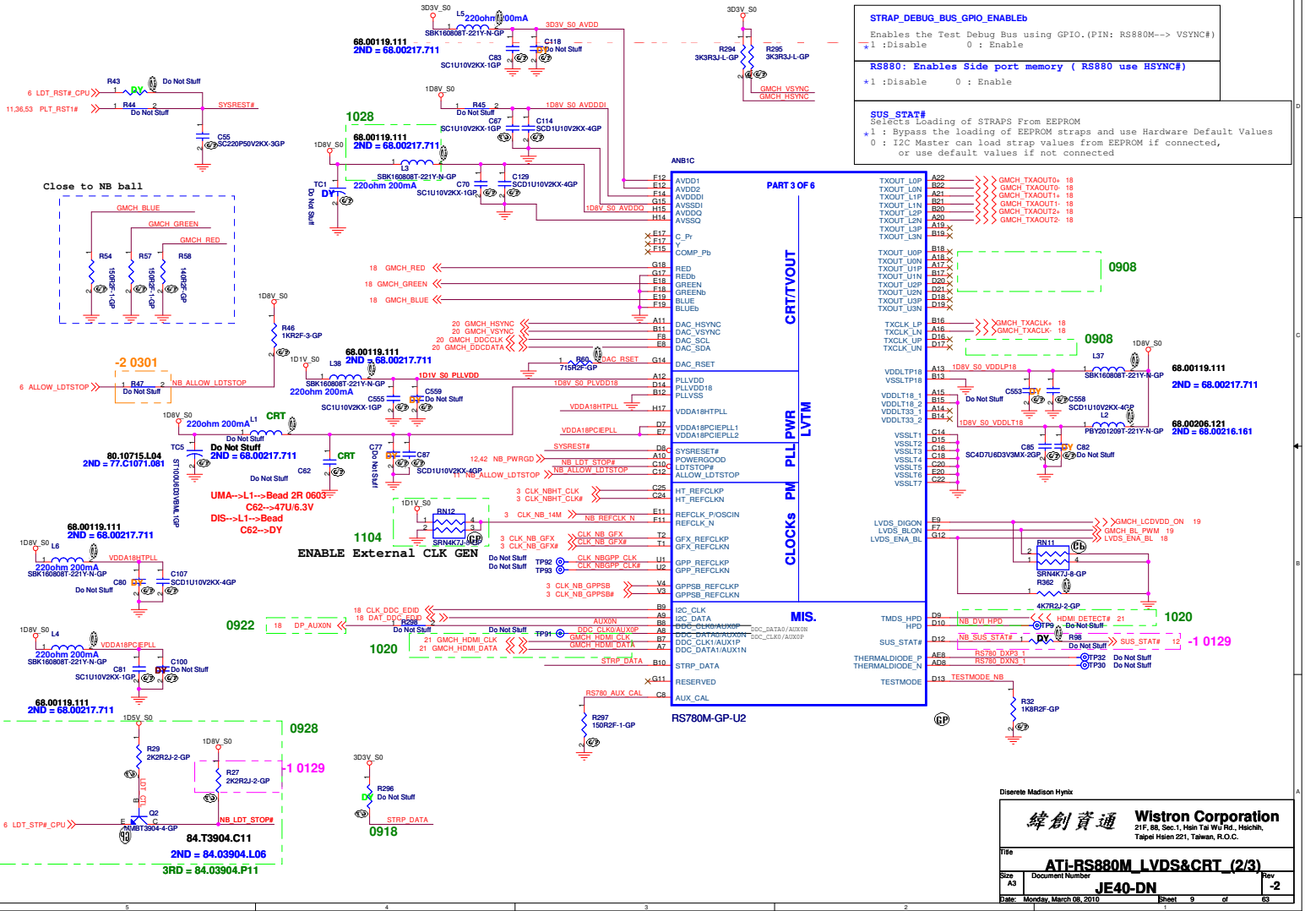
Part: **ATI-RS880M\_HT LINK&PCIE(1/3)**

Doc: **JE40-DN**

Date: Monday, March 08, 2010

Sheet 8 of 83



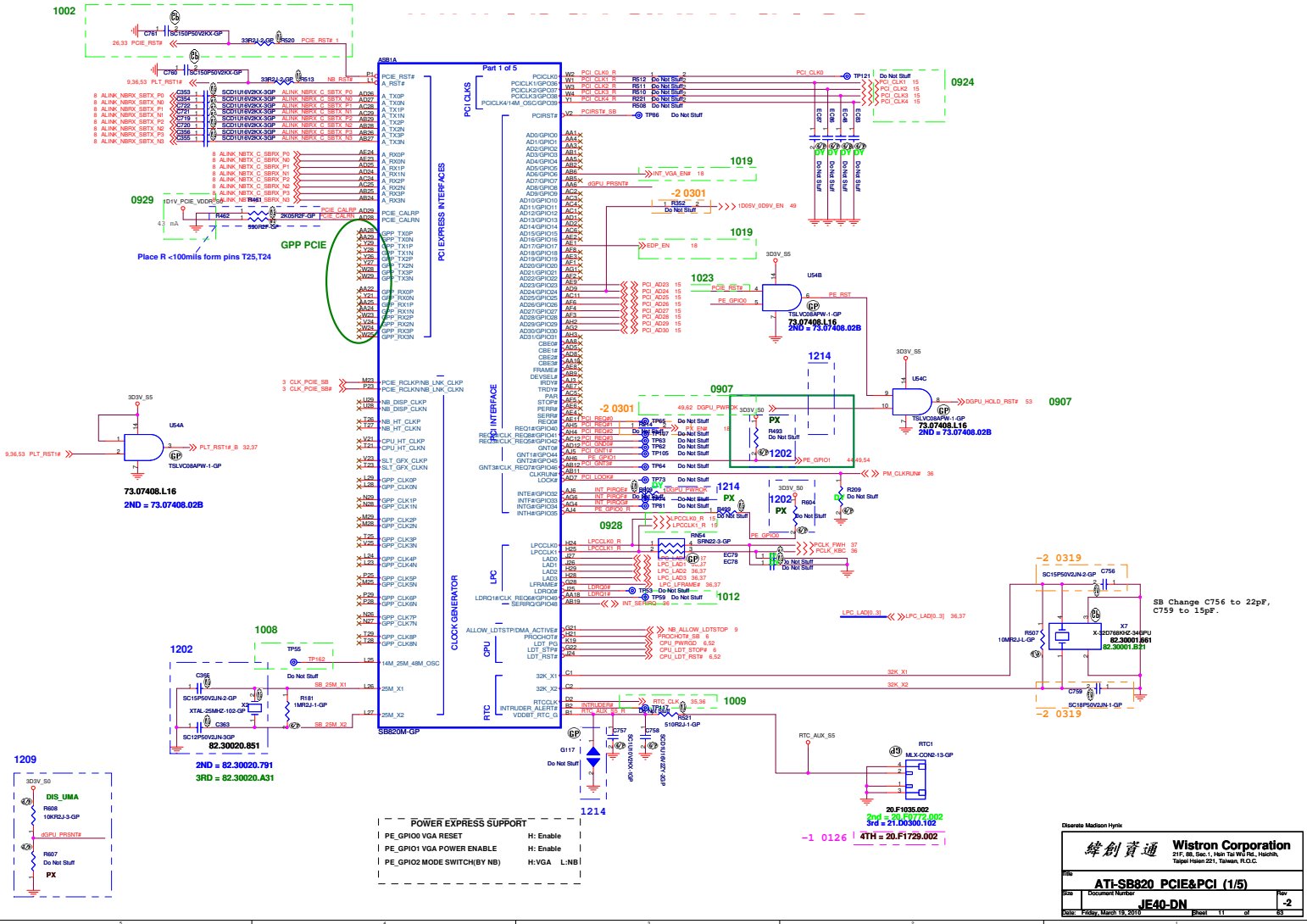


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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 321, Taiwan, R.O.C.

File: AT-RS880M\_LVDS&CRT (2/3)  
 Size: A3 Document Number: JE40-DN Rev: -2  
 Date: Monday, March 08, 2010 Sheet 9 of 83





POWER EXPRESS SUPPORT

PE_GPI00 VGA RESET	H: Enable
PE_GPI01 VGA POWER ENABLE	H: Enable
PE_GPI02 MODE SWITCH (BY NB)	H-VGA L-NB

Discrete Median Name

**緯創資通** Wistron Corporation

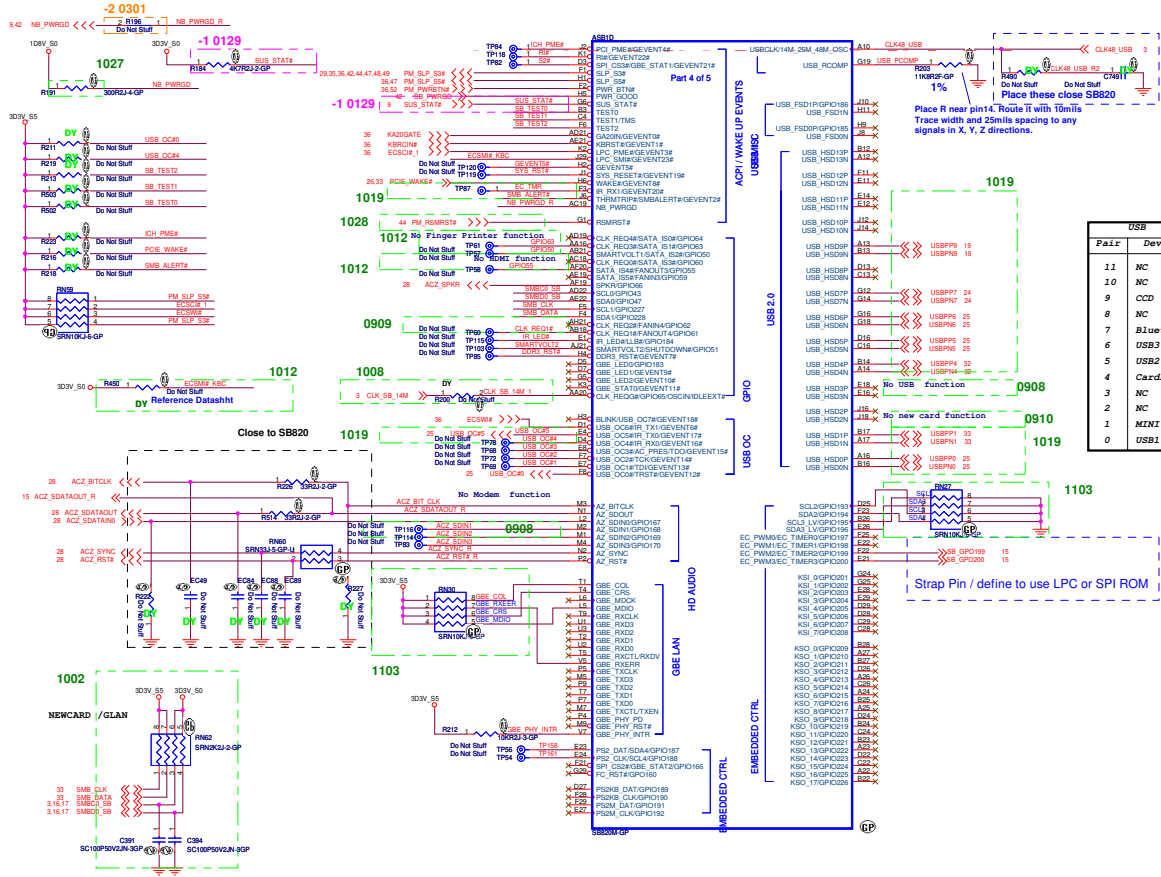
21F, 88, Sec.1, Hsin-Tai Rd. Hsinchu, Taipei Hsinchu, Taiwan, R.O.C.

Doc: **ATI-SB820 PCIE&PCI (1/5)**

Document Number: **JE40-DN**

Rev: **2**

Date: **Feb 18, 2010** | Page: **11** of **81**



Pair#	Device
11	NC
10	NC
9	CCD
8	NC
7	Bluetooth
6	USB3
5	USB2
4	CardReader
3	NC
2	NC
1	MINI CARD
0	USB1

OCF5#  
OCF0#

Strap Pin / define to use LPC or SPI ROM

Discrete Madson Hytec

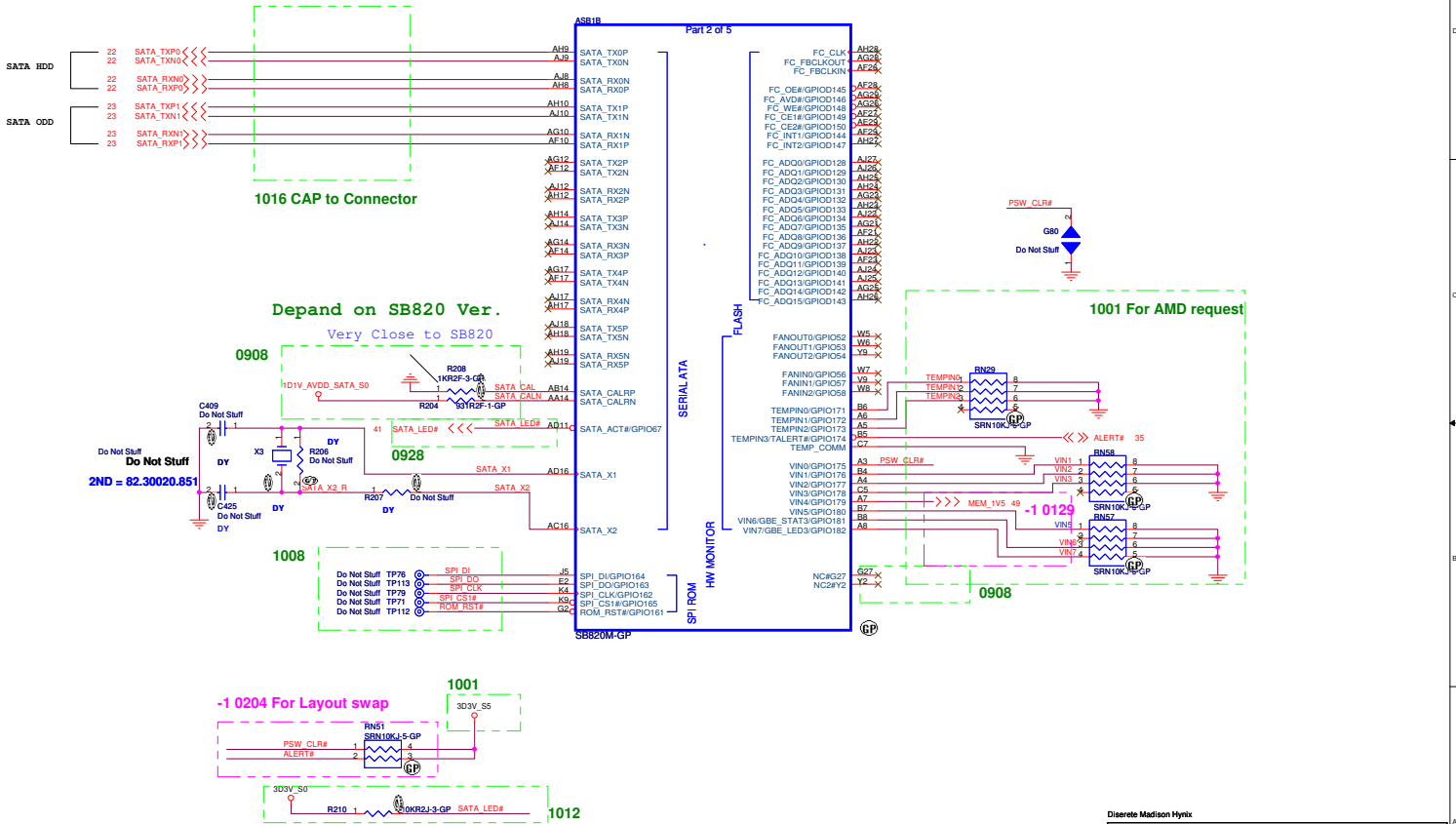
**緯創資通** **Wistron Corporation**  
31F, No. Sec. 1, Hsin-Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

File: **ATI-SB820 USB&GPIO (2/5)**

Doc: Document Number

Rev: **JE40-DN**

Date: Monday, March 08, 2010 Sheet 12 of 81



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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

File: **ATI-SB820 SATA-IDE (3/5)**

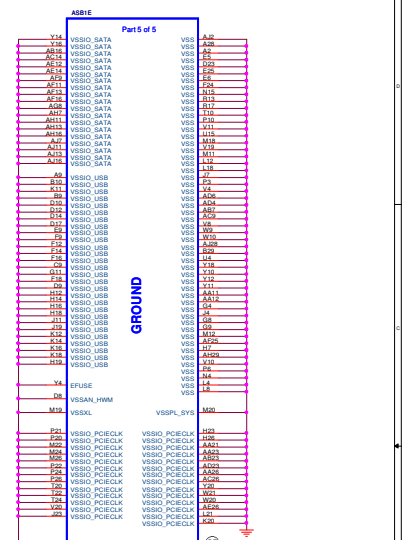
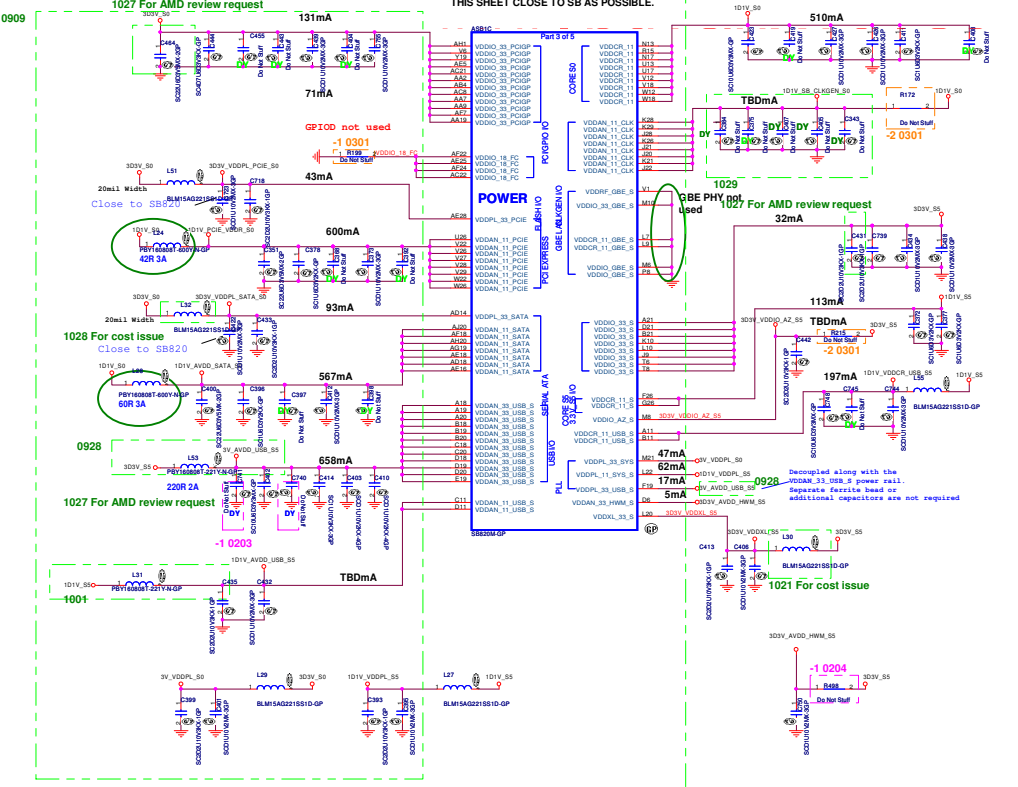
Size: **A3** Document Number: **JE40-DN** Rev: **-2**

Date: **Monday, March 08, 2010** Sheet **13** of **63**

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

0909

0909



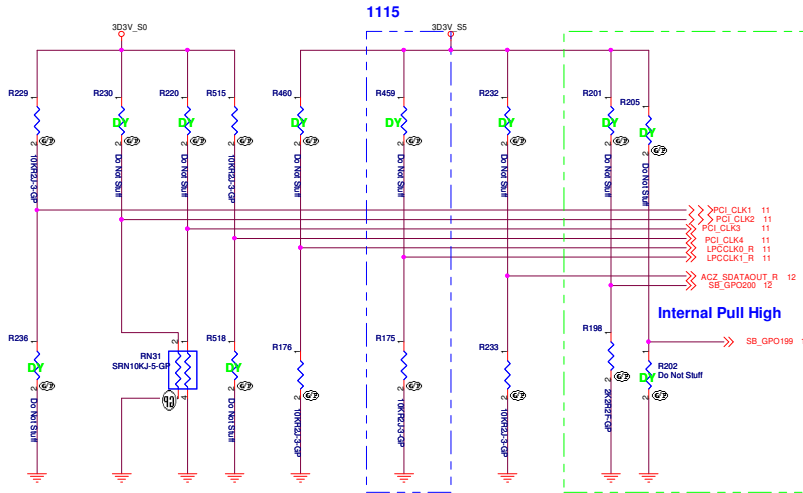
GROUND

Drawn: Madhu Hyva

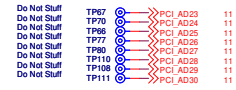
AT1-SB820 POWER&GND (4/5)
Revision: 1
Changes: JE40-DN
Date: 2010-03-03 2010 Sheet 11 of 31 -2

## REQUIRED STRAPS

### REQUIRED SYSTEM STRAPS



## DEBUG STRAPS

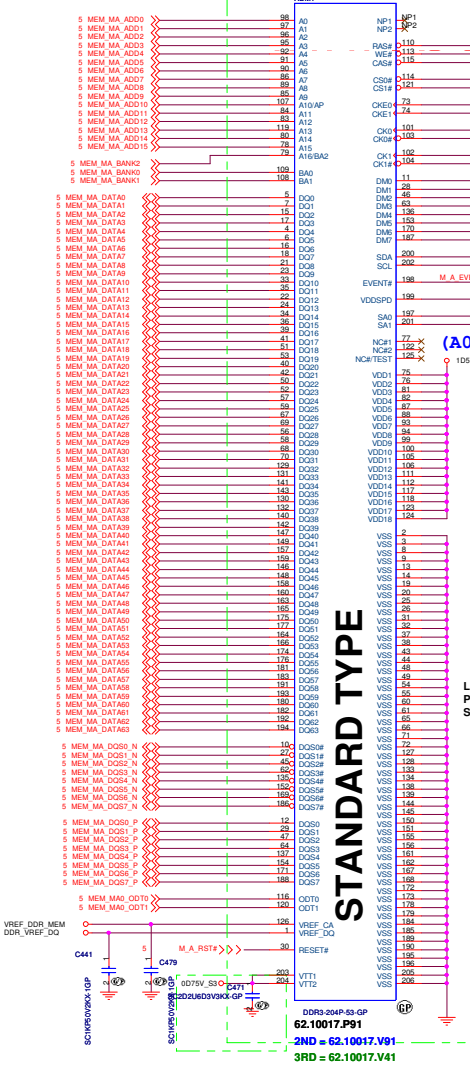


	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_SDOUT	GPIO200	GPIO199
<b>PULL HIGH</b>	ALLOW PCIE Gen2 <small>DEFAULT</small>	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE <small>DEFAULT</small>	EC ENABLED <small>DEFAULT</small>	CLKGEN ENABLED <small>DEFAULT</small>	LOW POWER MODE	H,H = Reserved H,L = SPI ROM	
<b>PULL LOW</b>	FORCE PCIE Gen1	Watchdog Timer Disabled <small>DEFAULT</small>	IGNORE DEBUG STRAP <small>DEFAULT</small>	FUSION CLOCK MODE	EC DISABLED	CLKGEN DISABLED	PERFORMANCE MODE <small>DEFAULT</small>	L,H = LPC ROM (Default) L,L = FWH ROM	

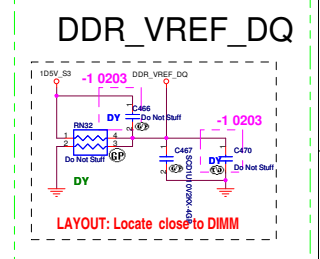
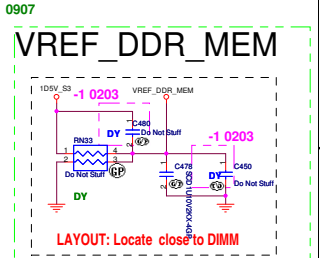
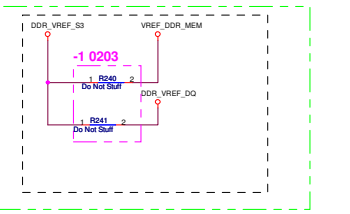
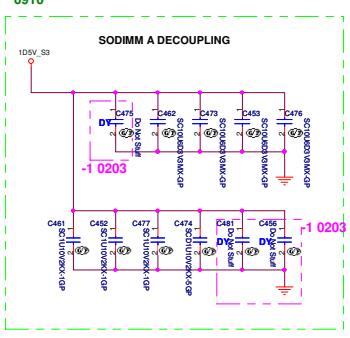
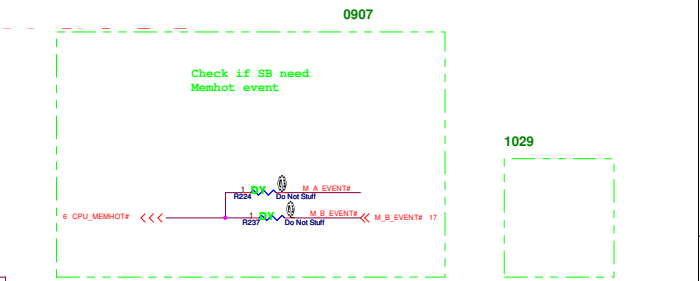
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE PCI PLL <small>DEFAULT</small>	DISABLE ILA AUTORUN <small>DEFAULT</small>	USE FC PLL <small>DEFAULT</small>	USE DEFAULT PCIE STRAPS <small>DEFAULT</small>	DISABLE PCI MEM BOOT <small>DEFAULT</small>
<b>PULL LOW</b>	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

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<b>緯創資通</b>		<b>Wistron Corporation</b> <small>21F, 88, Sec.1, Hsin-Tai Wu Rd., Hsueh, Taipei Hsien 221, Taiwan, R.O.C.</small>	
File			
<b>ATI-SB820 STRAPPING (5/5)</b>			
Size	Document Number		Rev
<b>A3</b>	<b>JE40-DN</b>		<b>-2</b>
Date:	Monday, March 08, 2010	Sheet	15 of 83



Layout Note:  
Place these Caps near  
SO-DIMMA.

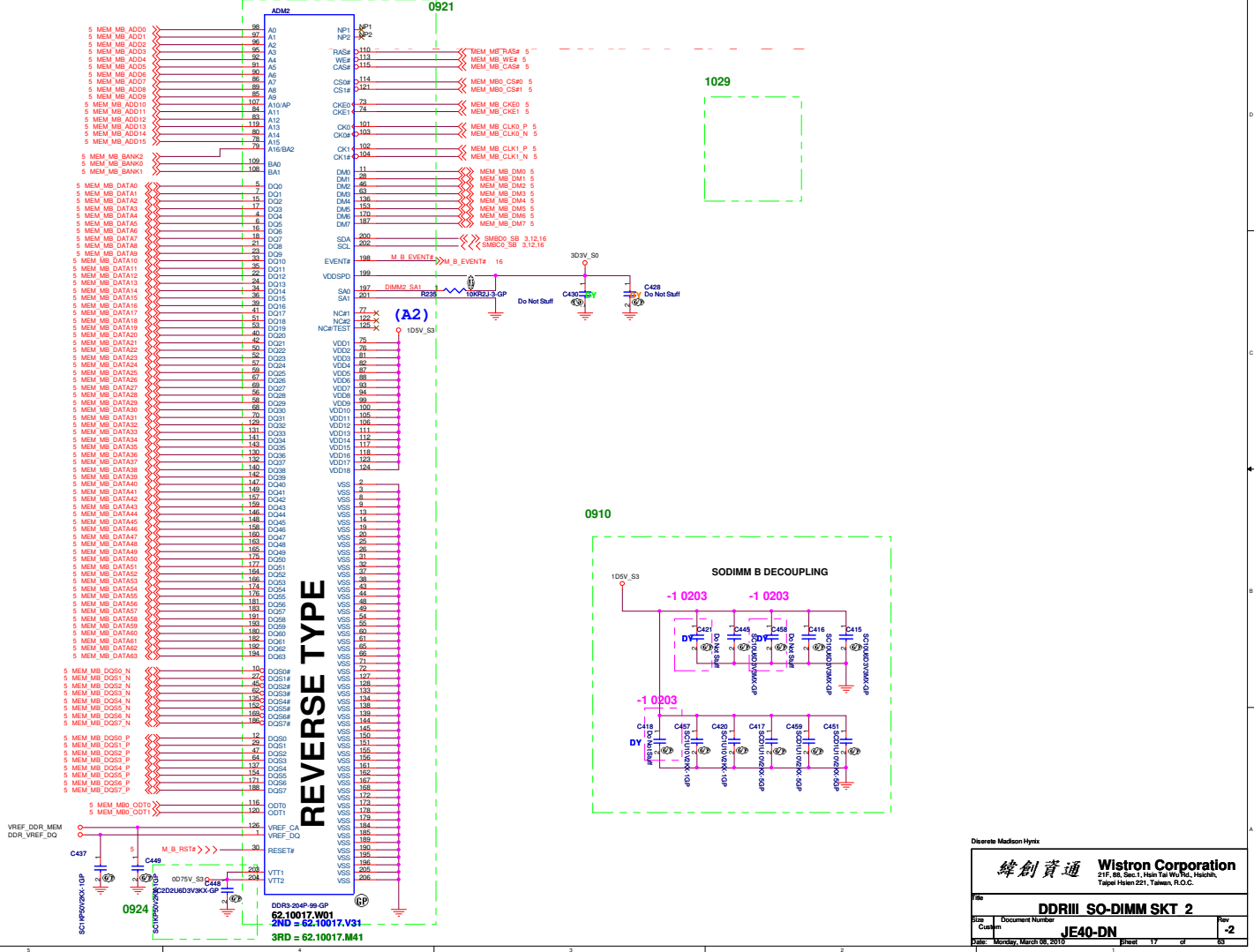


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File	<b>DDRIII SO-DIMM SKT 1</b>		Rev
Sheet	Document Number		-2
Class	<b>JE40-DN</b>		
Date	Monday, March 08, 2010	Sheet	15 of 53





**REVERSE TYPE**

Discrete Madison Hyix

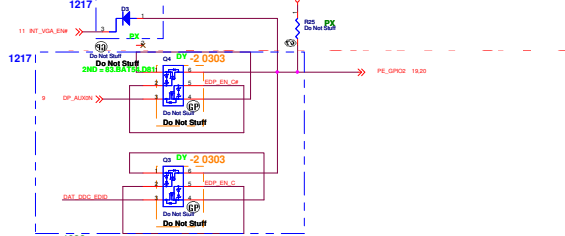
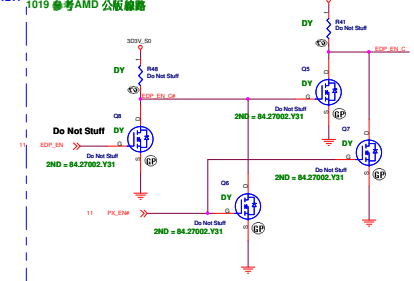
**緯創資通** **Wistron Corporation**  
 217, 8F, Sec.1, Hsin Fu Rd, Taipei, Taiwan, R.O.C.

File: **DDRIII SO-DIMM SKT 2**

Site: \_\_\_\_\_ Document Number: \_\_\_\_\_ Rev: **-2**

Customer: **JE40-DN**

Date: Monday, March 08, 2010 Sheet 17 of 88



**Truth Table**

Function	SEL
A <sub>N</sub> to N <sub>B</sub> 1	L
A <sub>N</sub> to N <sub>B</sub> 2	H

**CRT**

F	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S=0
L	H	IA1	IB1	IC1	ID1	S=1

**Function Table**

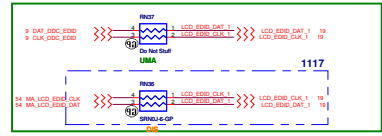
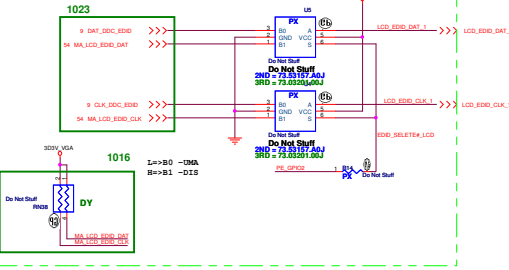
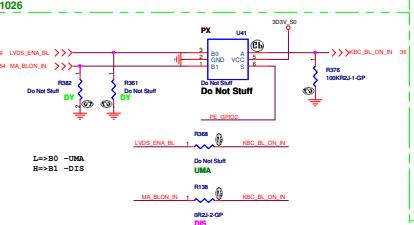
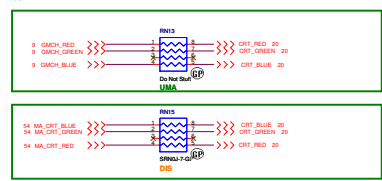
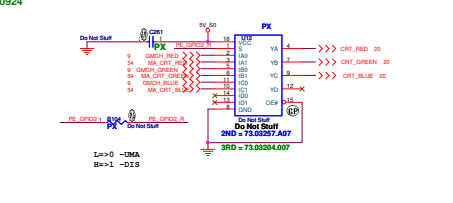
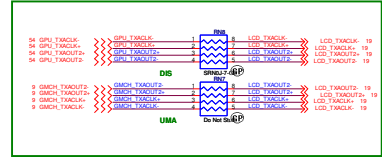
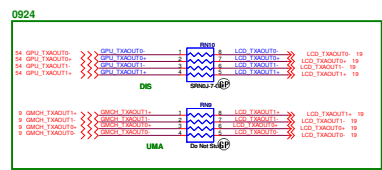
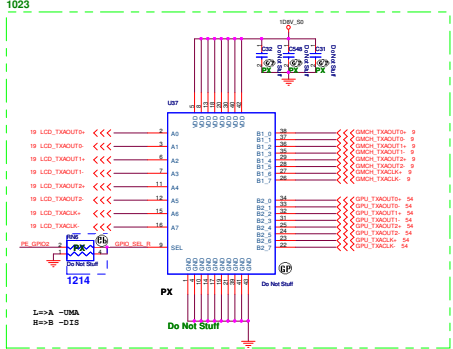
Input (S)	Function
L	B <sub>0</sub> Connected to A
H	B <sub>1</sub> Connected to A

H = HIGH Logic Level L = LOW Logic Level

**Function Table**

Input (S)	Function
L	B <sub>0</sub> Connected to A
H	B <sub>1</sub> Connected to A

H = HIGH Logic Level L = LOW Logic Level



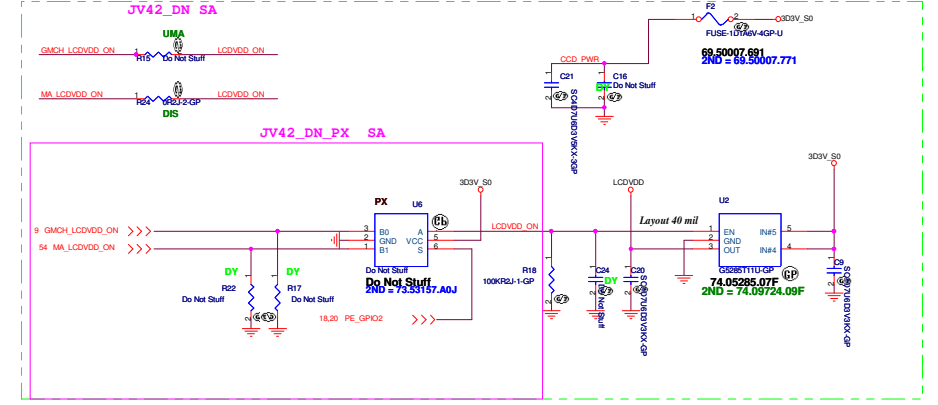
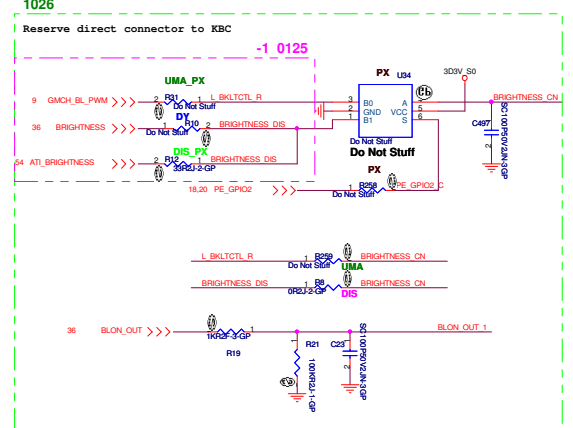
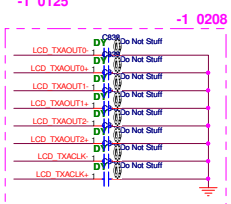
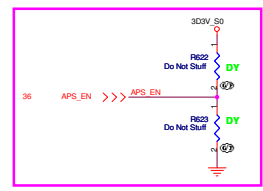
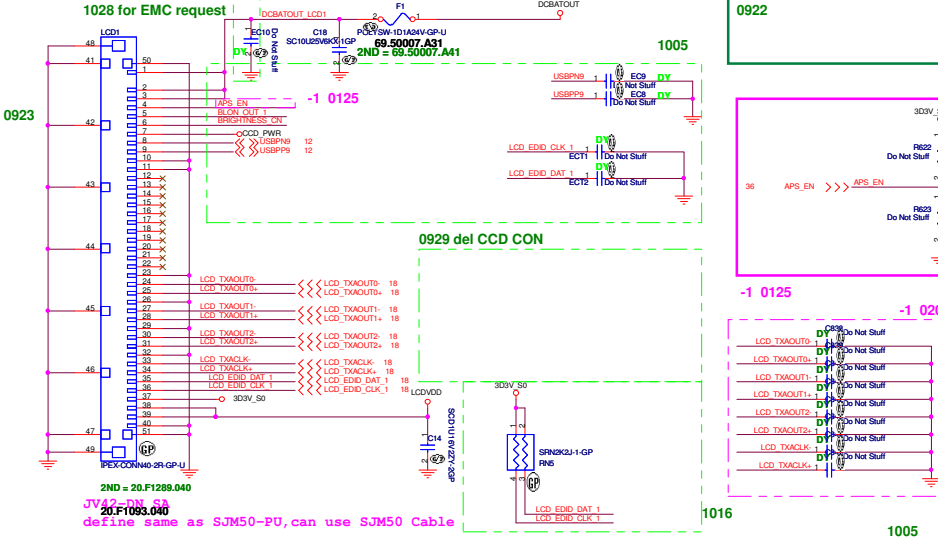
# LCD/INVERTER/CCD CONN

Change PX  
0922

Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND



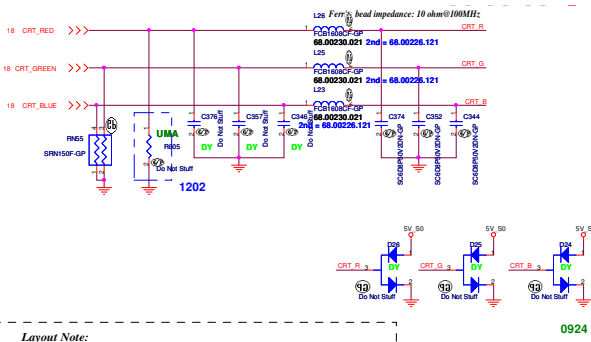
Discrete Medicom Hyink

**緯創資通 Wistron Corporation**

21F, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 301, Taiwan, R.O.C.

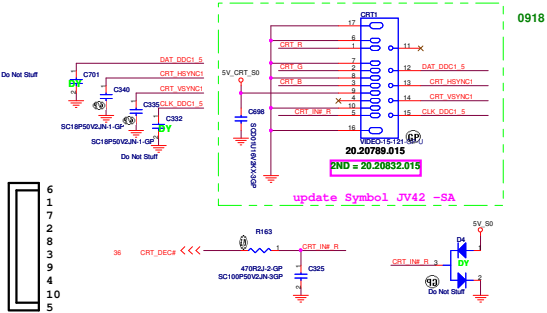
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Doc	Document Number		
Custom			
Part	<b>JE40-DN</b>	Rev	<b>-2</b>
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Check Value  
Place Value resistance  
close to the CRT-conn  
connection



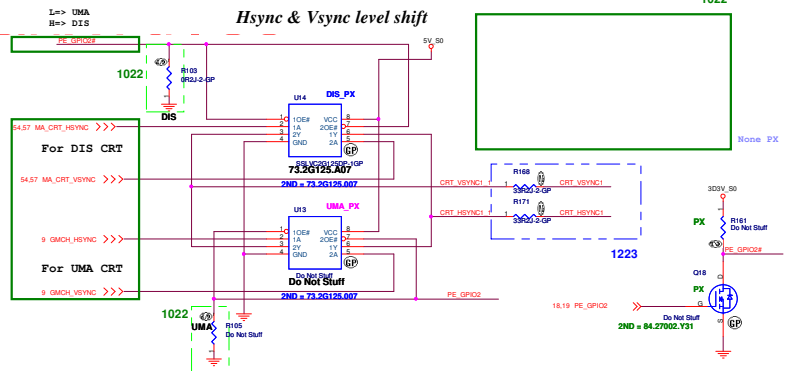
0924

### CRT I/F & CONNECTOR



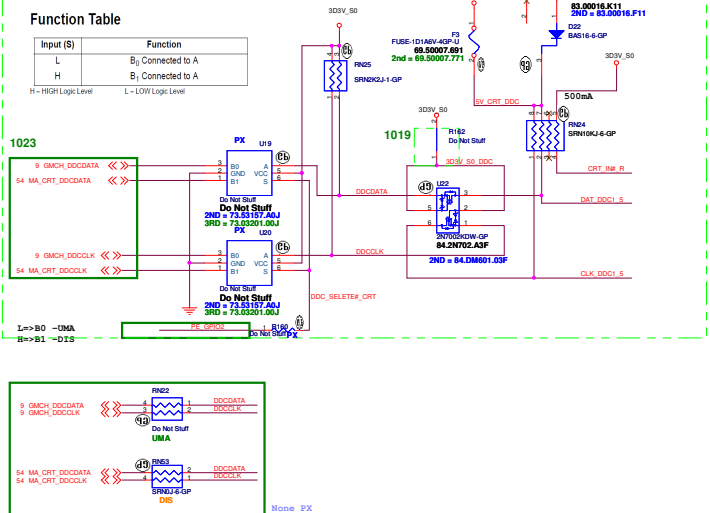
0918

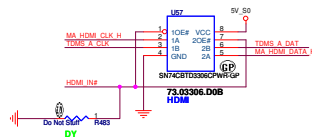
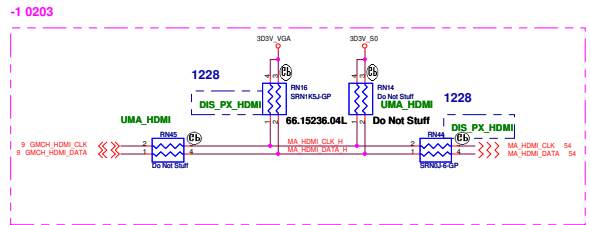
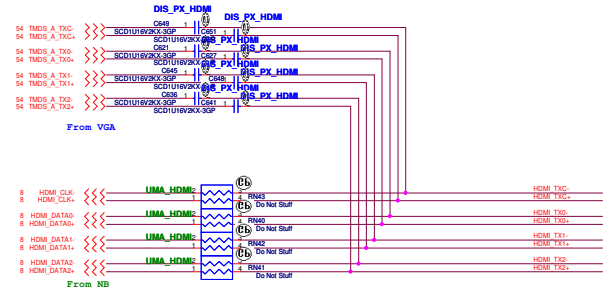
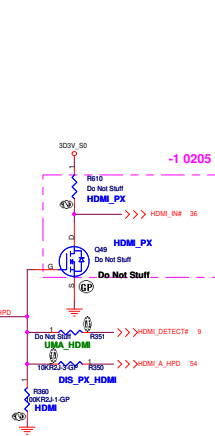
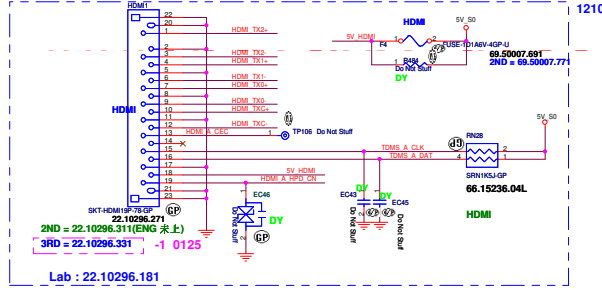
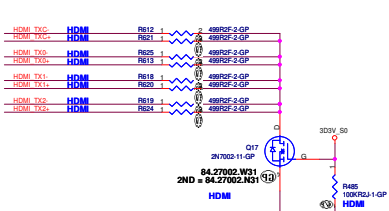
1012



0924

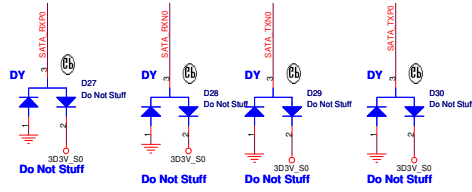
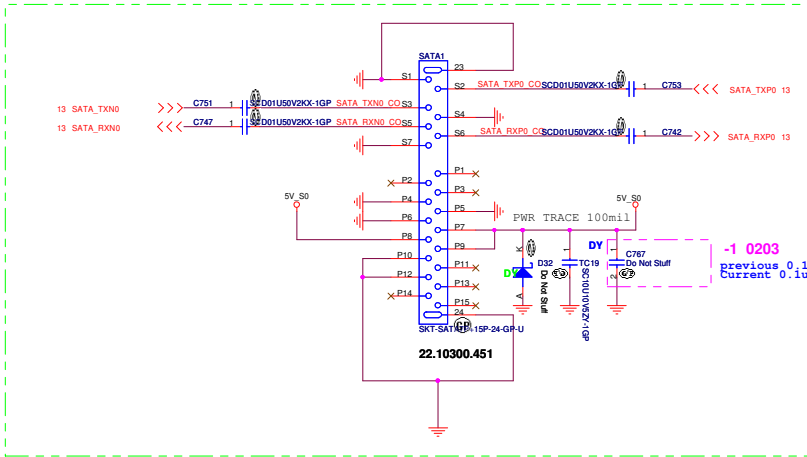
### DDC CLK & DATA level shift





# SATA Connector

0923



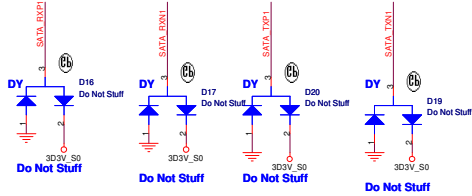
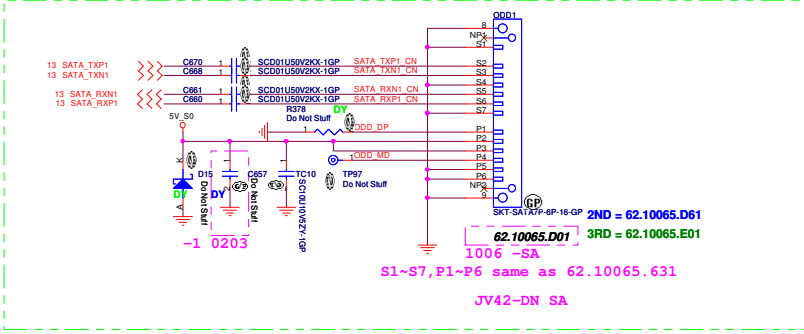
Discrete Medium Hynix

緯創資通 **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

File		<b>HDD</b>	
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# ODD Connector

1009



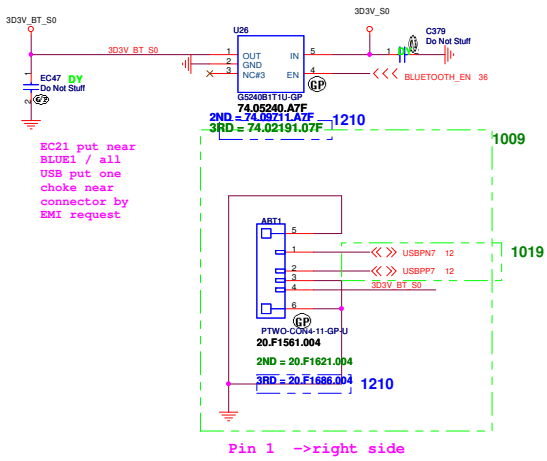
Discrete Madison Hynix

緯創資通  
**Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,  
 Taipei Hsien 221, Taiwan, R.O.C.

File			<b>ODD</b>
Size	Document Number	Rev	
	<b>JE40-DN</b>	<b>-2</b>	
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# BLUETOOTH MODULE

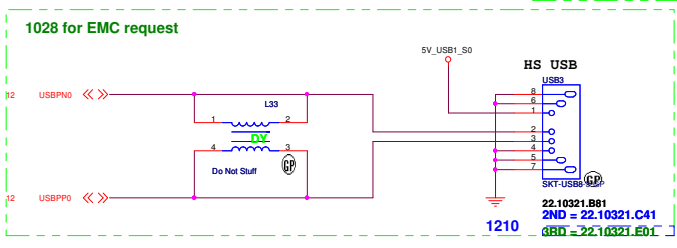
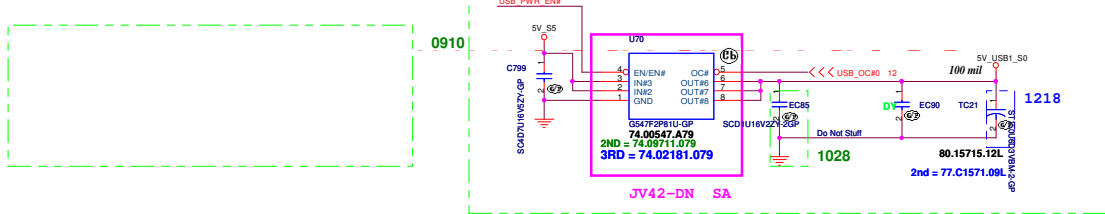
1.5A / High Active Voltage 2V



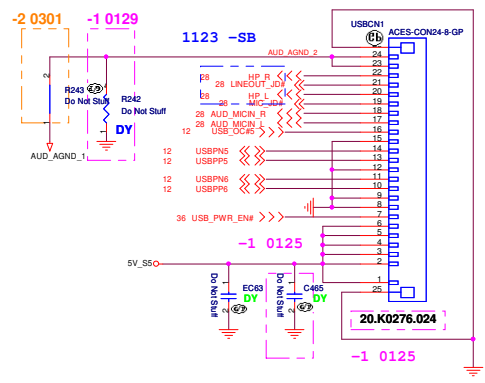
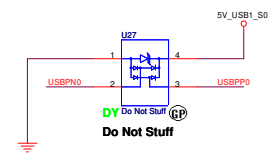
Discrete Madison Hyinx

 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.	
<b>BLUETOOTH</b>	
Size	Document Number
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Pin1 -> right side  
 22.10218.T51 Pin1 -> left side (JV42-DN)  
 change Net sequence



Eng stuff 20.K0216.024 Pin1 -> left side  
 PD change to 20.K0276.024 Pin1 -> left side  
 so do not swap net

Discrete Madison Hynix

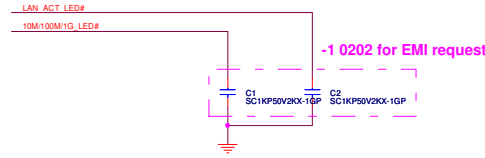
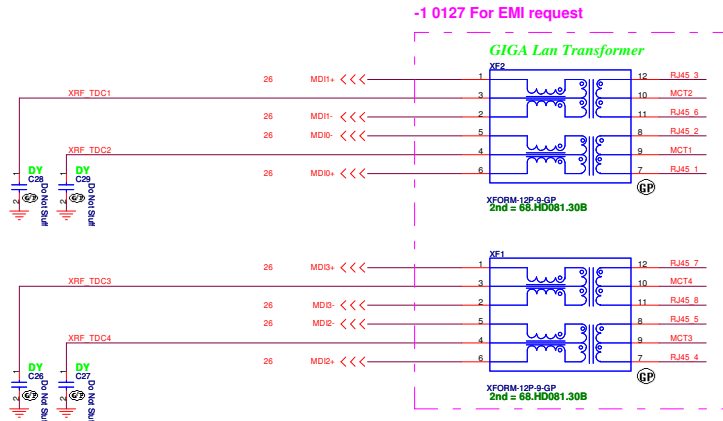
緯創資通		Wistron Corporation	
		217, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 321, Taiwan, R.O.C.	
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USB			
Size	Document Number	Rev	
	JE40-DN	-2	
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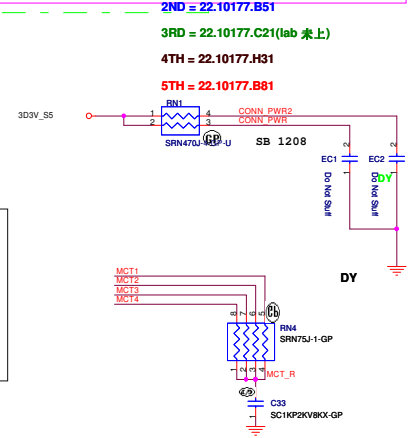
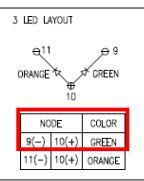
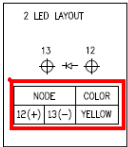
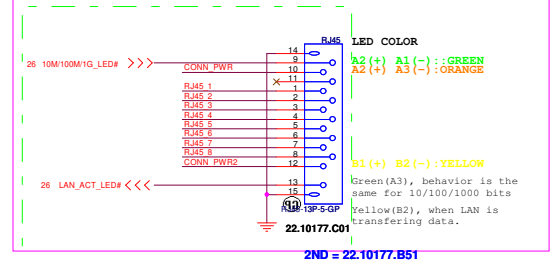
# LAN Connector

# LAN Connector

1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.



0923

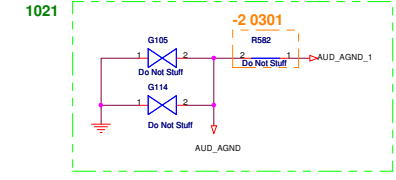
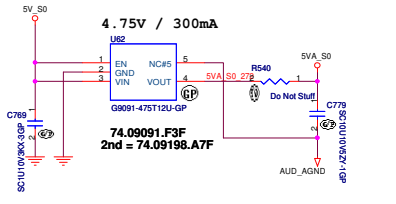
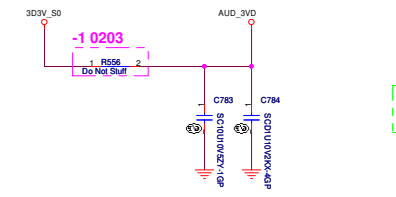
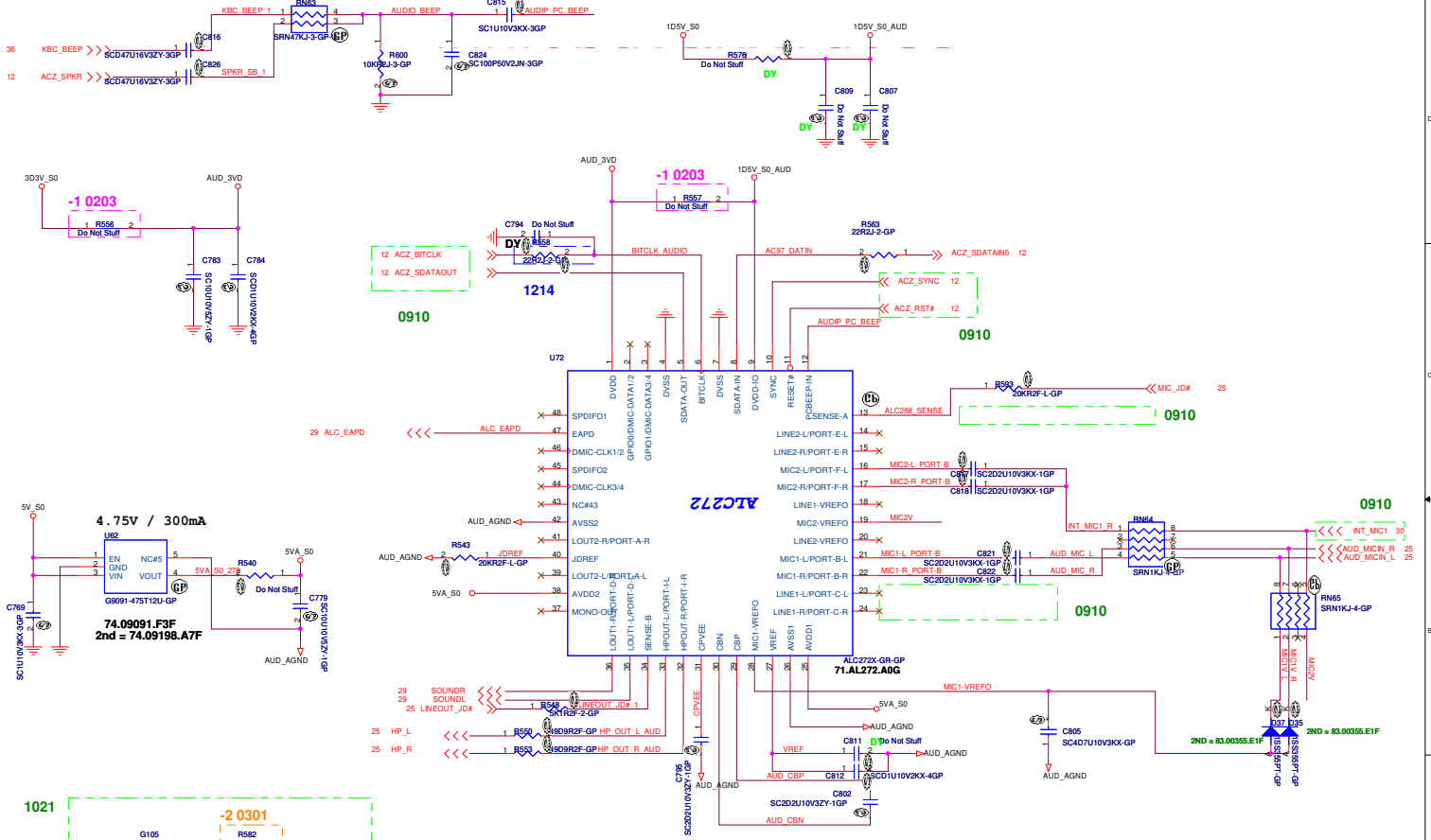


Discrete Medium Hybrid

**緯創資通 Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		<b>LAN CONN</b>	
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Discrete Madison Hynix

**緯創資通 Wistron Corporation**  
217, 8th, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

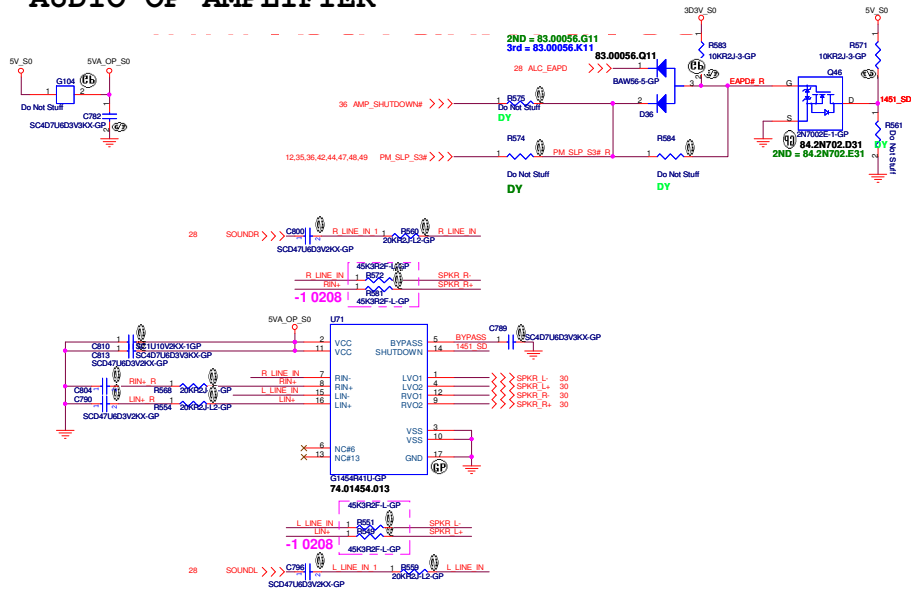
File: **Azalia codec ALC272**

Size	Document Number	Rev
K3		-2

**JE40-DN**

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# AUDIO OP AMPLIFIER



Discrete Medium Hybrid

緯創資通

**Wistron Corporation**  
2/F, 88, Sec.1, Hsin-Tai Wei Rd., Hsinchu,  
Taichung Hsien 321, Taiwan, R.O.C.

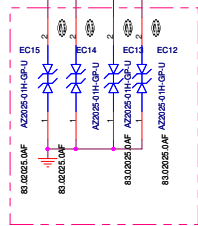
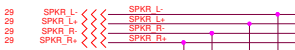
File		AUDIO AMP	
Doc	Document Number	JE40-DN	
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# Internal Speaker

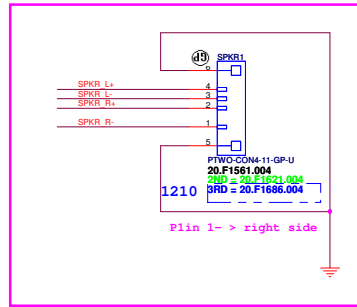
0914



0910



-1 0125 for EMI request



JV42-DN SA

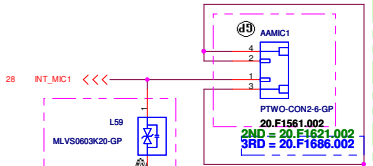
# LINE OUT

0911

0910

1016

# Internal Mic



-1 0209 For MIC issue

JV42-DN PX  
 Pin 1 -> right side  
 20.F1240.002 Pin1->left side  
 same as JV70-CP

Discrete Madison Hynix

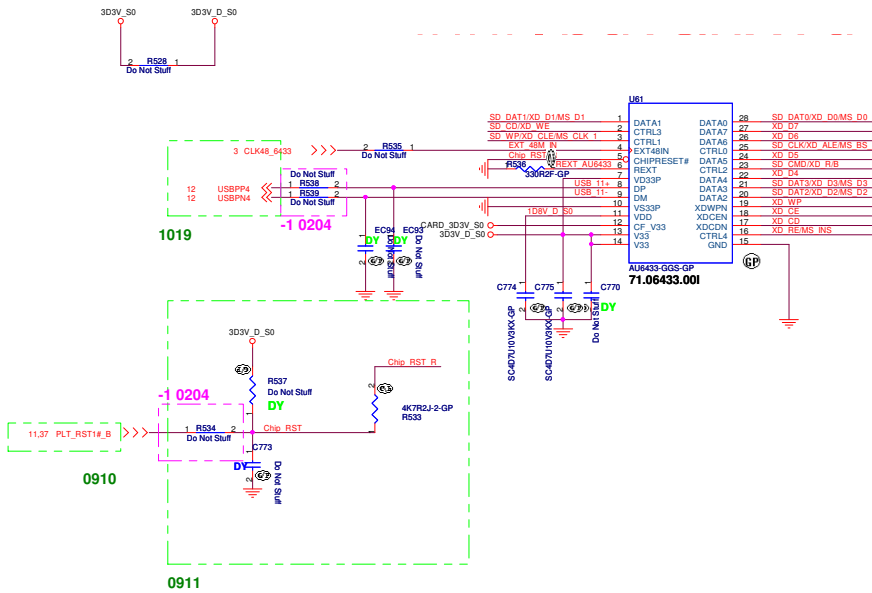
**緯創資通** Wistron Corporation  
 217, 8th, Sec.1, Hsin Tai Wu Rd., Hsinchu,  
 Taipei Hsien 221, Taiwan, R.O.C.

File		
<b>AUDIO JACK</b>		
Size	Document Number	Rev
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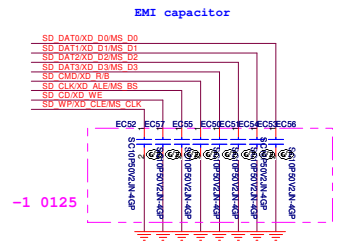
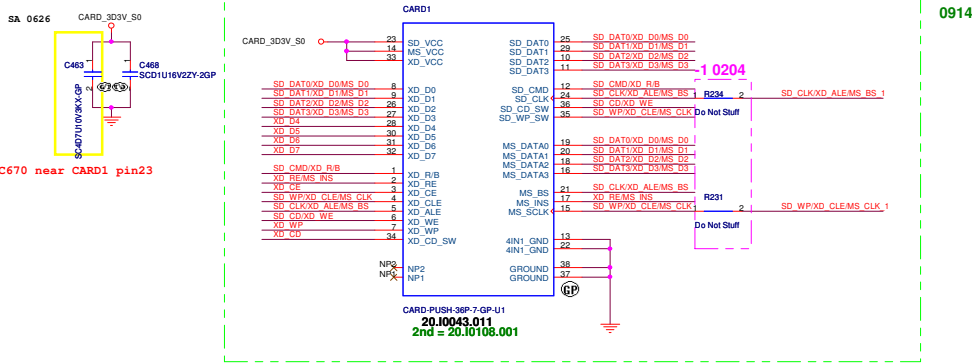
No Modem Function

Discrete Madison Hyrix

<b>緯創資通</b>		<b>Wistron Corporation</b>	
<small>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.</small>		<small>21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichia, Taipei Hsien 221, Taiwan, R.O.C.</small>	
<b>Title</b>			
<b>MDC</b>			
<b>Size</b>	<b>Document Number</b>		<b>Rev</b>
	<b>JE40-DN</b>		<b>-2</b>
<b>Date: Monday, March 08, 2010</b>			
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			<b>63</b>



### 5 IN 1 CARD-READER (SD/MMC/MS/MS PRO/XD)



Discrete Madison Hyrax

**緯創資通** Wistron Corporation  
21F, Sec. 1, Hsin-Tai Wu Rd., Hsueh, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CARDREADER**

Size: Document Number: **JE40-DN** Rev: **-2**

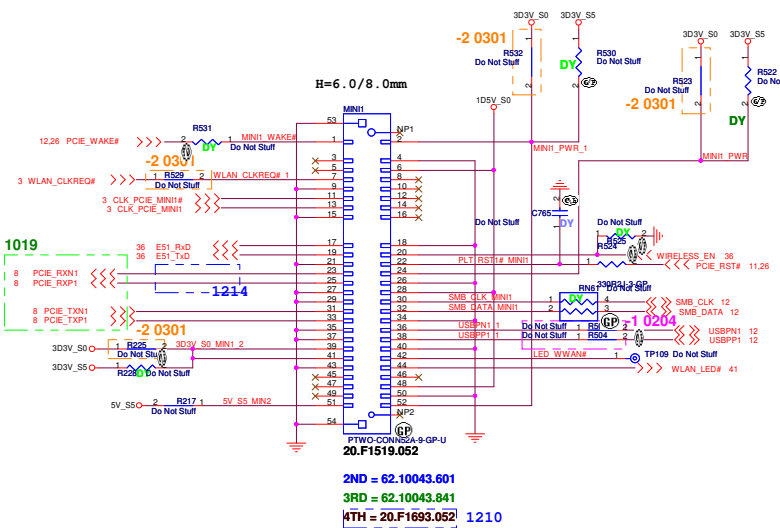
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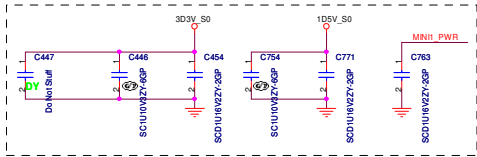
# Mini Card Connector(WLAN)

# No Mini Card Function (Robson2 and 3G)

0923



Place near MINI1



Discrete Madison Hynix

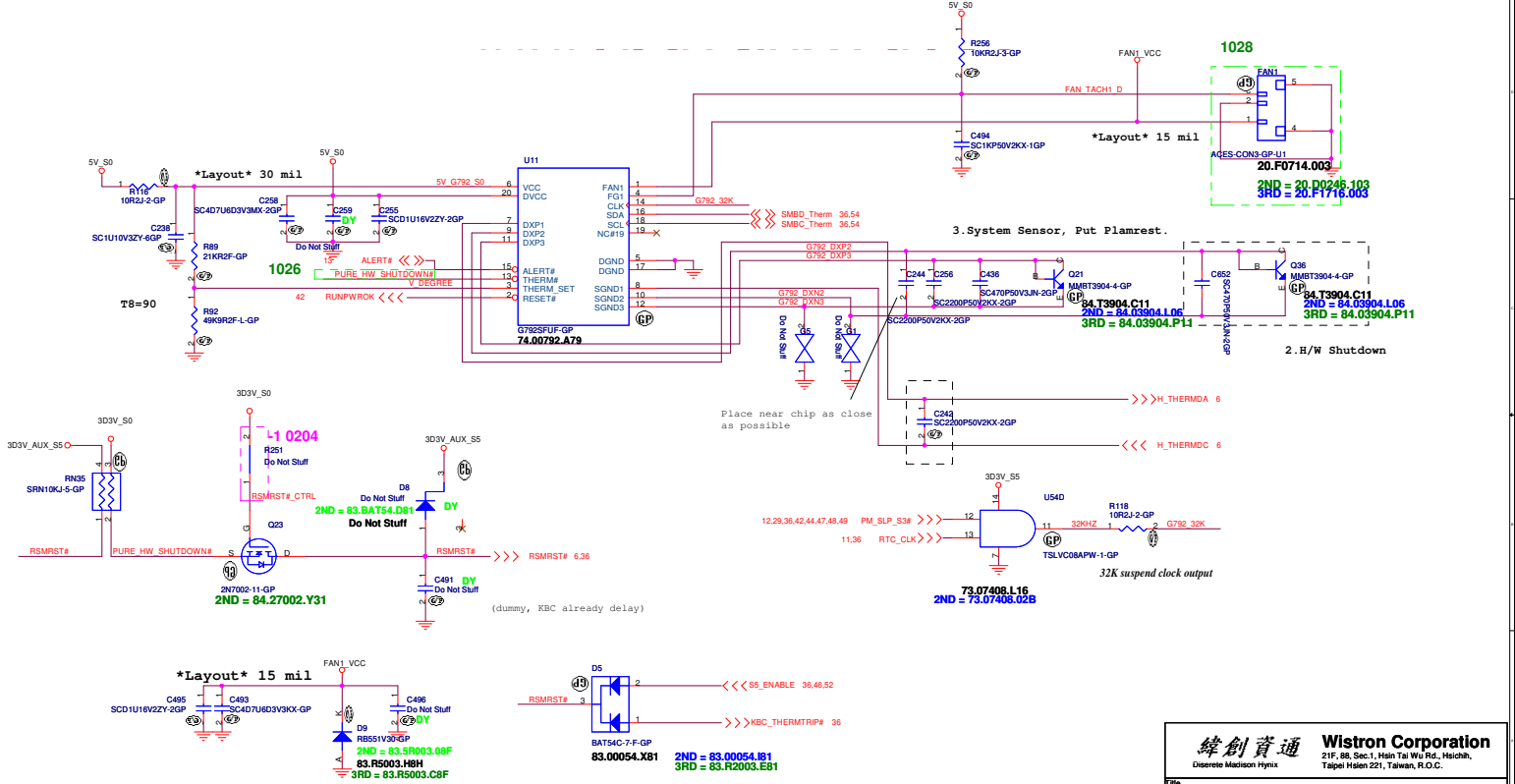
 <b>Wistron Corporation</b> <small>217, 8th, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 321, Taiwan, R.O.C.</small>		
<b>MINI CARD</b>		
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Size	Document Number	Rev
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**No NEWCARD Function**

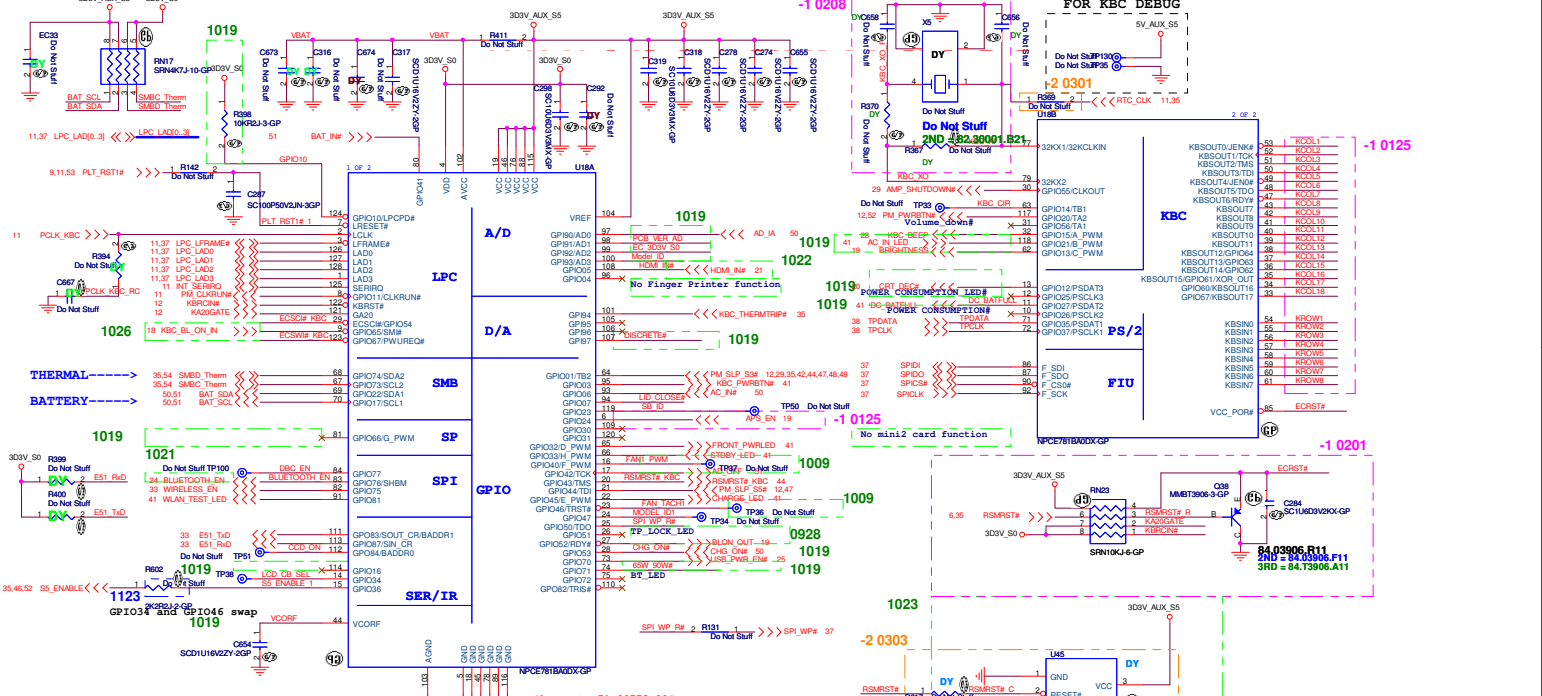
Discrete Madison Hynix

**緯創資通** **Wistron Corporation**  
217, 8th, Sec.1, Hsin Tai Wu Rd., Hsinchu,  
Taipai Hsien 321, Taiwan, R.O.C.

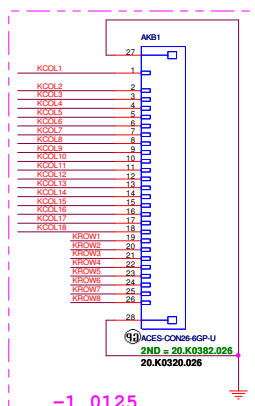
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Date:	Monday, March 08, 2010	Sheet 34 of 63



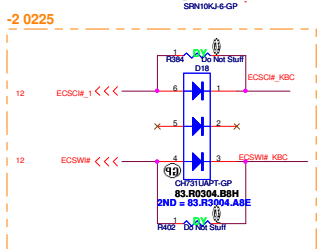
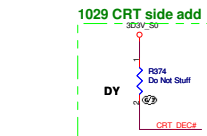
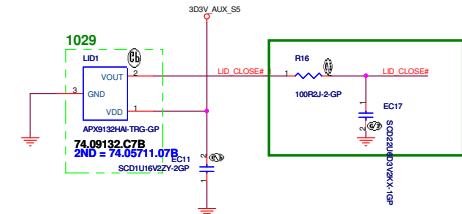
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsin 221, Taiwan, R.O.C.			
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Custom		<b>-2</b>	
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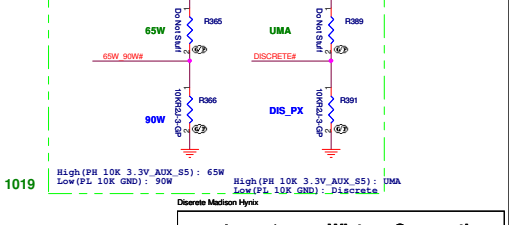
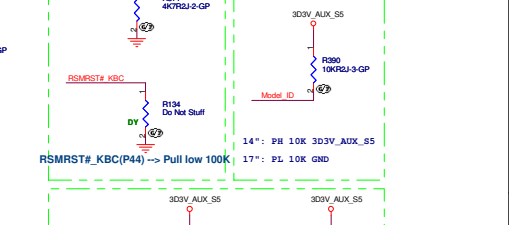
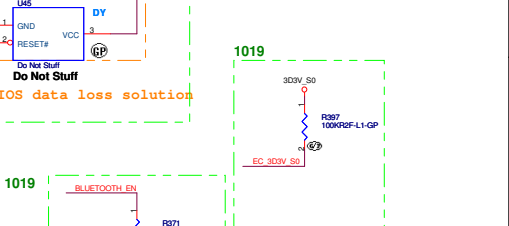
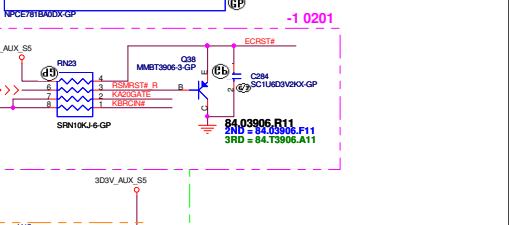
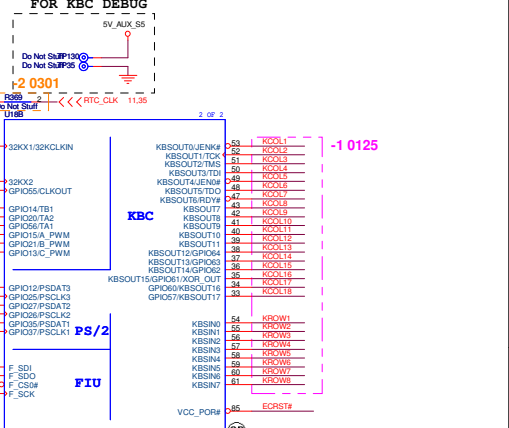
change connect to PPC (Same as Lab)  
 20.K0320.026 Pin 1 -> left side  
 20.K0320.026 Pin 1 -> right side (use in lab stage)  
 so swap net



**LID SWITCH**



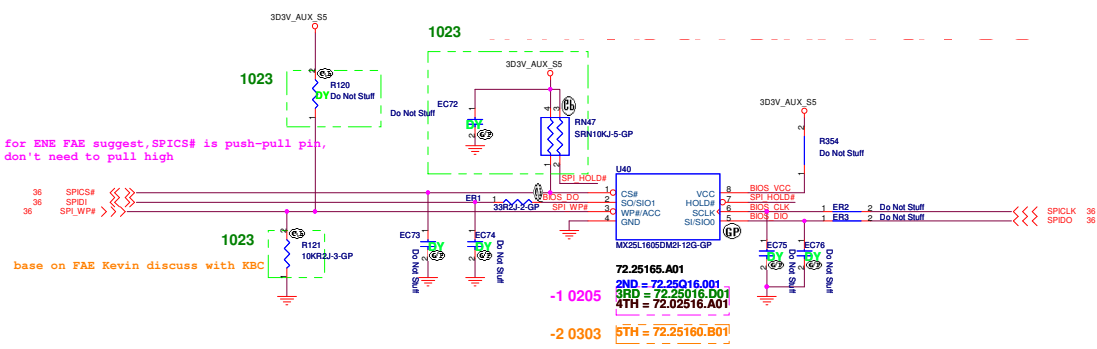
Pull-High Resistor (303V_AUX_S5)	Voltage
1.0 K	3.0 V
2.0 K	2.75 V
3.0 K	2.54 V
4.7 K	2.24 V
6.98 K	1.94 V
8.2 K	1.81 V
10.0 K	1.65 V



High (PH 10K 3.3V\_AUX\_S5) : 65W  
 Low (PL 10K GND) : 90W

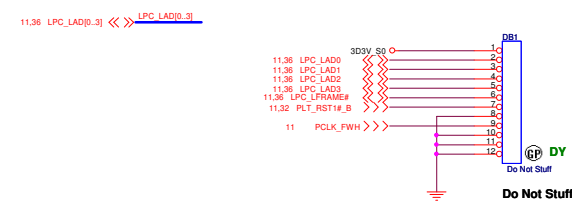
緯創資通 Wistron Corporation  
 25F, 8F, Sec.1, Hsin-Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.

File: KBC NPCE781B  
 Size: Document Number  
 Custom: JE40-DN  
 Date: Tuesday, March 09, 2010  
 Sheet: 36 of 53



3rd 4th source LAB ENG 未上  
**16M Bits**  
**SPI FLASH ROM**

**GOLDEN FINGER FOR DEBUG BOARD**



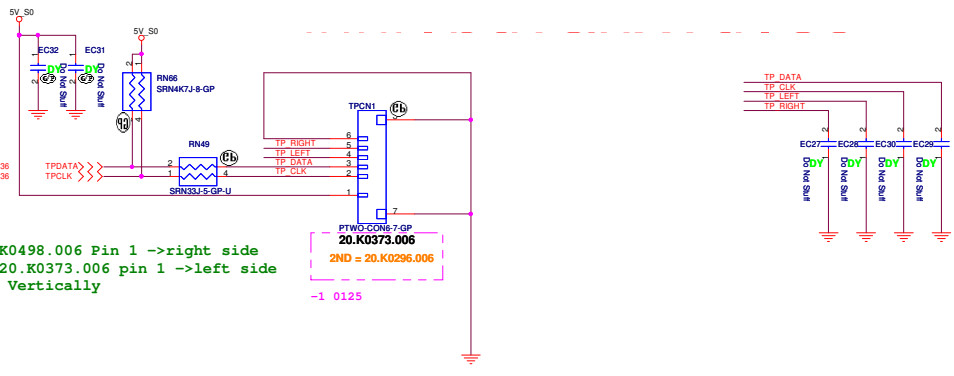
Discrete Medison Hynix

**緯創資通 Wistron Corporation**  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS**

Size: **A3** Document Number: **JE40-DN** Rev: **-2**

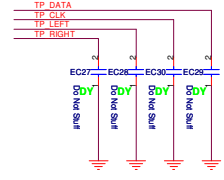
Date: Monday, March 08, 2010 Sheet 37 of 63



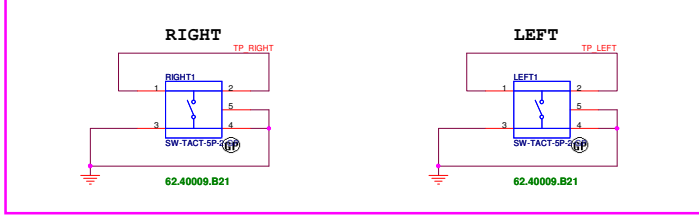
Eng stuff 20.K0498.006 Pin 1 ->right side  
 PD change to 20.K0373.006 pin 1 ->left side  
 so net mirror Vertically

PTWO-CON6-7-GP  
**20.K0373.006**  
 2ND = 20.K0296.006

-1 0125



-1 0205



No Finger printer Function

Discrete Madison Hynix

緯創資通 Wistron Corporation  
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 Taipei Hsein 221, Taiwan, R.O.C.

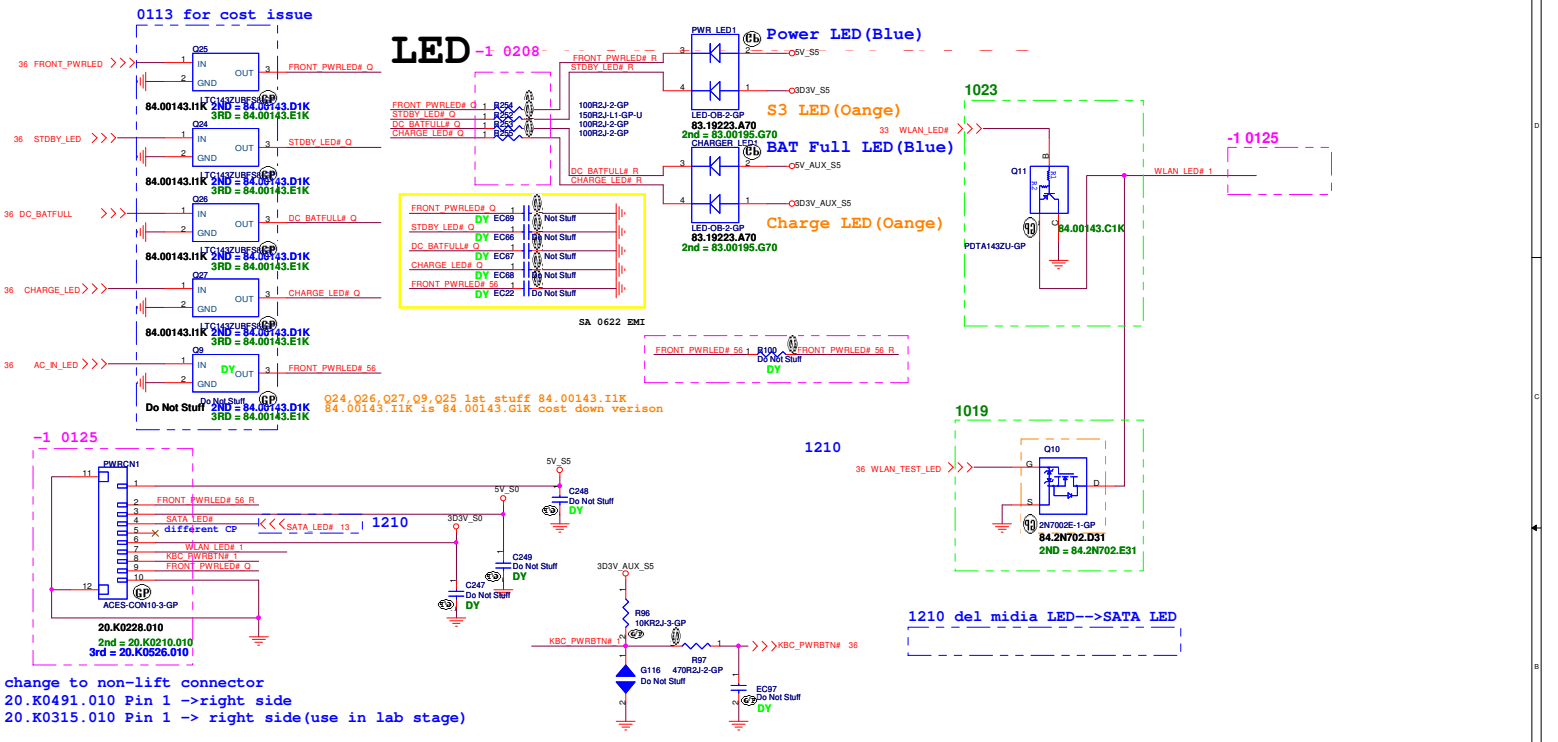
Title			<b>Touch PAD</b>		
Size	Document Number				Rev
A3	<b>JE40-DN</b>				-2
Date:	Monday, March 08, 2010	Sheet	38	of	93



<b>緯創資通</b>		<b>Wistron Corporation</b>
		<small>21F, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taippei Hsien 321, Taiwan, R.O.C.</small>
<b>NONE BOARD</b>		
File		
Size	Document Number	Rev
A3	<b>JE40-DN</b>	<b>-2</b>
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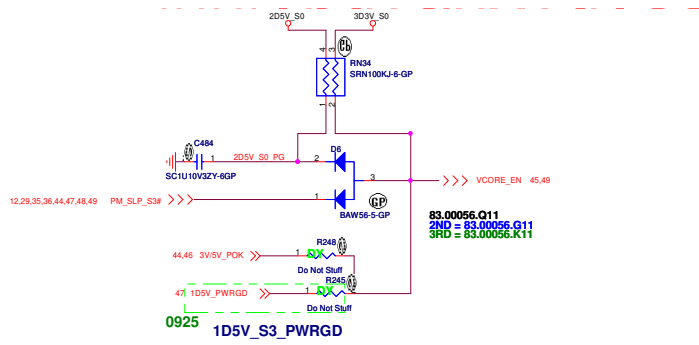
Pin 1	5V_S5	
Pin 2	FRONT_PWRLED#_56_R	AC IN
Pin 3	5V_S0	
Pin 4	SATA_LED#	HDD
Pin 5	NA	
Pin 6	3D3V_S0	
Pin 7	WLAN_LED#_R	WLAN
Pin 8	KBC_PWRBTN#_1	Power button
Pin 9	FRONT_PWRLED#_Q	Power LED
Pin 10	GND	

**緯創資通 Wistron Corporation**  
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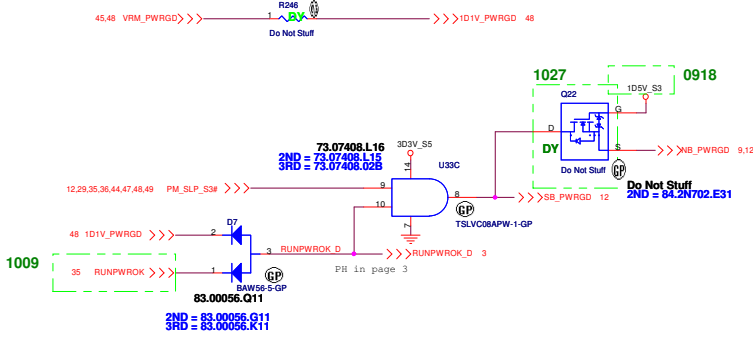
File  
**LED**

Size	Document Number	Rev
A3	<b>JE40-DN</b>	-2

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P/H @ 1D8V\_S3 PAGE

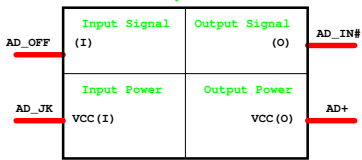


Discrete Medison Hynix

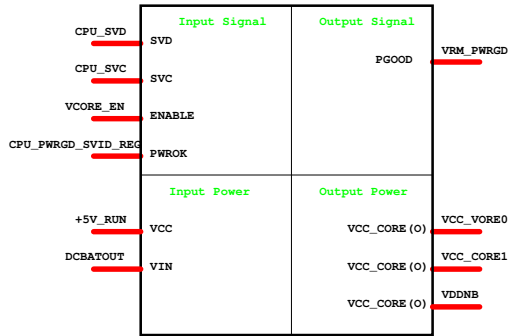
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			<b>POWER ON LOGIC</b>		
Size	Document Number				Rev
A3	<b>JE40-DN</b>				-2
Date:	Monday, March 08, 2010	Sheet	42	of	83

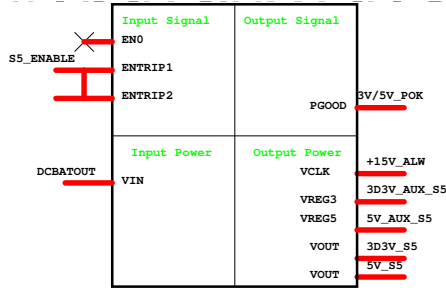
### Adapter



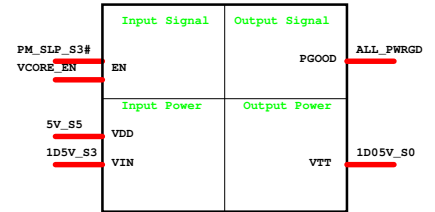
### CPU\_CORE ISL6265HRTZ



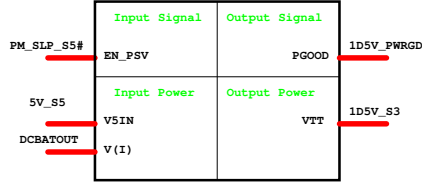
### DCDC 5V/3D3V(RT8223)



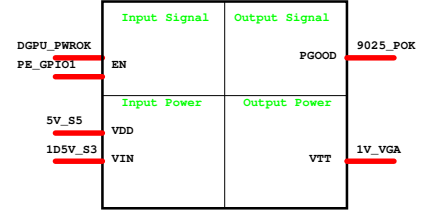
### DCDC 1D05V\_S0(RT9025)



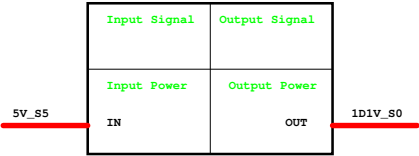
### DCDC 1D5V(RT8209E)



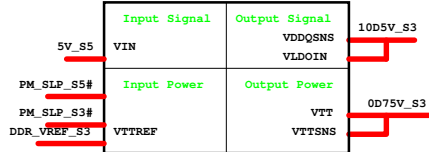
### DCDC 1V\_VGA(RT9025)



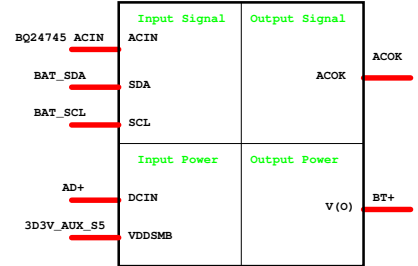
### 1D1V LDO RT8209E



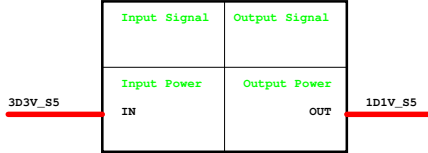
### 0D75V LDO RT9026



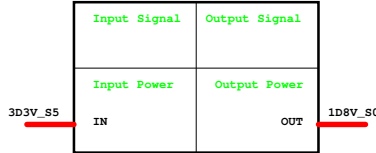
### CHARGER BQ24745



### 1D1V LDO RT9025



### 1D8V LDO RT8015A

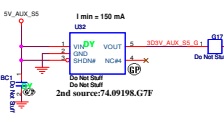


Discrete Madison Hynix

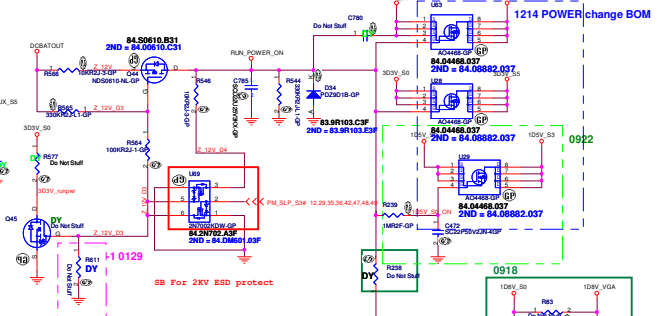
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsien Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

File			Power Block Diagram		
Size	Document Number		Rev		
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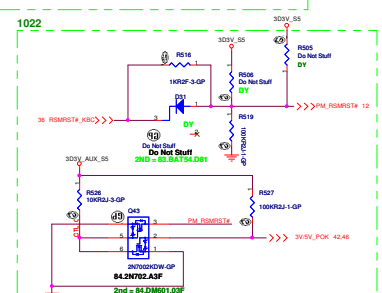
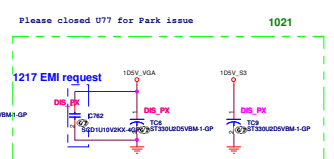
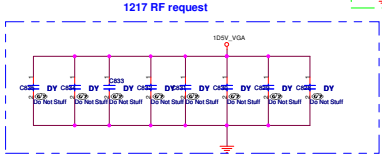
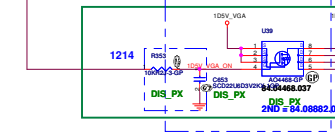
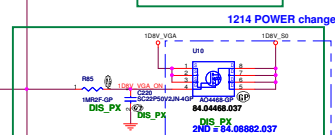
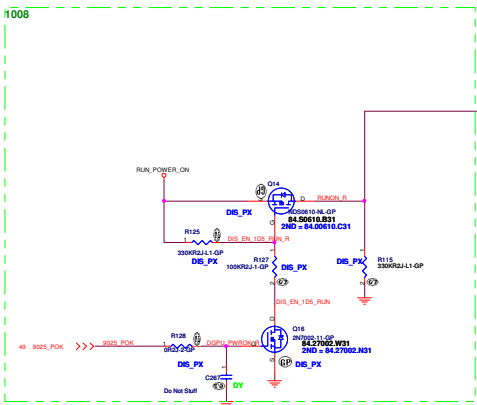
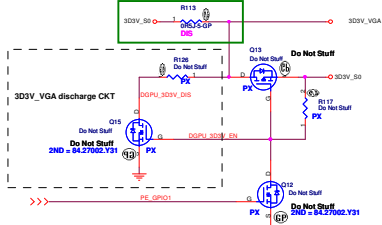
### Aux Power 3D3V\_AUX\_S5



### Run Power

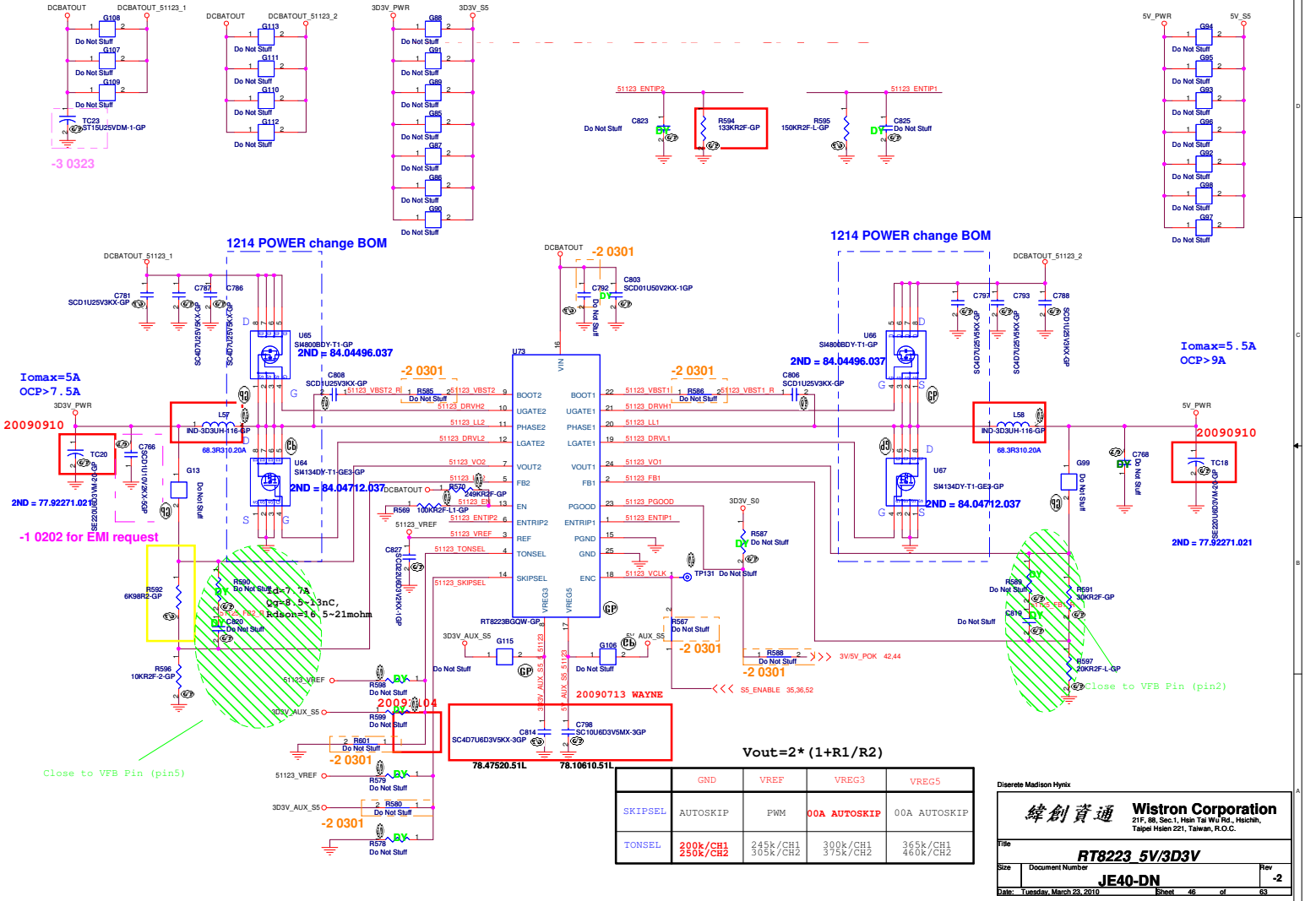


### +3VS to 3.3V\_DELAY Transfer



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 Tainan, R.O.C. Taiwan  
**RUN AND AUX POWER**  
 JE40-DN  
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**Vout=2\*(1+R1/R2)**

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

Discrete Madison Hyinx

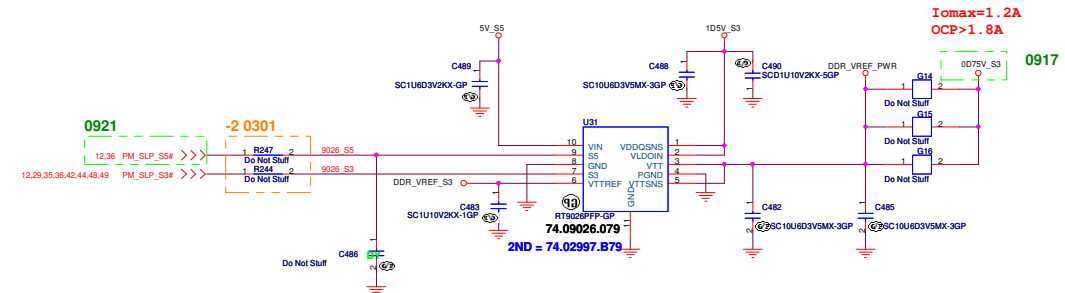
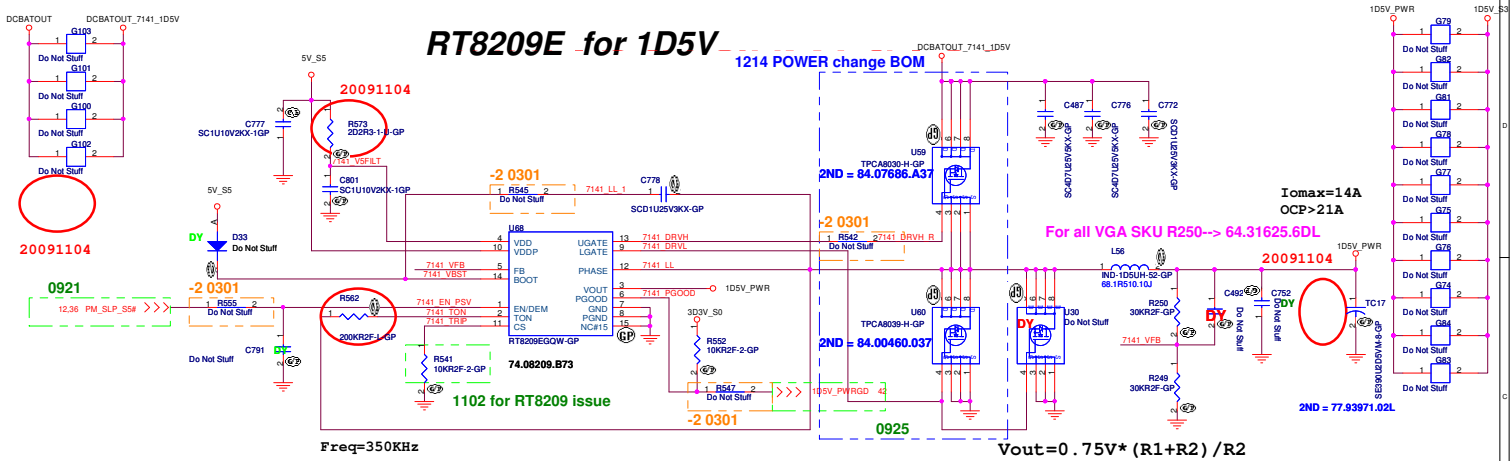
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

File: **RT8223 5V/3D3V**

Size	Document Number	Rev
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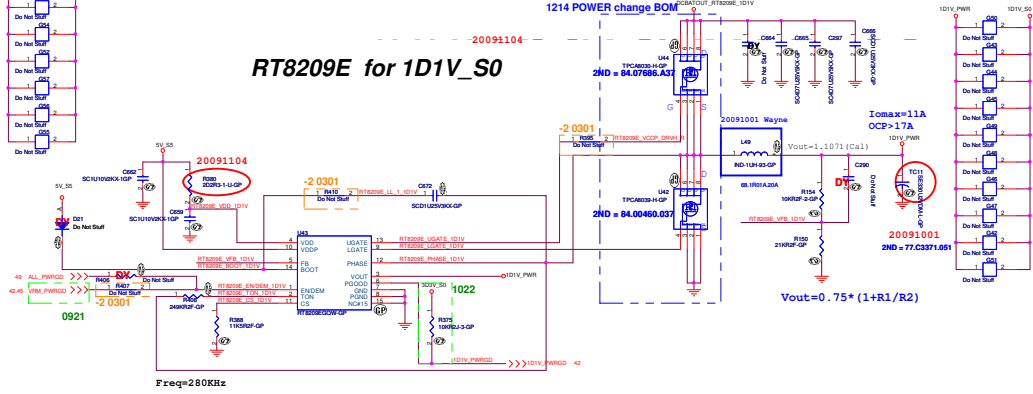
Date: Tuesday, March 23, 2010 Sheet 46 of 63

# RT8209E for 1D5V

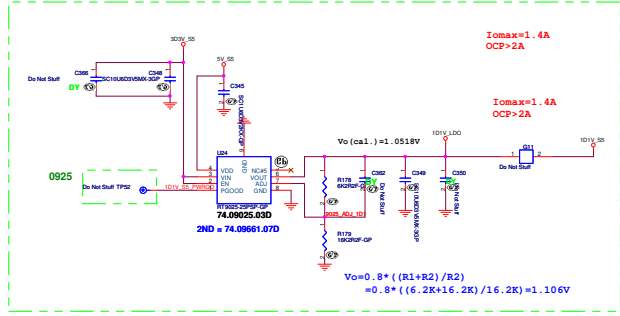


0917

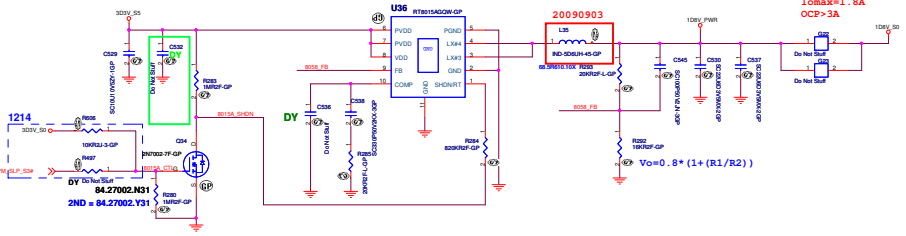
### RT2009E for 1D1V\_S0



### RT9025 for 1D1V\_S5

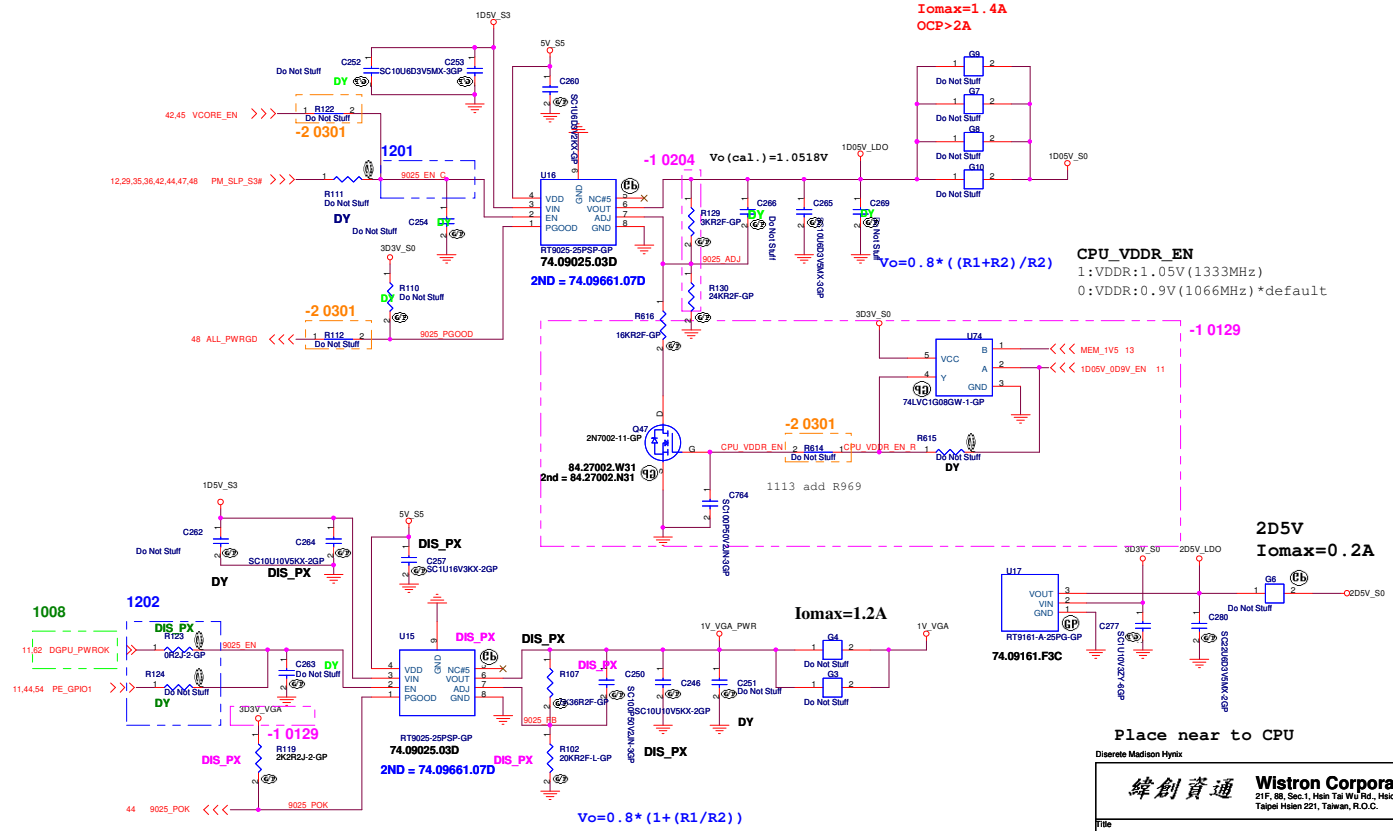


### RT8015A for 1D8V\_S0





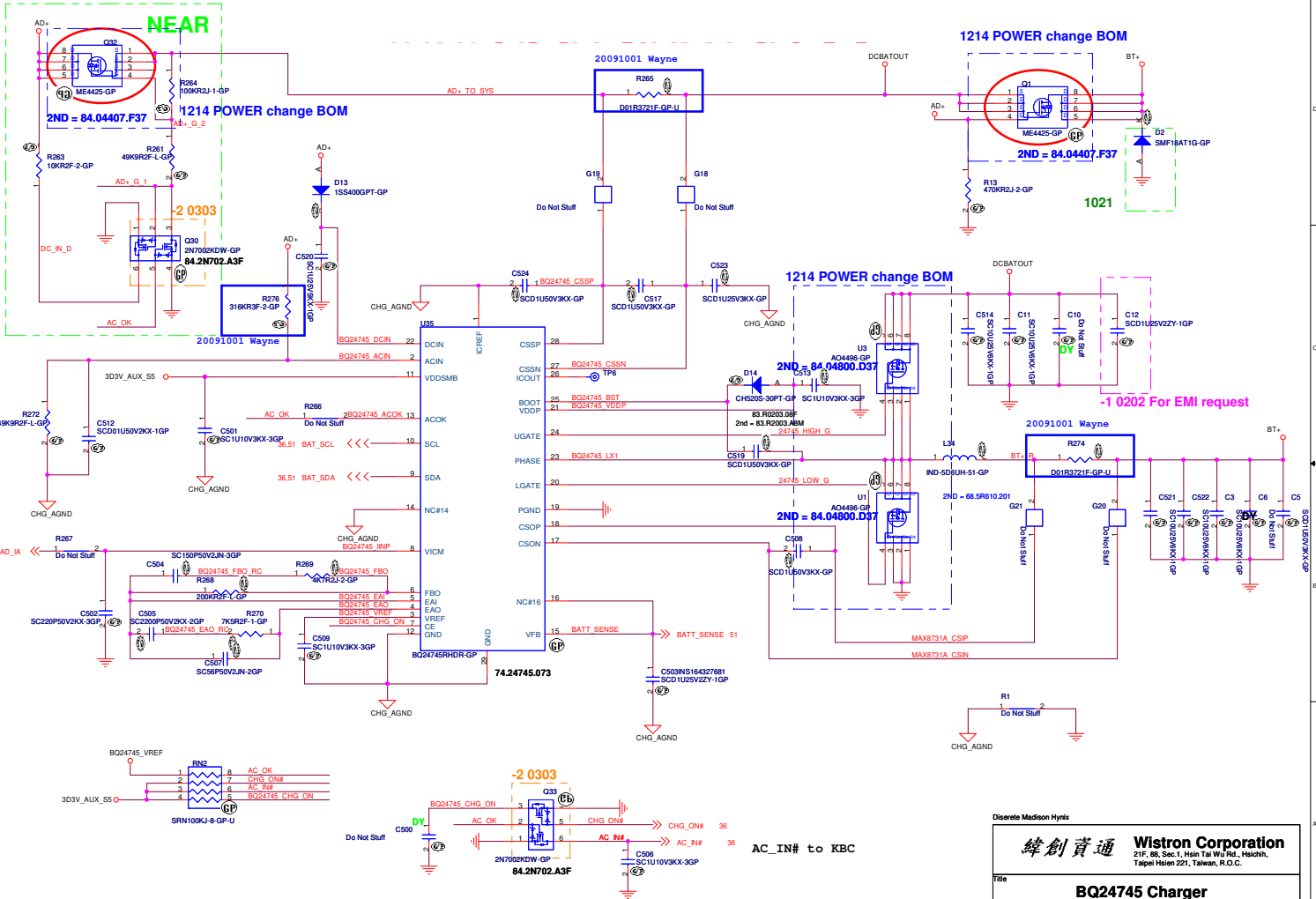
# RT9025 for 1D05V\_S0



Discrete Madison Hyrax

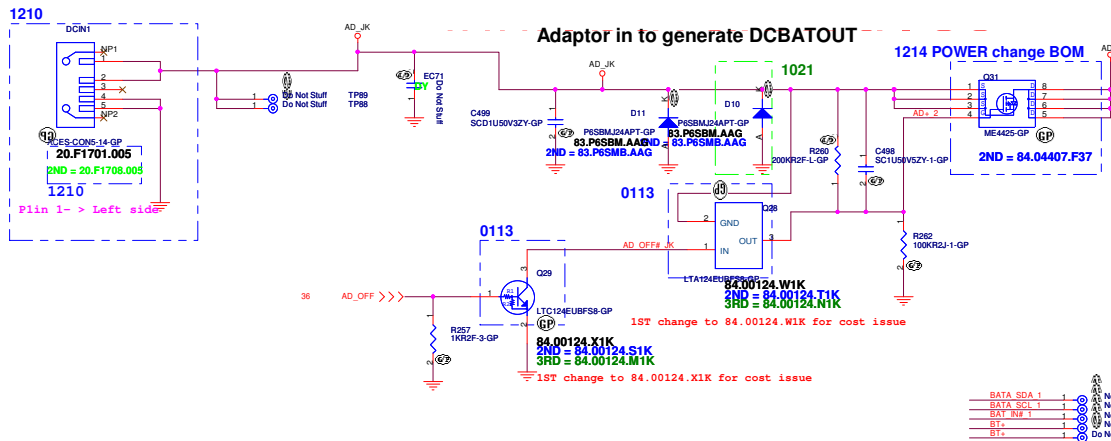
**緯創資通 Wistron Corporation**  
 217, 8th, Sec.1, Hsin Tai Wu Rd., Hsinchu,  
 Taipei Hsien 221, Taiwan, R.O.C.

File	<b>LDO 1D05V/2D5V/1V</b>		
Size	Document Number	Rev	
K3	<b>JE40-DN</b>	-2	
Date:	Monday, March 08, 2010	Sheet	49 of 63



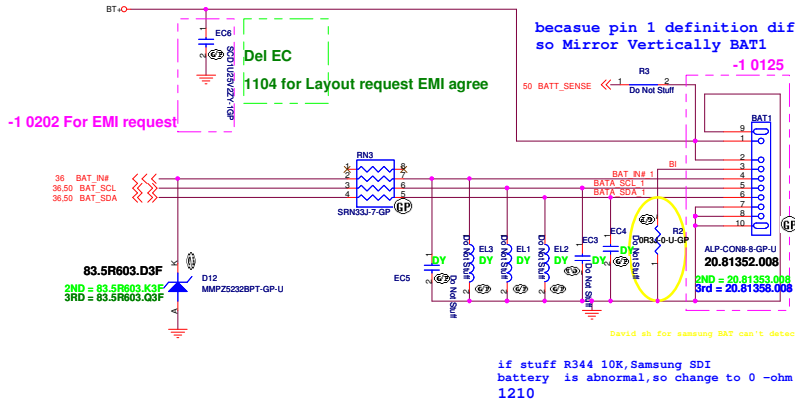
Discrete Madison Hynx

<b>緯創資通</b> <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin-Tai Wu Rd., Hsueh-shan, Taipei Hsien 221, Taiwan, R.O.C.	
<b>BQ24745 Charger</b>	
File	
Size K3	Document Number
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	Rev -2



BATA_SDA_1	1	Do Not Stuff	TP2
BATA_SCL_1	1	Do Not Stuff	TP1
BAT_INF_1	1	Do Not Stuff	TP3
BT+	1	Do Not Stuff	TP5
BT-	1	Do Not Stuff	TP4

**BATTERY CONNECTOR**



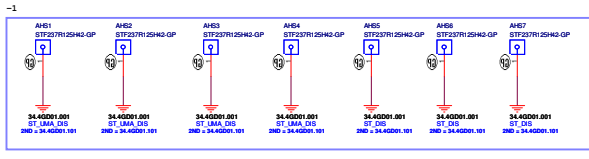
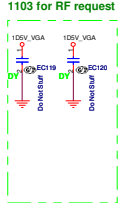
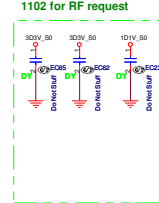
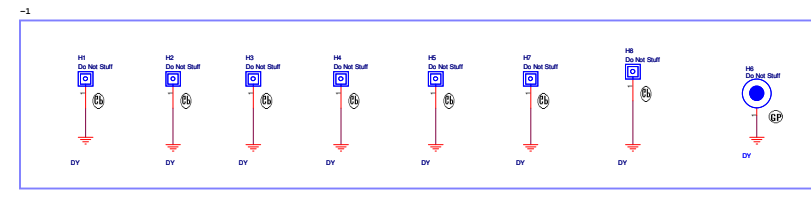
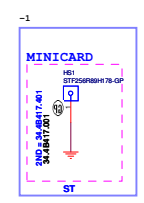
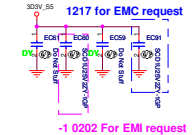
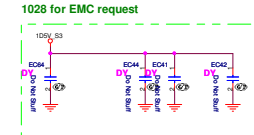
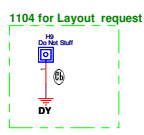
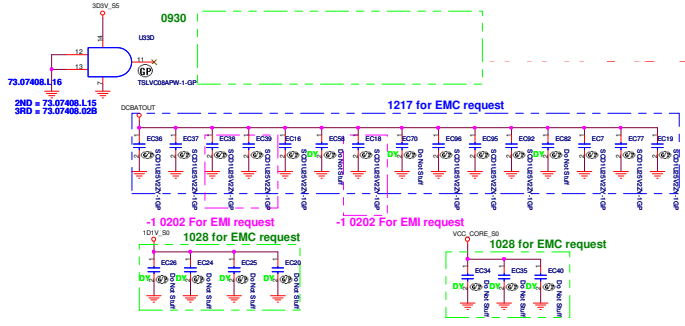
Pin Definition

1+	GND+	Batt-, Battery Negative Terminal+
2-	GND-	Batt-, Battery Negative Terminal-
3+	SMD+	SMBus data interface I/O pin+
4-	SMC-	SMBus clock interface I/O pin-
5+	TH+	Connect to Resistor to GND (10K to GND)
6+	BI+	System present pin, low active+
7+	BATT+	Batt-, Battery Positive Terminal+
8+	BATT-	Batt-, Battery Positive Terminal-

Discrete Madison Hynix

**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 101, Taiwan, R.O.C.

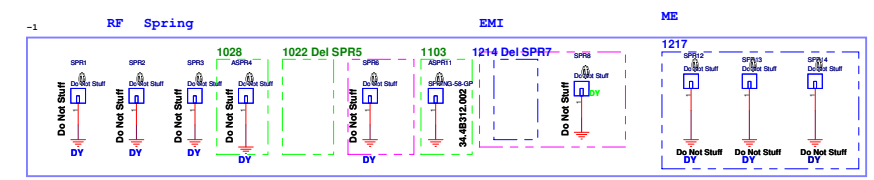
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<b>AD/BATT CONN</b>		
Size	Document Number	Rev
	<b>JE40-DN</b>	<b>-2</b>
Date:	Monday, March 08, 2010	Sheet 51 of 63

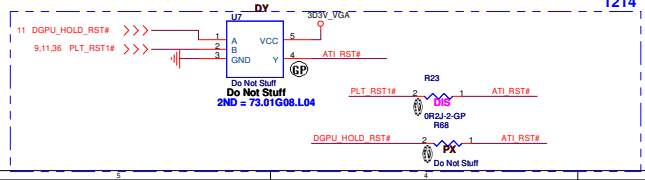
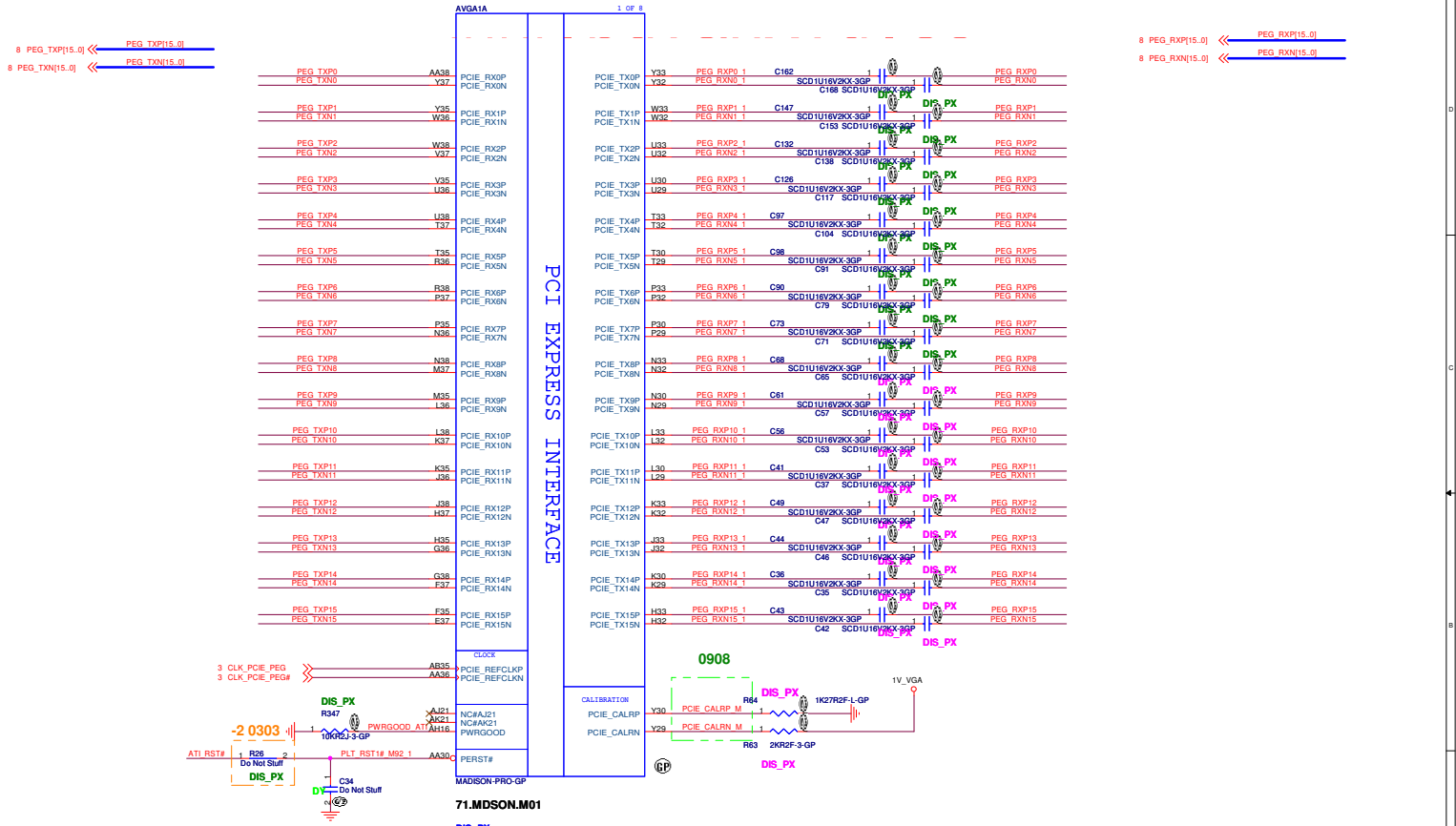


**Check test point**

30V_S0	TP126	Do Not Stuff
30V_AUX_S5	TP125	Do Not Stuff
30V_S5	TP125	Do Not Stuff
5V_S5	TP125	Do Not Stuff
12.38_PU_PWRSTW	TP124	Do Not Stuff
6.11_CPU_PWRD	TP127	Do Not Stuff
35.36.48_SE_ENABLE	TP128	Do Not Stuff
6.11_CPU_LDT_RST#	TP128	Do Not Stuff

Test Point放在Dimm Door打開可量測處





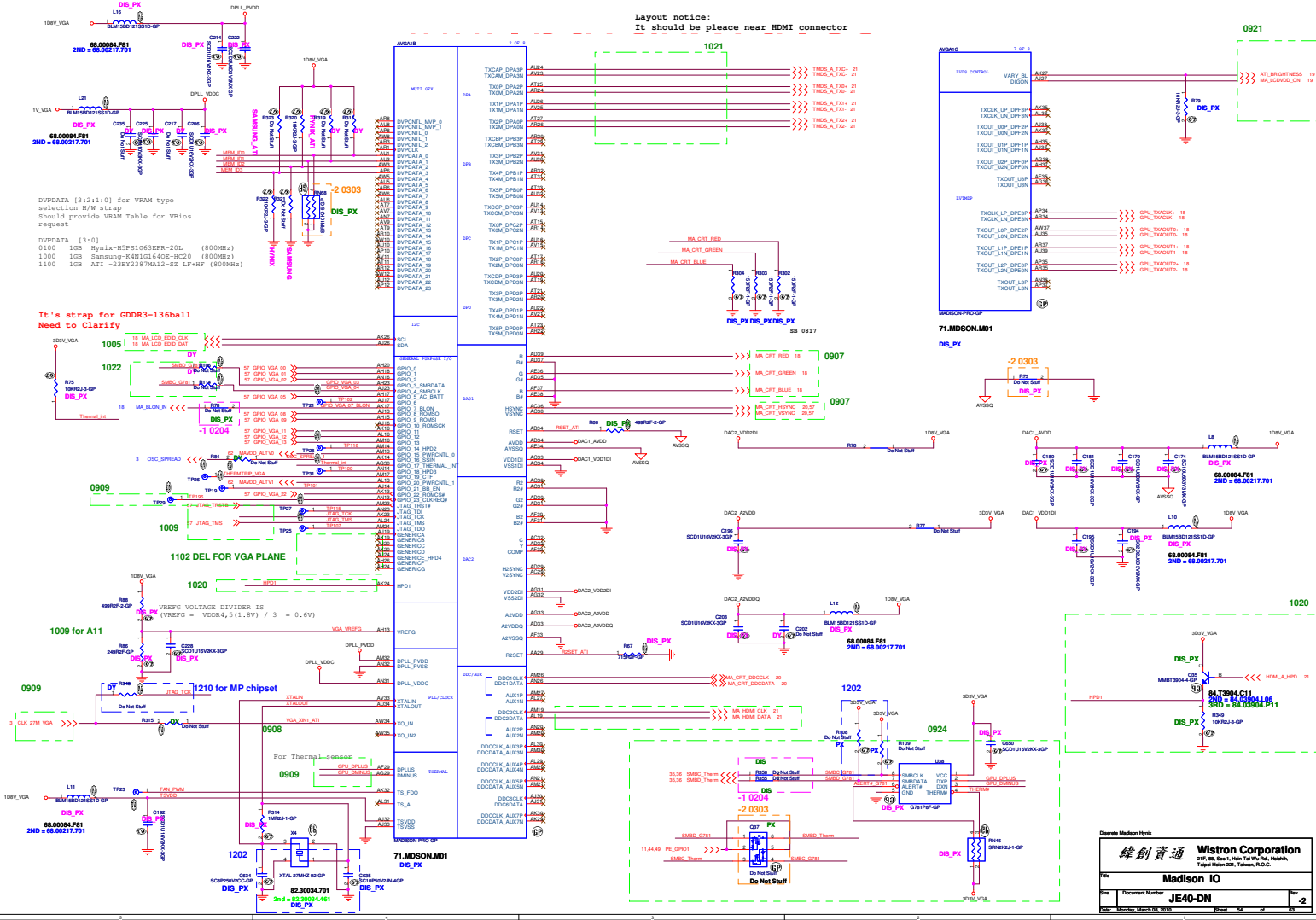
Discrete Madison Hyrich

**緯創資通 Wistron Corporation**  
 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

Title: **Madison PCIE**

Size: Document Number: **JE40-DN** Rev: **-2**

Date: Monday, March 08, 2010 Sheet: 53 of 63



Layout notice: It should be place near HDMI connector

0921

DVPPDATA [3:2:1:0] for VRAM type selection H/W strap  
Should provide VRAM table for Vbios request  
DVPPDATA [3:0]

It's strap for GDDR3-136ball Need to Clarify

1005 18 MA\_LCD\_EED\_OLA  
18 MA\_LCD\_EED\_OMI

1022 18 MA\_LCD\_EED\_OLA  
18 MA\_LCD\_EED\_OMI

1009 3 OSC\_SPREAD

1102 DEL FOR VGA PLANE

1009 for A11

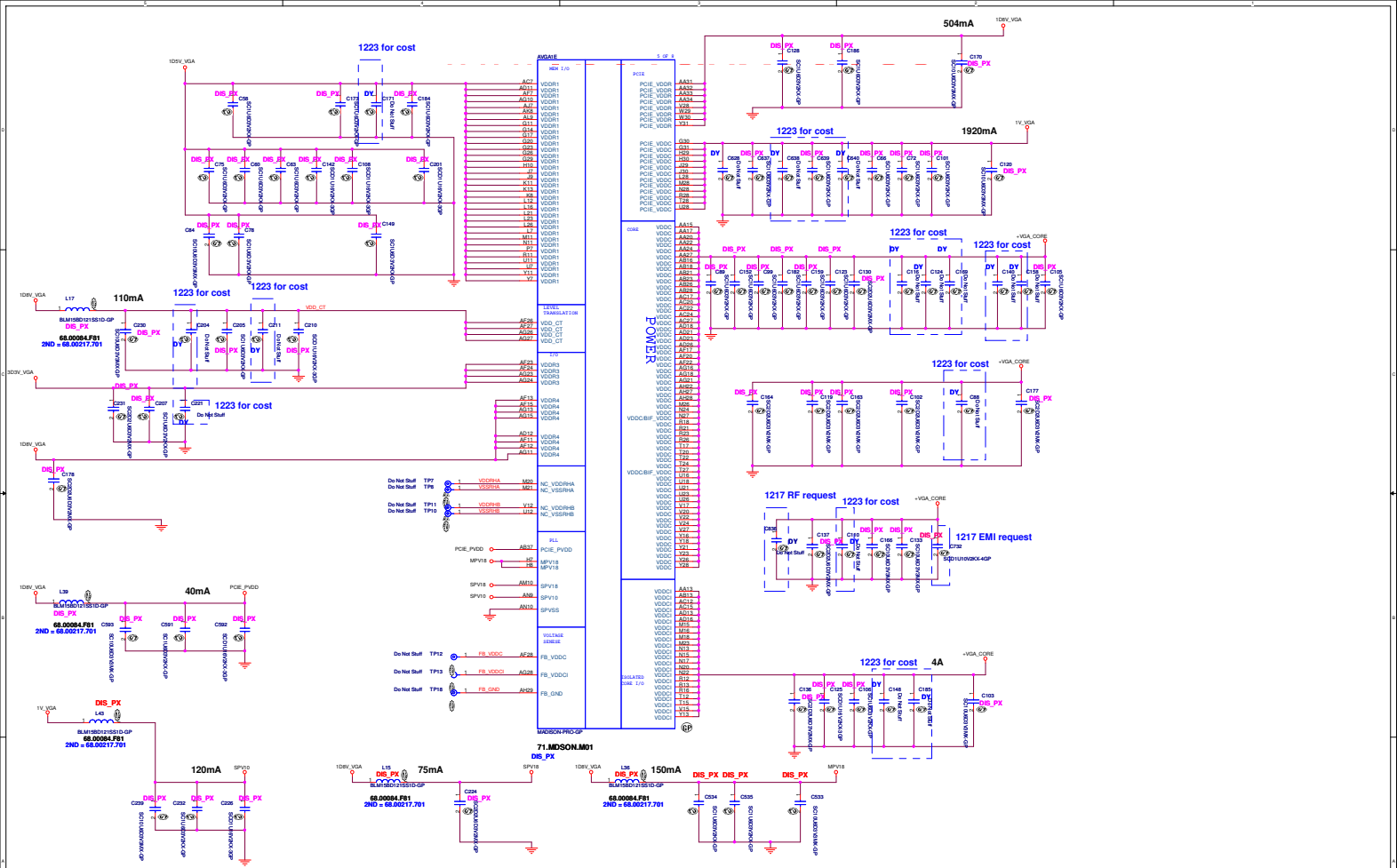
1210 for MP chipset

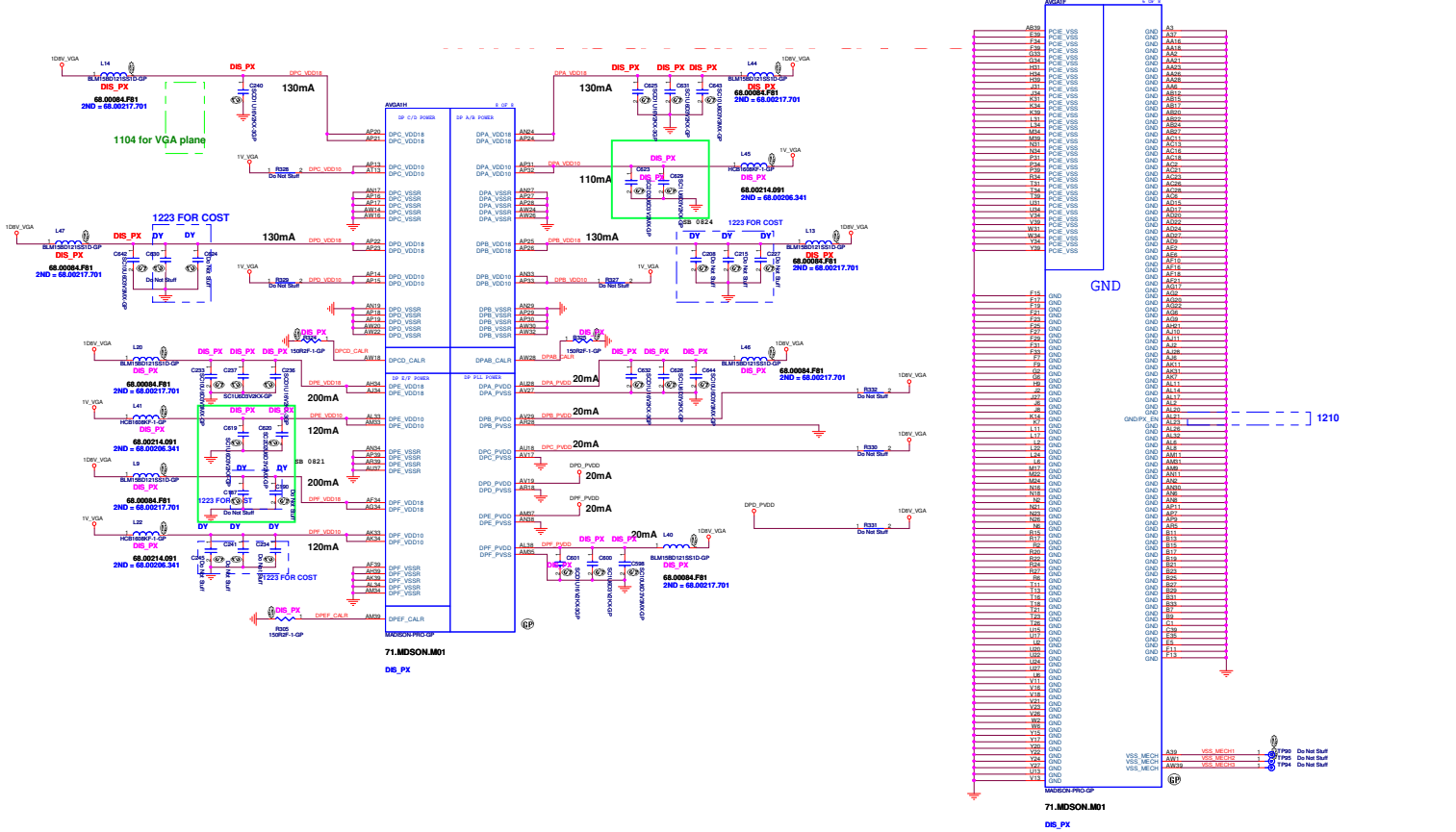
0908 For Thermal sensor

0909

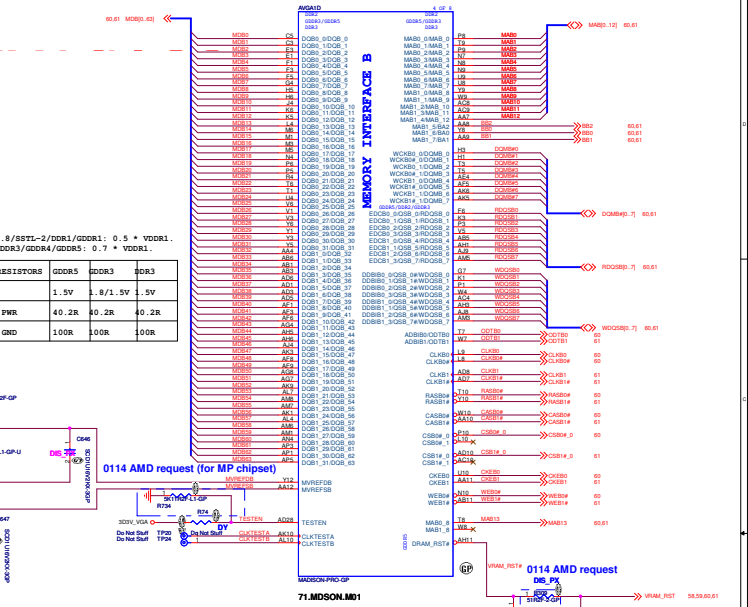
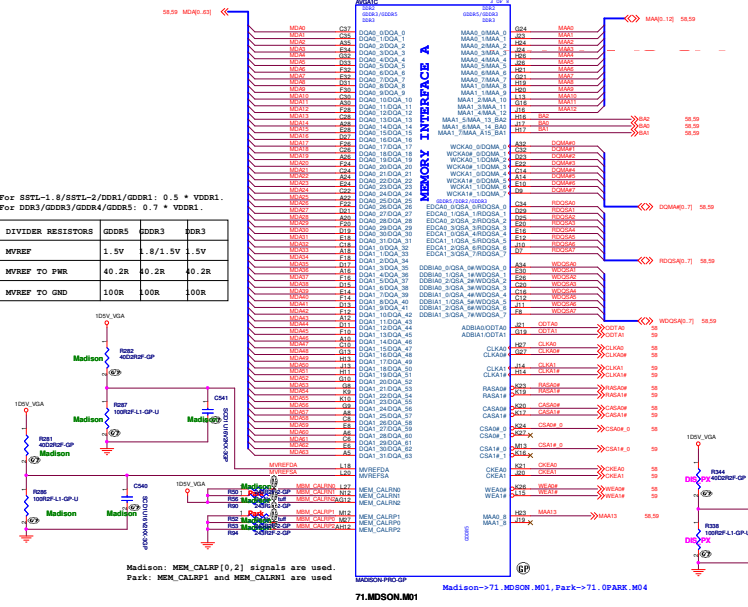
1202

Chinese Mediamix logo  
Wistron Corporation  
Madison IO  
JE40-DN





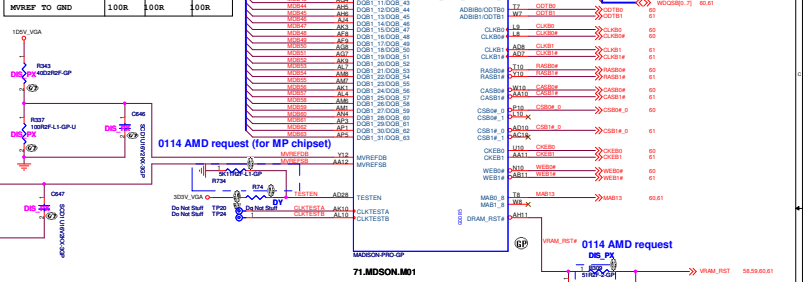
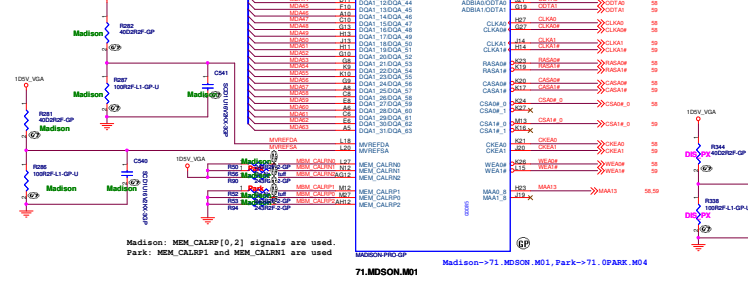




For SSTL-1.8/SSTL-2/DDRI/GDDR1: 0.5 \* VDDR1  
For DDR3/GDDR3/GDDR4/GDDR5: 0.7 \* VDDR1

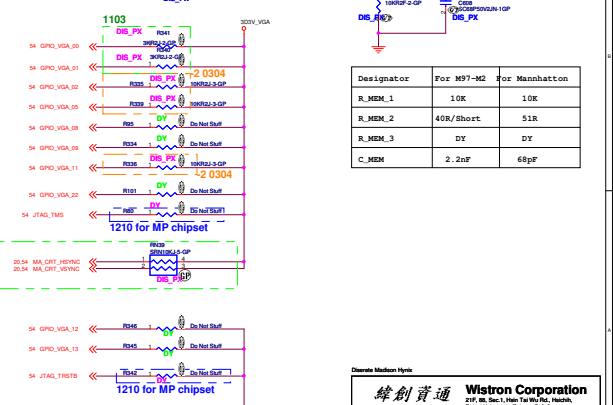
DIVIDER RESISTORS	GDDR5	DDR3	DDR3
VREF	1.5V	1.8/1.5V	1.5V
VREF TO PMR	40.2K	40.2K	40.2K
VREF TO GND	100K	100K	100K

DIVIDER RESISTORS	GDDR5	DDR3	DDR3
VREF	1.5V	1.8/1.5V	1.5V
VREF TO PMR	40.2K	40.2K	40.2K
VREF TO GND	100K	100K	100K



STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS (X: DO NOT PUT RESISTOR !, RETAIL VERSION! X: DESIGN DEPENDENT! N/A: NOT APPLICABLE)
TX_PWRS_ENB (Internal PD)	GP100	PCI FULL TX OUTPUT SWING Transmitter Power Savings Enable (= 50% Tx output swing = Full Tx output swing)	X
TX_DEEMPH_EN (Internal PD)	GP101	Transmitter de-emphasis enable = Tx de-emphasis disabled = Tx de-emphasis enabled	X
RESERVED	GP108	RESERVED	0
BIF_VGA_DIS	GP109	VGA ENABLED	0
RESERVED	GP1021	RESERVED	0
BIOS_ROM_EN	GP1022_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GP10[13,12,11]	BIOS ROM TYPE OR MEMORY APERTURE SIZE SELECT if $BIOS\_ROM\_EN=1$ , then Config[13:0] defines the ROM type if $BIOS\_ROM\_EN=0$ , then Config[13:0] defines the primary memory aperture size	XXX
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSVMC VGA_VSYNC	AUD[1:0] 0:Audio for DisplayPort and HDMI (if adapter is detected) 1:Audio for DisplayPort only 1:Audio for both DisplayPort and HDMI	X X

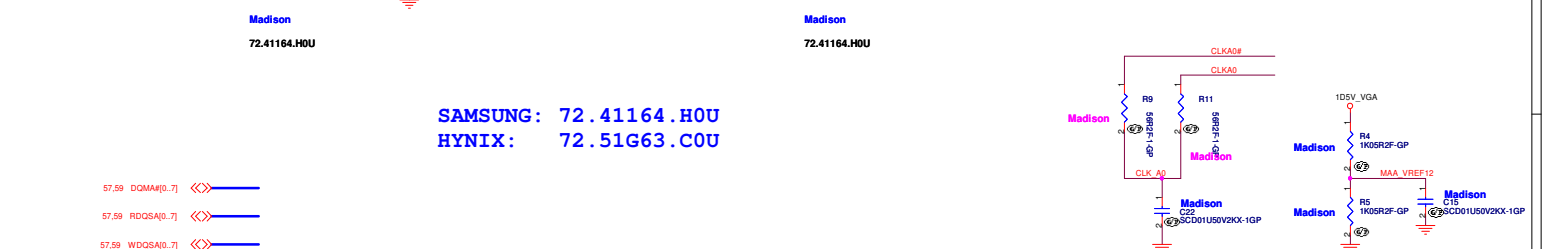
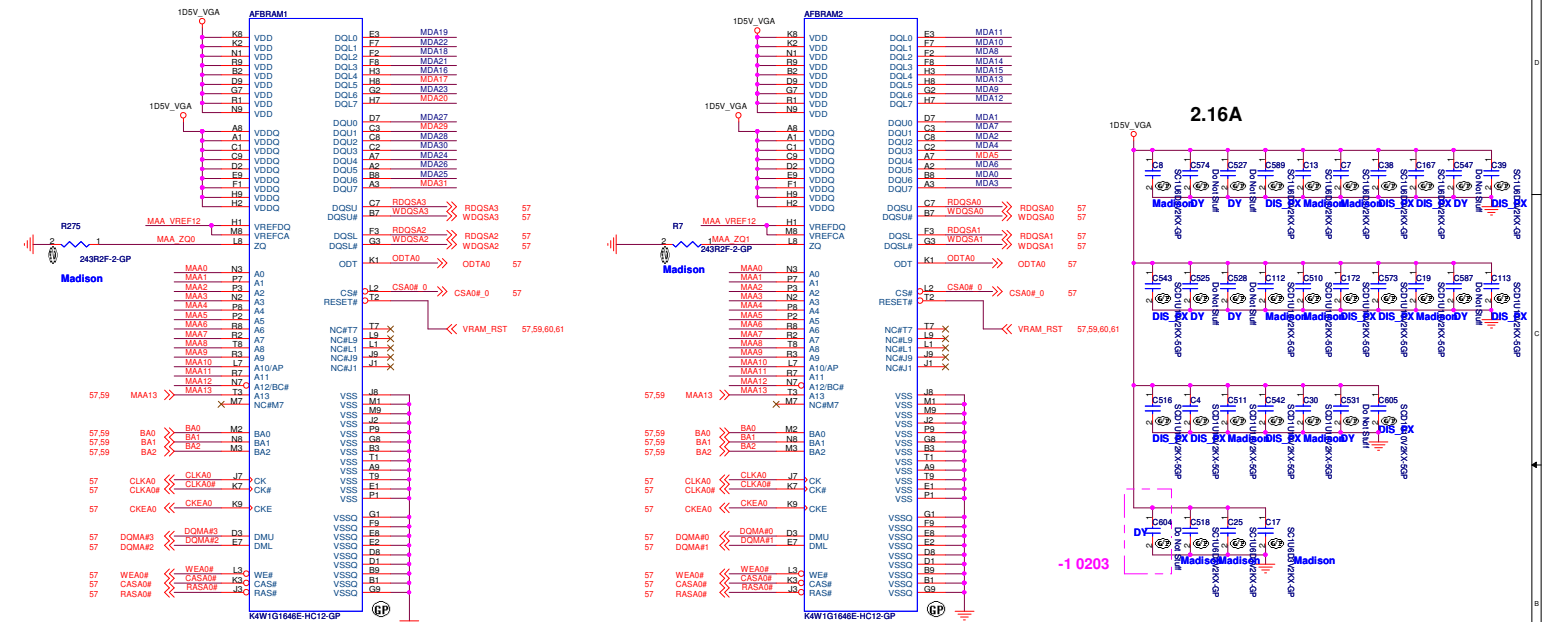
AMD RESERVED CONFIGURATION STRAPS			
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST HAVE COMPLEMENT SIGNALS			
H2SYNC, GENERICCC, GP102, GP1021			
If BIOS_ROM_EN (GP1022) = 0		If BIOS_ROM_EN (GP1022) = 1	
Size of the primary memory apertures	GP10[13,12,11]	Manufacturer	Part Number
128MB	x000	ST	M25P05A 0100
256MB	x001	Microelectronics	M25P10A 0101
512MB	x010		M25P40 0101
1GB	x		M25P80 0101
2GB	x	Winbond (formerly PMC)	W25Q128 0100
4GB	x		W25Q128 0101



Designator	For N97-MG	for Manhattan
R_MEM_1	10K	10K
R_MEM_2	40R/Short	51R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

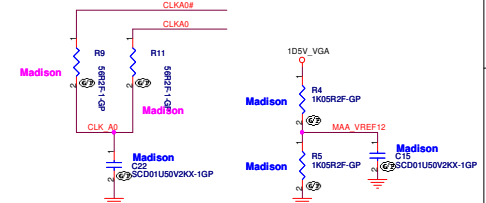
Wistron Corporation  
**緯創資通**  
 Document Number: JE40-DN  
 Revision: 1.0  
 Date: 2011.10

# DDR3



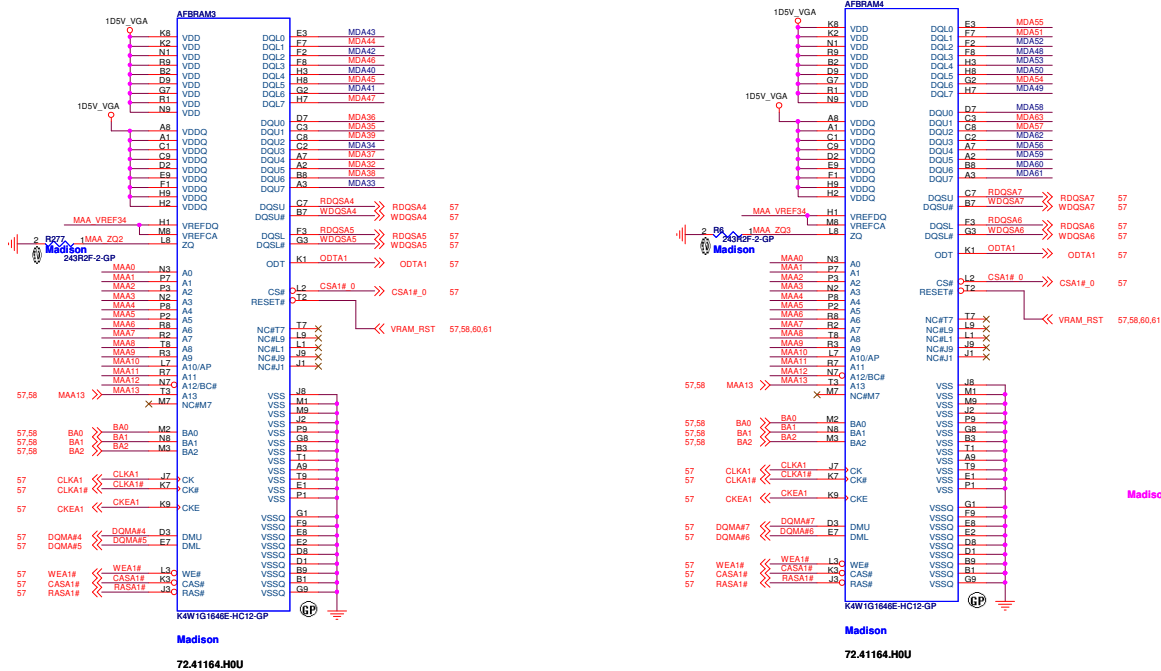
SAMSUNG: 72.41164.H0U  
 HYNIX: 72.51G63.COU

- 57.59 DQMA[0..7] <<>
- 57.59 RDQSA[0..7] <<>
- 57.59 WDQSA[0..7] <<>
- 57.59 MAA[0..12] <<> MAA[0..12]
- 57.59 MDA[0..63] <<> MDA[0..63]



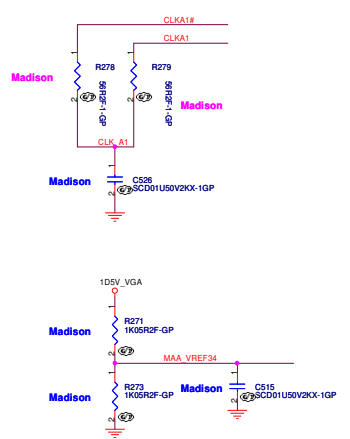
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File	VRAM(1/4)		
Size	Document Number	JE40-DN	
Date:	Monday, March 08, 2010	Sheet	58 of 63

# DDR3



SAMSUNG: 72.41164.H0U  
HYNIX: 72.51G63.CO0

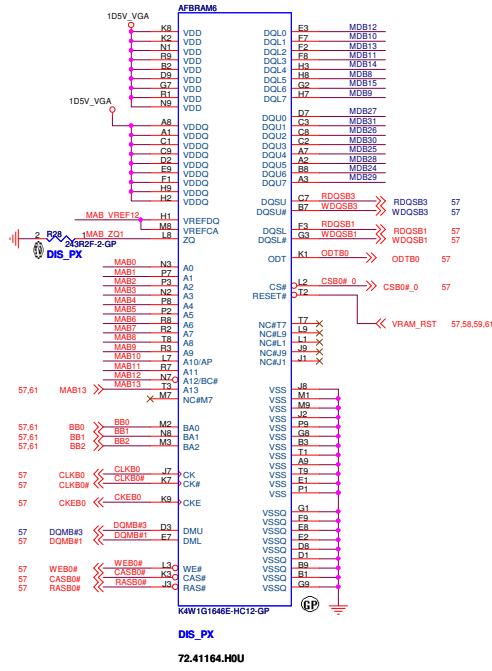
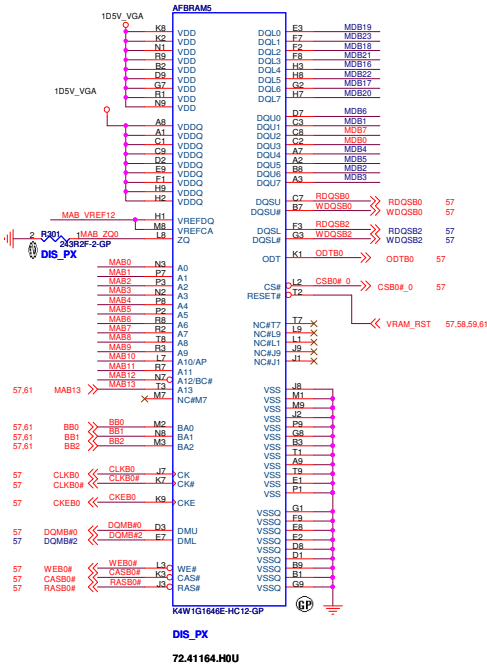
- 57.58 DQMA0[0..7] <<> DQMA0\_0[7]
- 57.58 RDQSA0[0..7] <<> RDQSA0\_0[7]
- 57.58 WDQSA0[0..7] <<> WDQSA0\_0[7]
- 57.58 MAA0[0..12] <<> MAA0\_0[12]
- 57.58 MDA0[0..63] <<> MDA0\_0[63]



Discrete Madison Hynix

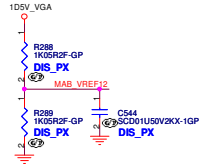
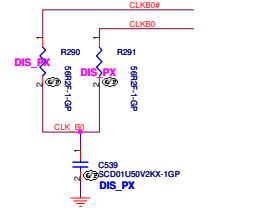
緯創資通 Wistron Corporation	
21F, 8th, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.	
File	
AS	
Document Number	
JE40-DN	
Date: Monday, March 08, 2010	Sheet 59 of 63

# DDR3



SAMSUNG: 72.41164.H0U  
 HYNIX: 72.51G63.CO0

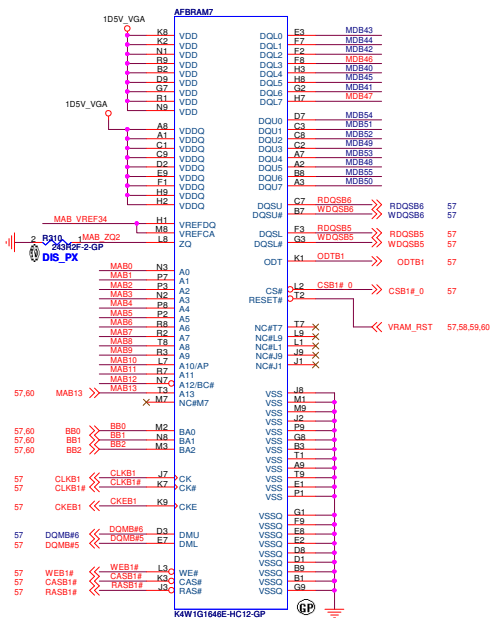
- 57.61 DQMB#0[0..7] <<>
- 57.61 RDQSB0[0..7] <<>
- 57.61 WDQSB0[0..7] <<>
- 57.61 MAB0[0..12] <<>
- 57.61 MAB0[0..63] <<>



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<b>Wistron Corporation</b> 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.	
Title: <b>VRAM(3/4)</b>	
Size: A3	Document Number: <b>JE40-DN</b>
Date: Monday, March 08, 2010	Rev: <b>-2</b>

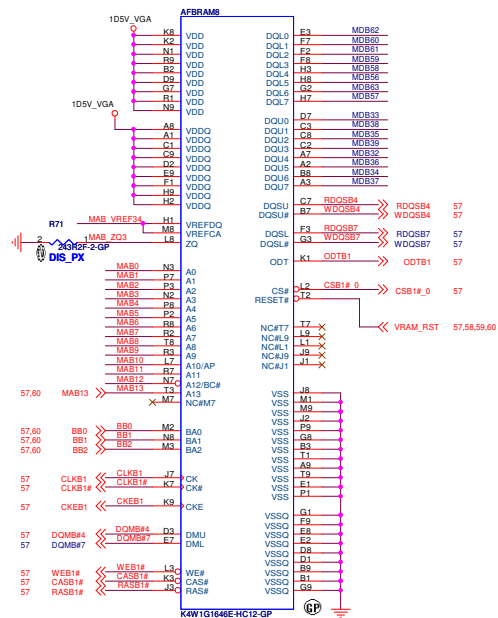
# DDR3



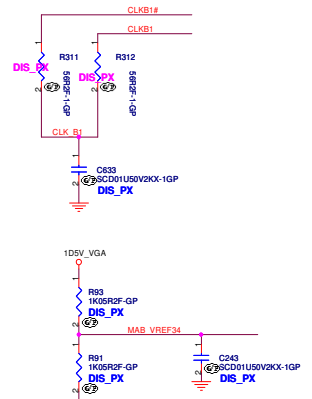
DIS\_PX  
72.41164.H0U

SAMSUNG: 72.41164.H0U  
HYNIX: 72.51G63.C0U

- 57.60 D0MB#0..7 <<>
- 57.60 RD0SB#0..7 <<>
- 57.60 WD0SB#0..7 <<>
- 57.60 MAB#0..12 <<>
- 57.60 MB#0..63 <<>

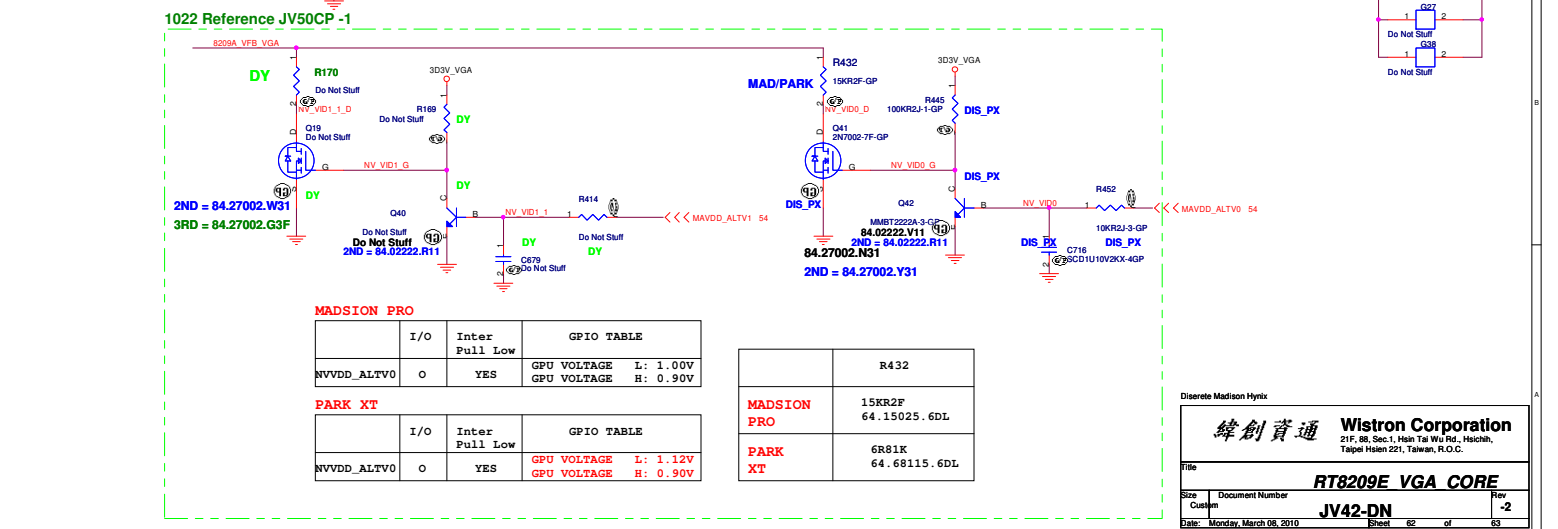
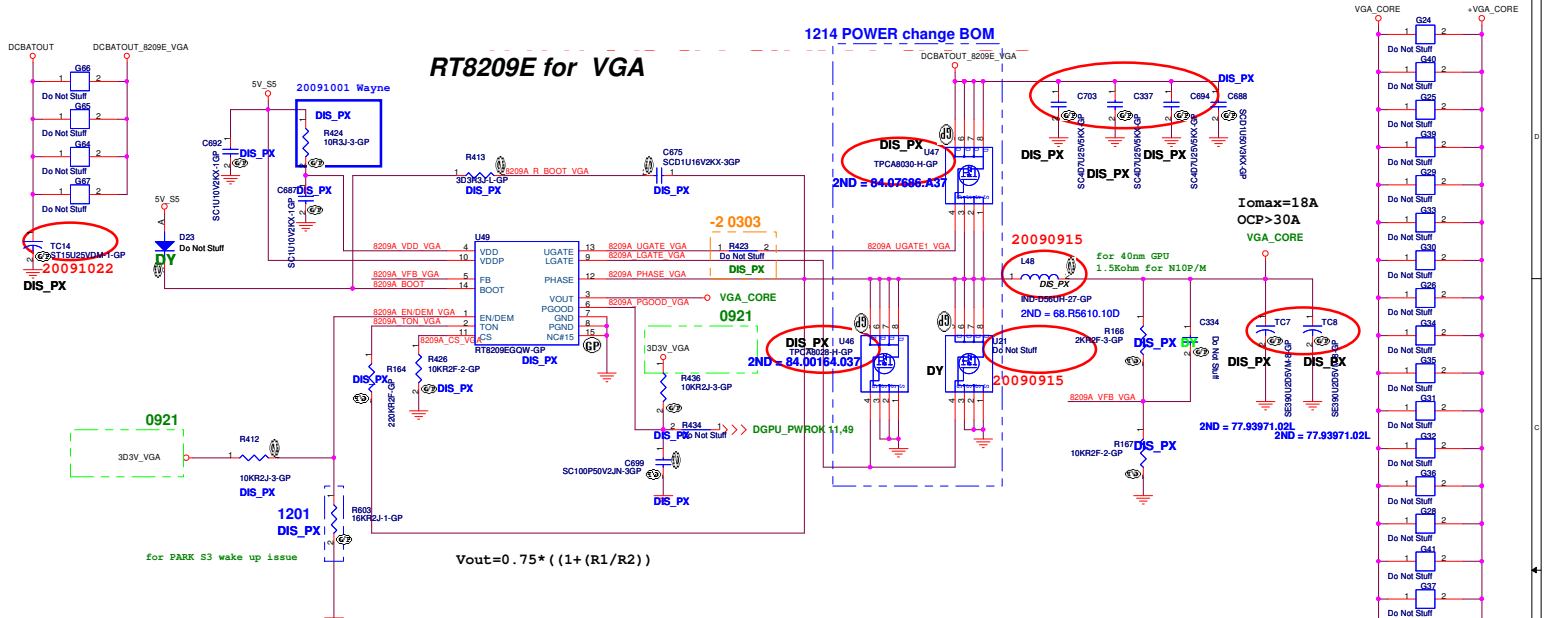


DIS\_PX  
72.41164.H0U



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File		
<b>VRAM(4/4)</b>		
Size	Document Number	Rev
A3	<b>JE40-DN</b>	-2
Date:	Monday, March 08, 2010	Sheet 61 of 63



NB  
RS780-->RS880M  
71.RS780.M02-->71.RS880.M02

BOM  
1st -> All SKU

SB  
SB820M-1-GP  
71.SB820.00U-->71.SB820.M03

SATA\_CALRP  
A11: 80歐姆 1% resistor to GND  
A12: TBD歐姆 1% resistor to GND

SATA\_CALRN  
A11:A11: 931歐姆 1% resistor to VDDAN\_11\_SATA  
A12: TBD歐姆 1% resistor to VDDAN\_11\_SATA.

R250  
Madison-->R250 64.32425.6DL R402H16 32K4R2F  
Park -->R250 64.32425.6DL R402H16 32K4R2F  
PX -->R250 64.32425.6DL R402H16 32K4R2F

VGA  
Madison--> PN:71.MDSON.M01  
Park--> PN:71.OPARK.M04

VRAM  
Samsung-->VRAM FBRAM1~8 PN:VR.1GB0B.006  
Hynix--> VRAM FBRAM1~8 PN:VR.1GB0G.004  
ATI--> VRAM FBRAM1~8 PN: VR.1GB0T.002

CRT  
UMA-->L1-->2R 0603  
C62-->47U/6.3V  
DIS-->L1-->Bead(L1 68.00217.711 L1608-UH38 SBK160808T-221Y-N-GP)  
C62-->DY  
PX--> 133 歐姆 (R58 63.10334.1DL R402H16 133R2F-GP)

R605(MAD/PARK/PX)  
Madison-->R605 64.15005.6DL R402H16150R2F-L-GP  
Park -->R605 64.15005.6DL R402H16150R2F-L-GP  
PX -->R605 64.15005.6DL R402H16150R2F-L-GP

HDMI  
UMA -->R612 R613 R618 R619 R620 R621 R624 R625 64.71505.6DL CHIP RES 715 F 1/16W 0402

R432(MAD/PARK)  
Madison-->15KR2F 64.15025.6DL  
Park-->R432 64.68115.6DL R402H16 6.81KR2F

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緯創資通		Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
NOTE		
Size A3	Document Number	Rev
	JV42-DN	-2
Date: Monday, March 08, 2010	Sheet 63	of 63