



# V40SA1 Schematics Rev:C

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PCB  
37GV30100-C0

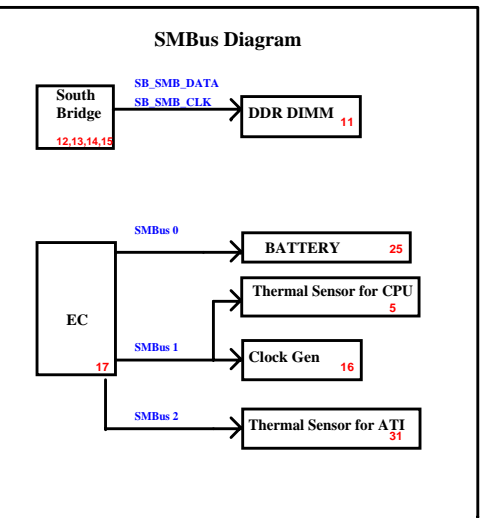
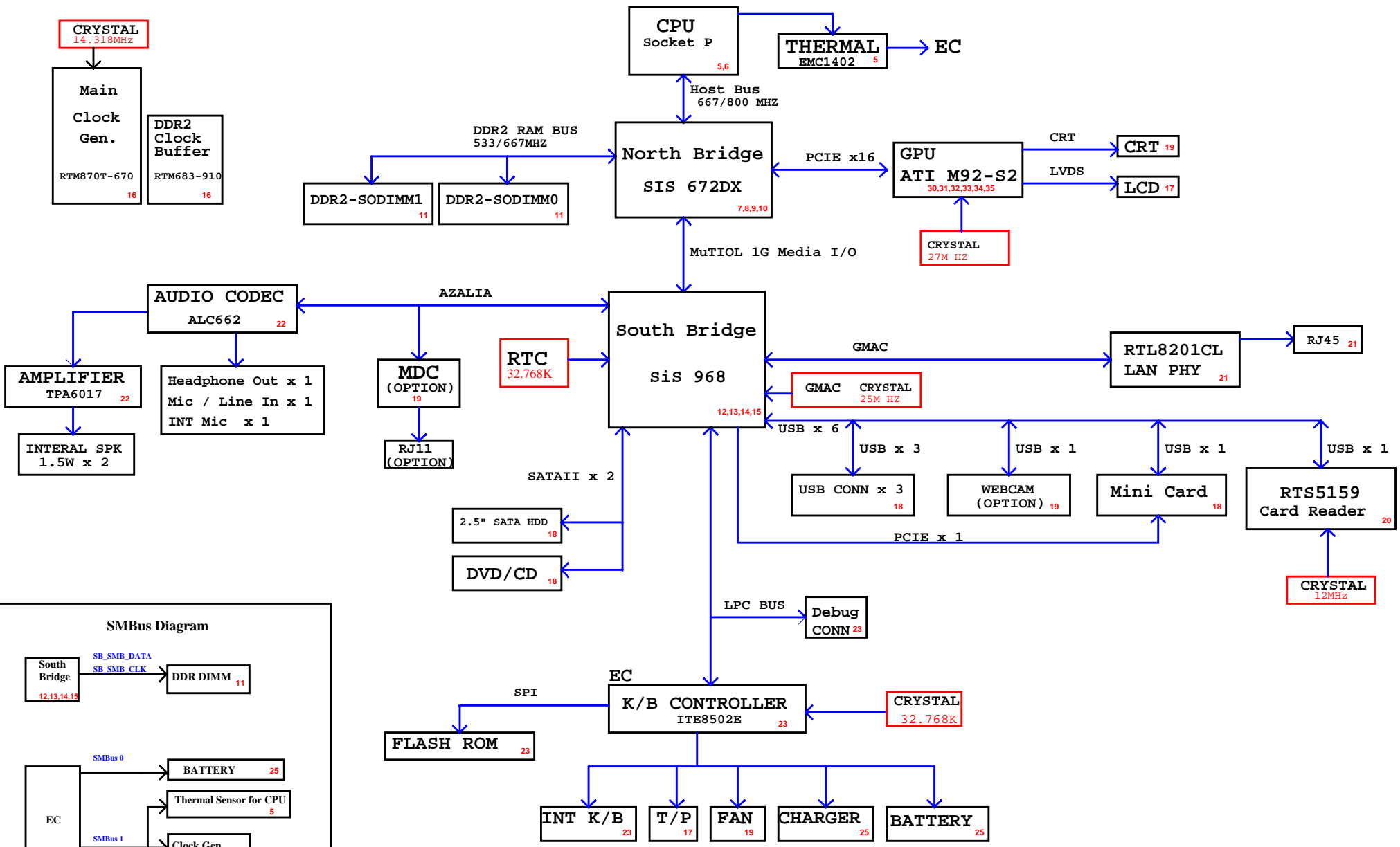
MB	Revision History	
A	12/18/08	Initial REV.A
B	02/11/09	Release REV.B
C	04/08/09	Release REV.C
01		

## V40SA1 REV.C P/N LIST

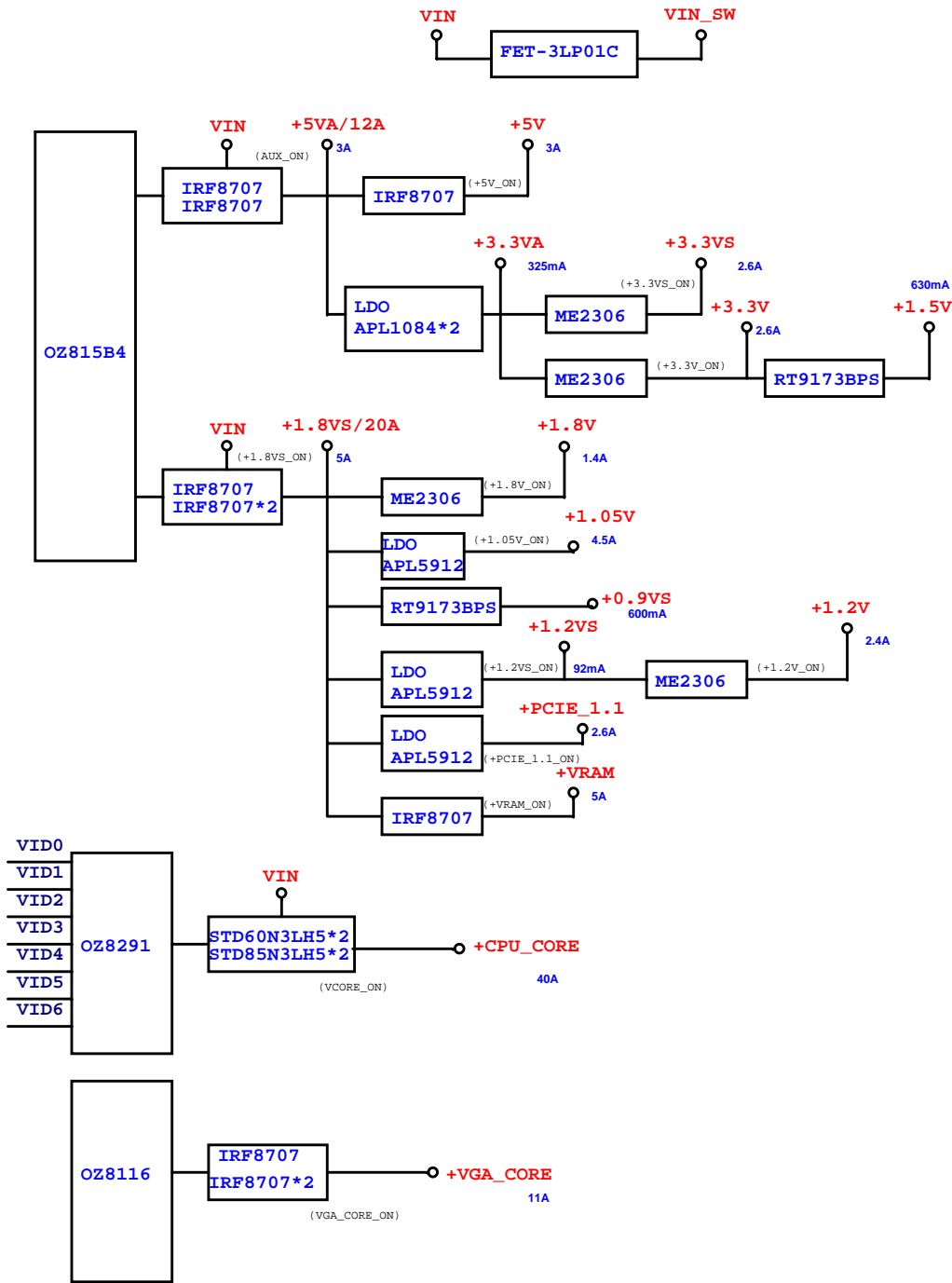
	PCB P/N	PCB ASSY P/N
Initial REV.A		
MB BD	37GV30100-A0	82GV30100-A0
LID BD	35GWV3010-A0	80GWV3010-A0
Release REV.B		
MB BD	37GV30100-B0	82GV30100-B0
LID BD	35GWV3010-B0	80GWV3010-B0
Release REV.C		
MB BD	37GV30100-C0	82GV30100-C0
LID BD	35GWV3010-C0	80GWV3010-C0

# V40SA1

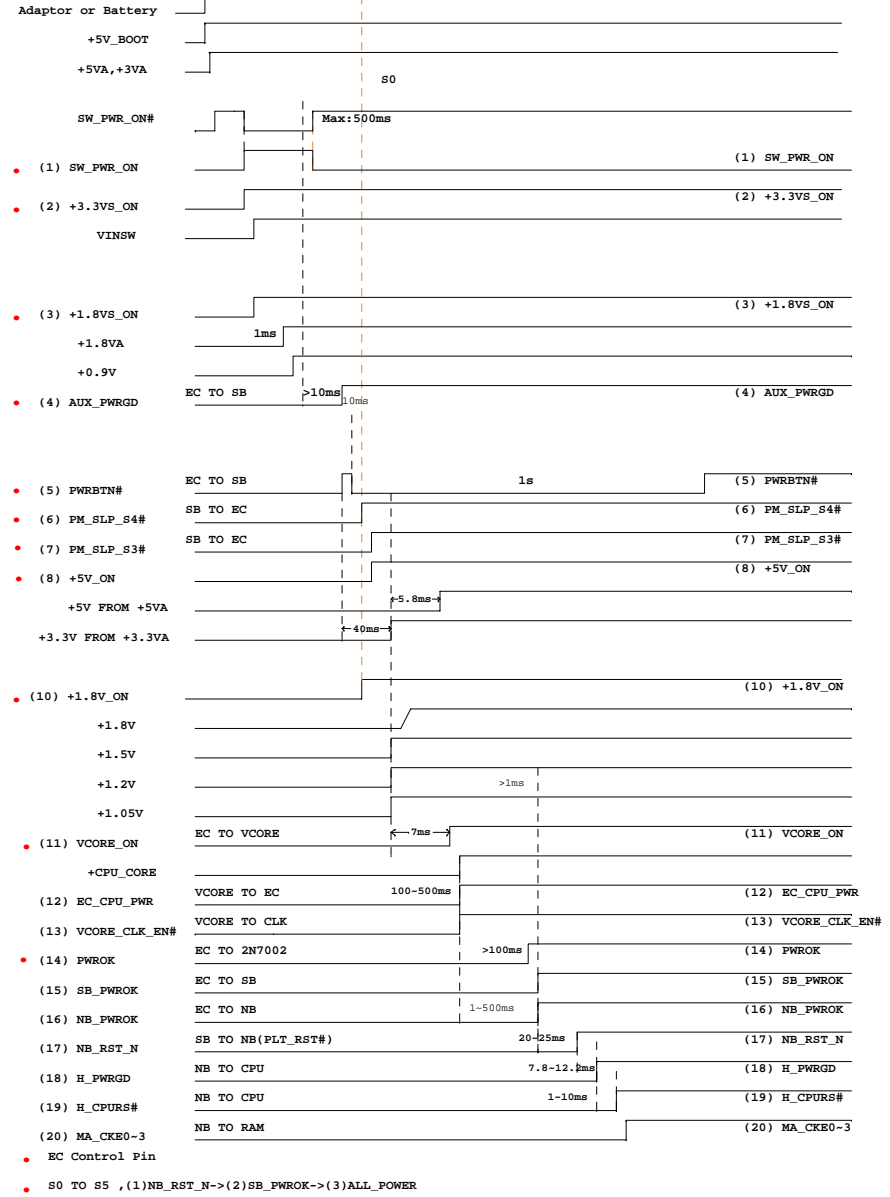
## SYSTEM BLOCK DIAGRAM



# POWER BLOCK DIAGRAM



# POWER Sequence (update later)



SIS968 GPIO	
GPIO0	EC_EXTSMI#
GPIO1	NC
GPIO2	PM_THROTTLING#
GPIO3	EC_EXTSCI#
GPIO4	NC
GPIO5	NC
GPIO6	NC
GPIO7	PCIE_WAKE
GPIO8	NC
GPIO9	NC
GPIO10	PM_SLP_S4#
GPIO11	AGPSTOP_N
GPIO12	CPU_DPSP#
GPIO13	PM DPRSLPVR
GPIO14	NC
GPIO15	PM_SLP_S3#
GPIO16	NC
GPIO17	H_A20GATE
GPIO18	H_RCIN#
GPIO19	SB_SMB_CLK
GPIO20	SB_SMB_DATA

ITE8502E GPIO	
GPA0	BTL_BEEP
GPA1	EC_BL_PWM
GPA2	AUX_PWRGD
GPA3	RF_LED
GPA4	WEBCAM_ON
GPA5	ODD_DET
GPA6	RF_ON
GPA7	VGA_CORE_ON
GPB0	SENBAT_V
GPB1	USB0_EN#
GPB2	+1.2V_ON
GPB3	BAT_SMBCLK
GPB4	BAT_SMBDAT
GPB5	H_A20GATE
GPB6	H_RCIN#
GPB7	MUTE_AMP#
GPC0	+PCIE_1.2_ON
GPC1	SMBCLK_EC
GPC2	SMBDAT_EC
GPC3	VDDR3_ON
GPC4	PWR_KEEP
GPC5	NC
GPC6	SB-PWRBTN#
GPC7	SB_RTCRST
GPD0	AC_IN
GPD1	NC
GPD2	PLT_RST#
GPD3	EC_EXTSCI#
GPD4	EC_EXTSMI#
GPD5	PWROK
GPD6	PM_THROTTLING#
GPD7	DELAY_VR_PWRGOOD
GPE0	+3.3VS_ON
GPE1	Low Voltage
GPE2	CHG_G_LED
GPE3	NC
GPE4	PWRON
GPE5	CHG_R_LED
GPE6	NC
GPE7	USB1_EN#
GPF0	H_SB_PROCHOT#
GPF1	+VRAM_ON
GPF2	CPU_BSEL0
GPF3	CPU_BSEL1
GPF4	TP_CLK
GPF5	TP_DATA
GPF6	SMB_CLK_VGA
GPF7	SMB_DATA_VGA
GPG0	LCDSW
GPG1	+3.3V_ON
GPG2	FLFRAME#
GPG6	LID#
GPH0	VCORE_ON
GPH1	+1.2VS_ON
GPH2	+5V_ON
GPH3	+1.8V_ON
GPH4	+1.05V_ON
GPH5	+1.8VS_ON
GPH6	PWR_LED

ITE8502E GPIO	
GPI0	BATT_TEMP
GPI1	ADAPTOR_I
GPI2	BAT_V
GPI3	BAT_I
GPI4	PM_SLP_S4#
GPI5	PM_SLP_S3#
GPI6	NC
GPI7	CPU_PWR
GPJ0	Fast-charge-EN
GPJ1	CHG_I
GPJ2	FAN_CTRL0
GPJ3	CHG_ON
GPJ4	EC_BRGHT
GPJ5	SET_V

CPU				
	CPU CORE (V)	ICC (mA)	W	TEMP ( )
2.0G	1.525	35.7	54.3	69
2.2G	1.525	37.5	57.1	70
2.26G	1.525	38.1	58.0	70
2.4G	1.525	39.3	59.8	71
2.5G	1.525	40	61.0	72
2.53G	1.525	40.4	61.5	72
2.6G	1.525	41.05	62.6	72
2.66G	1.525	43.35	66.1	74
2.8G	1.525	44.86	68.4	75
3.06G	1.525	55.9	85.2	81
VCC	ICC (mA)	W	TEMP ( )	
+1.5V	130	0.195	70	
+1.05V	4500	4.725		

M672FX			
VCC	ICC (mA)	W	TEMP ( )
+1.2V	3218	3.86	70
+1.8V	1189	2.14	
+1.05V	80	0.084	

SIS968			
VCC	ICC (mA)	W	TEMP ( )
+3.3V	95	0.314	70
+1.8V	1252	2.253	
+1.05V	22	0.023	

307ELV			
VCC	ICC (mA)	W	TEMP ( )
+3.3V	236	0.778	70
+1.8V	681	1.225	

CLOCK GENERATOR+BUFFER			
VCC	ICC (mA)	W	TEMP ( )
+3.3V	400	1.32	70
+1.8V	300	0.54	

ITE8502E			
VCC	ICC (mA)	W	TEMP ( )
+3.3V	200	0.66	70
+3.3VA	500	1.65	

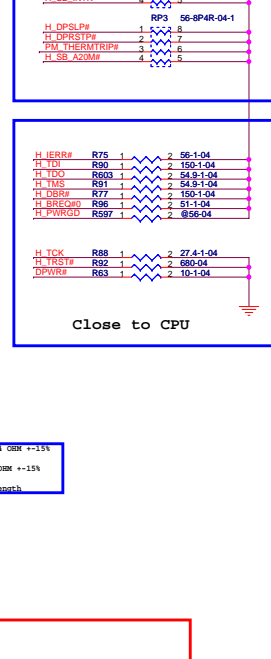
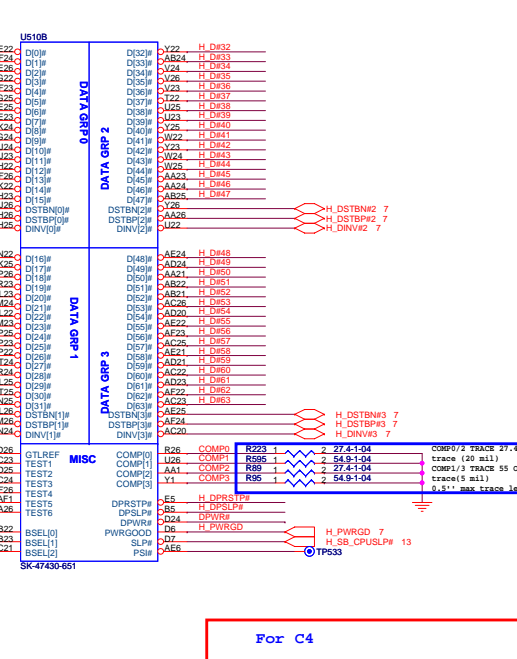
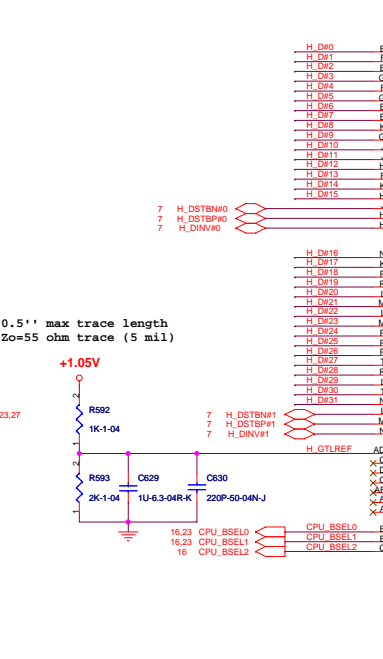
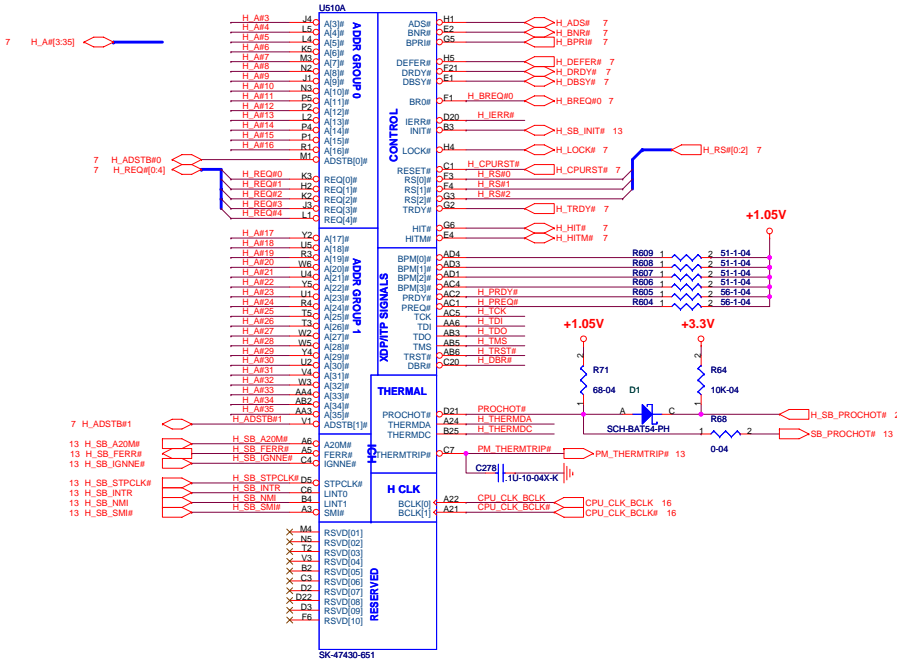
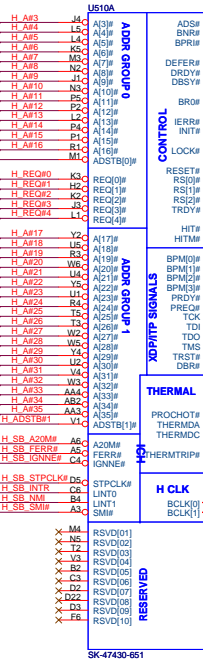
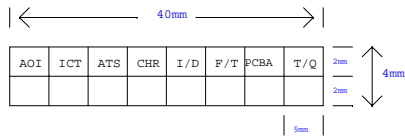
RTS5159			
VCC	ICC (mA)	W	TEMP ( )
+3.3V	293	0.966	85

RTL8201CL			
VCC	ICC (mA)	W	TEMP ( )
+3.3V	120	0.396	85

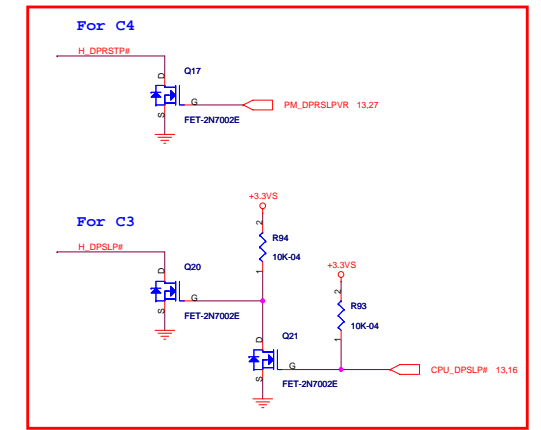
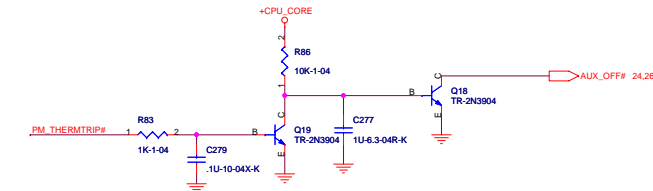
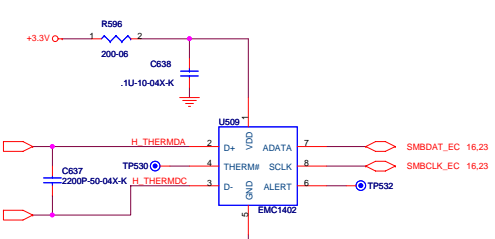
ALC662			
VCC	ICC (mA)	W	TEMP ( )
+3.3V	23	0.075	70
+5VA	38	0.19	

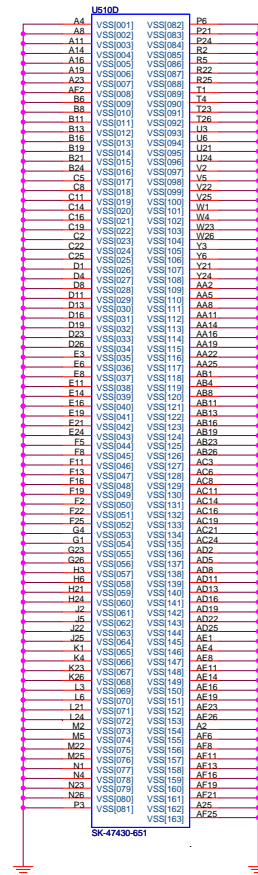
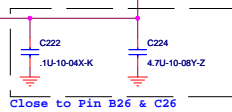
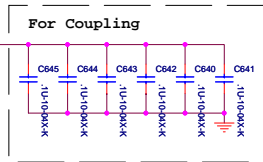
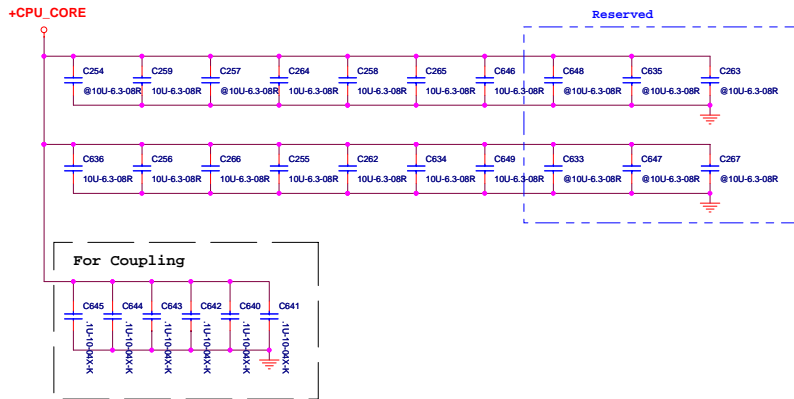
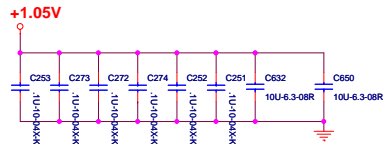
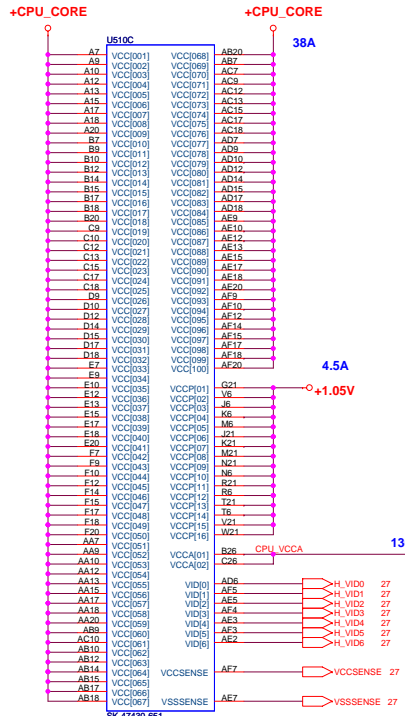
APA2068			
VCC	ICC (mA)	W	TEMP ( )
5V	20	0.1	85

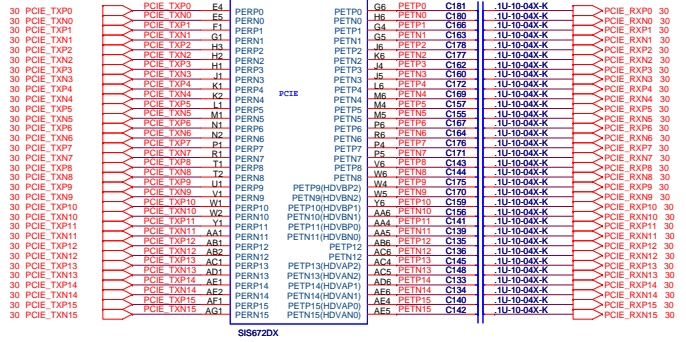
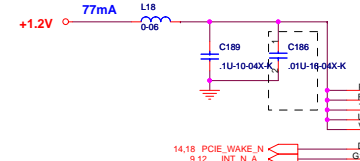
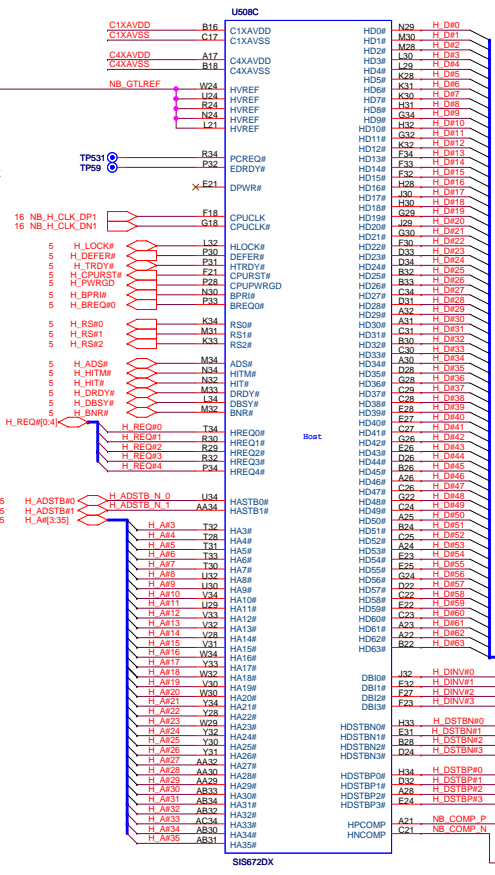
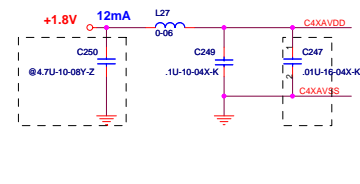
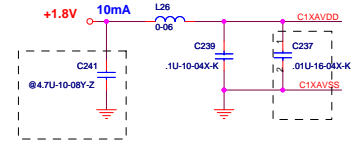
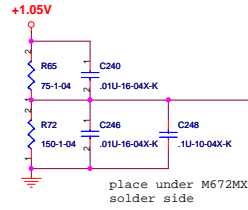
BMC1402			
VCC	ICC	W	TEMP ( )
+3.3V	150uA	0.495mW	140.8



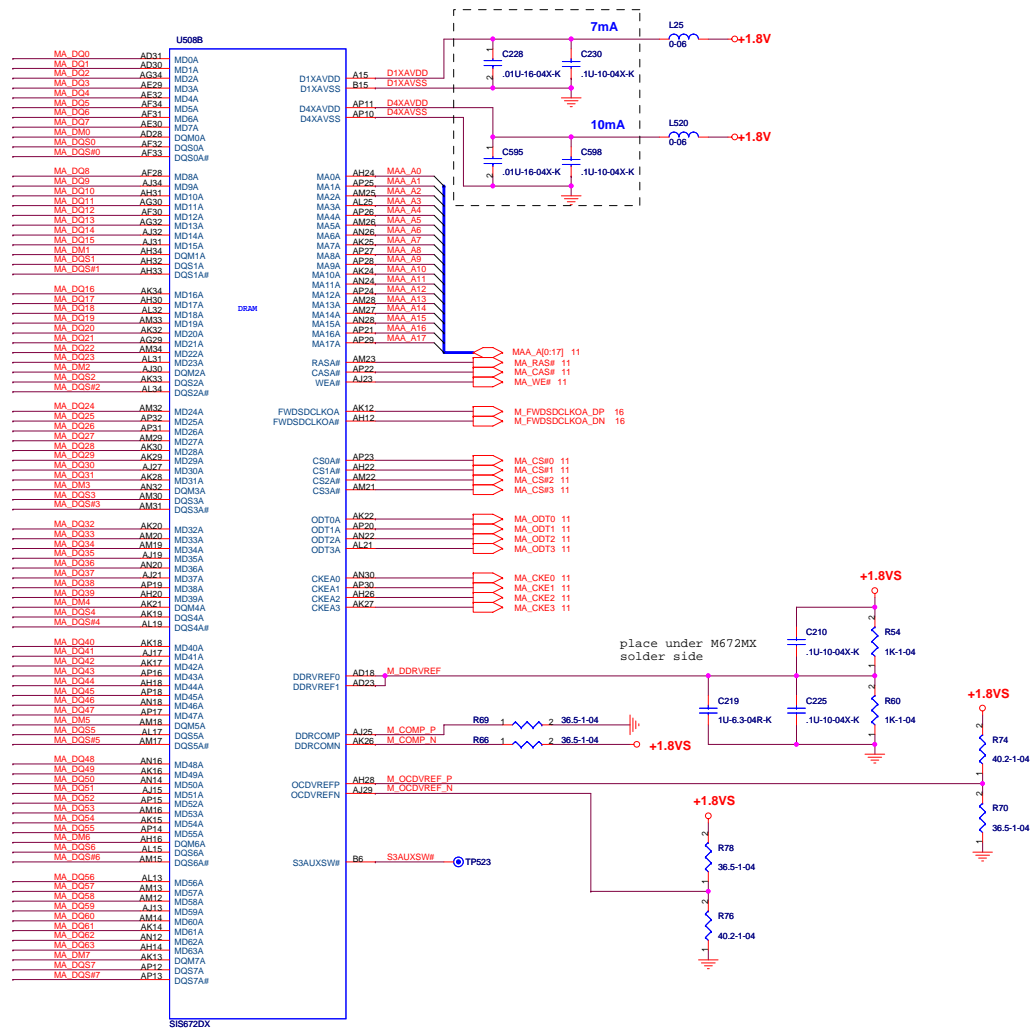
**CPU Thermal Sensor**



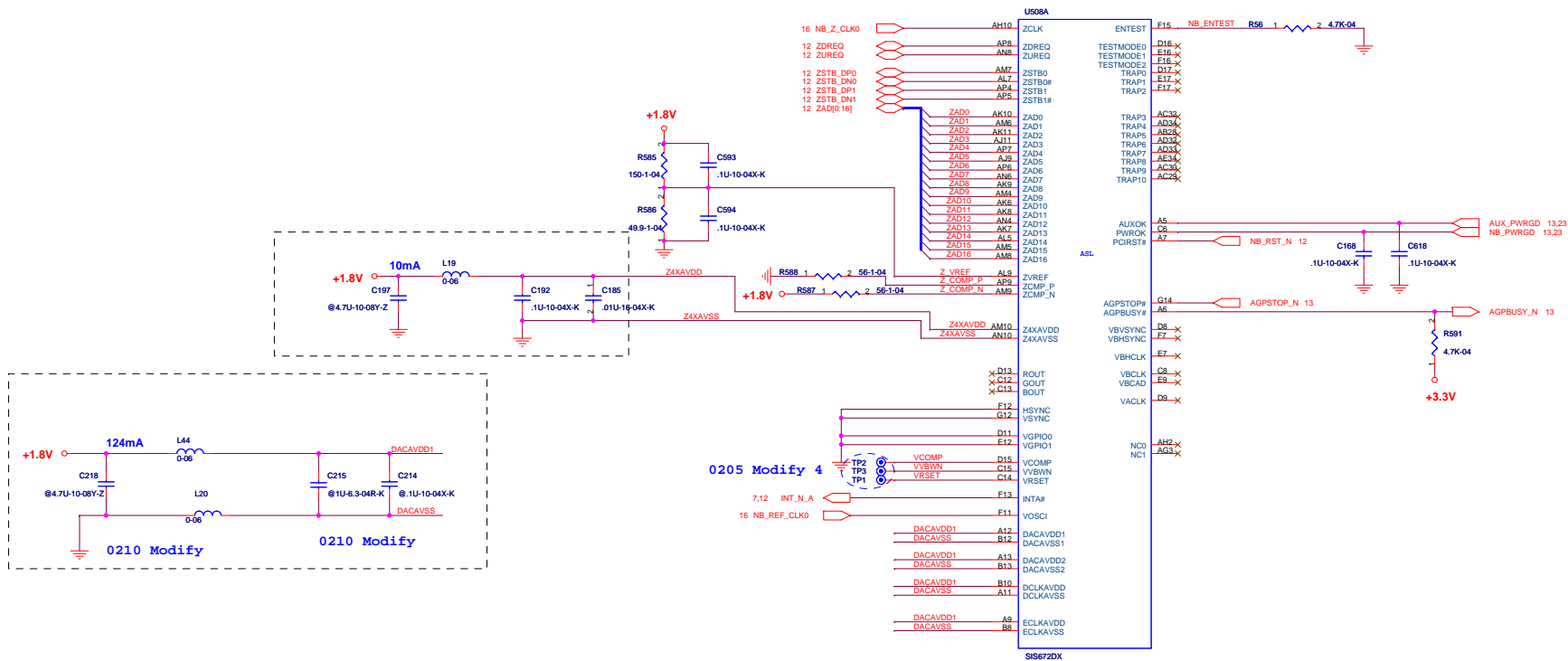




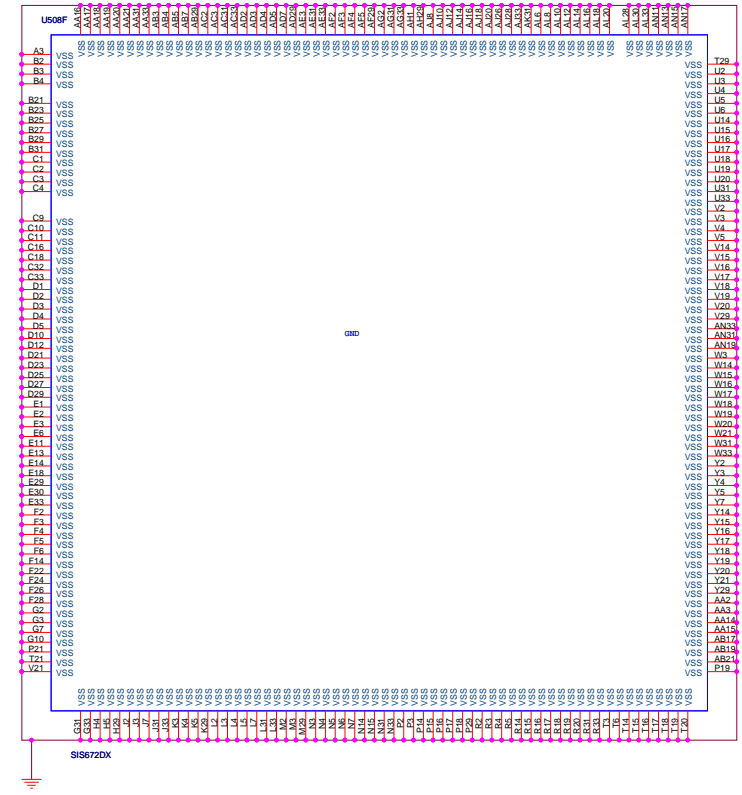
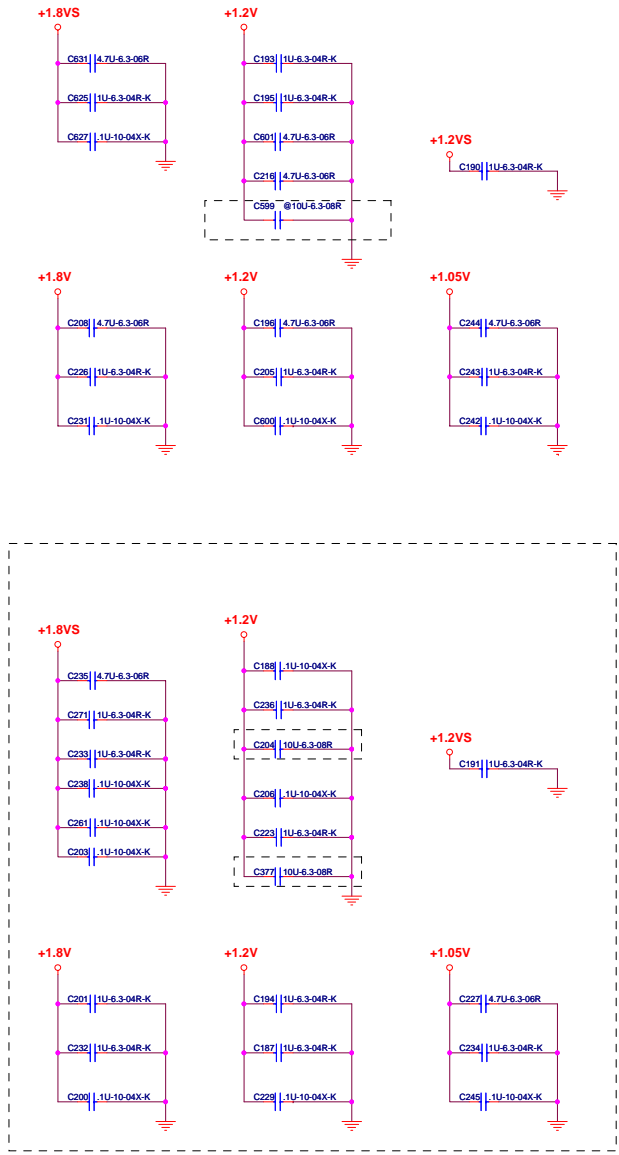
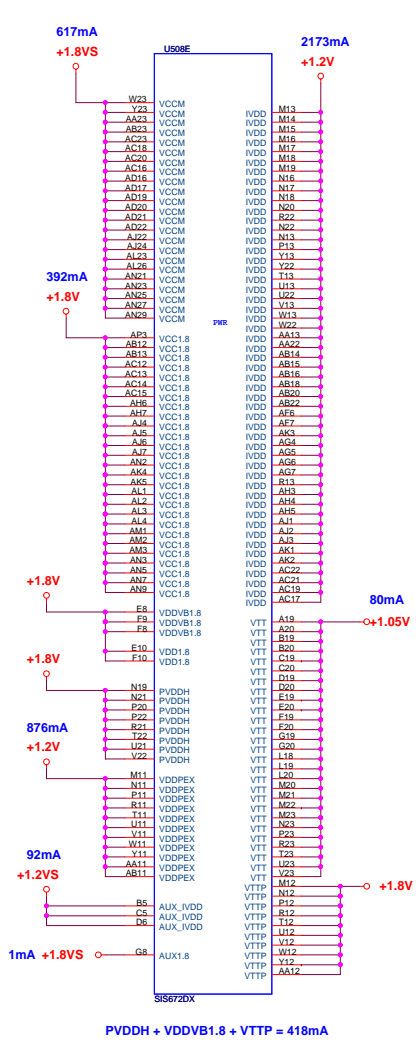
- MA\_DQ[0:63] 11
- MA\_DS[0:7] 11
- MA\_DS# [0:7] 11
- MA\_DM[0:7] 11

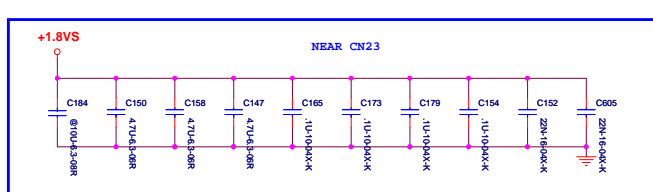
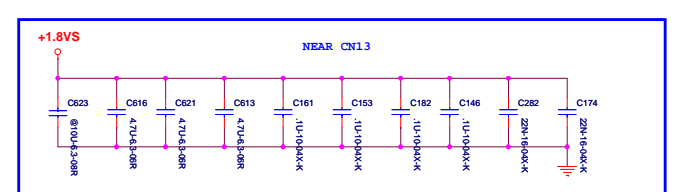
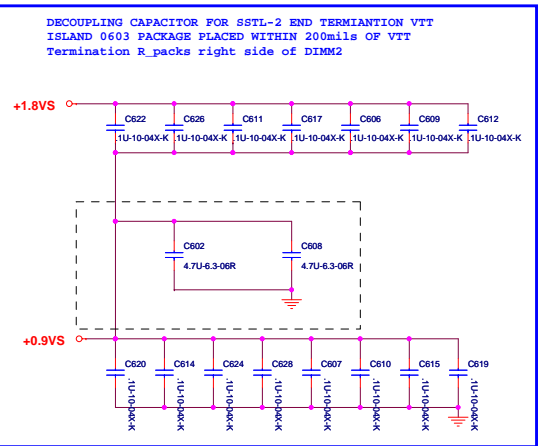
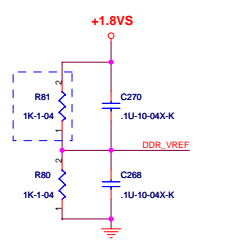
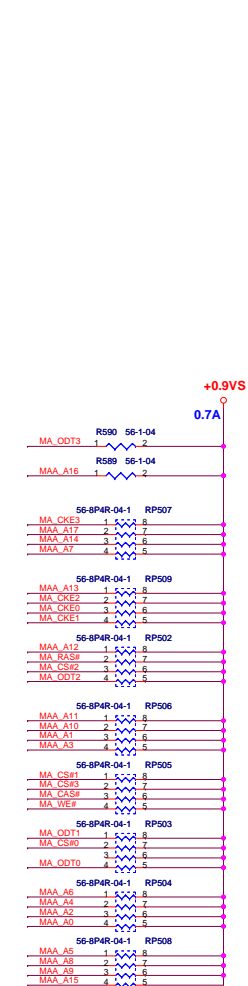
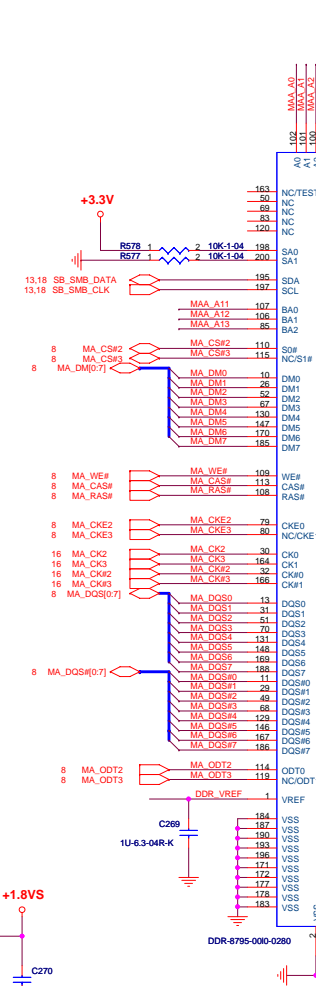
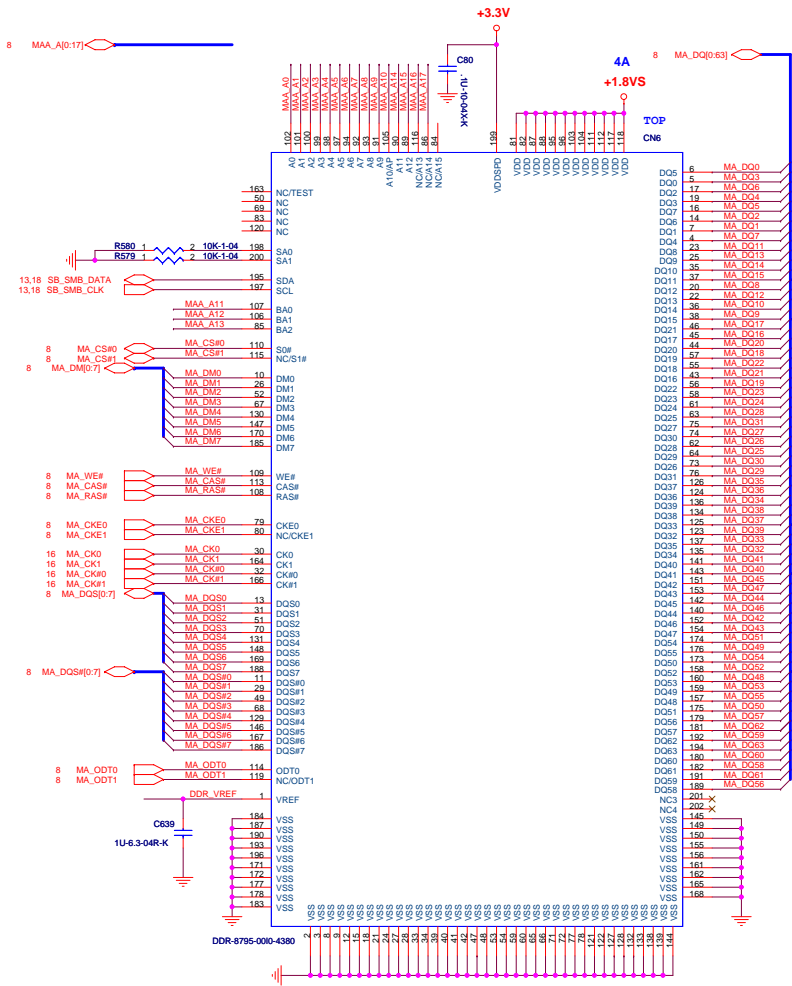


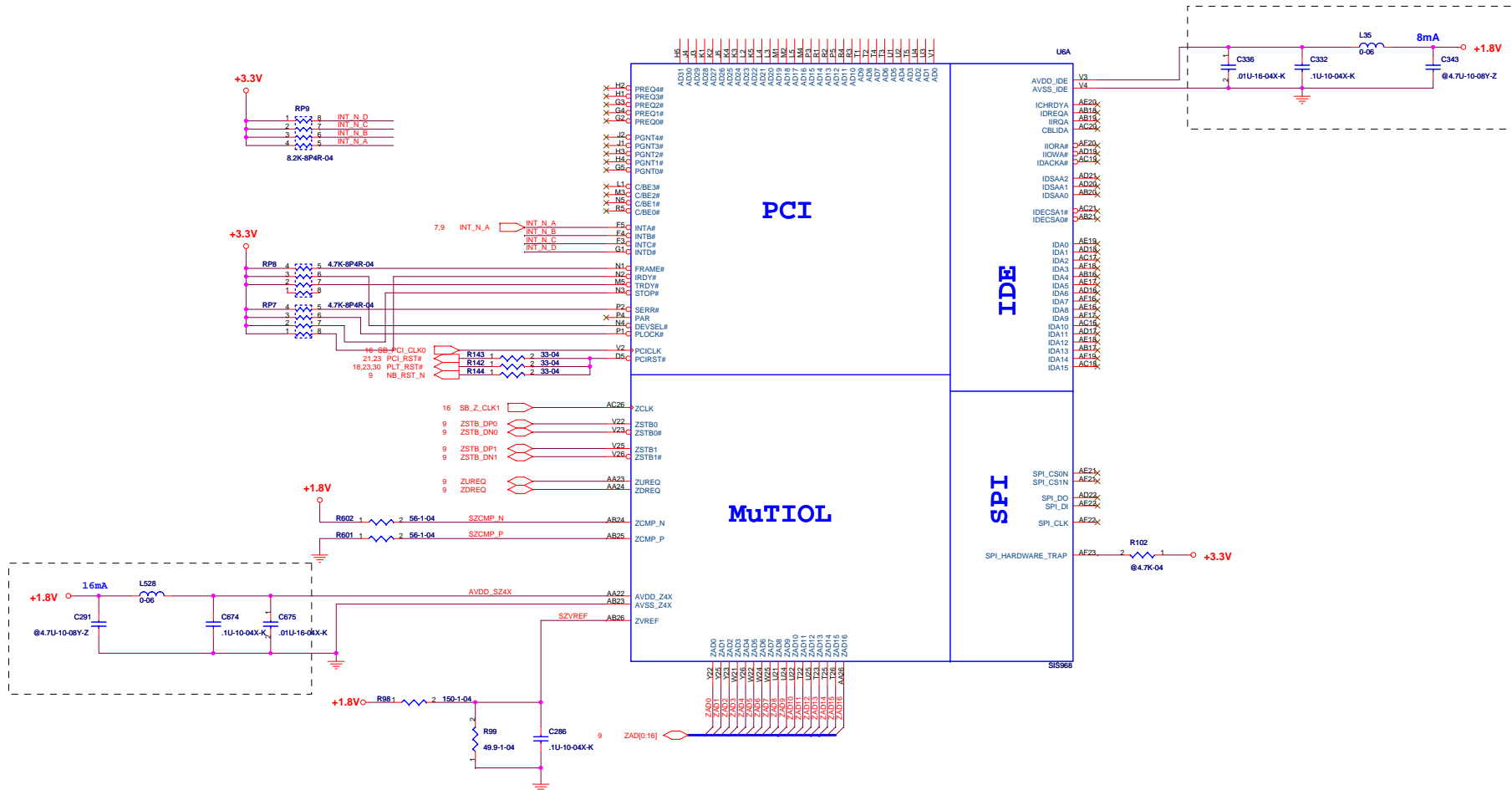


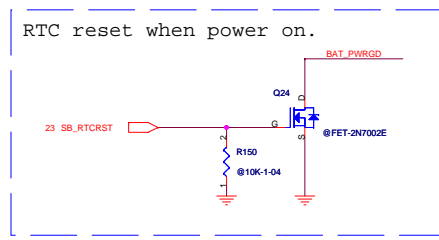
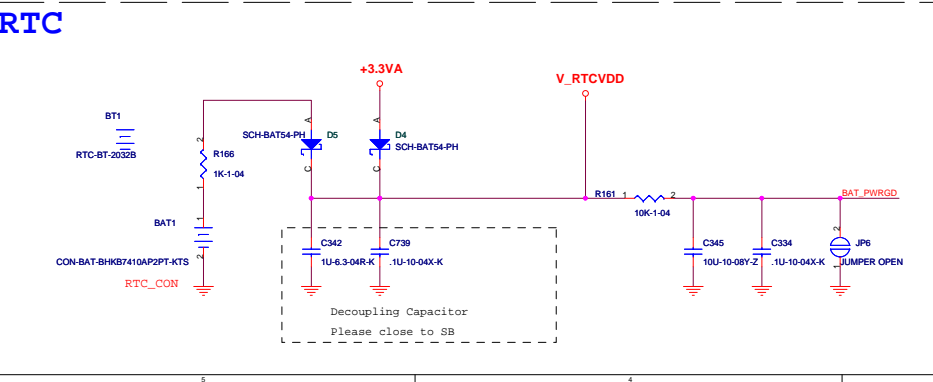
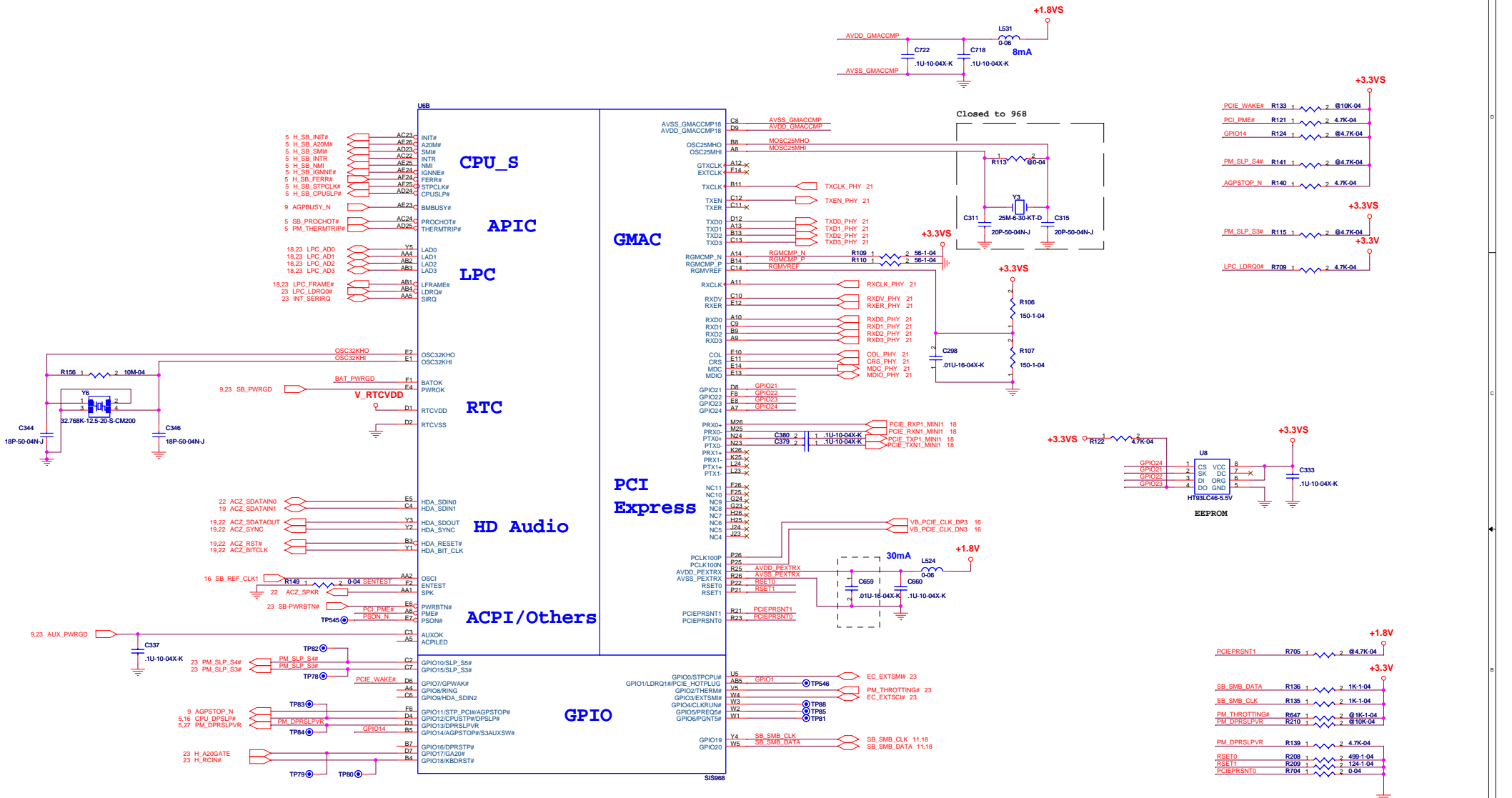


DACAVDD1 Spec.  
 Voltage: 1.5V +/- 5%  
 Current: 100mA  
 R51use a 3.3 ohm resistor make a voltage drop about 0.3V to meet the voltage above.



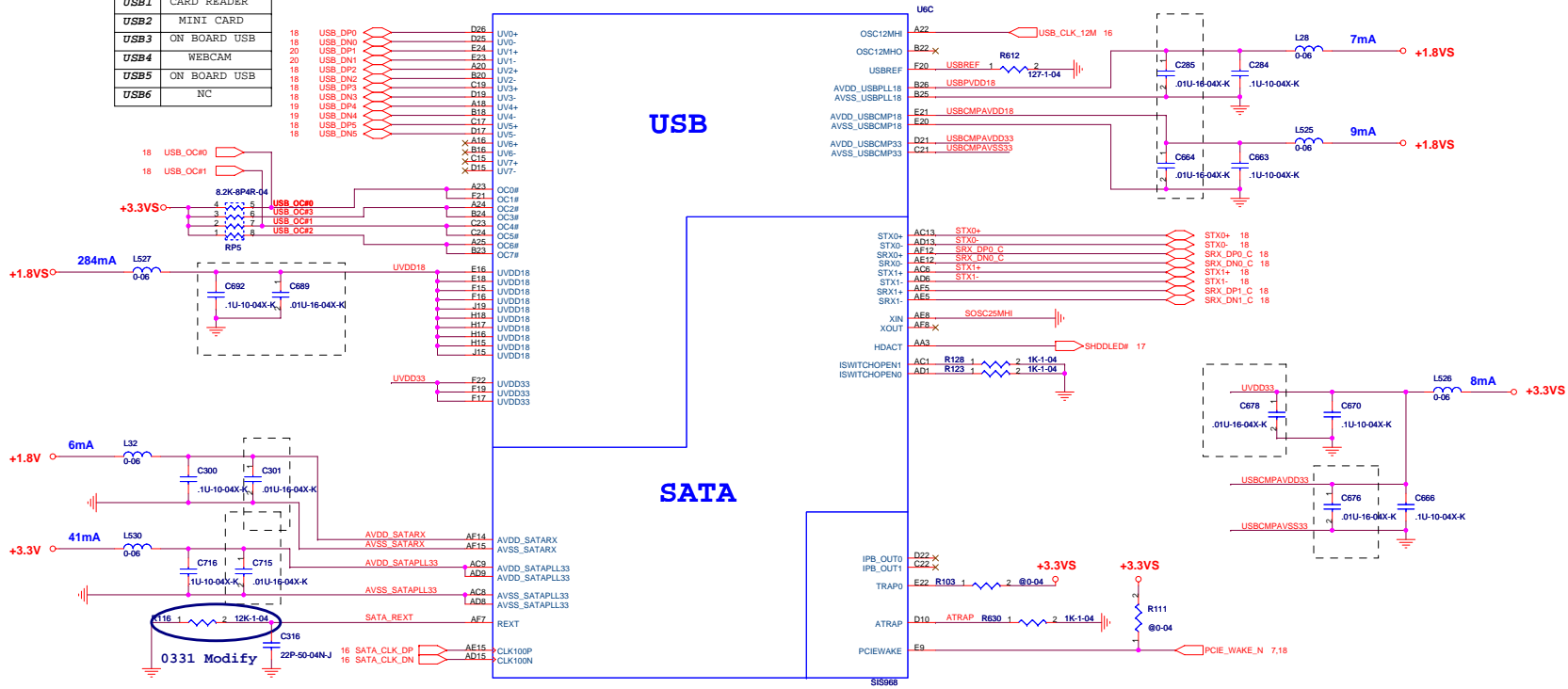


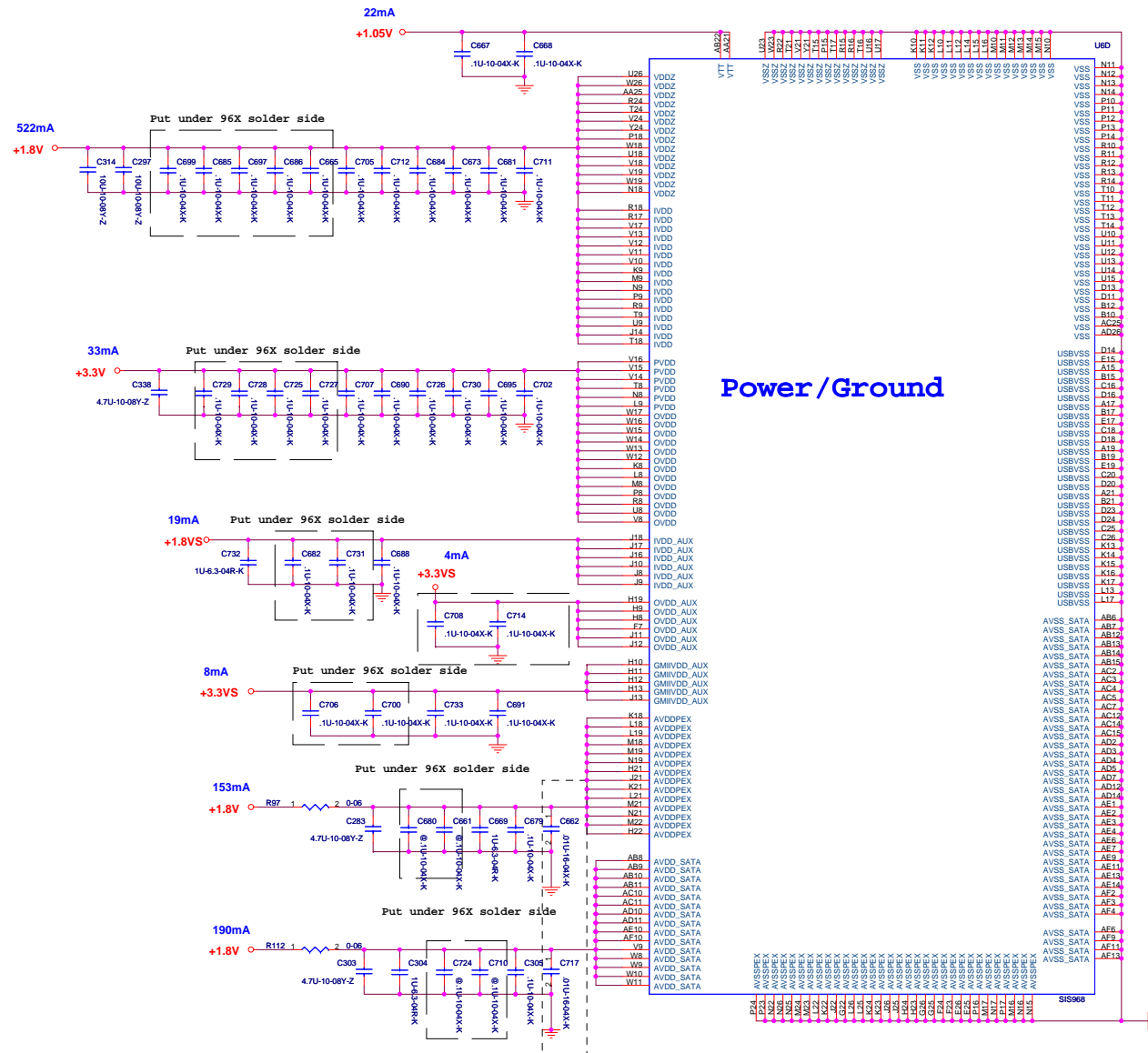


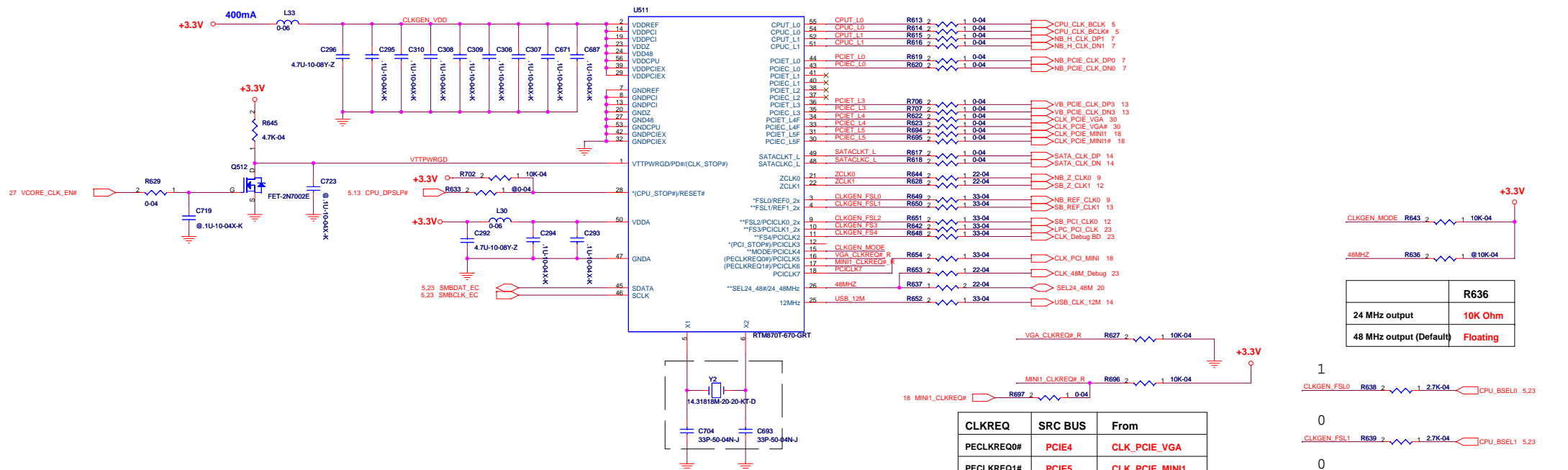


<b>Elitegroup Computer Systems</b>	
Title: <b>Project : V40SA</b>	
Size: <b>Document Number</b>	968_PCIE_LAN_GPIO
Schema: <b>SCHEMATIC1</b>	Rev: <b>C</b>
Date: <b>Wednesday, April 05, 2006</b>	Sheet: <b>13 of 37</b>

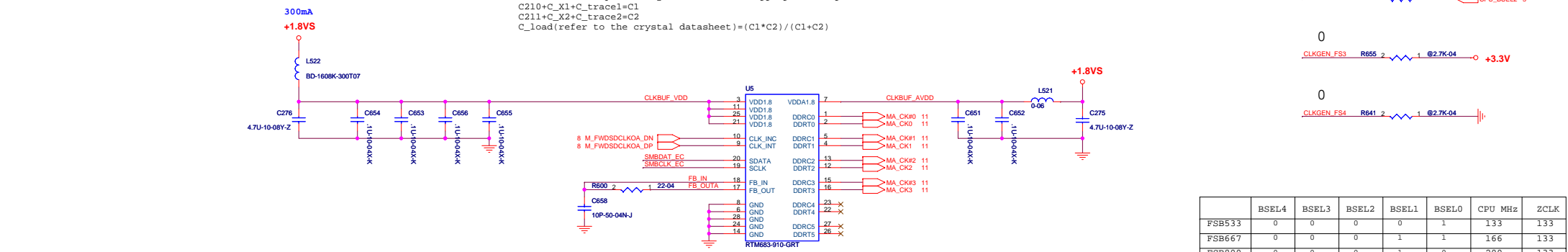
V40SAX	
USB0	ON BOARD USB
USB1	CARD READER
USB2	MINI CARD
USB3	ON BOARD USB
USB4	WEBCAM
USB5	ON BOARD USB
USB6	NC





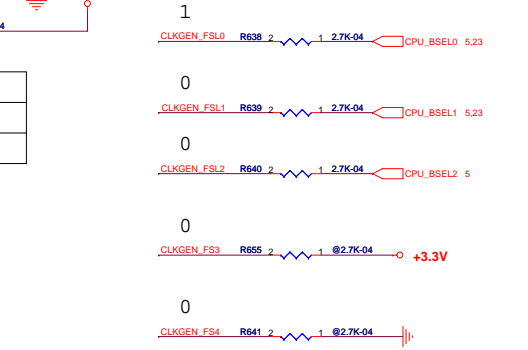


Please base on your design to choose the appropriate capacitor value.  
 $C_{210} + C_{X1} + C_{trace1} = C1$   
 $C_{211} + C_{X2} + C_{trace2} = C2$   
 $C_{load} (refer\ to\ the\ crystal\ datasheet) = (C1 * C2) / (C1 + C2)$



CLKREQ#	SRC BUS	From
PECLKREQ0#	PCIE4	CLK_PCIE_VGA
PECLKREQ1#	PCIE5	CLK_PCIE_MINI1

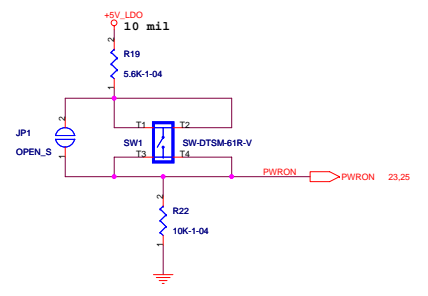
	R636
24 MHz output	10K Ohm
48 MHz output (Default)	Floating



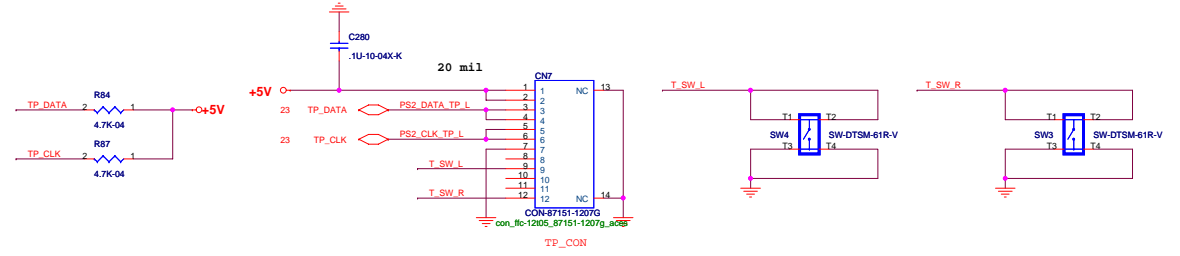
	BSEL4	BSEL3	BSEL2	BSEL1	BSEL0	CPU MHz	ZCLK
FSB533	0	0	0	0	1	133	133
FSB667	0	0	0	1	1	166	133
FSB800	0	0	0	1	0	200	133



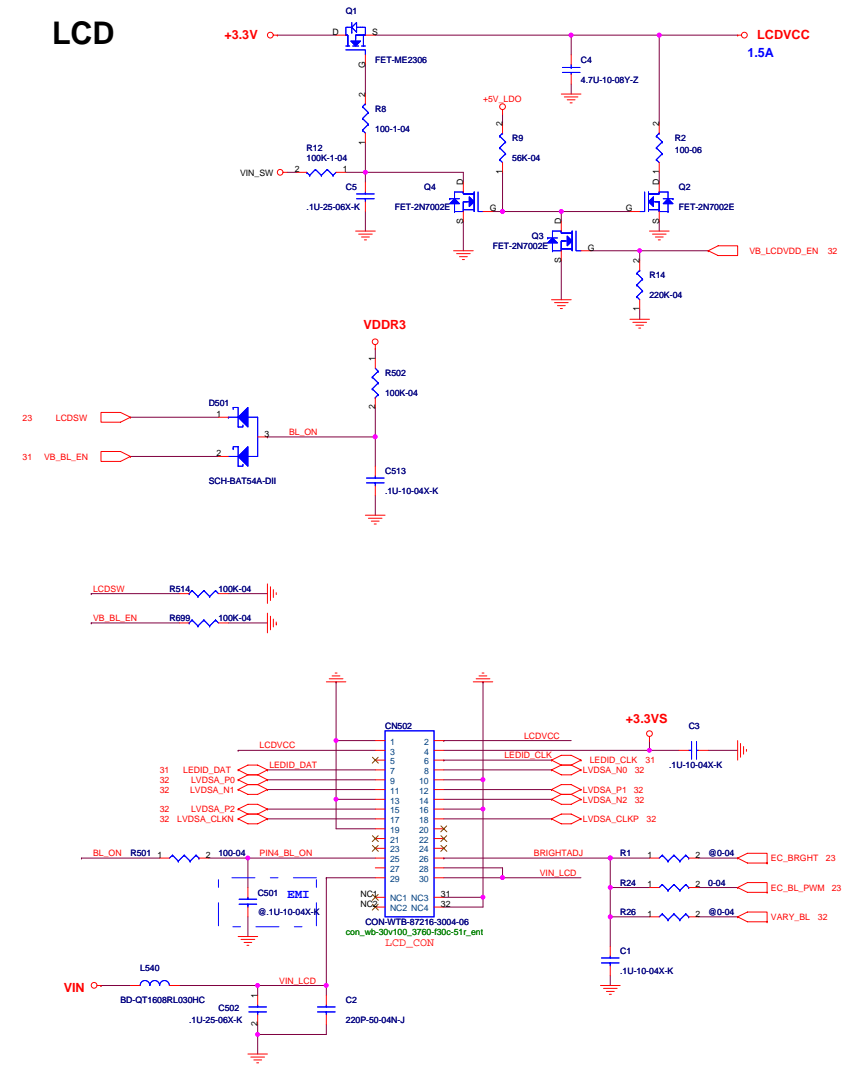
# PWR SW



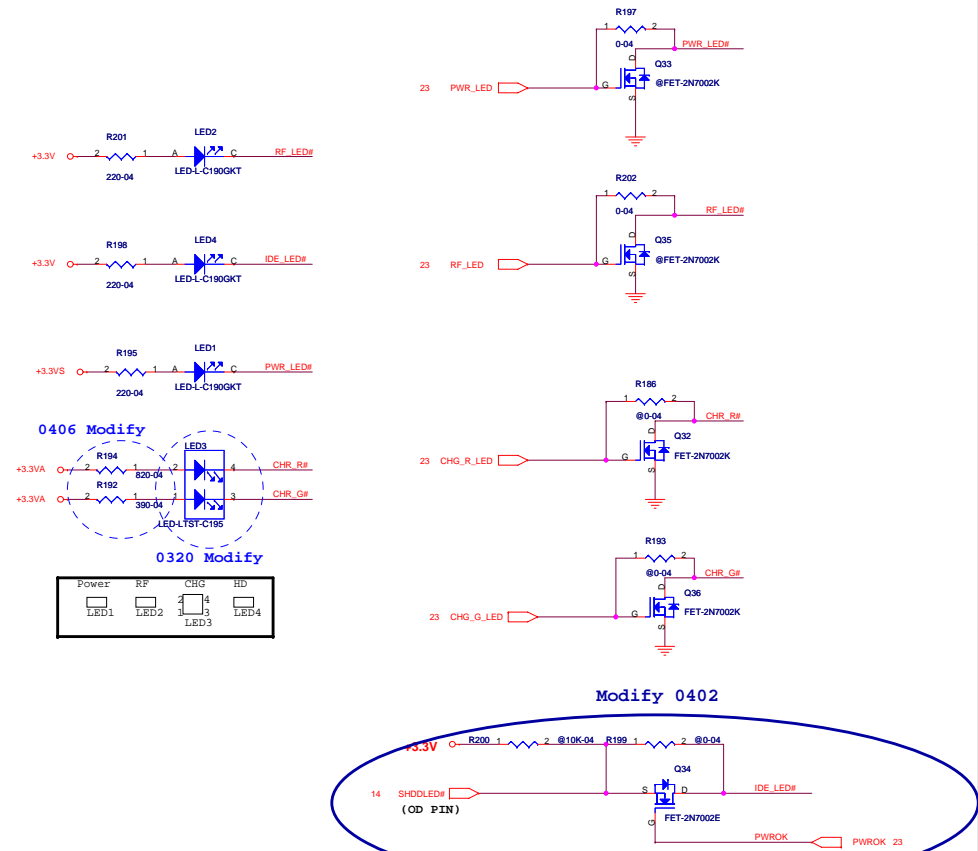
# Touch Pad



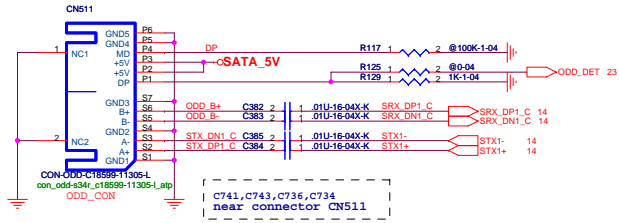
# LCD



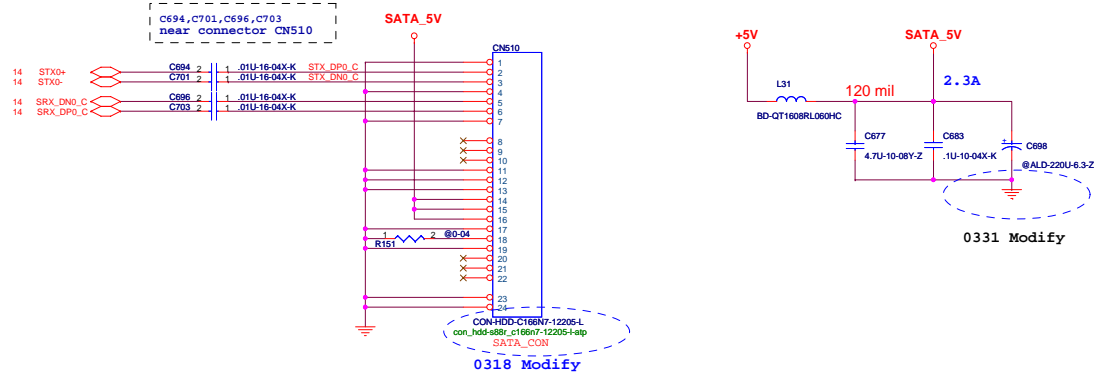
# LED



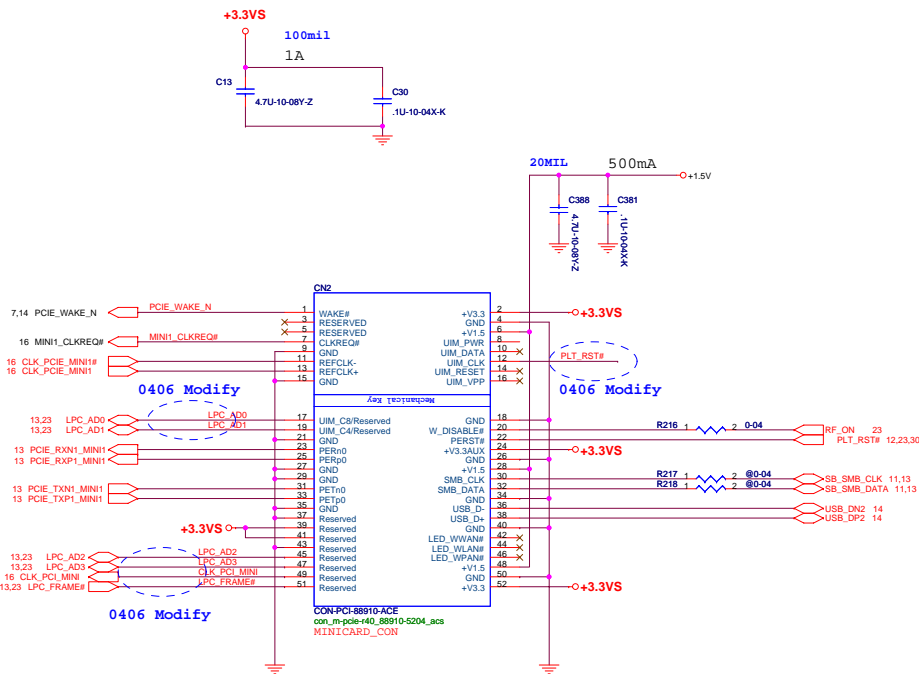
# CR-ROM



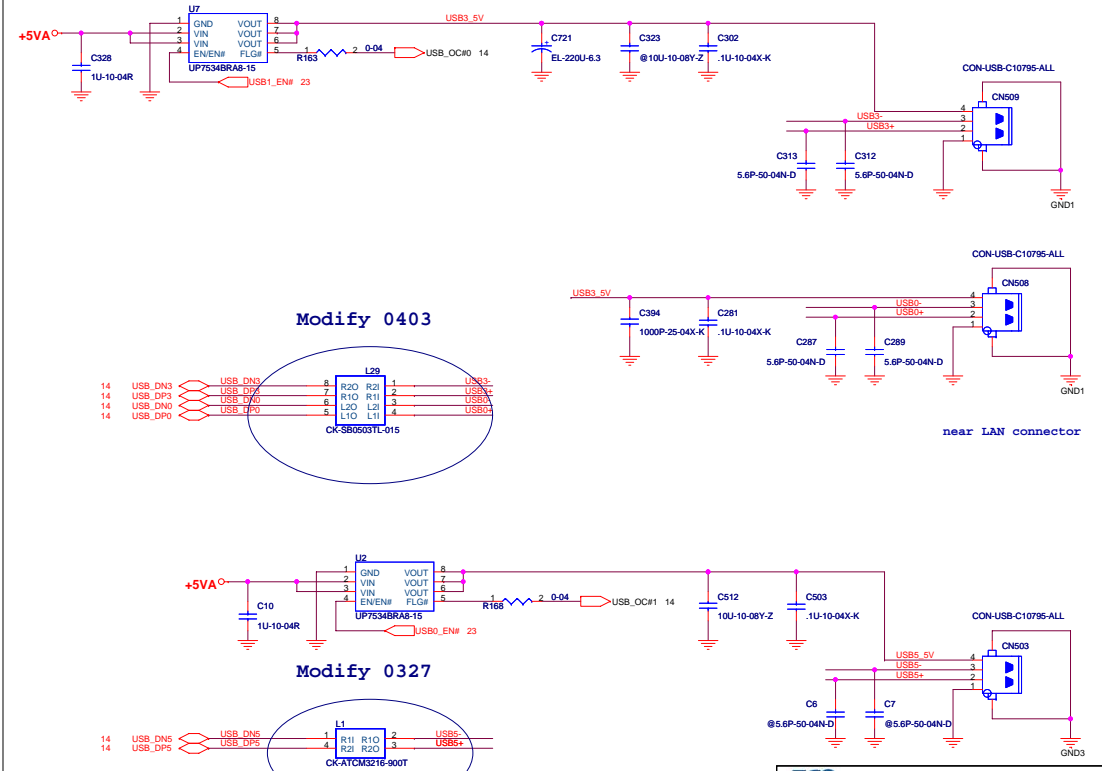
# SATA-HDD



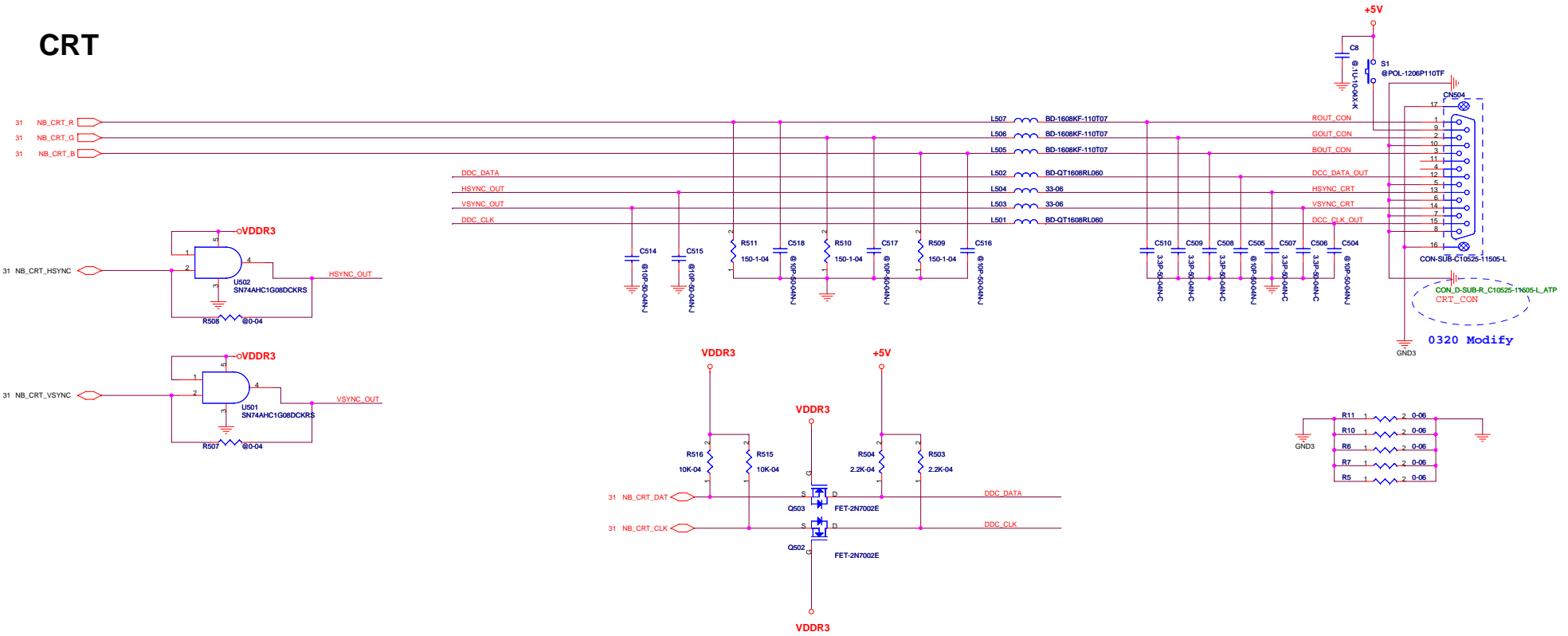
# MINI CARD CONN



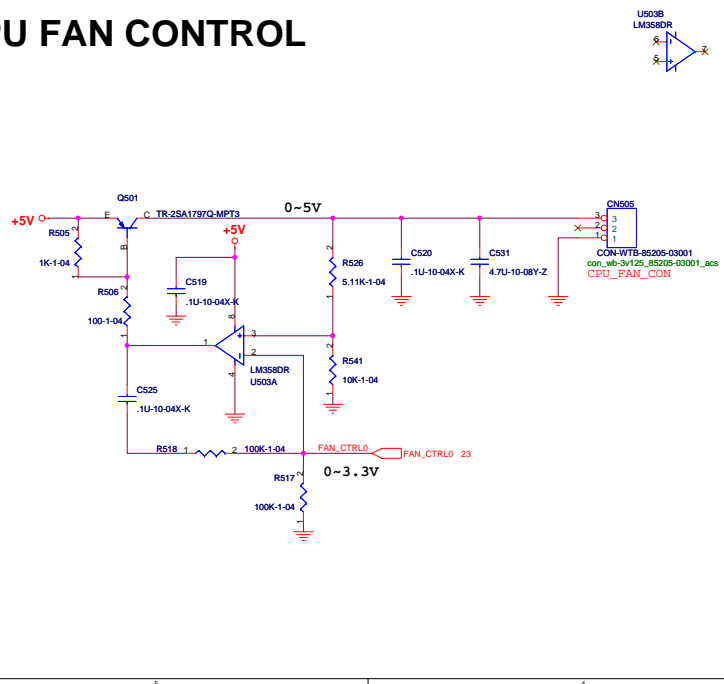
# USB Port (Colay Fuse & Bead)



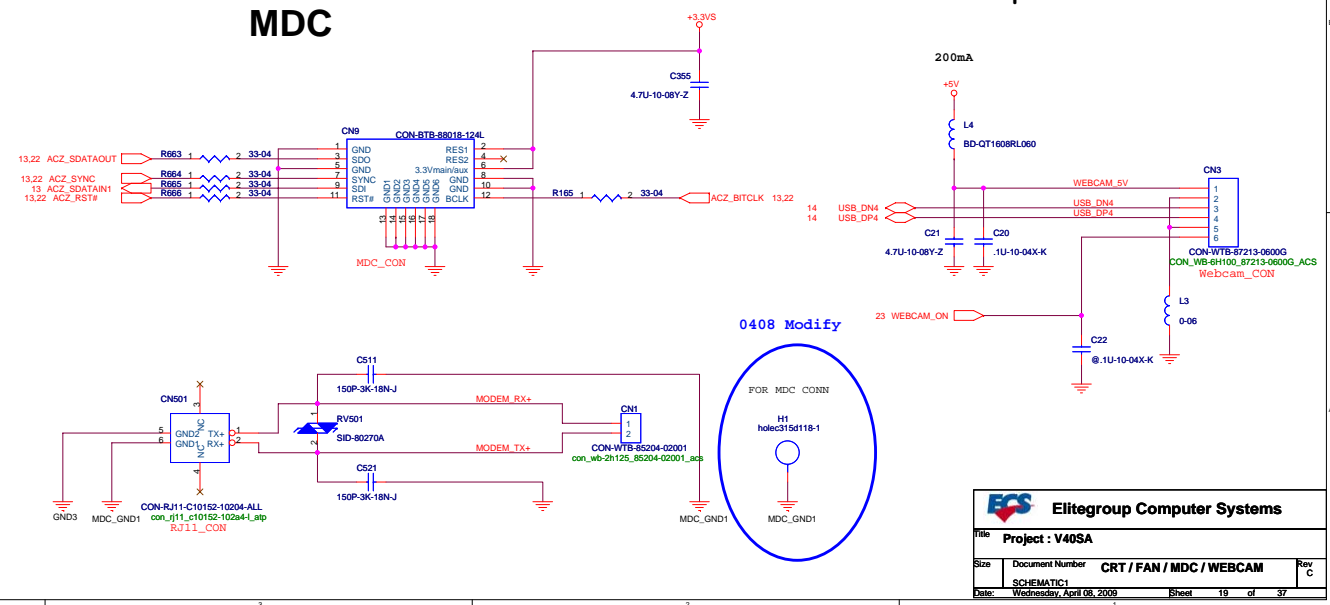
# CRT



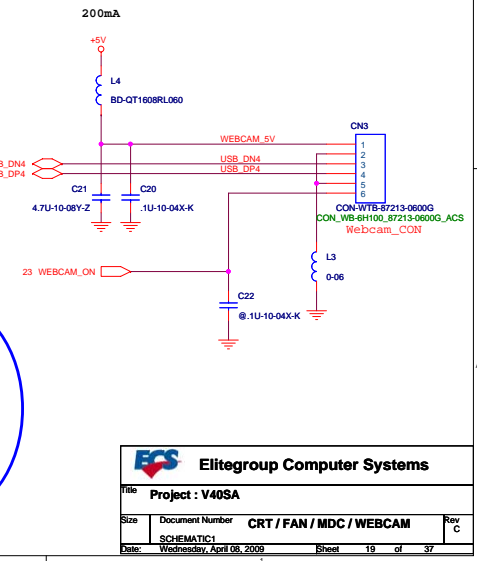
# CPU FAN CONTROL

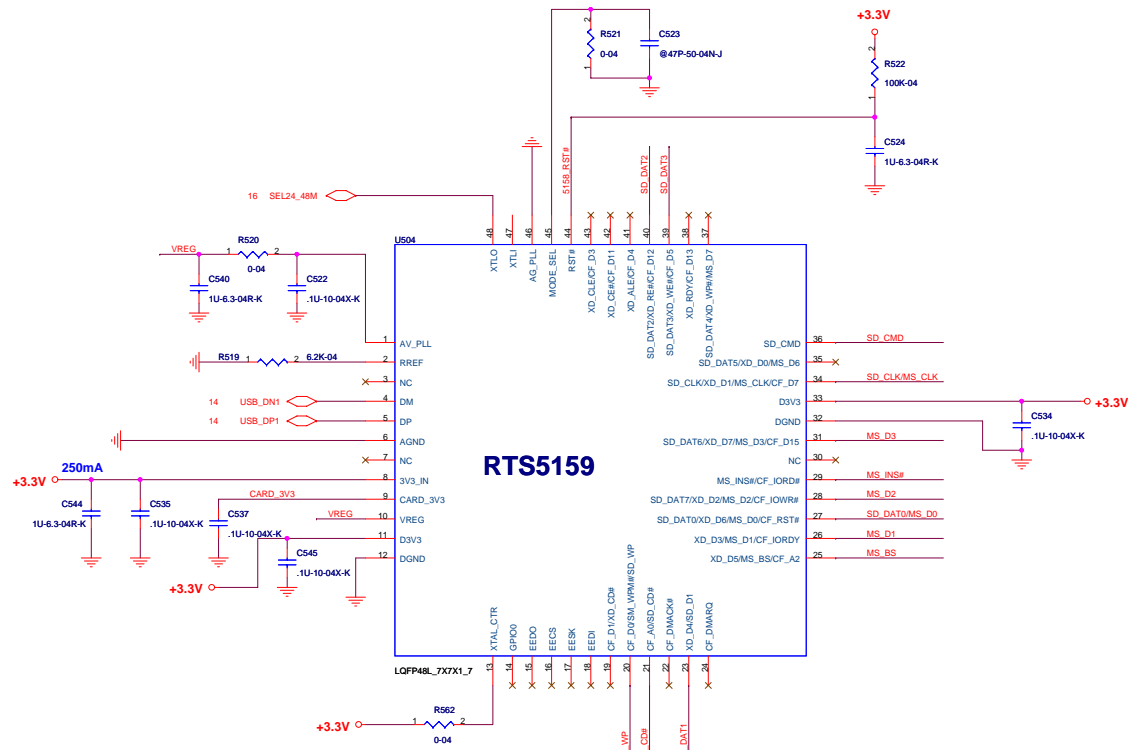


# MDC

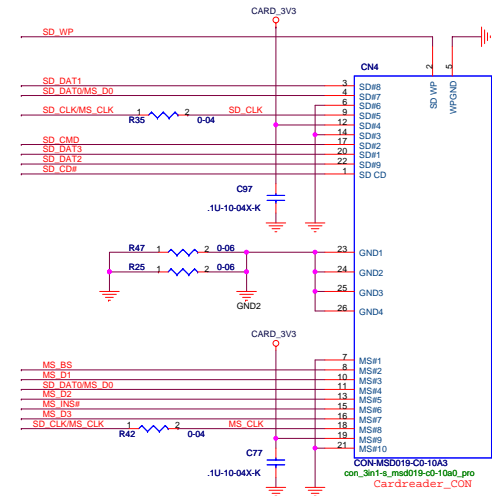


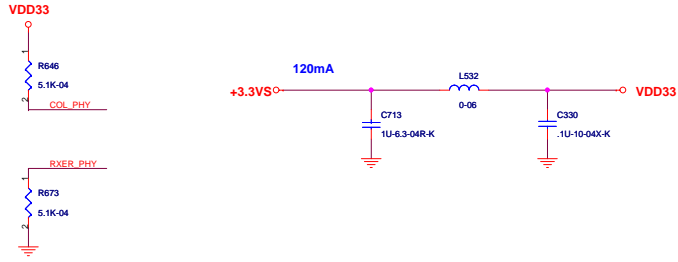
# Option WEBCAM



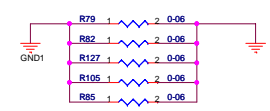
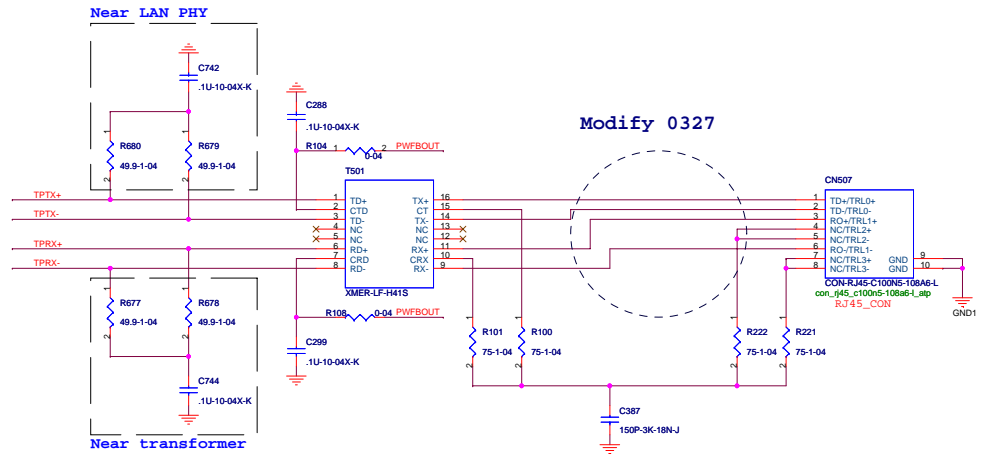
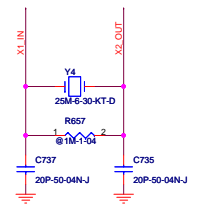
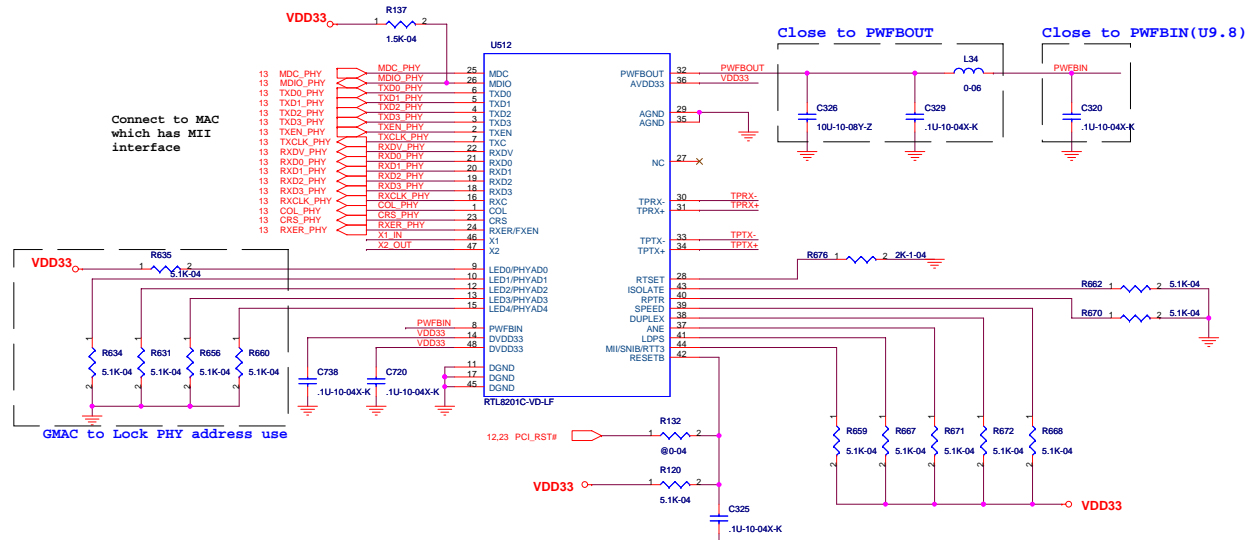


	R562
CLK GEN 48MHz input	0 Ohm
12MHz Crystal input	Floating

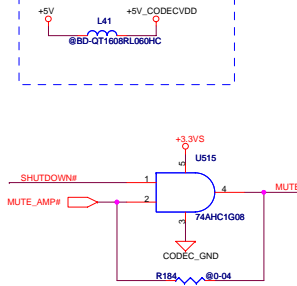
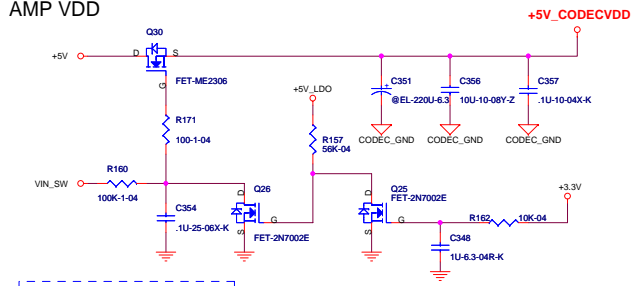




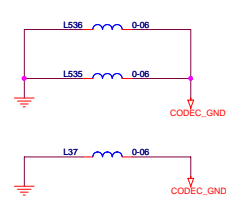
Connect to MAC  
which has MII  
interface



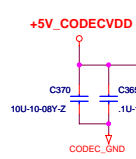
# AMP VDD



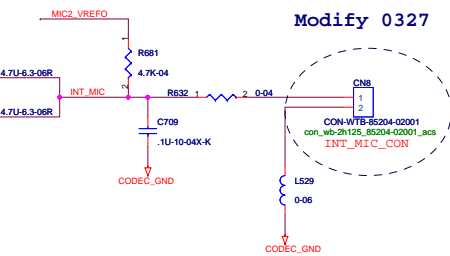
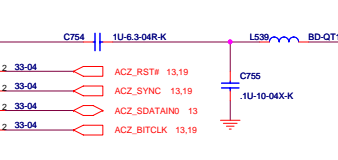
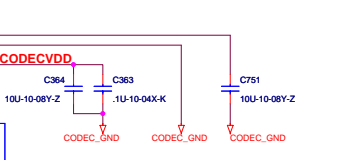
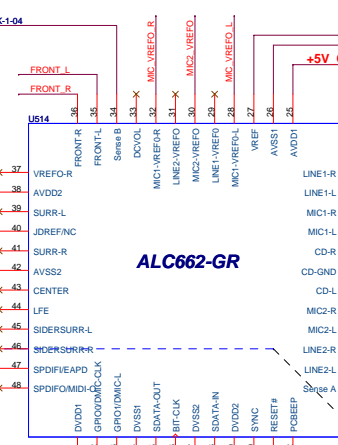
LOCATE UNDER CODEC.  
USE 80 MILLS WIDE TRACE  
BRIDGING AGND AND DGND PLANES



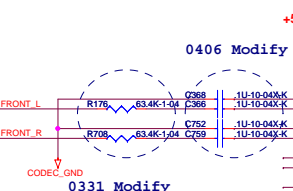
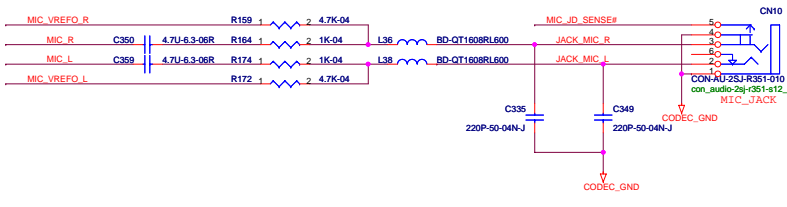
# HP JD SENSE#



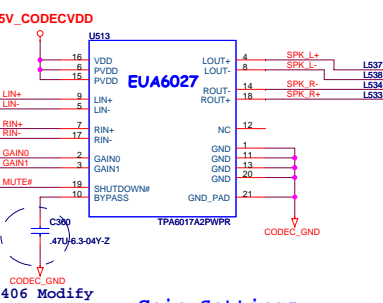
# Analog Digital



# MIC/Line In JACK



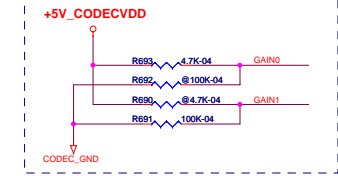
0331 Modify



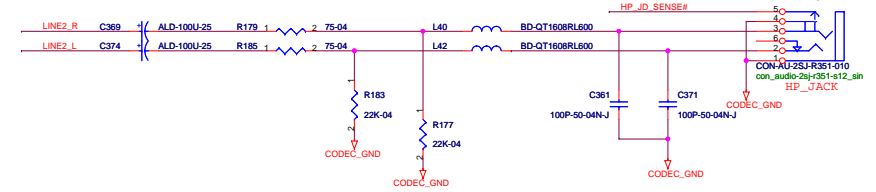
0406 Modify

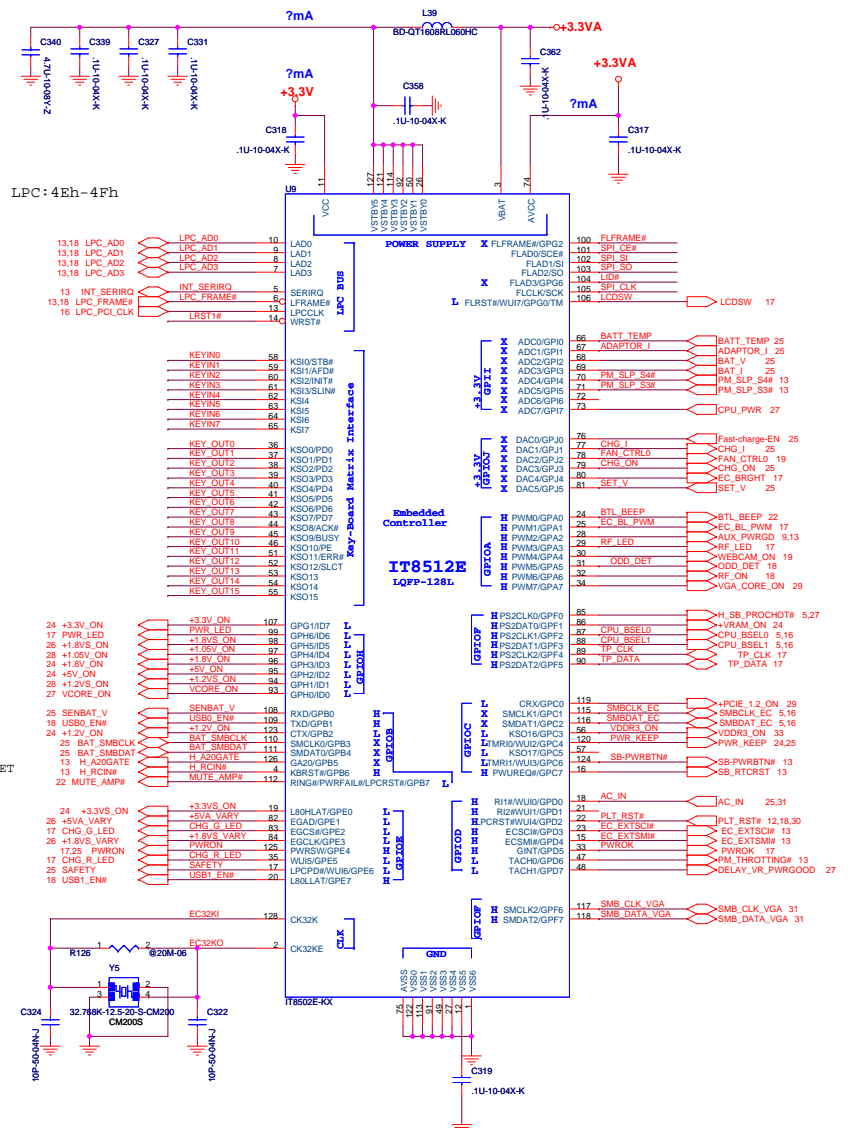
# Gain Settings

GAIN0	GAIN1	AV
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

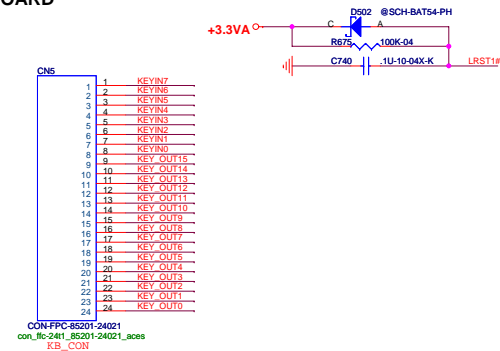


# HeadPhone JACK

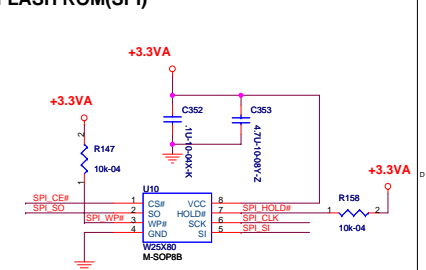




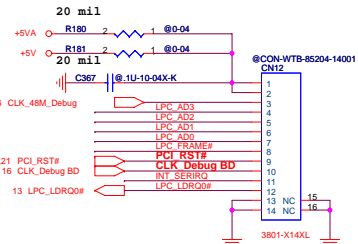
### KEYBOARD



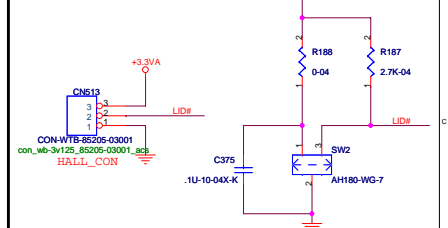
### FLASH ROM(SPI)



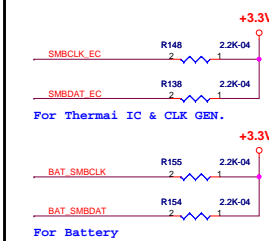
### DEBUG PORT



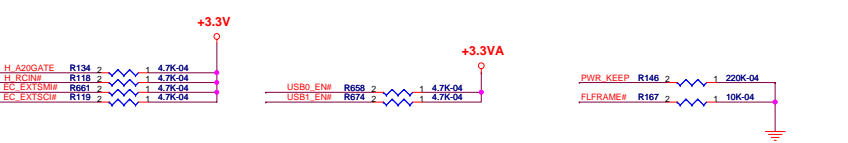
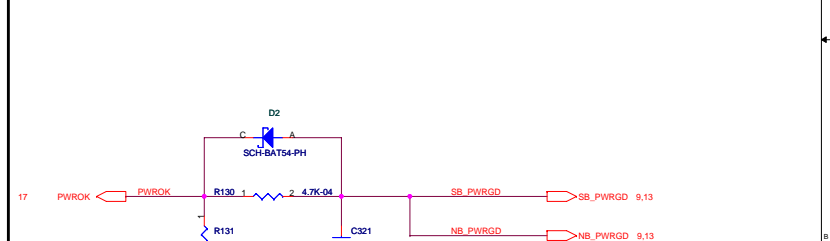
### HALL SENSOR

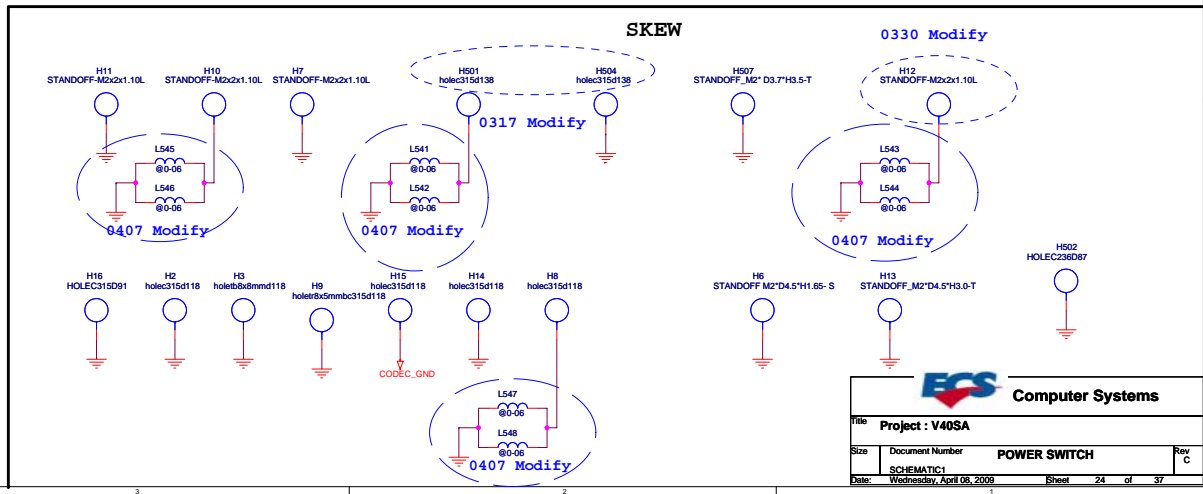
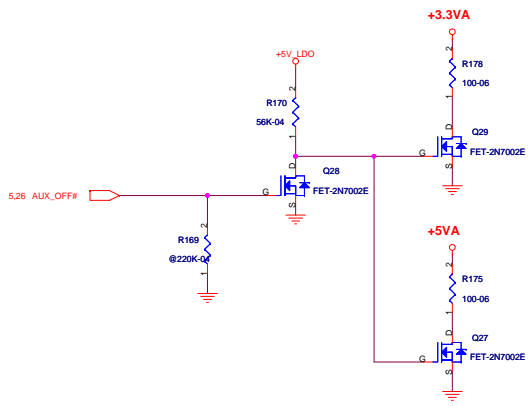
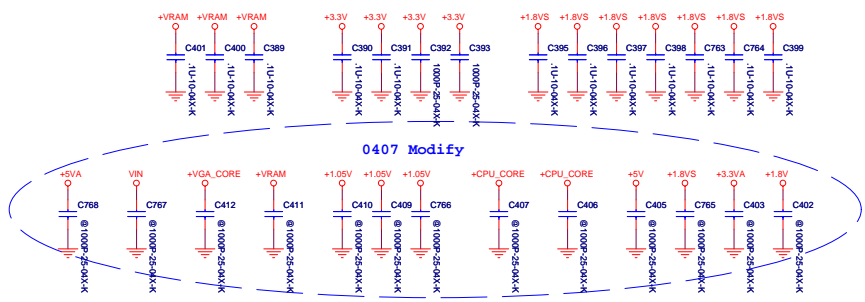
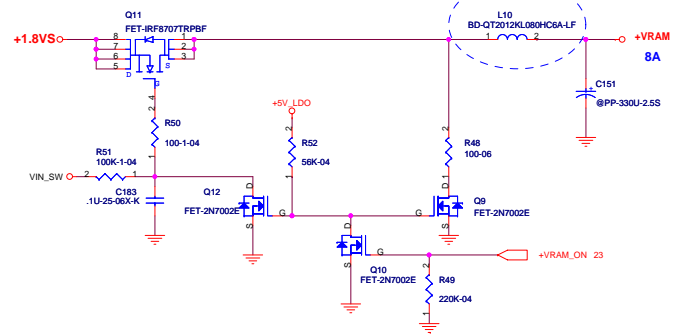
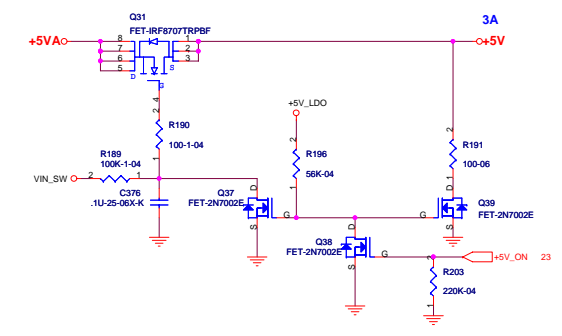
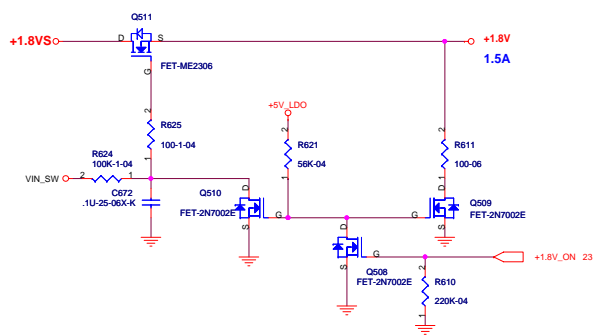
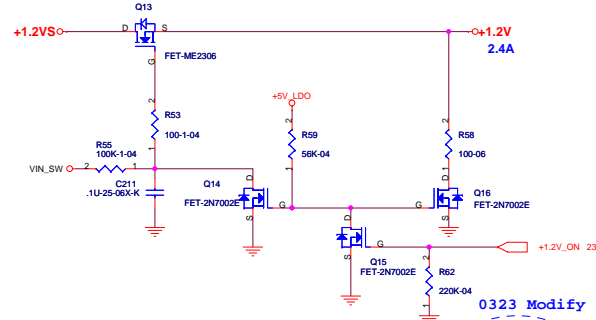
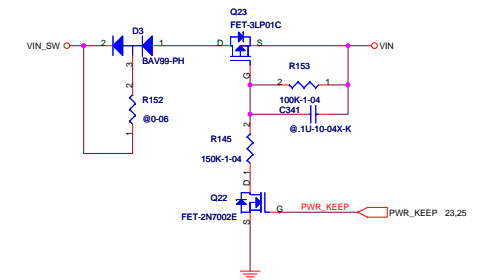
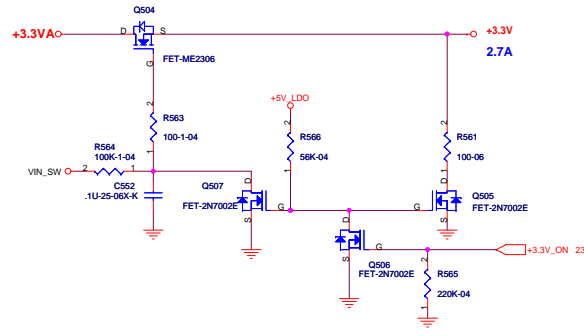
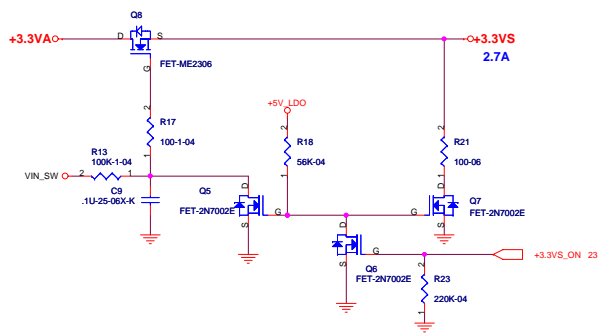


### EC SMBUS



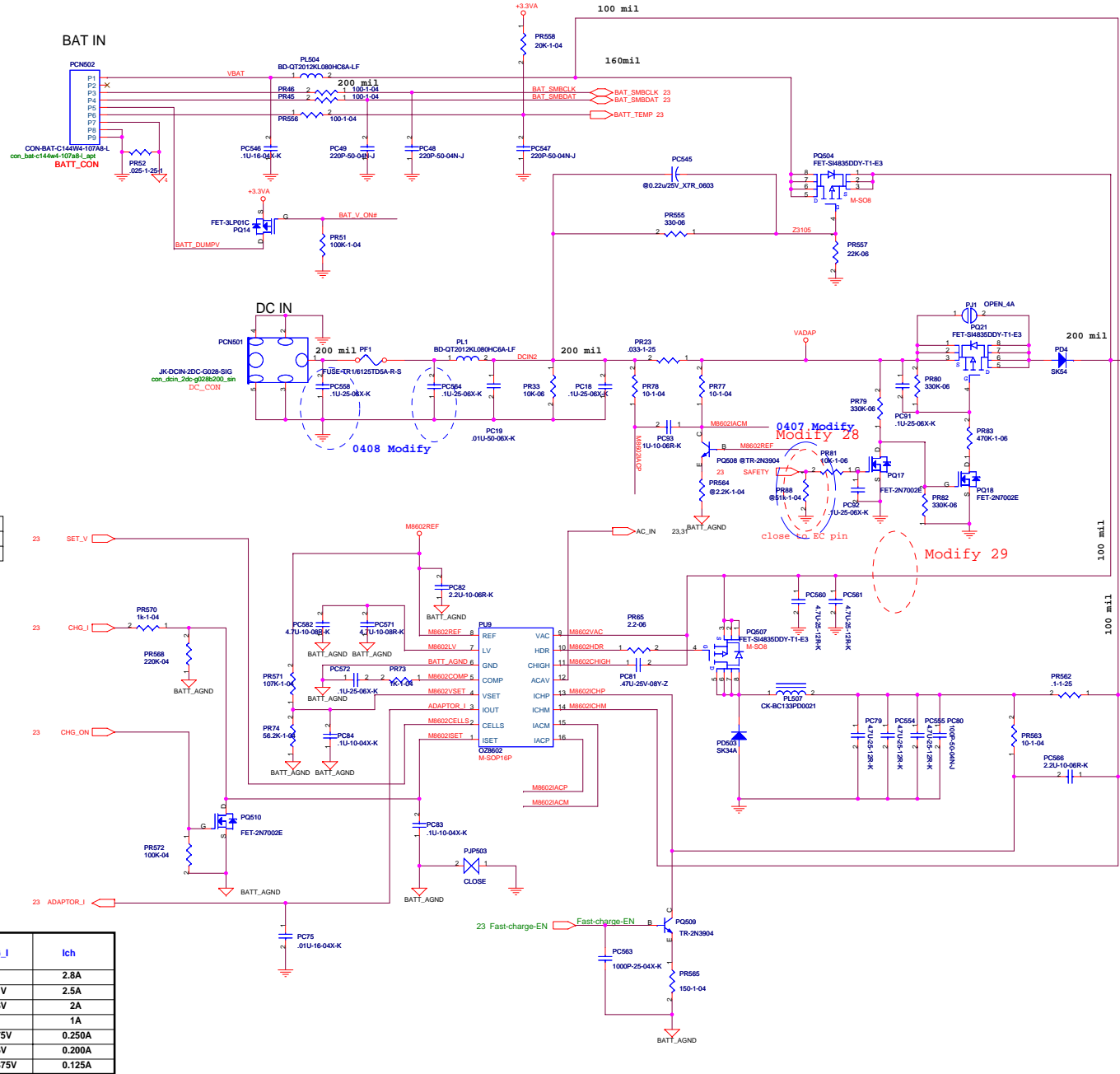
### NB / SB Power OK





<b>Computer Systems</b>	
Title: <b>Project : V40SA</b>	
Size: <b>SCHEMATIC1</b>	Document Number: <b>POWER SWITCH</b>
Date: <b>Wednesday, April 05, 2006</b>	Sheet: <b>24</b> of <b>37</b>



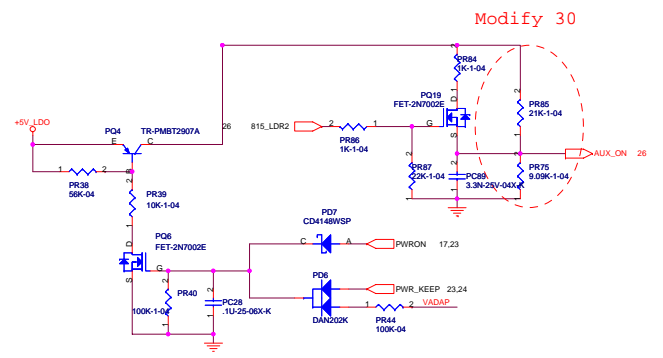


CHG V	
H	16.8V (4CELL)
L	12.6V (3CELL)

CHG ON	
L	CHARGER ON
H	CHARGER OFF

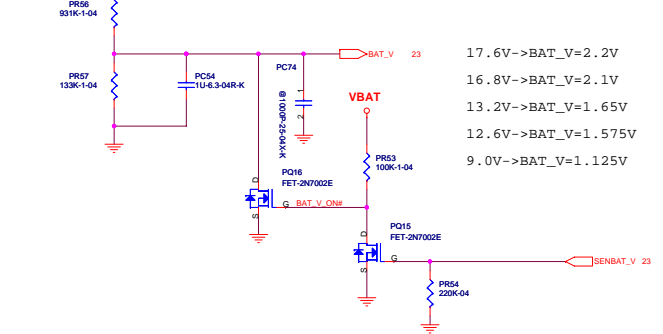
ADAPTOR I	
1A	0.33V
1.5A	0.495V
2A	0.66V
2.5A	0.825V
3A	0.99V
3.5A	1.155V

Fast-charge-EN	CHG_I	Ich
H	3V	2.8A
H	2.1V	2.5A
H	0.6V	2A
L	3V	1A
L	0.75V	0.250A
L	0.6V	0.200A
L	0.375V	0.125A



	BAT_AUX_ON	BAT_AUX_OFF
PQ22 2N7002	Remove	Add
PQ24 2N2907	Remove	Add

### Battery Voltage Detect

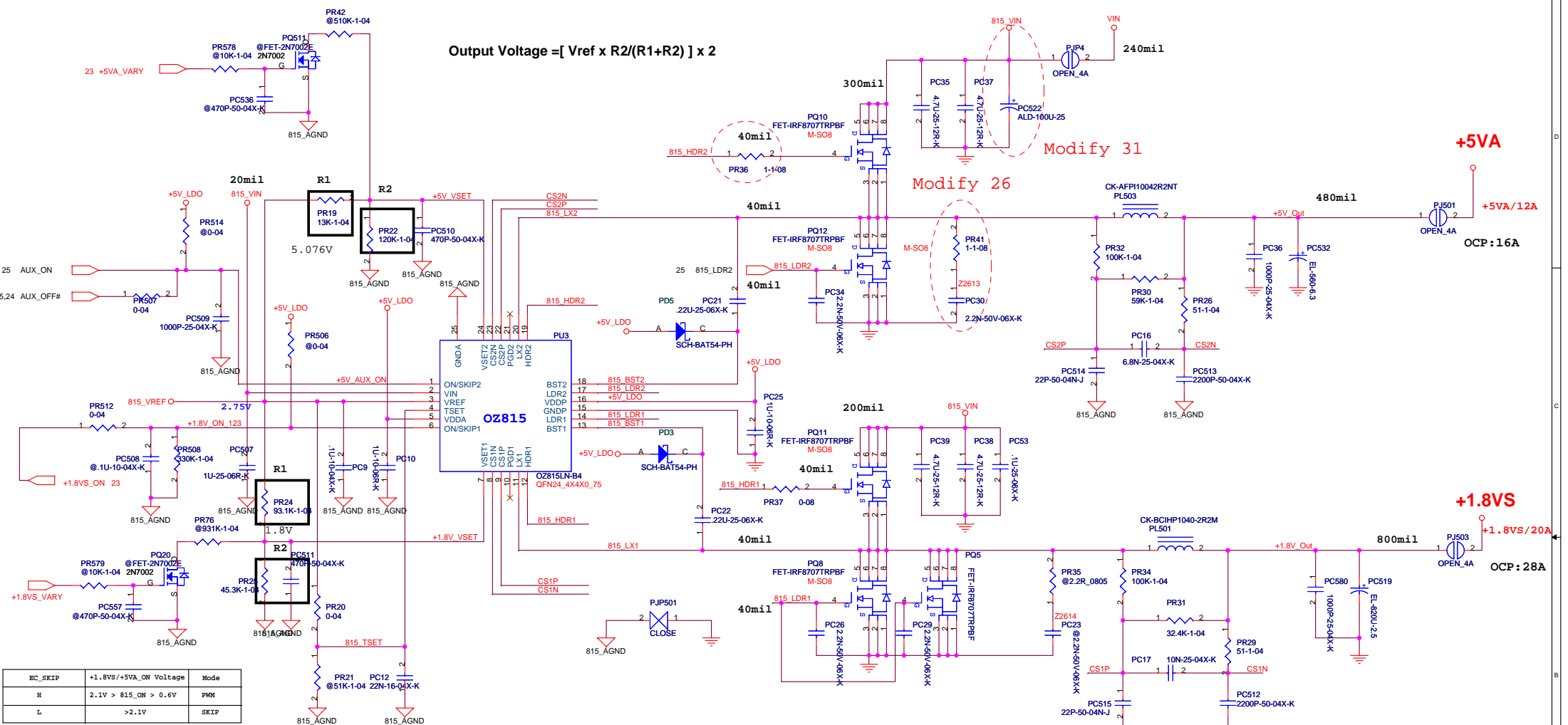


### Charge / Discharge Detect

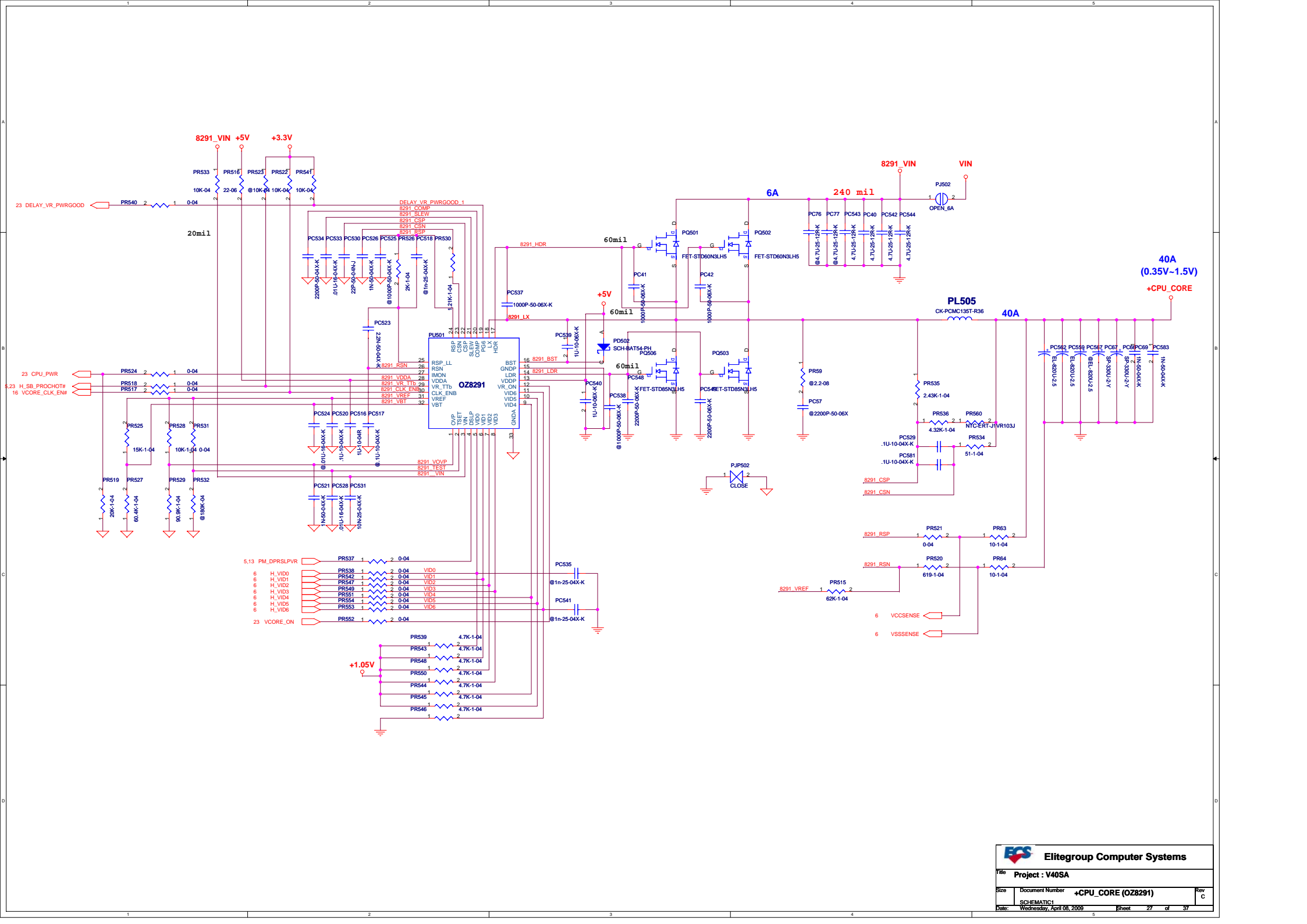
- 17.6V->BAT\_V=2.2V
- 16.8V->BAT\_V=2.1V
- 13.2V->BAT\_V=1.65V
- 12.6V->BAT\_V=1.575V
- 9.0V->BAT\_V=1.125V

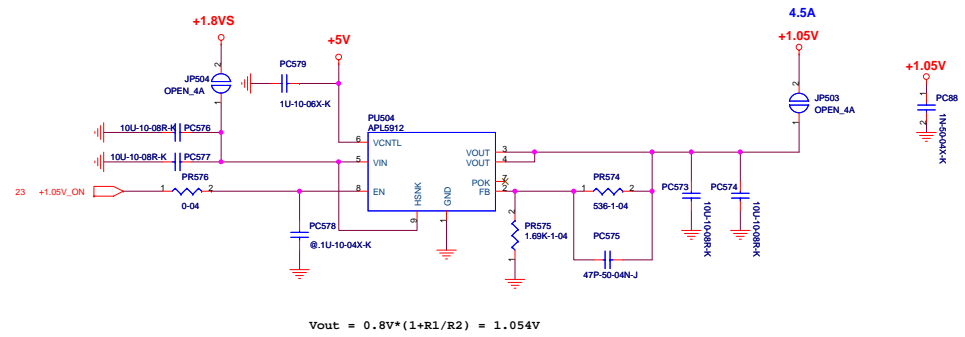
- +3A-->2.56V
- +2A-->2.276V
- +1A-->1.991V
- +0.25A-->1.778V
- 0A-->1.707V
- 3A-->0.853V
- 6A-->0V

Output Voltage = [ Vref x R2/(R1+R2) ] x 2

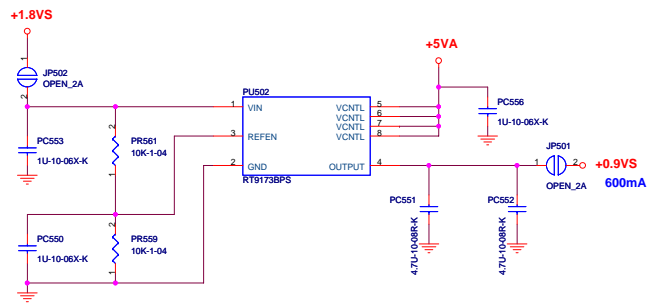


BC_SKIP	+1.8Vs/+5VA_ON Voltage	Mode
H	2.1V > 815_ON > 0.6V	PWM
L	>2.1V	SKIP

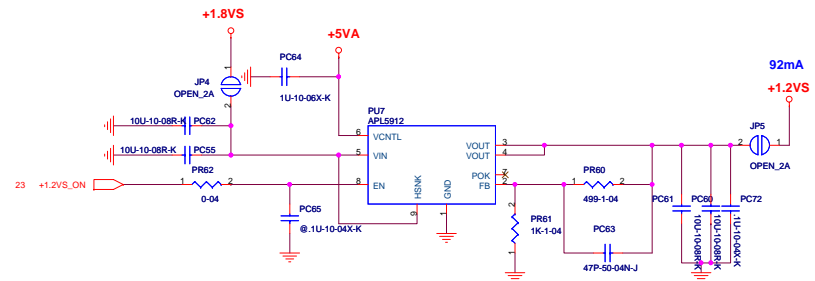




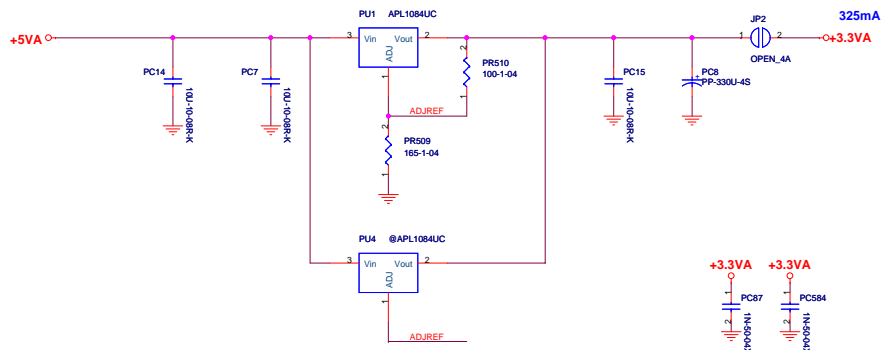
$$V_{out} = 0.8V * (1 + R1/R2) = 1.054V$$



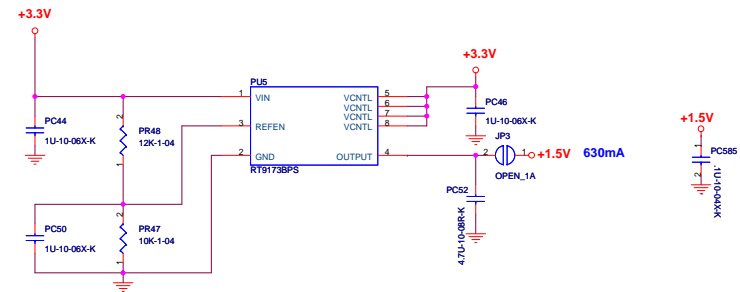
$$V_{out} = 1.8V - (1.8V * R1/R1 + R2) = 0.9V$$



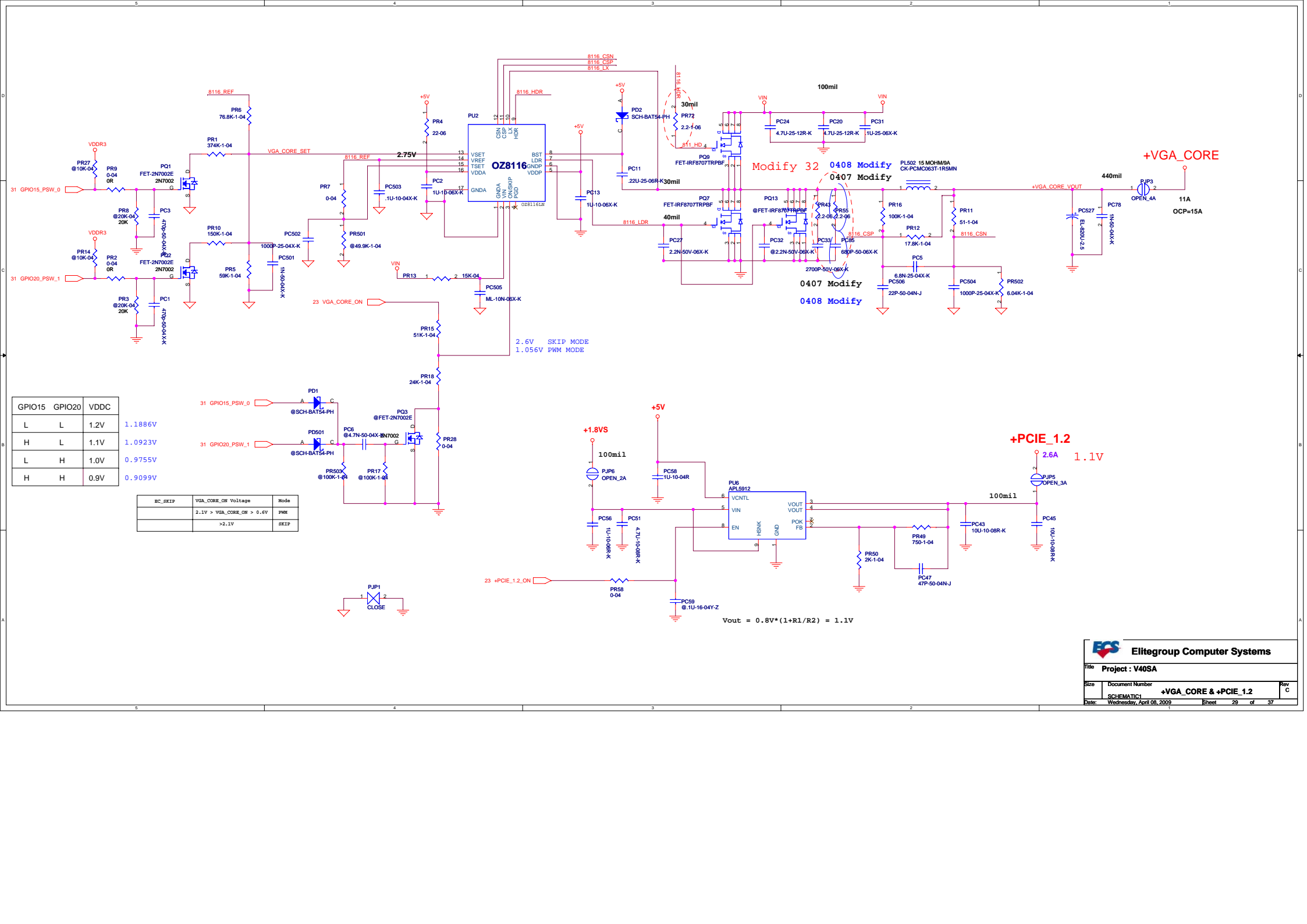
$$V_{out} = 0.8V * (1 + R1/R2) = 1.2V$$



$$V_{out} = R1 + R2 / R1 * 1.25V = 3.3125V$$



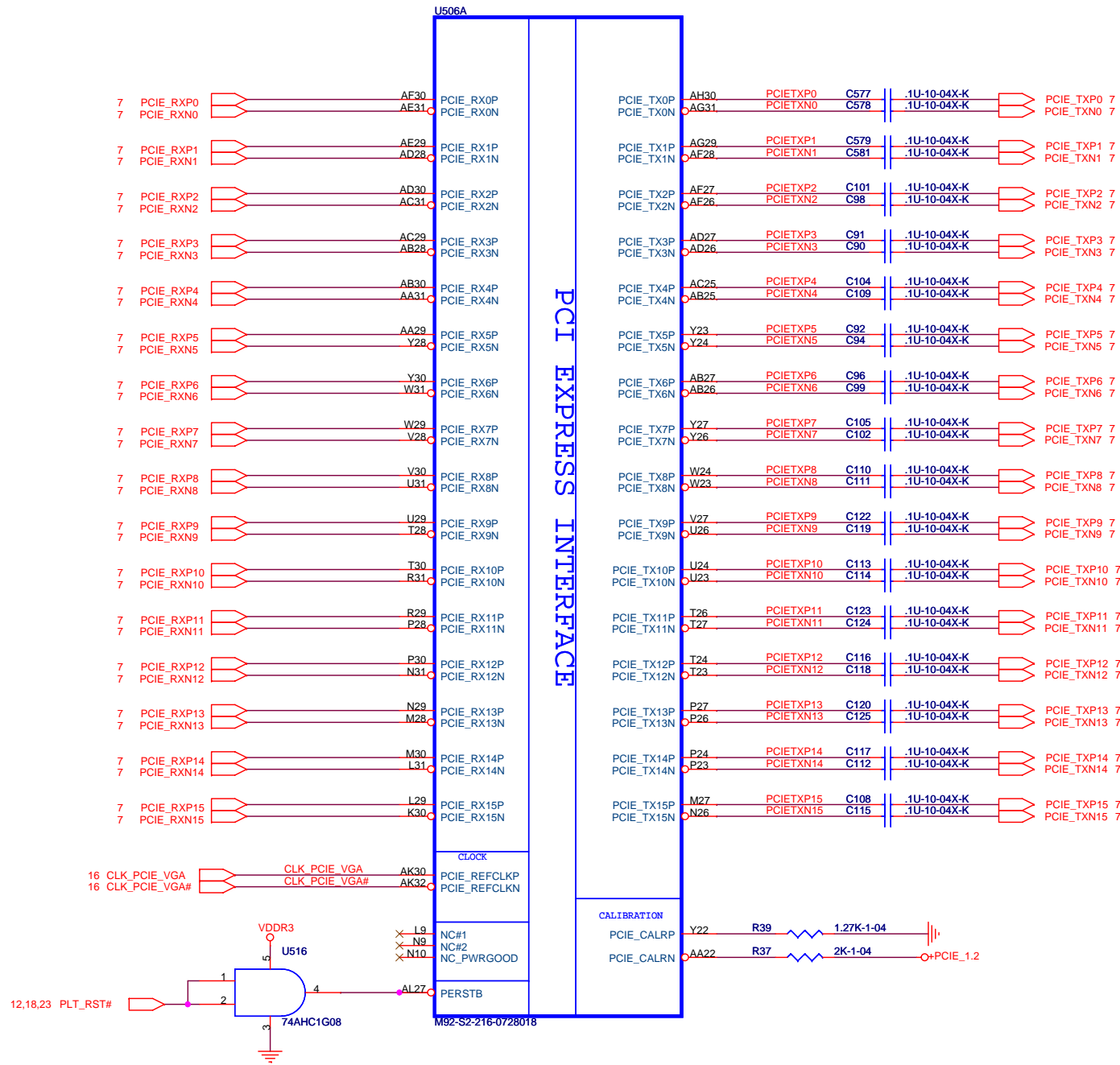
$$V_{out} = 3.3V - (3.3V * R1/R1 + R2) = 1.5V$$



GPIO15	GPIO20	VDDC
L	L	1.2V
L	L	1.1886V
H	L	1.1V
L	H	1.0V
L	H	0.9755V
H	H	0.9V
H	H	0.9099V

EC_SKIP	VDA_CORE_ON Voltage	Mode
	2.1V > VDA_CORE_ON > 0.6V	PMR
	>2.1V	SKIP

$$V_{out} = 0.8V * (1 + R1/R2) = 1.1V$$



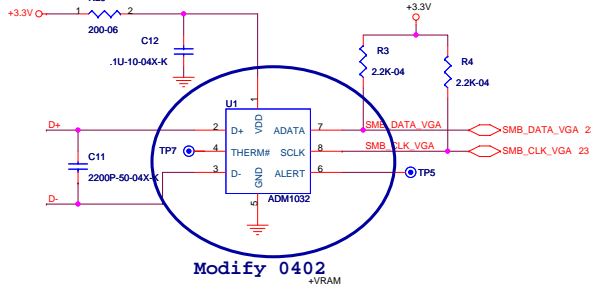
**ECS Elitegroup Computer Systems**

Title: **Project : V40SA**

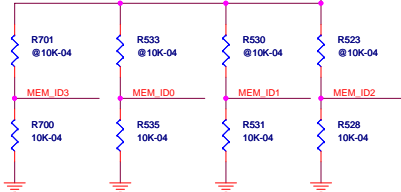
Size	Document Number	Rev
	<b>M92S_PCIE</b>	C

Date: Wednesday, April 08, 2009 Sheet 30 of 37

# VGA Thermal Sensor



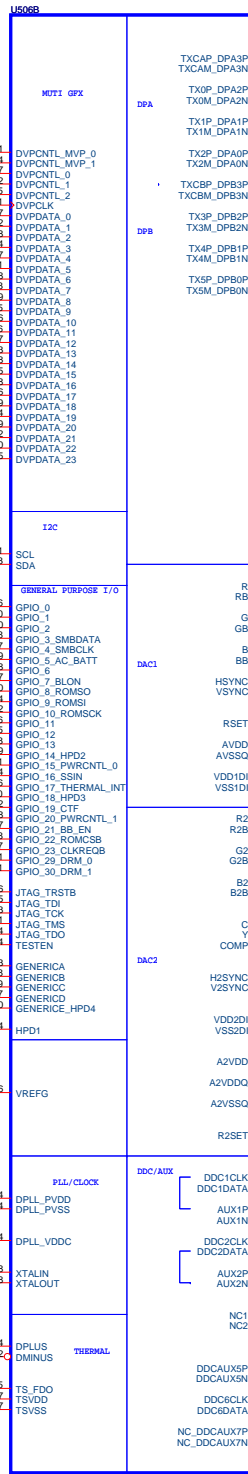
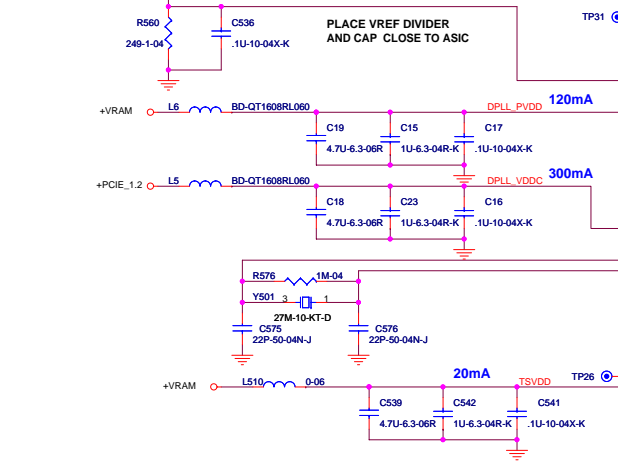
Modify 0402



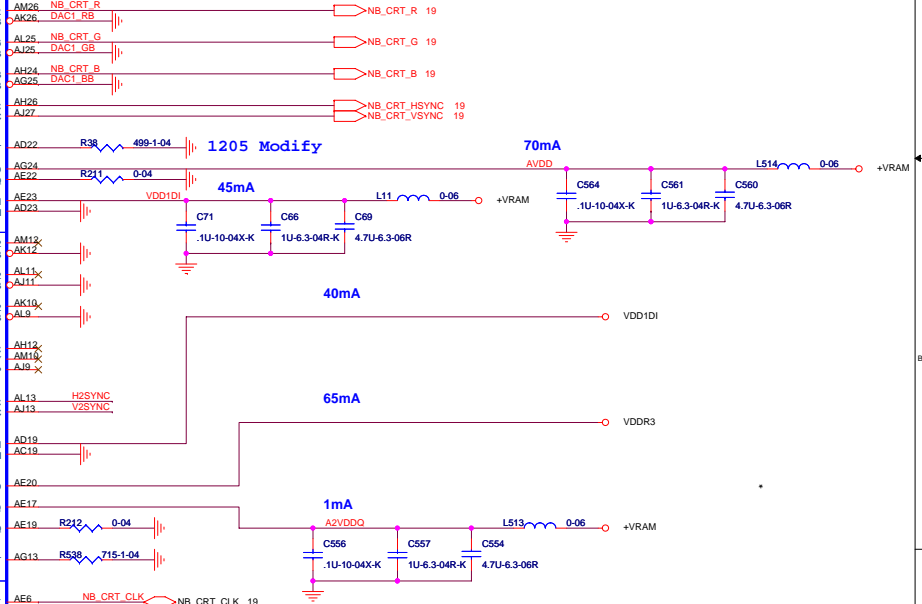
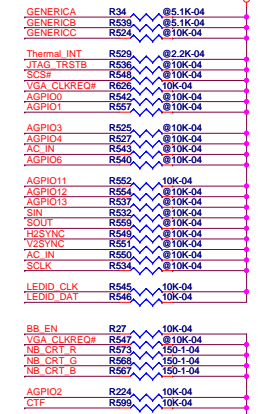
Test points for I2C Debug access

DDR2 64M*16	MEM ID[3..0]
Hynix H5PS1G63EER-20I	0 0 0 0
Sam K4N1G164QE-HC20	0 0 0 1
Sam K4N1G164QQ-HC20	0 0 1 0
Sam K4N51163QG-HC20	1 0 0 1
Sam K4N51163QZ-HC20	1 0 1 0

DDR2 32M*16	MEM ID[3..0]
Hynix H5PS162FFR-20I	1 0 0 0
Sam K4N51163QG-HC20	1 0 0 1
Sam K4N51163QZ-HC20	1 0 1 0



GPIO_22	0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device
GPIO_13	BIOS_ROM_EN = 1, ROM type
GPIO_12	BIOS_ROM_EN = 0, primary memory aperture size 256M [001]
GPIO_9	0 VGA Controller capacity enabled 1 will not be recognized as the system
GPIO_2	0 = PCIe device as 2.5 GT/s 1 = PCIe device as 5.0 GT/s
GPIO_1	0: Tx de-emphasis disabled 1: Tx de-emphasis enabled
GPIO_0	0: 50% Tx output swing 1: Full Tx output swing



**Elitegroup Computer Systems**

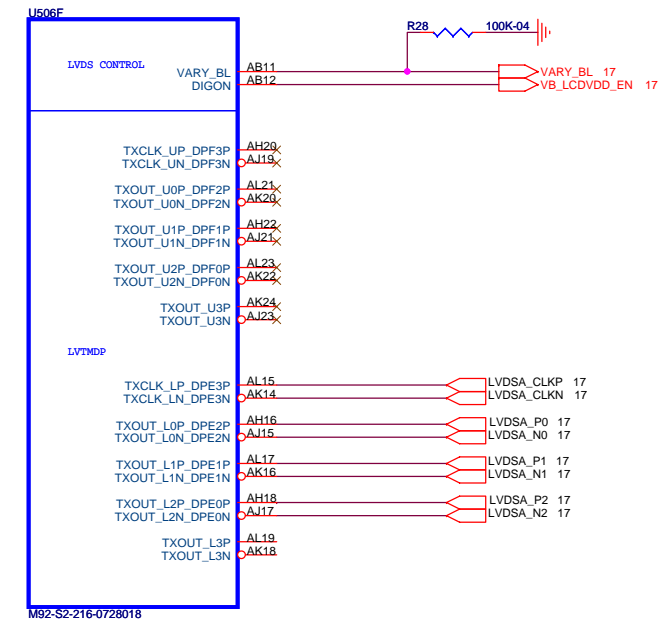
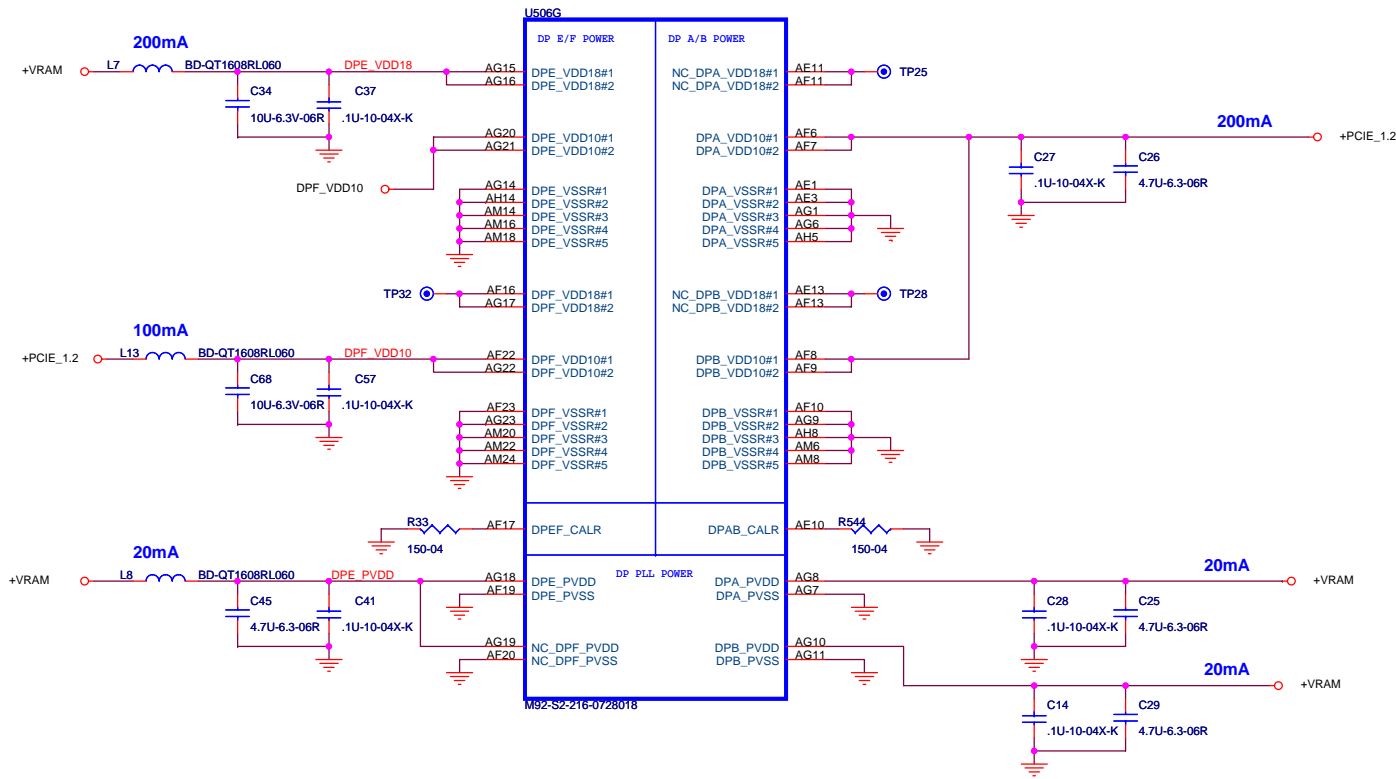
Project : V40SA

Document Number : M92S\_IQ/Thermal


SCHEMATIC

Wednesday, April 08, 2009

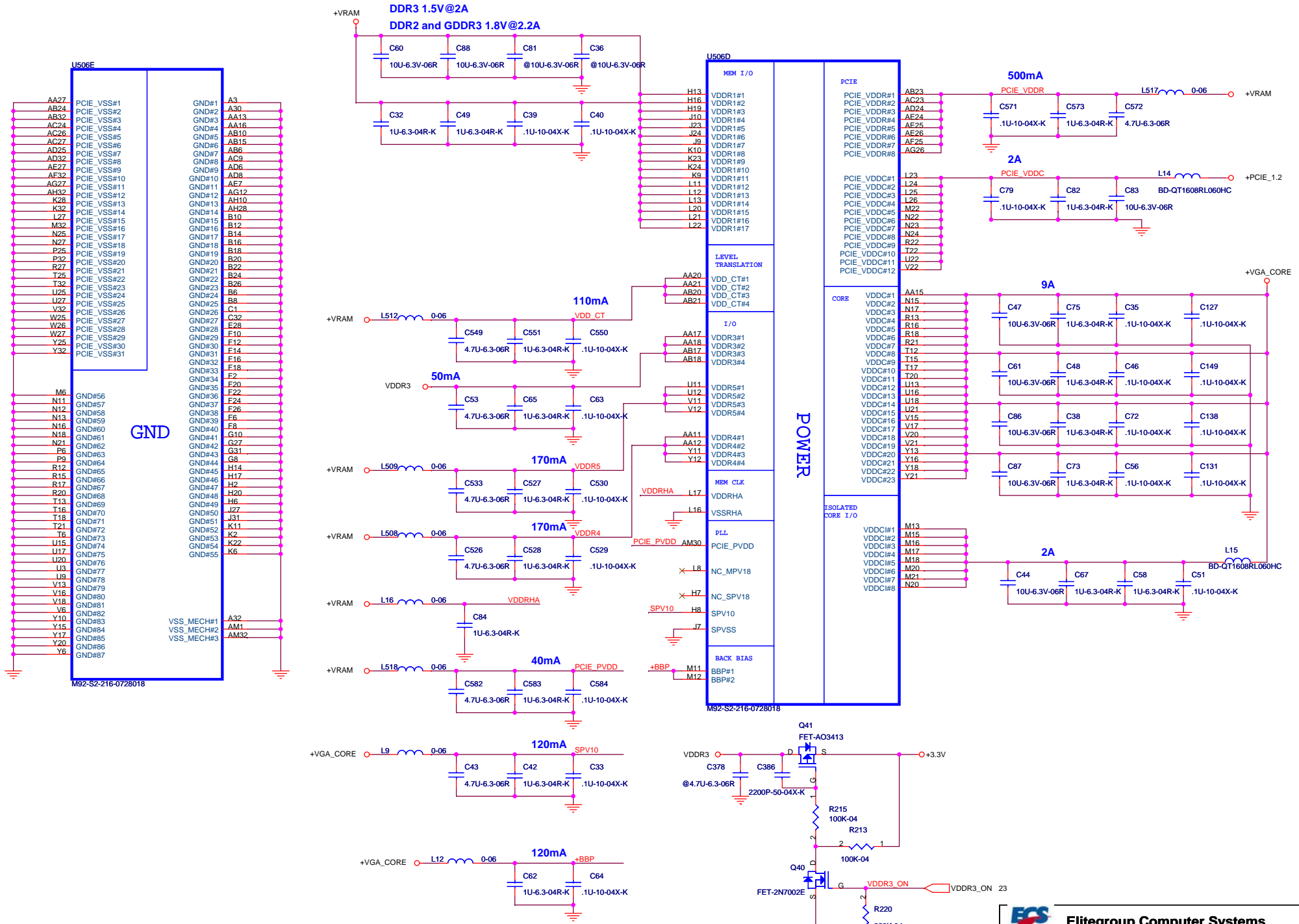
Sheet 31 of 37

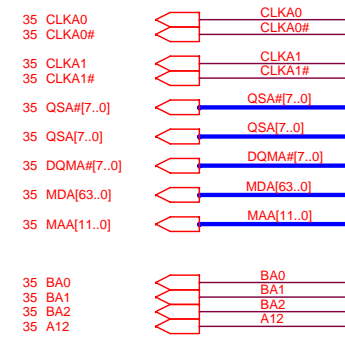
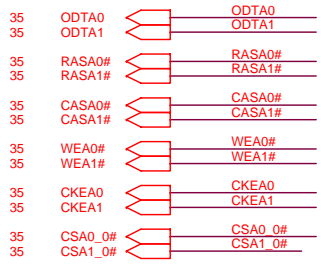


**NOTE: Single channel LVDS interfaces must use the lower LVDS channel (TXOUT\_Lxx)**

 <b>Elitegroup Computer Systems</b>	
Title <b>Project : V40SA</b>	
Size	Document Number <b>M92S_LVDS</b>
Date: Wednesday, April 08, 2009	
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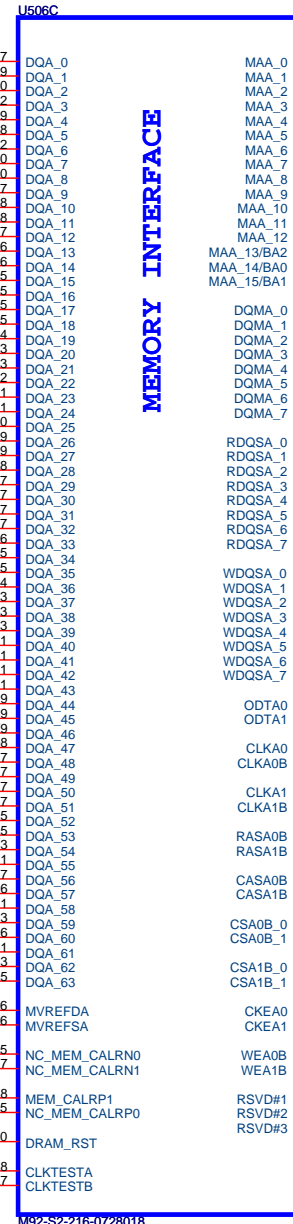
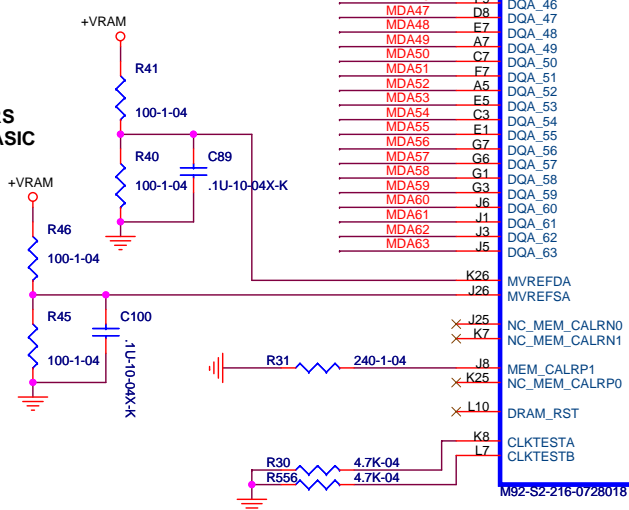






PLACE MVREF DIVIDERS  
AND CAPS CLOSE TO ASIC

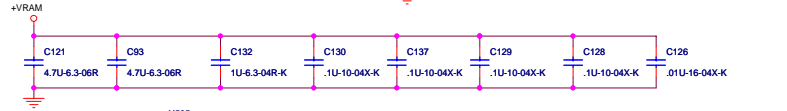
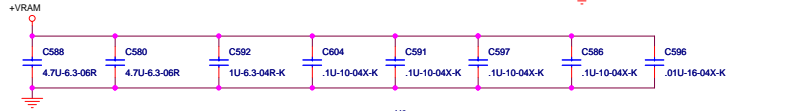
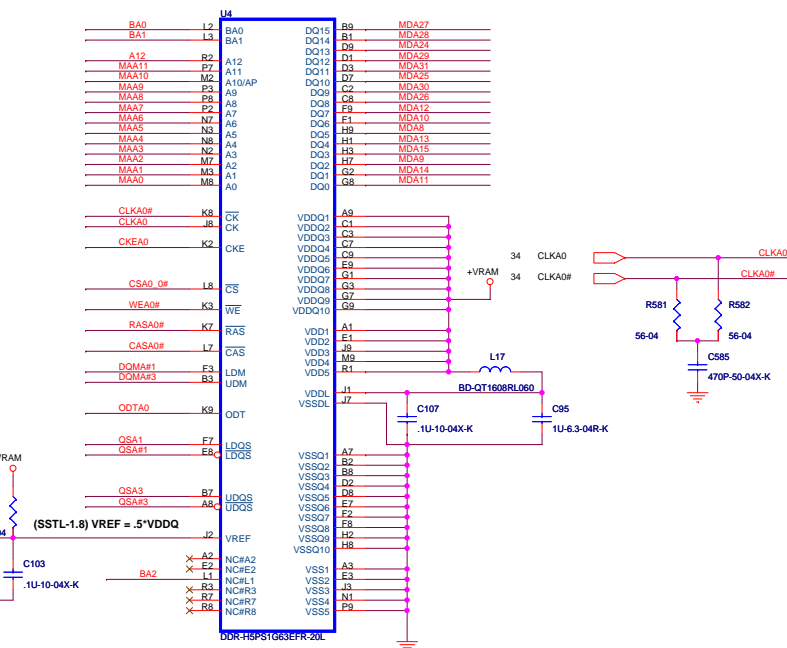
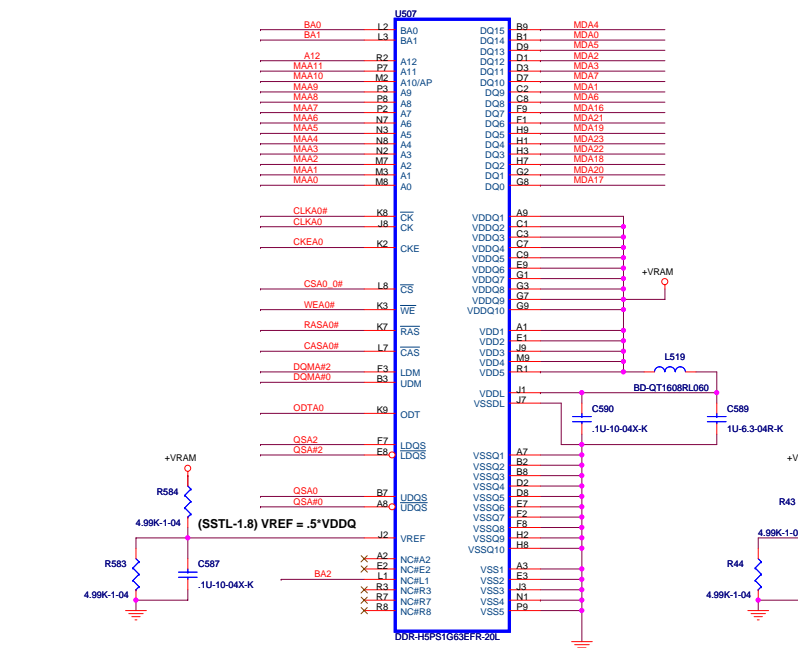
DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R



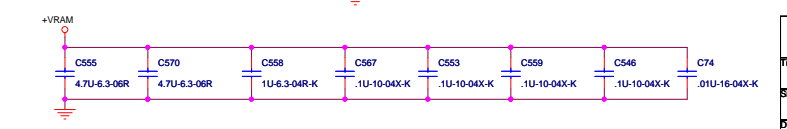
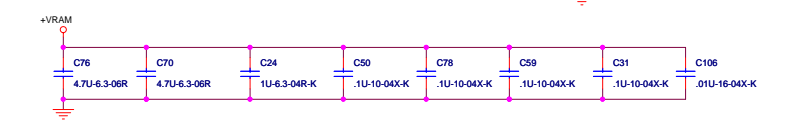
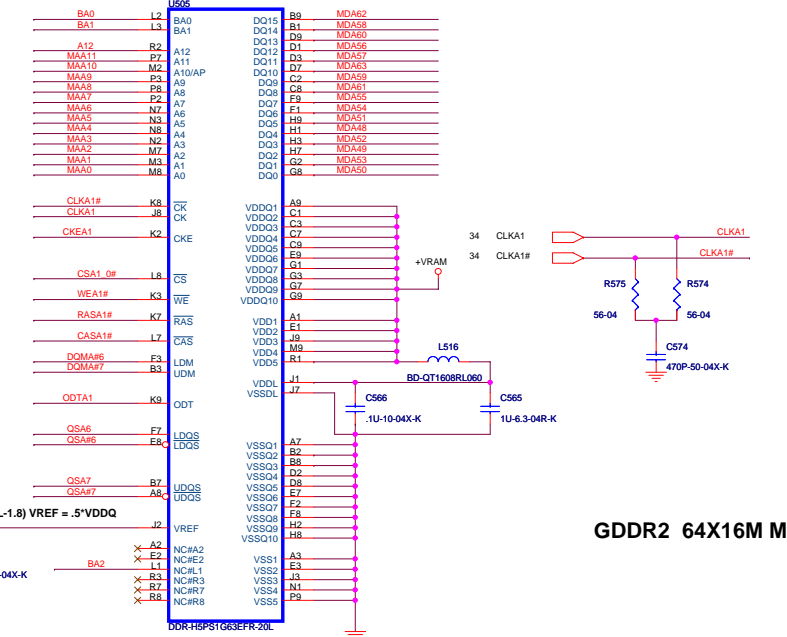
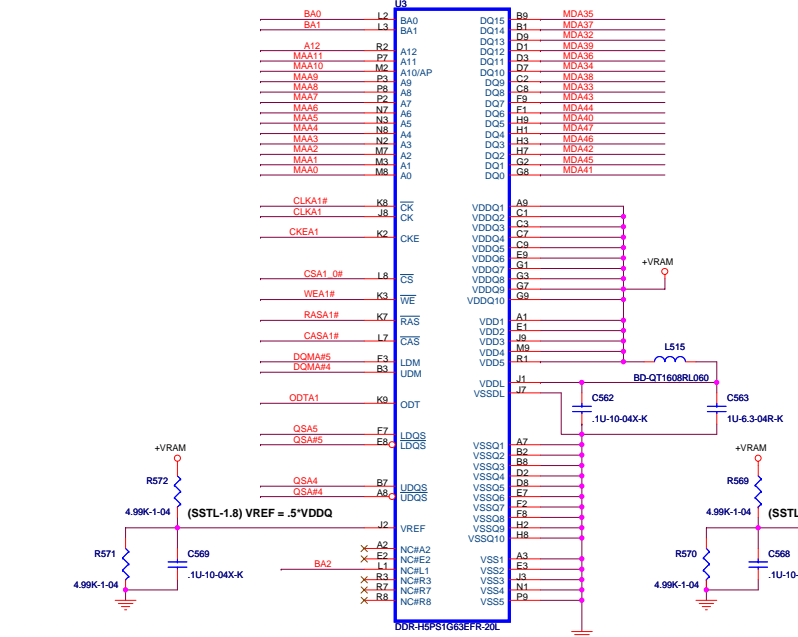
MEMORY INTERFACE

FOR DUAL RANK CONNECTIONS  
USE THE CSxB\_1 CHIP SELECT PINS

**Elitegroup Computer Systems**  
Title: Project : V40SA  
Size: Document Number: M92S\_MEMORY  
Date: Wednesday, April 08, 2009 Sheet 34 of 37



- 34 RAS0#
- 34 RAS1#
- 34 CASA0#
- 34 CASA1#
- 34 WEA0#
- 34 WEA1#
- 34 CKEA0
- 34 CKEA1
- 34 CSA0\_0#
- 34 CSA1\_0#
- 34 ODTA0
- 34 ODTA1
- 34 QSA#(7..0)
- 34 QSA7\_0
- 34 DQMA#(7..0)
- 34 DQMA#(7..0)
- 34 MDA#(3..0)
- 34 MDA#(3..0)
- 34 MAA#(11..0)
- 34 MAA11\_0
- 34 BA1
- 34 BA0
- 34 BA2
- 34 A12



**GDDR2 64X16M MEMORY**

**Elitegroup Computer Systems**

File: Project : V40SA

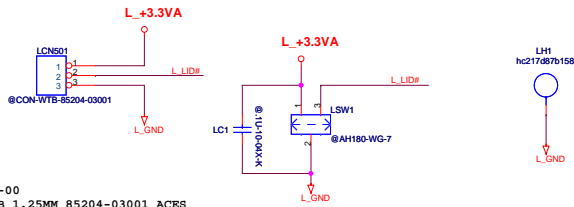
Size: Document Number

Schematic: **GDDR2 64MX16**

Date: Wednesday, April 08, 2009 Sheet 35 of 37

LID BD (Stuff LCN501,LSW1,LC1 only for V40XX series)

HALL SENSOR



**V40SAx C phase modify list:**

- MB 03/17  
1. page 24 : Modify value from H501 H504 to holec315d138  
MB 03/18  
2. page 18 : Modify footprint from CNS10 to con\_hdd-s88r\_c166n7-12205-l-atp  
MB 03/20  
3. page 19 : Modify footprint from CN504 to CON\_D-SUB-R\_C10525-11505-L\_ATP  
4. page 17 : Modify footprint from LED3 to LTST-C195KJRK7-3  
MB 03/23  
5. page 24 : Modify footprint from L10 to M-R0805  
MB 3/27  
6. page 18 : Modify footprint from L29 to CK-223LC0801T2.2  
7. page 18 : Modify footprint from L1 to CK-ATCM3216-900T  
8. page 18 : Remove RP6  
9. page 18 : Remove R15 R16  
10. page 21 : Remove L523 RPS10  
11. page 22 : Modify Value from CN8 to CON-WTB-85204-02001  
MB 3/30  
12. page 24 : Modify footprint from H12 to HOLEC315D150  
MB 3/31  
13. page 14 : Modify R116 11K to 12K  
14. page 22 : Modify R176 R708 68K-1-04 to 63.4K-1-04  
MB 4/02  
15. Page 17 : Modify R200 10K-04 Change To @10K-04  
16. Page 17 : Modify R199 0-04 Change To @0-04  
17. Page 17 : Modify Q34 @FET-2N7002E Change To FET-2N7002E  
18. Page 31 : Modify U1 EMC1402 Change To ADM1032  
MB 4/02  
19. page 18 : Modify Value from L29 to CK-SB0503TL-015  
MB 4/06  
20. page 17 : Modify Value from R194 to 820-04  
21. page 17 : Modify Value from R192 to 390-04  
22. page 22 : Modify Value C366 C368 C752 C759 from 1U-6.3-04R-K change to .1U-10-04X-K  
23. page 22 : Modify Value C360 from 1U-6.3-04R-k change to .47U-6.3-04Y-Z  
24. page 18 : Remove RP511  
25. page 18 : Remove RP501  
MB 4/07  
26. page 25 : Modify Location from PR573 to PR88  
27. page 29 : Modify Location from PR55 to PR580  
28. page 29 : Modify Location from PC86 to PC586  
29. page 24 : Add Part C402 C403 C756 C405 C406 C407 C766 C409 C410 C411 C412 C767 C768  
30. page 24 : Add Part L543 L544 L541 L542 L545 L546 L547 L548  
MB 4/08  
31. page 19 : Modify H1 footprint to holec315d118-1  
32. page 25 : Modify Location from PC4 to PC564  
33. page 25 : Modify Location from PC85 to PC558  
34. page 29 : Modify Location from PC586 to PC85  
35. page 29 : Modify Location from PR580 to PR55

**MB 3/19 Power Modify**

1. Page 26 : Modify 26 add PR36 1-1-08,PR41 1-1-08,PC30 2.2N-50V-06X-K SNB for RING OVERSHOOT  
2. Page 29 : Modify 27 add PR72 2.2-1-06,PR43 2.2-08,PC33 2700P-50V-06X-K,PR55 2.2-08,PC86 680P-50-06X-K SNB for RING OVERSHOOT

**MB 3/23 Power Modify**

1. Page 25 : Modify 28 add PR573 @51K-1-04 for safety request

**MB 4/5 Power Modify**

1. Page 25 : Modify 29 Remove PS501  
2. Page 25 : Modify 30 Add Non audio circuit  
3. Page 26 : Modify 31 Add PCS22 ALD-100U-25

**MB 4/7 Power Modify**

1. Page 29 : Modify 32 PR580,PR43 FOOTPRINT CHANGE TO M-R0603  
2. Page 25 : Modify 33 PL1,PL504 FOOTPRINT CHANGE TO M-R0805

**MB 4/8 Power Modify**

1. Page 26 : Delete PR42 510K-1-04,PO511 FET-2N7002E,PR578 10K-1-04,PCS36 470P-50-04X-K  
PR76 931K-1-04,PC20 FET-2N7002E,PR579 10K-1-04,PCS57 470P-50-04X-K  
FOR 5V1.5V -3% VOLTAGE  
PR19 15K-1-04 CHANGE TO 13K-1-04 FOR ENHANCE USB PORT  
Delete PR511 150K-1-04,PR513 330K-1-04  
Add PC509 1000P-25-04X-K

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