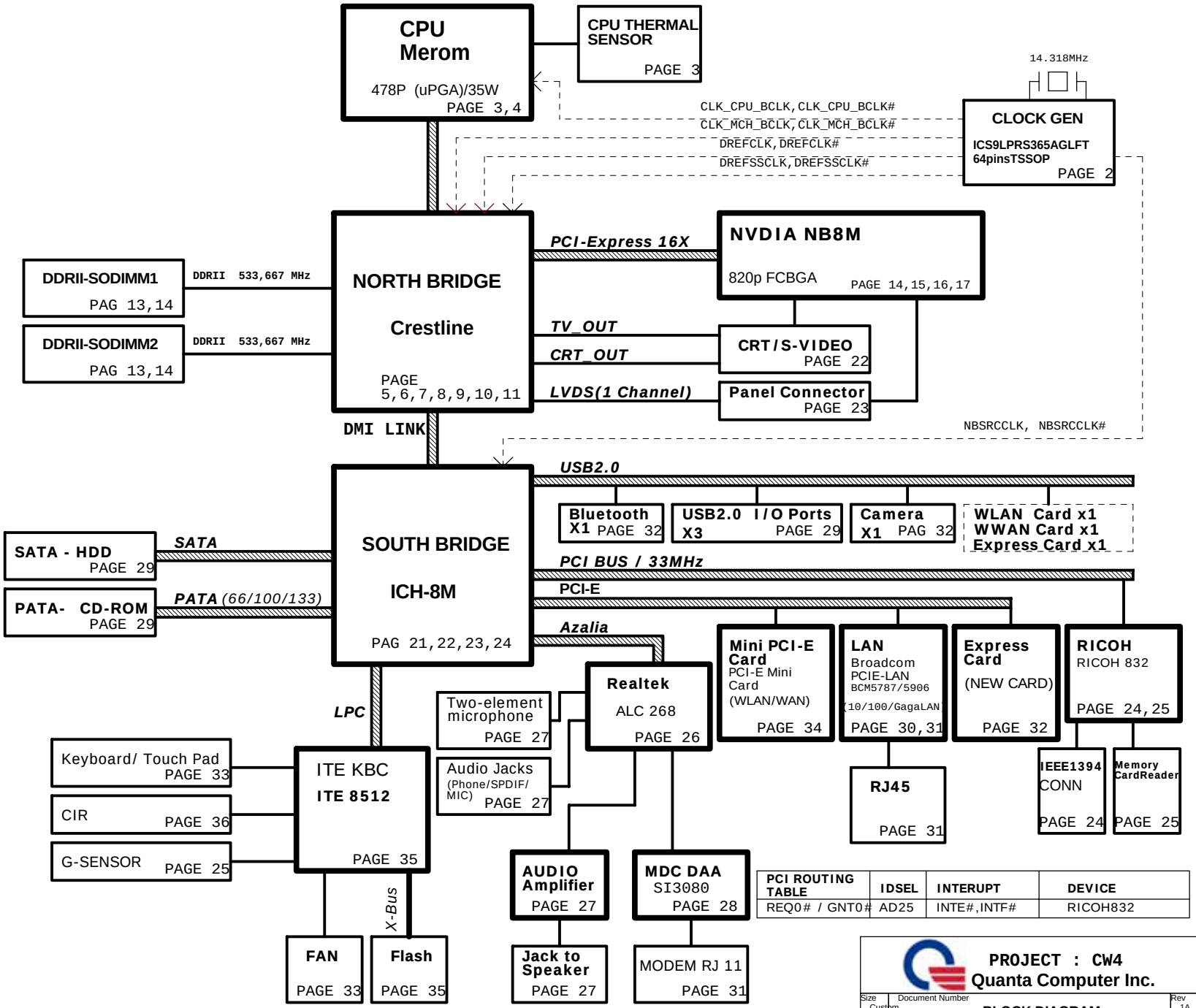
CW4 BLOCK DIAGRAM

01

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT



SYSTEM CHARGER(MAX8724)
PAGE 41

SYSTEM POWER ISL6236
PAGE 42

DDR II SMDDR_VTERM
1.8V/1.8VSUS(MAX8632ETI+)
PAGE 46

+1.05V / +1.5V (ISL6269A)
PAGE 44, 45

VGACORE(1.0V)MAX1993ETG
PAGE 45

CPU CORE MAX8770
PAGE 44

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832

PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

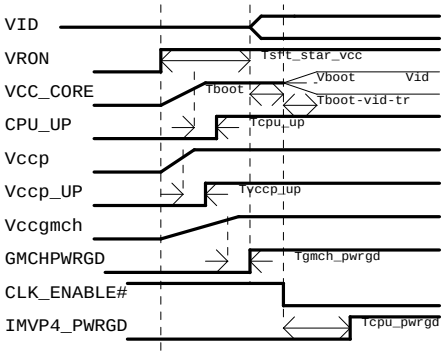
Date: Friday, November 03, 2006 Sheet 1 of 44

Board Stack up Description

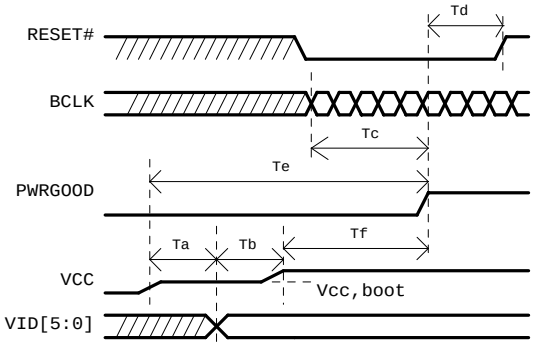
PCB Layers

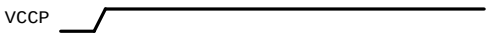
Layer 1		TOP
Layer 2		GND
Layer 3		IN1
Layer 4		IN2
Layer 5		SVCC
Layer 6		IN3
Layer 7		GND
Layer 8		BOTTOM

Power On Sequencing Timing Diagram



YONAH Power-up Timing Specifications



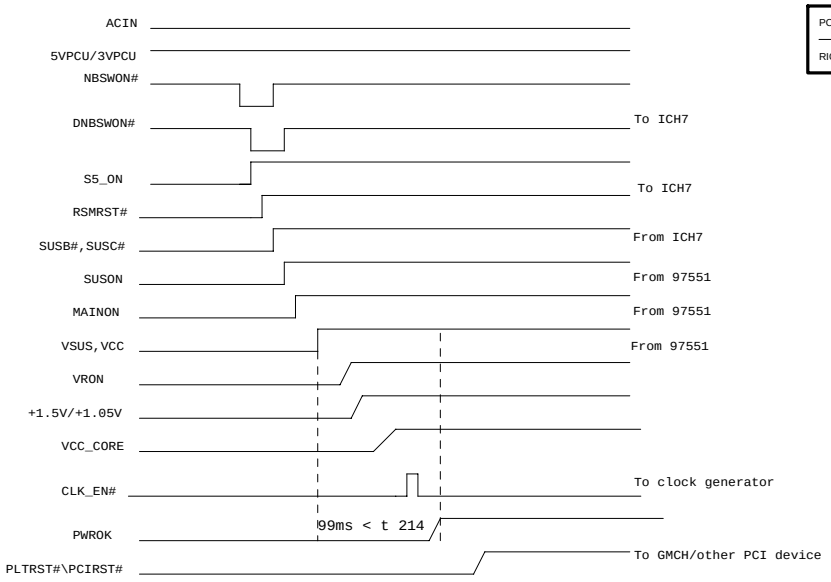


Ta=VCC and VCCP asseration to VID[5:0] vaild
Tb=VID[5:0] stable to VCC vaild
Tc=BCLK stable to PWRGOOD assertion
Td=PWRGOOD to RESET# de-assertion time
Te=Vcc,boot vaild to PWRGOOD assertion time

Voltage Rails

Voltage Rails	ON S0~S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE	X				VRON
+1.5V	X				MAINON
+1.05V	X				MAINON
5V_S5/3V_S5/1.5V_S5	X	X	X	X	S5_ON
5VSUS/3VSUS/1.8VSUS	X	X			SUSON
SMDDR_VTERM/+2.5V/+3V/+5V/+12V	X				MAINON
+VCC_GFX_CORE/+1.2V_GFX_PCIE	X				MAINON
LANVCC	X	X	X	X	LAN_ON
3VPCU	X	X	X	X	VL
5VPCU	X	X	X	X	VL

ACIN POWER ON TIMING



PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
RICOH832	AD25	REQ0# / GNT0#	INT E#/F#

PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SYSTEM INFORMATION	1A

Date: Friday, November 03, 2006 Sheet 2 of 44

internal have already build-in 33ohm damping resistor

U7 CK505

ICS9LPRS365BGLFT/SLG8SP512T

GCLK_SEL = FCTSEL1

FCTSEL1 (PIN13)	PIN13	PIN14	PIN17	PIN18
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

0=overclocking of CPU and SRC Allowed

1 = overclocking of CPU and SRC not Allowed

0=UMA
1 = External VGA

Disable ITP

CPU Clock select

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

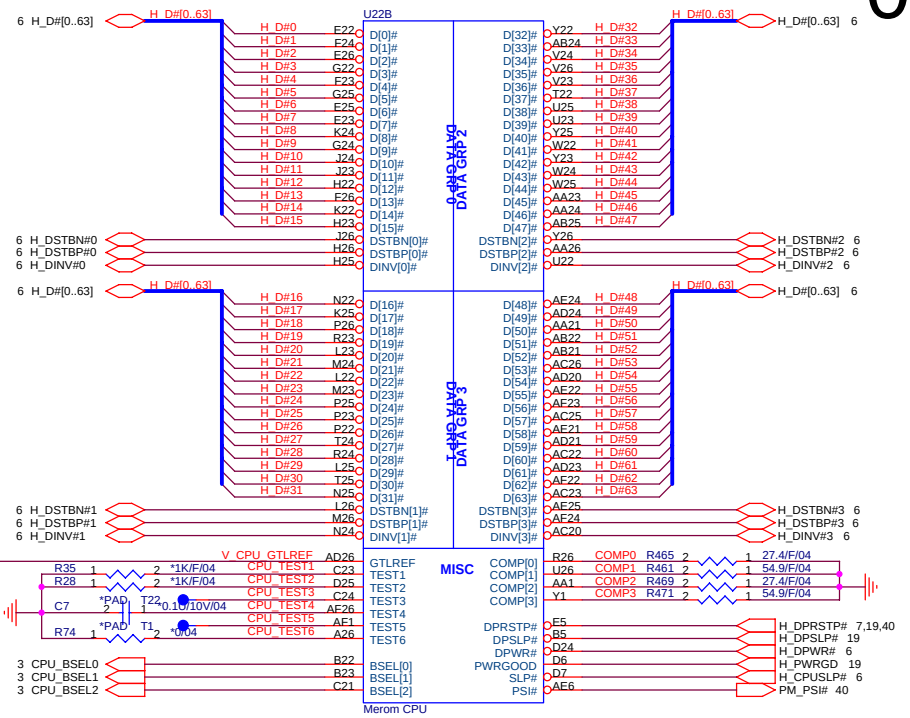
for EMI

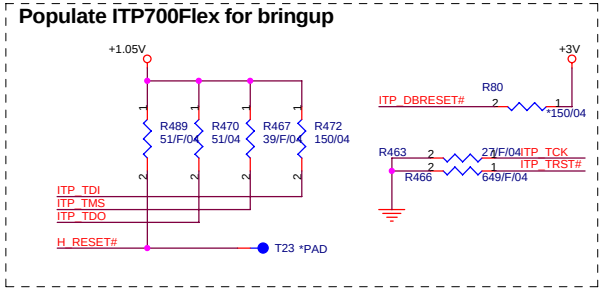
PROJECT : CW4
Quanta Computer Inc.

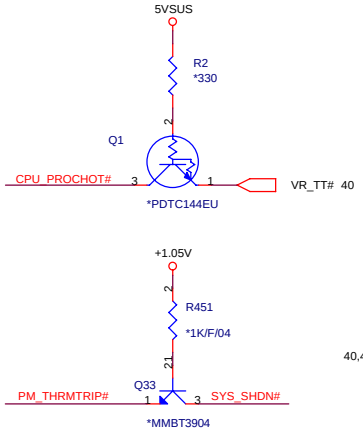
Size	Document Number	Rev
Custom	CLOCK GENERATOR	1A

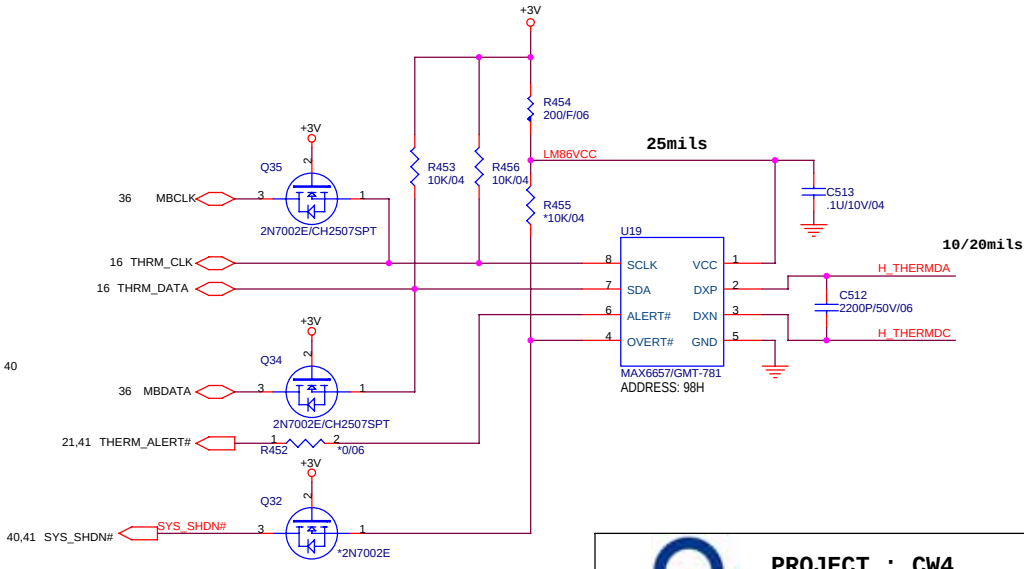
Date: Friday, November 03, 2006 Sheet 3 of 44

Layout Note:
Place voltage divider within 0.5" of GTLREF pin









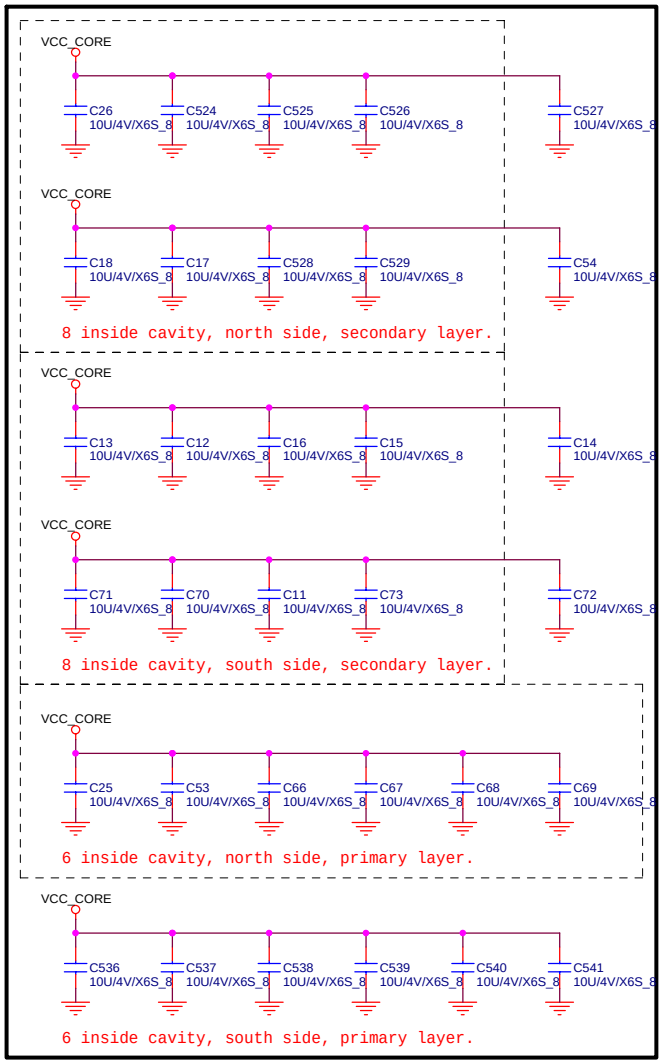
ITP disable guidelines

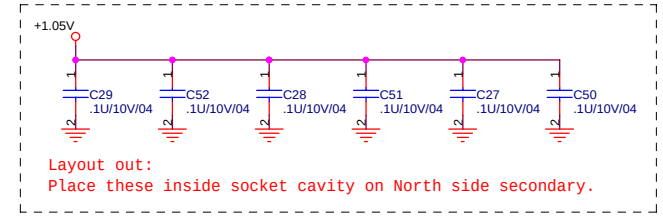
Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 1%	VTT	Within 2.0" of the ITP
TRST#	500-680ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 1%	GND	Within 2.0" of the ITP
TDO	150 ohm +/- 5%	VTT	Within 2.0" of the ITP

PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Merom (HOST BUS)	1A

Date: Friday, November 03, 2006 Sheet 4 of 44

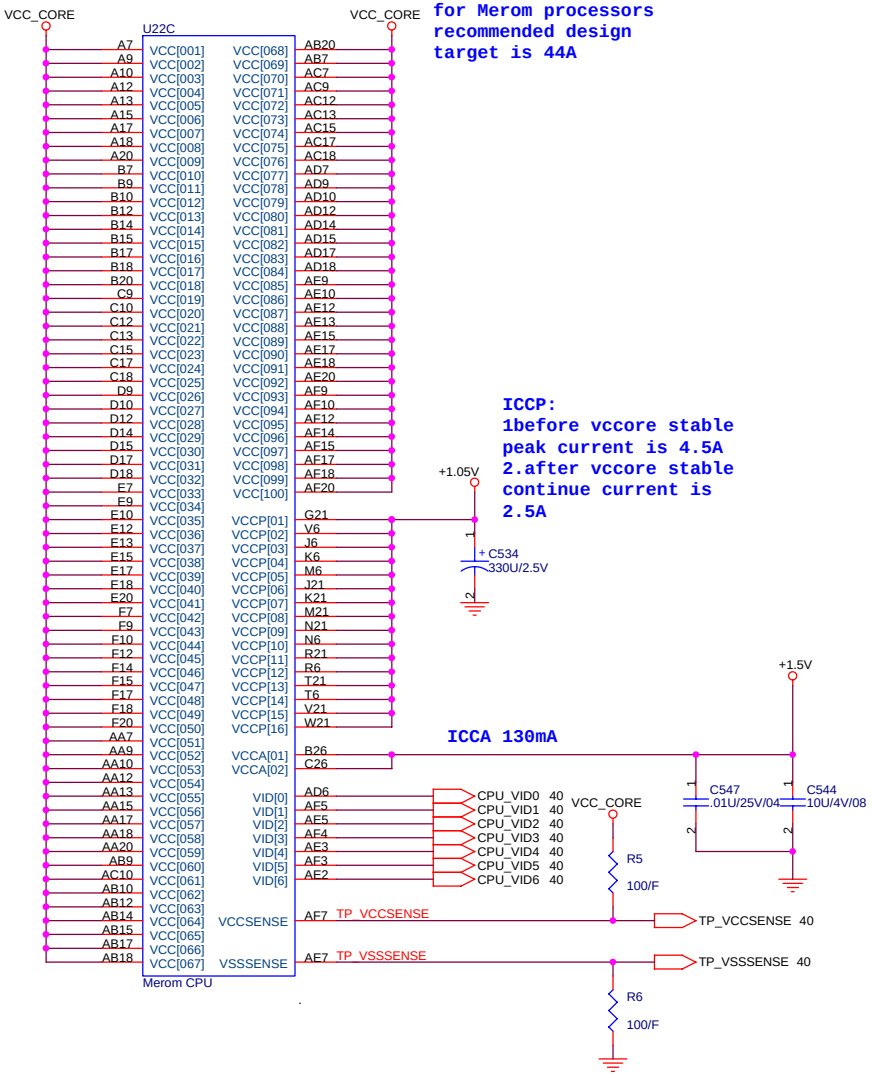


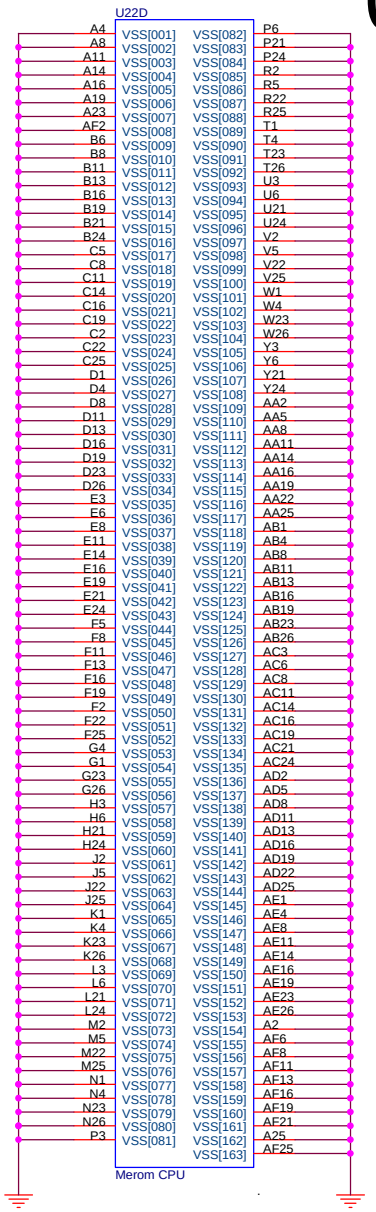


ICCODE:
for Merom processors
recommended design
target is 44A

ICCP:
1before vccore stable
peak current is 4.5A
2.after vccore stable
continue current is
2.5A

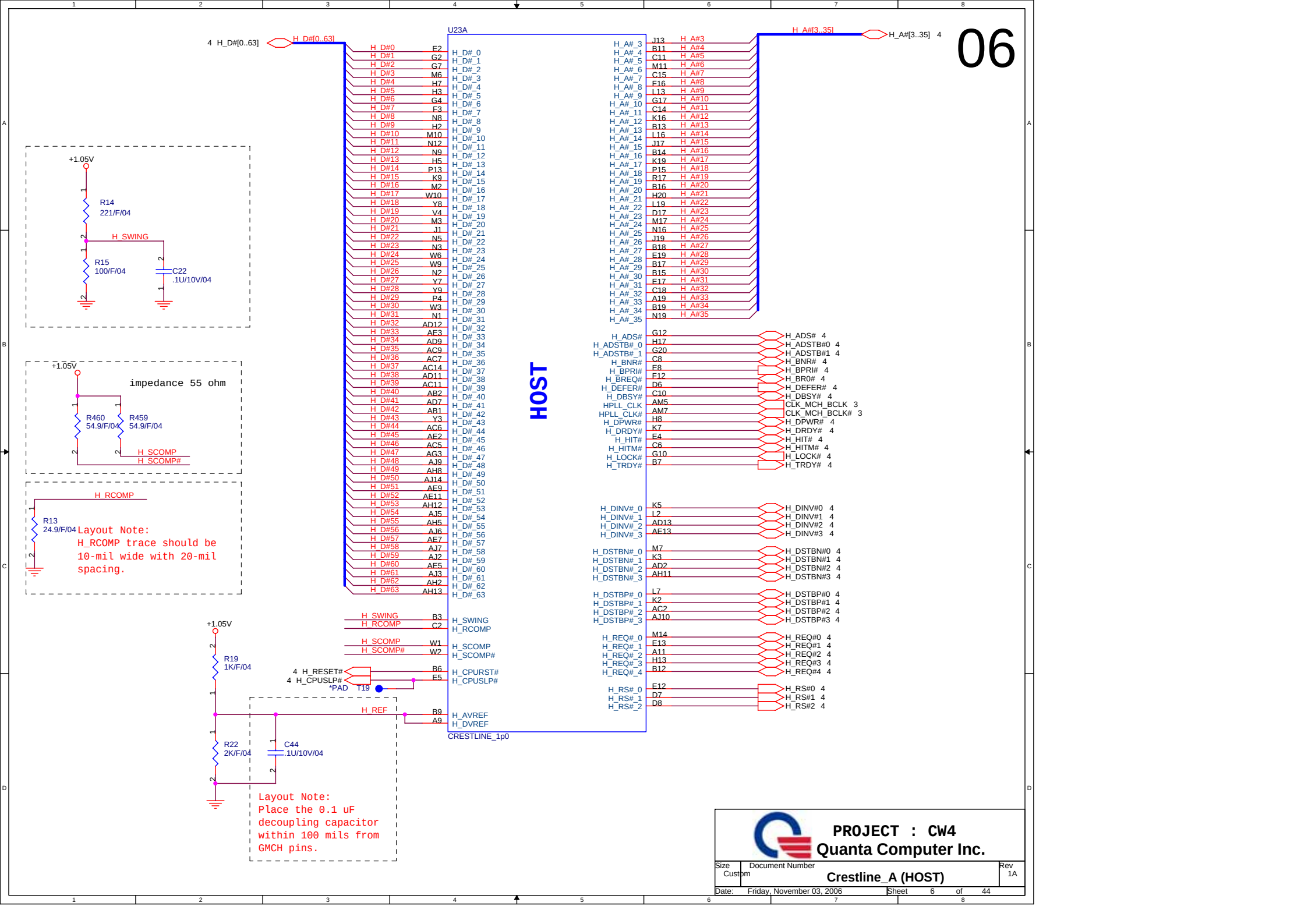
ICCA 130mA





PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Merom (POWER/NC)	1A
Date: Friday, November 03, 2006	Sheet 5 of 44	


06
U23A
HOST
CRESTLINE_1p0
4 H_D#[0..63]
H_D#[0..63]
H_A#[3..35]
H_A#[3..35] 4
+1.05V
R14
221/F/04
H_SWING
R15
100/F/04
C22
.1U/10V/04
+1.05V
impedance 55 ohm
R460
54.9/F/04
R459
54.9/F/04
H_SCOMP
H_SCOMP#
H_RCOMP
R13
24.9/F/04
Layout Note:
H_RCOMP trace should be
10-mil wide with 20-mil
spacing.
+1.05V
R19
1K/F/04
R22
2K/F/04
C44
.1U/10V/04
H_REF
Layout Note:
Place the 0.1 uF
decoupling capacitor
within 100 mils from
GMCH pins.
4 H_RESET#
4 H_CPUSLP#
*PAD T19
PROJECT : CW4
Quanta Computer Inc.
Size
Custom
Document Number
Crestline_A (HOST)
Rev
1A
Date: Friday, November 03, 2006
Sheet 6 of 44

WW22 update
--- MA14 needs to be routed if customers are planning on using 2Gb technology and width=8 (by 8) DIMMs

Layout Note:
Location of all MCH_CFG strap resistors needs to be close to minmize stub.

CRESTLINE_1p0

CRT Discrete / UMA

R48	NC	0
R49	NC	0
R2618	NC	39
R2627	0	1.3K/F
R2623	NC	39

Resistor Discret UMA

R64	0	NC
R60	0	NC
R64	0	NC
R60	0	NC
R74	0	150
R77	0	150
R65	0	150

PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline_B (VGA,DMI)	1A

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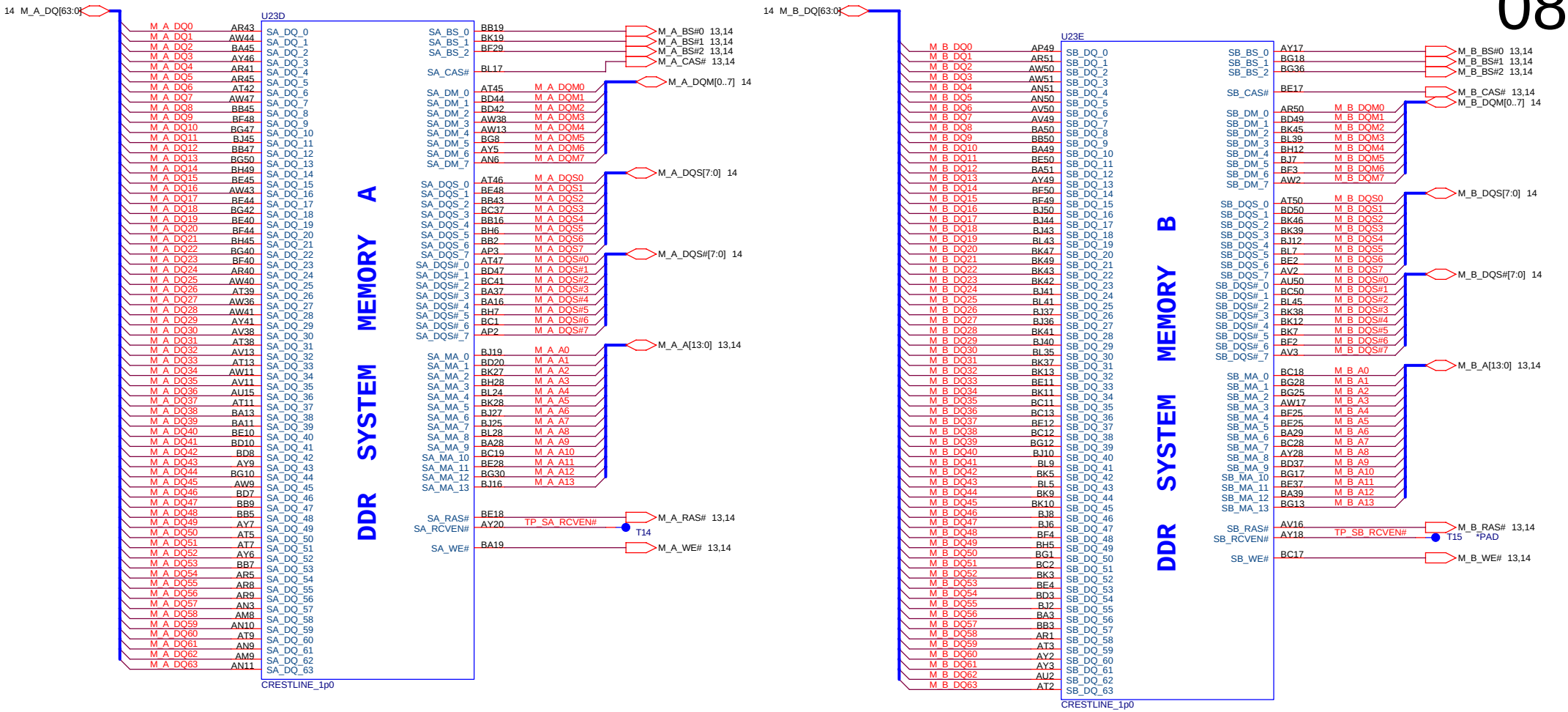
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U23D
DDR SYSTEM MEMORY A
SA_DQ_0 SA_DQ_1 SA_DQ_2 SA_DQ_3 SA_DQ_4 SA_DQ_5 SA_DQ_6 SA_DQ_7 SA_DQ_8 SA_DQ_9 SA_DQ_10 SA_DQ_11 SA_DQ_12 SA_DQ_13 SA_DQ_14 SA_DQ_15 SA_DQ_16 SA_DQ_17 SA_DQ_18 SA_DQ_19 SA_DQ_20 SA_DQ_21 SA_DQ_22 SA_DQ_23 SA_DQ_24 SA_DQ_25 SA_DQ_26 SA_DQ_27 SA_DQ_28 SA_DQ_29 SA_DQ_30 SA_DQ_31 SA_DQ_32 SA_DQ_33 SA_DQ_34 SA_DQ_35 SA_DQ_36 SA_DQ_37 SA_DQ_38 SA_DQ_39 SA_DQ_40 SA_DQ_41 SA_DQ_42 SA_DQ_43 SA_DQ_44 SA_DQ_45 SA_DQ_46 SA_DQ_47 SA_DQ_48 SA_DQ_49 SA_DQ_50 SA_DQ_51 SA_DQ_52 SA_DQ_53 SA_DQ_54 SA_DQ_55 SA_DQ_56 SA_DQ_57 SA_DQ_58 SA_DQ_59 SA_DQ_60 SA_DQ_61 SA_DQ_62 SA_DQ_63
M_A_DQ0 AR43
M_A_DQ1 AW44
M_A_DQ2 BA45
M_A_DQ3 AY46
M_A_DQ4 AR41
M_A_DQ5 AR45
M_A_DQ6 AT42
M_A_DQ7 AW47
M_A_DQ8 BB45
M_A_DQ9 BF48
M_A_DQ10 BG47
M_A_DQ11 BJ45
M_A_DQ12 BB47
M_A_DQ13 BG50
M_A_DQ14 BH49
M_A_DQ15 BE45
M_A_DQ16 AW43
M_A_DQ17 BE44
M_A_DQ18 BG42
M_A_DQ19 BE40
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M_A_DQ23 BF40
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M_A_DQ28 AW41
M_A_DQ29 AY41
M_A_DQ30 AV38
M_A_DQ31 AT38
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M_A_DQ37 AT11
M_A_DQ38 BA13
M_A_DQ39 BA11
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M_A_DQ41 BD10
M_A_DQ42 BD8
M_A_DQ43 AY9
M_A_DQ44 BG10
M_A_DQ45 AW9
M_A_DQ46 BD7
M_A_DQ47 BB9
M_A_DQ48 BB5
M_A_DQ49 AY7
M_A_DQ50 AT5
M_A_DQ51 AT7
M_A_DQ52 AY6
M_A_DQ53 BB7
M_A_DQ54 AR5
M_A_DQ55 AR8
M_A_DQ56 AR9
M_A_DQ57 AN3
M_A_DQ58 AM8
M_A_DQ59 AN10
M_A_DQ60 AT9
M_A_DQ61 AN9
M_A_DQ62 AM9
M_A_DQ63 AN11
CRESTLINE_1p0
SA_BS_0 BB19
SA_BS_1 BK19
SA_BS_2 BF29
SA_CAS# BL17
SA_DM_0 AT45
SA_DM_1 BD44
SA_DM_2 BD42
SA_DM_3 AW38
SA_DM_4 AW13
SA_DM_5 BG8
SA_DM_6 AY5
SA_DM_7 AN6
SA_DQS_0 AT46
SA_DQS_1 BE48
SA_DQS_2 BB43
SA_DQS_3 BC37
SA_DQS_4 BB16
SA_DQS_5 BH6
SA_DQS_6 BB2
SA_DQS_7 AP3
SA_DQS#_0 AT47
SA_DQS#_1 BD47
SA_DQS#_2 BC41
SA_DQS#_3 BA37
SA_DQS#_4 BA16
SA_DQS#_5 BH7
SA_DQS#_6 BC1
SA_DQS#_7 AP2
SA_MA_0 BJ19
SA_MA_1 BD20
SA_MA_2 BK27
SA_MA_3 BH28
SA_MA_4 BL24
SA_MA_5 BK28
SA_MA_6 BJ27
SA_MA_7 BJ25
SA_MA_8 BL28
SA_MA_9 BA28
SA_MA_10 BC19
SA_MA_11 BE28
SA_MA_12 BG30
SA_MA_13 BJ16
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M_A_DQM3
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M_A_DQM6
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M_A_A5
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M_A_A13
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TP_SA_RCVEN#
T14
M_A_WE# 13,14
14 M_B_DQ[63:0]
U23E
DDR SYSTEM MEMORY B
SB_DQ_0 SB_DQ_1 SB_DQ_2 SB_DQ_3 SB_DQ_4 SB_DQ_5 SB_DQ_6 SB_DQ_7 SB_DQ_8 SB_DQ_9 SB_DQ_10 SB_DQ_11 SB_DQ_12 SB_DQ_13 SB_DQ_14 SB_DQ_15 SB_DQ_16 SB_DQ_17 SB_DQ_18 SB_DQ_19 SB_DQ_20 SB_DQ_21 SB_DQ_22 SB_DQ_23 SB_DQ_24 SB_DQ_25 SB_DQ_26 SB_DQ_27 SB_DQ_28 SB_DQ_29 SB_DQ_30 SB_DQ_31 SB_DQ_32 SB_DQ_33 SB_DQ_34 SB_DQ_35 SB_DQ_36 SB_DQ_37 SB_DQ_38 SB_DQ_39 SB_DQ_40 SB_DQ_41 SB_DQ_42 SB_DQ_43 SB_DQ_44 SB_DQ_45 SB_DQ_46 SB_DQ_47 SB_DQ_48 SB_DQ_49 SB_DQ_50 SB_DQ_51 SB_DQ_52 SB_DQ_53 SB_DQ_54 SB_DQ_55 SB_DQ_56 SB_DQ_57 SB_DQ_58 SB_DQ_59 SB_DQ_60 SB_DQ_61 SB_DQ_62 SB_DQ_63
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M_B_DQ60 AY2
M_B_DQ61 AY3
M_B_DQ62 AU2
M_B_DQ63 AT2
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SB_BS_2 BG36
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SB_DM_1 BD49
SB_DM_2 BK45
SB_DM_3 BL39
SB_DM_4 BH12
SB_DM_5 BJ7
SB_DM_6 BF3
SB_DM_7 AW2
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SB_DQS_1 BD50
SB_DQS_2 BK46
SB_DQS_3 BK39
SB_DQS_4 BJ12
SB_DQS_5 BL7
SB_DQS_6 BE2
SB_DQS_7 AV2
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SB_DQS#_1 BC50
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SB_DQS#_4 BK12
SB_DQS#_5 BK7
SB_DQS#_6 BF2
SB_DQS#_7 AV3
SB_MA_0 BC18
SB_MA_1 BG28
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SB_MA_3 AW17
SB_MA_4 BF25
SB_MA_5 BE25
SB_MA_6 BA29
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M_B_DQS#7
M_B_DQS#[7:0] 14
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M_B_A6
M_B_A7
M_B_A8
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M_B_A12
M_B_A13
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TP_SB_RCVEN#
T15 *PAD
M_B_WE# 13,14
PROJECT : CW4
Quanta Computer Inc.
Size Custom
Document Number
Crestline_C (DDR2)
Rev 1A
Date: Friday, November 03, 2006
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POWER

IVCCSM supply current 1 channel 1.615A 2 channel 3.318A

Ivcc (External GFX 1.310 A, integrate 1.572 A)

Layout Note: 370 mils from edge.

Layout Note: Inside GMCH cavity.

Ivcc_AXG Graphics core supply current 7.7A

Layout Note: 370 mils from edge.

Layout Note: Inside GMCH cavity for VCC_AXG.

GMCH 1.05V	current(A)	Remark
VCC Core	1.573	(1.3A for external 6bx integrated Gfx
VCC_AXG	7.7	
VCC_AXD	0.2	
VTT	0.85	FSB VCCP
VCC_PEG	1.2	for PCIEG
VCC_AXM	0.54	for IAMT function
VCCR_RX_DMI	0.25	DMI
SUM	**12.313**	

Ivcc_AXM Controller supply current 540mA

Layout Note: Inside GMCH cavity.

Layout Note: Place close to GMCH edge.

Layout Note: Place C901 where LVDS and DDR2 taps.

Layout Note: Place on the edge.

CRESTLINE_1p0

CRESTLINE_1p0

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Quanta Computer Inc.	
Size: Custom	Document Number: Crestline_D (VCC,NCTF)
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LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If LVDS enable
VCCD_LVDS	GND	1.8V
VCCA_LVDS	GND	1.8V
VCC_TX_LVDS	GND	1.8V

CRT/TV Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT_DAC	3.3V	GND	VCCA_TVC_DAC	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVDAC	1.5V	1.5V
VCCD_QDAC	1.5V	GND	VCCA_DAC_BG	3.3V	GND
VCCA_TVA_DAC	3.3V	GND	VSS_DAC_BG	GND	GND
VCCA_TVB_DAC	3.3V	GND	VCCSYNC	3.3V	GND

IV&EV Dis/Enable setting

FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC

FB_120ohm+-25%_100mHz _200mA_0.2ohm DC

FB_180ohm+-25% 100mHz_1500mA_ 0.09ohm DC

FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC

FB_220ohm+-25%_100MHz _2A_0.1ohm DC

0.1Caps should be placed 200 mils with in its pins.

22nF & 0.1uF for VCC_TVDACA:C_R should be placed with in 250 mils from Crestline.

Ivcc_VTT FSB supply current 0.85A

Place on the edge.

Reserved L81 pad for inductor.

Place caps close to VCC_AXD.

Ivcc_DMI supply current 100mA

Place caps close to VCC_AXF

Ivcc_PEG supply current 1.2A

Ivcc_RX_DMI supply current 250mA

Ivcca_PEG_BG supply current 100mA

+3V_VCC_HV

40 mil wide

POWER

CRESTLINE_1p0

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Quanta Computer Inc.	
Size: Custom	Document Number: Crestline_E (POWER)
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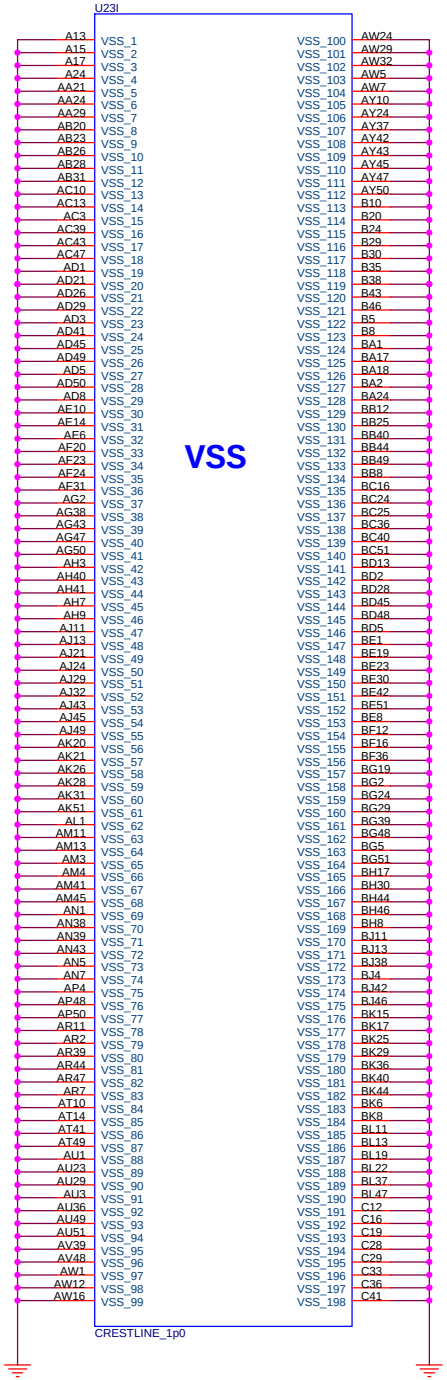

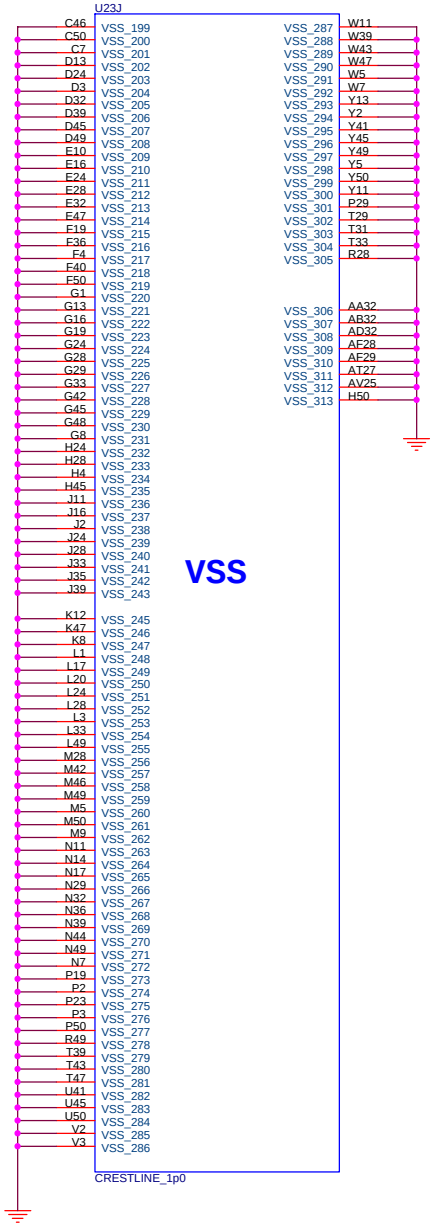

PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Crestline_F (VSS)	1A

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Strap table

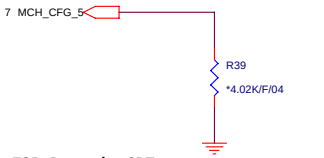
All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal

CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

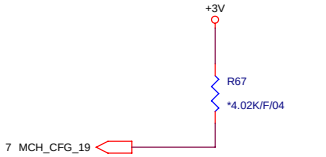
DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIX4(Default)



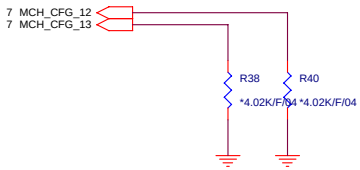
DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane



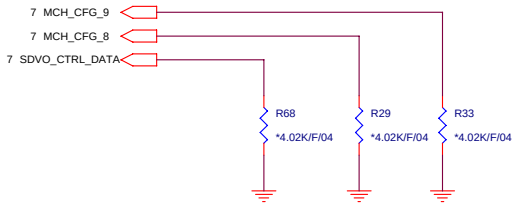
XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)

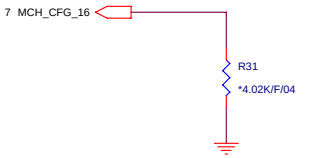


SDVO Present

Strap define at External DVI control page

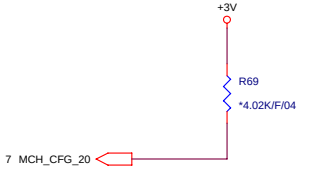
FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)



SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port



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Quanta Computer Inc.

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Custom	Crestline_F Strap	1A
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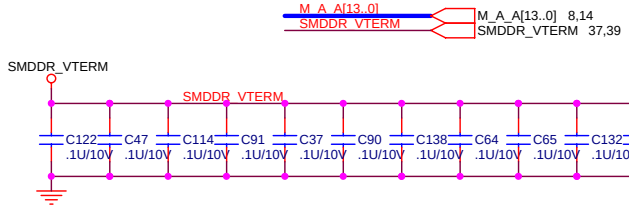
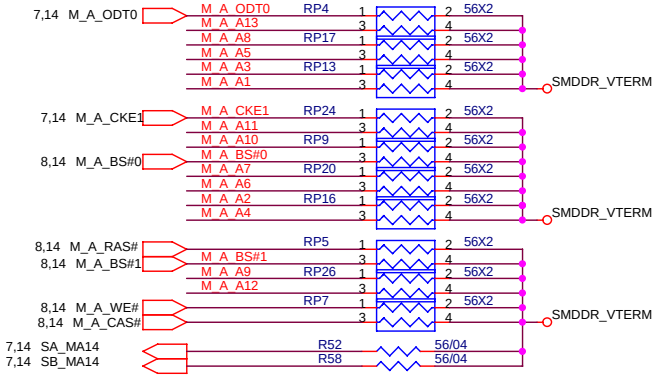
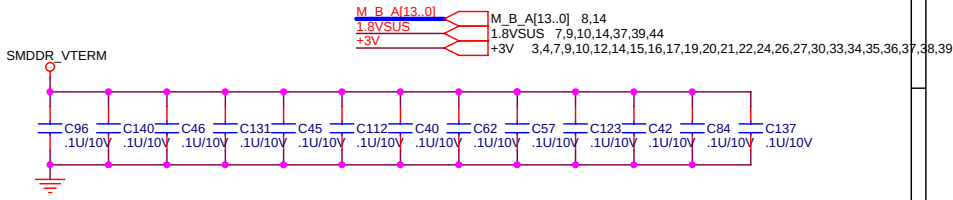
DDRII DUAL CHANNEL A,B.

DDRII A CHANNEL

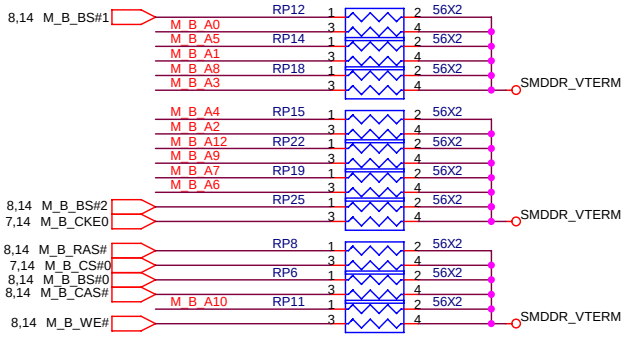


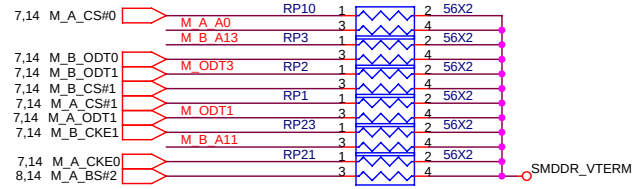


DDRII B CHANNEL



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM





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Quanta Computer Inc.

Size	Document Number	Rev
B	DDRII RES. ARRAY	1A

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CGCLK_SMB — CGCLK_SMB 3,35
CGDAT_SMB — CGDAT_SMB 3,35

M_A_CKE[0..1] — M_A_CKE[0..1] 7,13
M_A_CS#[0..1] — M_A_CS#[0..1] 7,13

M_A_RAS# — M_A_RAS# 8,13
M_A_CAS# — M_A_CAS# 8,13
M_A_WE# — M_A_WE# 8,13

M_A_CLK0 — M_A_CLK0 7
M_A_CLK0# — M_A_CLK0# 7
M_A_CLK1 — M_A_CLK1 7
M_A_CLK1# — M_A_CLK1# 7
M_A_BS#[0..2] — M_A_BS#[0..2] 8,13
M_A_ODT[0..1] — M_A_ODT[0..1] 7,13

M_A_DQM[0..7] — M_A_DQM[0..7] 8
M_A_DQ[0..63] — M_A_DQ[0..63] 8
M_A_DQS[0..7] — M_A_DQS[0..7] 8
M_A_DQS#[0..7] — M_A_DQS#[0..7] 8
M_A_A[13..0] — M_A_A[13..0] 8,13

+3V — +3V 3,4,7,9,10,12,15,16,17,19,20,21,22,24,26,27,30,33,34,35,36,37,38,39,40,41,42,43,44
1.8VSUS — 1.8VSUS 7,9,10,37,39,44

M_B_CKE[0..1] — M_B_CKE[0..1] 7,13
M_B_CS#[0..1] — M_B_CS#[0..1] 7,13

M_B_RAS# — M_B_RAS# 8,13
M_B_CAS# — M_B_CAS# 8,13
M_B_WE# — M_B_WE# 8,13

M_B_CLK0 — M_B_CLK0 7
M_B_CLK0# — M_B_CLK0# 7
M_B_CLK1 — M_B_CLK1 7
M_B_CLK1# — M_B_CLK1# 7
M_B_BS#[0..2] — M_B_BS#[0..2] 8,13
M_B_ODT[0..1] — M_B_ODT[0..1] 7,13

M_B_DQM[0..7] — M_B_DQM[0..7] 8
M_B_DQ[0..63] — M_B_DQ[0..63] 8
M_B_DQS[0..7] — M_B_DQS[0..7] 8
M_B_DQS#[0..7] — M_B_DQS#[0..7] 8
M_B_A[13..0] — M_B_A[13..0] 8,13

CN13A — PC2100 DDR2 SDRAM SO-DIMM (200P) — DDRII_SOCKET---2ND

CN13B — PC2100 DDR2 SDRAM SO-DIMM (200P) — DDRII_SOCKET---2ND

CN12A — PC2100 DDR2 SDRAM SO-DIMM (200P) — DDRII_SOCKET---1ST

CN12B — PC2100 DDR2 SDRAM SO-DIMM (200P) — DDRII_SOCKET---1ST

CKEA 0,1
H 9.2

CKEB 0,1
H 5.2

DIM2_SA0 — R458 10K/04 — DIM2_SA1 — R457 10K/04 — +3V
SMbus address A4

R4 10K/04 DIM1_SA0 — R3 10K/04 DIM1_SA1
SMbus address A0

Place these Caps near So-Dimm1.

1.8VSUS — C554 2.2U/6.3V/06 — C543 2.2U/6.3V/06 — C100 2.2U/6.3V/06 — C58 2.2U/6.3V/06 — C104 2.2U/6.3V/06 — C545 2.2U/6.3V/06 — C126 .1U/10V/04 — C80 .1U/10V/04 — C74 .1U/10V/04 — C556 .1U/10V/04 — C75 .1U/10V/04

SMDDR_VREF_DIMM — C587 .1U/10V/04 — C582 2.2U/6.3V/06

+3V — C1 2.2U/6.3V/06 — C2 .1U/10V/04

SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.

Place these Caps near So-Dimm2.

1.8VSUS — C550 2.2U/6.3V/06 — C77 2.2U/6.3V/06 — C127 2.2U/6.3V/06 — C59 2.2U/6.3V/06 — C81 2.2U/6.3V/06 — C553 .1U/10V/04 — C93 .1U/10V/04 — C108 .1U/10V/04 — C87 .1U/10V/04 — C98 .1U/10V/04 — C109 .1U/10V/04

SMDDR_VREF_DIMM — C590 .1U/10V/04 — C591 2.2U/6.3V/06

+3V — C4 2.2U/6.3V/06 — C3 .1U/10V/04

SO-DIMM BYPASS PLACEMENT :
Place these Caps near So-Dimm2
No Vias Between the Trace of PIN to CAP.

SMDDR_VREF_DIMM — C583 470P/50V/04 — R111 0/06 — SMDDR_VREF
R112 — 1.8VSUS
R117 *10K/F/06 — *10K/F/06

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Quanta Computer Inc.

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Custom	DDRII SO-DIMM(200P)	1A
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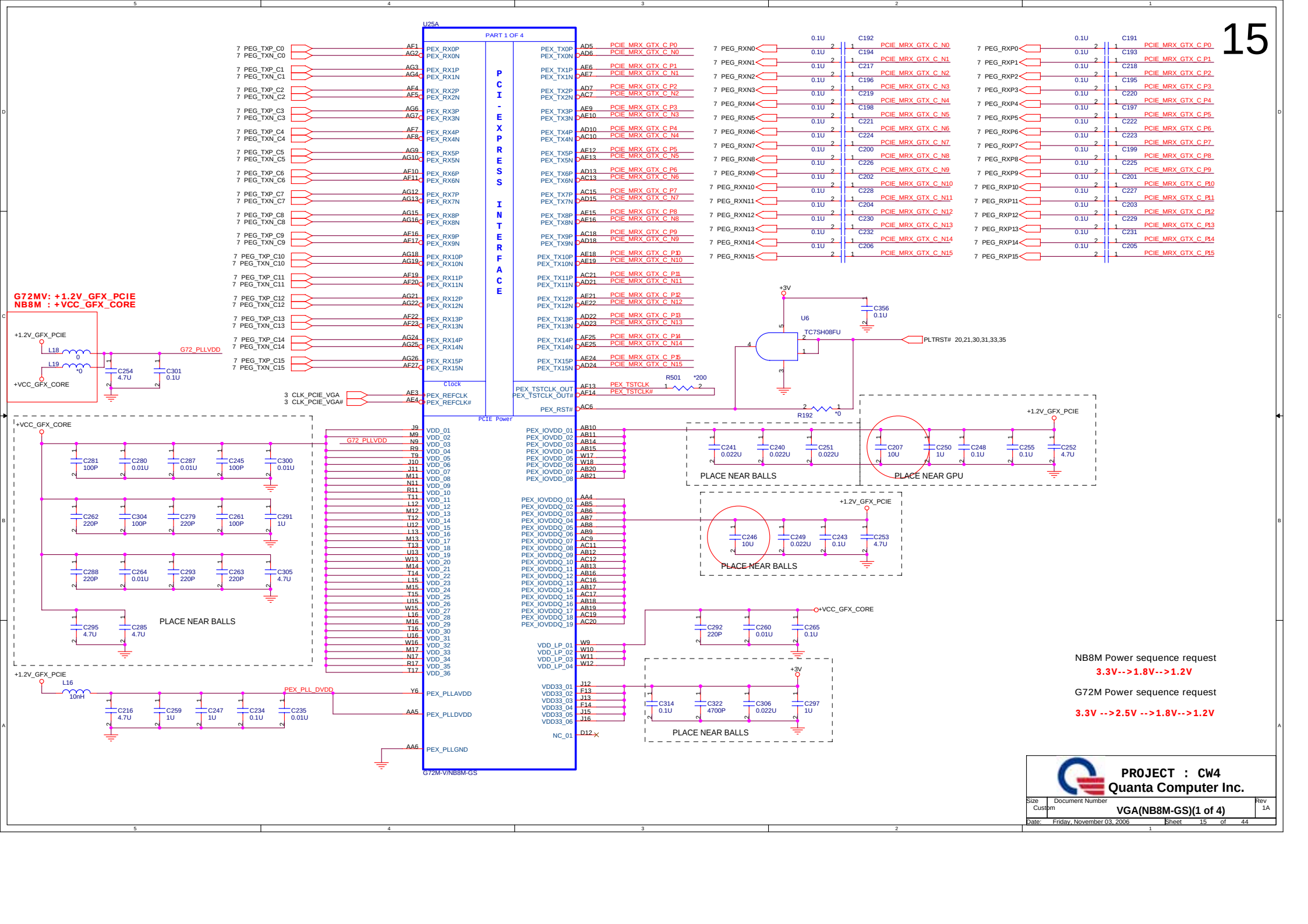
U25A
PART 1 OF 4
PCI-EXPRESS INTERFACE
PEX_RX0P
PEX_RX0N
PEX_RX1P
PEX_RX1N
PEX_RX2P
PEX_RX2N
PEX_RX3P
PEX_RX3N
PEX_RX4P
PEX_RX4N
PEX_RX5P
PEX_RX5N
PEX_RX6P
PEX_RX6N
PEX_RX7P
PEX_RX7N
PEX_RX8P
PEX_RX8N
PEX_RX9P
PEX_RX9N
PEX_RX10P
PEX_RX10N
PEX_RX11P
PEX_RX11N
PEX_RX12P
PEX_RX12N
PEX_RX13P
PEX_RX13N
PEX_RX14P
PEX_RX14N
PEX_RX15P
PEX_RX15N
PEX_TX0P
PEX_TX0N
PEX_TX1P
PEX_TX1N
PEX_TX2P
PEX_TX2N
PEX_TX3P
PEX_TX3N
PEX_TX4P
PEX_TX4N
PEX_TX5P
PEX_TX5N
PEX_TX6P
PEX_TX6N
PEX_TX7P
PEX_TX7N
PEX_TX8P
PEX_TX8N
PEX_TX9P
PEX_TX9N
PEX_TX10P
PEX_TX10N
PEX_TX11P
PEX_TX11N
PEX_TX12P
PEX_TX12N
PEX_TX13P
PEX_TX13N
PEX_TX14P
PEX_TX14N
PEX_TX15P
PEX_TX15N
Clock
PEX_REFCLK
PEX_REFCLK#
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT#
PEX_TSTCLK
PEX_TSTCLK#
PEX_RST#
PCIE Power
PEX_IOVDD_01
PEX_IOVDD_02
PEX_IOVDD_03
PEX_IOVDD_04
PEX_IOVDD_05
PEX_IOVDD_06
PEX_IOVDD_07
PEX_IOVDD_08
PEX_IOVDDQ_01
PEX_IOVDDQ_02
PEX_IOVDDQ_03
PEX_IOVDDQ_04
PEX_IOVDDQ_05
PEX_IOVDDQ_06
PEX_IOVDDQ_07
PEX_IOVDDQ_08
PEX_IOVDDQ_09
PEX_IOVDDQ_10
PEX_IOVDDQ_11
PEX_IOVDDQ_12
PEX_IOVDDQ_13
PEX_IOVDDQ_14
PEX_IOVDDQ_15
PEX_IOVDDQ_16
PEX_IOVDDQ_17
PEX_IOVDDQ_18
PEX_IOVDDQ_19
VDD_LP_01
VDD_LP_02
VDD_LP_03
VDD_LP_04
VDD33_01
VDD33_02
VDD33_03
VDD33_04
VDD33_05
VDD33_06
NC_01
VDD_01
VDD_02
VDD_03
VDD_04
VDD_05
VDD_06
VDD_07
VDD_08
VDD_09
VDD_10
VDD_11
VDD_12
VDD_13
VDD_14
VDD_15
VDD_16
VDD_17
VDD_18
VDD_19
VDD_20
VDD_21
VDD_22
VDD_23
VDD_24
VDD_25
VDD_26
VDD_27
VDD_28
VDD_29
VDD_30
VDD_31
VDD_32
VDD_33
VDD_34
VDD_35
VDD_36
PEX_PLLAVDD
PEX_PLLDVDD
PEX_PLLGND
G72M-V/NB8M-GS
G72MV: +1.2V_GFX_PCIE
NB8M : +VCC_GFX_CORE
+1.2V_GFX_PCIE
+VCC_GFX_CORE
L18
L19
G72_PLLVDD
PEX_PLL_DVDD
L16
10nH
PLACE NEAR BALLS
PLACE NEAR GPU
U6
TC7SH08FU
+3V
PLTRST# 20,21,30,31,33,35
R501 *200
R192 *0
CLK_PCIE_VGA
CLK_PCIE_VGA#
PCIE_MRX_GTX_C_P0
PCIE_MRX_GTX_C_N0
PCIE_MRX_GTX_C_P1
PCIE_MRX_GTX_C_N1
PCIE_MRX_GTX_C_P2
PCIE_MRX_GTX_C_N2
PCIE_MRX_GTX_C_P3
PCIE_MRX_GTX_C_N3
PCIE_MRX_GTX_C_P4
PCIE_MRX_GTX_C_N4
PCIE_MRX_GTX_C_P5
PCIE_MRX_GTX_C_N5
PCIE_MRX_GTX_C_P6
PCIE_MRX_GTX_C_N6
PCIE_MRX_GTX_C_P7
PCIE_MRX_GTX_C_N7
PCIE_MRX_GTX_C_P8
PCIE_MRX_GTX_C_N8
PCIE_MRX_GTX_C_P9
PCIE_MRX_GTX_C_N9
PCIE_MRX_GTX_C_P10
PCIE_MRX_GTX_C_N10
PCIE_MRX_GTX_C_P11
PCIE_MRX_GTX_C_N11
PCIE_MRX_GTX_C_P12
PCIE_MRX_GTX_C_N12
PCIE_MRX_GTX_C_P13
PCIE_MRX_GTX_C_N13
PCIE_MRX_GTX_C_P14
PCIE_MRX_GTX_C_N14
PCIE_MRX_GTX_C_P15
PCIE_MRX_GTX_C_N15
NB8M Power sequence request
3.3V-->1.8V-->1.2V
G72M Power sequence request
3.3V -->2.5V -->1.8V-->1.2V
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Quanta Computer Inc.
VGA(NB8M-GS)(1 of 4)
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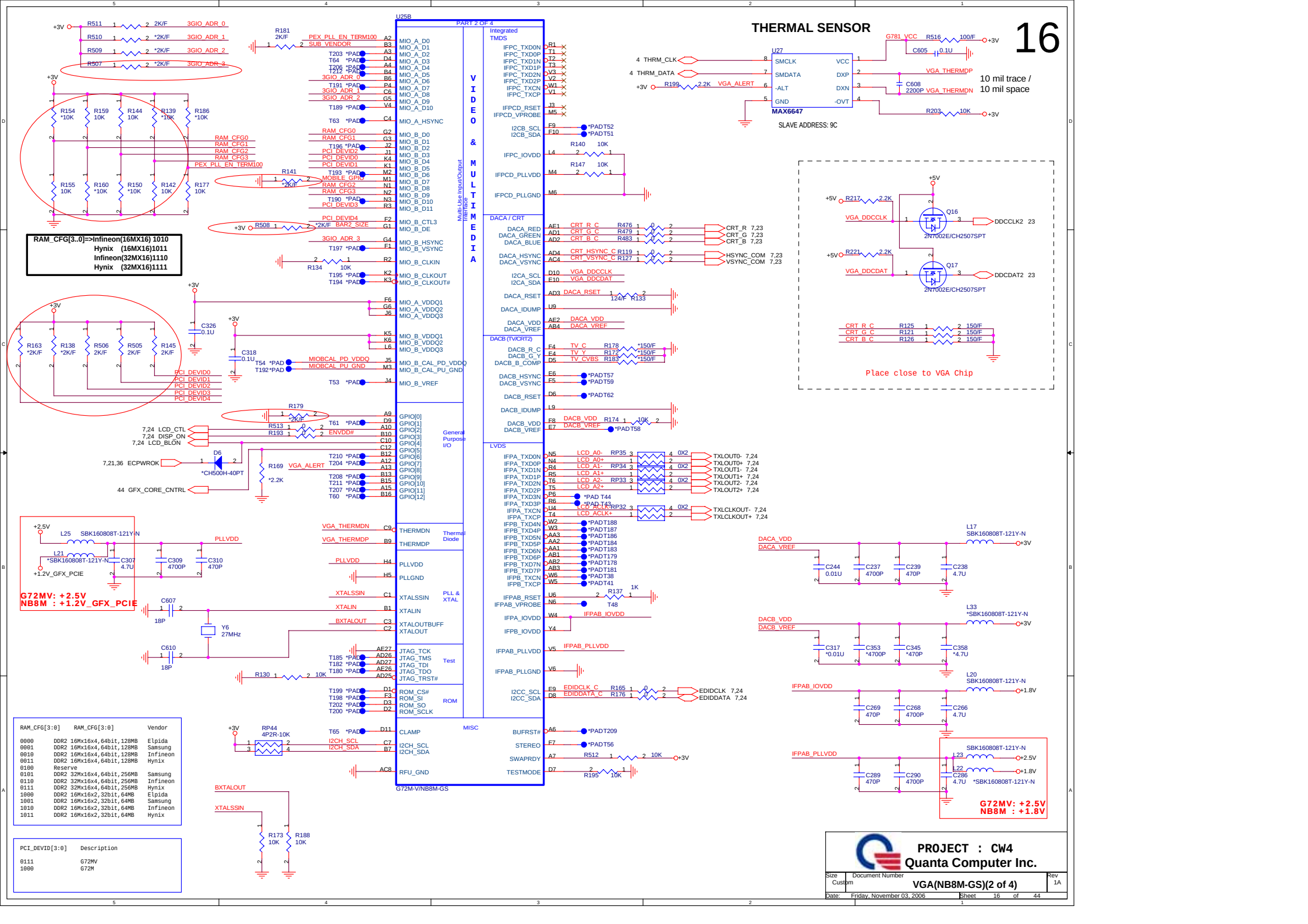
THERMAL SENSOR
16
U25B
PART 2 OF 4
VIDEO & MULTIMEDIA
Multi-Use Input/Output Interface
Integrated TMDS
DACA / CRT
DACB (TV/CRT2)
LVDS
General Purpose I/O
Thermal Diode
PLL & XTAL
Test
ROM
MISC
G72M-V/NB8M-GS
U27
MAX6647
SMCLK
SMDATA
-ALT
GND
VCC
DXP
DXN
-OVT
SLAVE ADDRESS: 9C
10 mil trace /
10 mil space
Place close to VGA Chip
RAM_CFG[3..0]=>Infineon(16MX16) 1010
Hynix (16MX16)1011
Infineon(32MX16)1110
Hynix (32MX16)1111
RAM_CFG[3:0] RAM_CFG[3:0] Vendor
0000 DDR2 16Mx16x4,64bit,128MB Elpida
0001 DDR2 16Mx16x4,64bit,128MB Samsung
0010 DDR2 16Mx16x4,64bit,128MB Infineon
0011 DDR2 16Mx16x4,64bit,128MB Hynix
0100 Reserve
0101 DDR2 32Mx16x4,64bit,256MB Samsung
0110 DDR2 32Mx16x4,64bit,256MB Infineon
0111 DDR2 32Mx16x4,64bit,256MB Hynix
1000 DDR2 16Mx16x2,32bit,64MB Elpida
1001 DDR2 16Mx16x2,32bit,64MB Samsung
1010 DDR2 16Mx16x2,32bit,64MB Infineon
1011 DDR2 16Mx16x2,32bit,64MB Hynix
PCI_DEVID[3:0] Description
0111 G72MV
1000 G72M
G72MV: +2.5V
NB8M : +1.2V_GFX_PCIE
G72MV: +2.5V
NB8M : +1.8V
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VGA(NB8M-GS)(2 of 4)
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FB_CMD[0..26] 18
FBD[0..63] 18
FBDQM[0..7] 18
FBDQS[0..7] 18
FBDQS#[0..7] 18

U25C

Part 3 of 4

MEMORY INTERFACE

FBD0	A26	FB_DQ0	FB_CMD0	G27	FB_CMD0
FBD1	C24	FB_DQ1	FB_CMD1	D25	FB_CMD1
FBD2	B24	FB_DQ2	FB_CMD2	F26	FB_CMD2
FBD3	A24	FB_DQ3	FB_CMD3	F25	FB_CMD3
FBD4	C22	FB_DQ4	FB_CMD4	G25	FB_CMD4
FBD5	A25	FB_DQ5	FB_CMD5	J25	FB_CMD5
FBD6	B25	FB_DQ6	FB_CMD6	J27	FB_CMD6
FBD7	D23	FB_DQ7	FB_CMD7	M26	FB_CMD7
FBD8	G22	FB_DQ8	FB_CMD8	C27	FB_CMD8
FBD9	J23	FB_DQ9	FB_CMD9	C25	FB_CMD9
FBD10	E24	FB_DQ10	FB_CMD10	D24	FB_CMD10
FBD11	F23	FB_DQ11	FB_CMD11	N27	FB_CMD11
FBD12	J24	FB_DQ12	FB_CMD12	G24	FB_CMD12
FBD13	F24	FB_DQ13	FB_CMD13	J26	FB_CMD13
FBD14	G23	FB_DQ14	FB_CMD14	M27	FB_CMD14
FBD15	H24	FB_DQ15	FB_CMD15	C26	FB_CMD15
FBD16	D16	FB_DQ16	FB_CMD16	M25	FB_CMD16
FBD17	E16	FB_DQ17	FB_CMD17	D26	FB_CMD17
FBD18	D17	FB_DQ18	FB_CMD18	D27	FB_CMD18
FBD19	F18	FB_DQ19	FB_CMD19	K26	FB_CMD19
FBD20	E19	FB_DQ20	FB_CMD20	K25	FB_CMD20
FBD21	E18	FB_DQ21	FB_CMD21	K24	FB_CMD21
FBD22	D20	FB_DQ22	FB_CMD22	F27	FB_CMD22
FBD23	D19	FB_DQ23	FB_CMD23	K27	FB_CMD23
FBD24	A18	FB_DQ24	FB_CMD24	G26	FB_CMD24
FBD25	B18	FB_DQ25	FB_CMD25	B27	FB_CMD25
FBD26	A19	FB_DQ26	FB_CMD26	N24	FB_CMD26
FBD27	B19	FB_DQ27			
FBD28	D18	FB_DQ28			
FBD29	C19	FB_DQ29			
FBD30	C16	FB_DQ30			
FBD31	C18	FB_DQ31			
FBD32	N26	FB_DQ32			
FBD33	N25	FB_DQ33			
FBD34	R25	FB_DQ34			
FBD35	R26	FB_DQ35			
FBD36	R27	FB_DQ36			
FBD37	T25	FB_DQ37			
FBD38	T27	FB_DQ38			
FBD39	T26	FB_DQ39			
FBD40	AB23	FB_DQ40			
FBD41	Y24	FB_DQ41			
FBD42	AB24	FB_DQ42			
FBD43	AB22	FB_DQ43			
FBD44	AC24	FB_DQ44			
FBD45	AC22	FB_DQ45			
FBD46	AA23	FB_DQ46			
FBD47	AA22	FB_DQ47			
FBD48	T24	FB_DQ48			
FBD49	T23	FB_DQ49			
FBD50	R24	FB_DQ50			
FBD51	R23	FB_DQ51			
FBD52	R22	FB_DQ52			
FBD53	T22	FB_DQ53			
FBD54	N23	FB_DQ54			
FBD55	P24	FB_DQ55			
FBD56	AA24	FB_DQ56			
FBD57	AA27	FB_DQ57			
FBD58	AA26	FB_DQ58			
FBD59	AB25	FB_DQ59			
FBD60	AB26	FB_DQ60			
FBD61	AB27	FB_DQ61			
FBD62	AA25	FB_DQ62			
FBD63	W25	FB_DQ63			

*PADT49

*PADT47

NB8M A VER:
NC

FB_DQM0	D21	FBDQM0
FB_DQM1	F22	FBDQM1
FB_DQM2	F20	FBDQM2
FB_DQM3	A21	FBDQM3
FB_DQM4	V27	FBDQM4
FB_DQM5	W22	FBDQM5
FB_DQM6	V22	FBDQM6
FB_DQM7	V24	FBDQM7

read strobe

FB_DQS_RN0	A22	FBDQS#0
FB_DQS_RN1	E22	FBDQS#1
FB_DQS_RN2	F21	FBDQS#2
FB_DQS_RN3	B21	FBDQS#3
FB_DQS_RN4	V26	FBDQS#4
FB_DQS_RN5	W23	FBDQS#5
FB_DQS_RN6	V23	FBDQS#6
FB_DQS_RN7	W27	FBDQS#7

write strobe

FB_DQS_WP0	B22	FBDQS0
FB_DQS_WP1	D22	FBDQS1
FB_DQS_WP2	F21	FBDQS2
FB_DQS_WP3	C21	FBDQS3
FB_DQS_WP4	V25	FBDQS4
FB_DQS_WP5	W24	FBDQS5
FB_DQS_WP6	U24	FBDQS6
FB_DQS_WP7	W26	FBDQS7

18 FB_CLK0	L24	FB_CLK0
18 FB_CLK0#	K23	FB_CLK0#
18 FB_CLK1	M22	FB_CLK1
18 FB_CLK1#	N22	FB_CLK1#
T45 *PAD	M23	FB_REFCLK
T50 *PAD	M24	FB_REFCLK#
	K22	FB_DEBUG
	A16	FB_VREF
+3V	F12	I2CS_SCL
	F11	I2CS_SDA
	D14	FB_PLLVDD
	D13	FB_PLLAVDD
	C15	FB_PLLAGND

FBVTT_01	E15	
FBVTT_02	F15	
FBVTT_03	F16	
FBVTT_04	J17	
FBVTT_05	J18	
FBVTT_06	L19	
FBVTT_07	N19	
FBVTT_08	R19	
FBVTT_09	U19	
FBVTT_10	W19	
FBVDDQ_01	F17	
FBVDDQ_02	F19	
FBVDDQ_03	J19	
FBVDDQ_04	M19	
FBVDDQ_05	T19	
FBVDDQ_06	J22	
FBVDDQ_07	L22	
FBVDDQ_08	P22	
FBVDDQ_09	U22	
FBVDDQ_10	Y22	
FBCAL_PD_VDDQ	D15	FBCAL_PD_VDDQ
FBCAL_PU_GND	E13	FBCAL_PU_GND
FBCAL_TERM_GND	H22	FBCAL_TERM_GND

G72M-V/NB8M-GS

U25D

Part 4 of 4

GND

B2	GND_01		GND_48	P14	
E2	GND_02		GND_49	R14	
H2	GND_03		GND_50	U14	
L2	GND_04		GND_51	W14	
P2	GND_05		GND_52	AC14	
U2	GND_06		GND_53	AD14	
Y2	GND_07		GND_54	N15	
AC2	GND_08		GND_55	P15	
AF2	GND_09		GND_56	R15	
AF3	GND_10		GND_57	AF15	
B5	GND_11		GND_58	N16	
E5	GND_12		GND_59	P16	
L5	GND_13		GND_60	R16	
P5	GND_14		GND_61	AD16	
U5	GND_15		GND_62	B17	
Y5	GND_16		GND_63	E17	
AC5	GND_17		GND_64	L17	
H6	GND_18		GND_65	P17	
AF6	GND_19		GND_66	U17	
B8	GND_20		GND_67	AD17	
E8	GND_21		GND_68	AF18	
AD8	GND_22		GND_69	K19	
K9	GND_23		GND_70	P19	
P9	GND_24		GND_71	V19	
V9	GND_25		GND_72	AD19	
AD9	GND_26		GND_73	B20	
AF9	GND_27		GND_74	E20	
B11	GND_28		GND_75	AD20	
E11	GND_29		GND_76	AF21	
			GND_77	B23	
L11	GND_31		GND_78	F23	
P11	GND_32		GND_79	H23	
U11	GND_33		GND_80	L23	
AD11	GND_34		GND_81	P23	
N12	GND_35		GND_82	U23	
P12	GND_36		GND_83	Y23	
R12	GND_37		GND_84	AC23	
AD12	GND_38		GND_85	AF24	
AF12	GND_39		GND_86	B26	
N13	GND_40		GND_87	E26	
P13	GND_41		GND_88	H26	
R13	GND_42		GND_89	L26	
B14	GND_43		GND_90	P26	
E14	GND_44		GND_91	U26	
J14	GND_45		GND_92	Y26	
L14	GND_46		GND_93	AC26	
N14	GND_47		GND_94	AF26	

G72M-V/NB8M-GS

+1.8V
Rt R515 1K/F
FBVREF
Rb R514 1K/F
C602 0.1U

FBVREF = FBVDDQ * Rb/(Rt + Rb).
VREF = 0.5 * FBVDDQ.
DDR: 0.9V = 1.8V * 1K/(1K + 1K).

NB8M A VER:
STUFF

G72MV: NC
NB8M : +1.2V_GFX_PCIE

G72MV: NC
NB8M : 2.2K

FB_CMD12 R149 FB_DEBUG
*0_4
FBVREF
R180 2.2K/F
R184 2.2K/F
L60 *SBK160808T-121Y-N
FBA_PLLVDD
+1.2V_GFX_PCIE
L59 0
FB_PLLAVDD
C604 4.7U
C331 1U
C603 0.01U

+1.8V
R170 40/F
R158 *40/F
R162 30/F

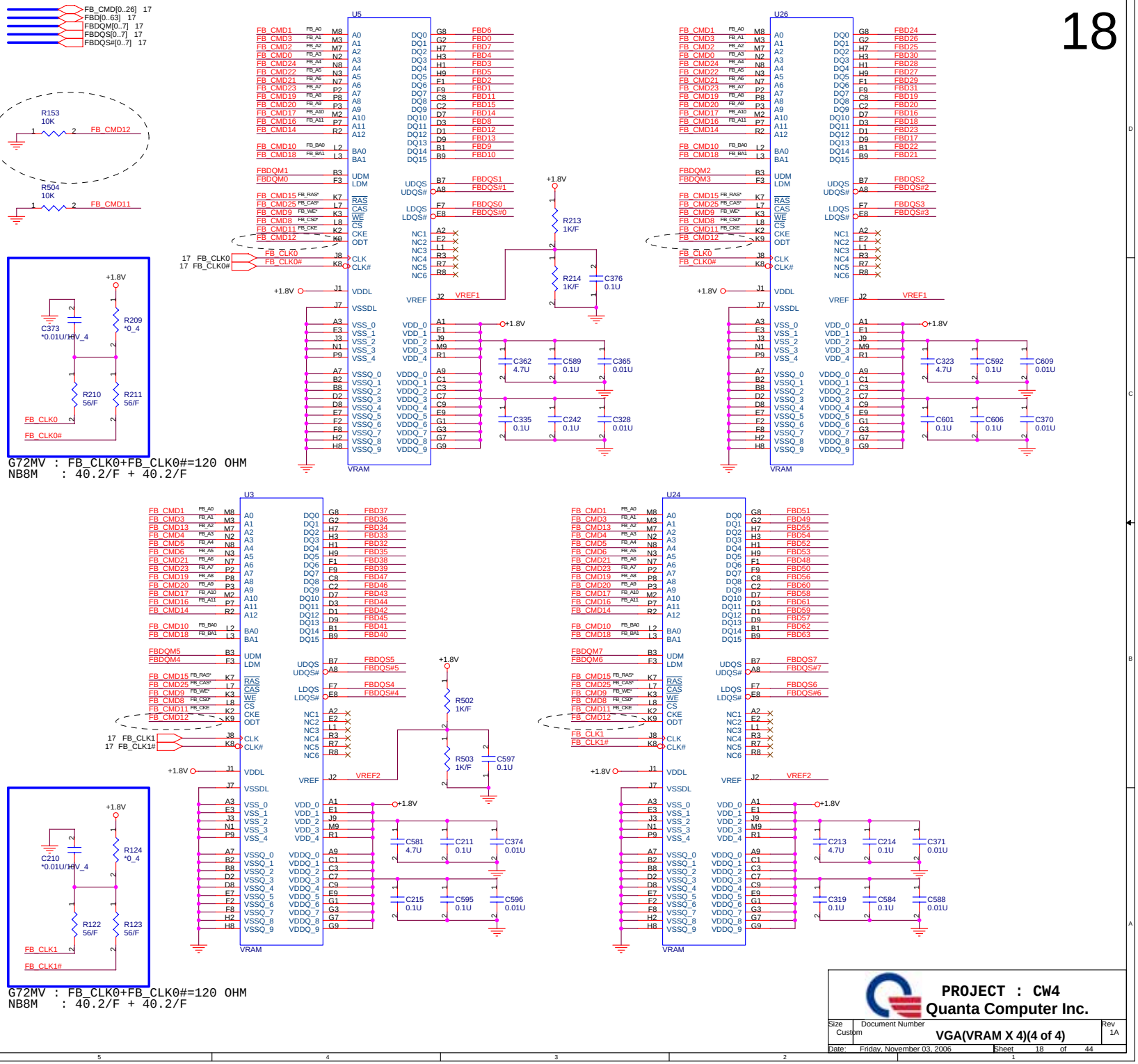
PLACE BELOW GPU

+1.8V
C256 4700P
C277 0.022U
C298 0.1U
C594 4700P
C324 0.1U
C325 4.7U
C302 1U
C275 4700P
C278 0.022U
C270 0.1U
C316 4700P
C313 0.022U
C334 0.1U
C360 4.7U
C312 4700P
C294 0.022U
C593 0.1U
C336 0.022U
C321 0.1U
C284 1U

PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VGA(NB8M-GS)(3 of 4)	1A

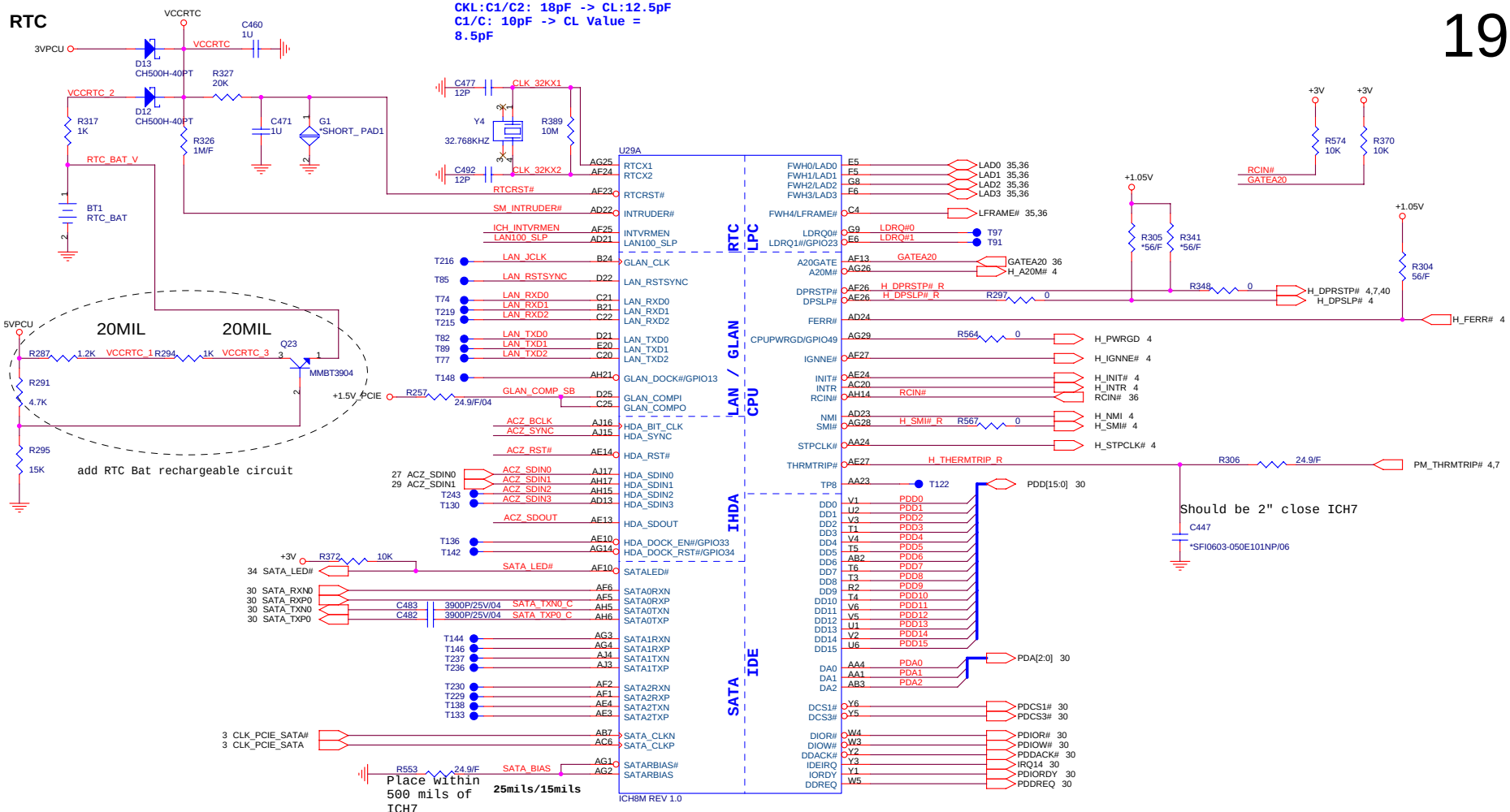
Date: Friday, November 03, 2006 Sheet 17 of 44



PROJECT : CW4			
Quanta Computer Inc.			
Size: Custom	Document Number: VGA(VRAM X 4)(4 of 4)		Rev: 1A
Date: Friday, November 03, 2006	Sheet 18 of 44		

RTC

CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF



SB Strap

ICH8-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

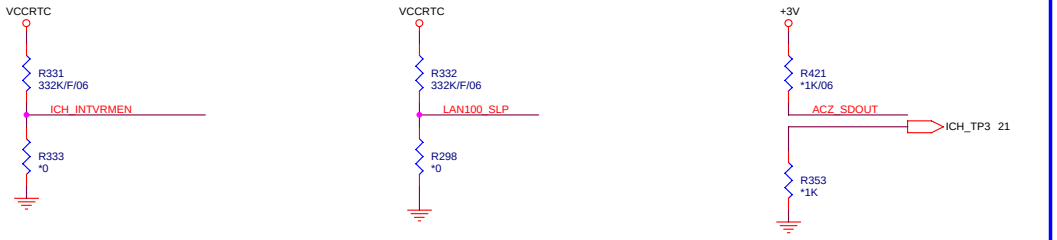
INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

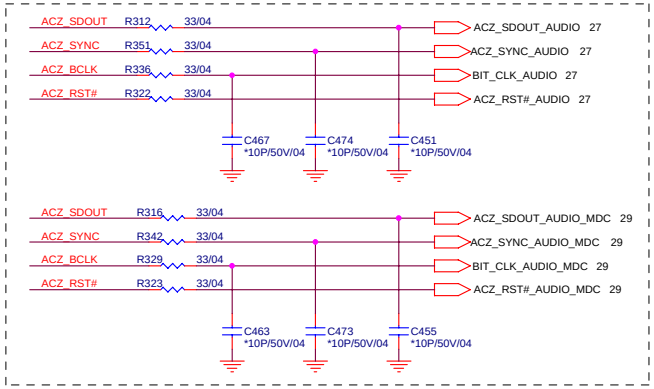
ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1





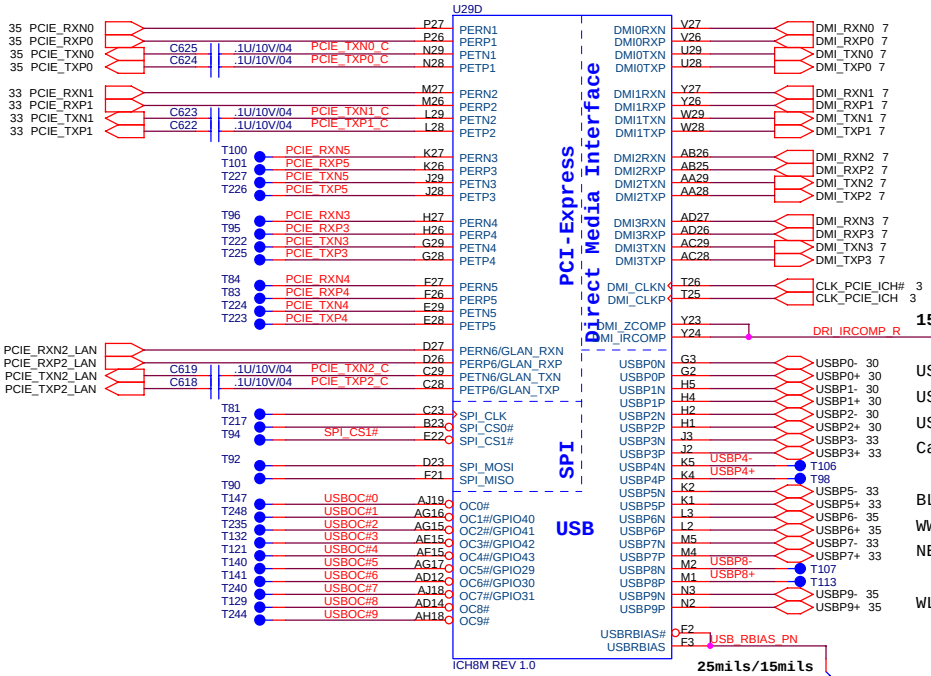
PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH8-M HOST (1 of 4)	1A
Date: Friday, November 03, 2006	Sheet 19 of 44	

MINI CARD PCI-E

EXPRESS CARD (NEW CARD)

PCIE-LAN



USB Connector

USB Connector

USB Connector

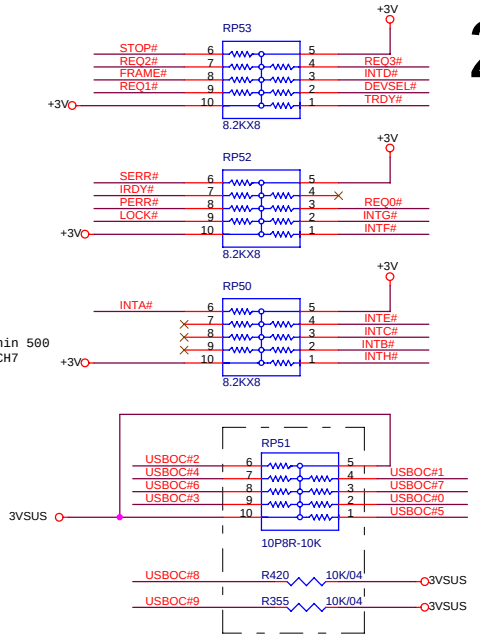
Carama USB

BLUETOOTH

WWAN

NEW CARD

WLAN



A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

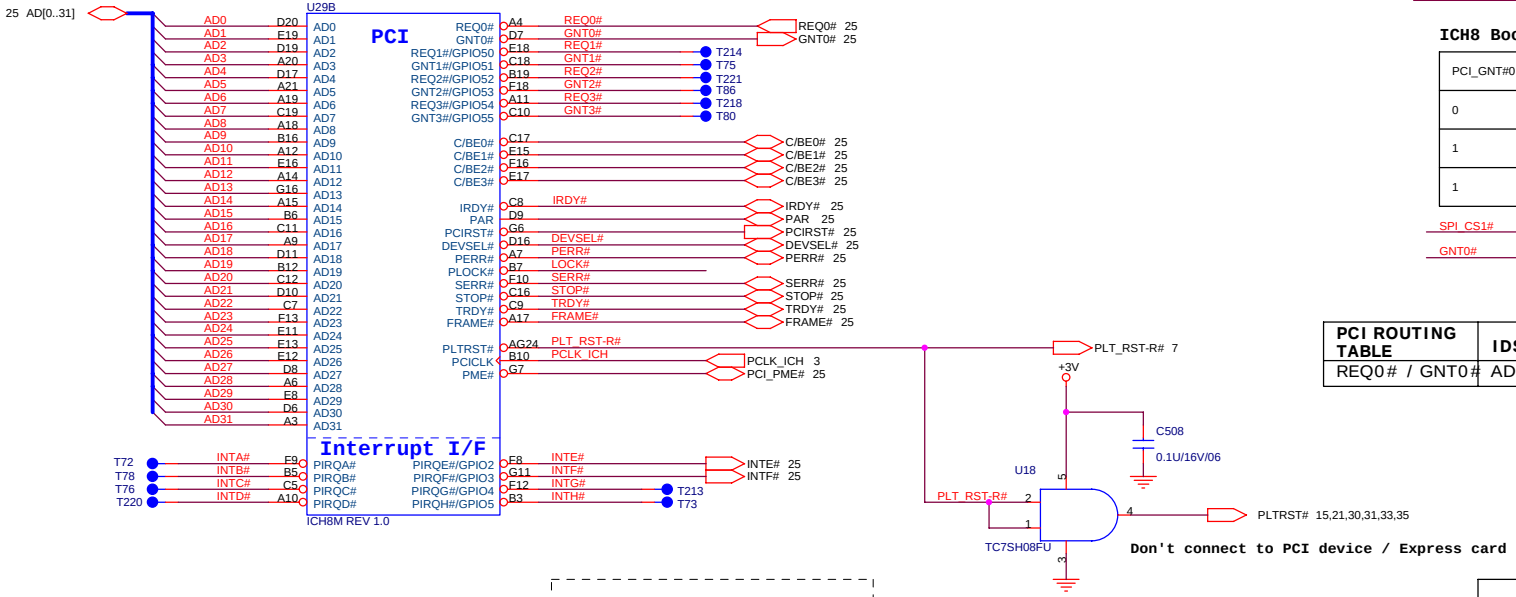
GNT3# R254 *1K

ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC

SPI_CS1# R263 *1K

GNT0# R255 *1K

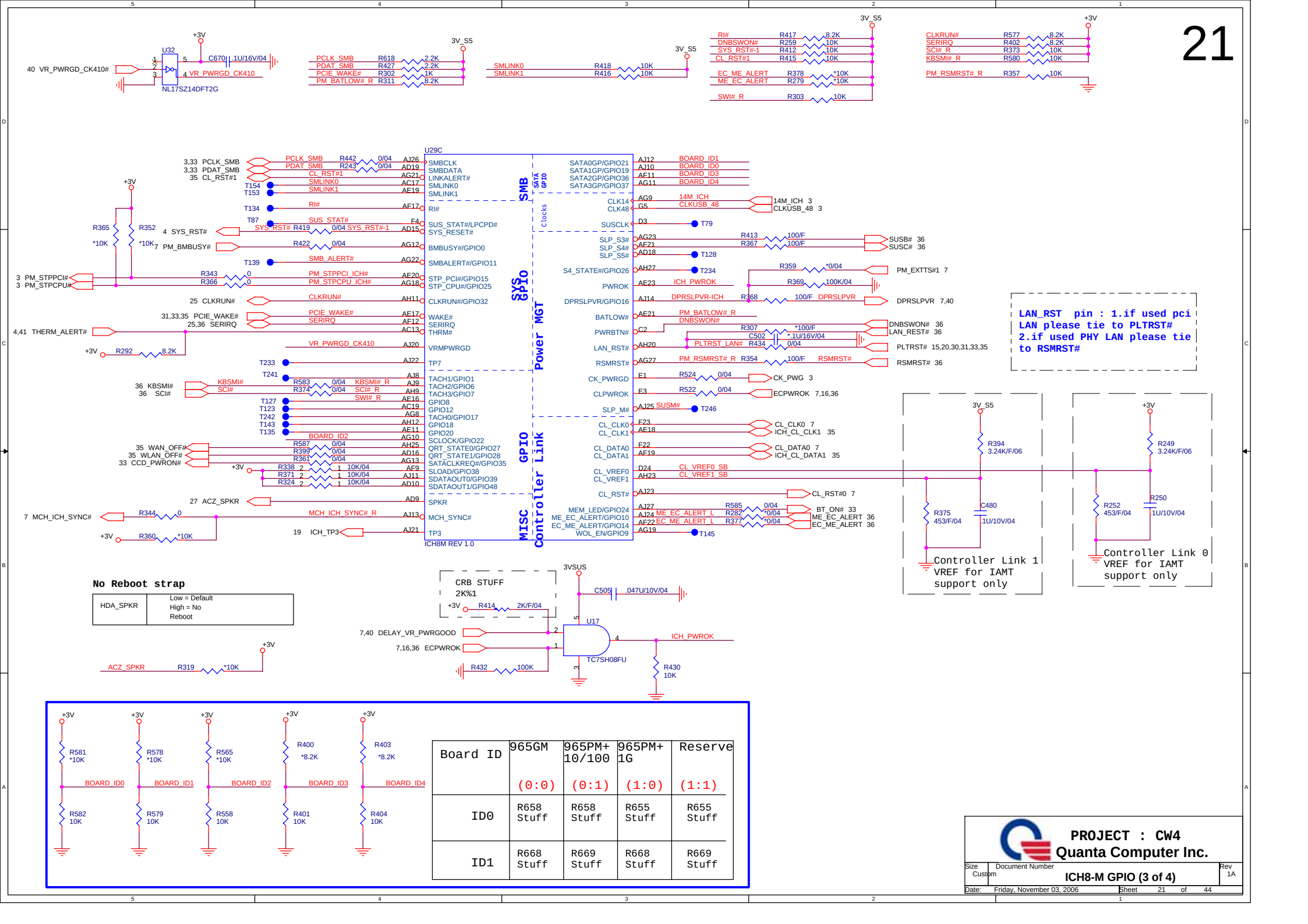


Don't connect to PCI device / Express card

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD25	INTE#,INTF#	RICOH832

PCLK_ICH R256 *0 C400 *33P/50V

for EMI request

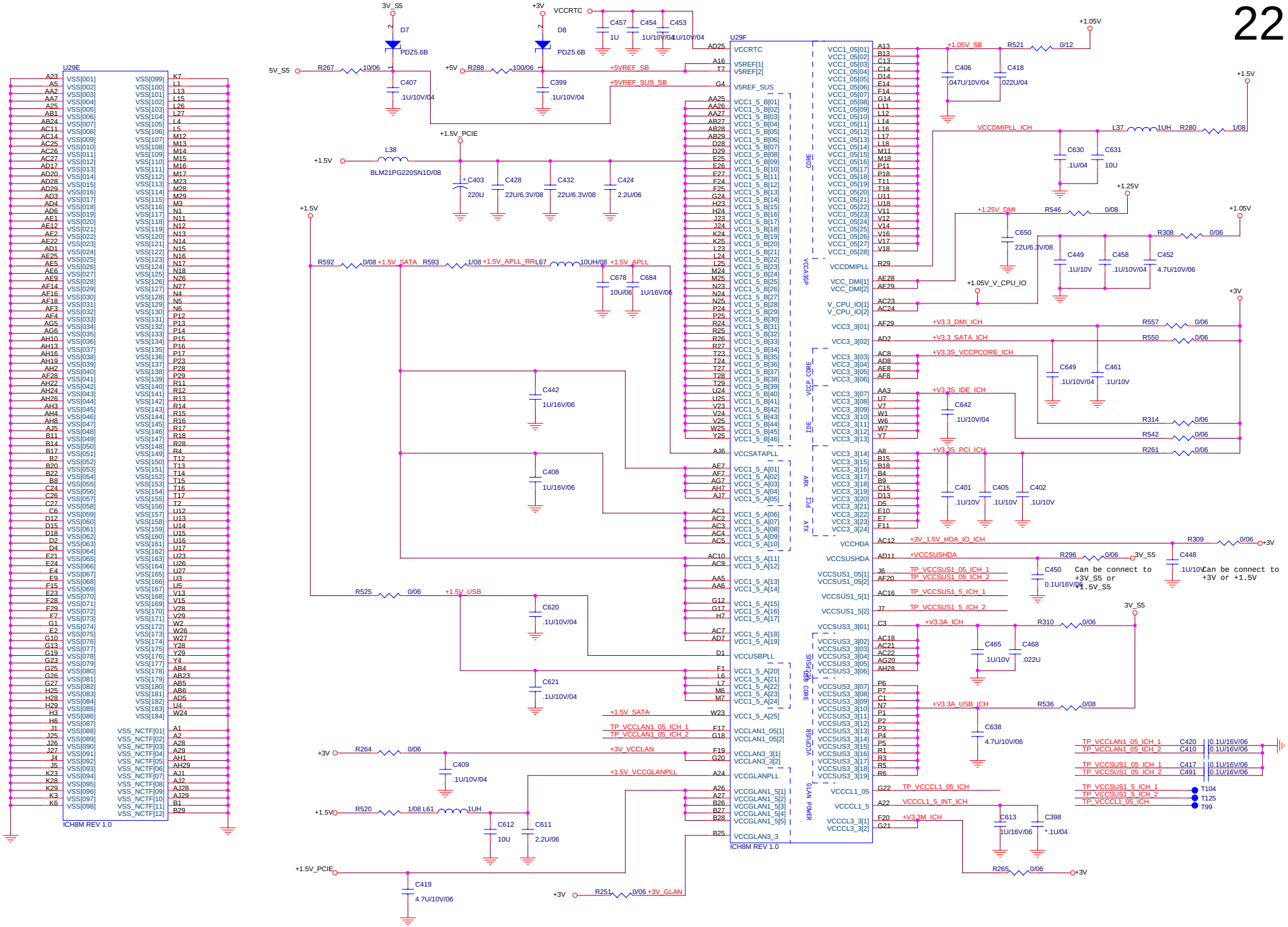


Board ID	965GM (0:0)	965PM+ 10/100 (0:1)	965PM+ 1G (1:0)	Reserve (1:1)
ID0	R658 Stuff	R658 Stuff	R655 Stuff	R655 Stuff
ID1	R668 Stuff	R669 Stuff	R668 Stuff	R669 Stuff

PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH8-M GPIO (3 of 4)	1A

Date: Friday, November 03, 2006 Sheet 21 of 44


U29E
ICH8M REV 1.0
U29F
ICH8M REV 1.0
3V_S5
D7
PDZ5.6B
D8
PDZ5.6B
VCCRTC
+3V
+5V
5V_S5
R267 10/06
R288 100/06
C407 .1U/10V/04
C399 .1U/10V/04
C457 1U
C454 .1U/10V/04
C453 .1U/10V/04
+5VREF_SB
+5VREF_SUS_SB
+1.5V_PCIE
+1.5V
L38
BLM21PG220SN1D/08
C403 220U
C428 22U/6.3V/08
C432 22U/6.3V/08
C424 2.2U/06
R592 0/08 +1.5V_SATA
R593 1/08 +1.5V_APLL_RR
L67 10UH/08 +1.5V_APLL
C678 10U/06
C684 1U/16V/06
C442 1U/16V/06
C408 1U/16V/06
R525 0/06 +1.5V_USB
C620 .1U/10V/04
C621 .1U/10V/04
+1.5V_SATA
TP_VCCLAN1_05_ICH_1
TP_VCCLAN1_05_ICH_2
+3V_VCCLAN
+1.5V_VCCGLANPLL
R264 0/06
C409 .1U/10V/04
R520 1/08 L61 1UH
C612 10U
C611 2.2U/06
C419 4.7U/10V/06
R251 0/06 +3V_GLAN
+1.05V
R521 0/12
+1.05V_SB
C406 .047U/10V/04
C418 .022U/04
VCCDMIPLL_ICH
L37 1UH
R280 1/08
C630 .1U/04
C631 10U
+1.25V
+1.25V_DMI
R546 0/08
C650 22U/6.3V/08
R308 0/06
C449 .1U/10V
C458 .1U/10V/04
C452 4.7U/10V/06
+1.05V_V_CPU_IO
+3V
+V3.3_DMI_ICH
R557 0/06
+V3.3_SATA_ICH
R550 0/06
+V3.3S_VCCPCORE_ICH
C649 .1U/10V/04
C461 .1U/10V
+V3.3S_IDE_ICH
C642 .1U/10V/04
R314 0/06
R542 0/06
+V3.3S_PCI_ICH
R261 0/06
C401 .1U/10V
C405 .1U/10V
C402 .1U/10V
+1.5V_1.5V_HDA_IO_ICH
R309 0/06
+VCCSUSHDA
R296 0/06
3V_S5
C448 .1U/10V
C450 0.1U/16V/06
Can be connect to +3V_S5 or +1.5V_S5
Can be connect to +3V or +1.5V
+3.3A_ICH
R310 0/06
C465 .1U/10V
C468 .022U
+V3.3A_USB_ICH
R536 0/08
C638 4.7U/10V/06
TP_VCCLAN1_05_ICH_1 C420 0.1U/16V/06
TP_VCCLAN1_05_ICH_2 C410 0.1U/16V/06
TP_VCCSUS1_05_ICH_1 C417 0.1U/16V/06
TP_VCCSUS1_05_ICH_2 C491 0.1U/16V/06
TP_VCCSUS1_5_ICH_1 T104
TP_VCCSUS1_5_ICH_2 T125
TP_VCCCL1_05_ICH T99
TP_VCCCL1_05_ICH
VCCCL1_5_INT_ICH
+V3.3M_ICH
C613 1U/16V/06
C398 *.1U/04
R265 0/06
PROJECT : CW4
Quanta Computer Inc.
Size Custom
Document Number
ICH8-M GPIO (3 of 4)
Rev 1A
Date: Friday, November 03, 2006
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CRT PORT

+5V
D2
CRTVDD1
CH500H-40PT
F1
POLY_SWITCH_1.1A
CRTVDD2
L1
BLM18PG121SN
CRTVDD_5V
CRT_GND
C24
*0.1U
CN11
CRT_CONN
T159

7,16 CRT_R
7,16 CRT_G
7,16 CRT_B
L4 BLM18BA470SN1 CRT_R_1
L3 BLM18BA470SN1 CRT_G_1
L2 BLM18BA470SN1 CRT_B_1
R18 150/F
R17 150/F
R16 150/F
C39 5.6P
C35 5.6P
C31 5.6P
C30 5.6P
C34 5.6P
C38 5.6P

R7 0
R37 0
CRT_GND

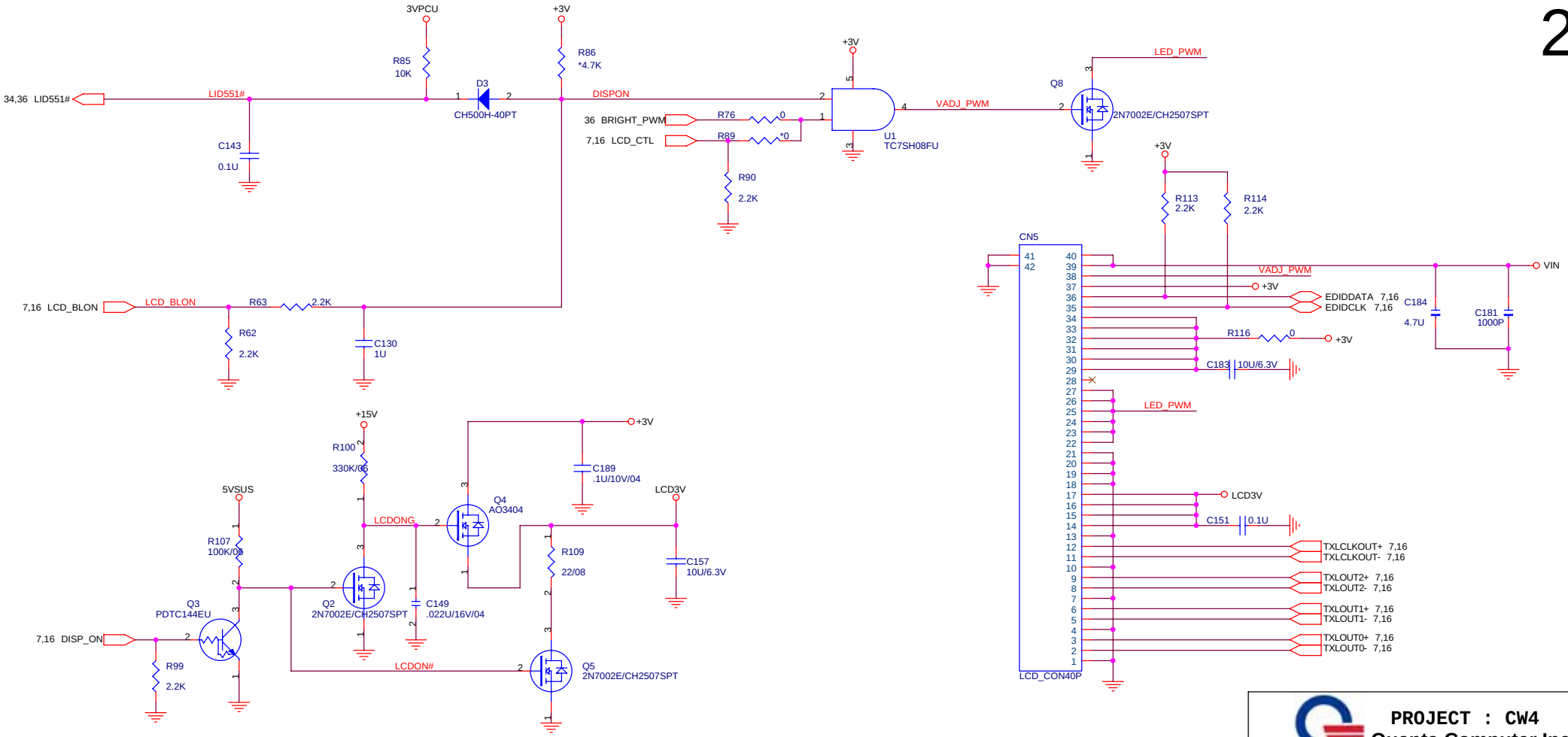
+2.5V
R468 *2.2K
Q36 *CH2507SPT
7 DDCCLK
R464 2.2K
DDCCLK2
L50 HB-1T1608-121JT
DDCCLK_1
16 DDCCLK2

CRTVDD_5V
AHCT1G125DCH
C23 0.1U
U20
U21
7,16 VSYNC_COM
7,16 HSYNC_COM
CRTVS_VGA
CRTHS_VGA
L51 HB-1T1608-121JT
L52 HB-1T1608-121JT
CRT_VS_1
CRT_HS_1

16 DDCDAT2
+2.5V
R473 *2.2K
Q37 *CH2507SPT
7 DDCDATA
DDCDAT2
L53 HB-1T1608-121JT
DDCDAT_1
R474 2.2K
C523 *33P
C530 *33P
C531 *33P
C535 *33P

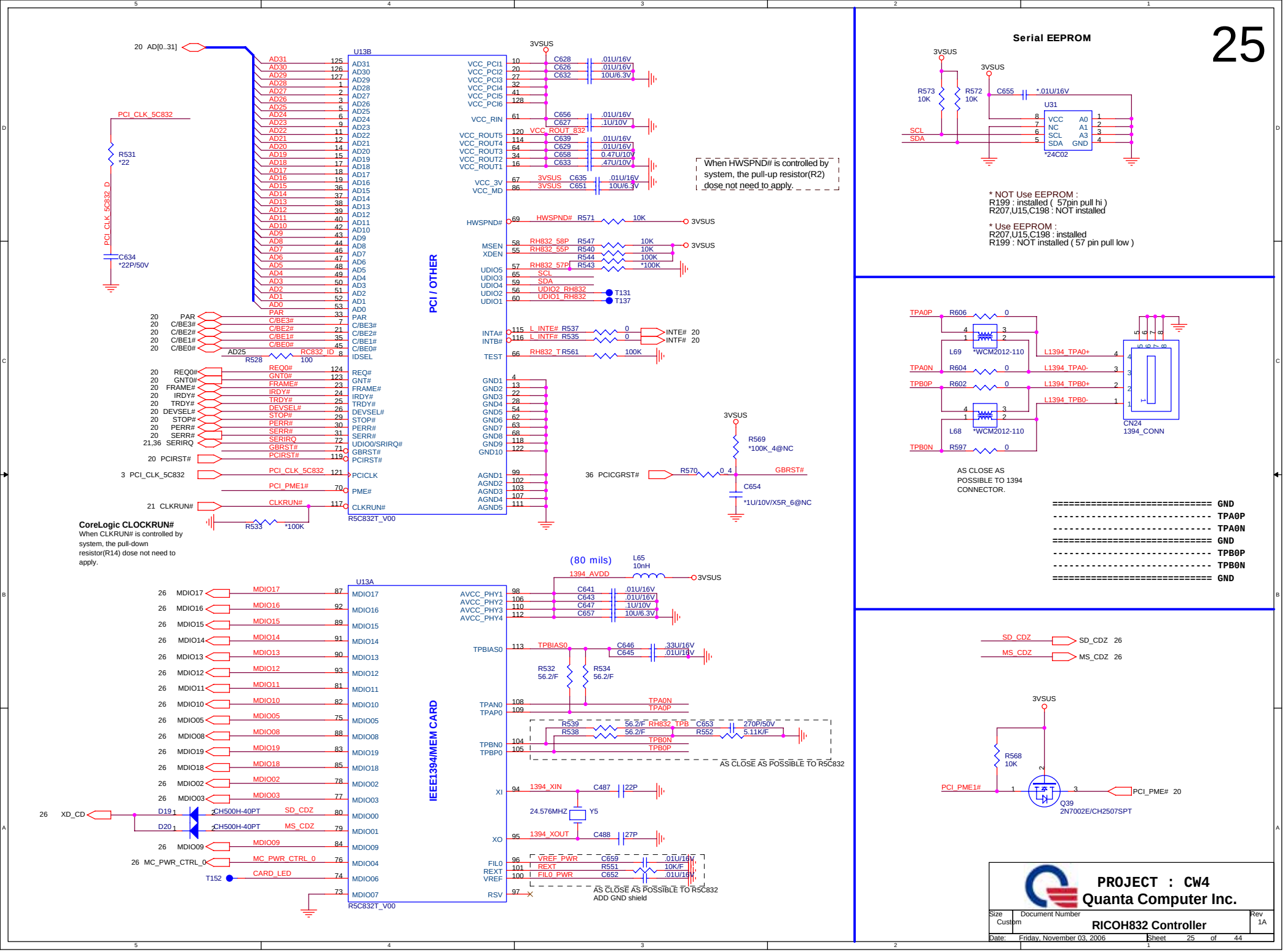
PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT CON	1A
Date: Friday, November 03, 2006	Sheet 23 of 44	



PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD & LID CON	1A
Date: Friday, November 03, 2006	Sheet 24 of 44	



Serial EEPROM

* NOT Use EEPROM :
R199 : installed (57pin pull hi)
R207,U15,C198 : NOT installed

* Use EEPROM :
R207,U15,C198 : installed
R199 : NOT installed (57 pin pull low)

AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.

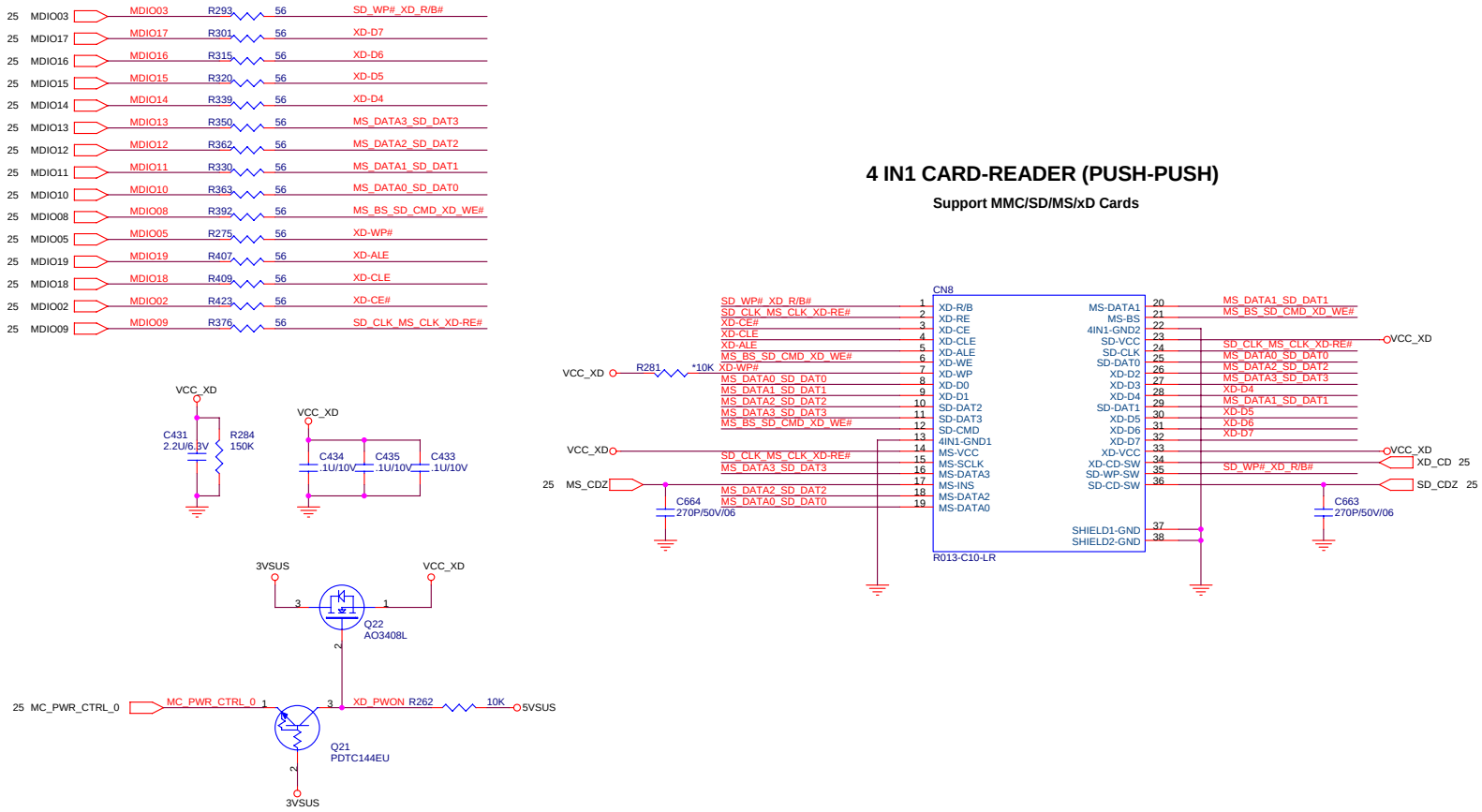
```
============================== GND
------------------------------ TPA0P
------------------------------ TPA0N
============================== GND
------------------------------ TPB0P
------------------------------ TPB0N
============================== GND
```


PROJECT : CW4
Quanta Computer Inc.

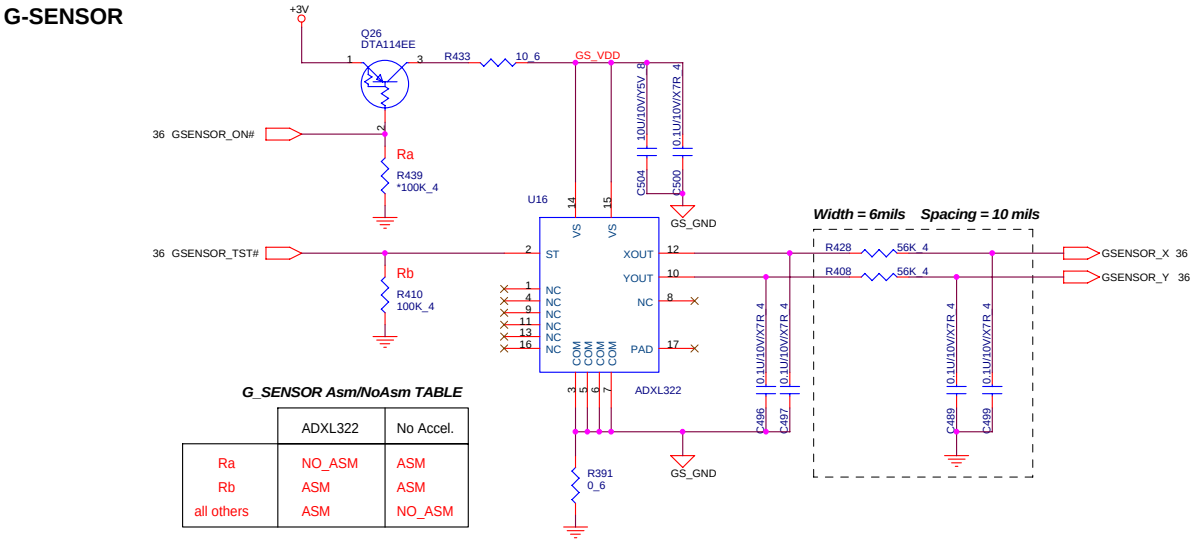
Size	Document Number	Rev
Custom	RICOH832 Controller	1A
Date: Friday, November 03, 2006	Sheet 25 of 44	

4 IN1 CARD-READER (PUSH-PUSH)

Support MMC/SD/MS/xD Cards



G-SENSOR

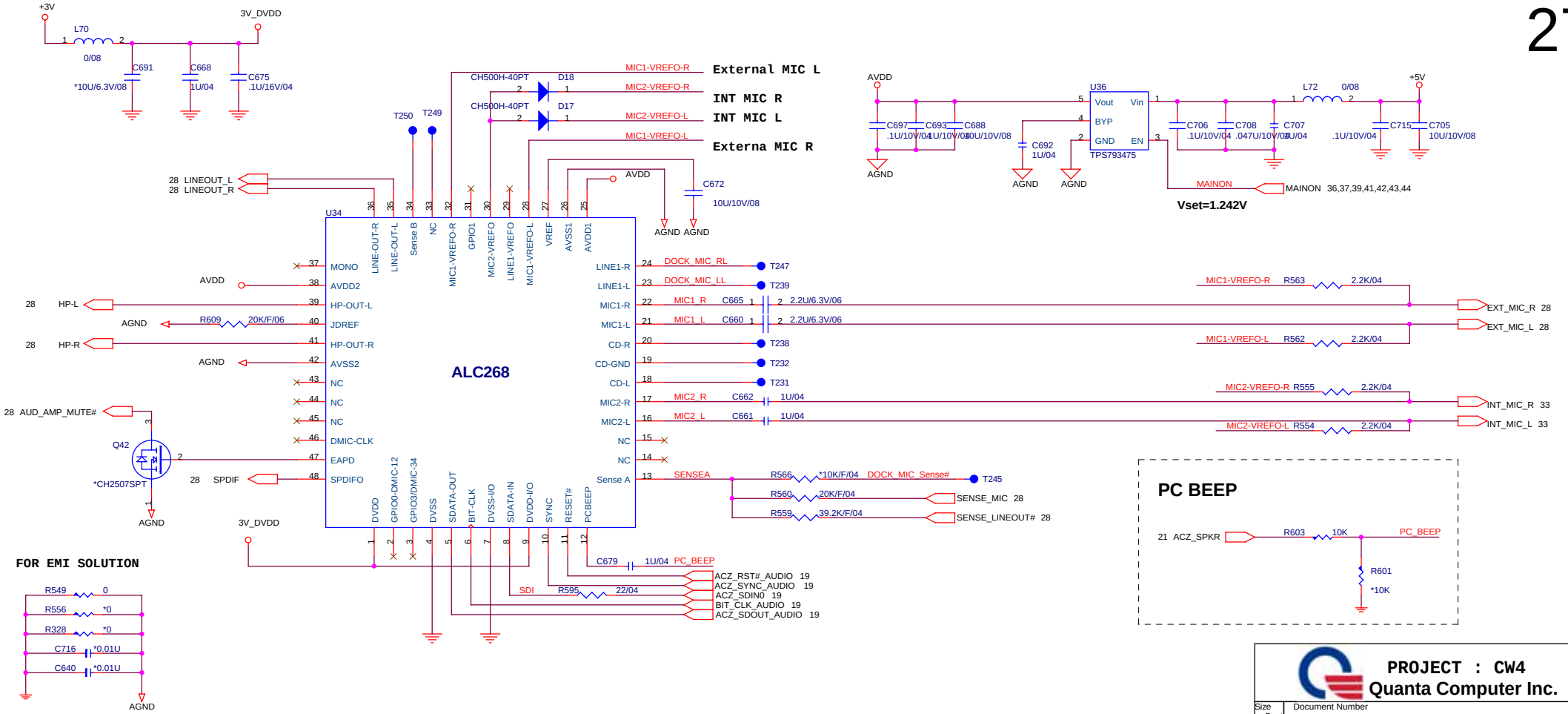


G_SENSOR Asm/NoAsm TABLE

	ADXL322	No Accel.
Ra	NO_ASM	ASM
Rb	ASM	ASM
all others	ASM	NO_ASM

PROJECT : CW4
Quanta Computer Inc.

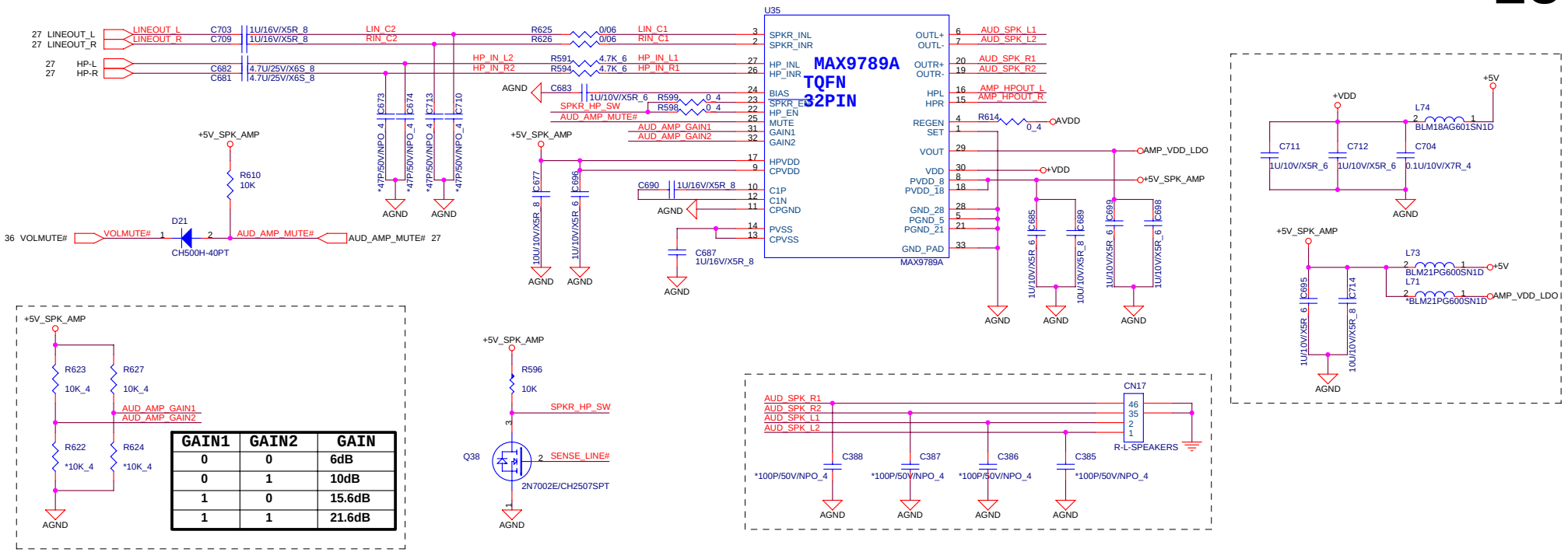
Size	Document Number	Rev
Custom	CARD-READER & G-SENSOR	1A
Date: Friday, November 03, 2006	Sheet 26 of 44	



PROJECT : CW4
Quanta Computer Inc.

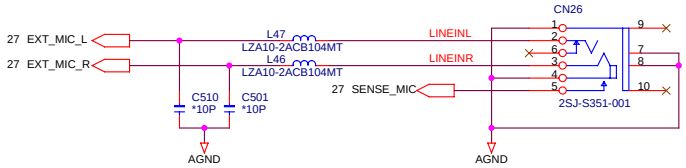
Size	Document Number	Rev
Custom	AZALIA ALC268	1A
Date: Friday, November 03, 2006	Sheet 27 of 44	

INTERNAL SPEAKER AMPLIFIER

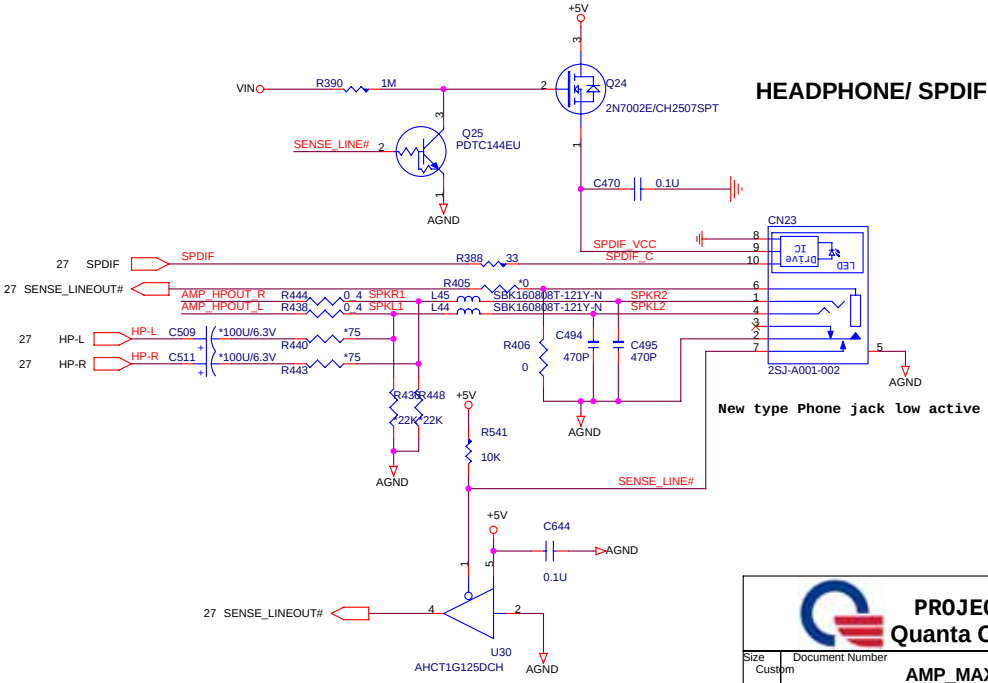


GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

MIC-IN JACK



HEADPHONE/ SPDIF OUT

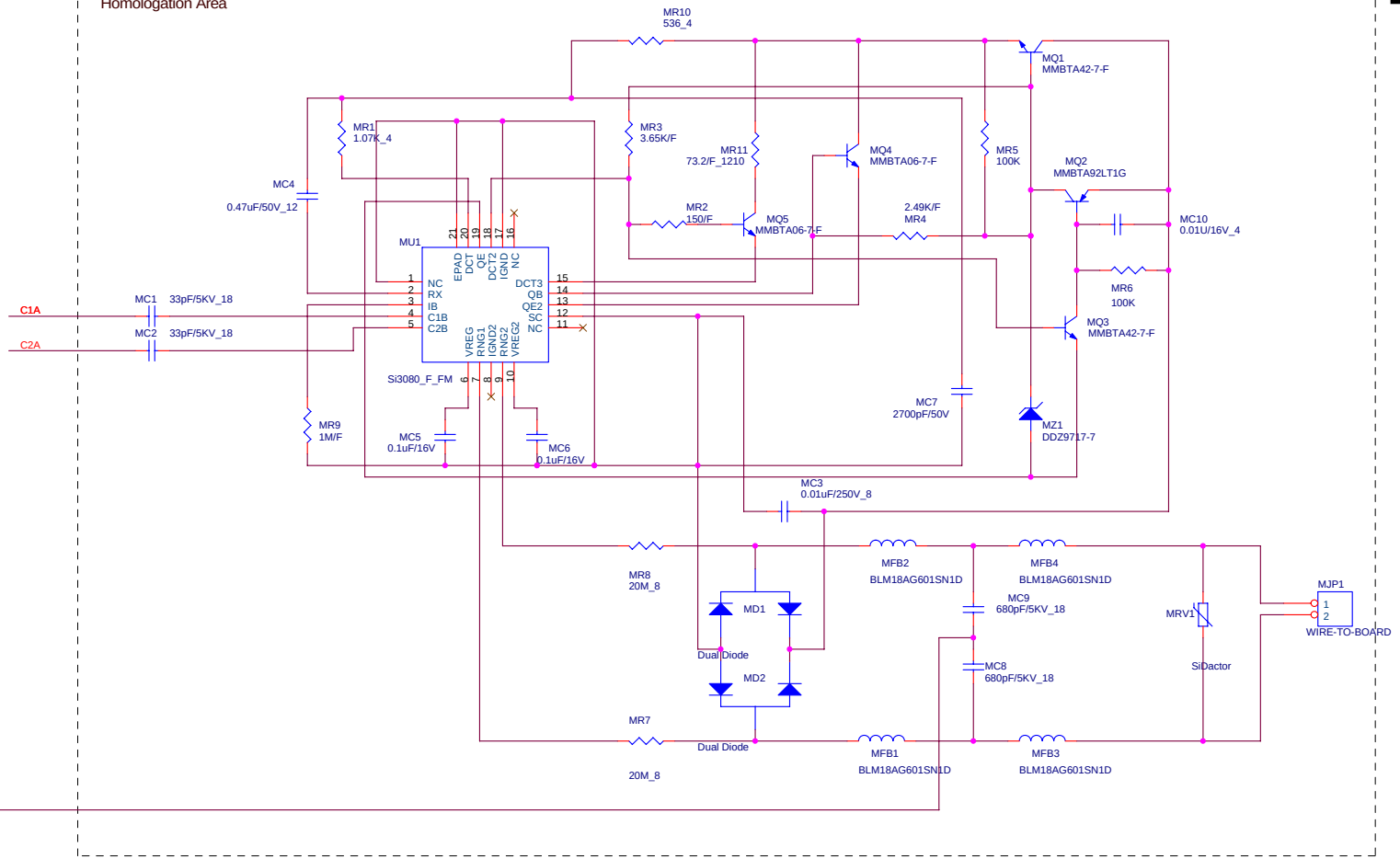


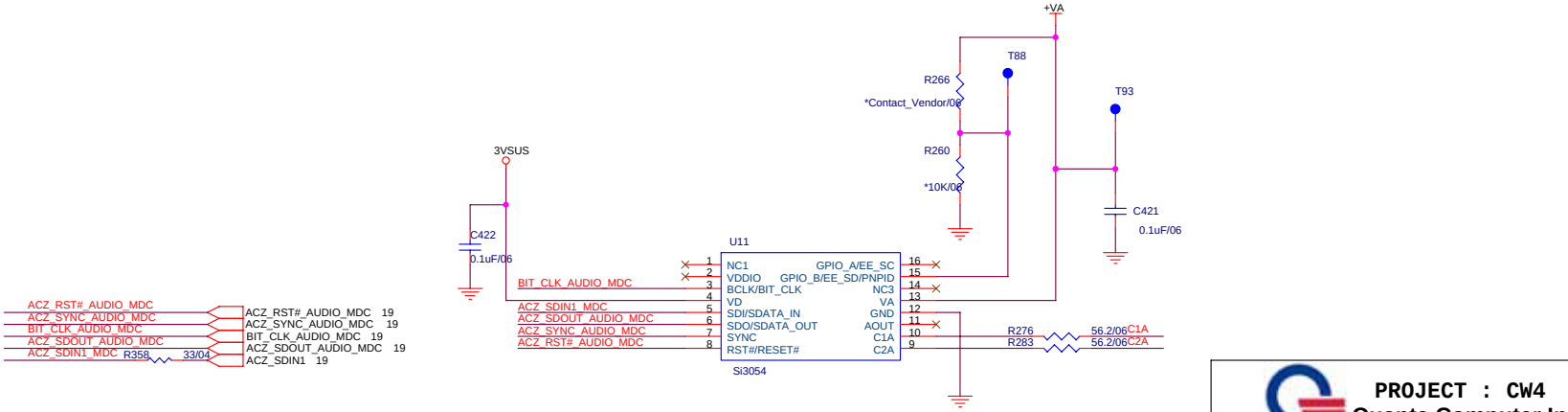
PROJECT : CW4 Quanta Computer Inc.		
Size: Custom	Document Number: AMP_MAX9789A & JACK	Rev: 1A
Date: Friday, November 03, 2006	Sheet 28 of 44	

MODEM

No Ground Plane In DAA Section

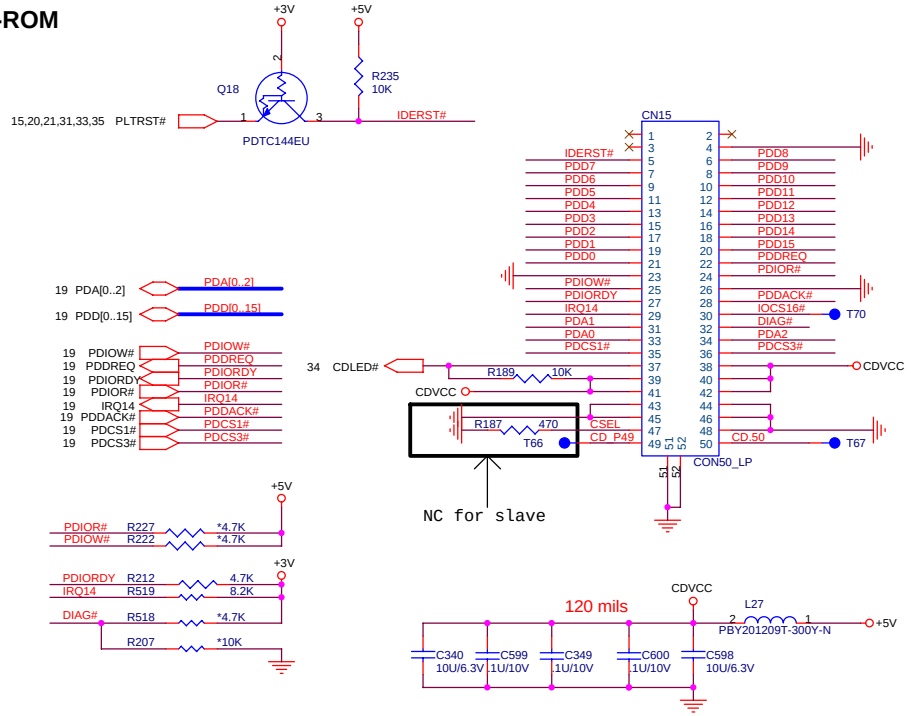
Homologation Area



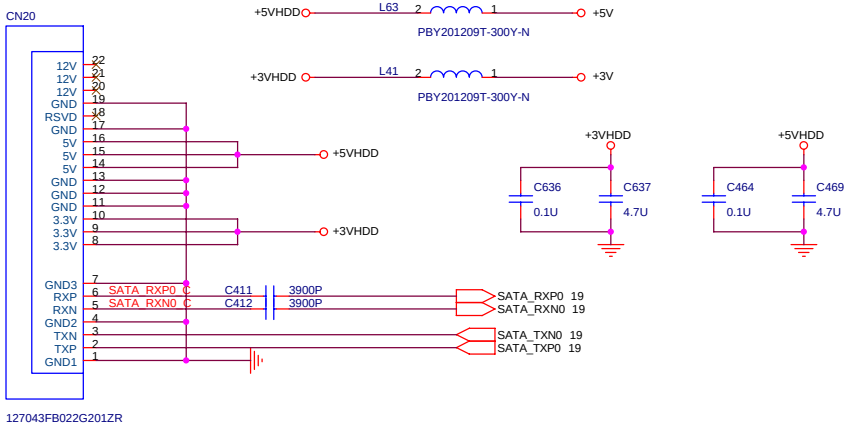


PROJECT : CW4		
Quanta Computer Inc.		
Size: Custom	Document Number: MODEM(SI3054+SI3080)	Rev: 1A
Date: Friday, November 03, 2006	Sheet 29 of 44	

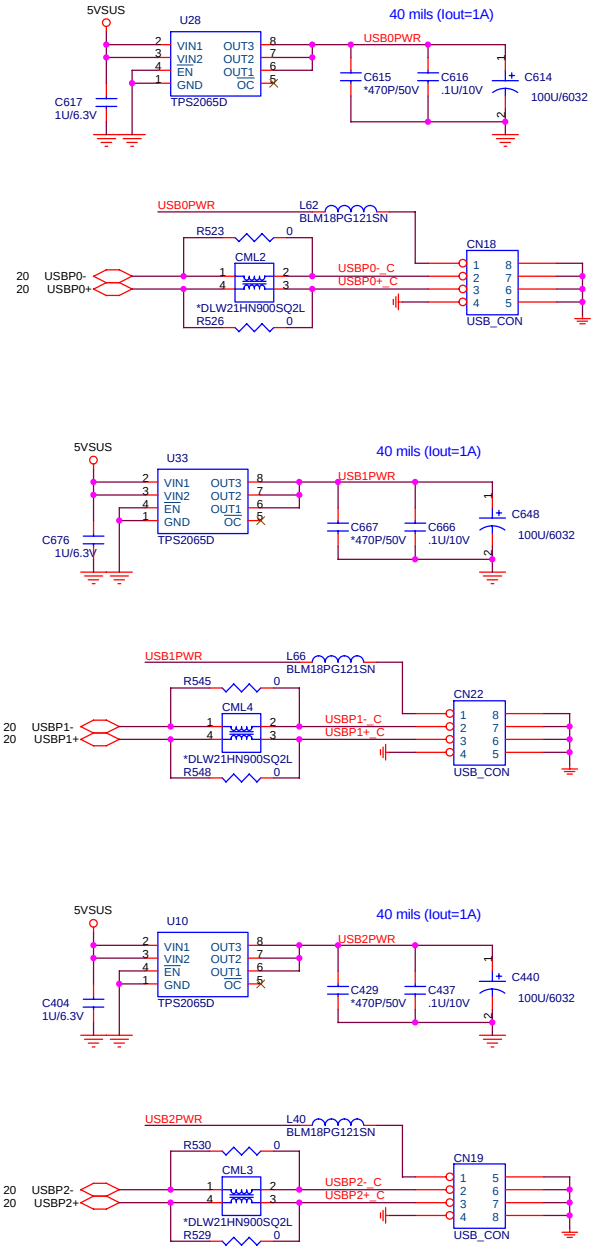
CD-ROM



SATA-HDD CONNECTOR



USBX3



PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD/CD-ROM/USBX3	1A

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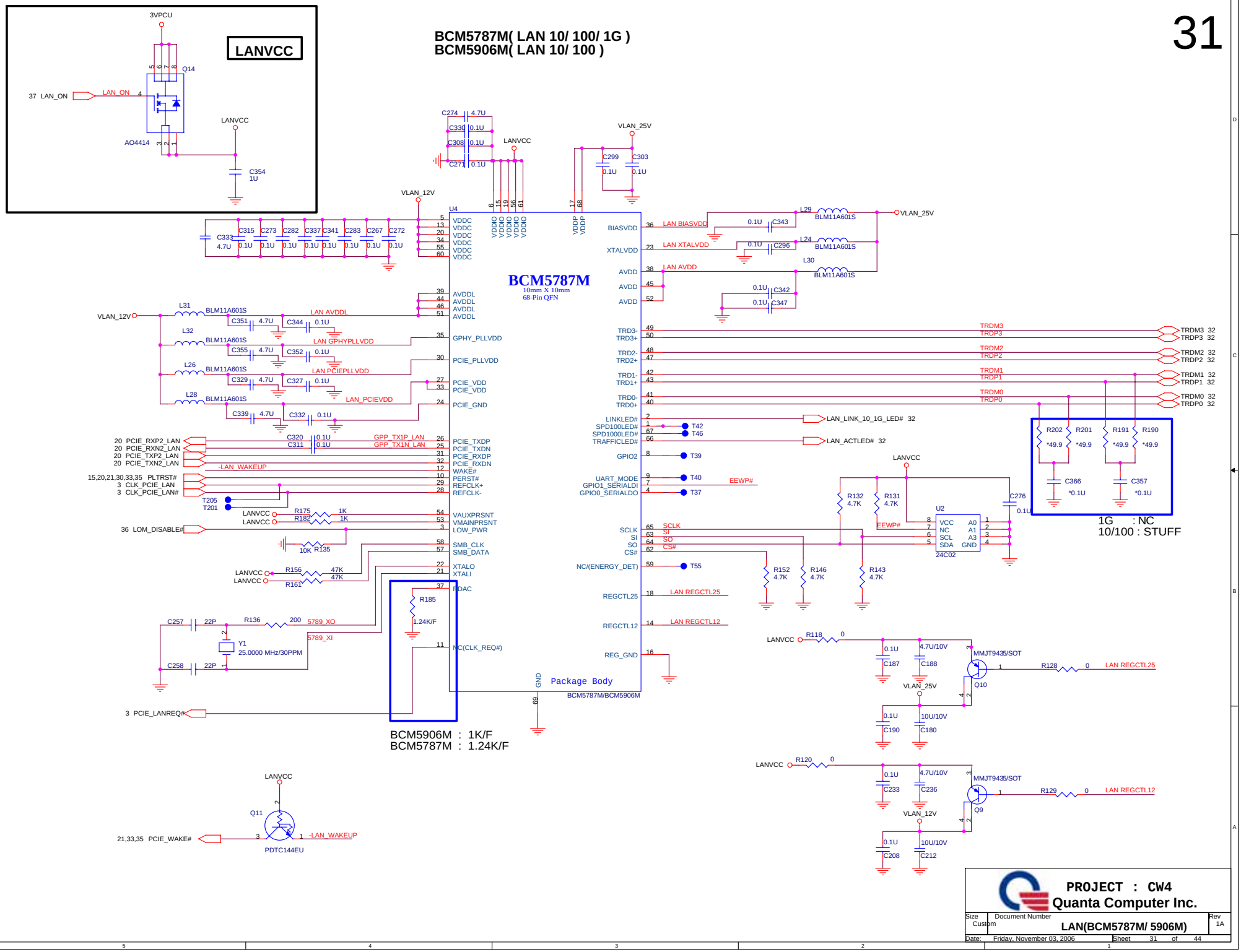
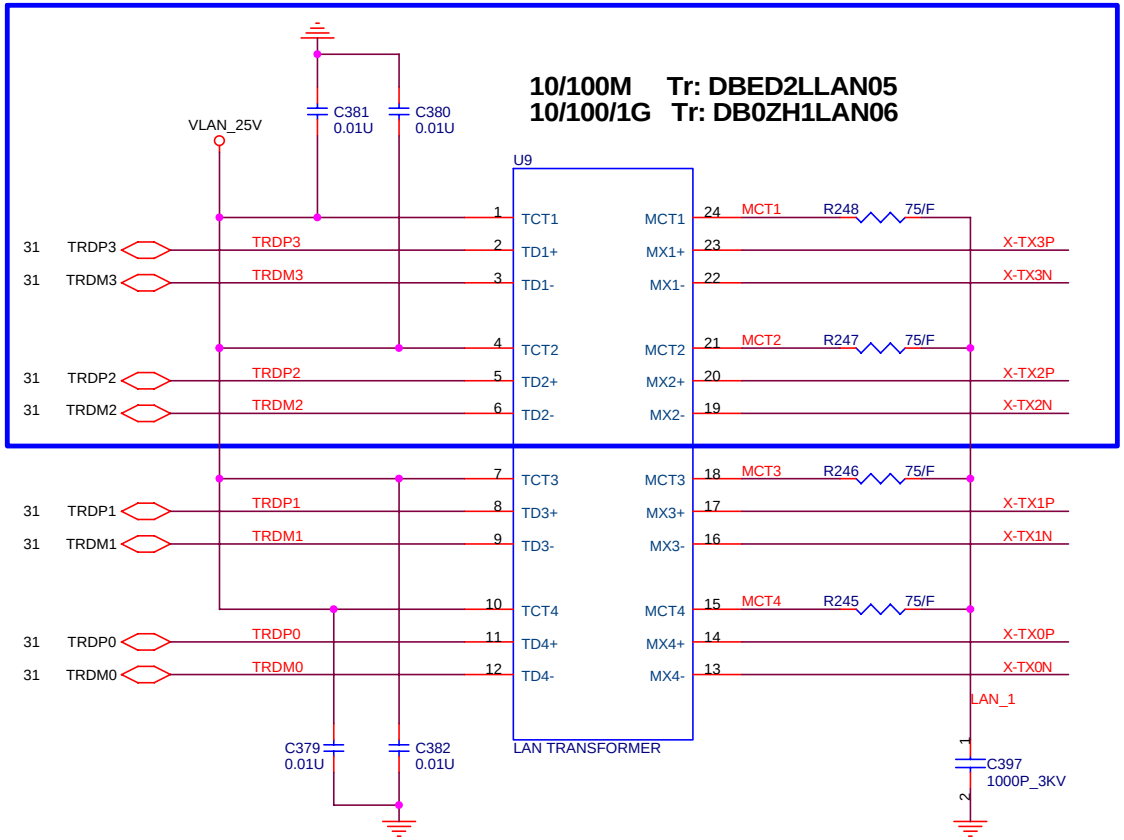
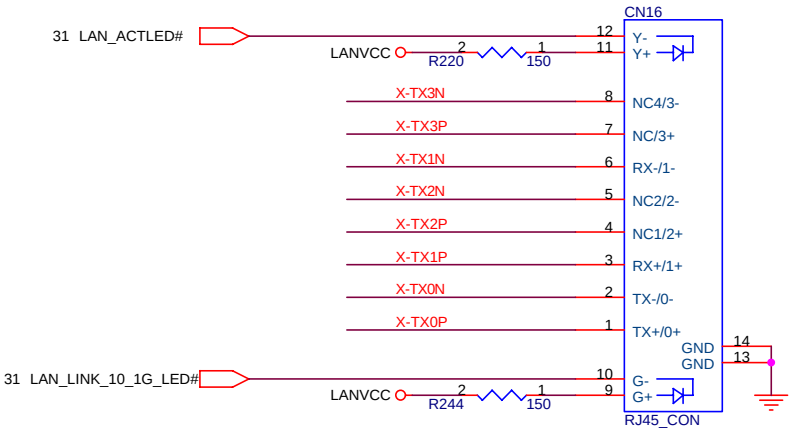
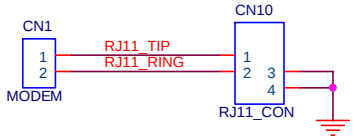
BCM5787M(LAN 10/ 100/ 1G)
BCM5906M(LAN 10/ 100)



RJ45 Connector







PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RJ11/RJ45 CONNECTOR	1A
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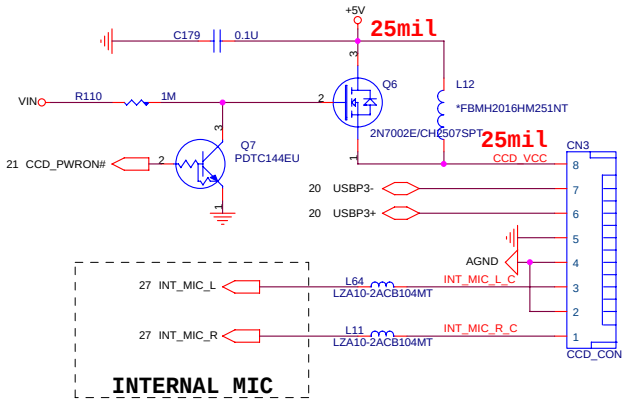
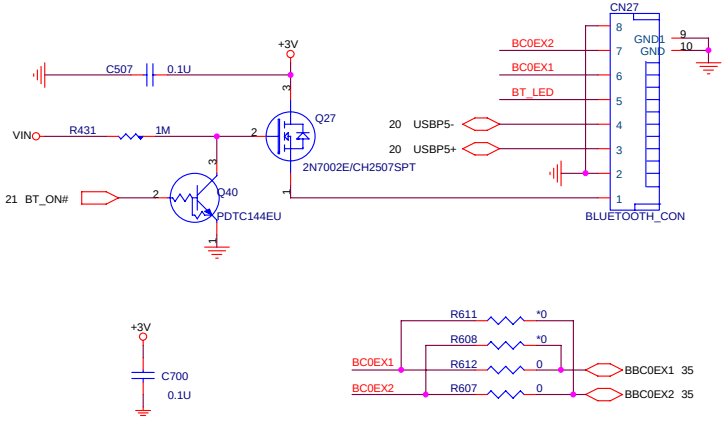
CCD MODULE

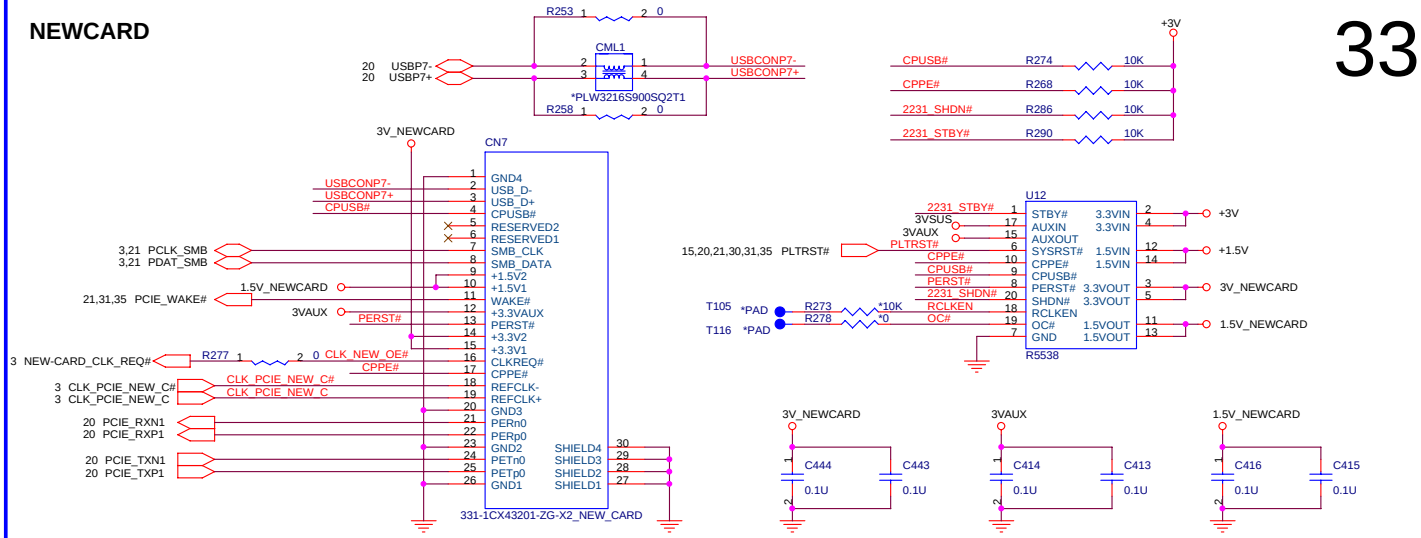


	High	Low
CCD_PWRON#	Disable	Enable

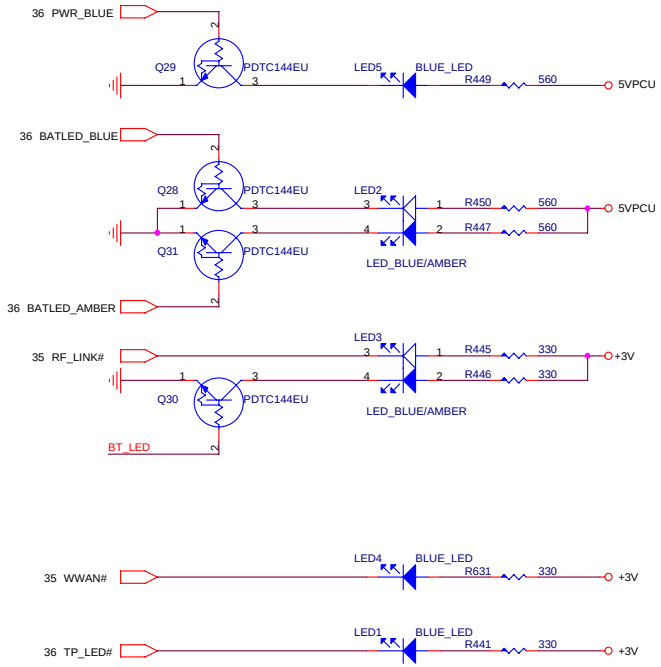
BLUETOOTH



NEWCARD



LED



PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CCD, NEW CARD, B/T, LED	1A

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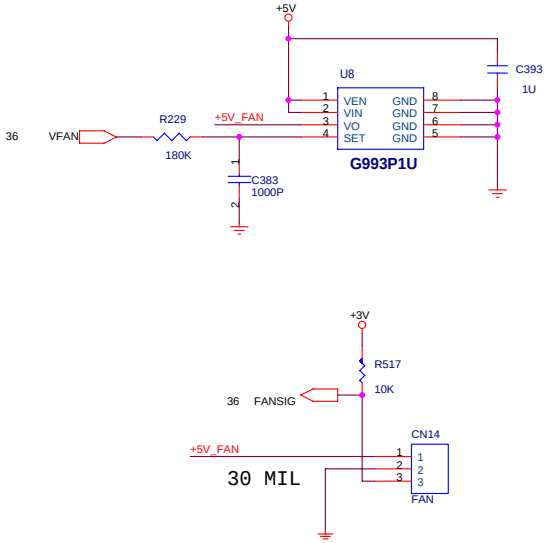
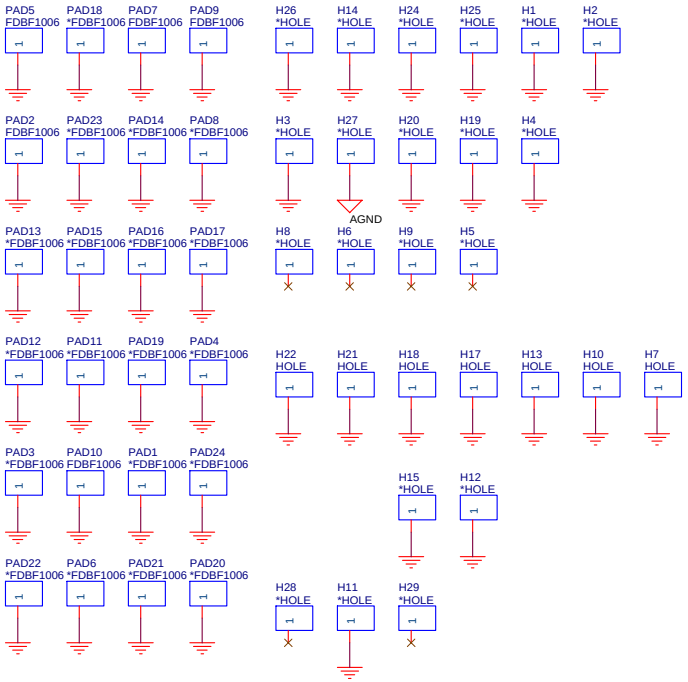
FAN CONTROL

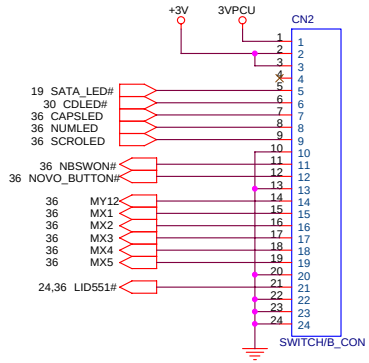


EMI PAD

HOLES

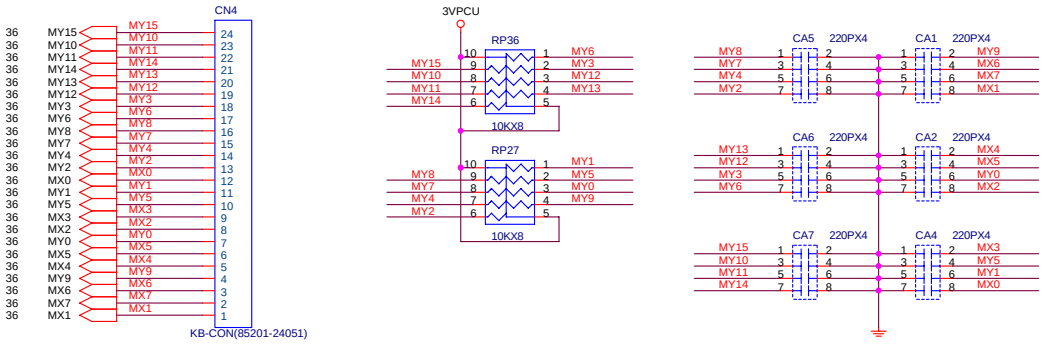


SWITCH BOARD CON.

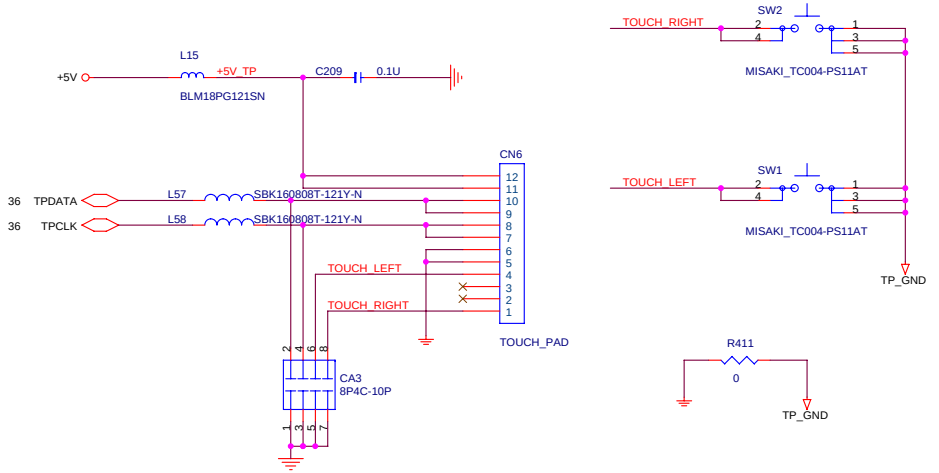


34

KEYBOARD



TOUCH PAD



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Quanta Computer Inc.			
Size: Custom	Document Number: T/P,FAN,KB,T/B CON		Rev: 1A
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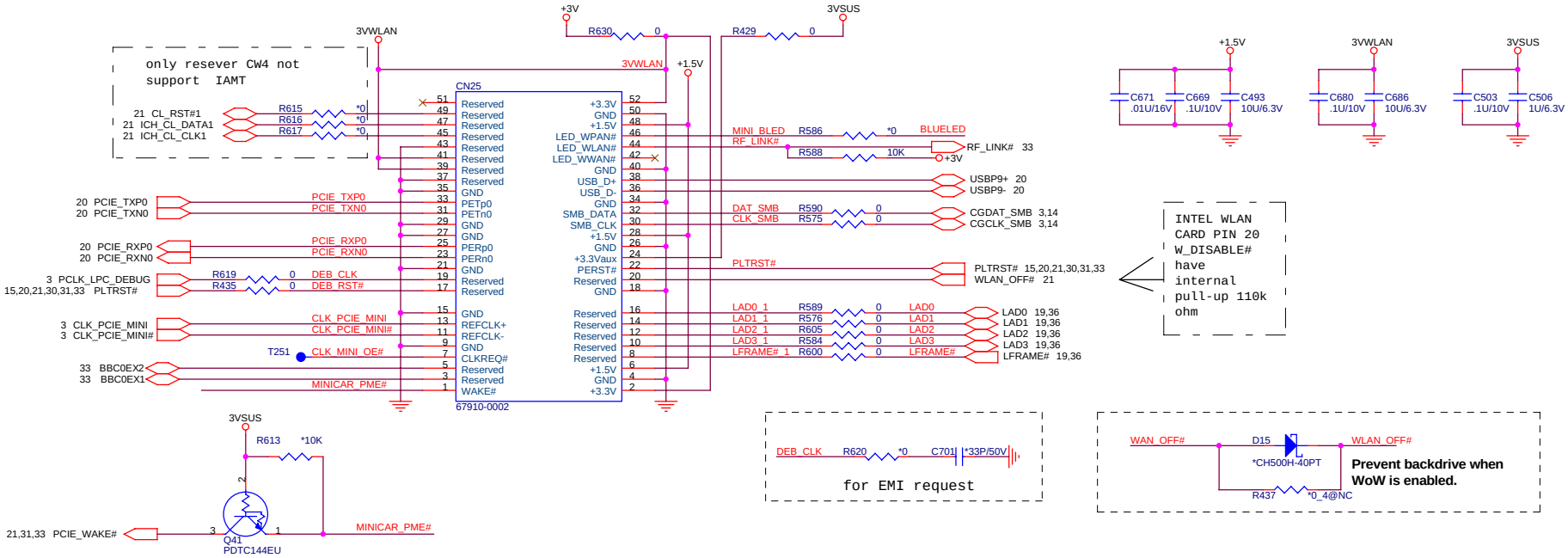
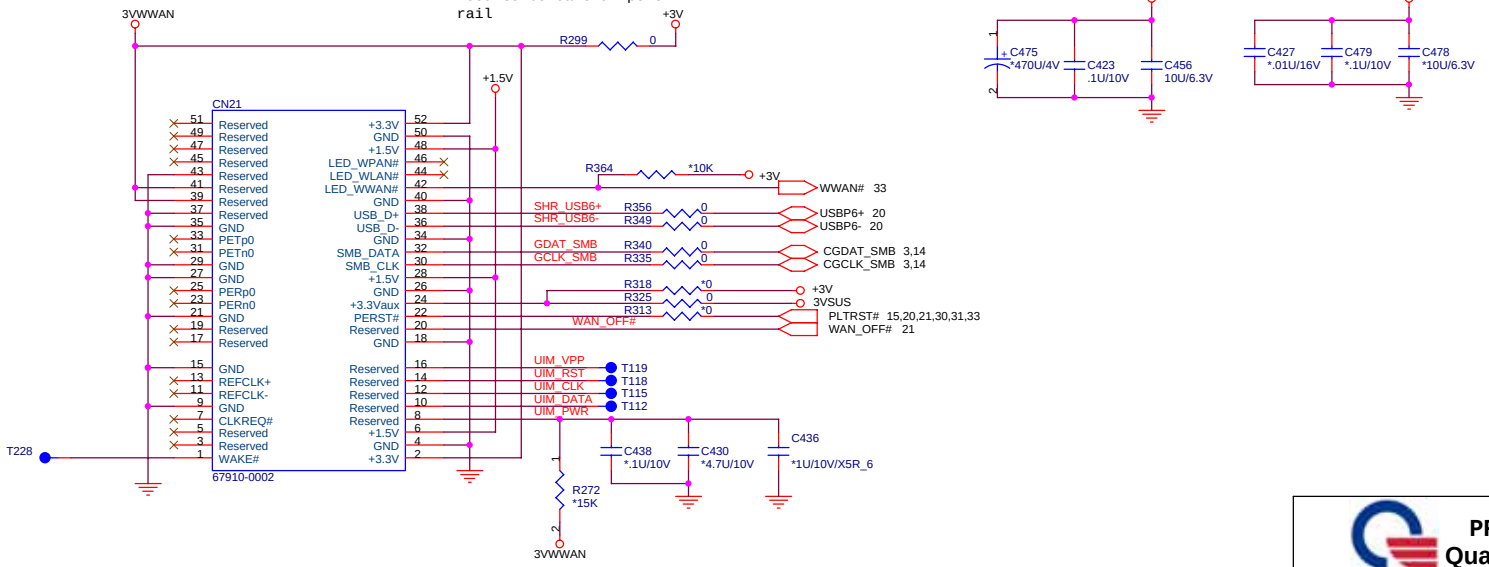
Mini PCI-E Card 1
WLAN



Mini PCI-E Card 2
WWAN(W/SIM)

WWAN -- have 2.8A 7W power consumption
power pin 24.39.41
GND pin 37,43
need to be careful power rail



PROJECT : CW4			
Quanta Computer Inc.			
Size: Custom	Document Number: WLAN & WWAN CON		Rev: 1A
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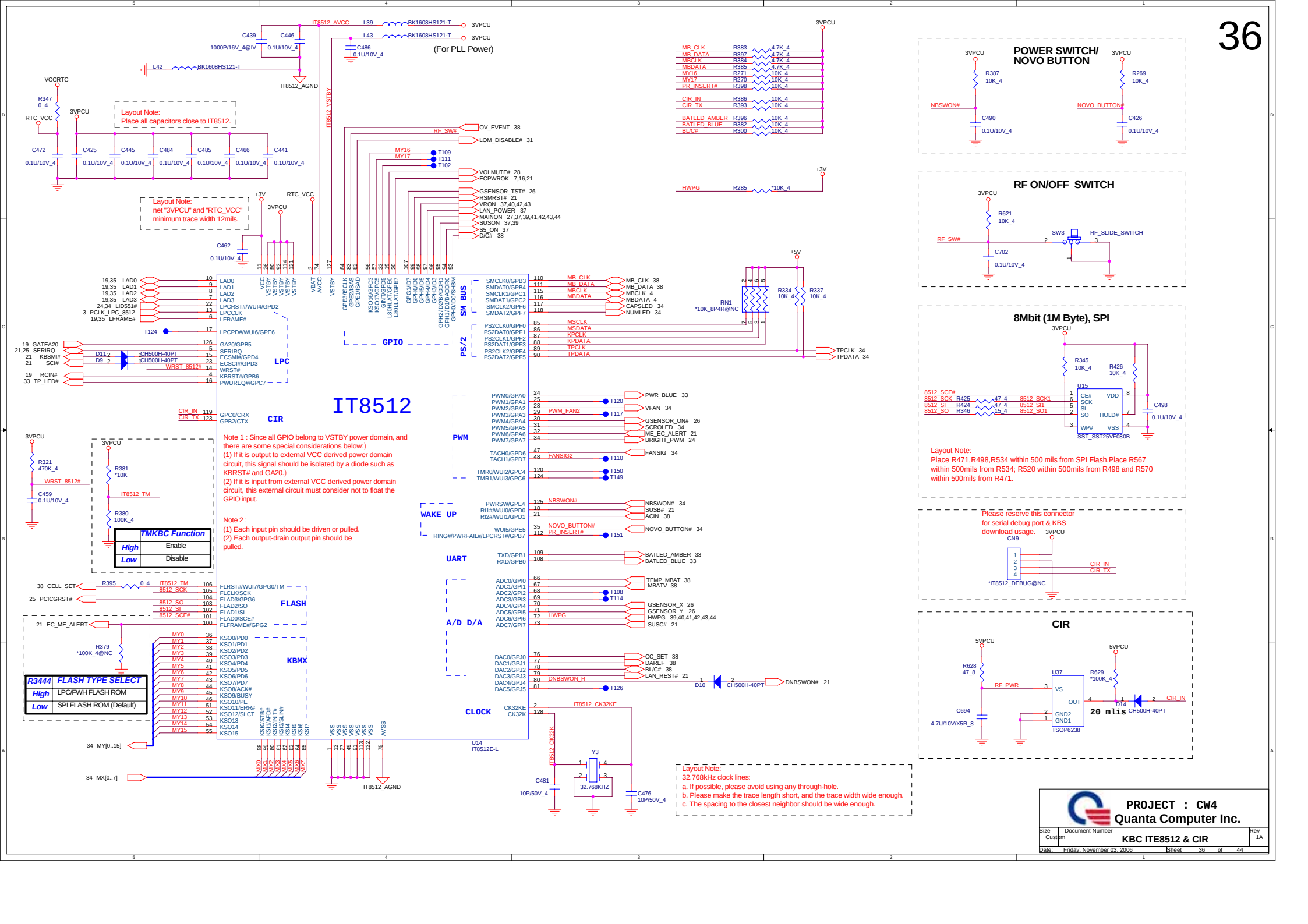
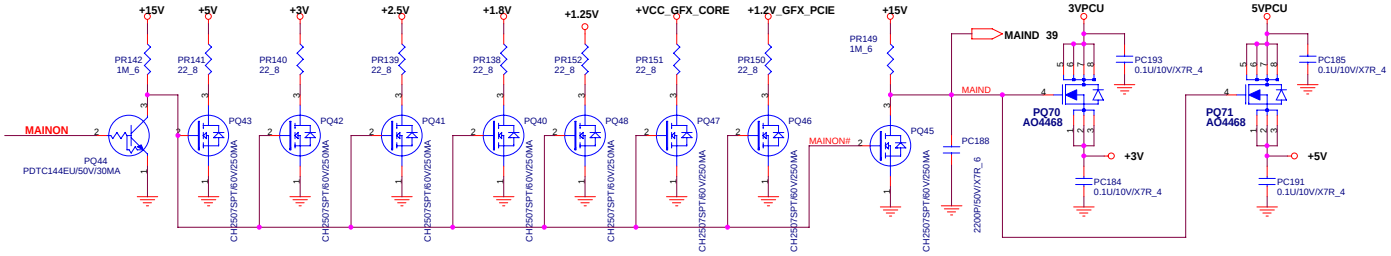
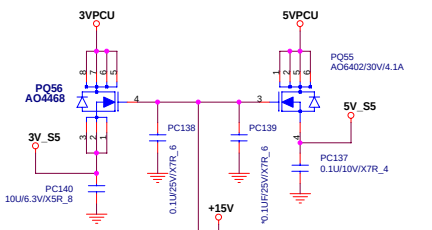
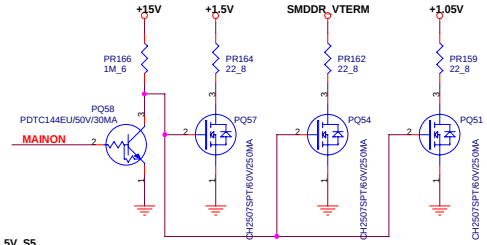
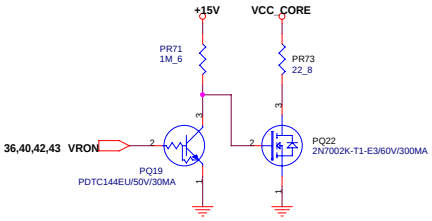

IT8512
(For PLL Power)
Layout Note:
Place all capacitors close to IT8512.
Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.
Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:)
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.)
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.
Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.
TMKBC Function
High Enable
Low Disable
R3444 FLASH TYPE SELECT
High LPC/FWH FLASH ROM
Low SPI FLASH ROM (Default)
Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.
POWER SWITCH/ NOVO BUTTON
RF ON/OFF SWITCH
8Mbit (1M Byte), SPI
SST_SST25VF080B
Layout Note:
Place R471,R498,R534 within 500 mils from SPI Flash.Place R567 within 500mils from R534; R520 within 500mils from R498 and R570 within 500mils from R471.
Please reserve this connector for serial debug port & KBS download usage.
CIR
PROJECT : CW4
Quanta Computer Inc.
KBC ITE8512 & CIR
Date: Friday, November 03, 2006

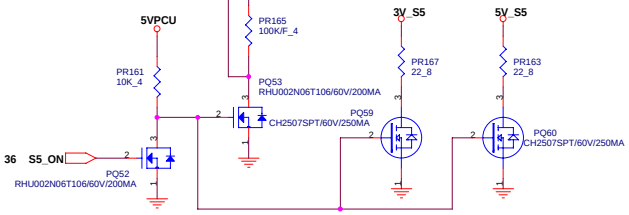
DISCHARGE

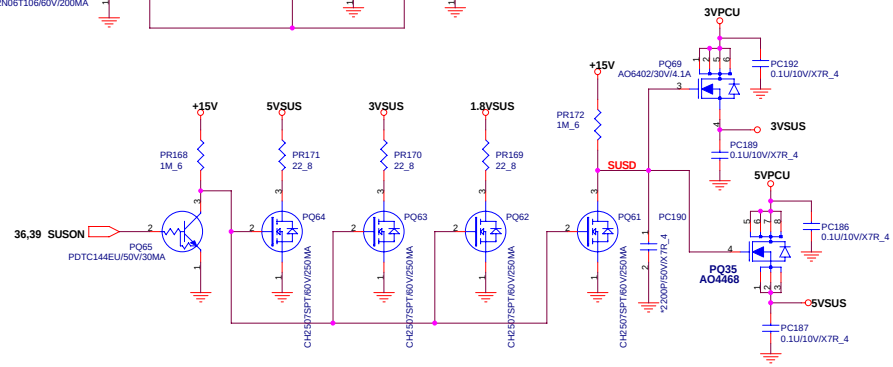


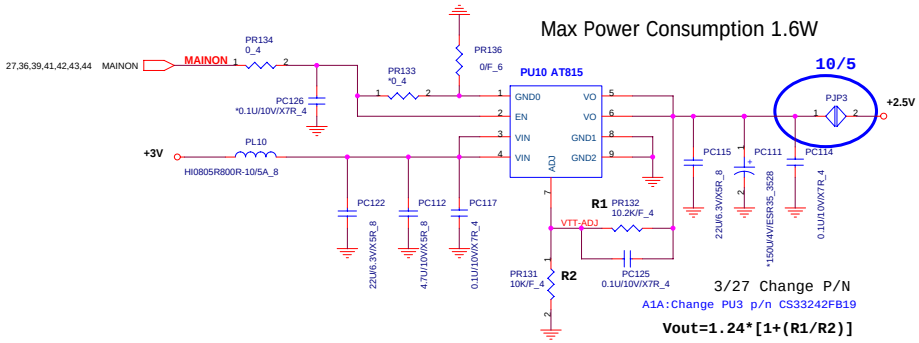


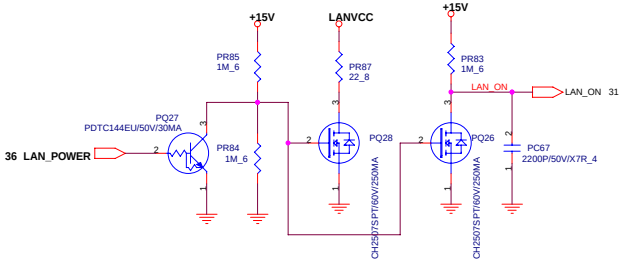












PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
C	DISCHARGE CIRCUIT	1A

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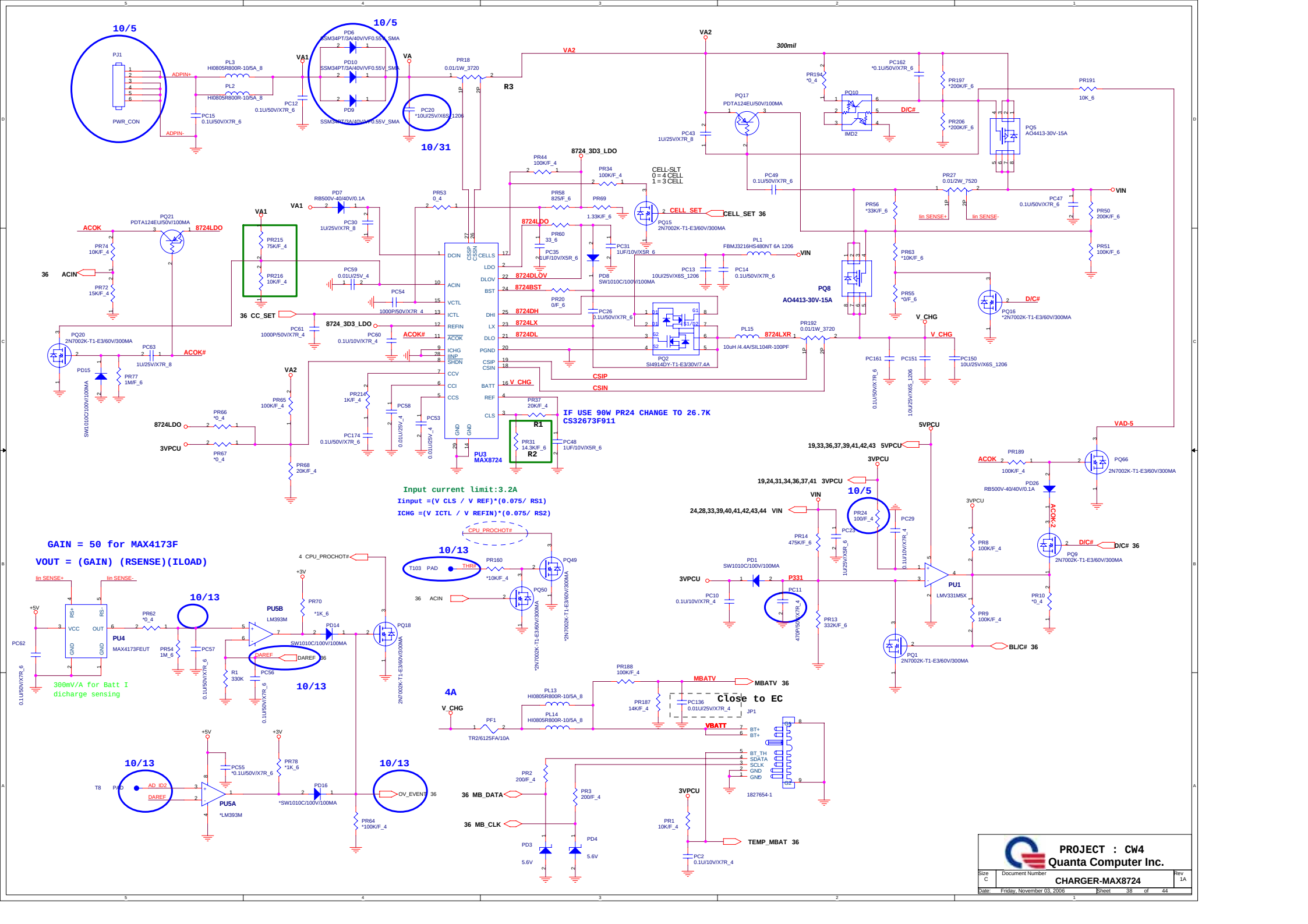

PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
C	CHARGER-MAX8724	1A

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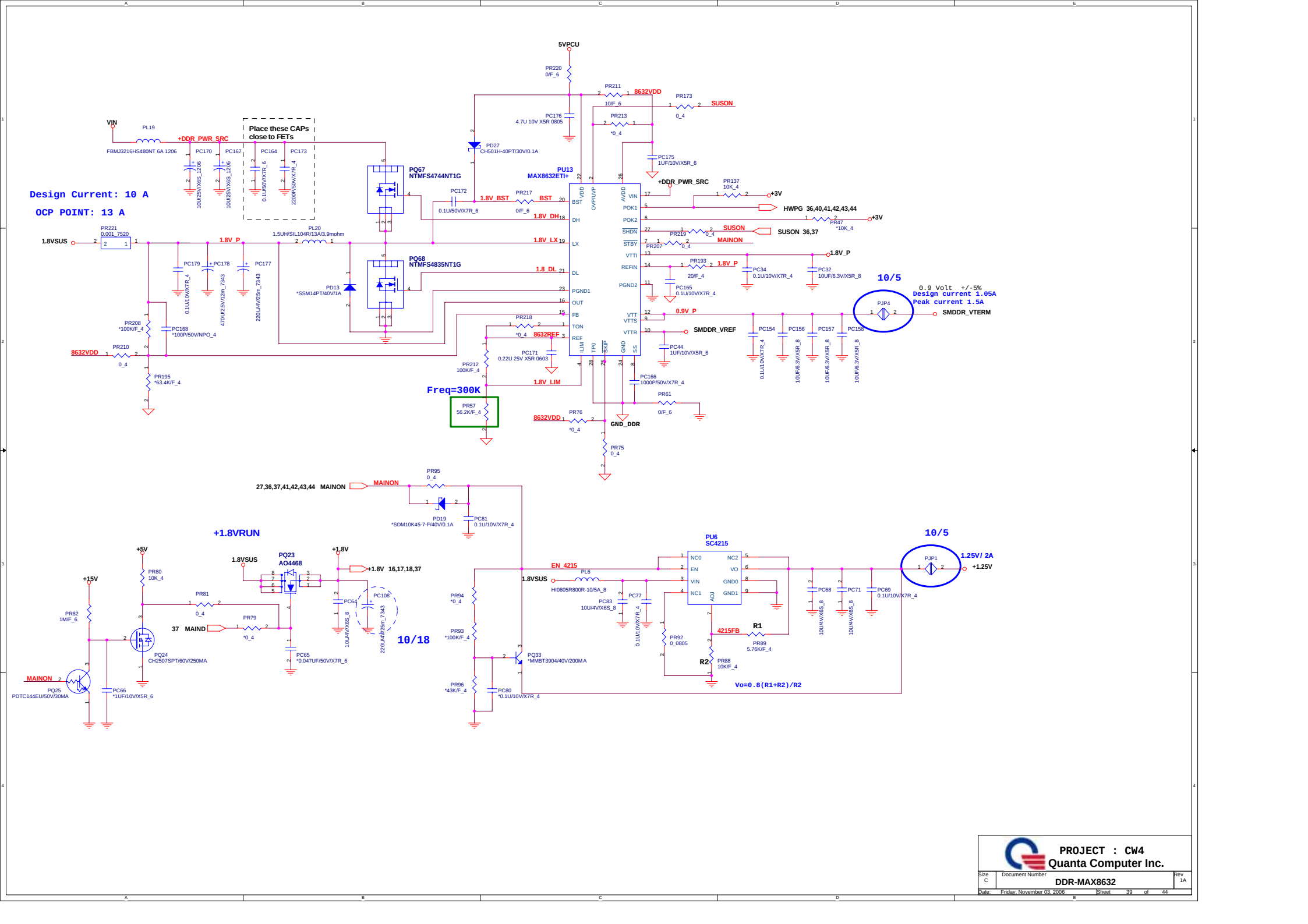
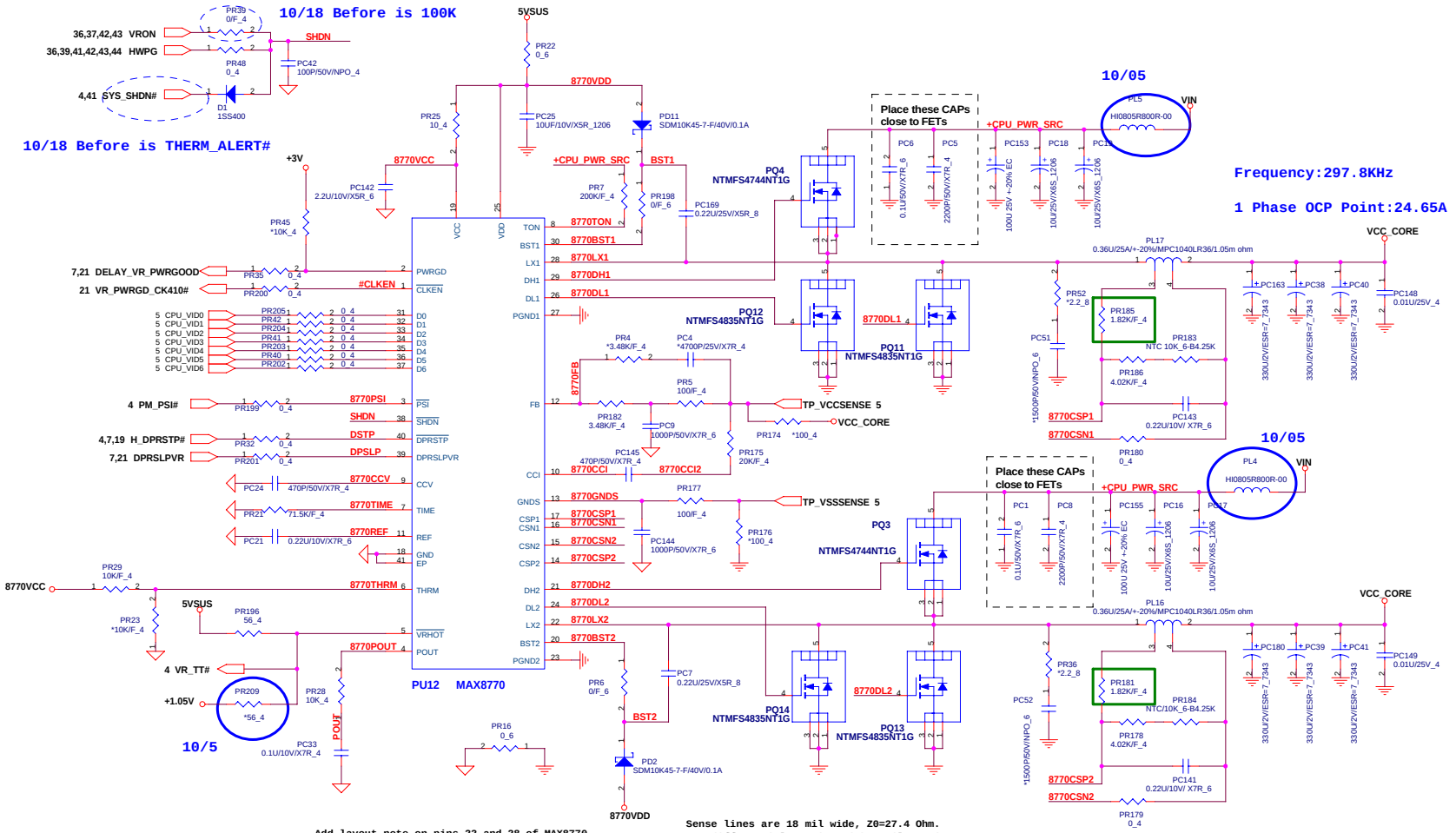
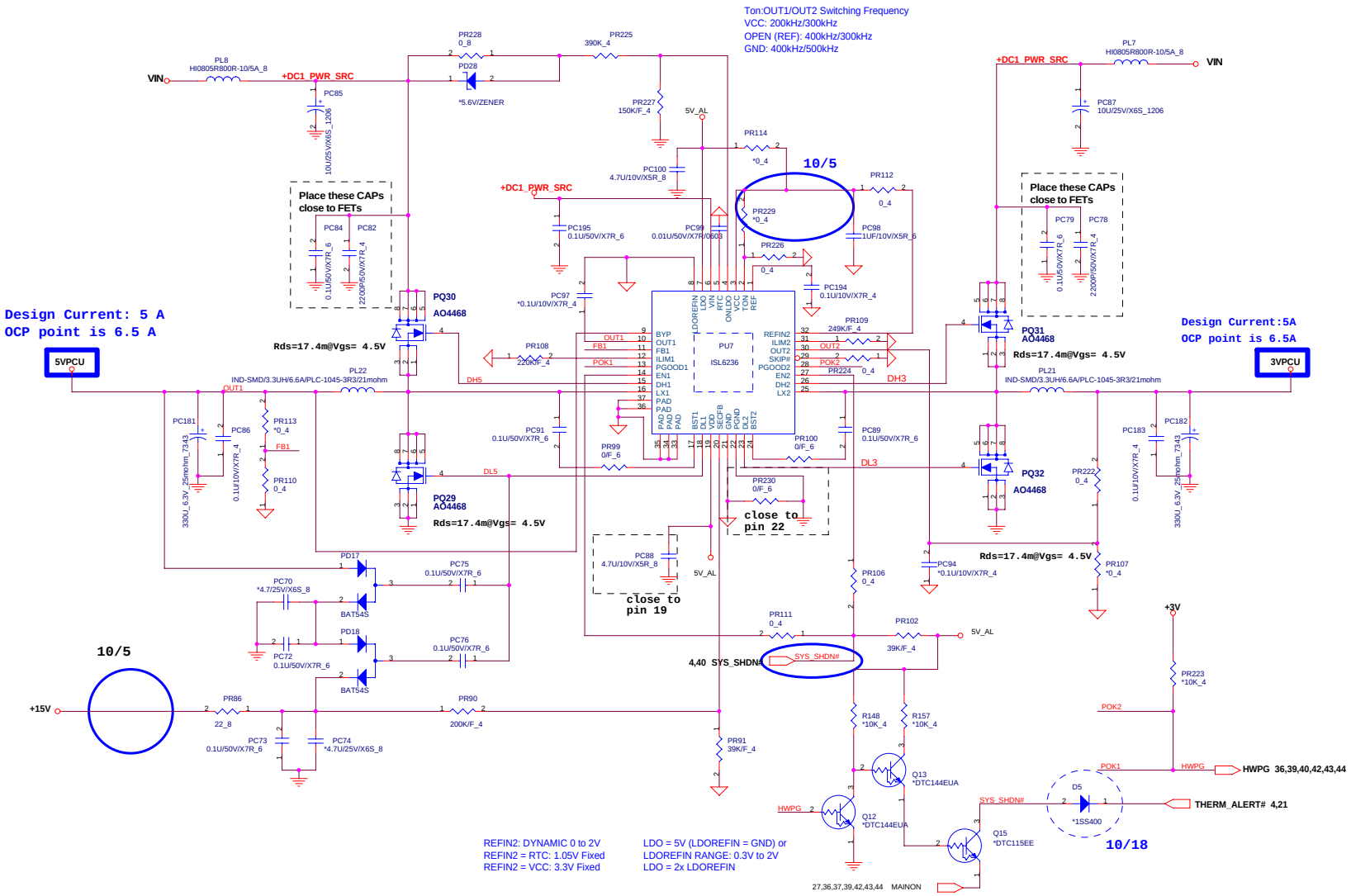

Design Current: 10 A
OCP POINT: 13 A
Place these CAPs close to FETs
Freq=300K
+1.8VRUN
10/5
10/18
10/5
Design current 1.05A
Peak current 1.5A
0.9 Volt +/-5%
Vo=0.8(R1+R2)/R2
PROJECT : CW4
Quanta Computer Inc.
DDR-MAX8632
Friday, November 03, 2006

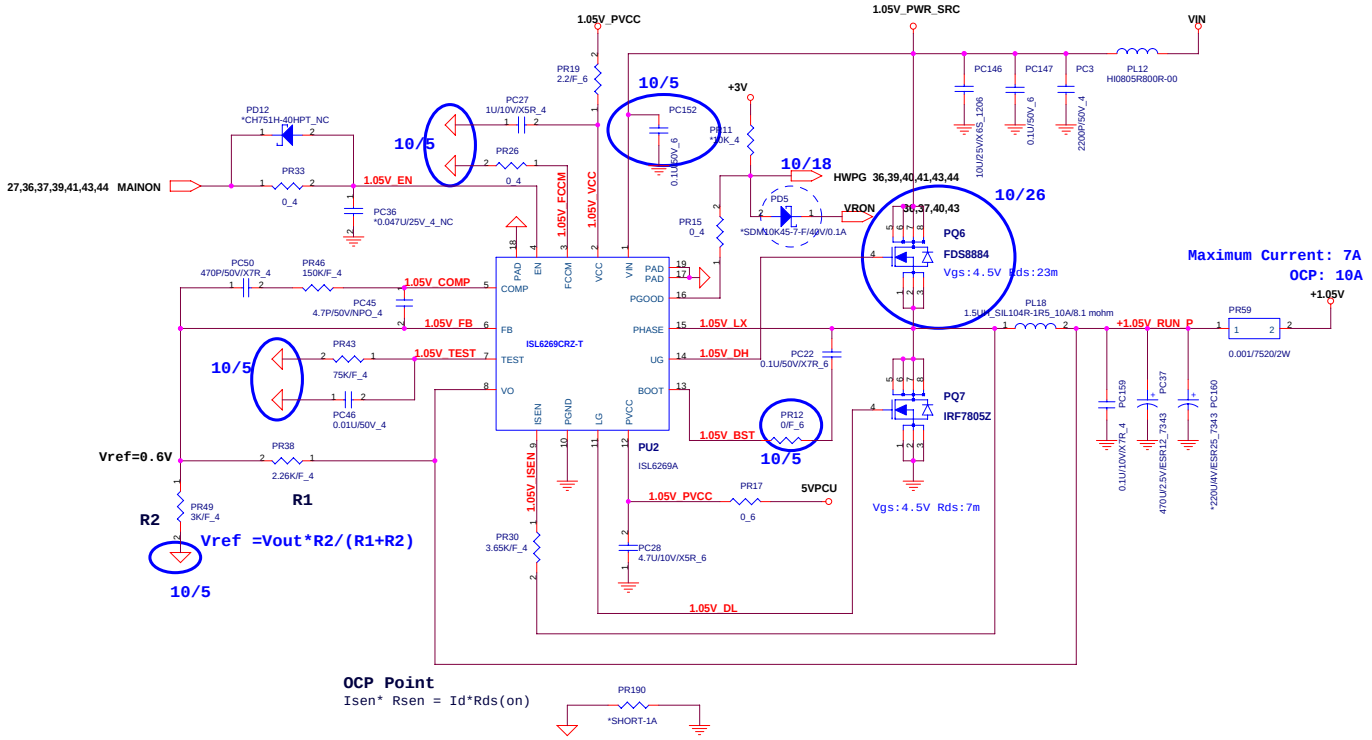


PROJECT : CW4			
Quanta Computer Inc.			
Size: C	Document Number: CPU Core (MAX8770)		Rev: 1A
Date: Friday, November 03, 2006	Sheet 40 of 44		

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW



PROJECT : CW4			
Quanta Computer Inc.			
Size C	Document Number	DC TO DC-ISL6236	Rev 1A
Date: Friday, November 03, 2006	Sheet 41 of 44		



PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
C	1.05V-ISL6269A	1A

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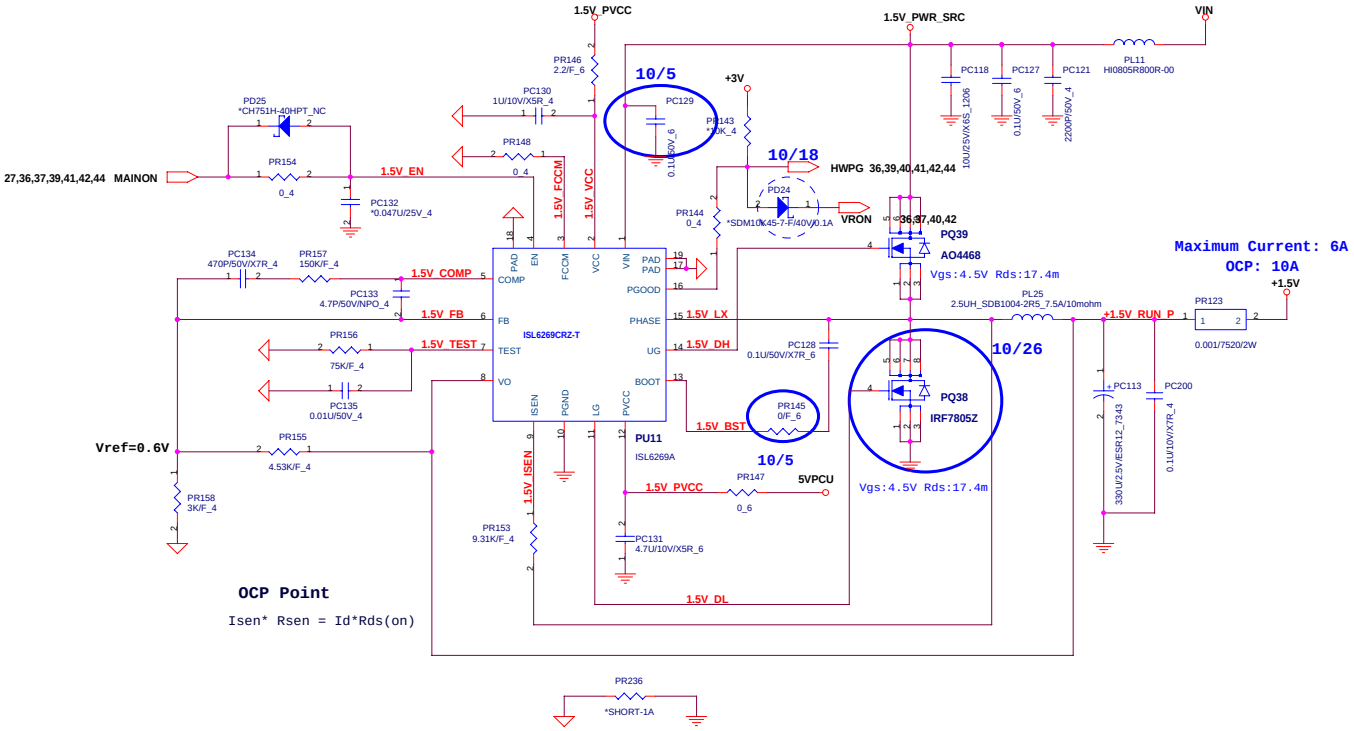
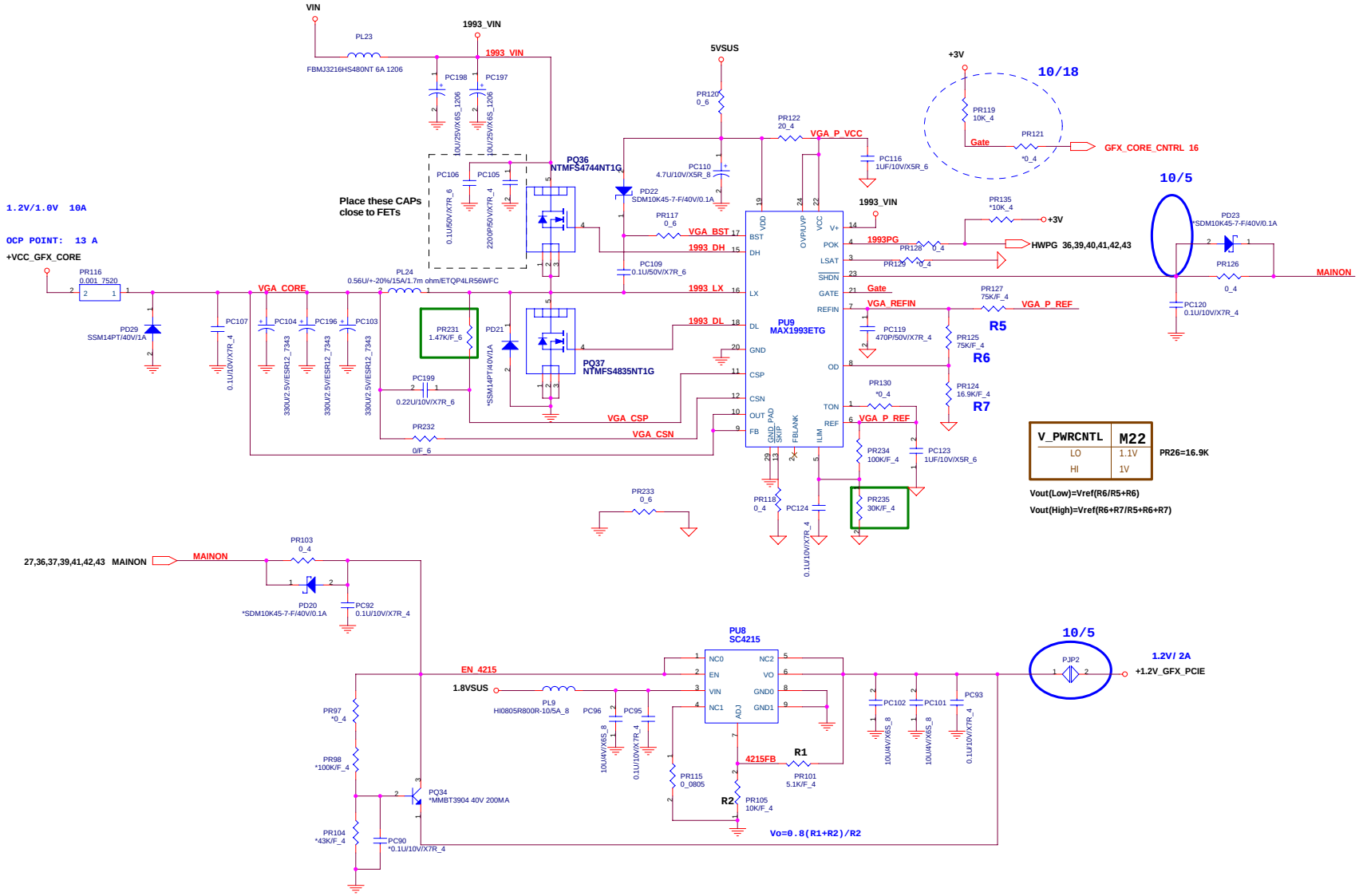


PROJECT : CW4
Quanta Computer Inc.

Size	Document Number	Rev
C	1.5V-ISL6269A	1A

Date: Friday, November 03, 2006 Sheet 43 of 44



PROJECT : CW4			
Quanta Computer Inc.			
Size C	Document Number VGA (MAX1993)		Rev 1A
Date: Friday, November 03, 2006	Sheet 44 of 44		