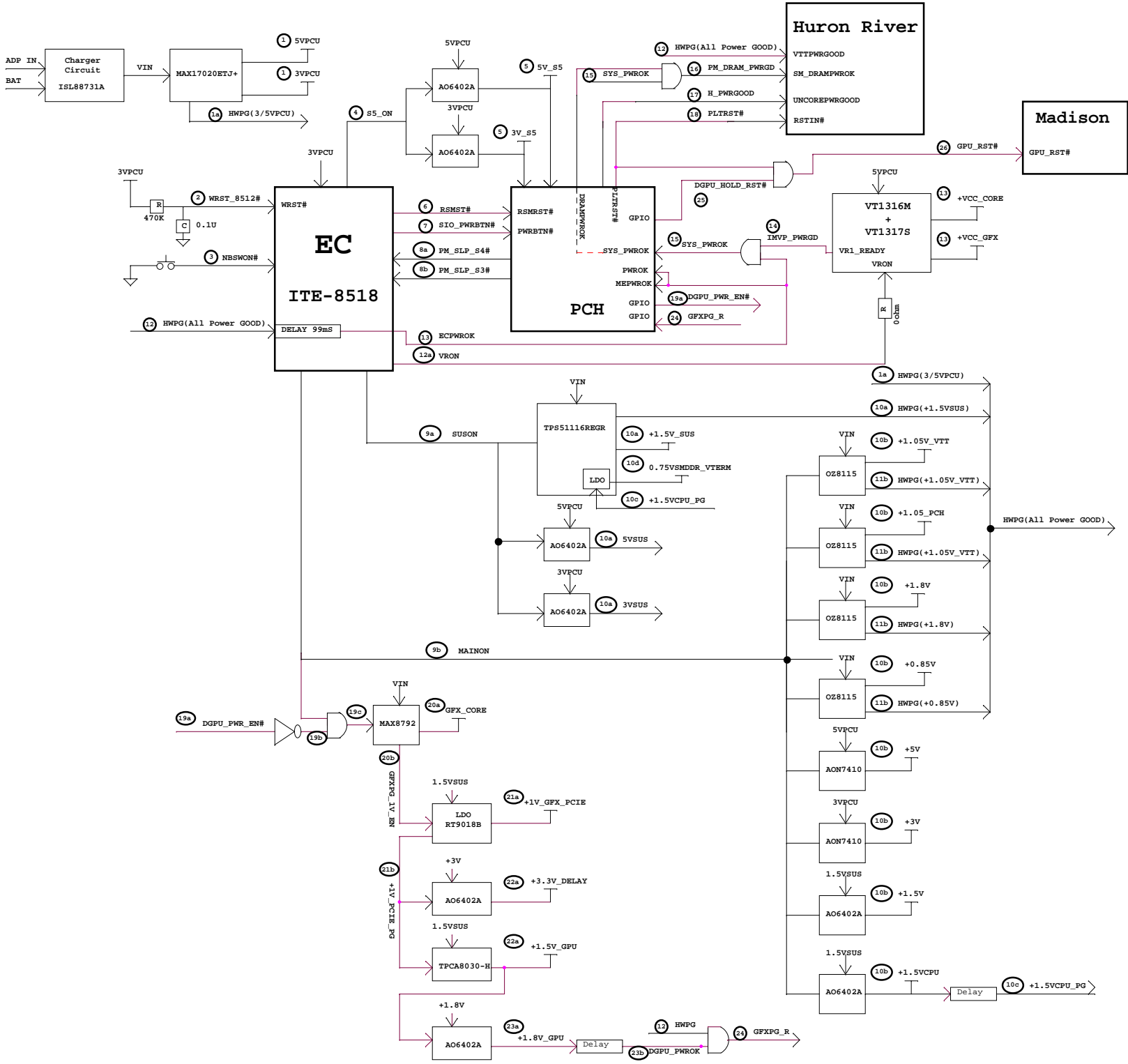


REGULATOR (DDR3) 1.5VSUS, 0.75VSMDDR_VTERM,1.5V 1.5V_GPU,1.5V_CPU
REGULATOR +1.05V_VTT,+1.8V
DC/DC 3VPCU, 5VPCU, +15V PG 42
CPU Core PG 43
VGA Core Discrete PG 44



CLK Gen(CLK)

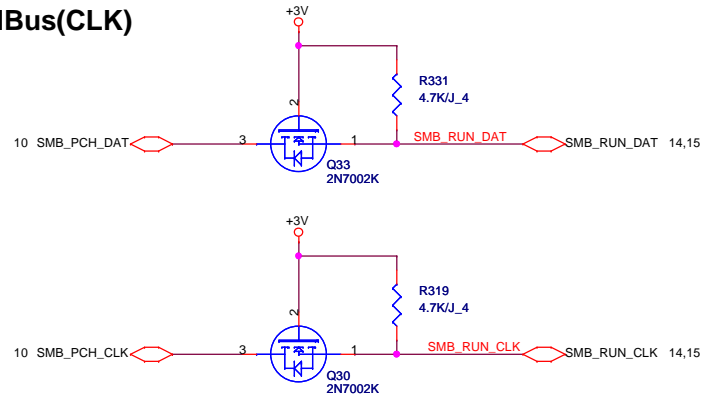
02/20 DEL for Pre-ES1

CPU_CLK select(CLK)

02/20 DEL for Pre-ES1

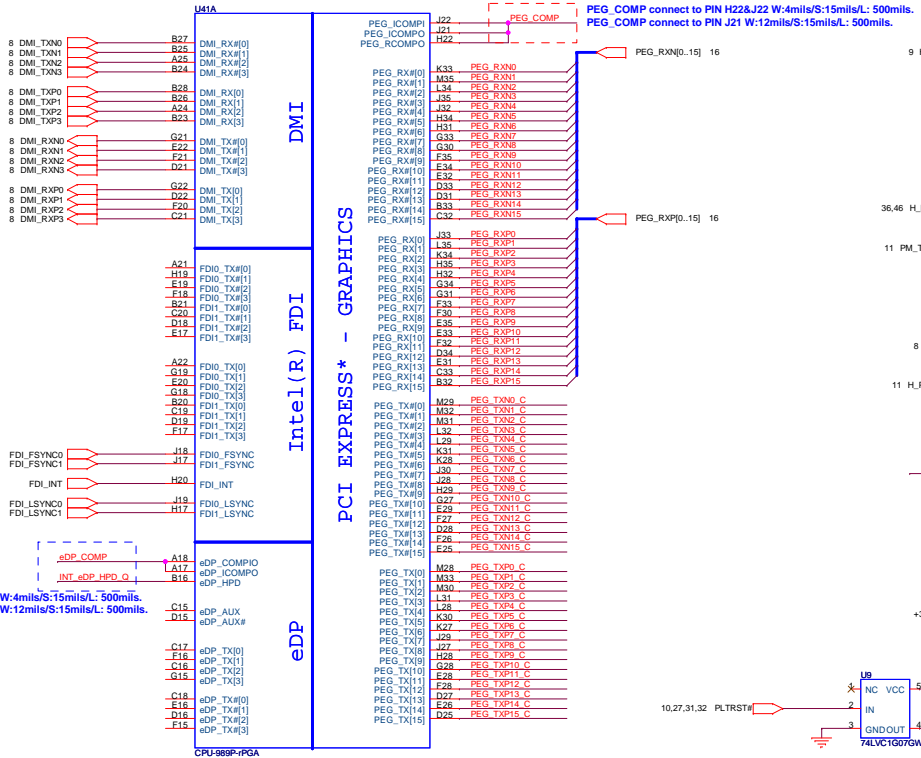
	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus(CLK)

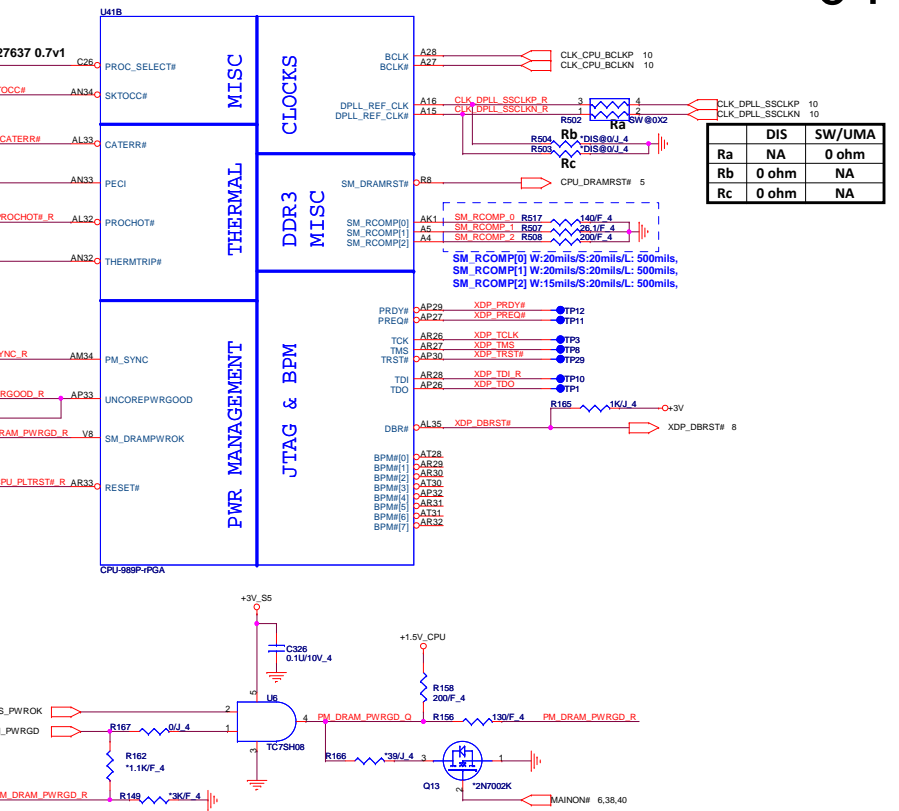


		PROJECT : KL2D Quanta Computer Inc.	
		Size: _____ Document Number: _____ Clock Generator	Rev: 1A
Date: Saturday, July 24, 2010		Sheet 3 of 47	

Sandy Bridge Processor (DMI,PEG,FDI)

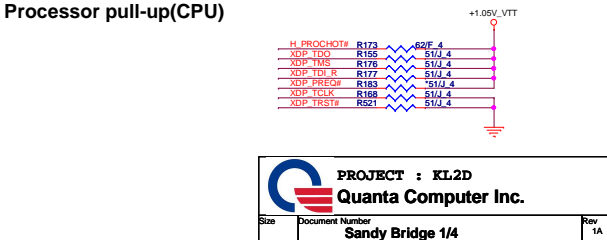
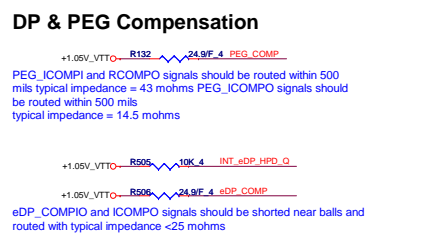
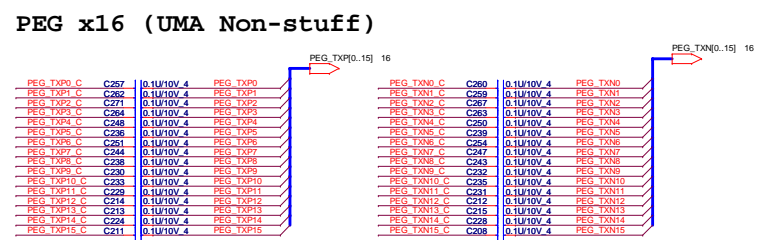
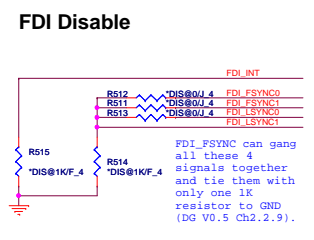


•DP_COMP connect to PIN A18 W:4mils/S:15mils/L: 500mils.
 •DP_COMP connect to PIN A17 W:12mils/S:15mils/L: 500mils.



Ra	DIS	SW/UMA
Rb	0 ohm	NA
Rc	0 ohm	NA

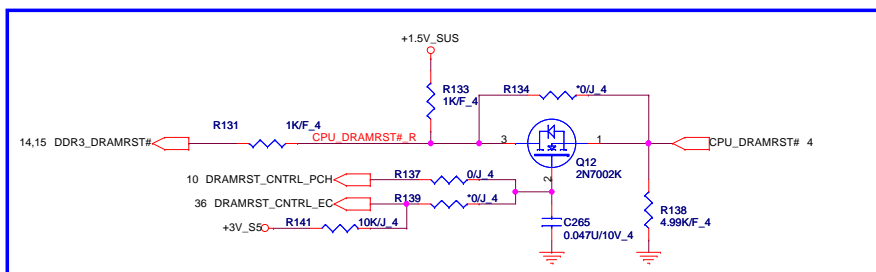
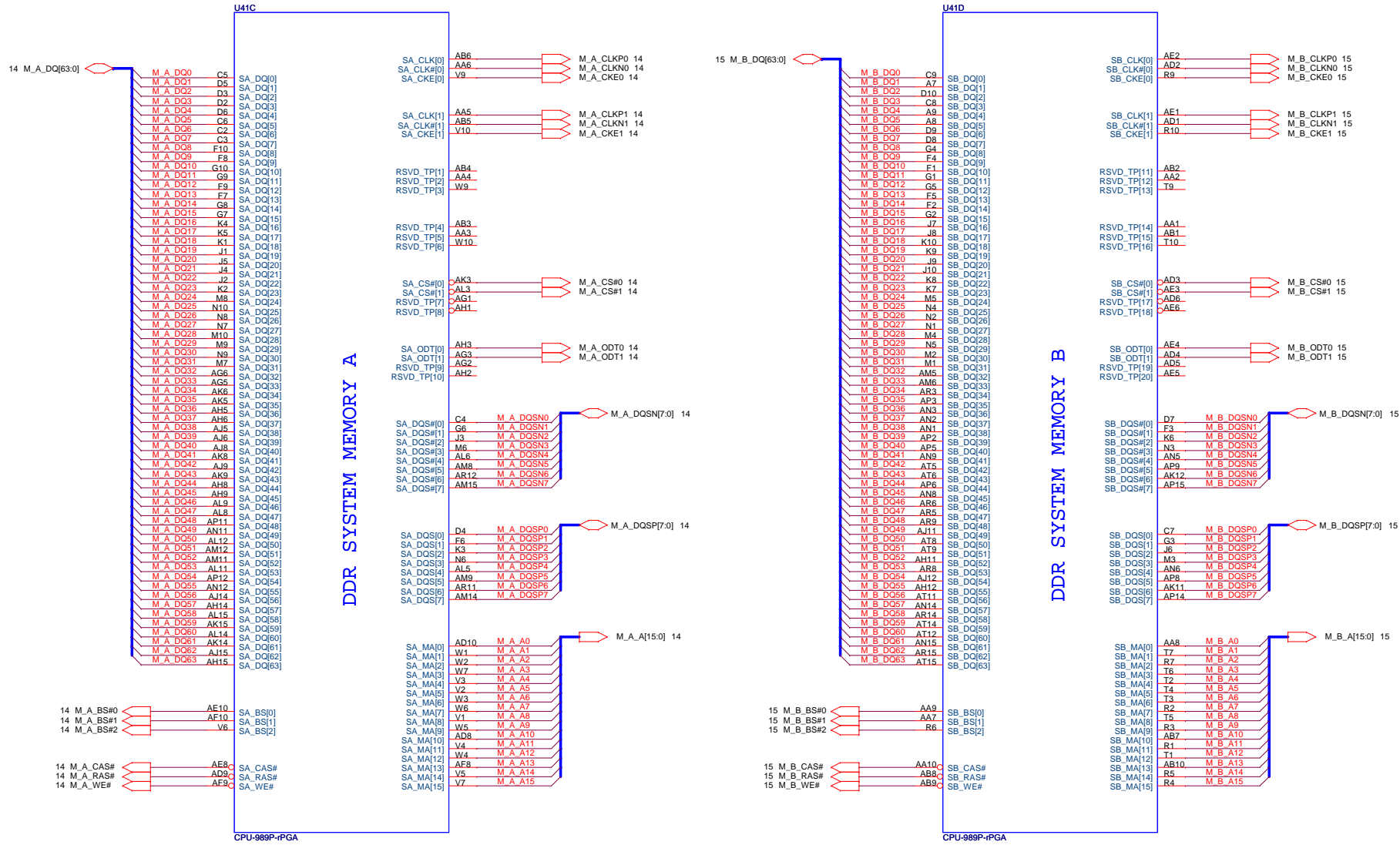
SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
 SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
 SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,



PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
	Sandy Bridge 1/4	1A

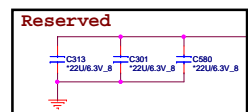
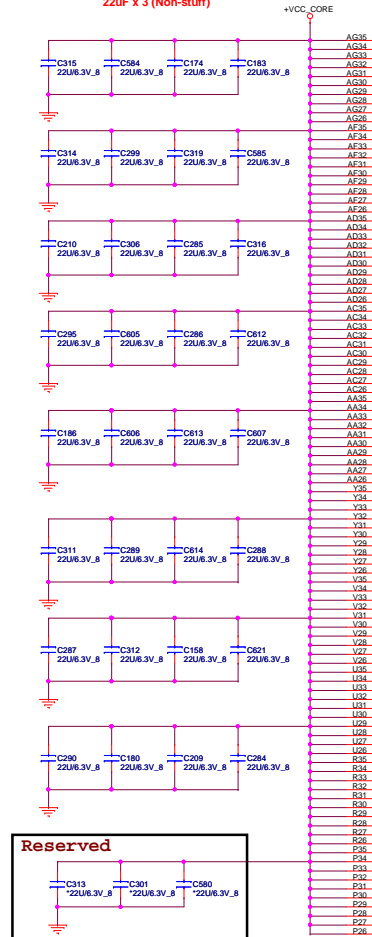
Date: Saturday, July 24, 2010 Sheet 4 of 47



Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

CPU Core Power
SNB 45W:55A
22uF x 32
22uF x 3 (Non-stuff)



POWER

- U41F
- AG3C
- AG34
- AG33
- VCC1
- VCC10
- VCC11
- VCC12
- VCC13
- VCC14
- VCC15
- VCC16
- VCC17
- VCC18
- VCC19
- VCC20
- VCC21
- VCC22
- VCC23
- VCC24
- VCC25
- VCC26
- VCC27
- VCC28
- VCC29
- VCC30
- VCC31
- VCC32
- VCC33
- VCC34
- VCC35
- VCC36
- VCC37
- VCC38
- VCC39
- VCC40
- VCC41
- VCC42
- VCC43
- VCC44
- VCC45
- VCC46
- VCC47
- VCC48
- VCC49
- VCC50
- VCC51
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- VCC54
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- VCC57
- VCC58
- VCC59
- VCC60
- VCC61
- VCC62
- VCC63
- VCC64
- VCC65
- VCC66
- VCC67
- VCC68
- VCC69
- VCC70
- VCC71
- VCC72
- VCC73
- VCC74
- VCC75
- VCC76
- VCC77
- VCC78
- VCC79
- VCC80
- VCC81
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- VCC88
- VCC89
- VCC90
- VCC91
- VCC92
- VCC93
- VCC94
- VCC95
- VCC96
- VCC97
- VCC98
- VCC99
- VCC100

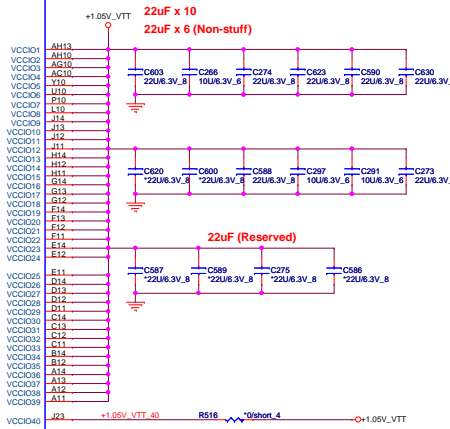
PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

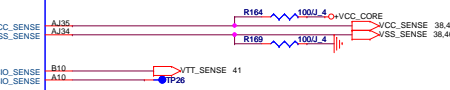
CPU VTT
SNB 45W:8.5A
22uF x 10
22uF x 6 (Non-stuff)



CPU VCCPL
SNB 45W:3A
330uF/7mohm x 1
10uF x 1
1uF x 2



VCC_SENSE
VSS_SENSE



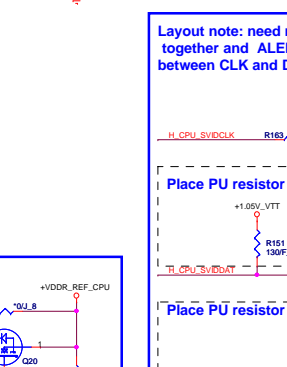
VTT_SENSE



CPU VGT
SNB 45W:22A
22uF x 12
22uF x 4 (Reserved)



GPU VTT
SNB 45W:8.5A
22uF x 10
22uF x 6 (Non-stuff)



POWER

- U41G
- AT20
- AT21
- AT22
- AT23
- AT24
- AT25
- AT26
- AT27
- AT28
- AT29
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- AT99
- AT100

GRAPHICS

DDR3 -1.5V RAILS

SA RAIL

MISC

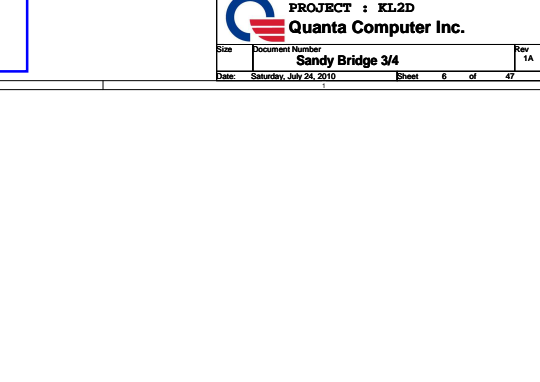
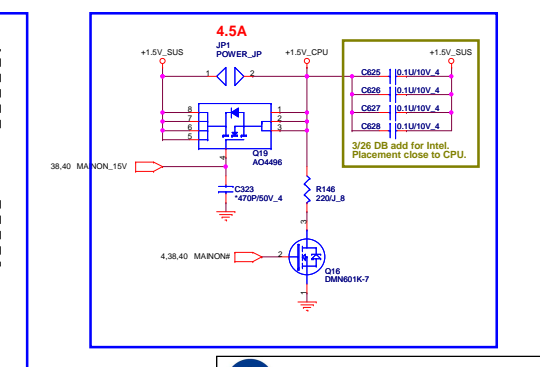
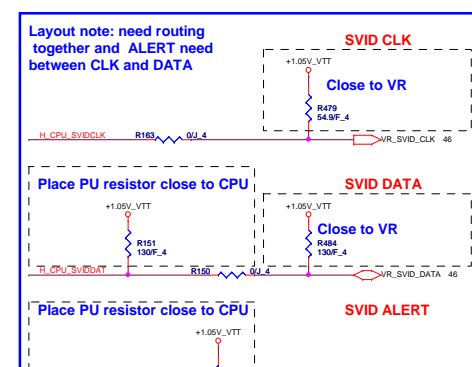
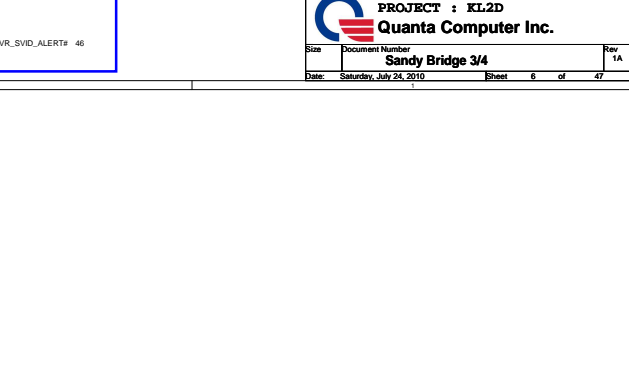
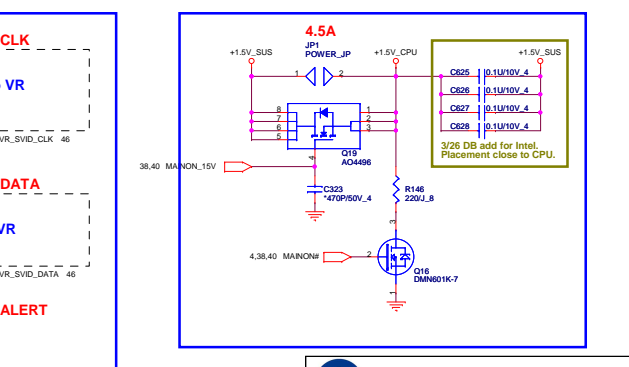
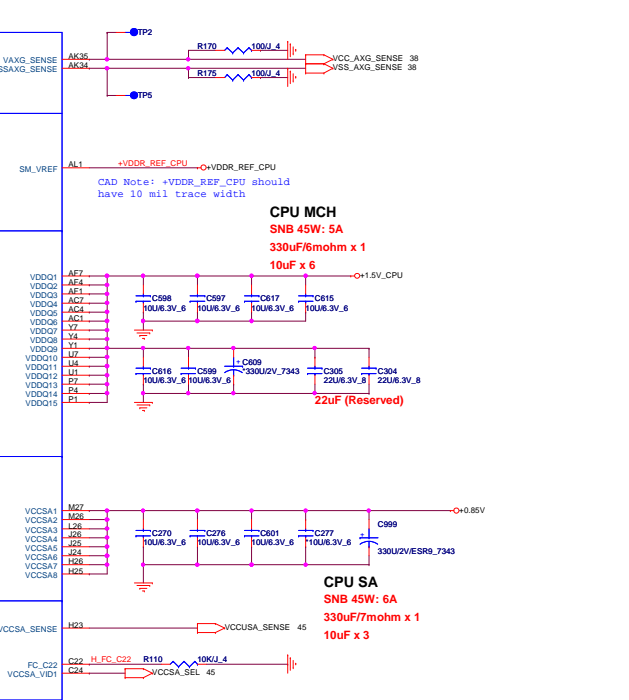
1.8V RAIL

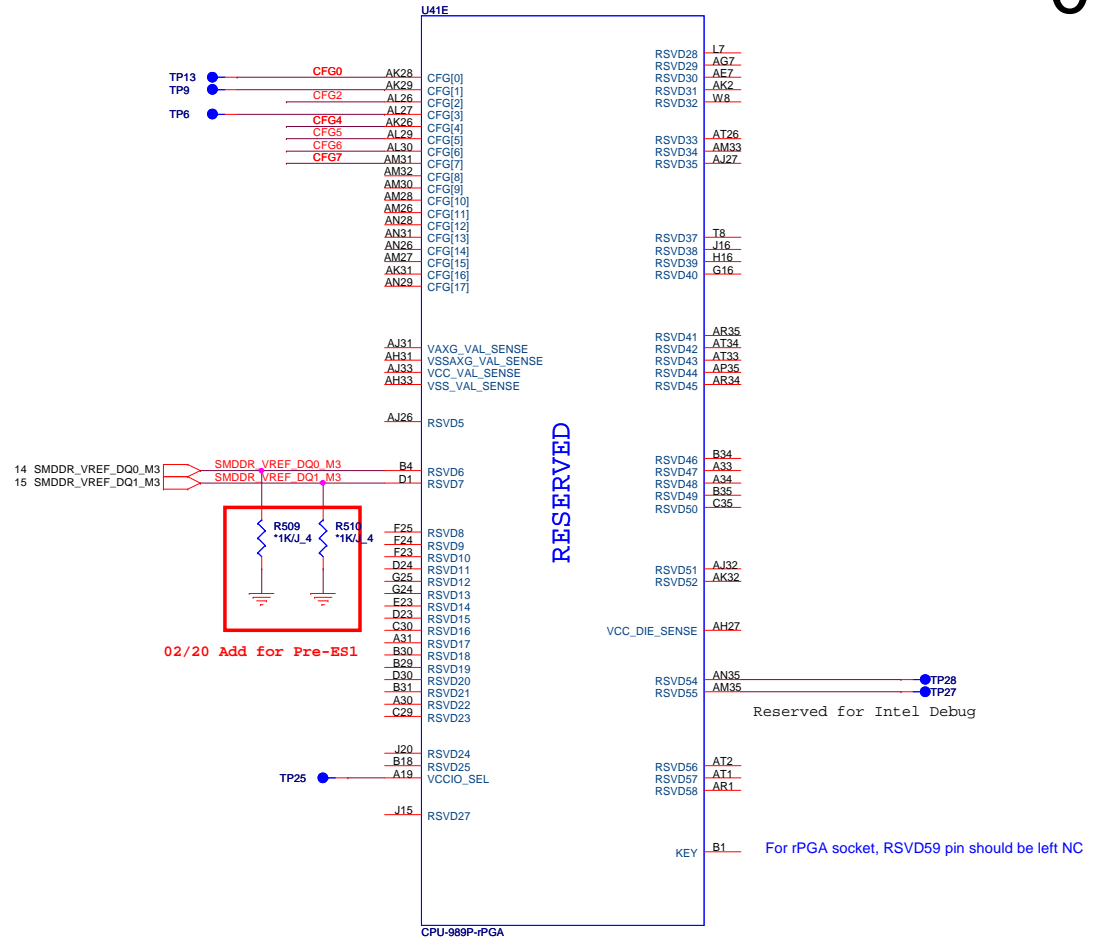
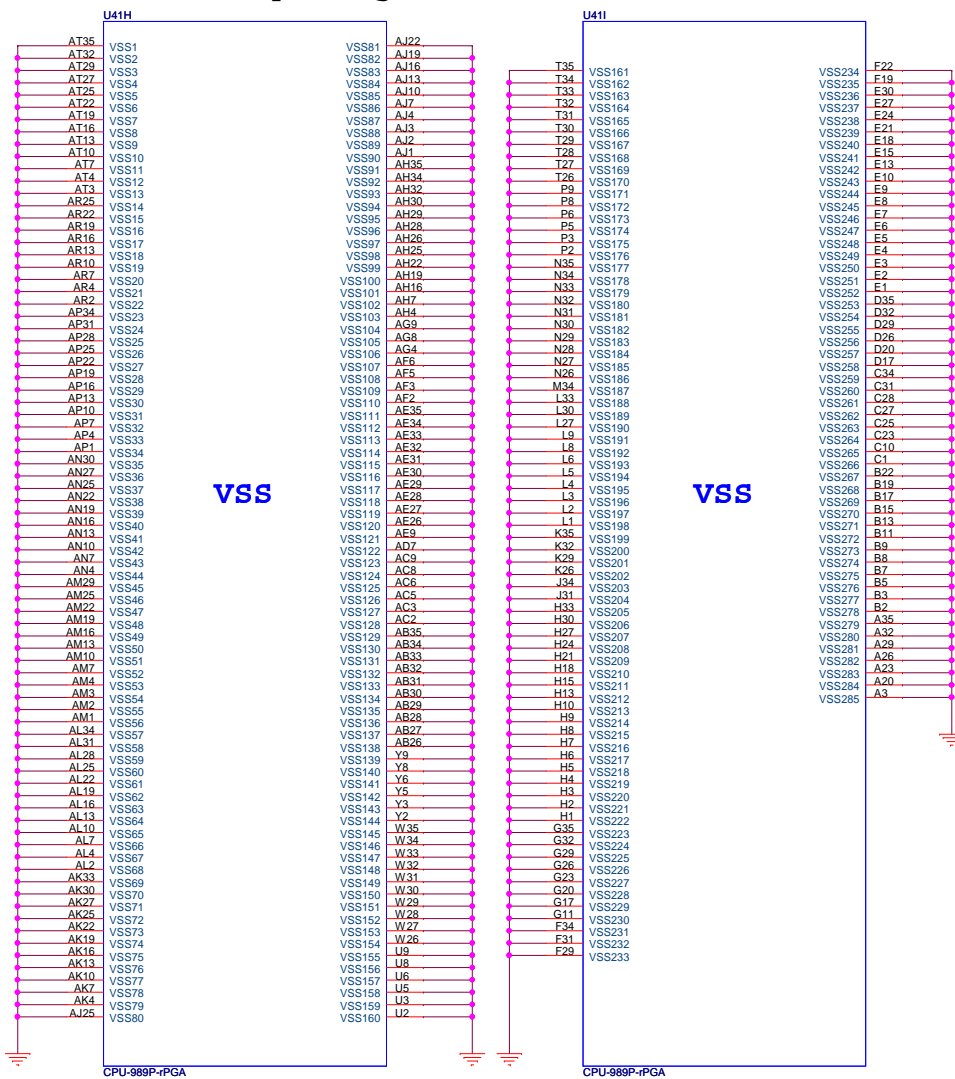
SENSE LINES

VREF

VDDREF_CPU

VDDREF_CPU

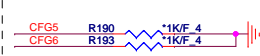




Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



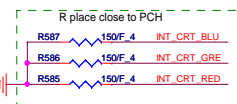
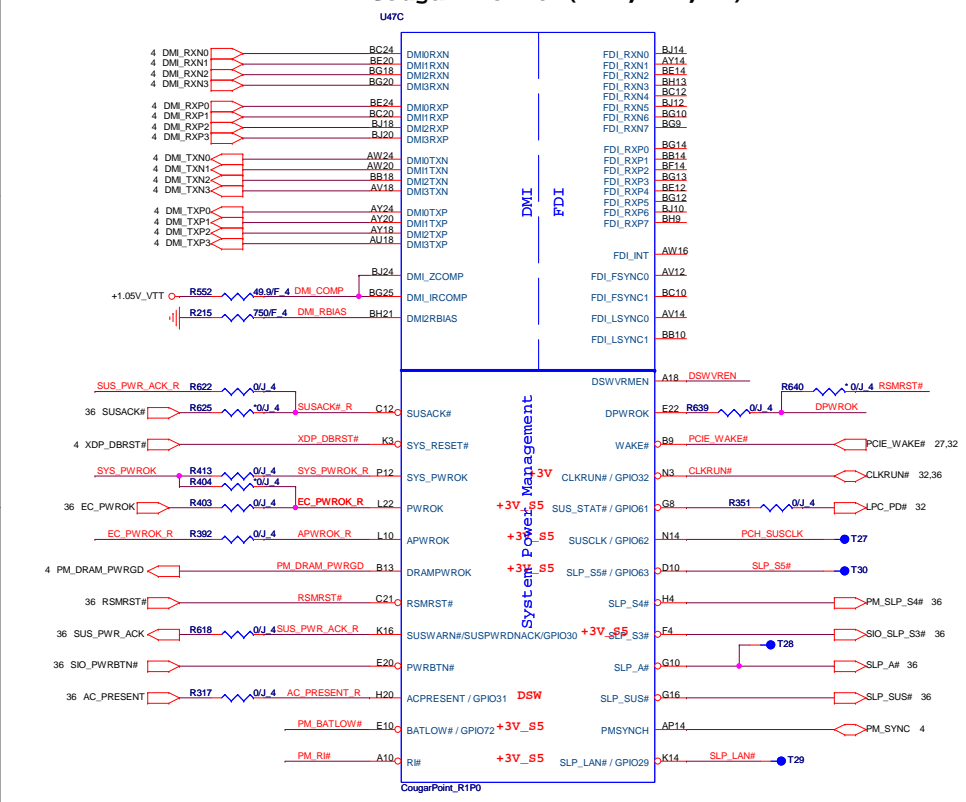
CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

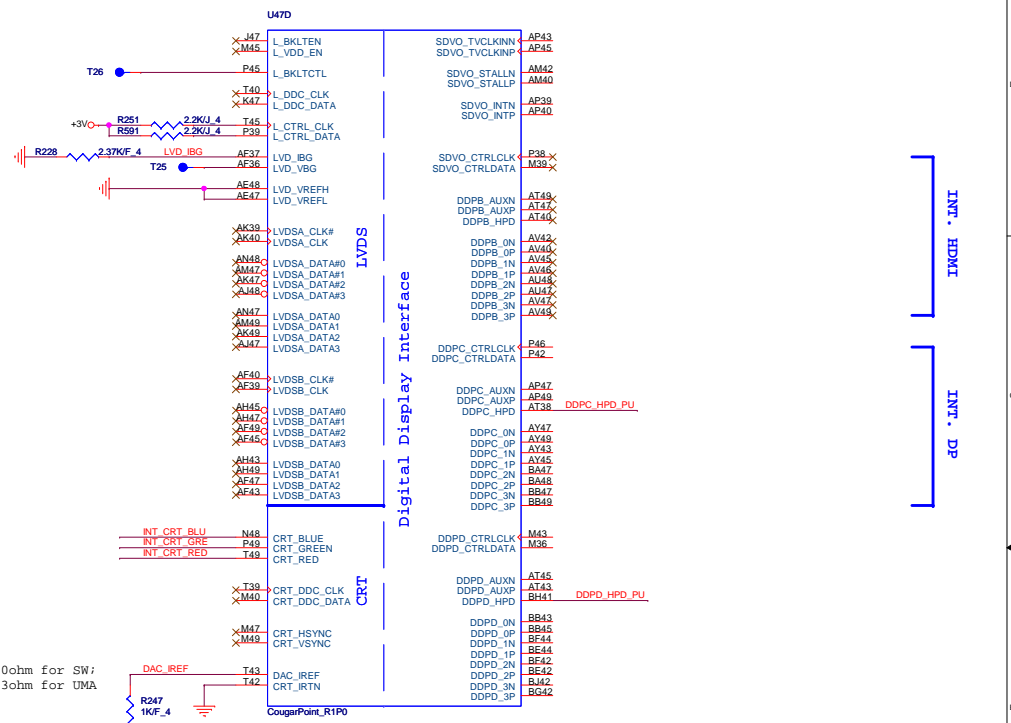
PROJECT : KL2D
Quanta Computer Inc.

Size	Document Number	Rev
	Sandy Bridge 4/4	1A
Date:	Saturday, July 24, 2010	Sheet 7 of 47

Cougar Point (DMI,FDI,PM)



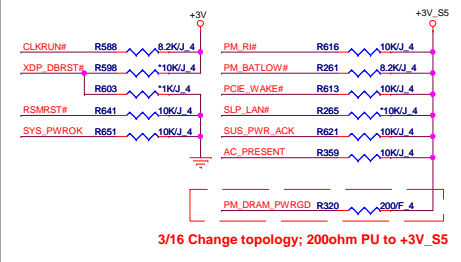
20ohm for SW;
33ohm for UMA



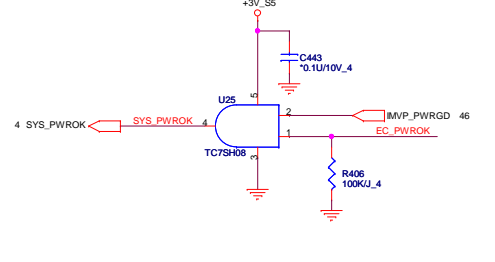
INT. HDMI

INT. DP

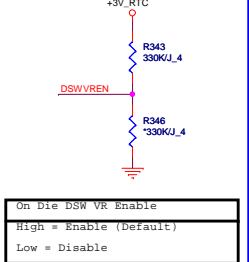
PCH Pull-high/low(CLG)



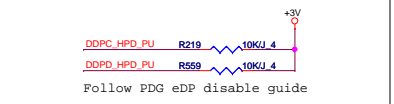
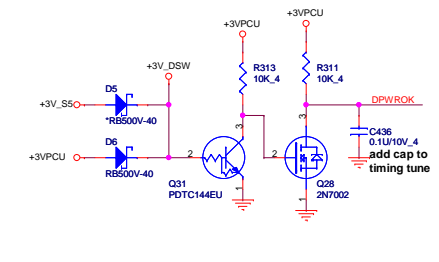
System PWR_OK(CLG)



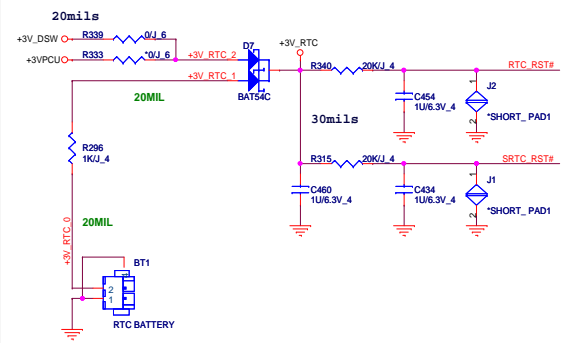
DPWROK FOR DSW



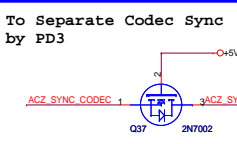
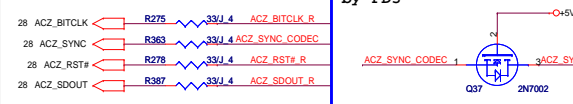
DPWROK FOR DSW



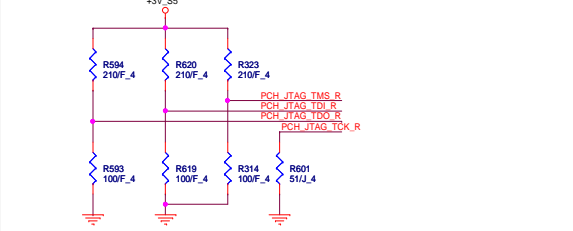
RTC Circuitry(RTC)



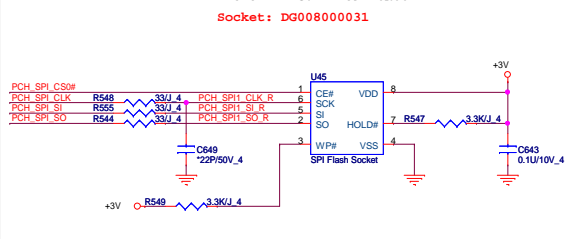
HDA Bus(CLG)



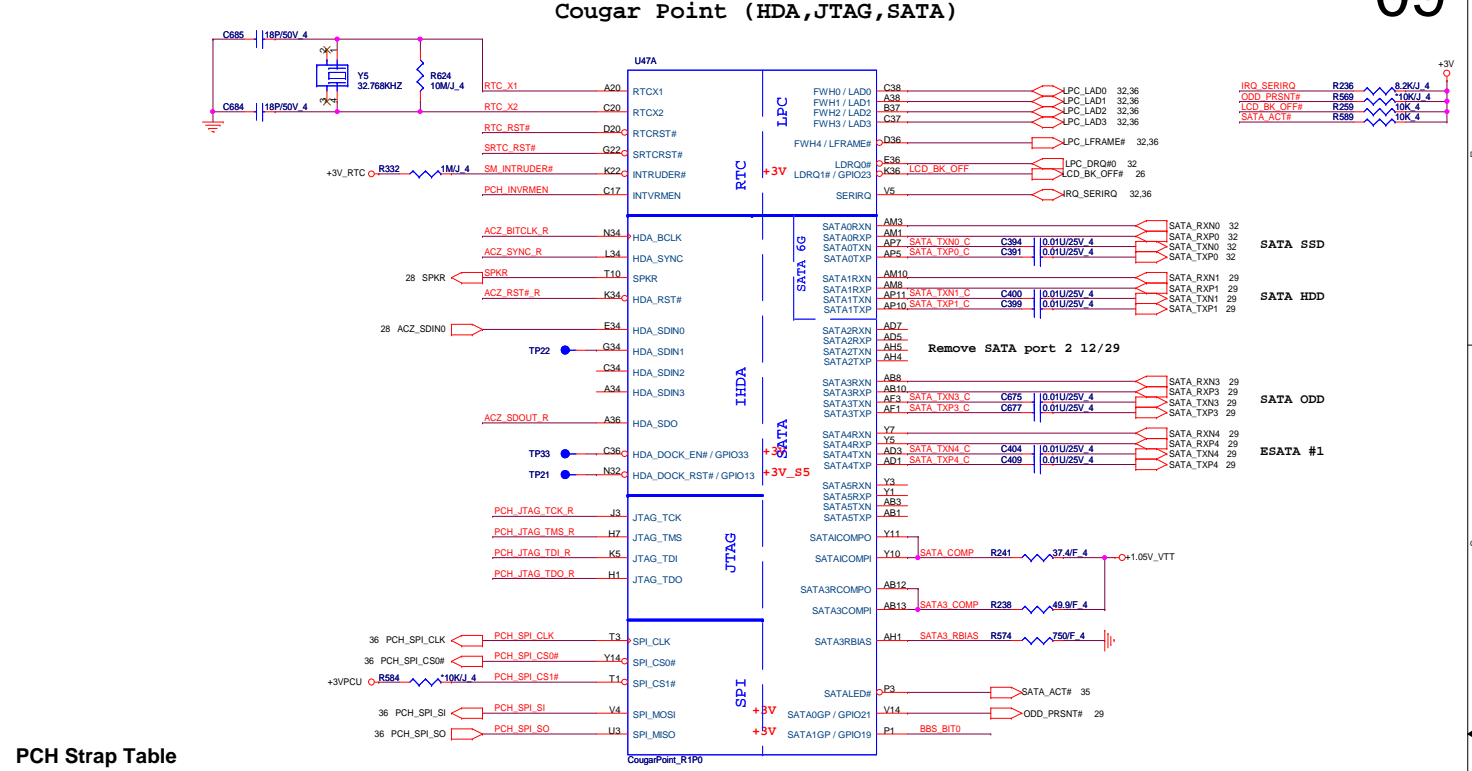
PCH JTAG Debug (CLG)



PCH Dual SPI (CLG)



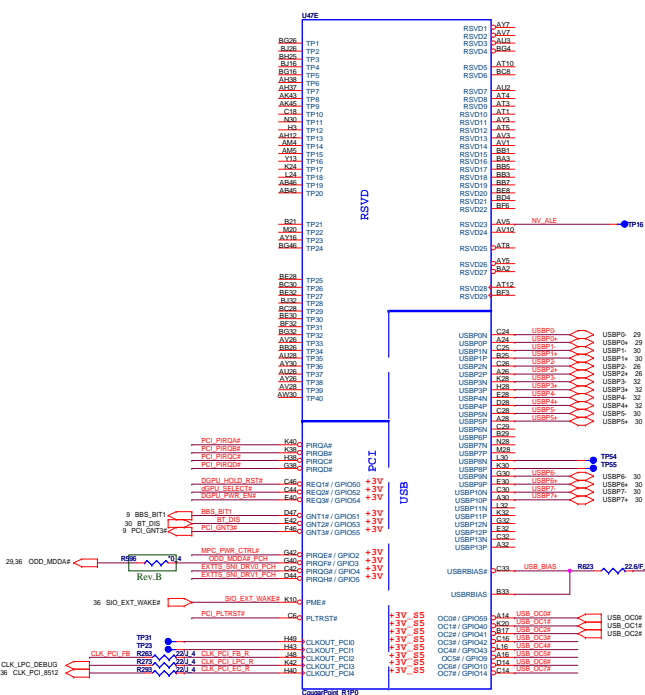
PCH2 (CLG)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V0 - R583 *1KJ_4 SPKR									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R606 *1KJ_4 PCI_GNT3# 10									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC - R312 330KJ_4 PCH_INVRMEN									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>GNT1#</th> <th>GNT0#</th> <th>Boot Location</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>1</td> <td>SPI *</td> </tr> <tr> <td>0</td> <td>0</td> <td>LPC</td> </tr> </tbody> </table>	GNT1#	GNT0#	Boot Location	1	1	SPI *	0	0	LPC	<p>Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]</p> R604 *1KJ_4 BBS_BIT1 10 R590 *1KJ_4 BBS_BIT0
GNT1#	GNT0#	Boot Location											
1	1	SPI *											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK		+3V_S5 - R390 *1KJ_4 ACZ_SDOUT_R									
HDA_SDO	Flash Descriptor Security	RSMRST	0 = Override 1 = Default (weak pull-up 20K)	+3V_S5 - R390 *1KJ_4 ACZ_SDOUT_R									
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R566 *2.2KJ_4 -O+1.8V R570 *3.7KJ_4 DF_TVS 11 H_SNB_IVB# 4									
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R394 *1KJ_4 PLL_ODVR_EN 11,36									
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V_S5 - R355 *1KJ_4 ACZ_SYNC_R									
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)										
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	+3V0 - R554 *1KJ_4 PCH_SPI_SI									
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)										

Cougar Point-M (PCI,USB,NVRAM)



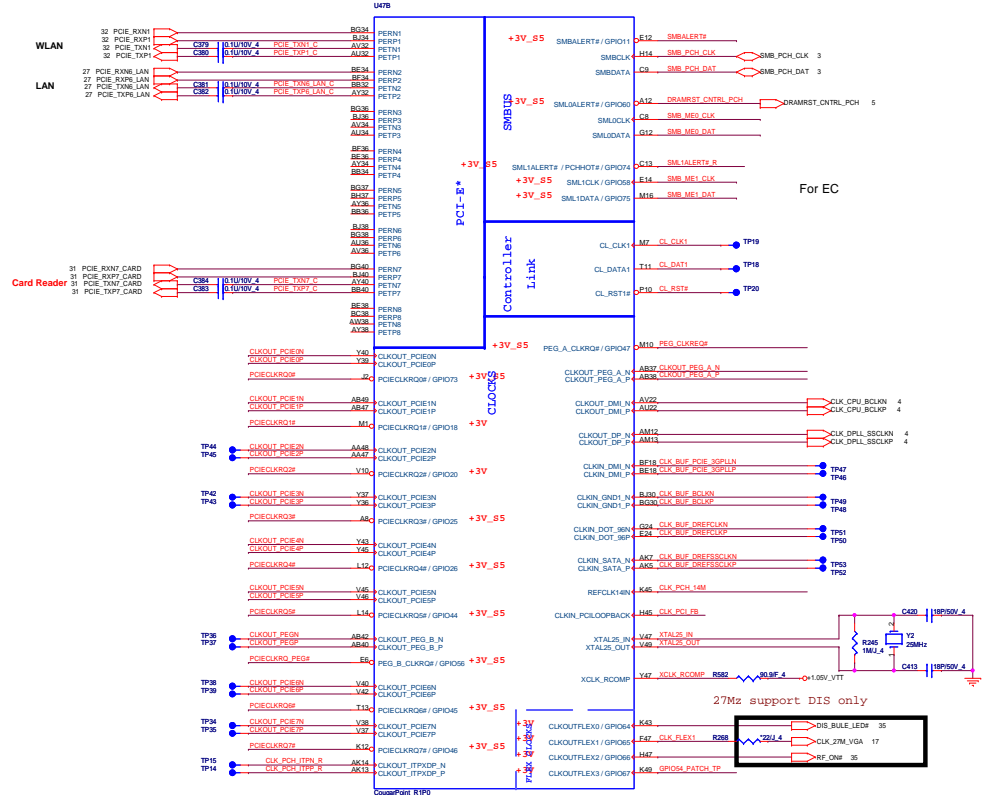
BlueTooth
USB/eSATA Combo #1
CCD on LVDS
WLAN
WWAN
USB #1

USB #2
USB #3

EHC1

EHC2

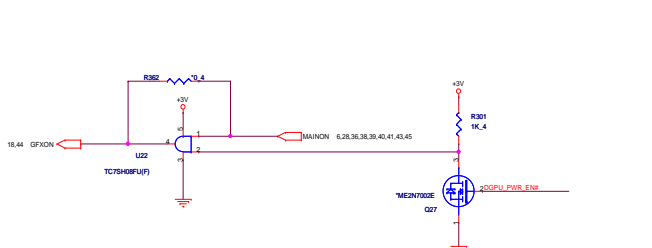
Cougar Point-M (PCI-E, SMBUS, CLK)



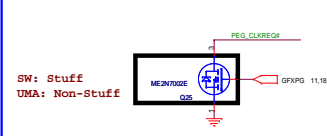
For EC

27Mz support DIS only

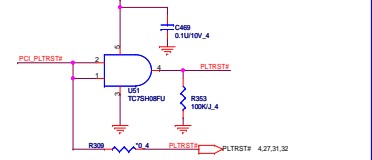
DGPU Power ON



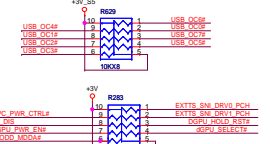
PEG CLK detect



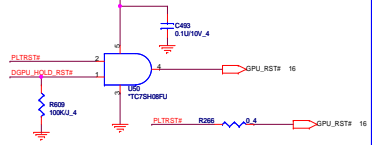
PLTRST#(CLG)



PCI/USB0# Pull-up(CLG)



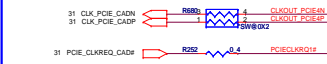
GPU RST#(CLG)



WLAN



LAN



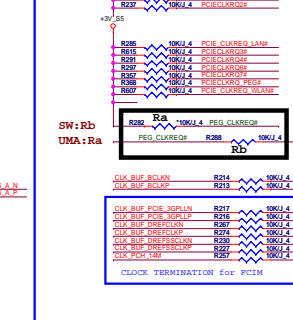
Card Reader



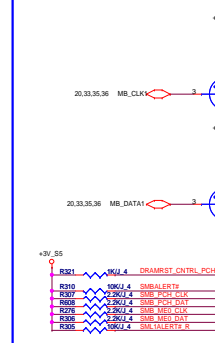
SW:Stuff



CLK_REQ/Strap Pin(CLG)

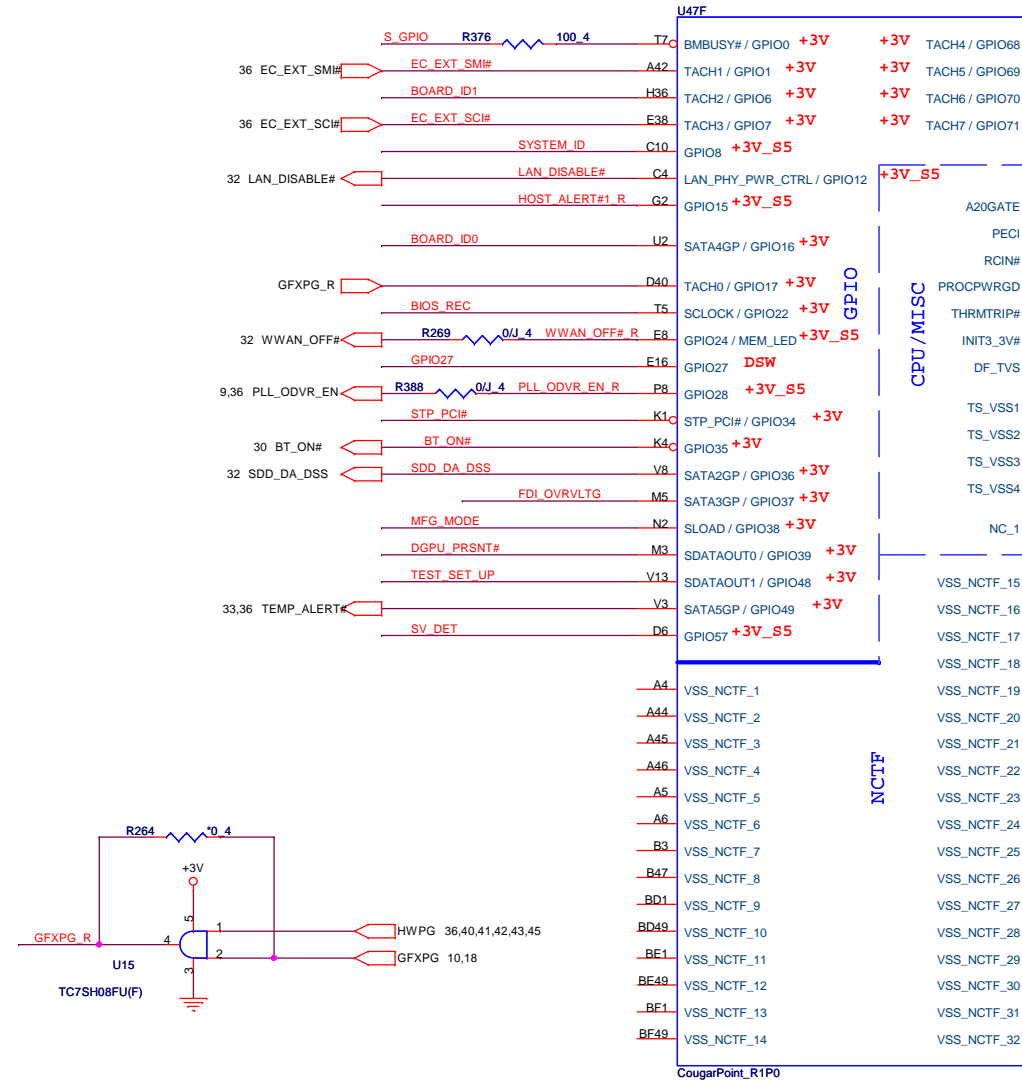


SMBus/Pull-up(CLG)

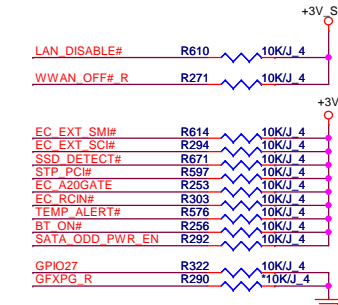


PROJECT : KL2D
 Quanta Computer Inc.
 Document Number: Cougar Point 3/6
 Date: Saturday, July 24, 2010
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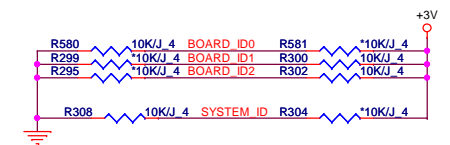
Cougar Point (GPIO,VSS_NCTF,RSVD)



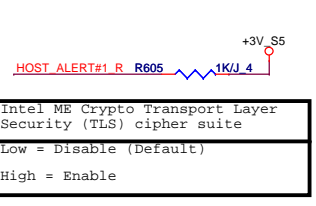
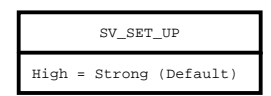
GPIO Pull-up/Pull-down(CLG)



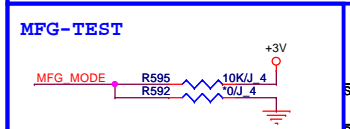
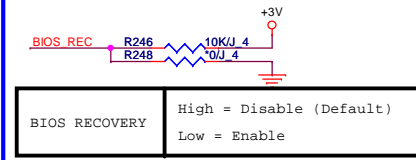
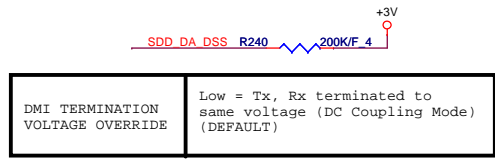
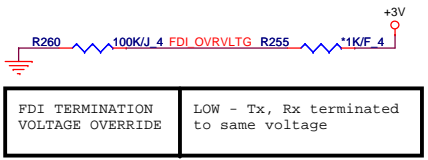
Model	BOARD_ID2	BOARD_ID1	BOARD_ID0
Reserve	0	0	0
UMA	0	0	1
Muxless	0	1	0
Discrete	0	1	1
Reserve	1	0	0
Reserve	1	0	1
Reserve	1	1	0



3/16 Connected to GND
DG rev0.9



	SWITCHABLE	UMA
Stuff	R8489	R8490
No Stuff	R8490	R8489



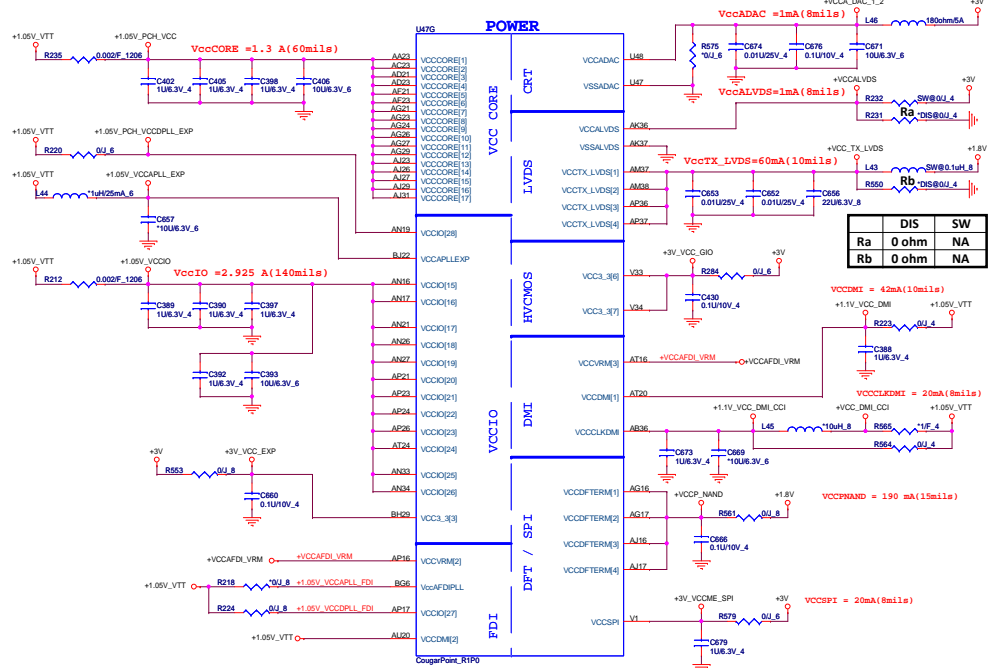
PROJECT : KL2D
Quanta Computer Inc.

Size: _____ Document Number: _____ Rev: 1A

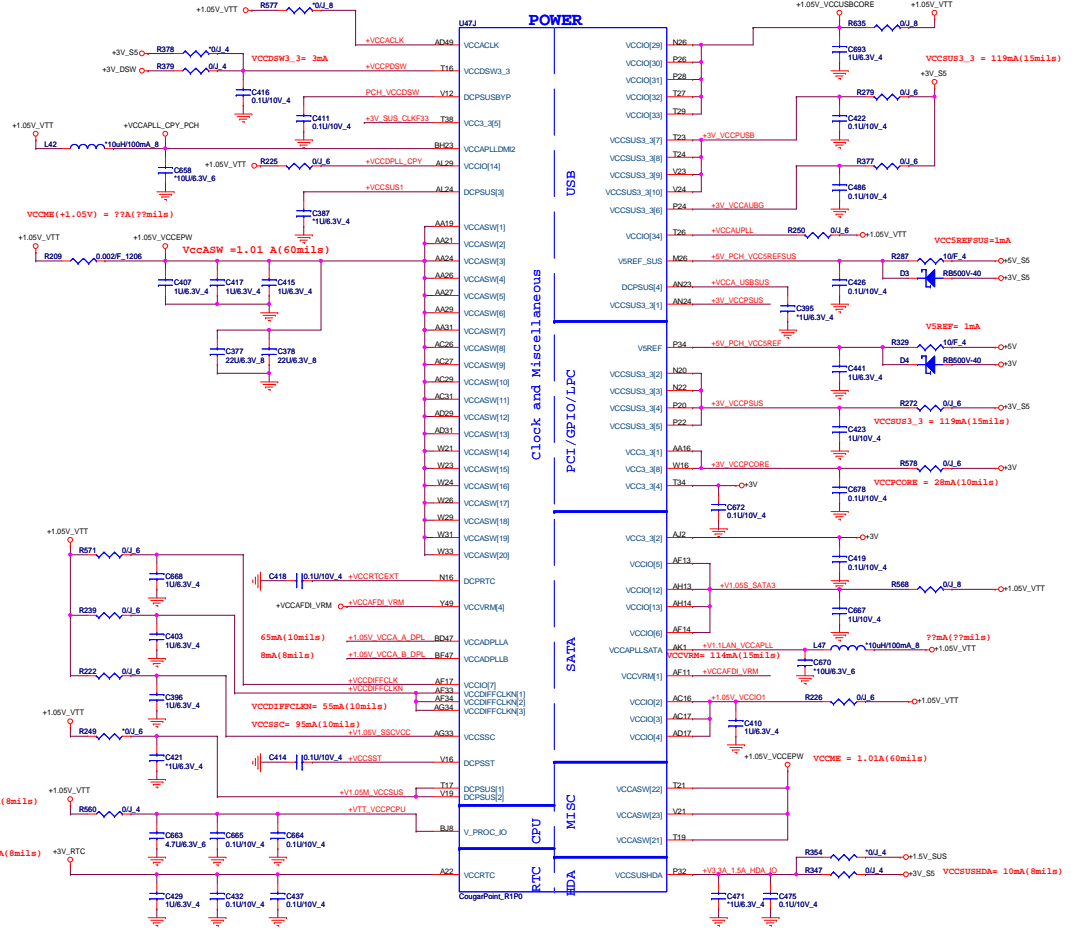
Cougar Point 4/6

Date: Saturday, July 24, 2010 Sheet 11 of 47

COUGAR POINT (POWER)

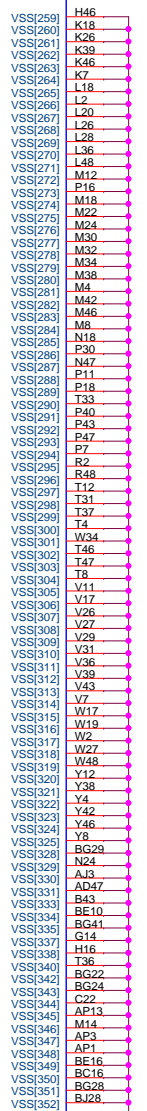
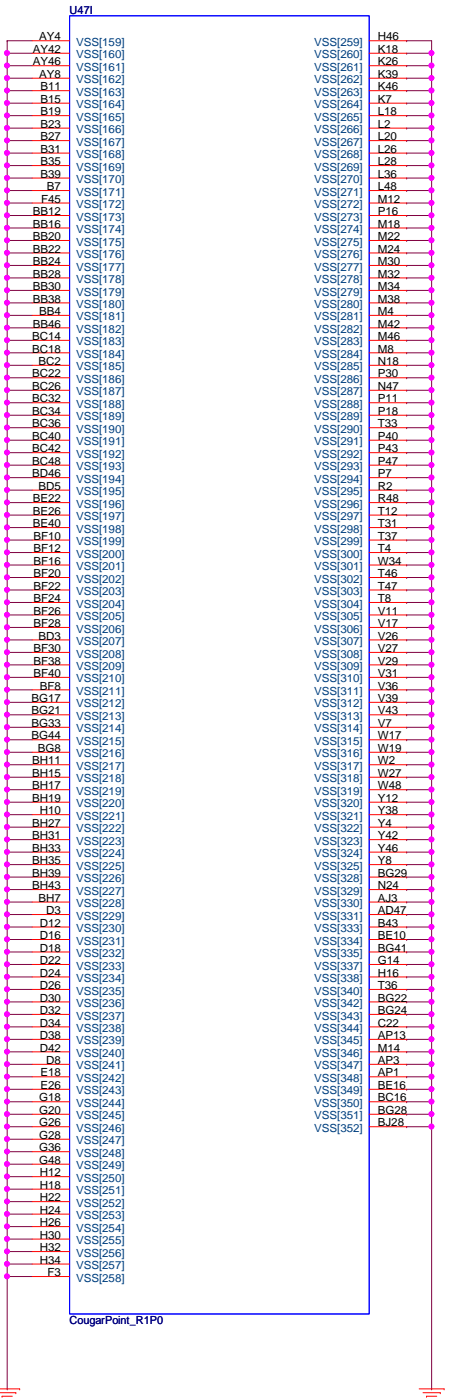
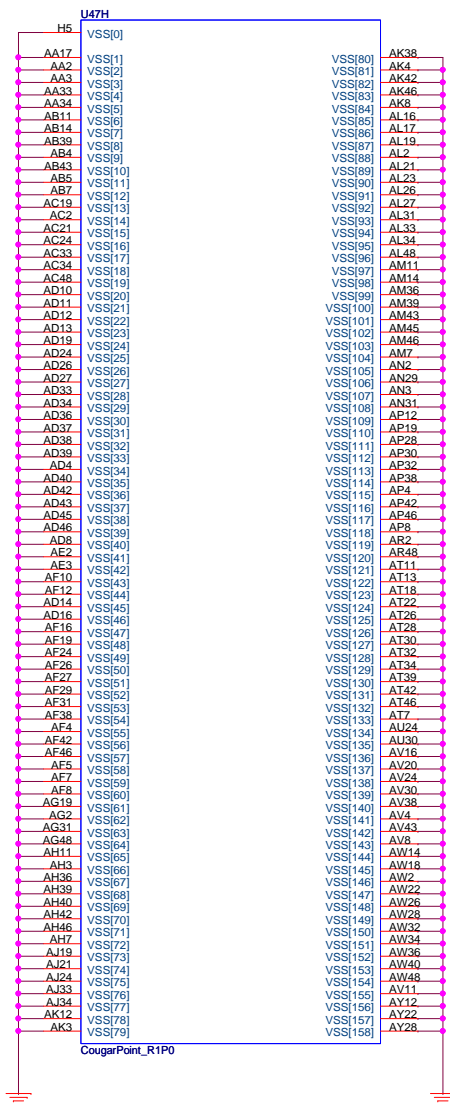


Cougar Point-M (POWER)



VCCVDM[1] = 1.8V (Desktop) 1.5V (Mobile) 20 dsl for Pre-ES1

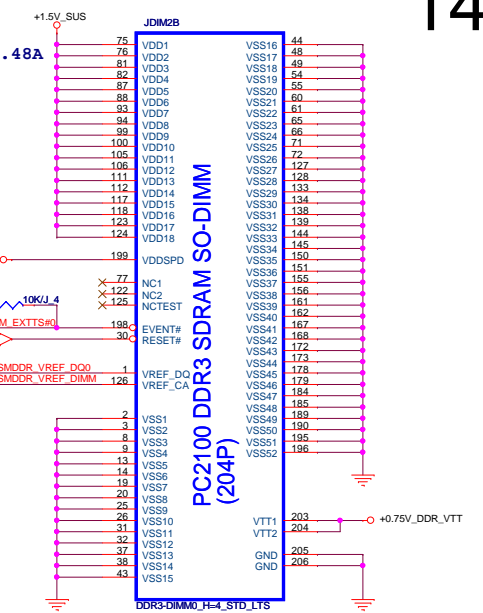
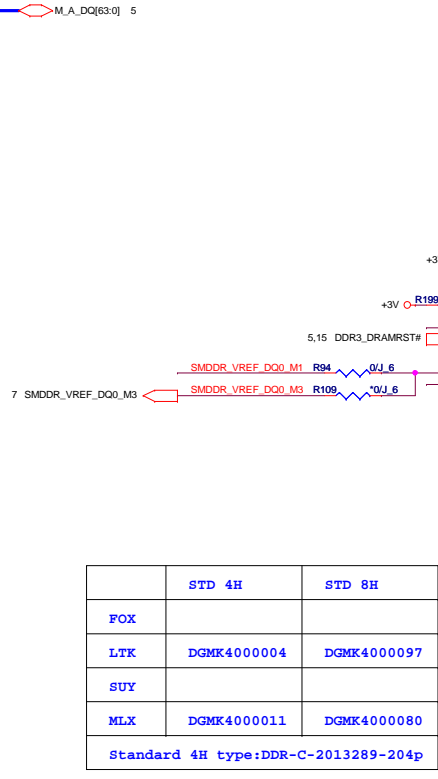
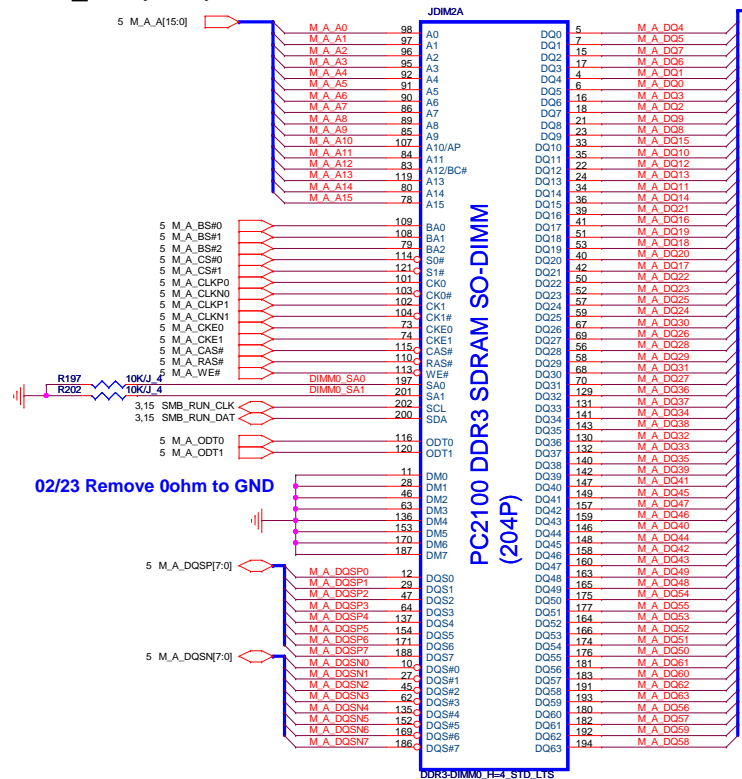
IBEX PEAK-M (GND)



PROJECT : KL2D
Quanta Computer Inc.

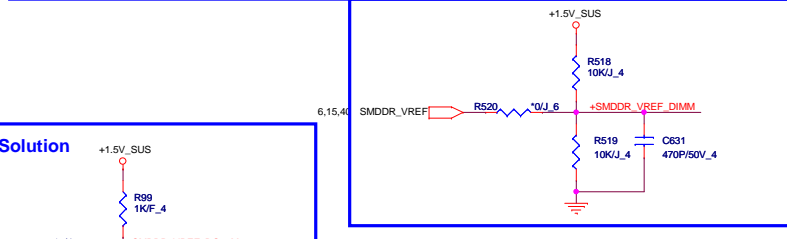
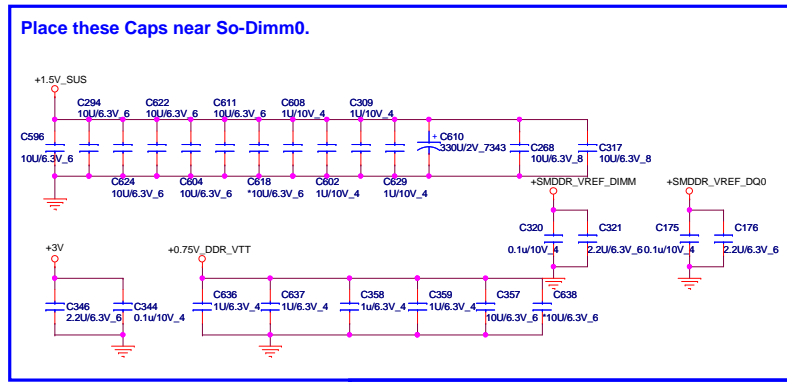
Size Document Number Rev
Cougar Point 6/6 1A

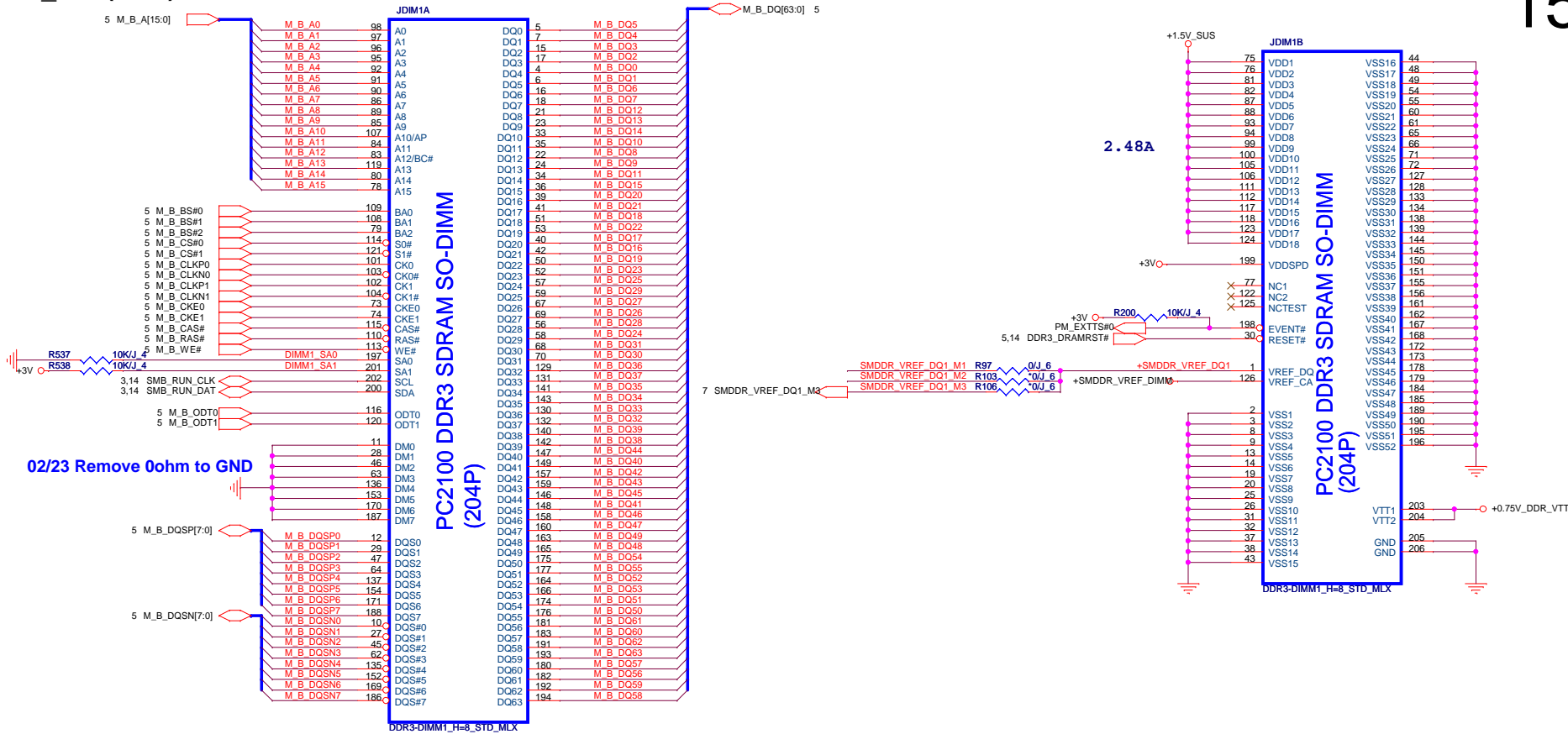
Date: Saturday, July 24, 2010 Sheet 13 of 47



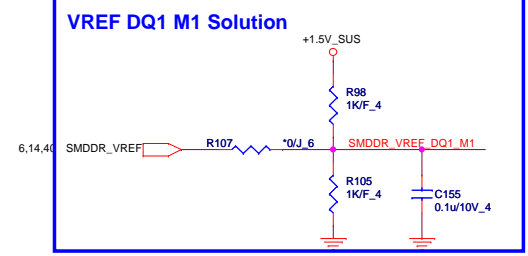
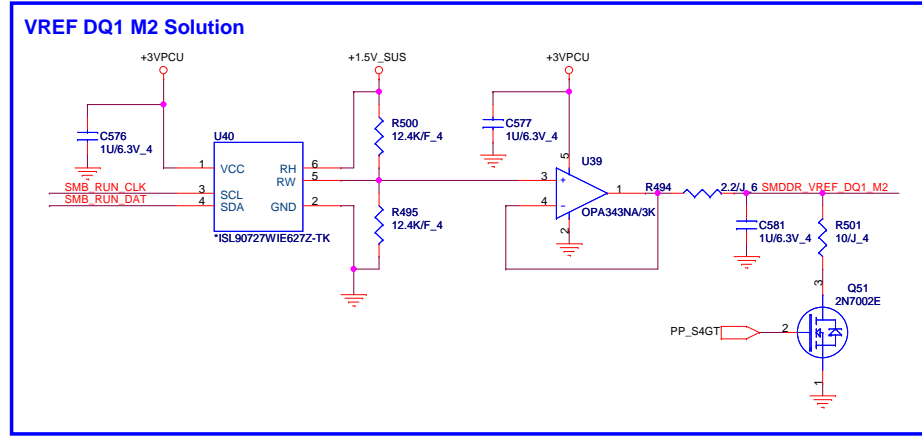
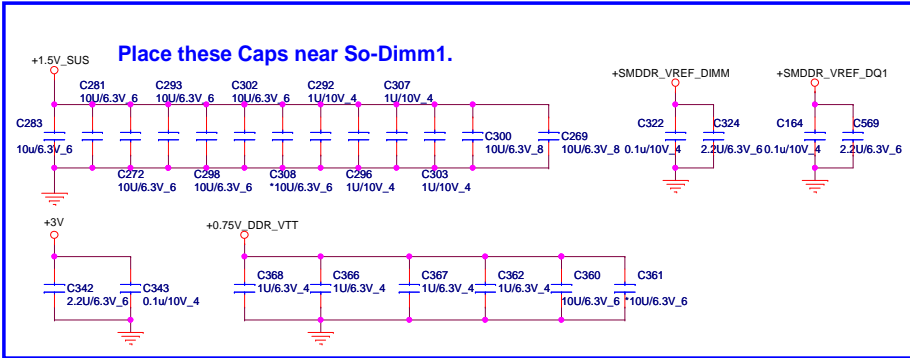
	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080

Standard 4H type:DDR-C-2013289-204p





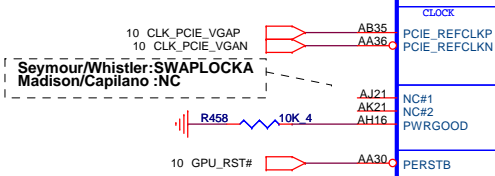
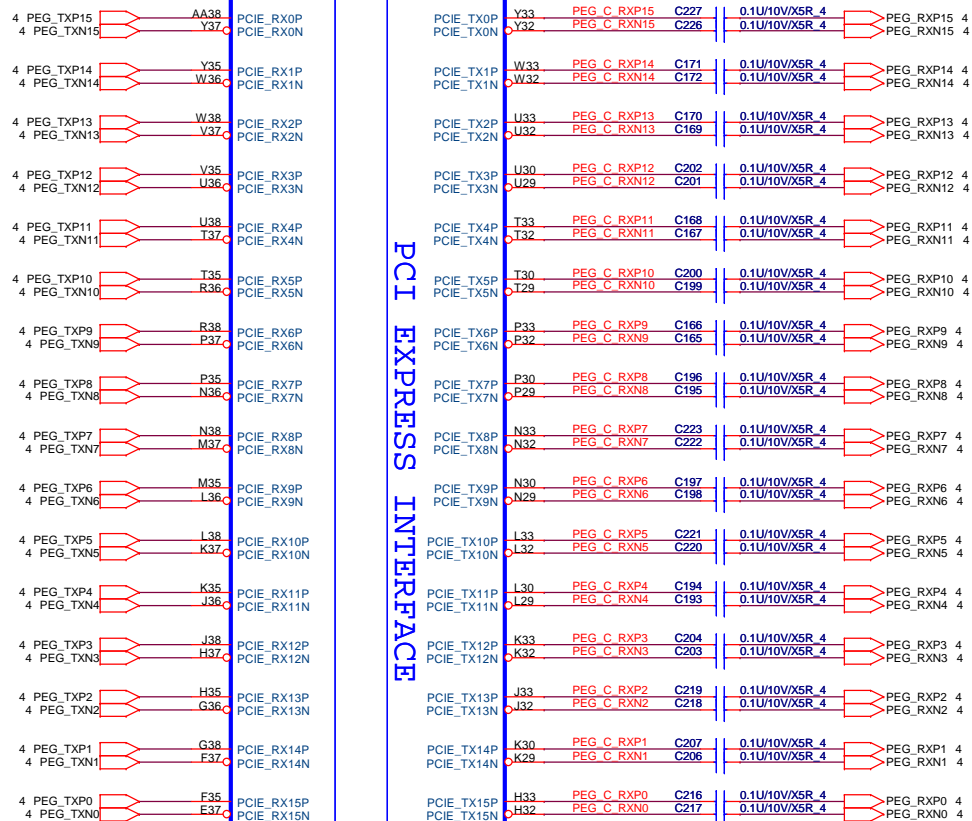
02/23 Remove 0ohm to GND



	STD 4H	STD 8H
FOX		
LTK	DGMK4000004	DGMK4000097
SUY		
MLX	DGMK4000011	DGMK4000080
Standard 8H type:DDR-C-2013310-204p-1		

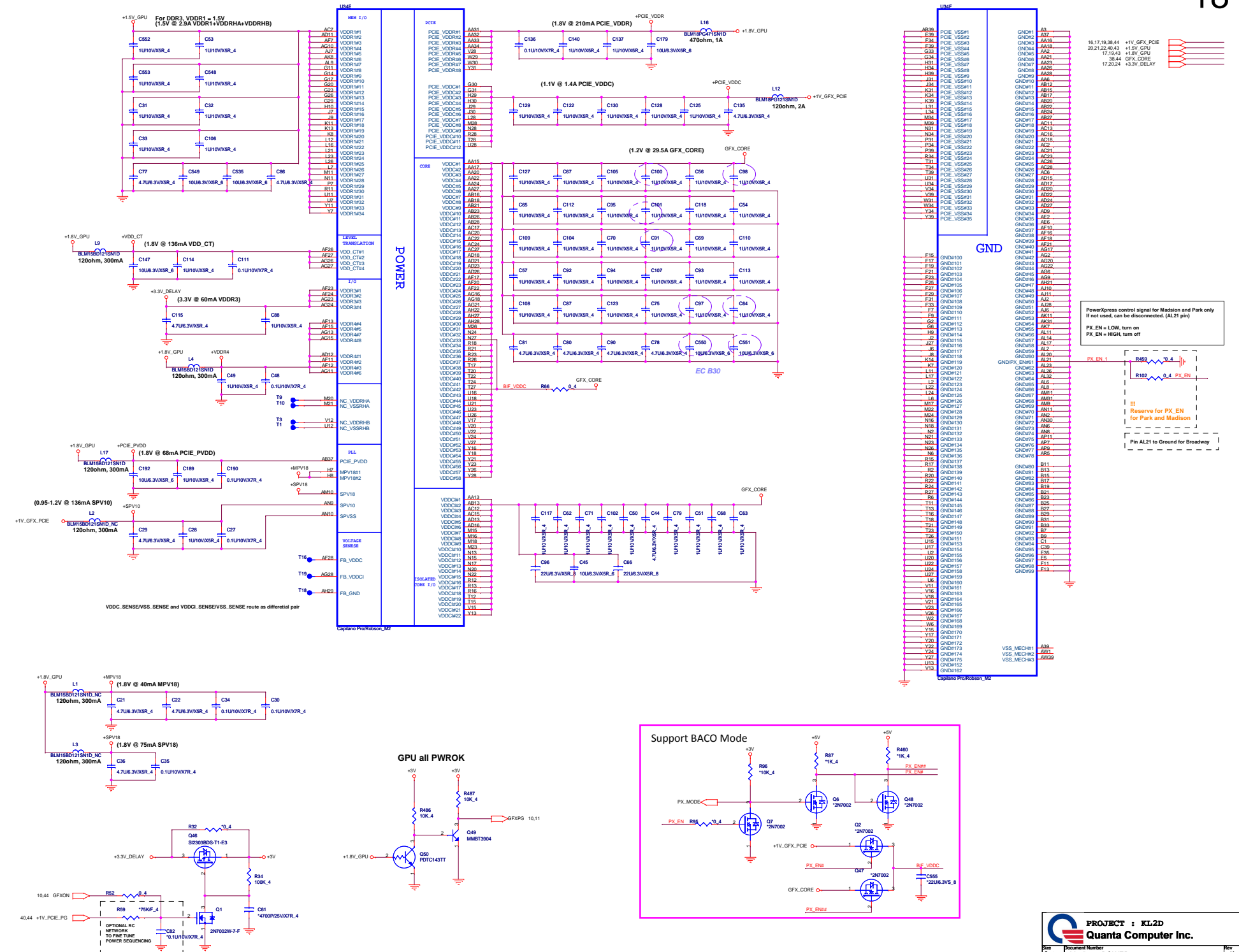
U34A

PCI EXPRESS INTERFACE



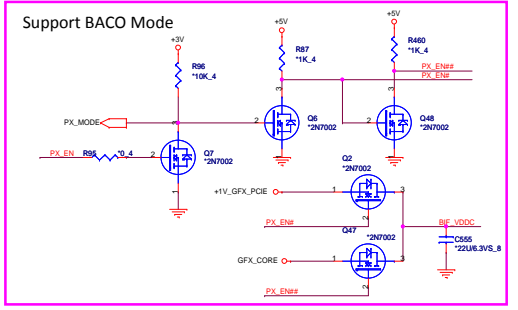
Capilano Pro/Robson_M2



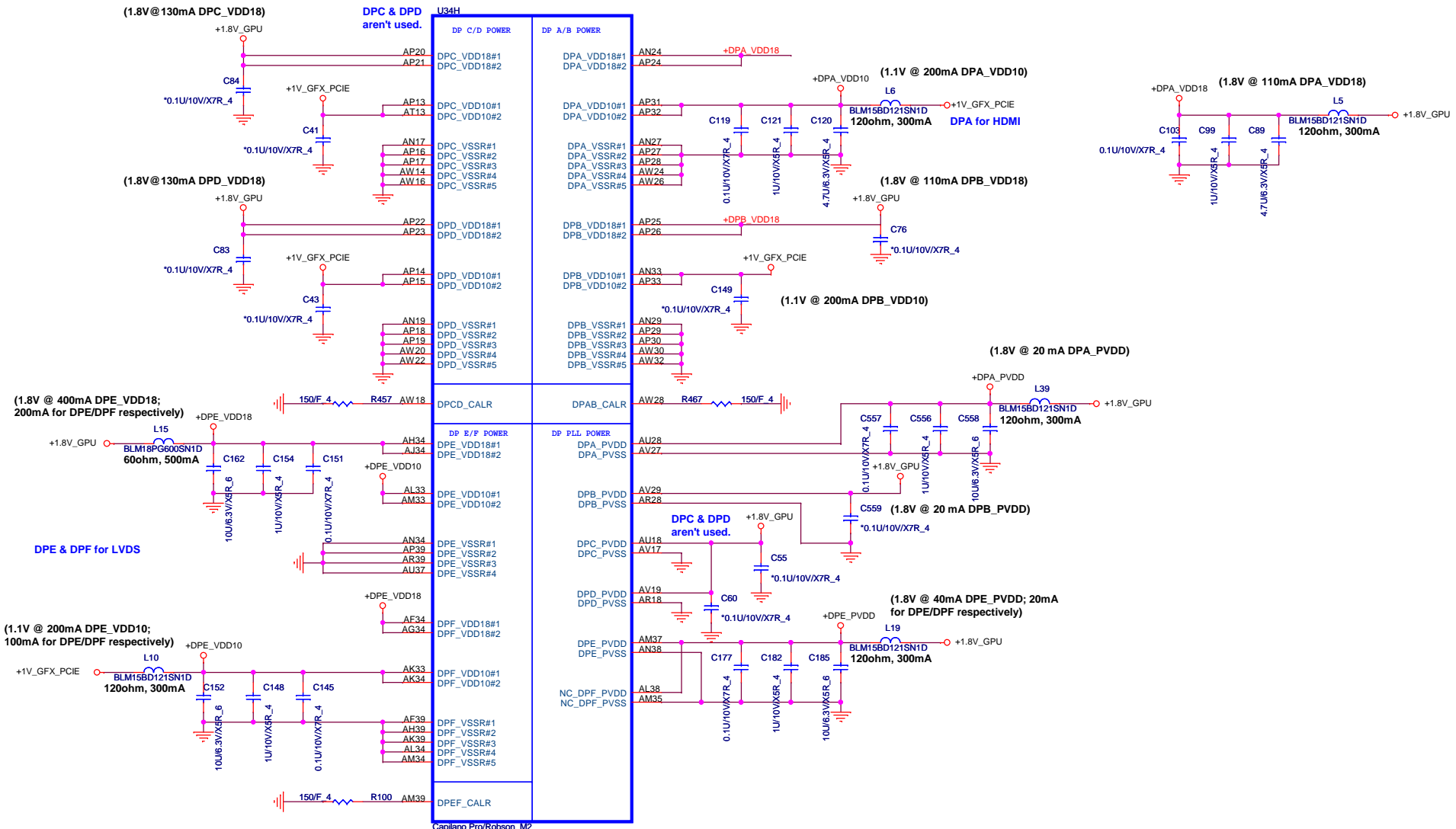


PowerXpress control signal for Madison and Park only
 If not used, can be disconnected. (AL21 pin)
 PX_EN = LOW, turn on
 PX_EN = HIGH, turn off

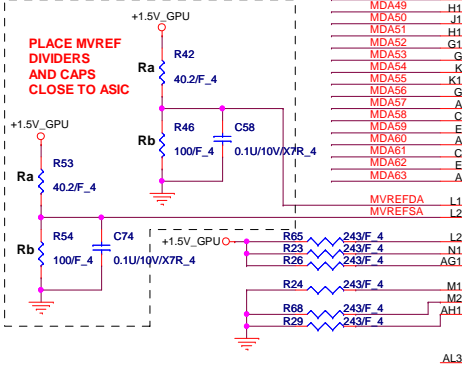
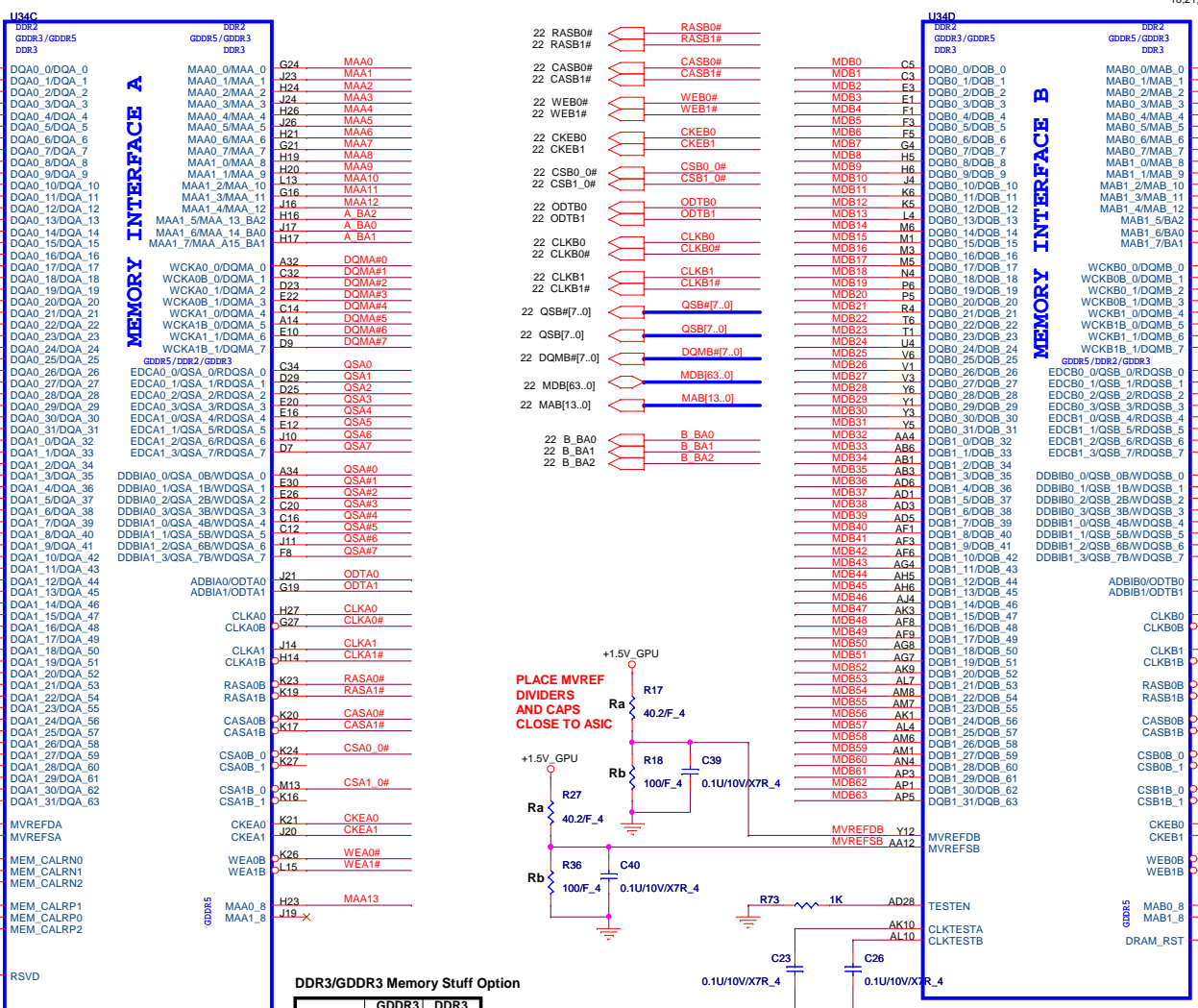
Reserve for PX_EN for Park and Madison
 Pin AL21 to Ground for Broadway



!!!
For M96/92, DPx_VDD10 = 1.1V
For M97 DPx_VDD10 = 1.0V



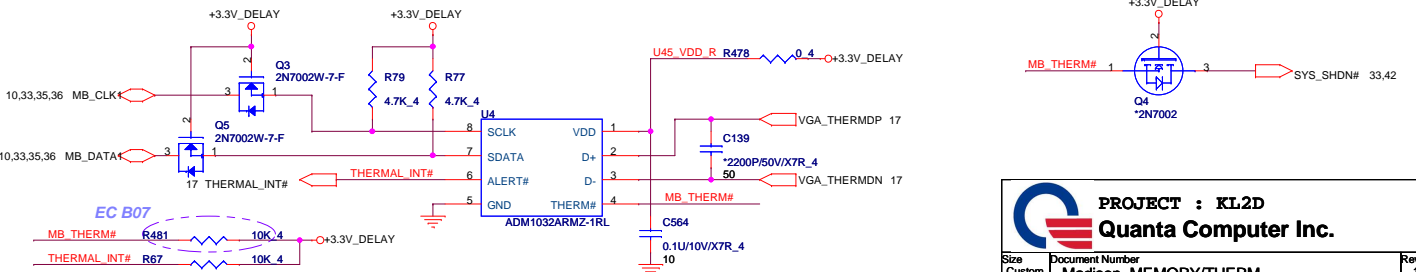
Capilano Pro/Robson_M2



DDR3/GDDR3 Memory Stuff Option

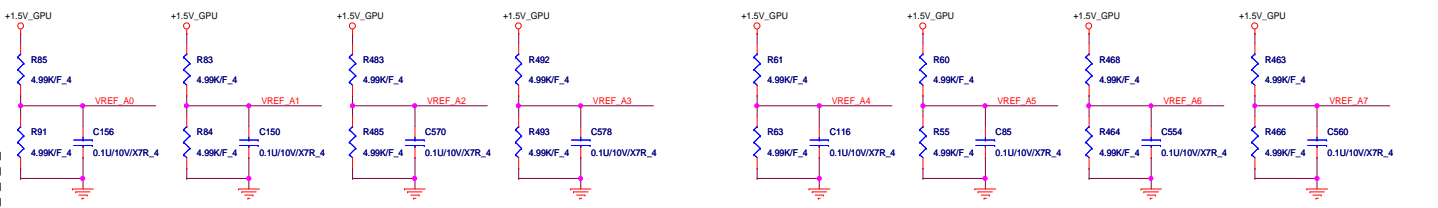
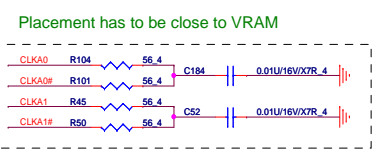
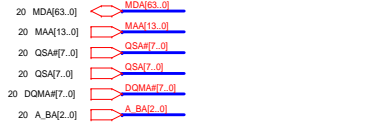
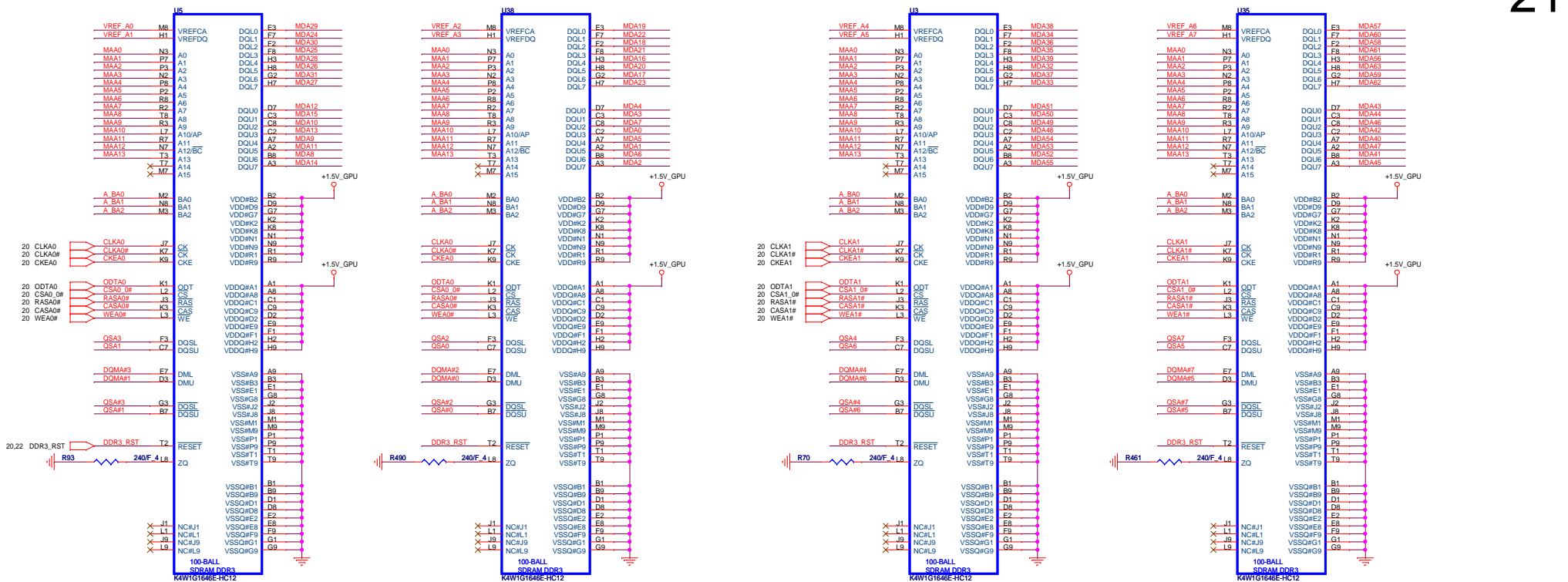
	GDDR3	DDR3
MVDDQ	1.8V	1.5V
Ra	40.2R	100R
Rb	100R	100R

THERMAL MONITOR

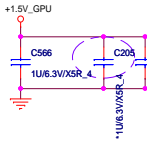


PROJECT : KL2D
Quanta Computer Inc.

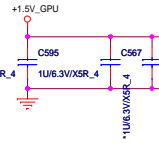
Size: Custom
 Document Number: Madison_MEMORY/THERM
 Date: Saturday, July 24, 2010
 Sheet: 20 of 47
 Rev: 1A



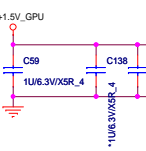
Close to U4



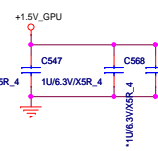
Close to U44



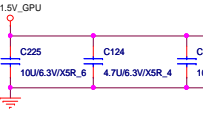
Close to U3



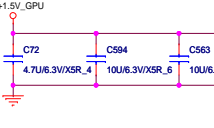
Close to U41



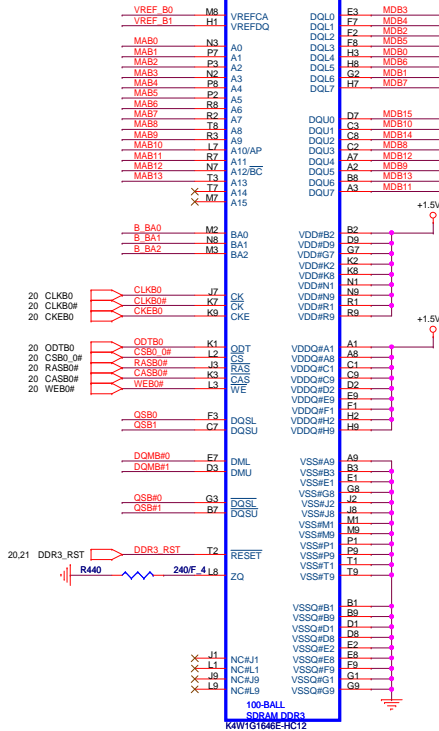
Close to U4 & U44



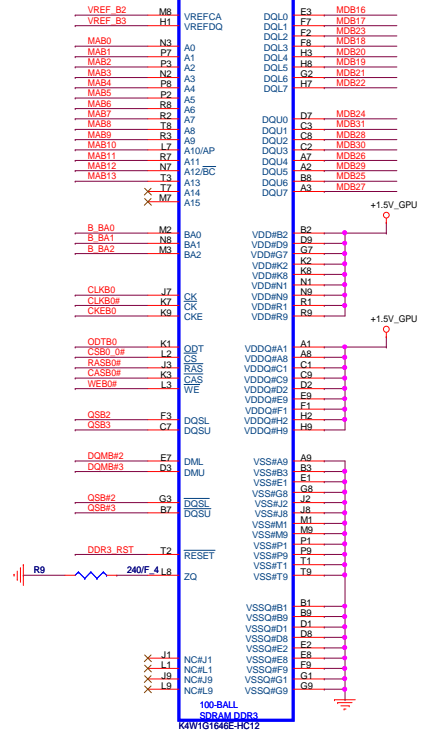
Close to U3 & U41



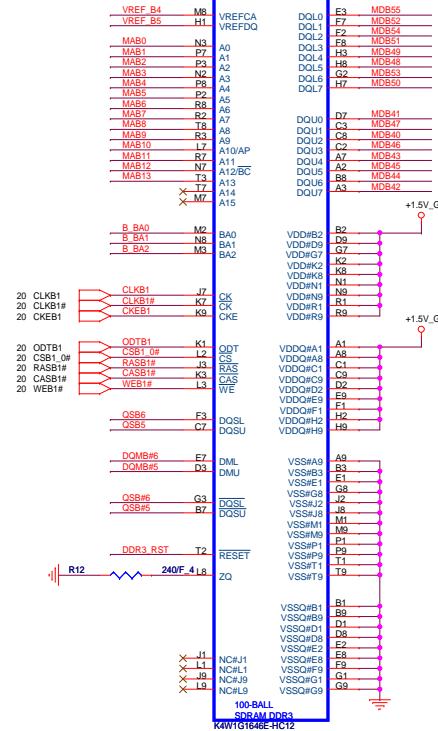
U30



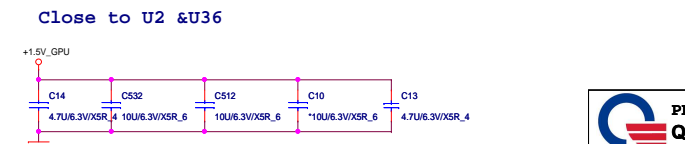
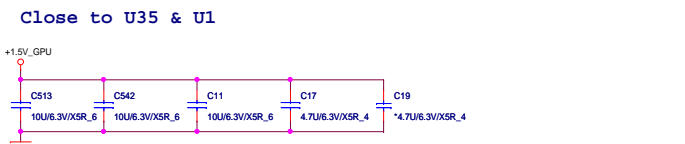
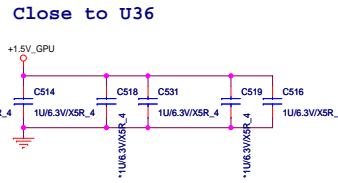
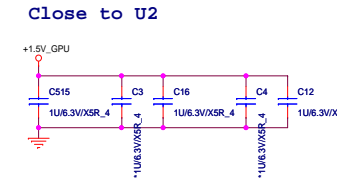
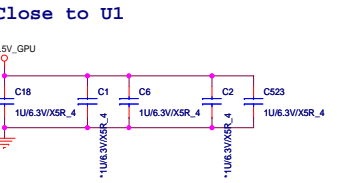
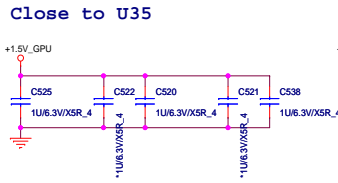
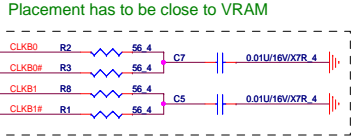
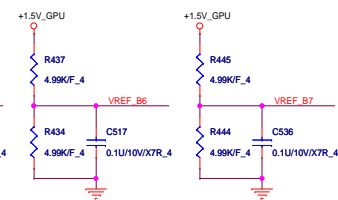
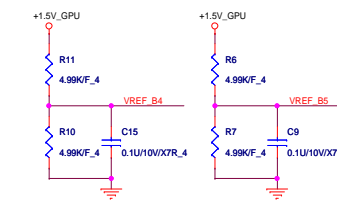
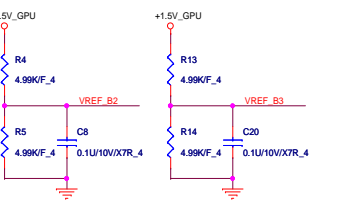
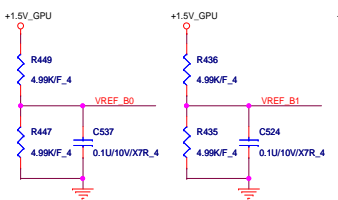
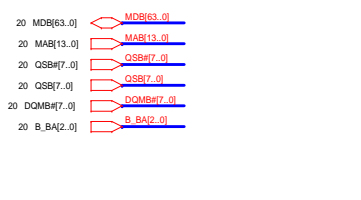
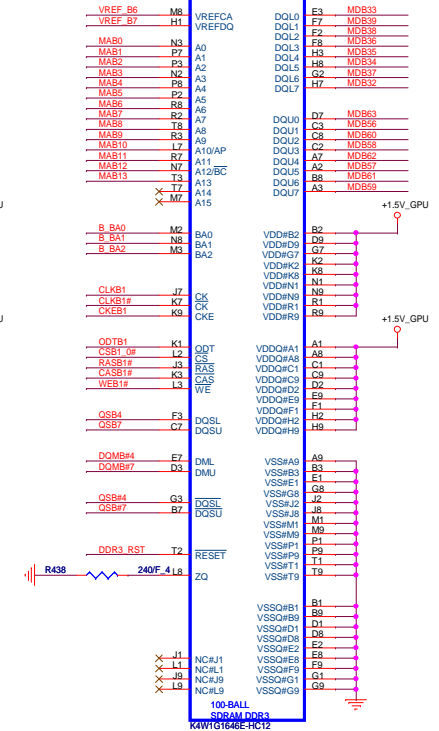
U1



U2



U29



Placement has to be close to VRAM

Close to U35

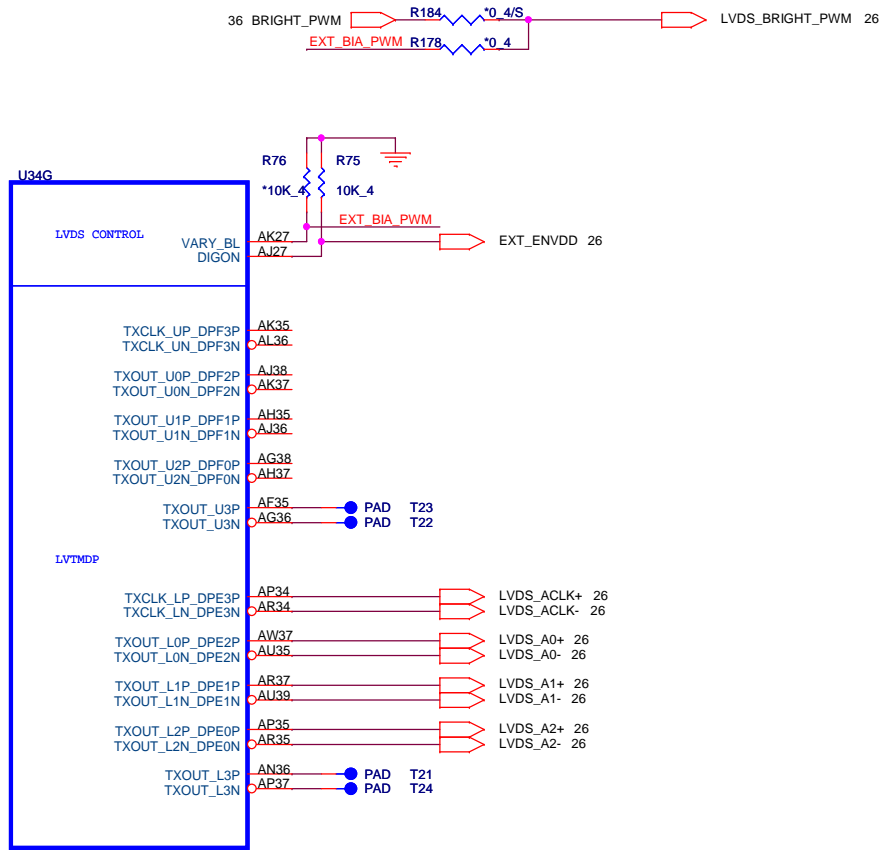
Close to U1

Close to U2

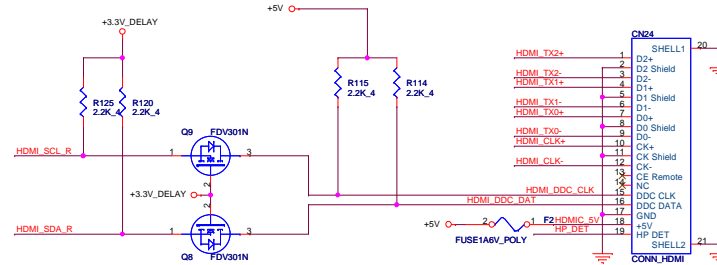
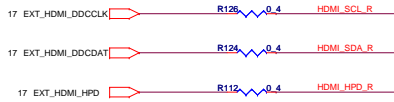
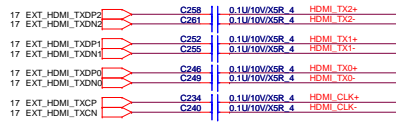
Close to U36

Close to U35 & U1

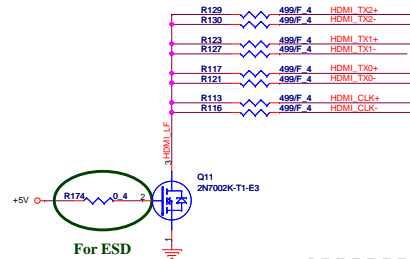
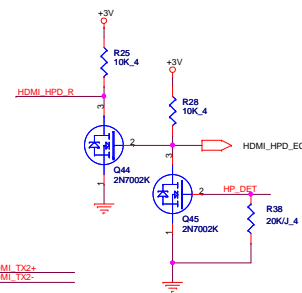
Close to U2 & U36



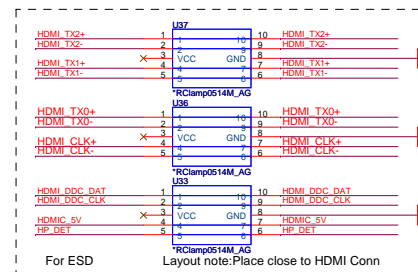
Capilano Pro/Robson_M2



HDMI Hot-PLUG to EC and GPU



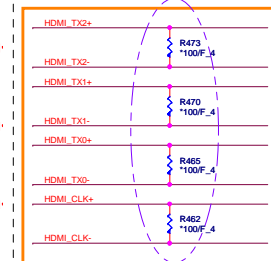
For ESD



For ESD

Layout note: Place close to HDMI Conn

EMI reserve for HDMI



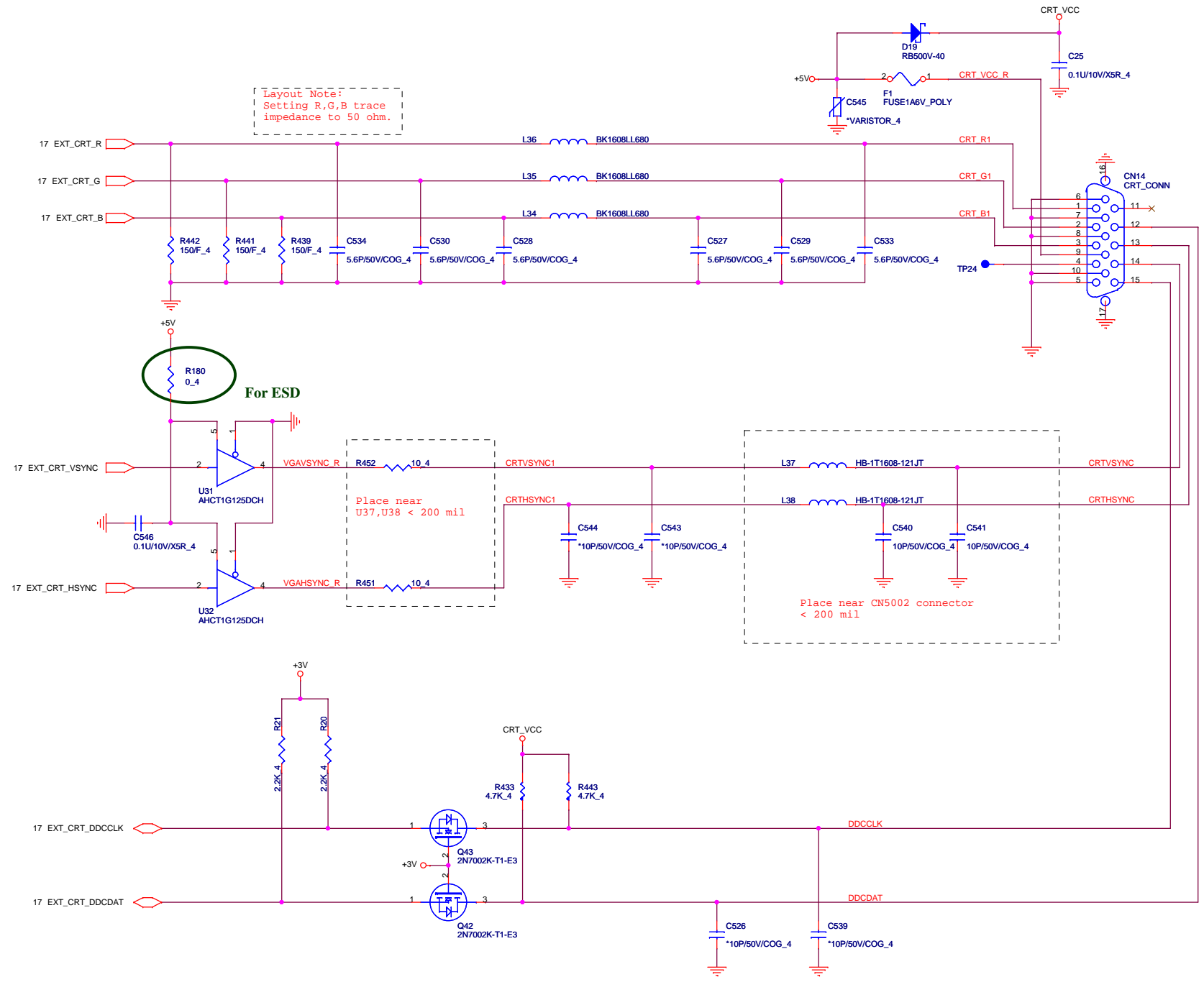
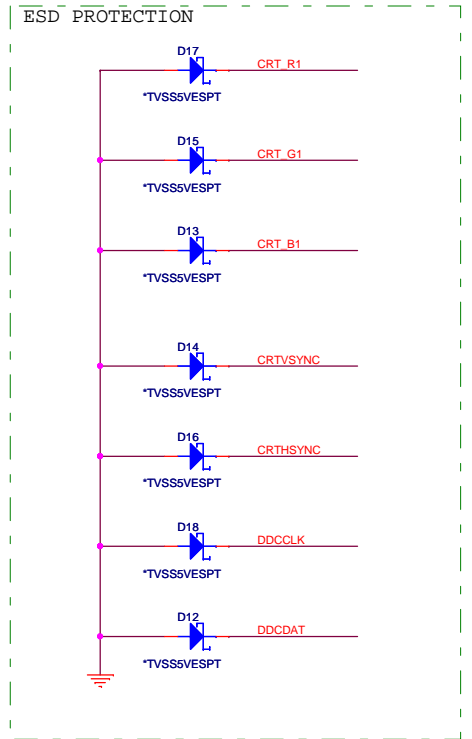
UMA Only / Muxless HDMI

Layout Note:
Setting R,G,B trace impedance to 50 ohm.

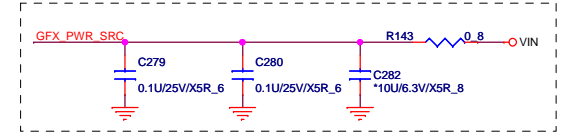
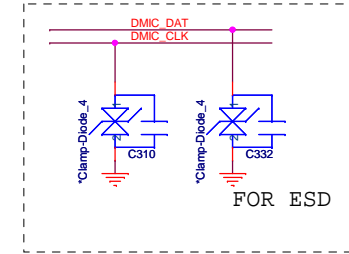
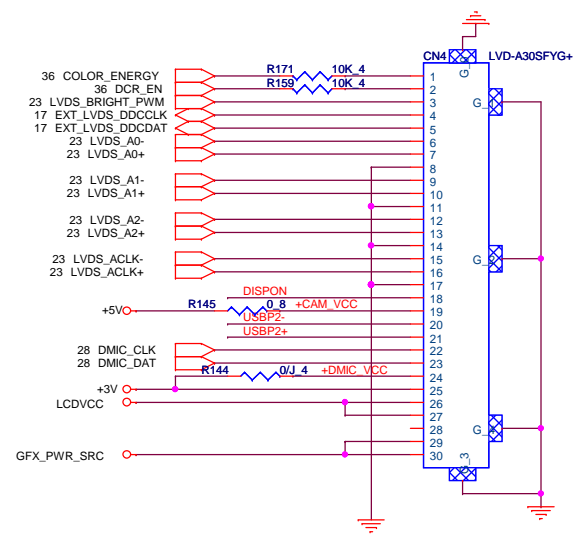
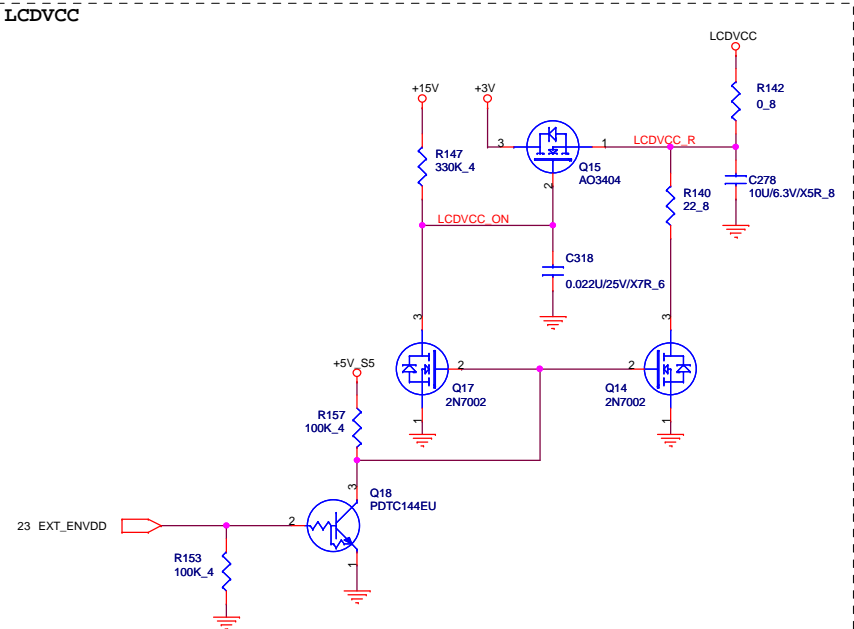
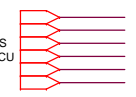
For ESD
R180
0_4

Place near U37,U38 < 200 mil

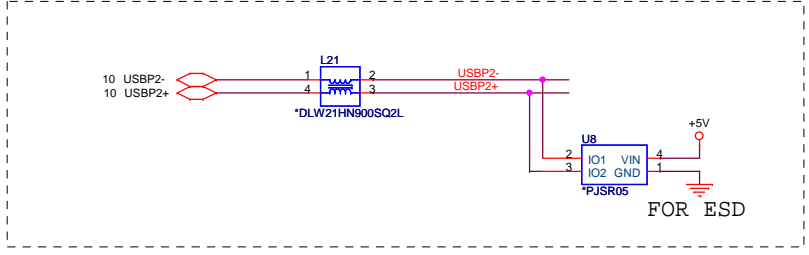
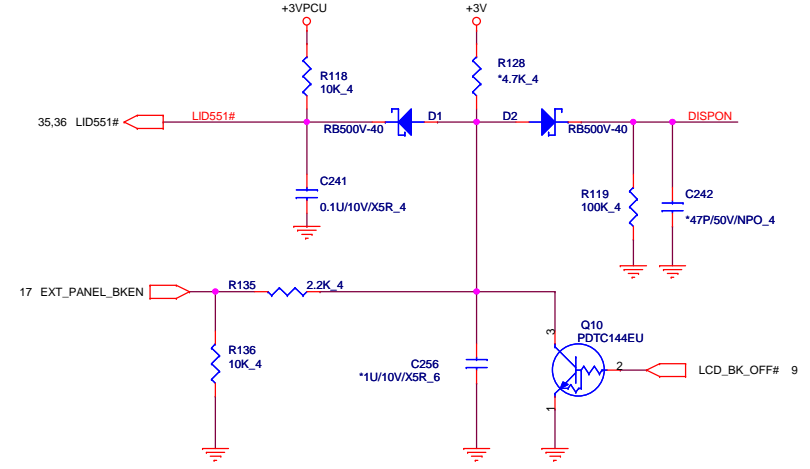
Place near CN5002 connector < 200 mil

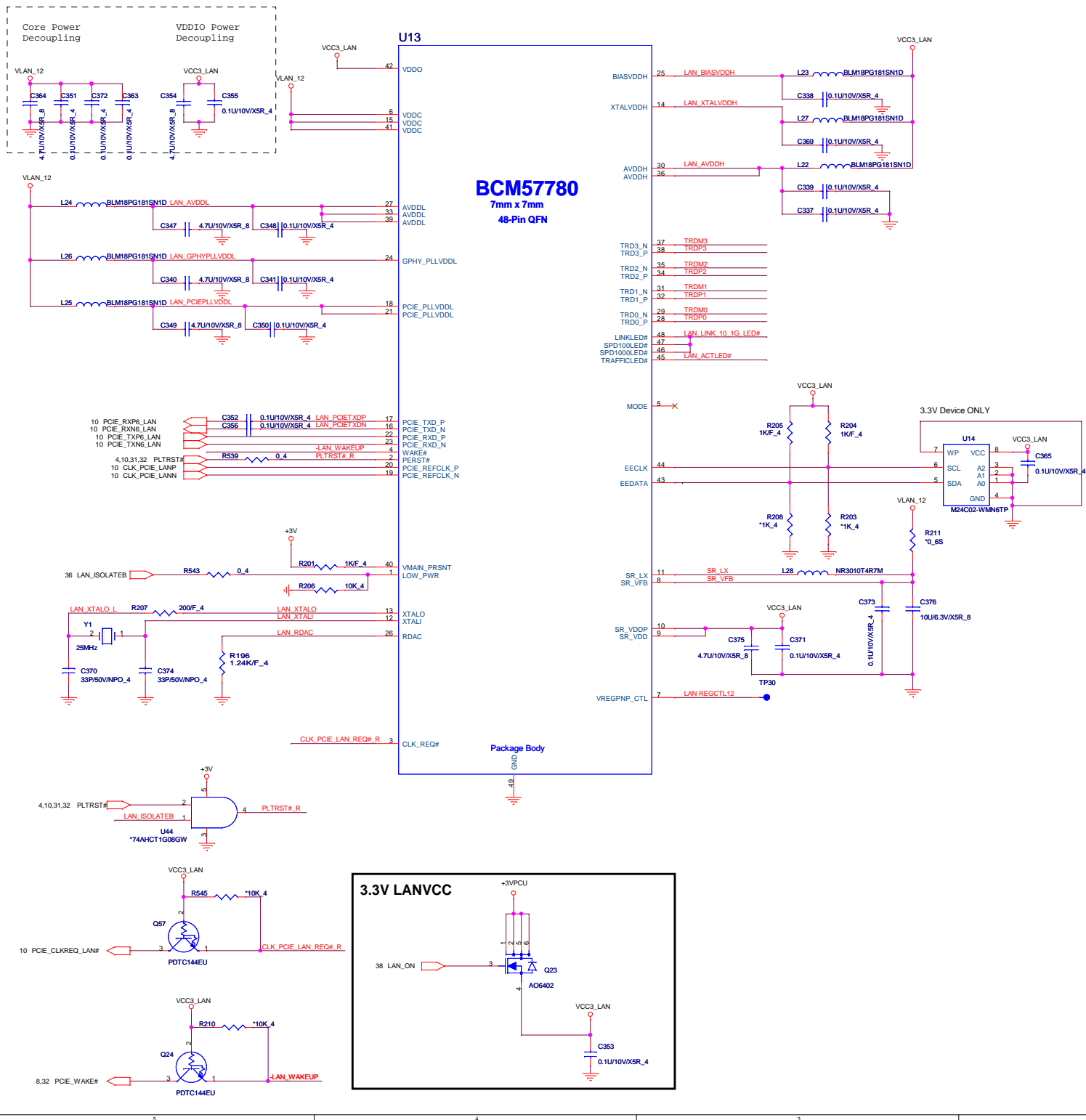


3,4,8,9,10,11,12,14,15,18,24,25,27,28,29,30,31,32,33,34,35,36,38,39,43,44,45,46
 28,30,38,40,42,43
 +3V
 +15V
 5V/SUS
 +3V/PCU
 VIN
 +5V

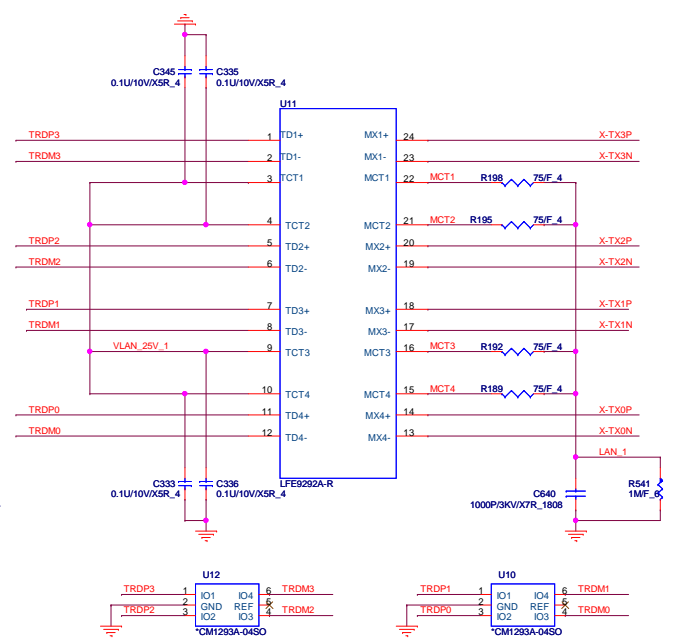


back light

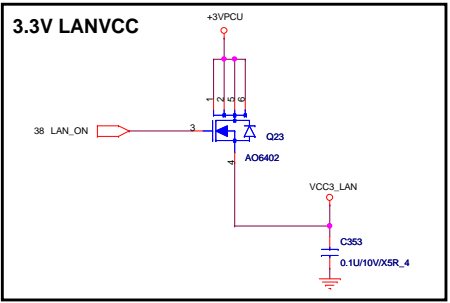
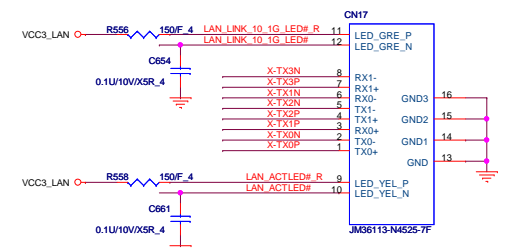




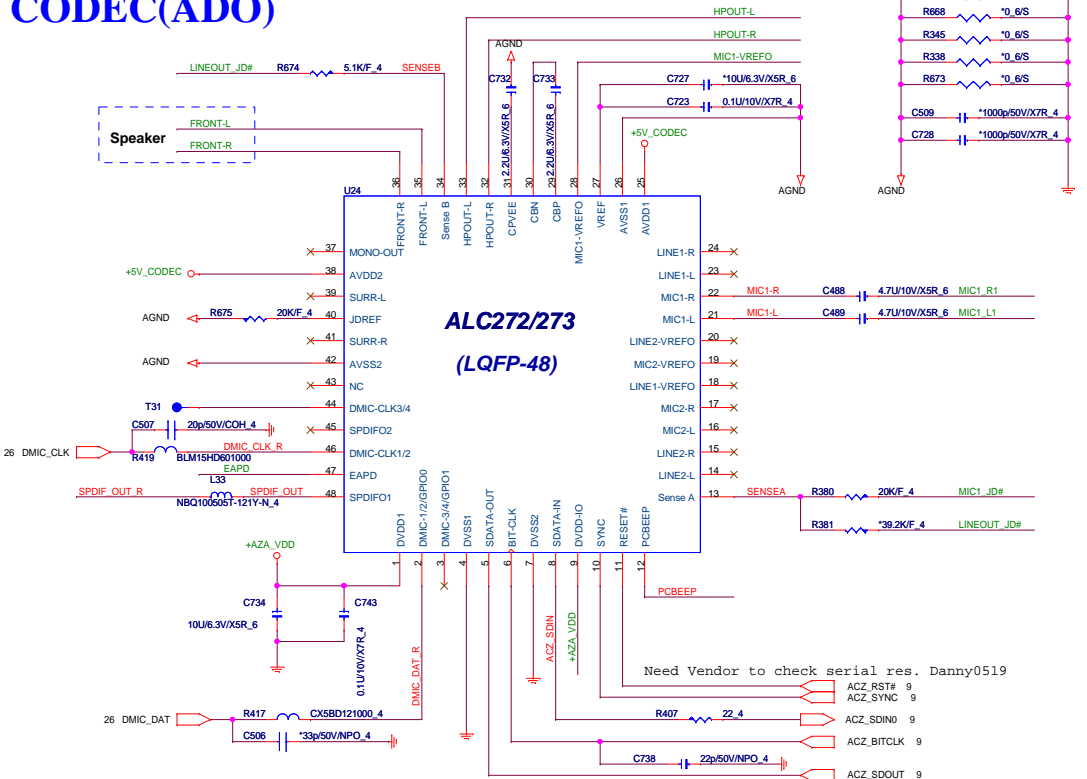
Transformer



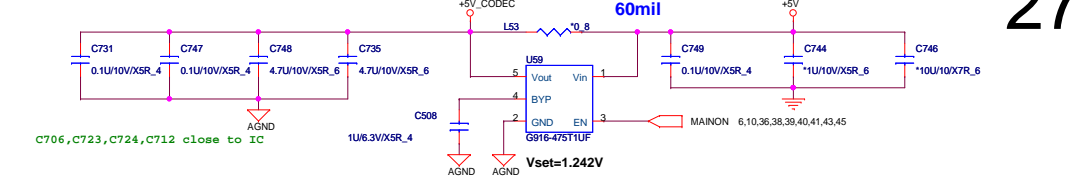
RJ45 Connector



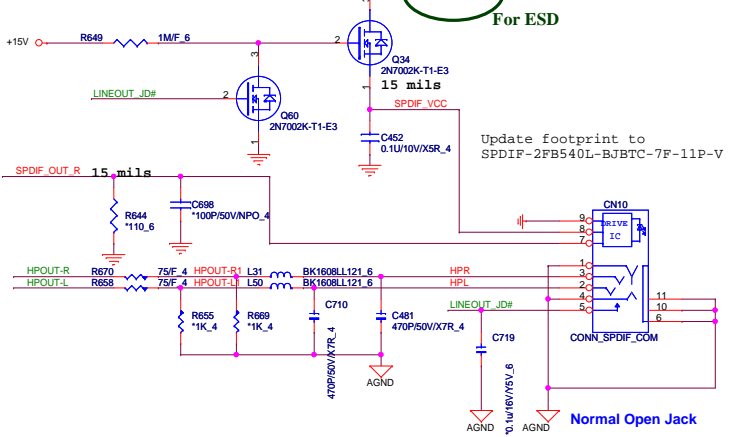
CODEC(ADO)



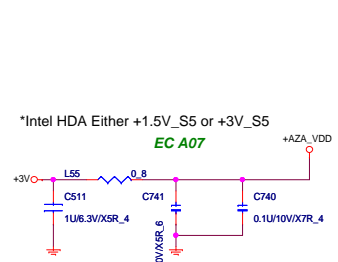
Codec Power(ADO)



Earphone(AMP)

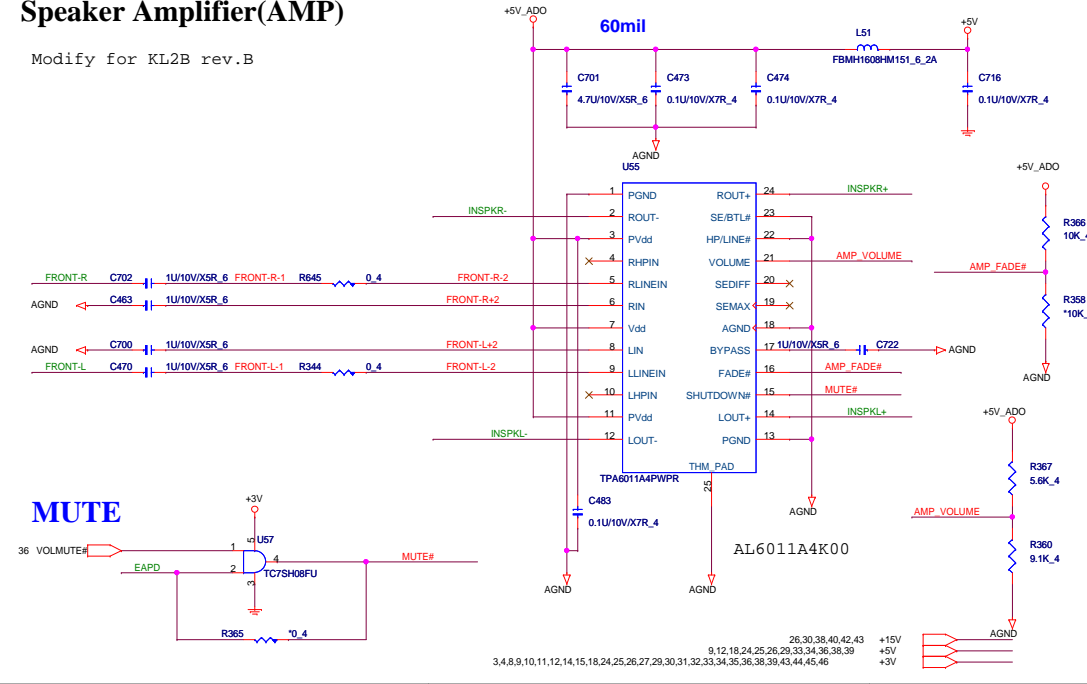


HDA Power(ADO)

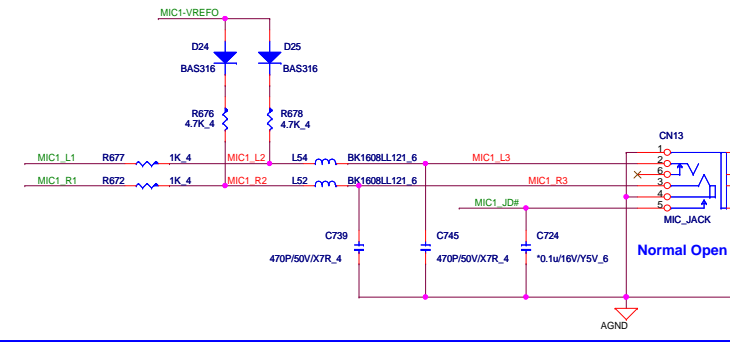


Speaker Amplifier(AMP)

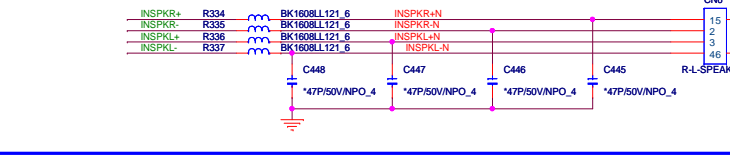
Modify for KL2B rev.B



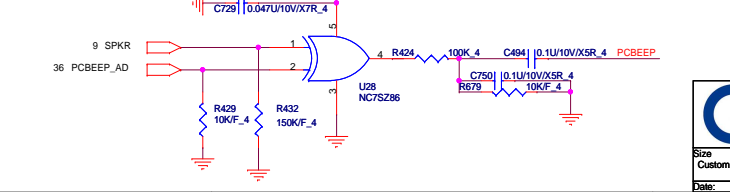
System MIC(AMP)



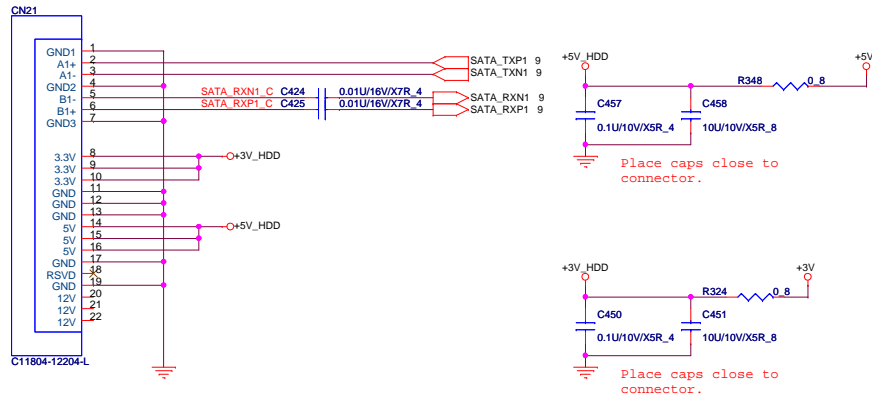
Speaker(AMP)



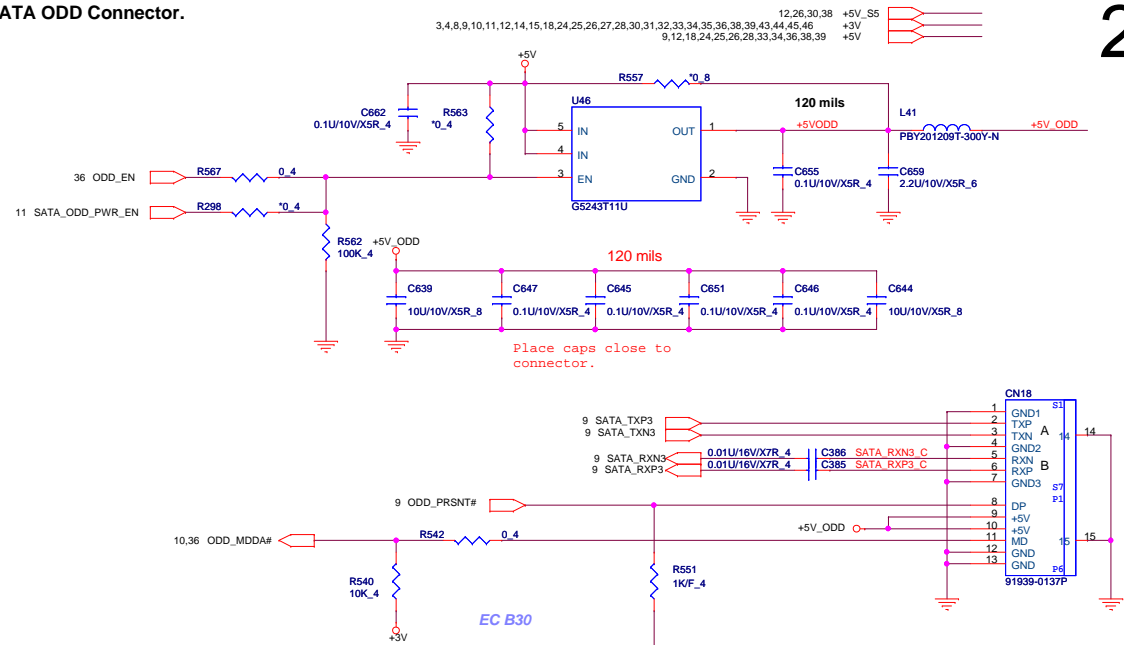
PC BEEP



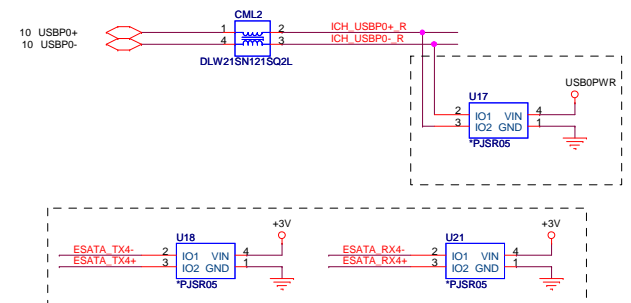
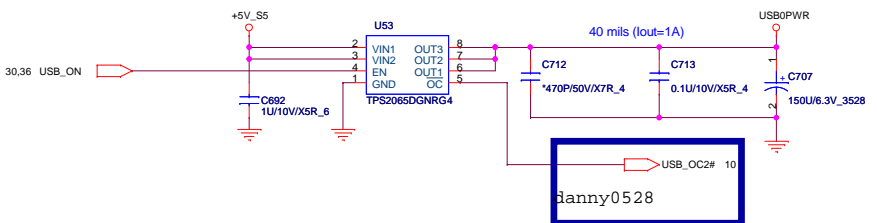
SATA HDD Connector.



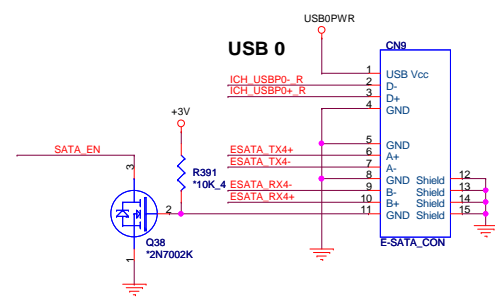
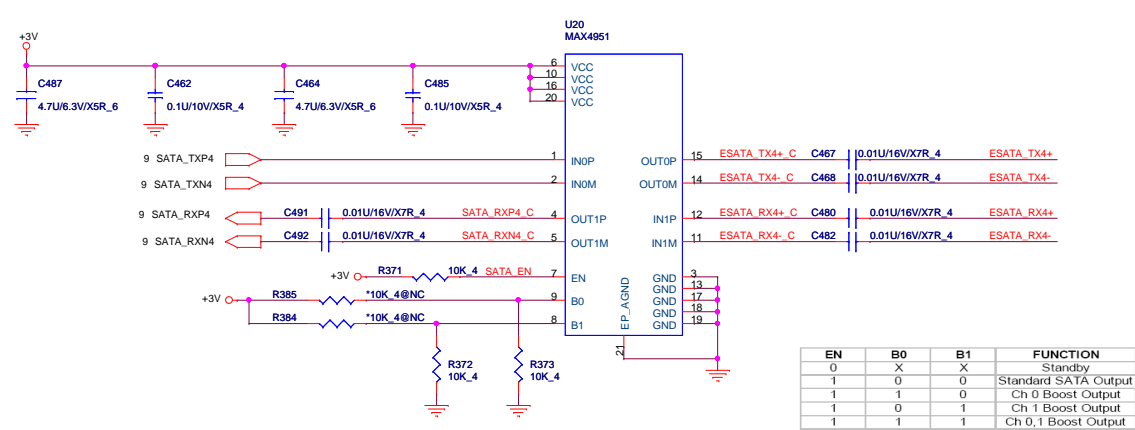
SATA ODD Connector.



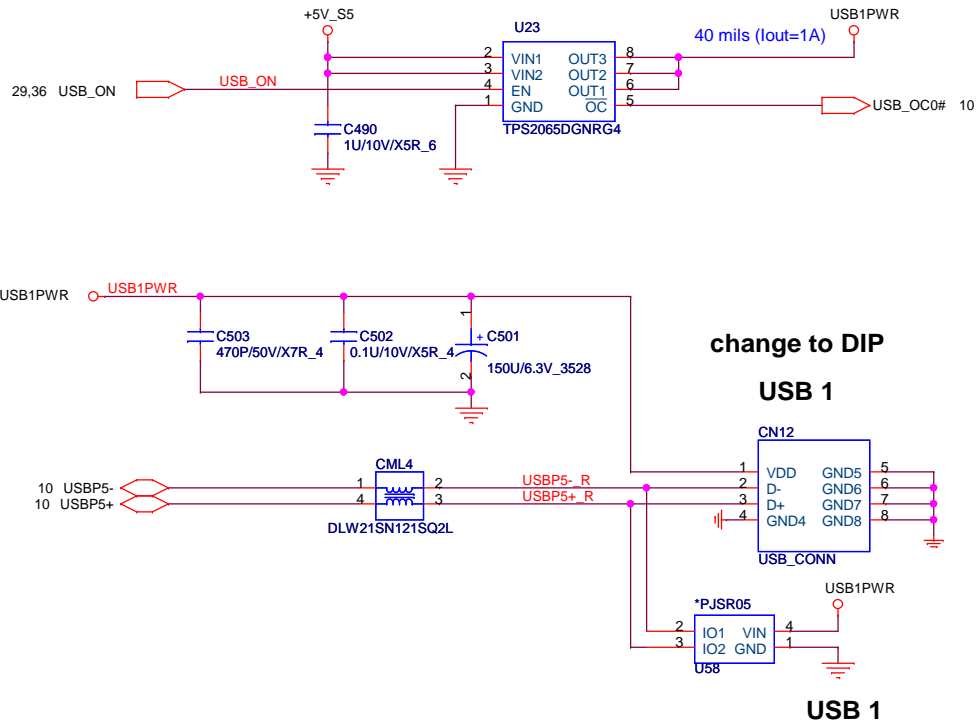
USB + E-SATA



E-SATA RE-DRIVER

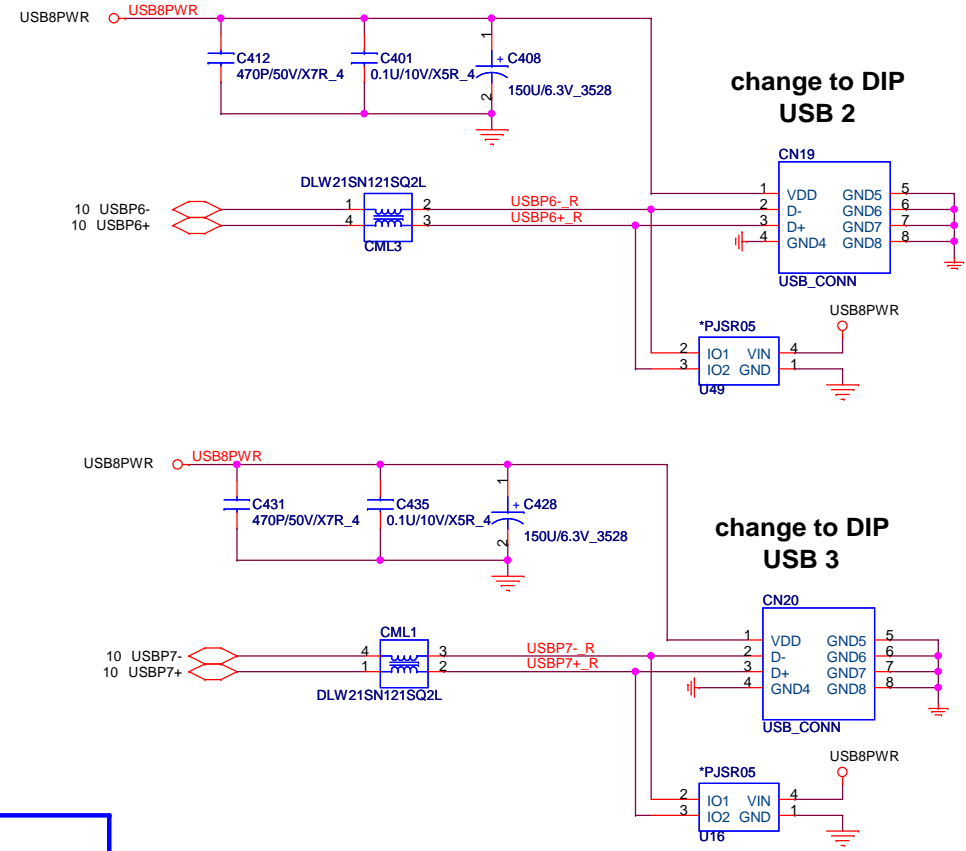


USBX3

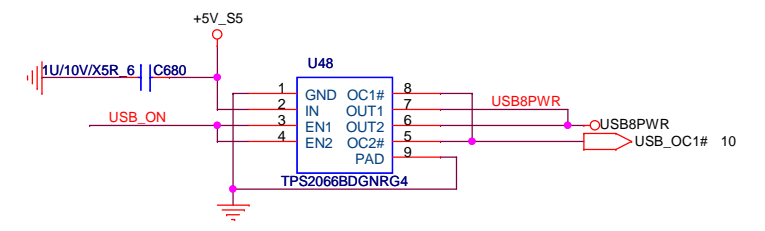
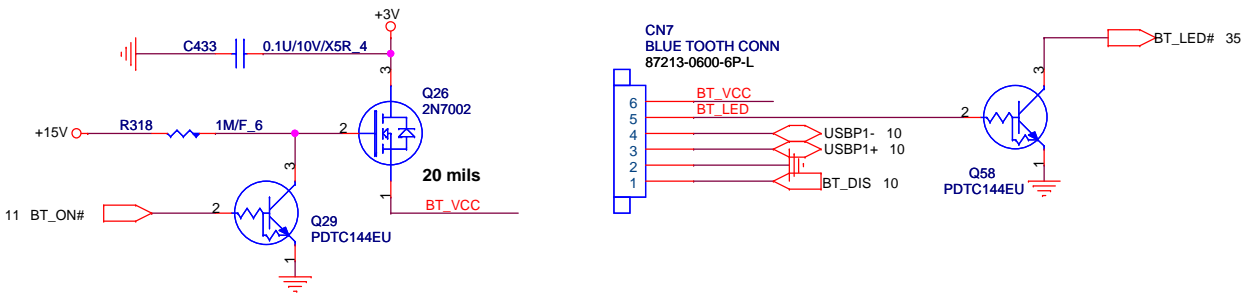


3,4,8,9,10,11,12,14,15,18,24,25,26,27,28,29,31,32,33,34,35,36,38,39,43,44,45,46
 12,26,29,38 +5V_S5
 26,28,38,40,42,43 +3V
 +15V

29

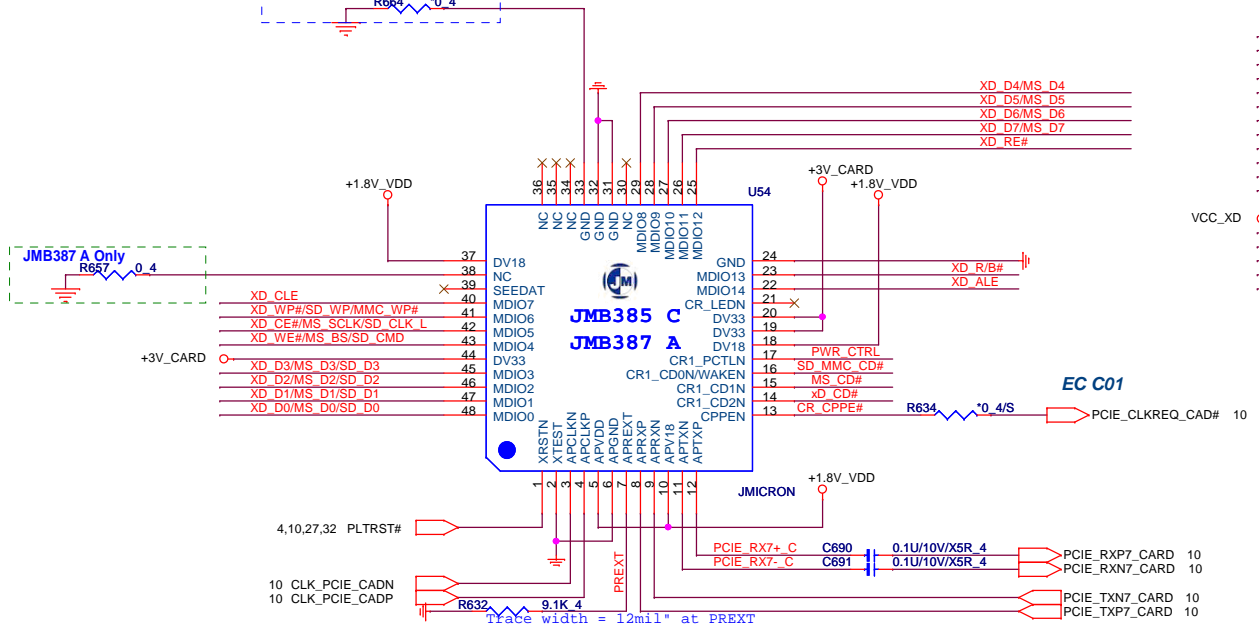
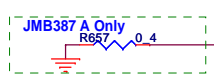
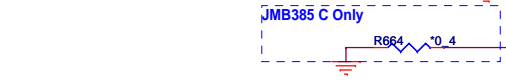
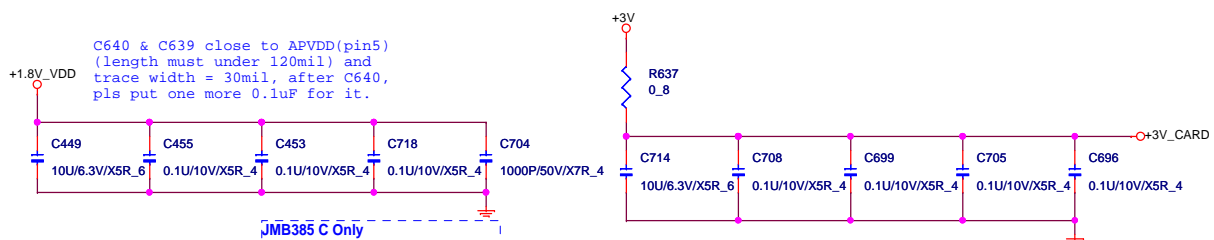


BLUETOOTH

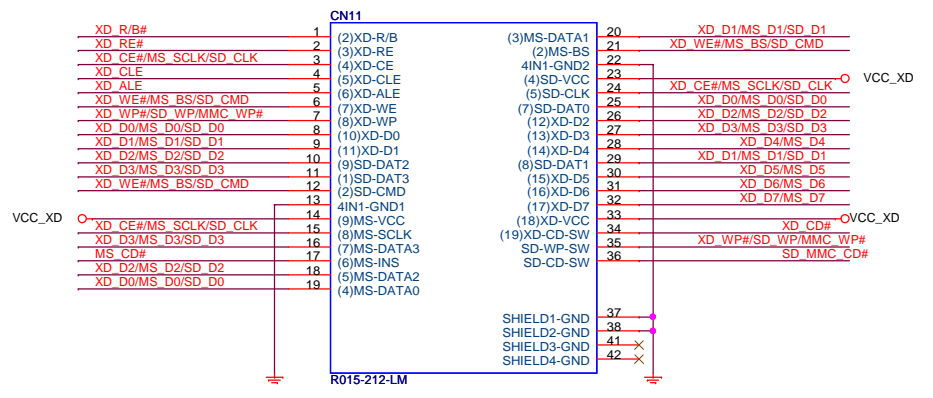


PROJECT : KL2D
Quanta Computer Inc.

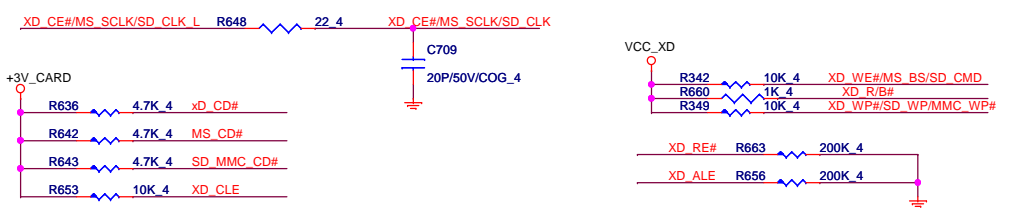
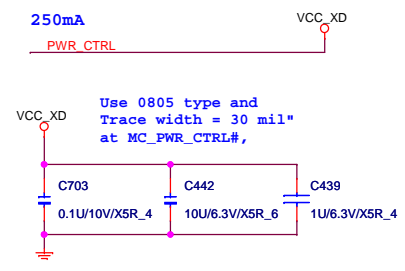
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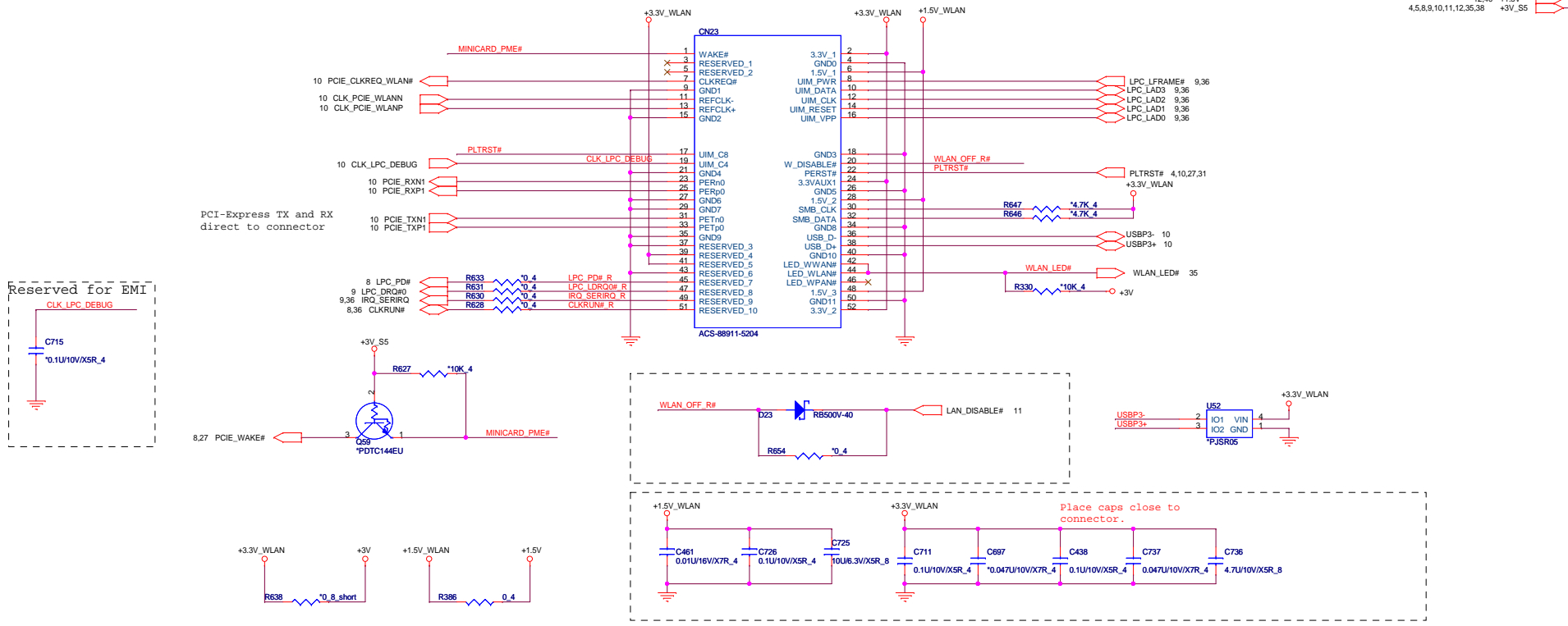
7 IN 1 CARD READER



Memory Card Power Supply

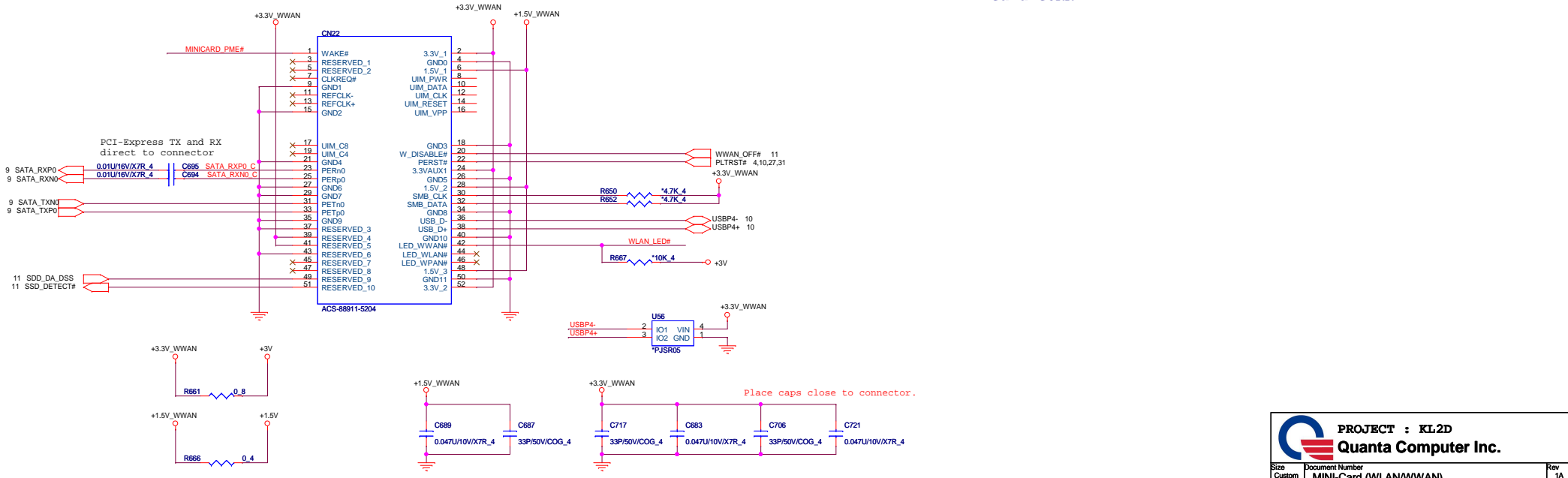


MiniCard WLA connector



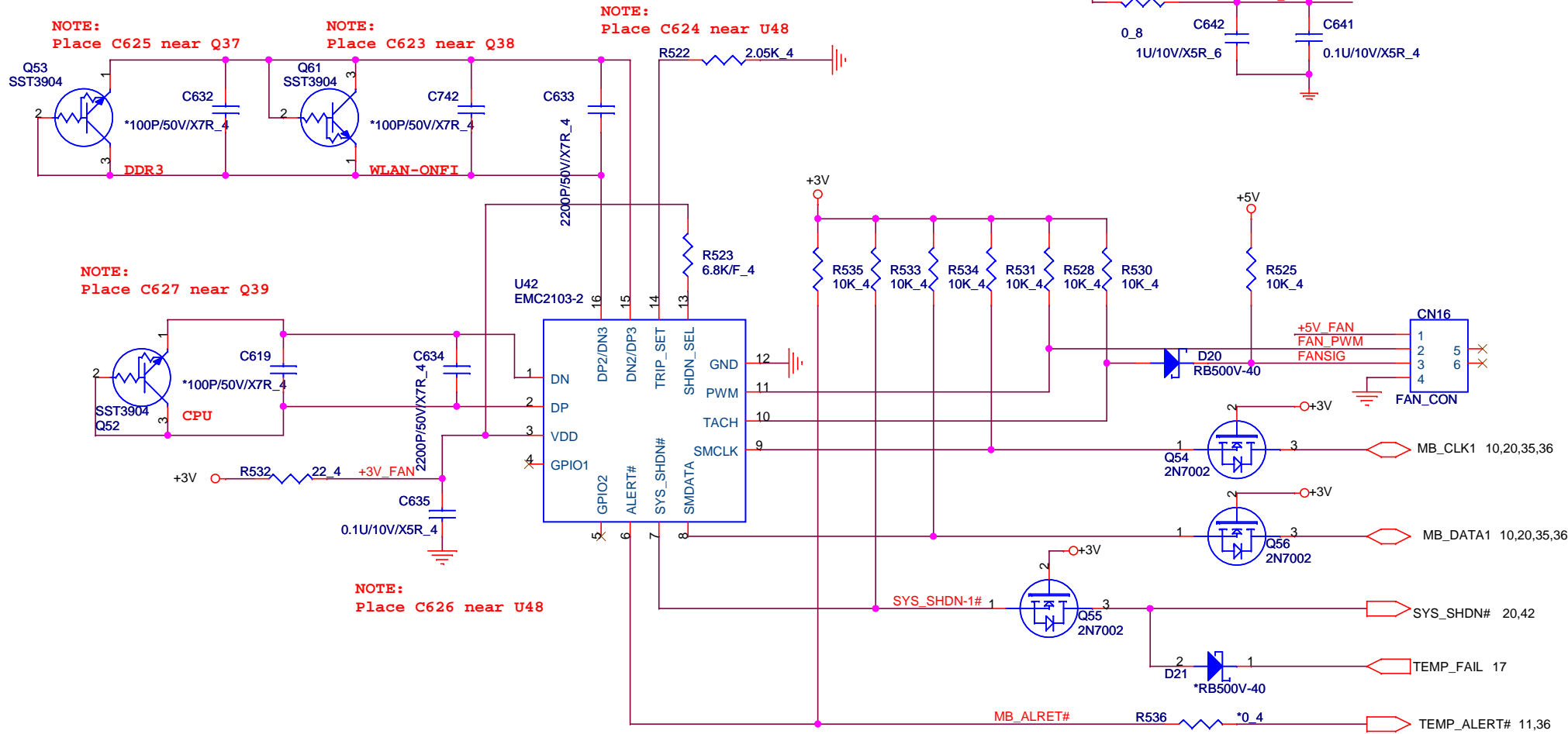
MiniCard WWAN/SATA SSD connector


SIM Card CONN



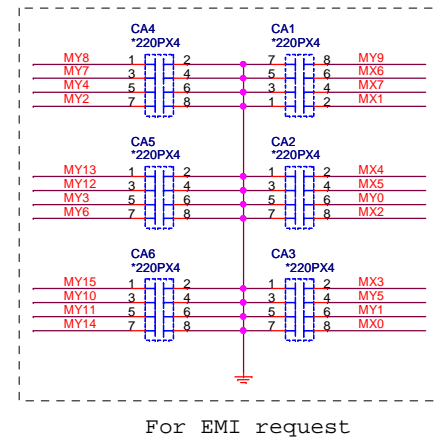
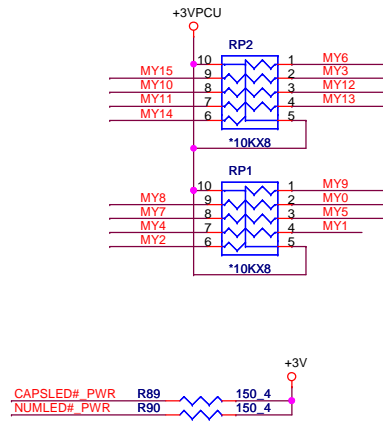
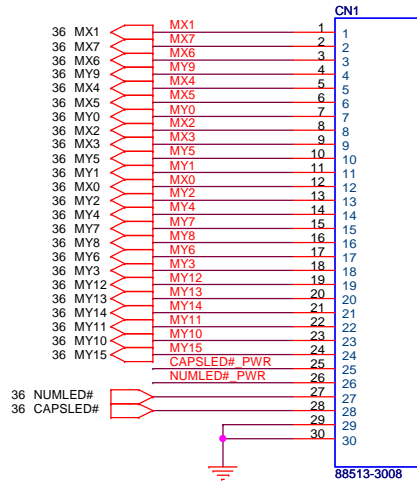
FAN CONTROL

3,4,8,9,10,11,12,14,15,18,24,25,26,27,28,29,30,31,32,34,35,36,38,39,43,44,45,46 +3V
 9,12,18,24,25,26,28,29,34,36,38,39 +5V



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		Custom	FAN /THERMAL	1A
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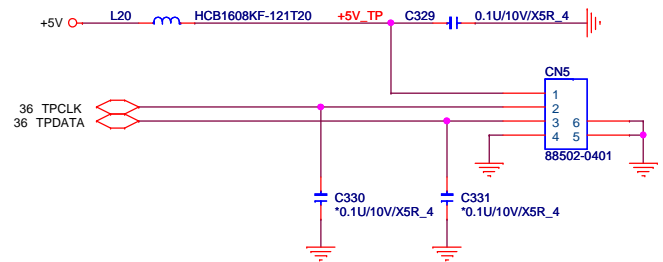
KEYBOARD



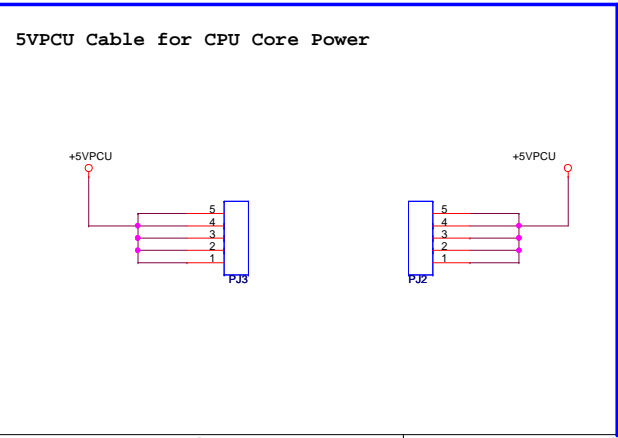
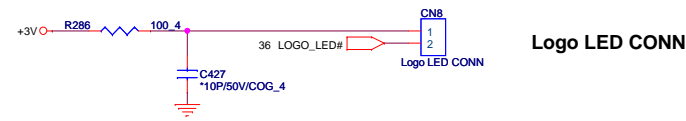
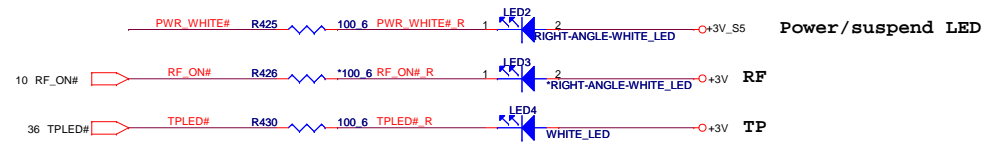
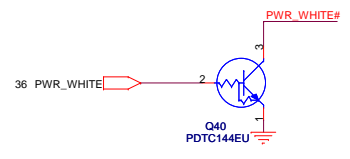
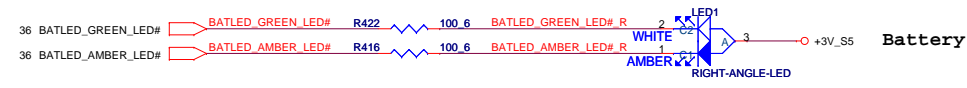
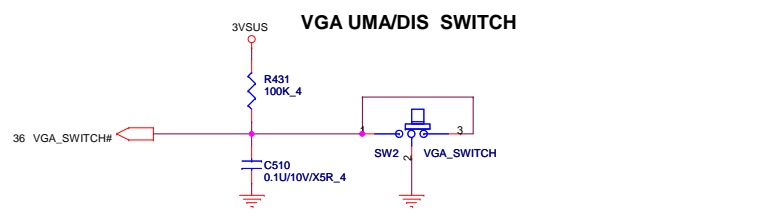
9,12,18,24,25,26,28,29,33,36,38,39 +5V
 8,9,15,26,27,35,36,38,39,42,44,46 +3VPCU
 26,28,30,38,40,42,43 +15V
 3,4,8,9,10,11,12,14,15,18,24,25,26,27,28,29,30,31,32,33,35,36,38,39,43,44,45,46 +3V
 5VSUS

34

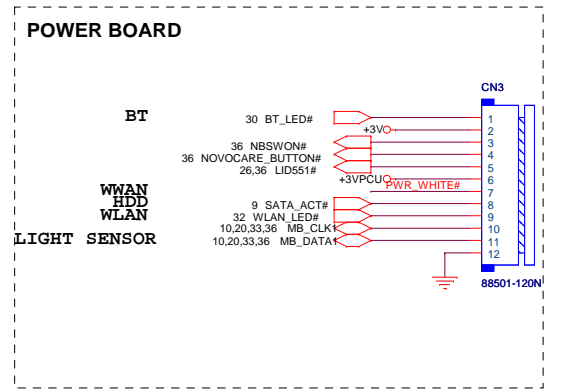
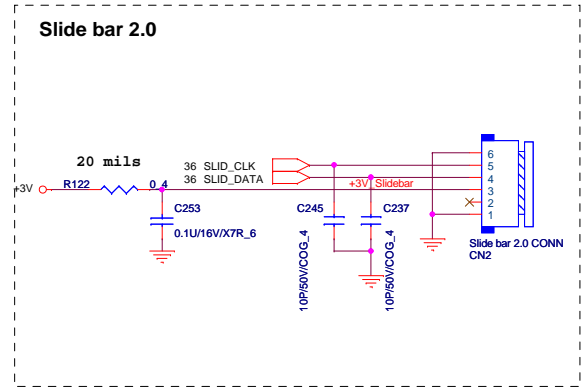
Touch pad



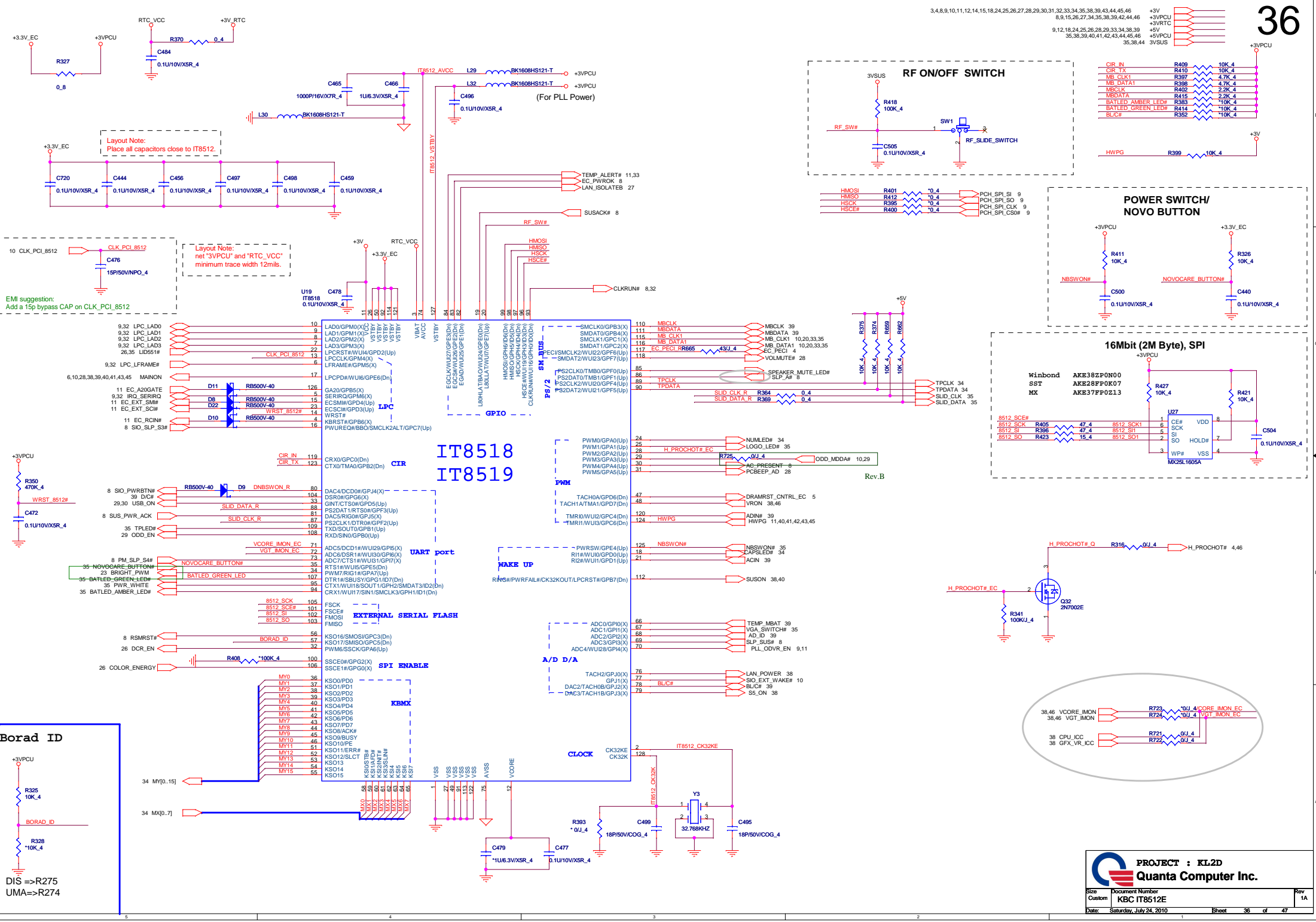
Backlight Keyboard Con.



6,9,15,26,27,34,36,38,39,42,44,46
 3,4,8,9,10,11,12,14,15,18,24,25,26,27,28,29,30,31,32,33,34,36,38,39,43,44,45,46
 +3VPCU
 +3V
 3VSUS



3,4,8,9,10,11,12,14,15,16,24,25,26,27,28,29,30,31,32,33,34,35,38,39,43,44,45,46	+3V
8,9,15,26,27,34,35,38,39,42,44,46	+3VPCU
9,12,18,24,25,26,28,29,33,34,38,39	+3VRTC
35,38,39,40,41,42,43,44,45,46	+5VPCU
35,38,44	3VSUS

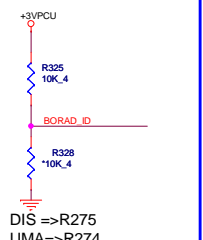


Layout Note:
Place all capacitors close to IT8512.

Layout Notes:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

EMI suggestion:
Add a 15pF bypass CAP on CLK_PCI_8512

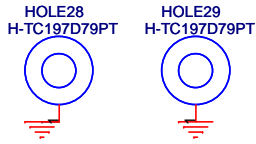
Borad ID



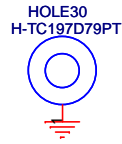
PROJECT : KL2D
Quanta Computer Inc.

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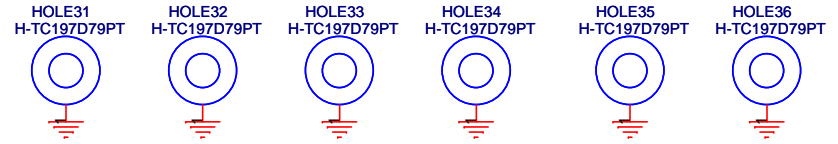
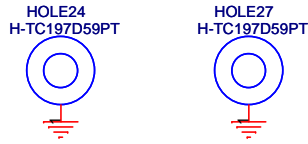
MiniCard WLAN



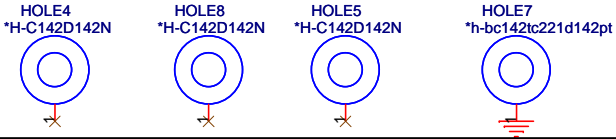
MiniCard WWAN



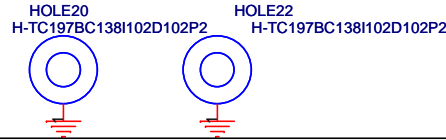
Hole for PCH support



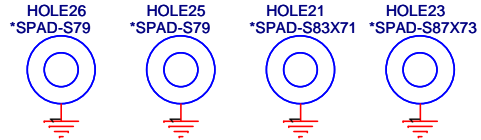
Hole for CPU support



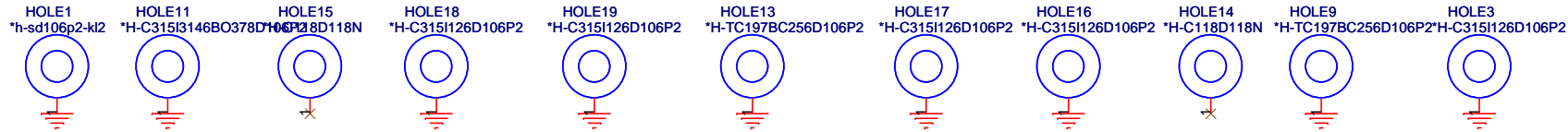
VGA nut



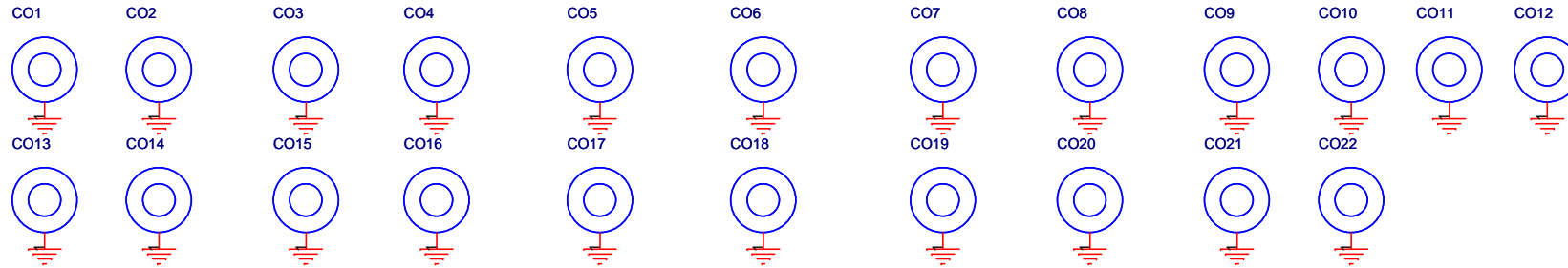
PAD



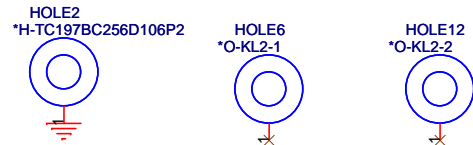
Boundary Hole



ESD Mask Copper

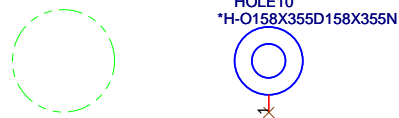


Boundary Hole



HDD PAD

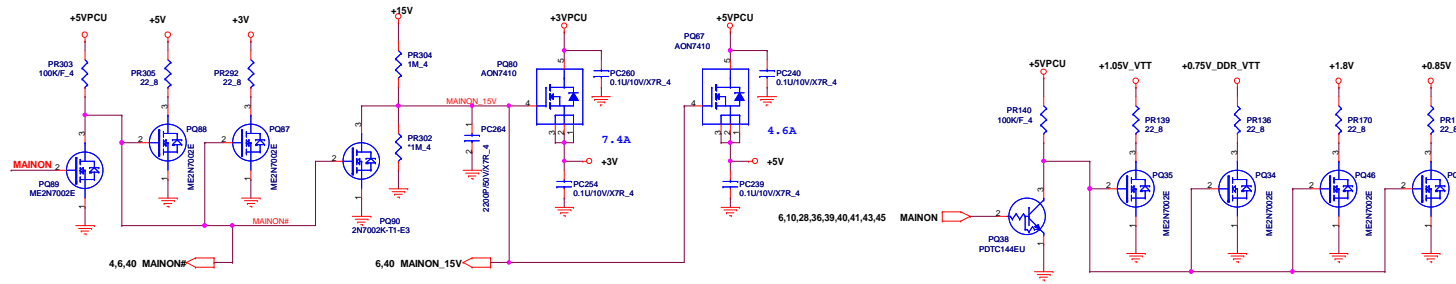
EC QV08



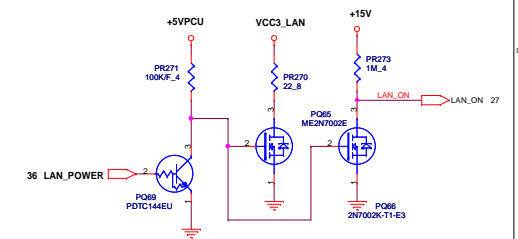
PROJECT : KL2D
Quanta Computer Inc.

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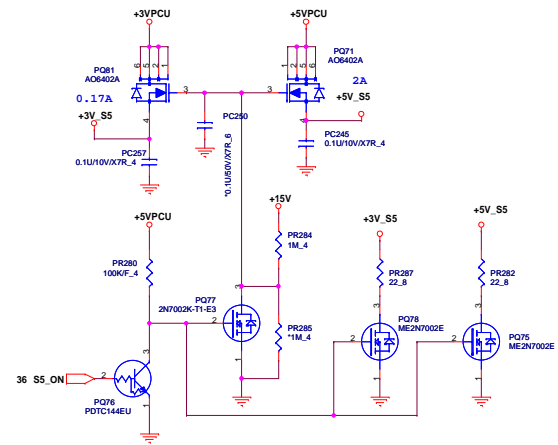
+3V, +5V



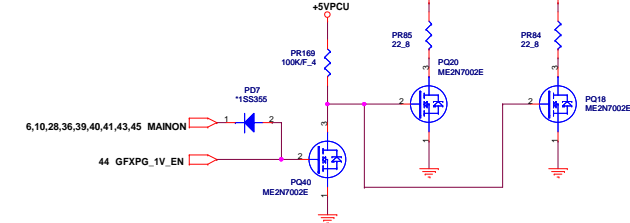
LANVCC



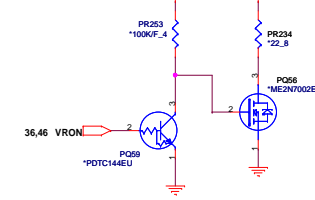
3V_S5, 5V_S5



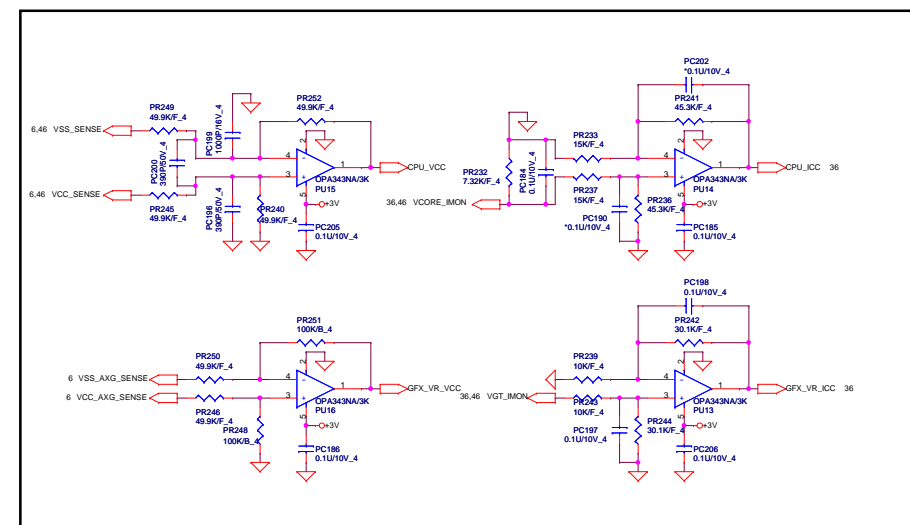
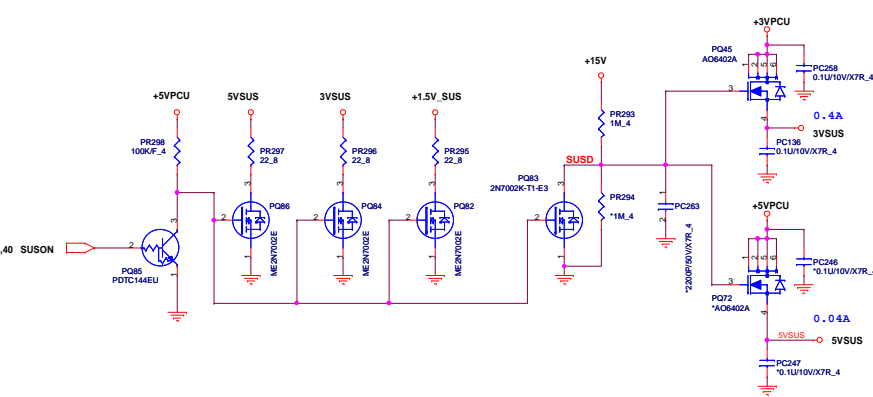
GFX_CORE, +1V_GFX_PCIE



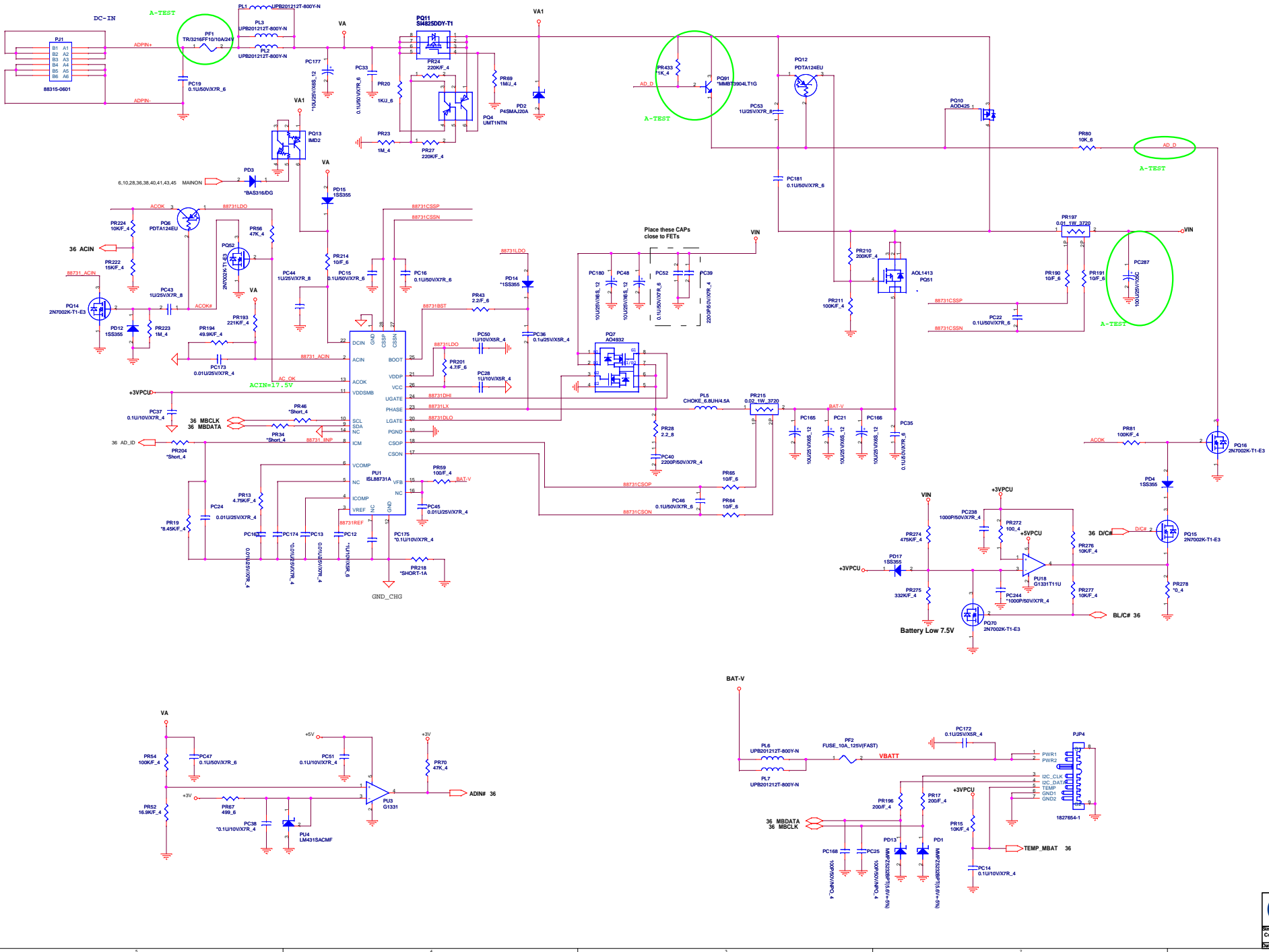
+5VPCU, +VCC_CORE

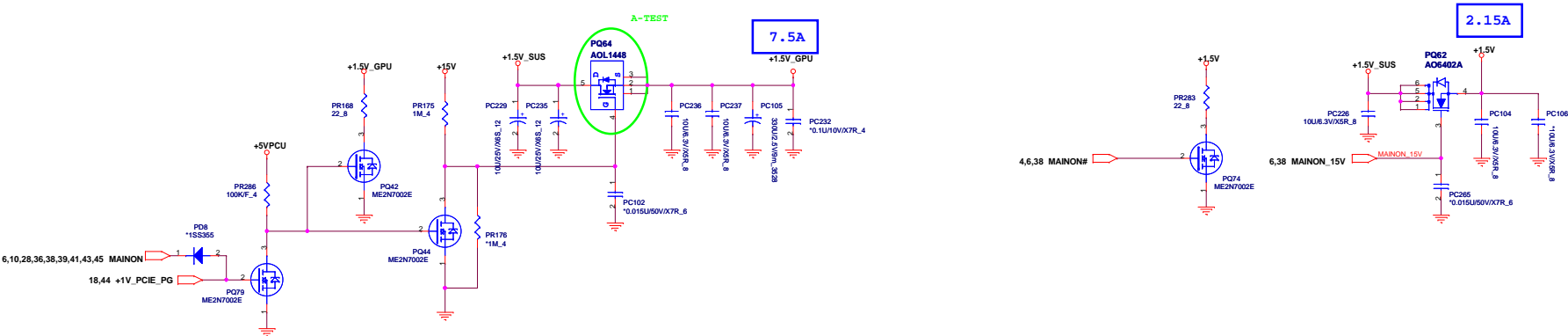
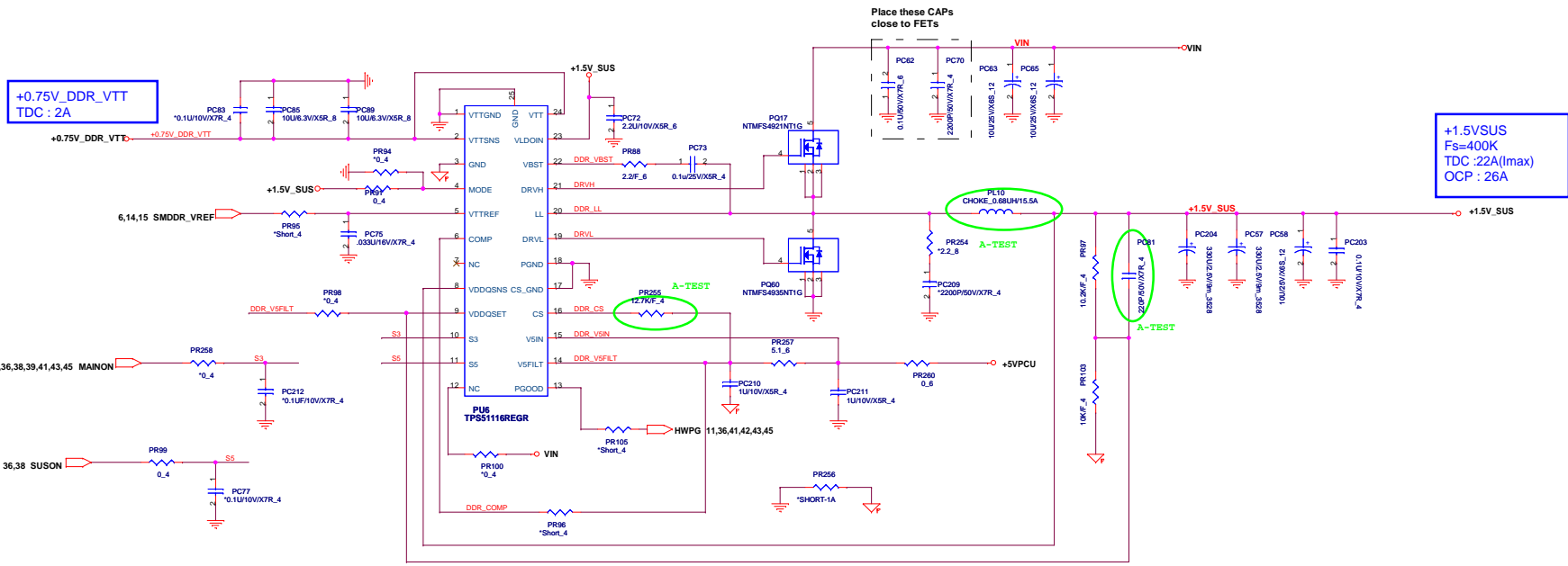


3VSUS, 5VSUS

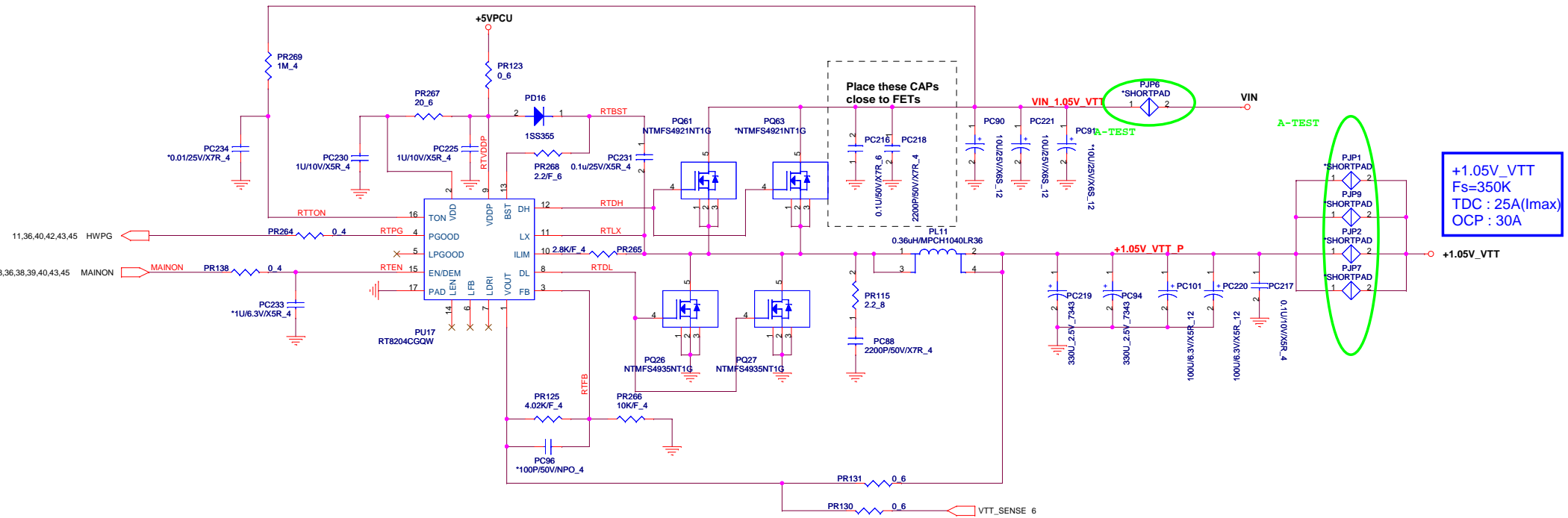


R138=0.02m ohm for 65W adapter-->current limit is 3A;




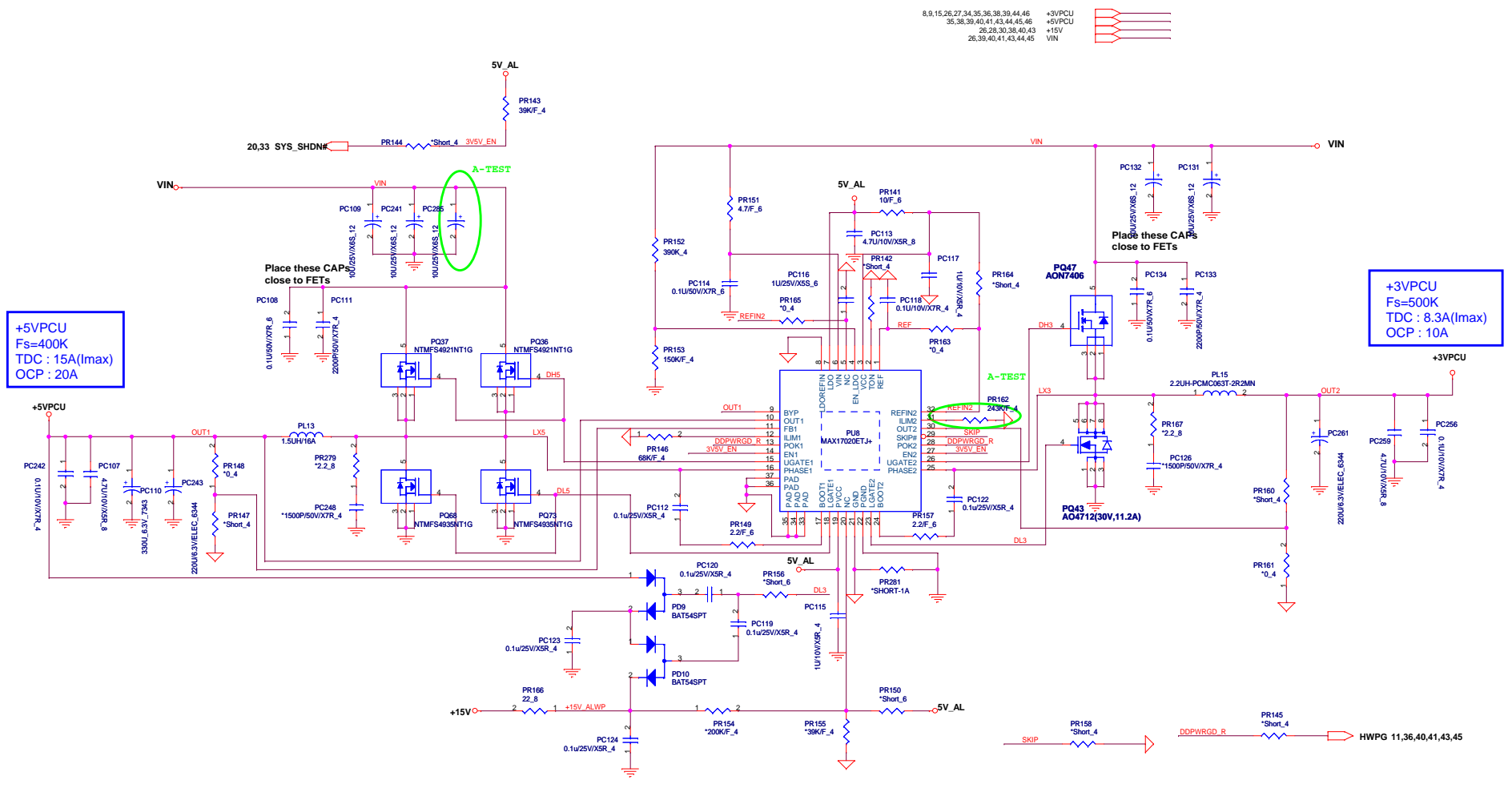


For S3 Power Saving



+1.05V_VTT
 Fs=350K
 TDC : 25A(I_{max})
 OCP : 30A

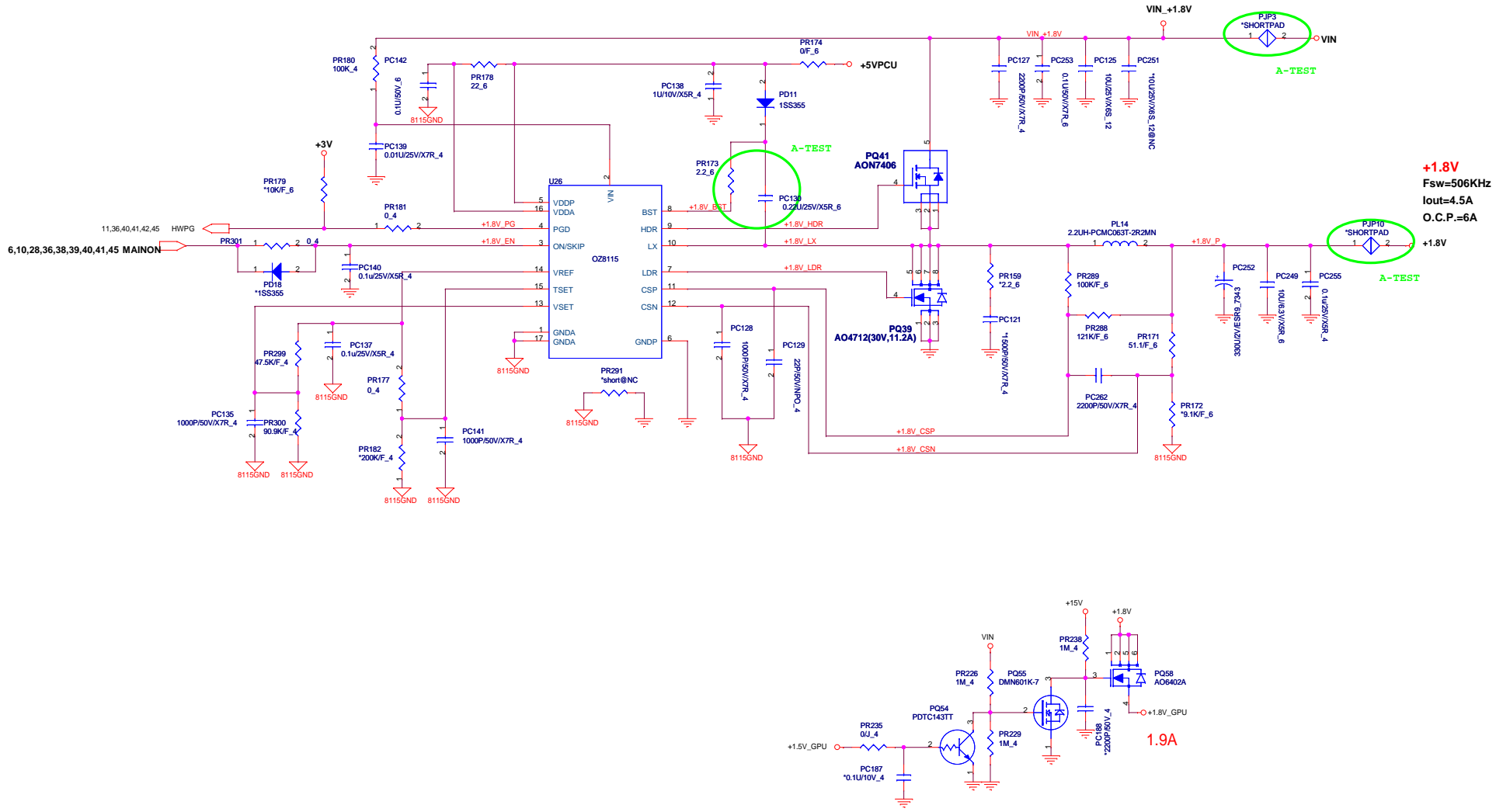
 PROJECT : KL2D Quanta Computer Inc.		
Size Custom	Document Number 1.05V_VTT (RT8204)	Rev 1A
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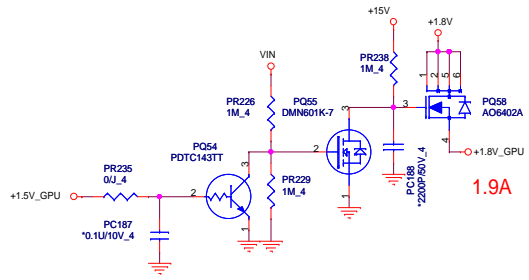
+5VPCU
 Fs=400K
 TDC : 15A(I_{max})
 OCP : 20A

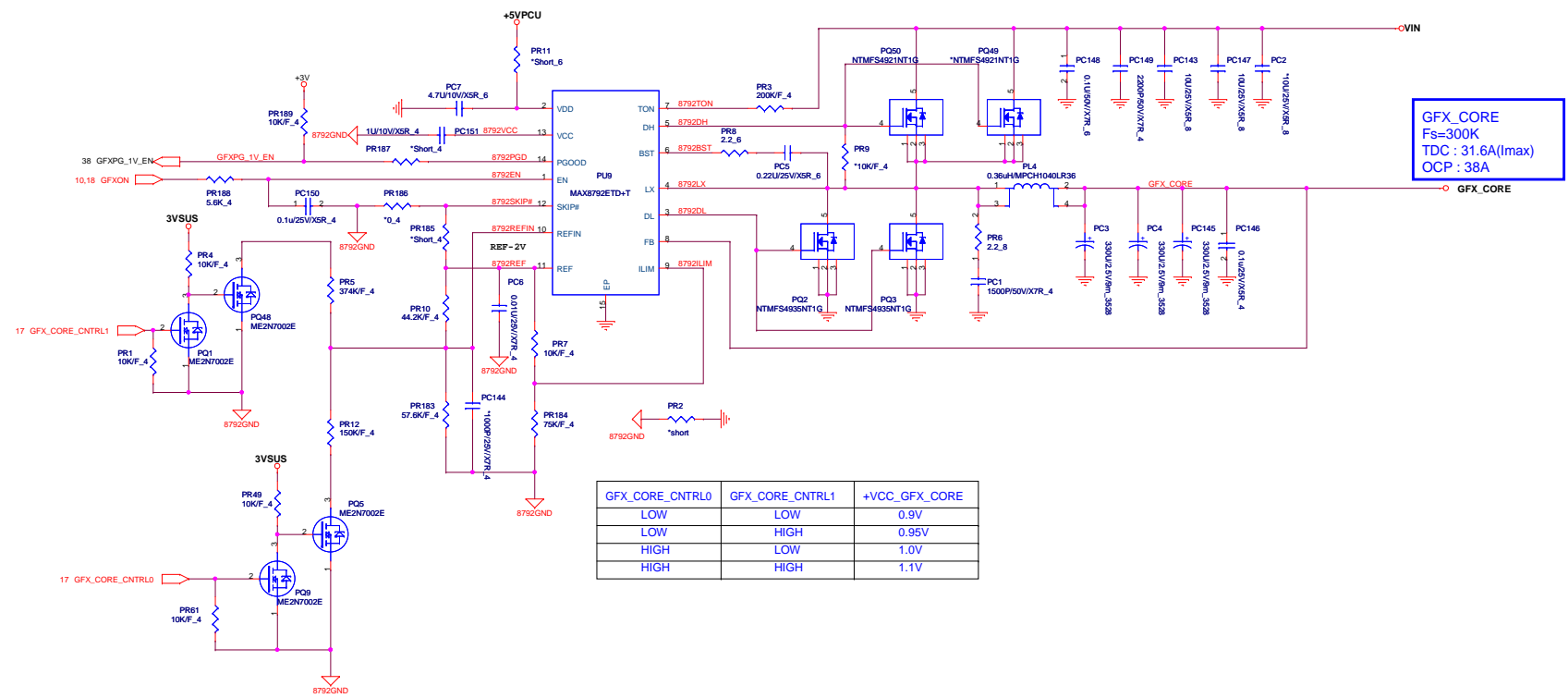
+3VPCU
 Fs=500K
 TDC : 8.3A(I_{max})
 OCP : 10A

- 8,9,15,26,27,34,35,36,38,39,44,46 +3VPCU
- 35,38,39,40,41,43,44,45,46 +5VPCU
- 26,28,30,38,40,43 +15V
- 26,39,40,41,43,44,45 VIN

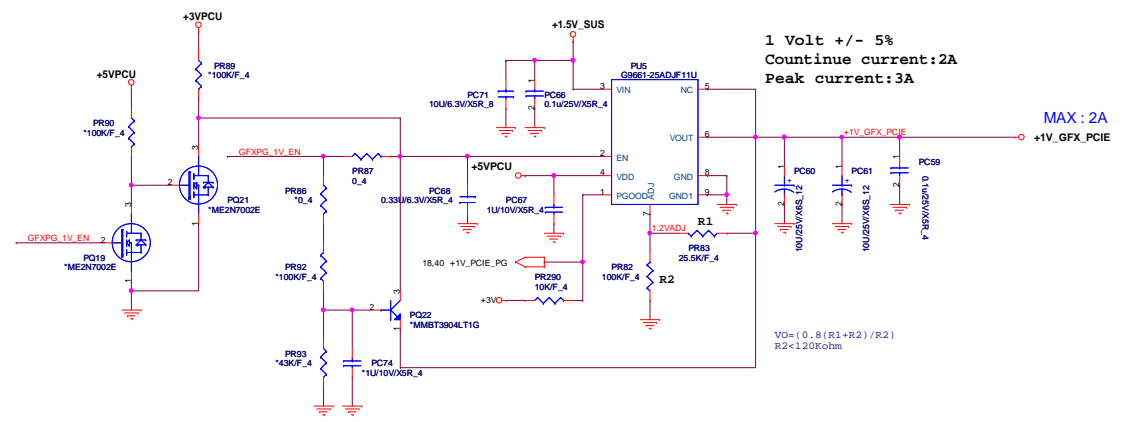


+1.8V
 Fsw=506KHz
 Iout=4.5A
 O.C.P.=6A



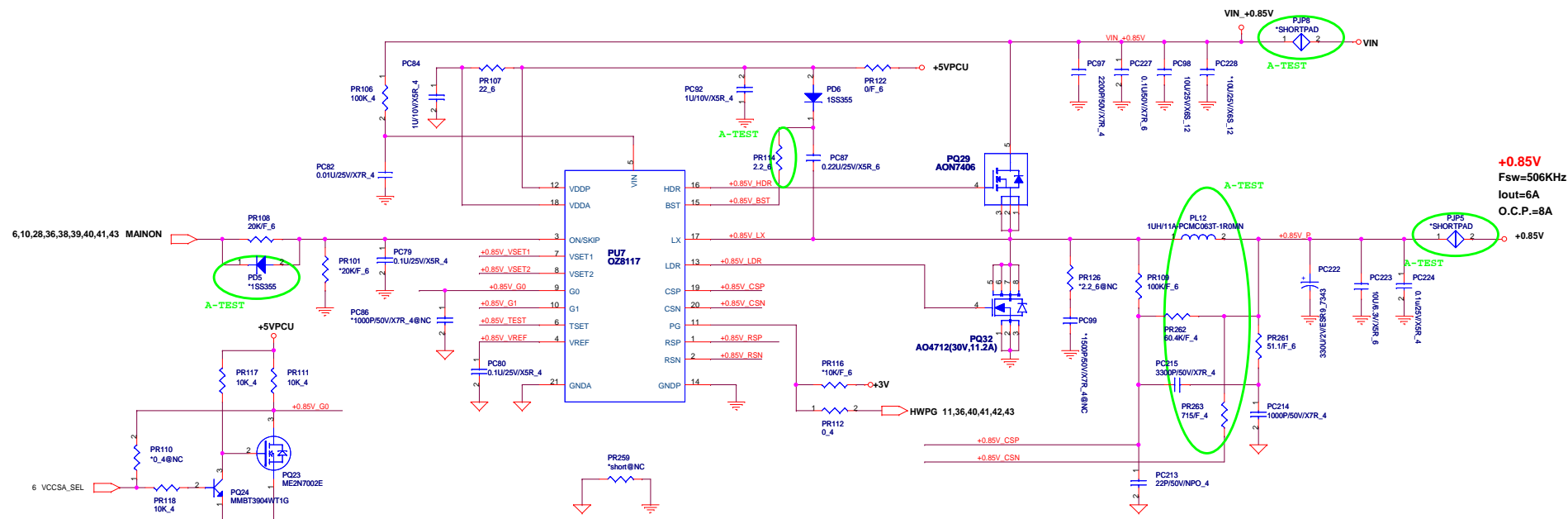


GFX_CORE
 Fs=300K
 TDC : 31.6A(I_{max})
 OCP : 38A



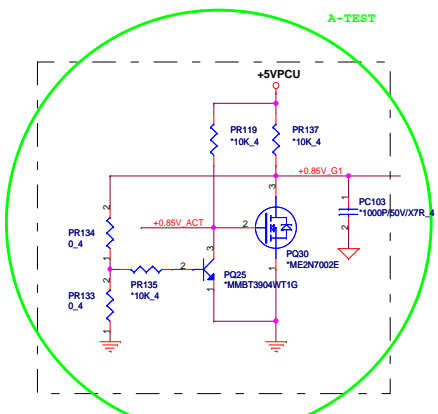
1 Volt +/- 5%
 Countinue current:2A
 Peak current:3A

$$V_O = (0.8(R1+R2) / R2) \\ R2 < 120Kohm$$

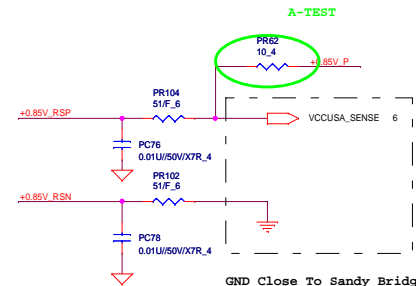
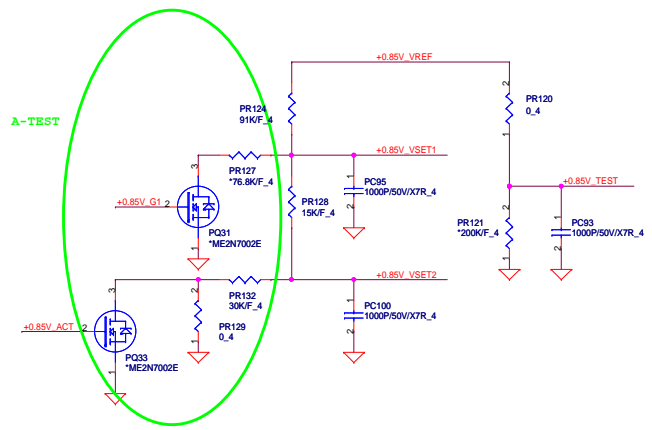


+0.85V
Fsw=506KHz
Iout=6A
O.C.P.=8A

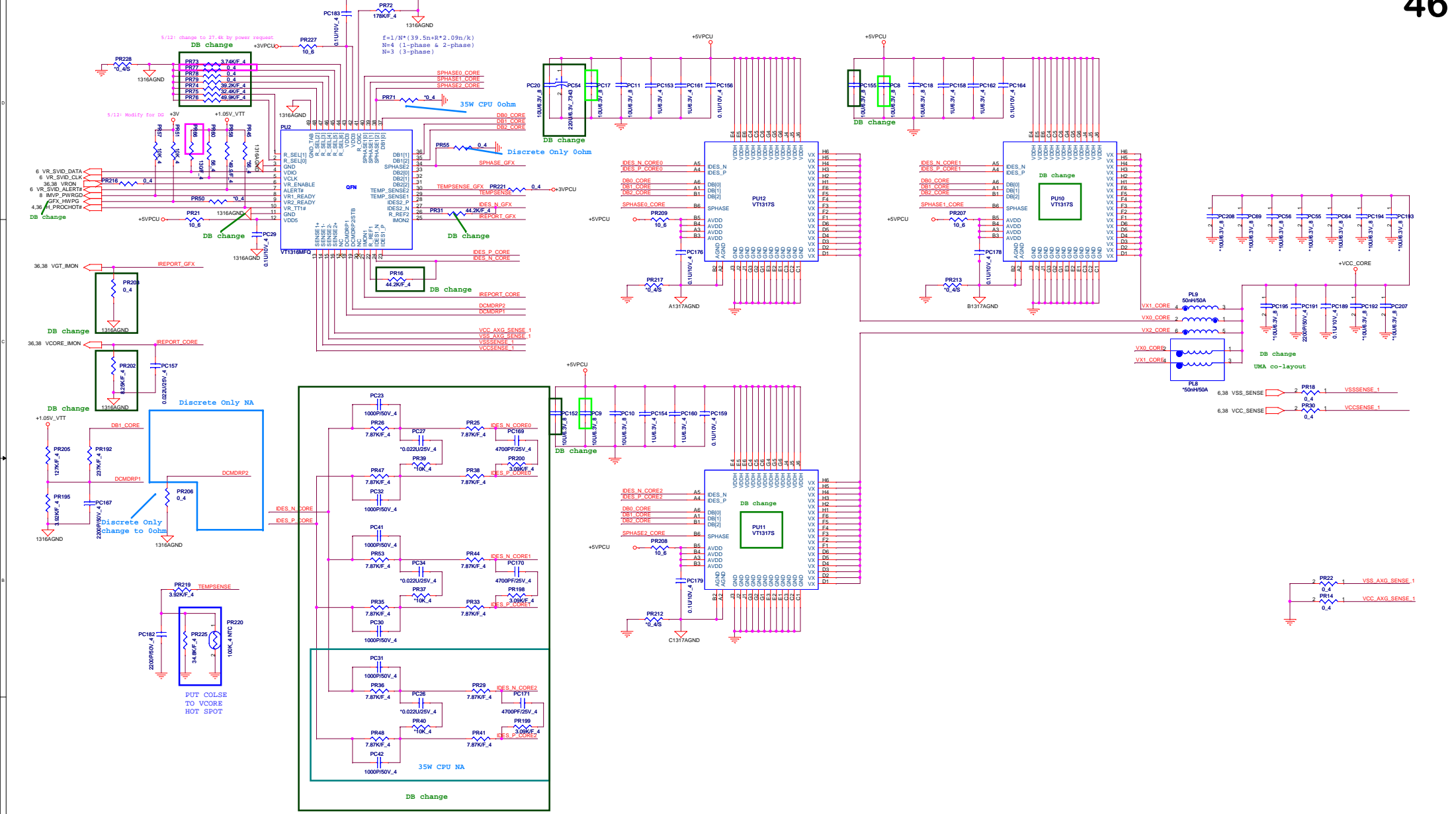
	VCCSA_SEL	VCCUA(+0.85V)
0	0	0.9V
0	1	0.8V




For Sandy Bridge And IV Bridge VID Select



GND Close To Sandy Bridge Processor (POWER) Side



EC #	Page	Description	Part Affected

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