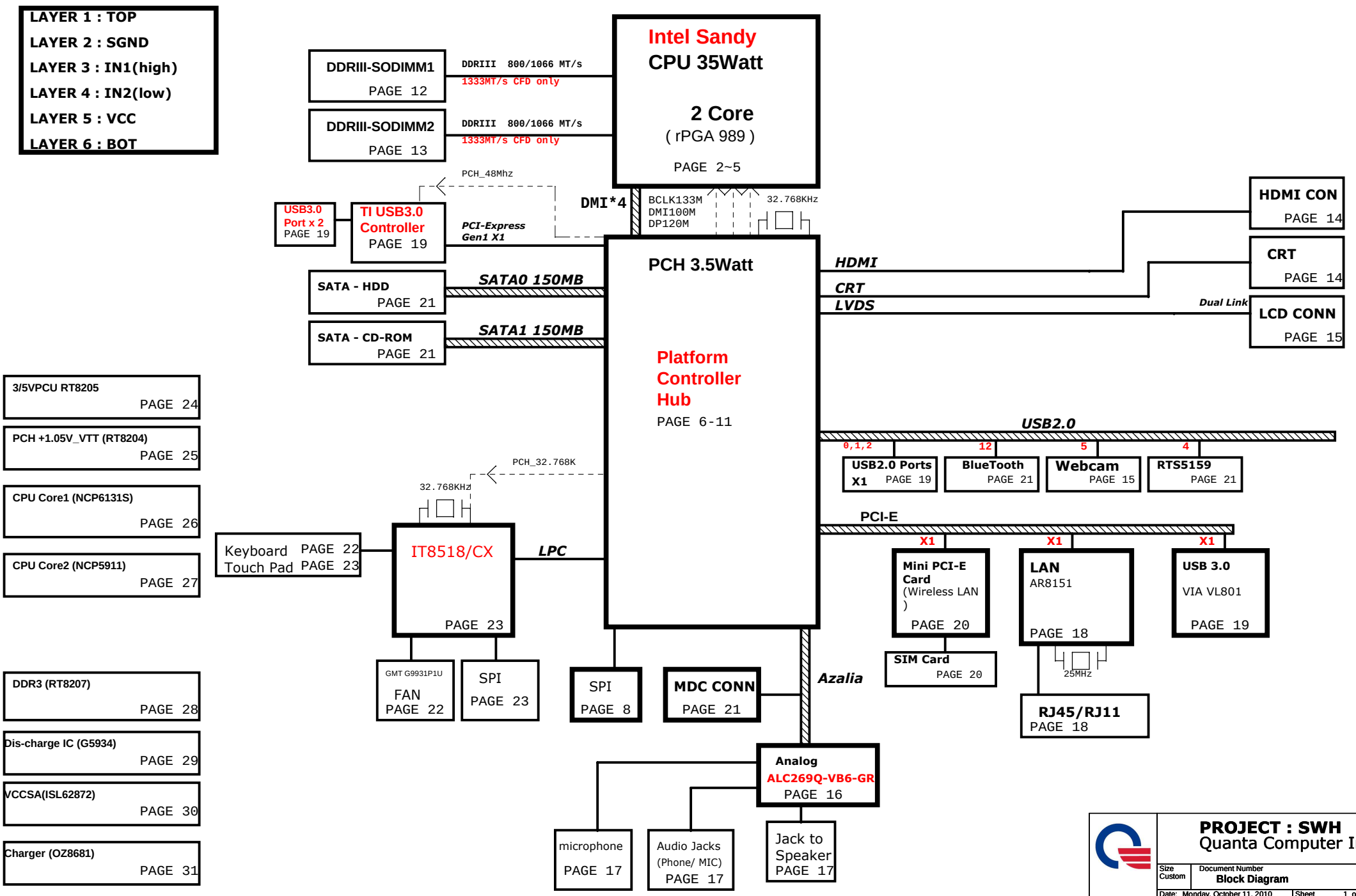
SWH_UMA (14") BLOCK DIAGRAM

01

PCB STACK UP
6L UMA

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1(high)
- LAYER 4 : IN2(low)
- LAYER 5 : VCC
- LAYER 6 : BOT



PROJECT : SWH
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Custom	Block Diagram	1A

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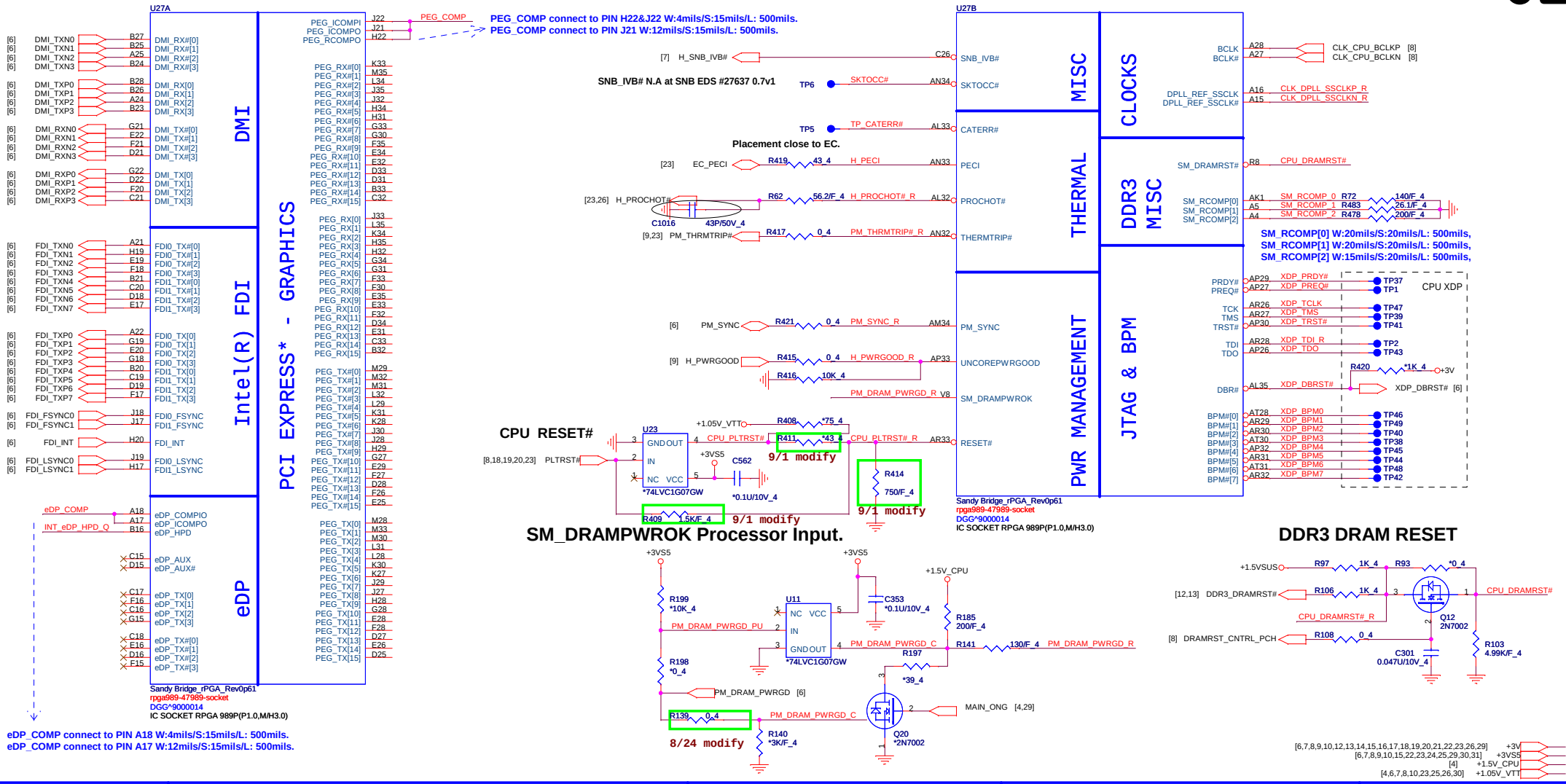
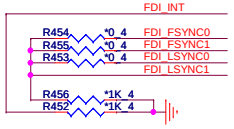
Sandy Bridge Processor (DMI,PEG,FDI)

Sandy Bridge Processor (CLK,MISC,JTAG)

02



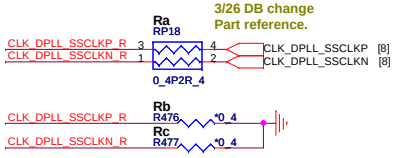
FDI disable (DIS only stuff)



FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (DG V0.5 Ch2.2.9).

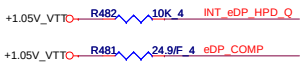
PEG x16 disable (UMA only remove)

Embedded Display PLL Clock



	Ra	Rb	Rc
DIS	NC	Stuff	Stuff
SG/UMA	Stuff	NC	NC

DP & PEG Compensation

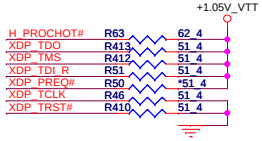


eDP_HPD can be left as no connect if entire eDP is disabled.

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up (CPU)



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Custom	SNB 1/4 (PCIE&DMI&FDI)	1A
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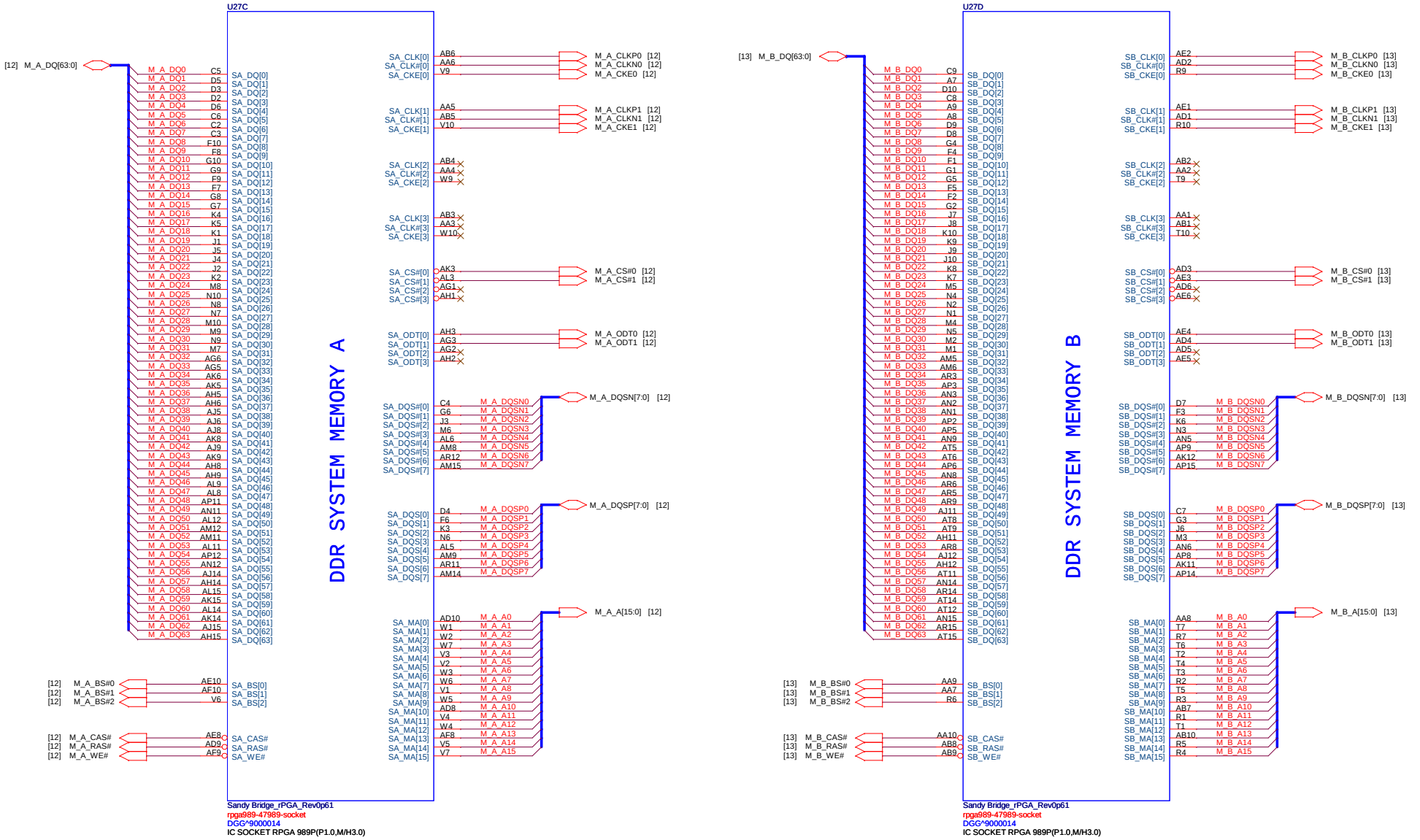
Sandy Bridge Processor (DDR3)



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Custom	SNB 2/4 (DDR3 I/F)	1A

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Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

04

SNB: 55A

+VCC_CORE

U27F

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

SNB: 8.5A

+1.05V_VTT

22uF_8 x7 Socket TOP cavity
22uF_8 x5 Socket BOT cavity
22uF_8 x2 Socket TOP cavity (no stuff)
22uF_8 x5 Socket BOT cavity (no stuff)
330uF_7343 x2

5/14 modify

22uF_8 x8 Socket TOP cavity
22uF_8 x10 Socket BOT cavity
22uF_8 x8 Socket TOP edge
470uF_7343 x4

Sandy Bridge_rPGA_Rev0p61
rpga989-47989-socket
DGG^9000014
IC SOCKET RPGA 989P(P1.0,M/H3.0)

22uF_8 x2 Socket TOP cavity
22uF_8 x2 Socket BOT cavity
22uF_8 x4 Socket TOP edge
22uF_8 x4 Socket BOT edge
470uF_7343 x2

U27G

GRAPHICS

SNB: 21.5A

+VCC_GFX

	DIS	SG/UMA
Ra	Stuff	NC

SNB: 1.5A

+1.8V

330uF x1, 10uF_8 x1, 1uF_4 x2
Socket BOT edge.

1.8V RAIL

SENSE LINES

VREF

DDR3 -1.5V RAILS

SA RAIL

MISC

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

SNB: 5A

10uF_8 x6 Socket BOT edge.

SNB: 6A

330uF x1, 10uF_8 x1 Socket BOT edge,
10uF_8 x2 Socket BOT cavity.

Add for intel CRB

40mile routing

Layout note: need routing together and ALERT need between CLK and DATA.

SVID CLK

SVID DATA

SVID ALERT

Place PU resistor close to VR

Place PU resistor close to CPU

Trace Route to Power IC area.

CPU VDDQ

add for Intel.
Placement close to CPU.

PROJECT : SWH
Quanta Computer Inc.

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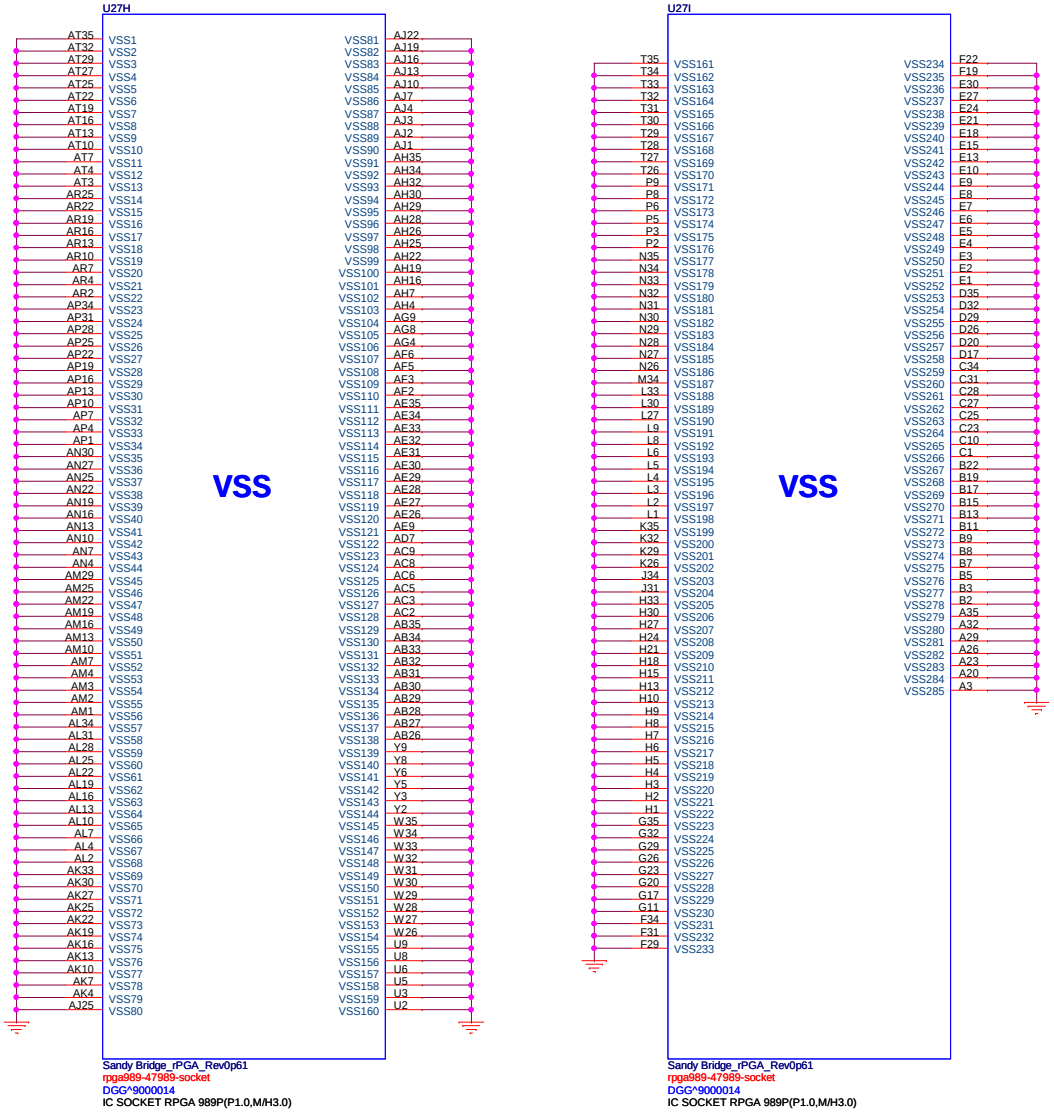
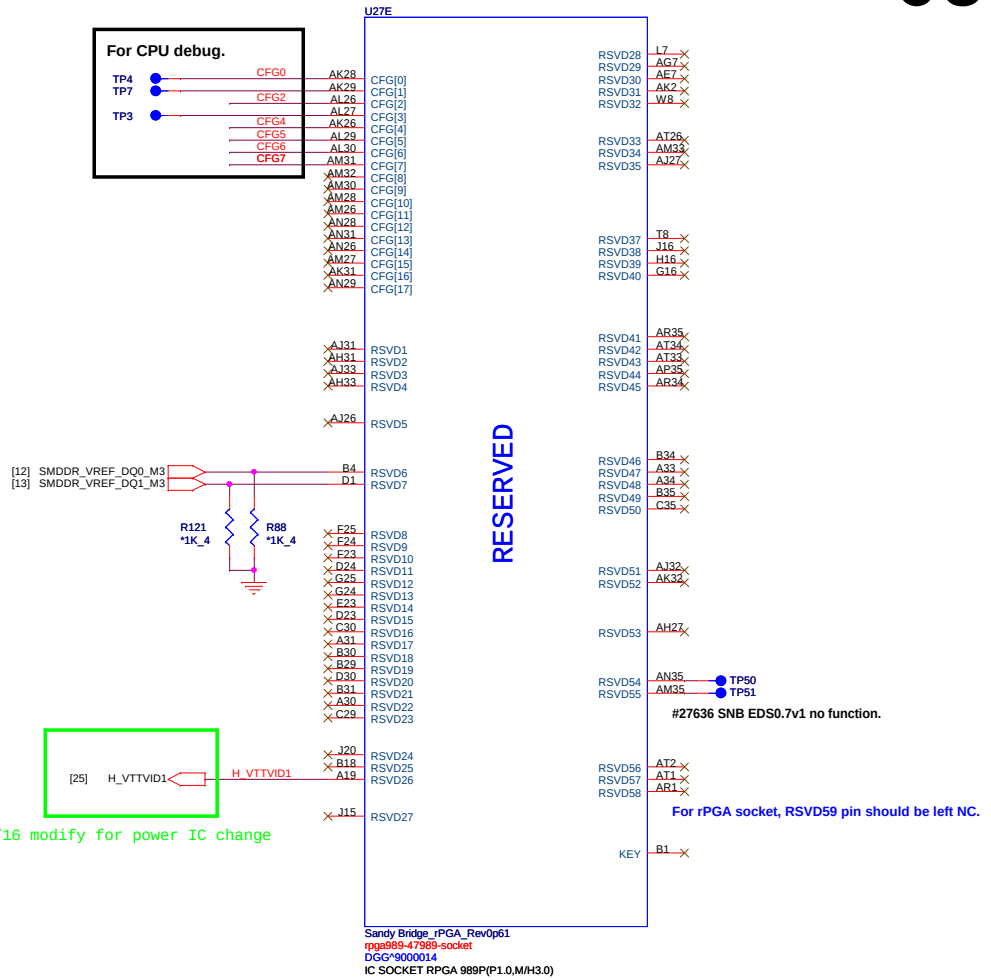
Sandy Bridge Processor (GND)



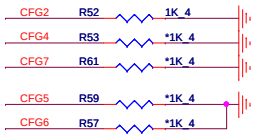
Sandy Bridge Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PROJECT : SWH
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Custom	SNB 4/4 (GND)	1A

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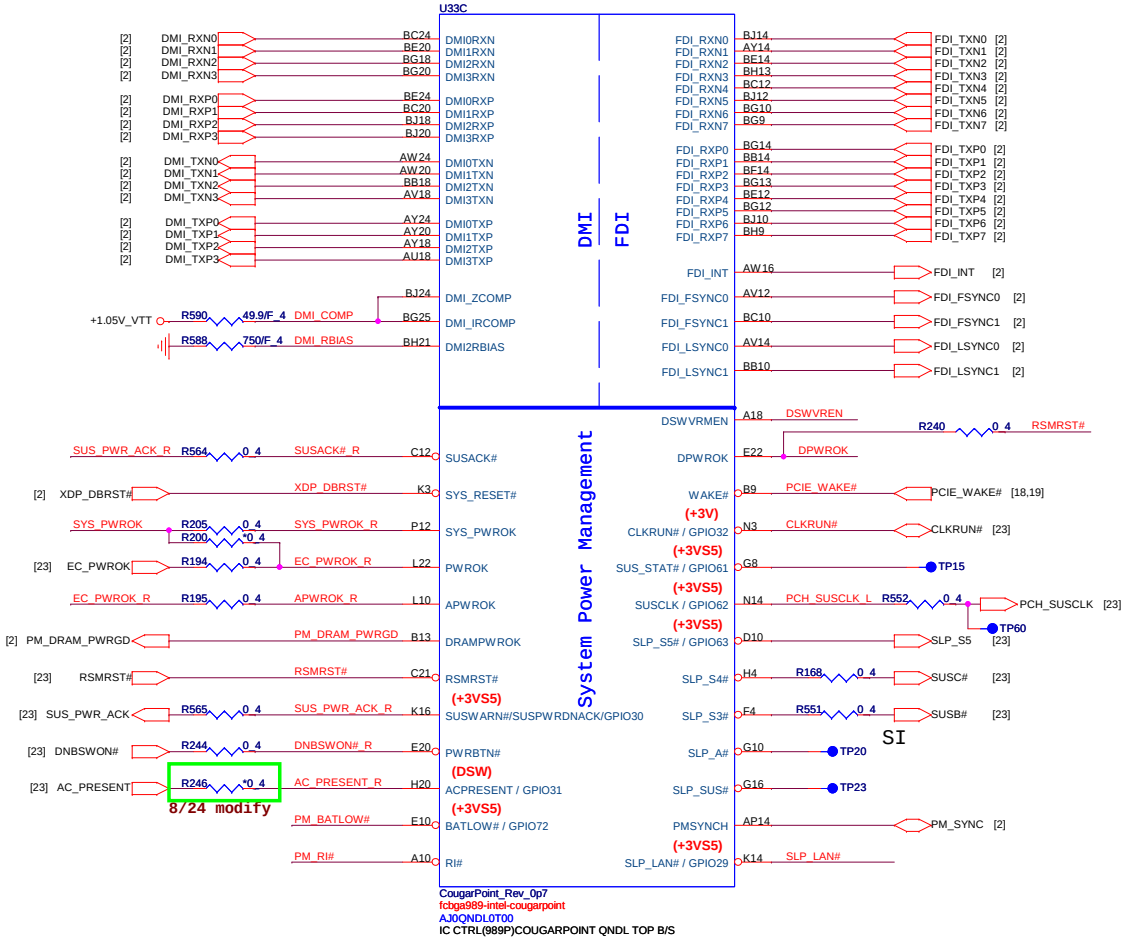
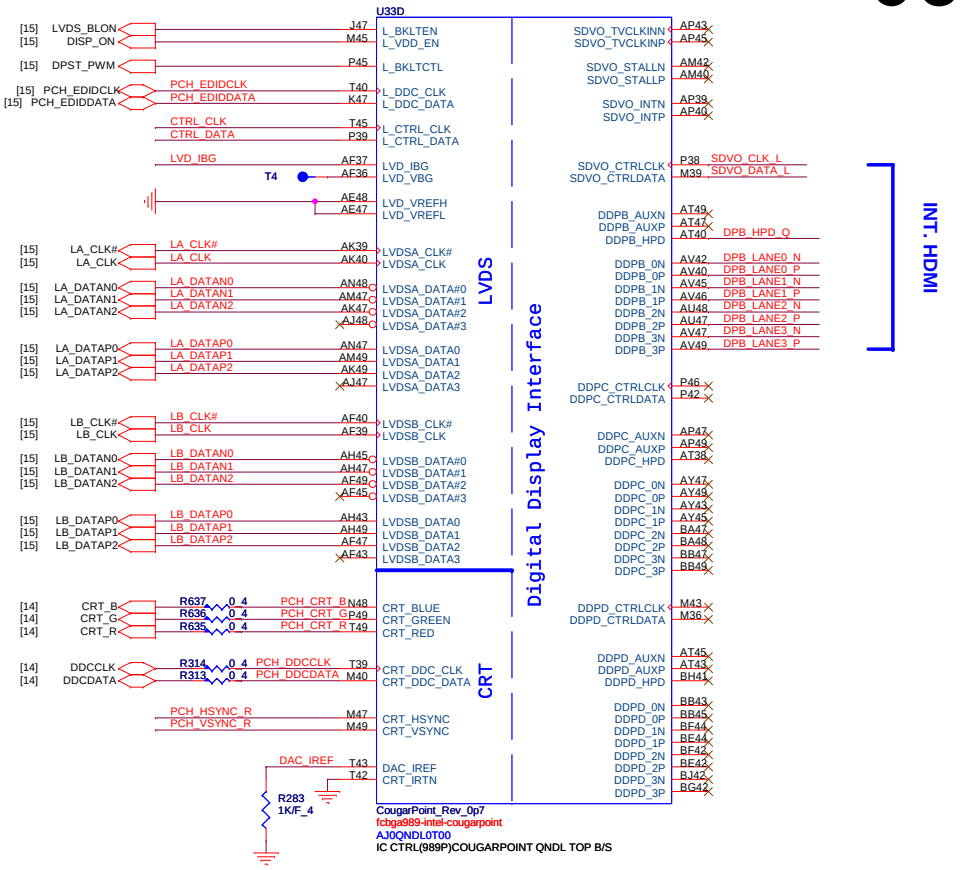
Cougar Point (DMI,FDI,PM)

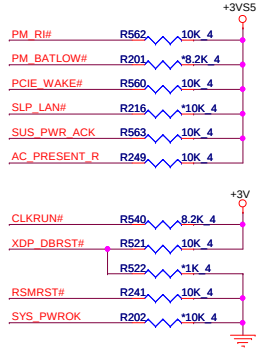


Cougar Point (LVDS,DDI)

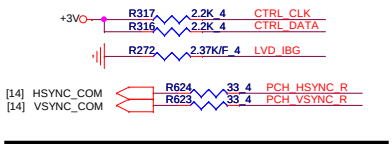


[2,7,8,9,10,12,13,14,15,16,17,18,19,20,21,22,23,26,29] +3V
[2,7,8,9,10,15,22,23,24,25,29,30,31] +3VS5
[7] +3V_DSW
[7,10,23] +3V_RTC
[2,4,7,8,10,23,25,26,30] +1.05V_VTT

PCH Pull-high/low(CLG)

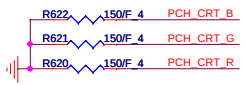


INT LVDS & CRT disable (DIS only remove)

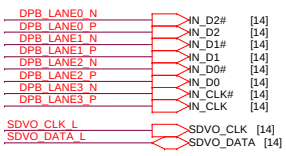


PD Res place close to PCH

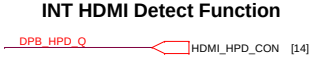
PCH to Res routeing 50 ohm Impedance.
Res to connector filter routeing 37.5ohm Impedance.



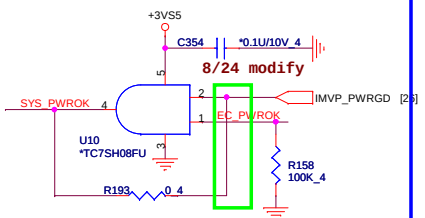
INT HDMI disable (DIS only remove)

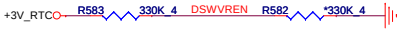


INT HDMI Detect Function



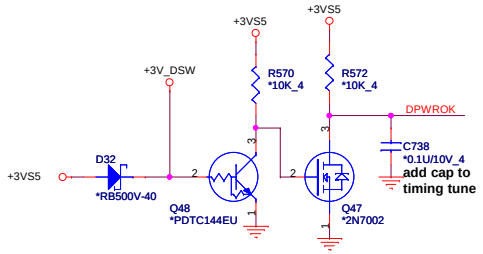
System PWR_OK(CLG)





On Die DSW VR Enable
High = Enable (Default) Low = Disable

DPWROK FOR DSW



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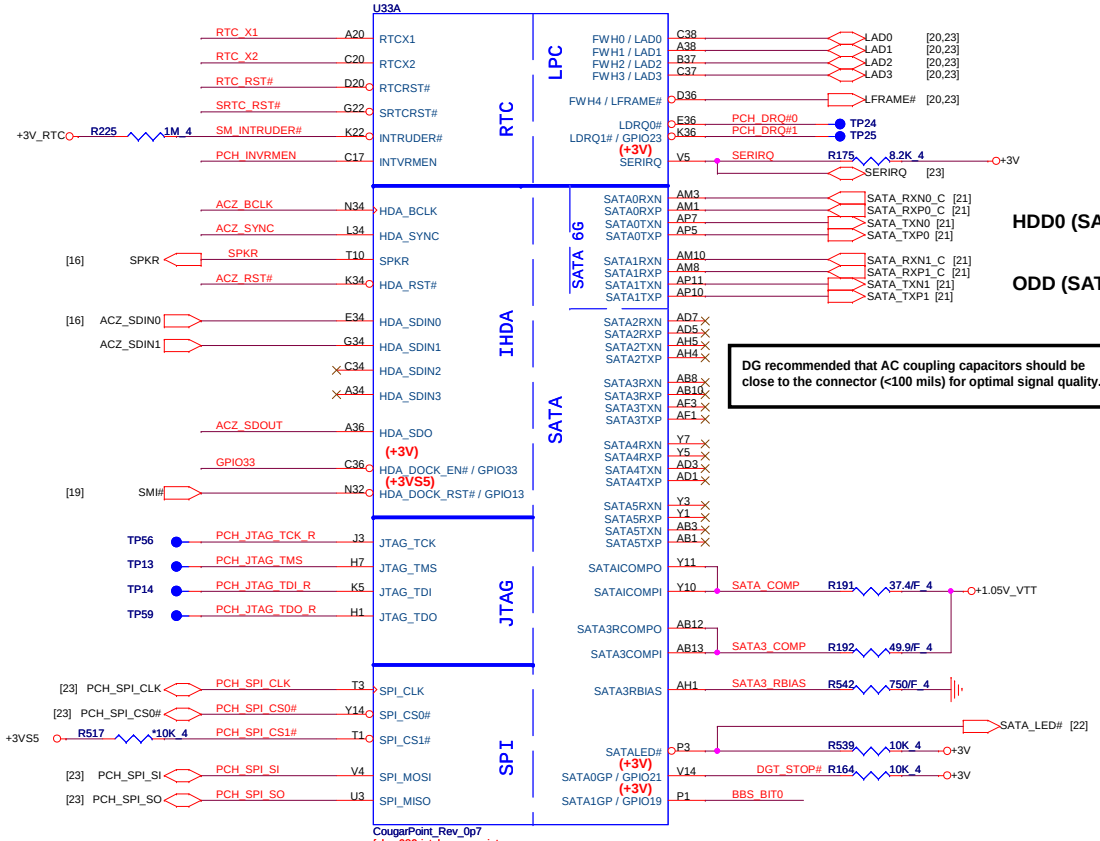
Cougar Point (HDA,JTAG,SATA)



HDD0 (SATA3 6.0Gb/s)

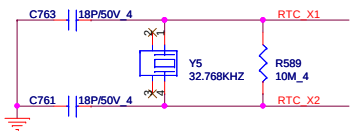
ODD (SATA3 6.0Gb/s)

DG recommended that AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

PCH Strap Table

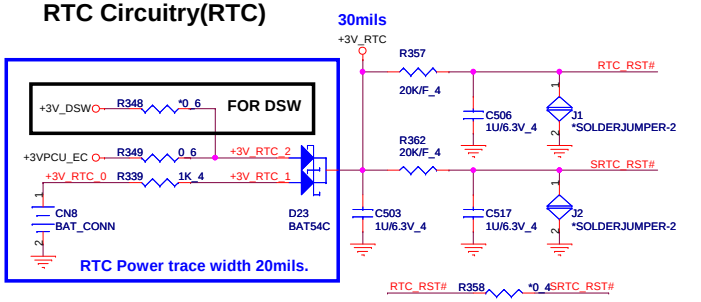
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR Different from Calpella	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R174 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V R617 *1K_4 R627 10K_4 PCI_GNT3# [8]
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R581 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R597 *1K_4 GPIO33_E 8/24 modify
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# 1 0 / GNT0# 1 0 / Boot Location SPI LPC	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK		R518 *1K_4 BBS_BIT0 R615 *1K_4 BBS_BIT1 [8]
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R190 *1K_4 NV_ALE [8]
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R533 2.2K_4 R553 4.7K_4 NV_CLE [8] H_SNB_IVB# [2] N.A at CPT EDS 0.7
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VS5 R277 1K_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	9/15 modify [23] GPIO33_E ACZ_SDOUT R598 *1K_4 +V3.3A_1.5A_HDA_IO
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R561 *1K_4 ICC_EN# [9]
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R157 *1K_4 PLL_ODVR_EN [9]
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R251 1K_4 +3V

RTC Clock 32.768KHz

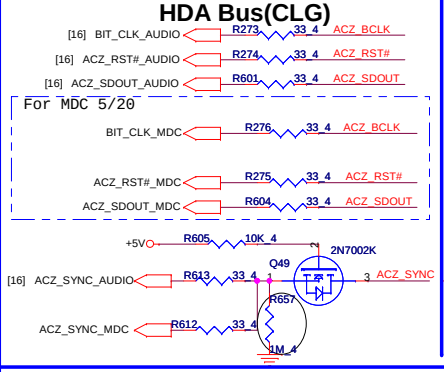


07

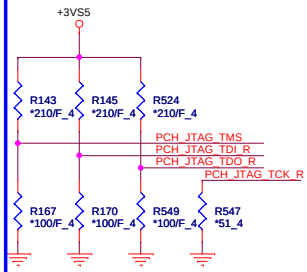
RTC Circuitry(RTC)



HDA Bus(CLG)

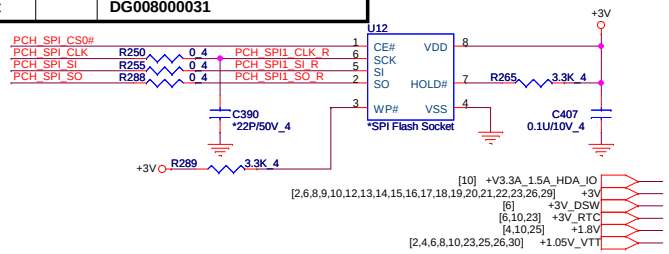


PCH JTAG Debug(CLG)



Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031

PCH SPI ROM(CLG)



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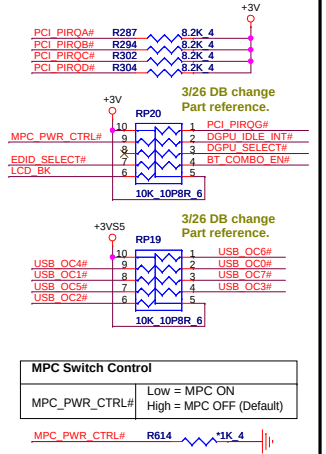
Cougar Point-M (PCI,USB,NVRAM)

Cougar Point-M (PCI-E,SMBUS,CLK)

08

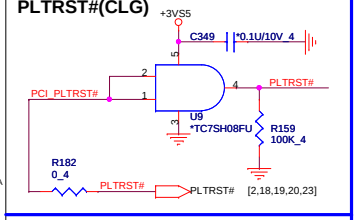
PCI/USBOC# Pull-up(CLG)



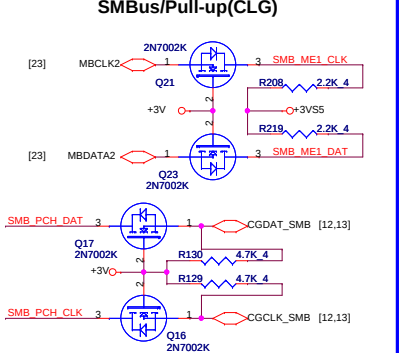
MPC Switch Control	
MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

MPC_PWR_CTRL# R614 *1K_4

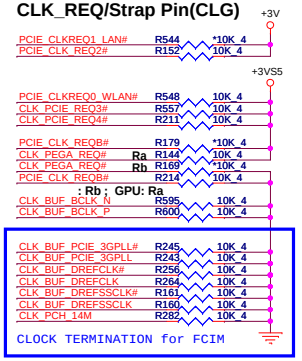
PLTRST#(CLG)



SMBus/Pull-up(CLG)



CLK_REQ/Strap Pin(CLG)

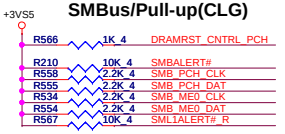


PCIE Clock

3/26 DB change Part reference.

8/26 remove for UMA

SMBus/Pull-up(CLG)



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Custom	PCH 3/6 (PCIE/USB/CLK)	1A
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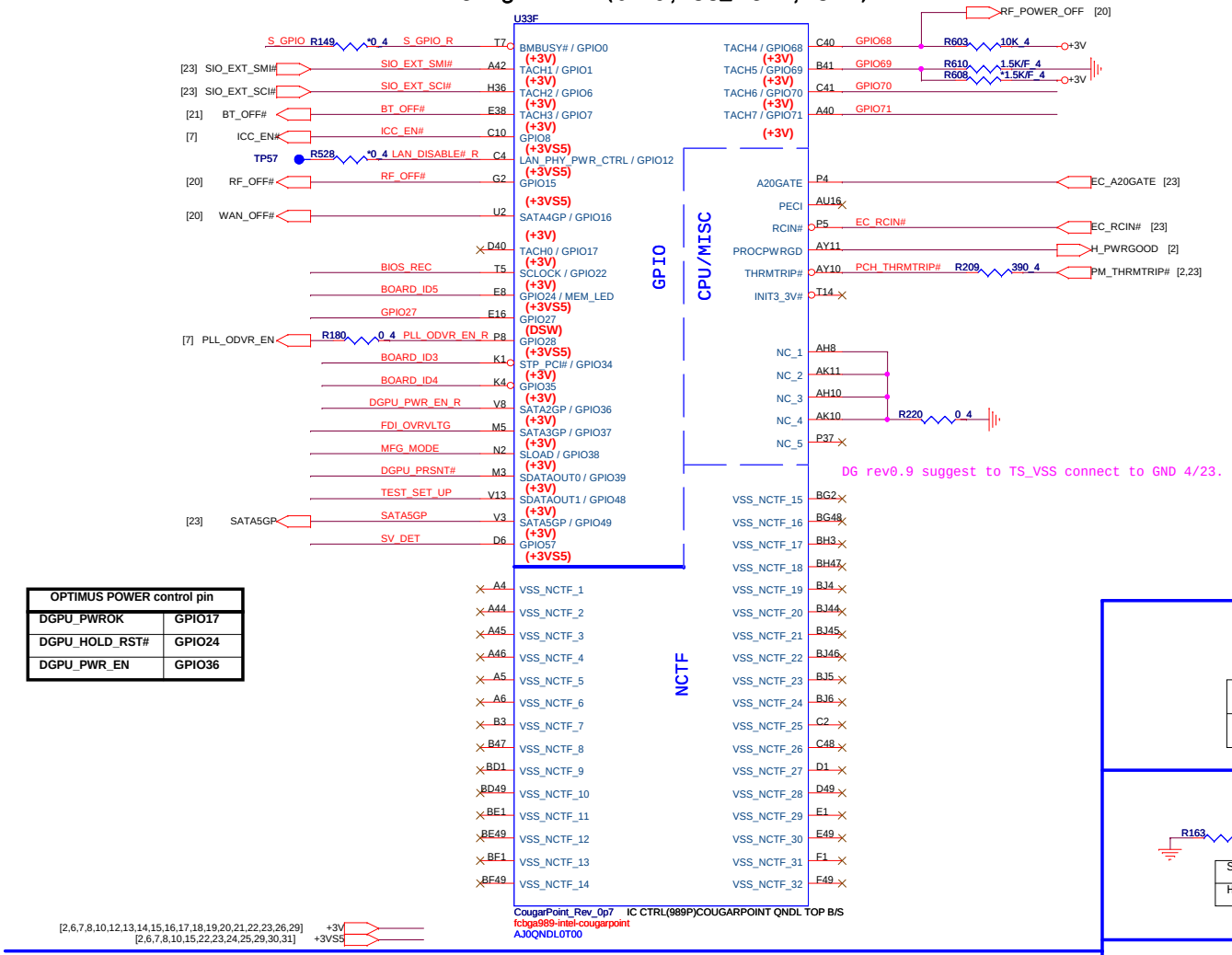
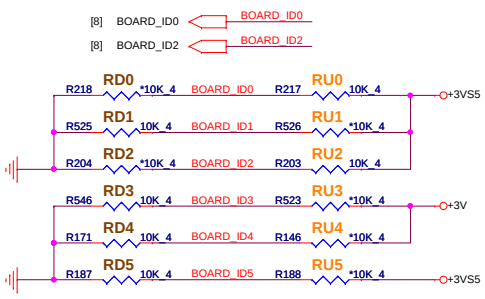
Cougar Point (GPIO,VSS_NCTF,RSVD)



OPTIMUS POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

BOARD ID SETTING

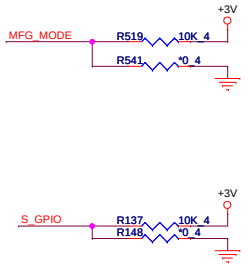
Board ID	ID0	ID1	ID2	ID3	ID4	ID5	ID6
LG/CB	0=LG 1=CB						
15.6"/ 14"			0=QLH/TWH 1=QLC/SWH				
dolby					0=NO 1=YES		



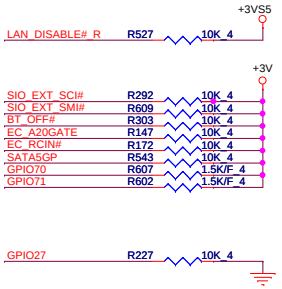
Clock Gen Power OK (CLG)

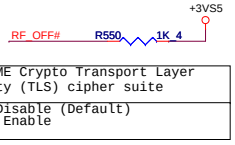
3/26 DB del external clock generator.

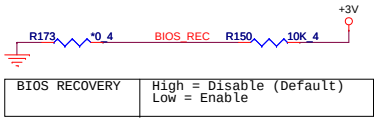
MFG-TEST

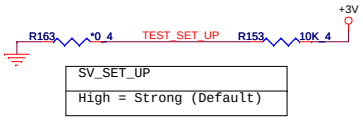


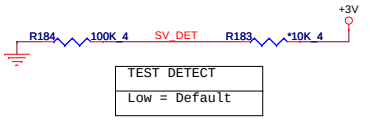
GPIO Pull-up/Pull-down(CLG)

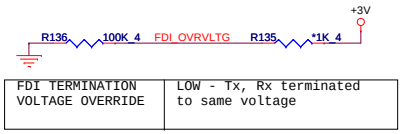




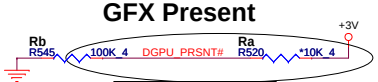








GFX Present



	SG	UMA
Stuff	Ra	Rb
NC	Rb	Ra

PROJECT : SWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	1A
Date: Thursday, October 28, 2010	Sheet 9 of 32	

09

Cougar Point-M (POWER)

COUGAR POINT (POWER)

U33J

Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
MISC
RTC
HDA

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QMZQ0T00
IC CTRL(989P)COUGARPOINT QMVY TOP B/S

U33G

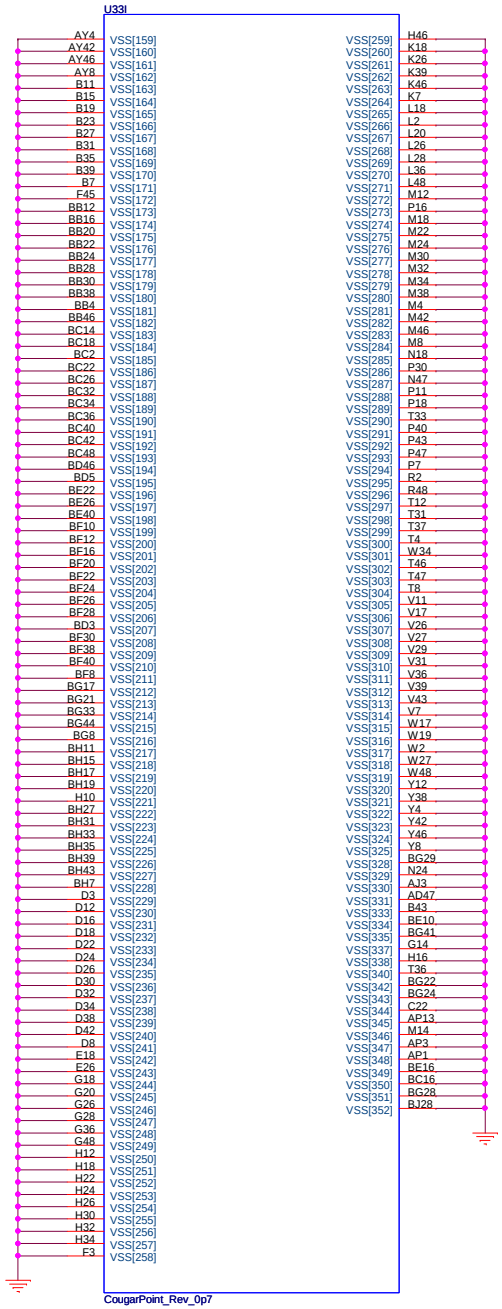
VCC CORE
CRT
LVDS
HVCMOS
DMI
VCCIO
FDI
NAND / SPI

CougarPoint_Rev_0p7
fcbga989-intel-cougarpoint
AJ0QNDL0T00
IC CTRL(989P)COUGARPOINT QNDL

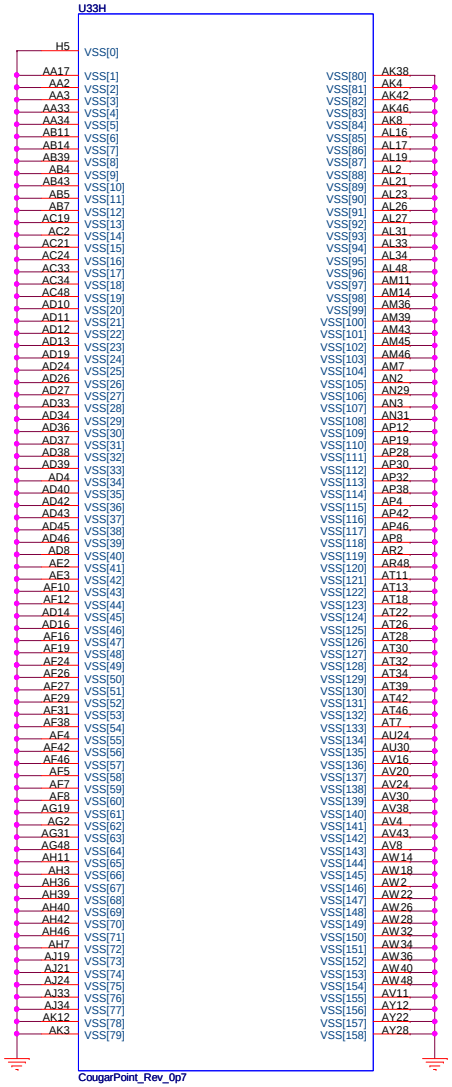
SG & UMA : Ra
DIS : Rb

PROJECT : SWH	Quanta Computer Inc.
Size: Custom	Document Number: PCH 5/6 (POWER)
Rev: 1A	
Date: Thursday, October 28, 2010	Sheet 10 of 32

IBEX PEAK-M (GND)

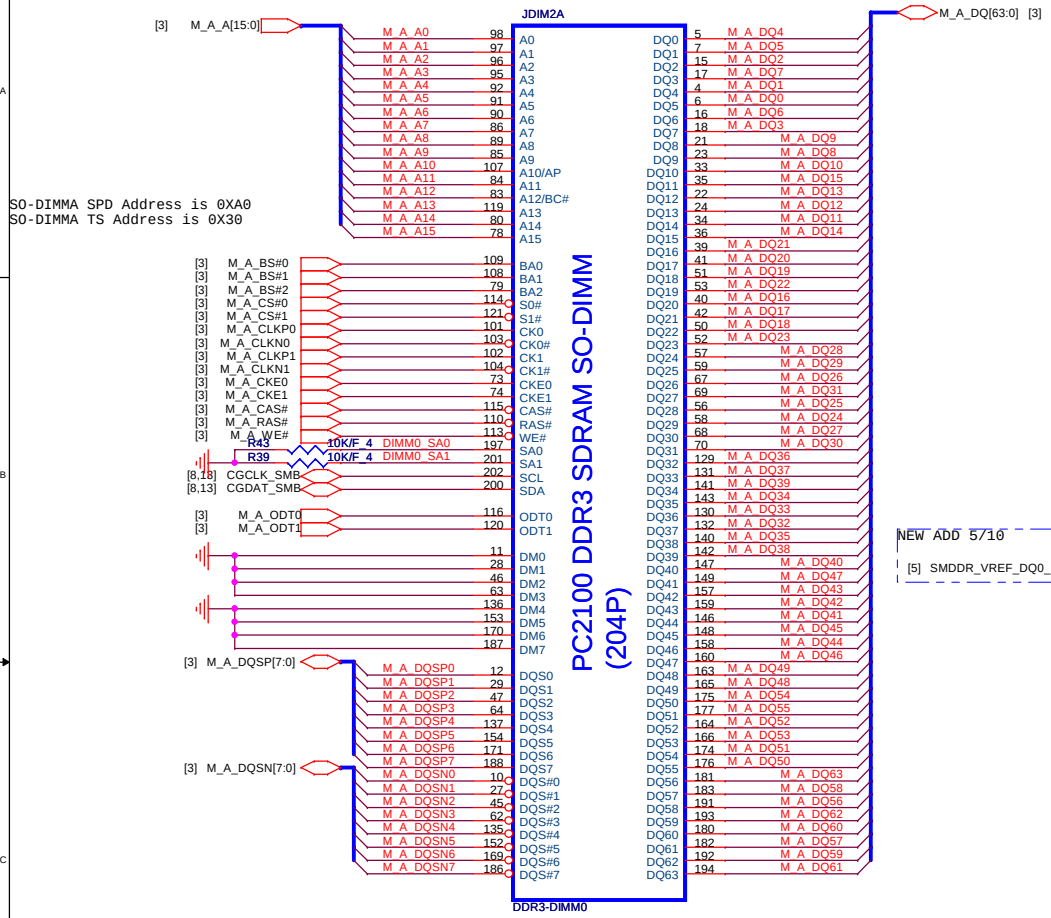


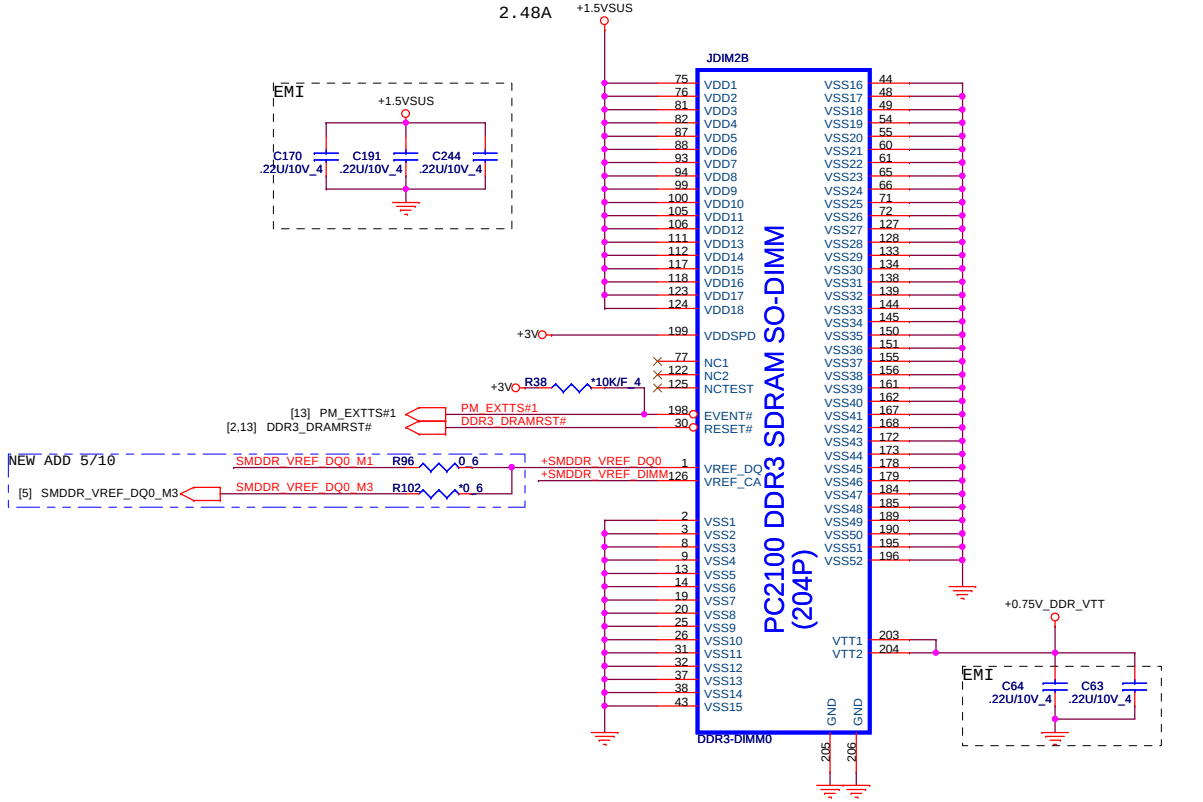
IBEX PEAK-M (GND)



PROJECT : SWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 6/6 (GND)	1A
Date: Monday, October 04, 2010	Sheet 11 of 32	

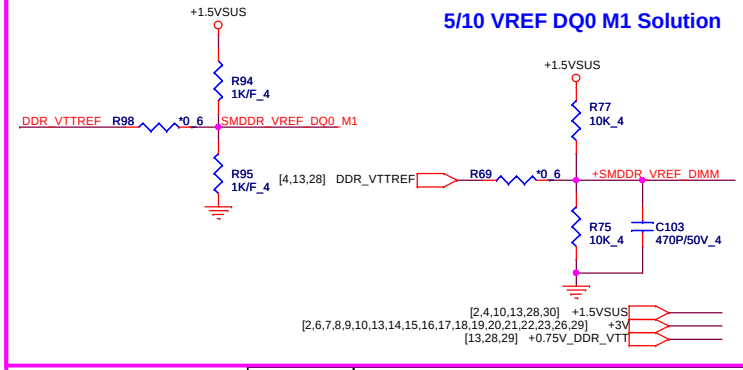




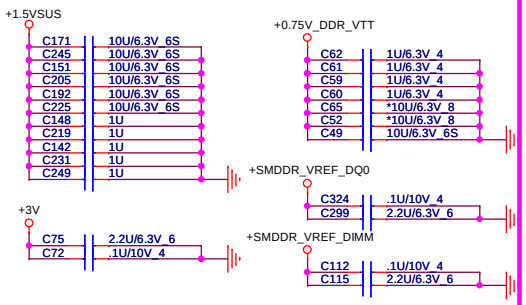
6/22:Document Number: 436996
Intel remove the DDR3 verf M2
circuitry

VREF DQ0 M2 Solution

5/10 VREF DQ0 M1 Solution

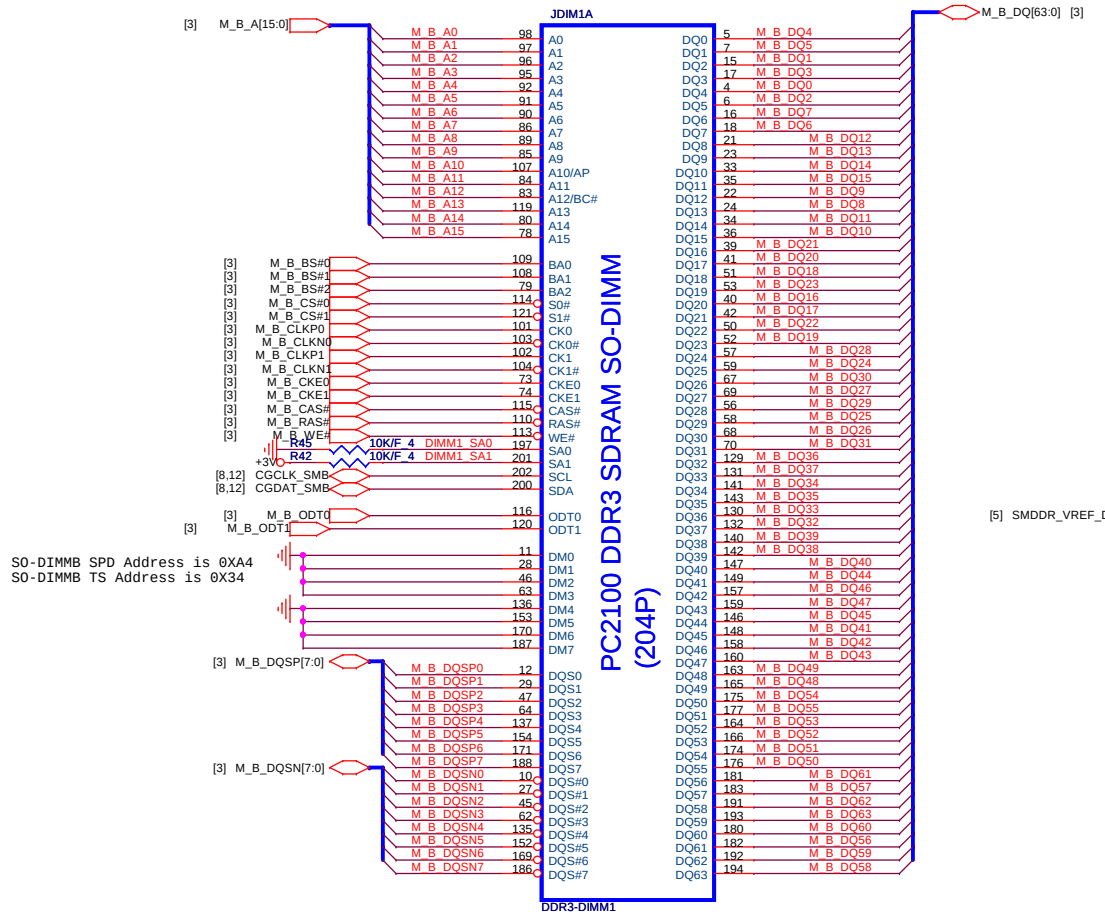


Place these Caps near So-Dimm0. 11/6

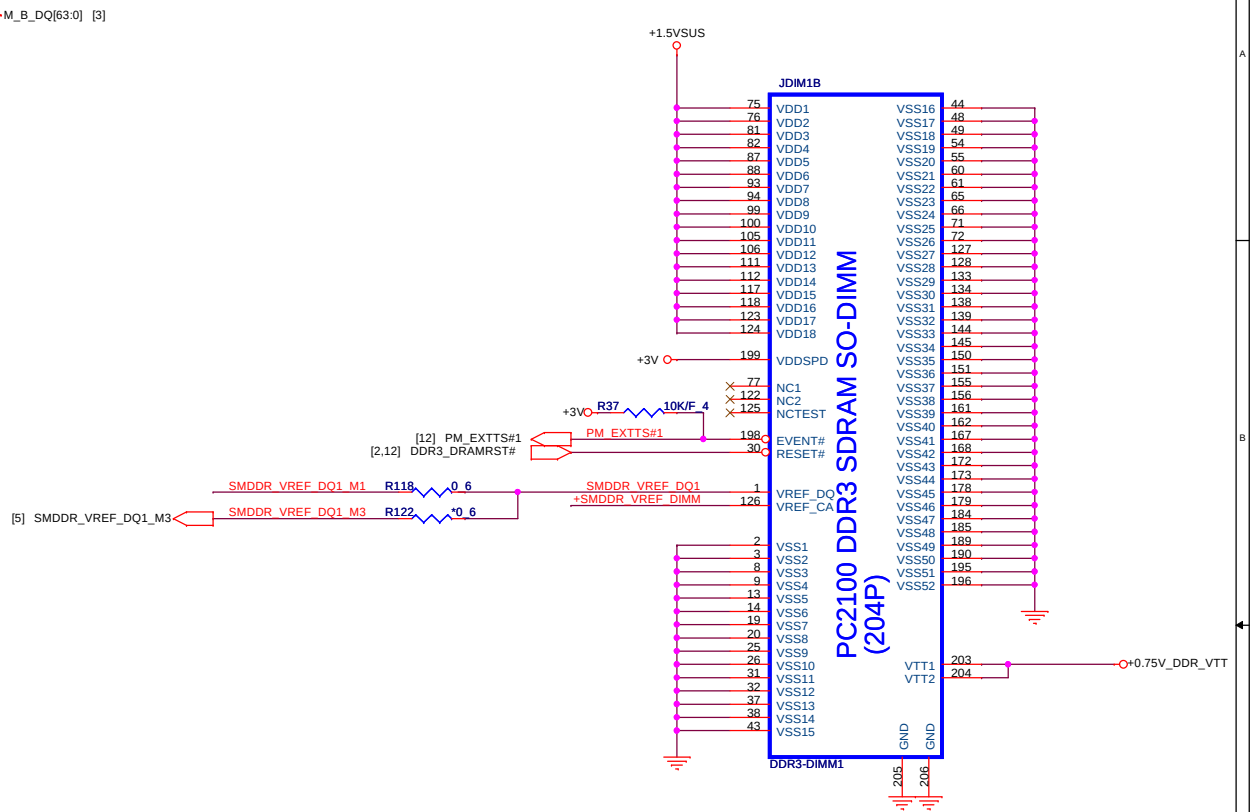


PROJECT : SWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-0	1A
Date: Thursday, October 28, 2010	Sheet 12 of 32	



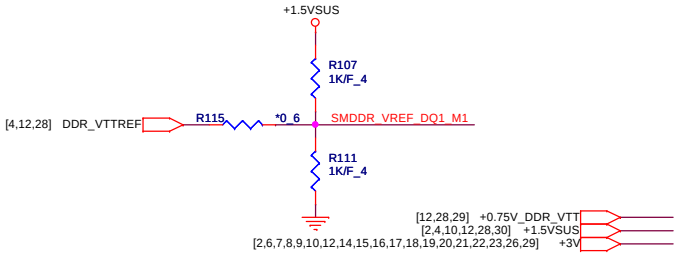
SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34



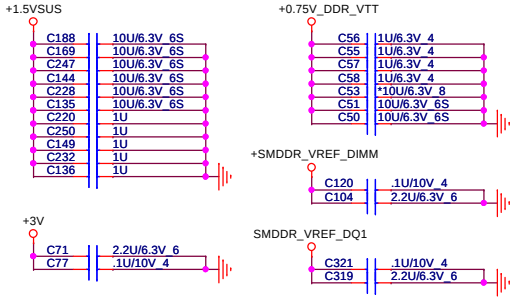
6/22:Document Number: 436996
Intel remove the DDR3 verf M2 circuitry

VREF DQ1 M2 Solution

VREF DQ1 M1 Solution



Place these Caps near So-Dimm1.



PROJECT : SWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-1	1A

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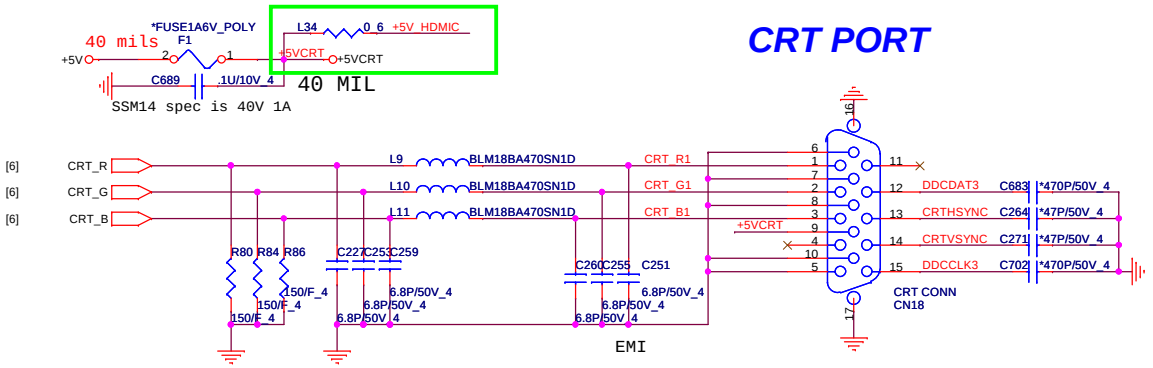
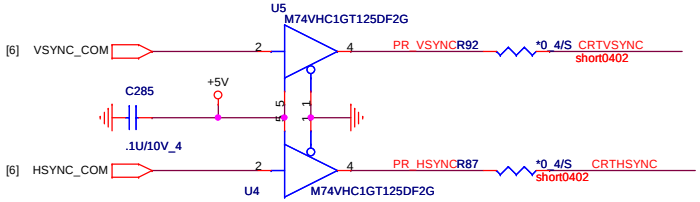
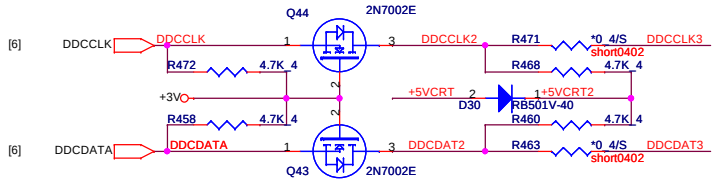
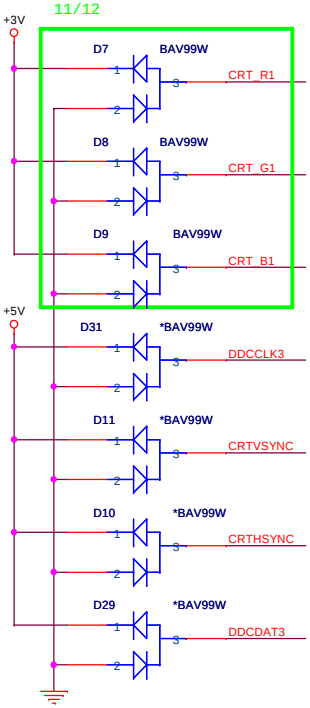
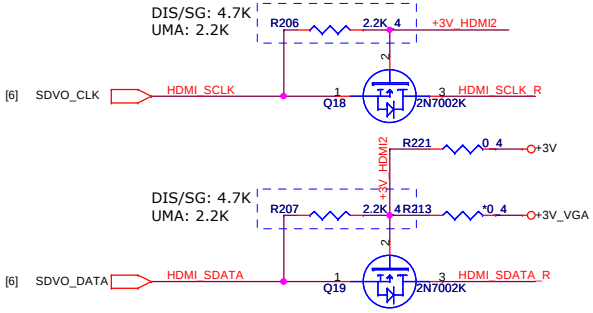
CRT PORT

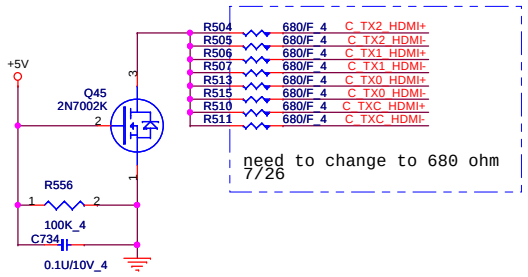


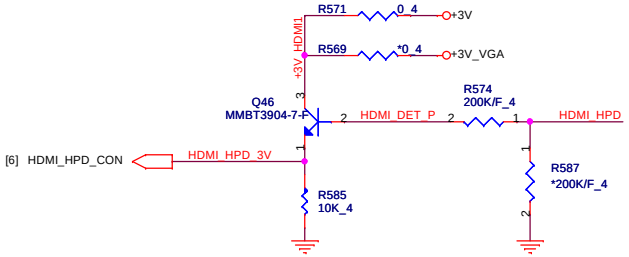




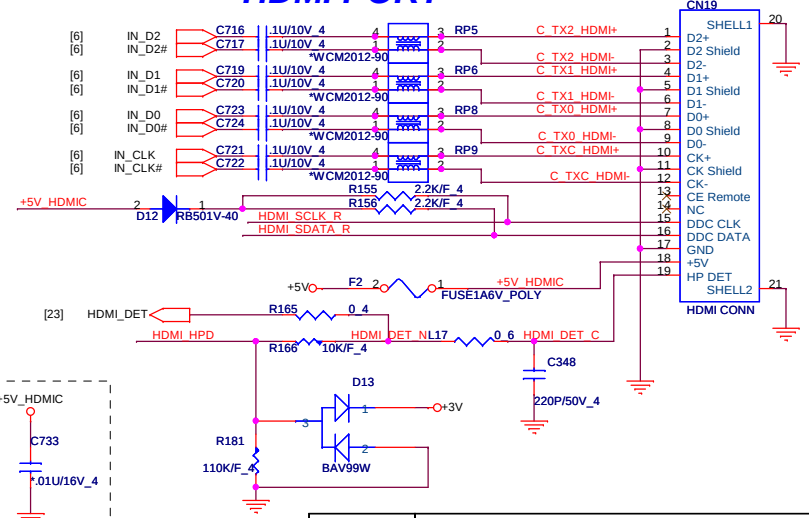








HDMI PORT



for EMI request

[2,6,7,8,9,10,12,13,15,16,17,18,19,20,21,22,23,26,29] +3V
[7,10,15,16,17,20,21,22,29,32] +5V

PROJECT : SWH
Quanta Computer Inc.

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Custom	CRT/HDMI Conn	1A
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5/18 Change to from PCH output control

DPST_PWM DISP_ON LVDS_BLON EDIDCLK

EDIDDATA

0820 add camera function

CAMERA

MIC

0520 add for cost down +5VSUS

14.5v

AO3404 ID current 5.8A

Close to EC

Close to Pin3

EMI

SI-2 modified for fix camera power fail

Vout=1.25(1+R1/R2)

1. NBSWON1#
2. GND
3. GND
4. LID_EC#
5. +3V
6. +3VPCU

PROJECT : SWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN	1A
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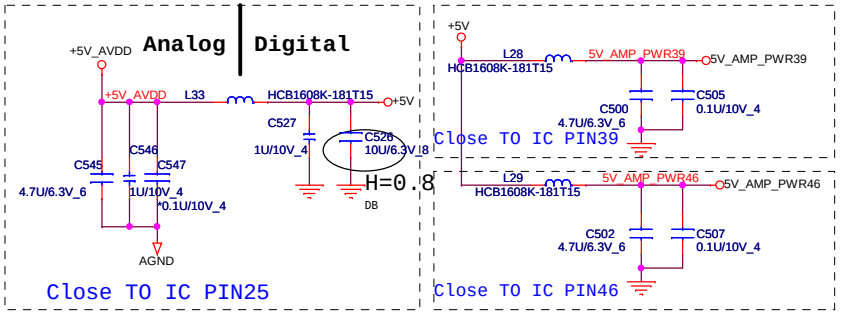
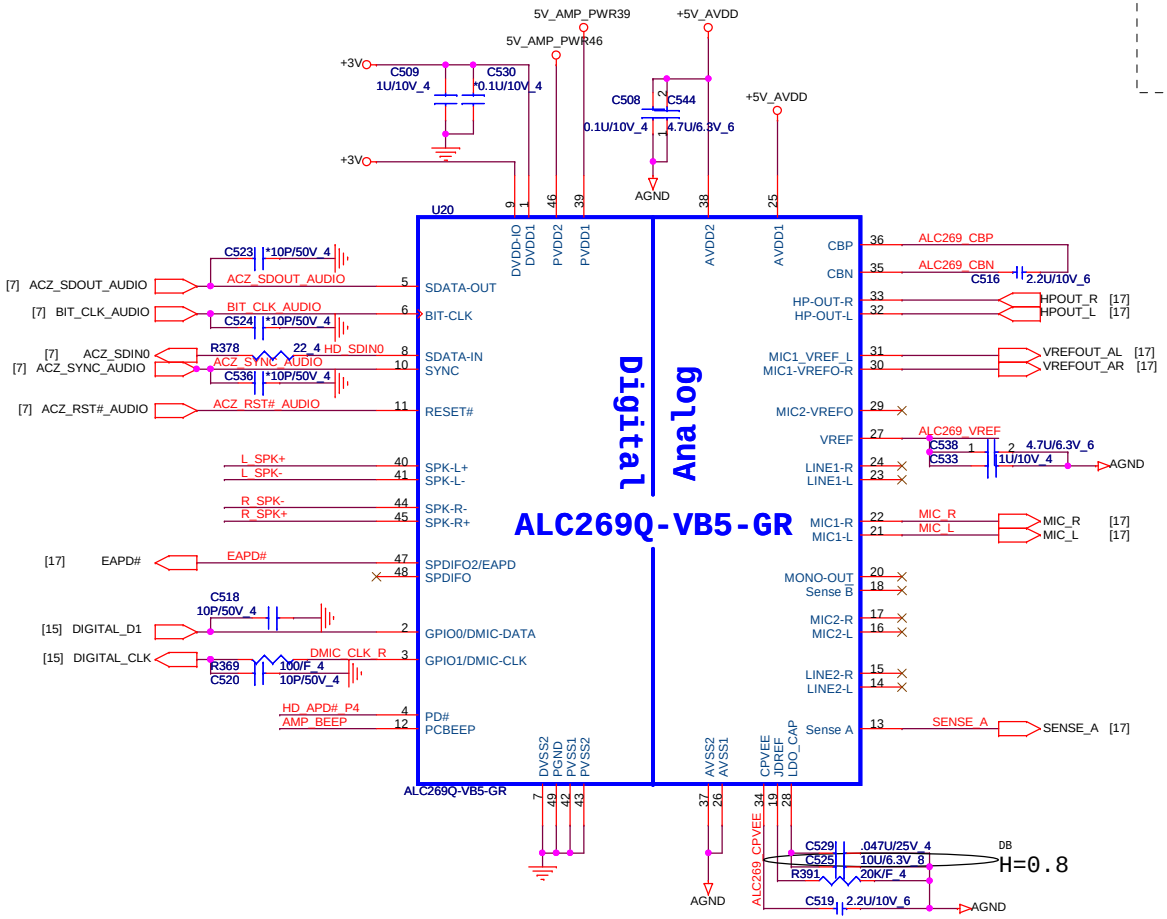
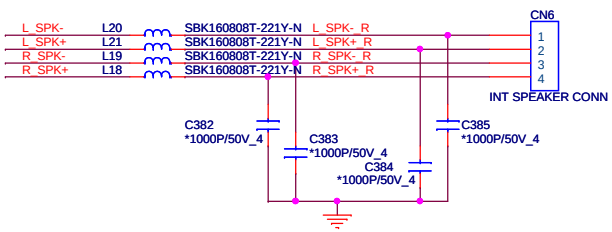
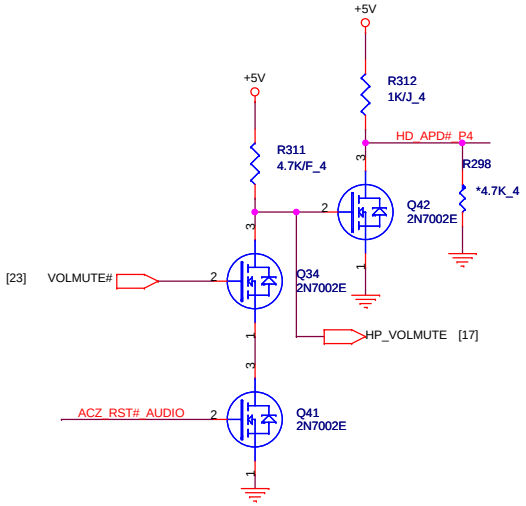
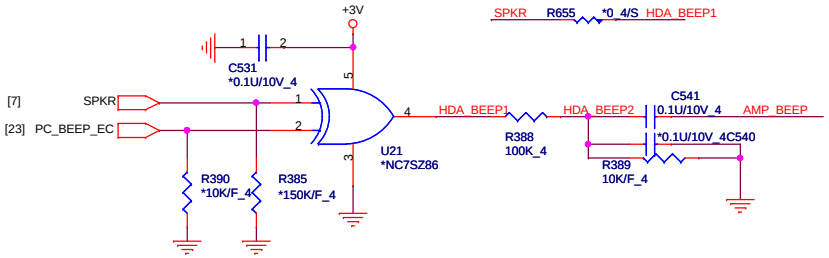


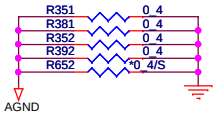


INT. SPEAKER









PROJECT : SWH
Quanta Computer Inc.

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Custom	ALC269Q-VB5-GR	2A

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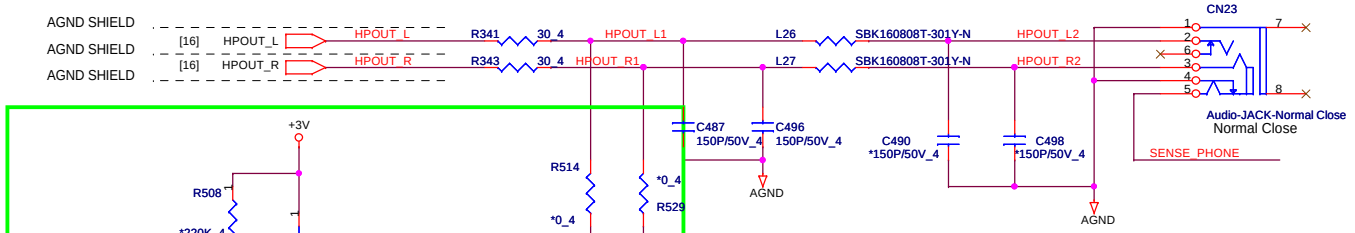
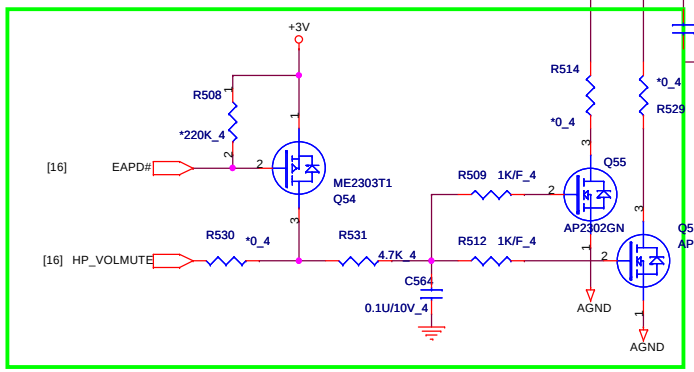
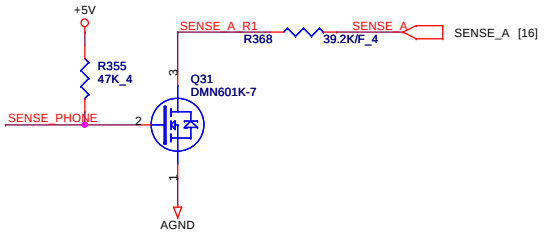
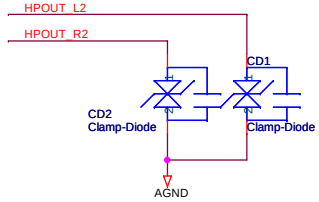
Line out



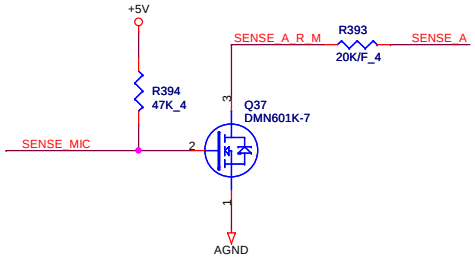


9/1 modify

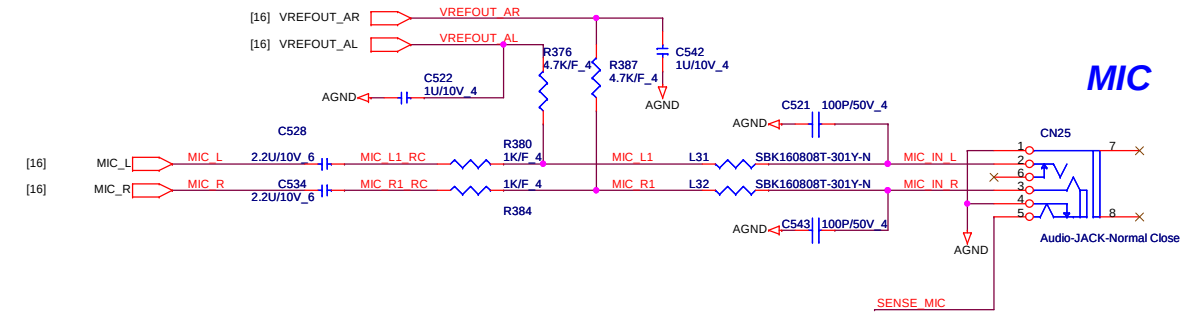


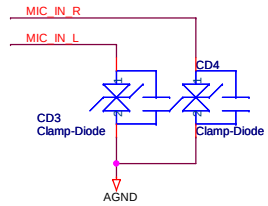


20100421 modify:
CD1, CD2, CD3 and CD4 change to CYPGB101B00 from CY000050B00 for Audio EA.



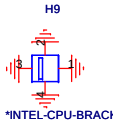
MIC



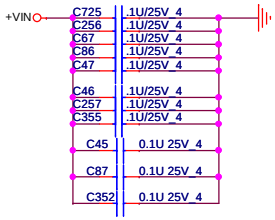


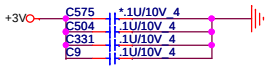
[7,10,14,15,16,20,21,22,29,32] +5V
[2,6,7,8,9,10,12,13,14,15,16,18,19,20,21,22,23,26,29] +3V

CPU bracket Hole.

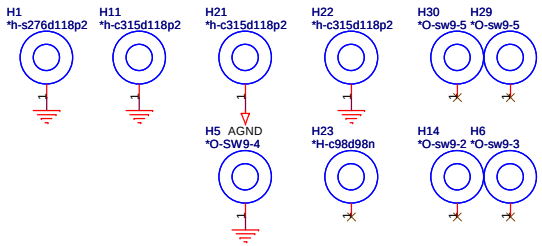


EMI capacitive

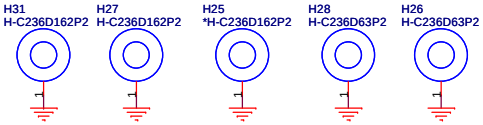




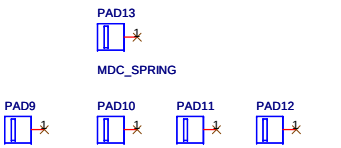
PAD and HOLE

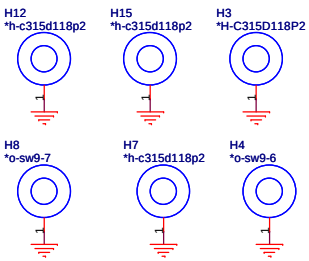


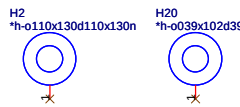
MINI CARD Hole on BOT Side

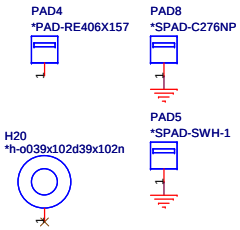


Modem SPRING

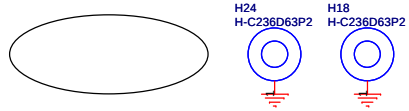








MDC/SB Hole on TOP Side



PROJECT : SWH
Quanta Computer Inc.

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Custom	AUDIO JACK/MDC/LED	1A

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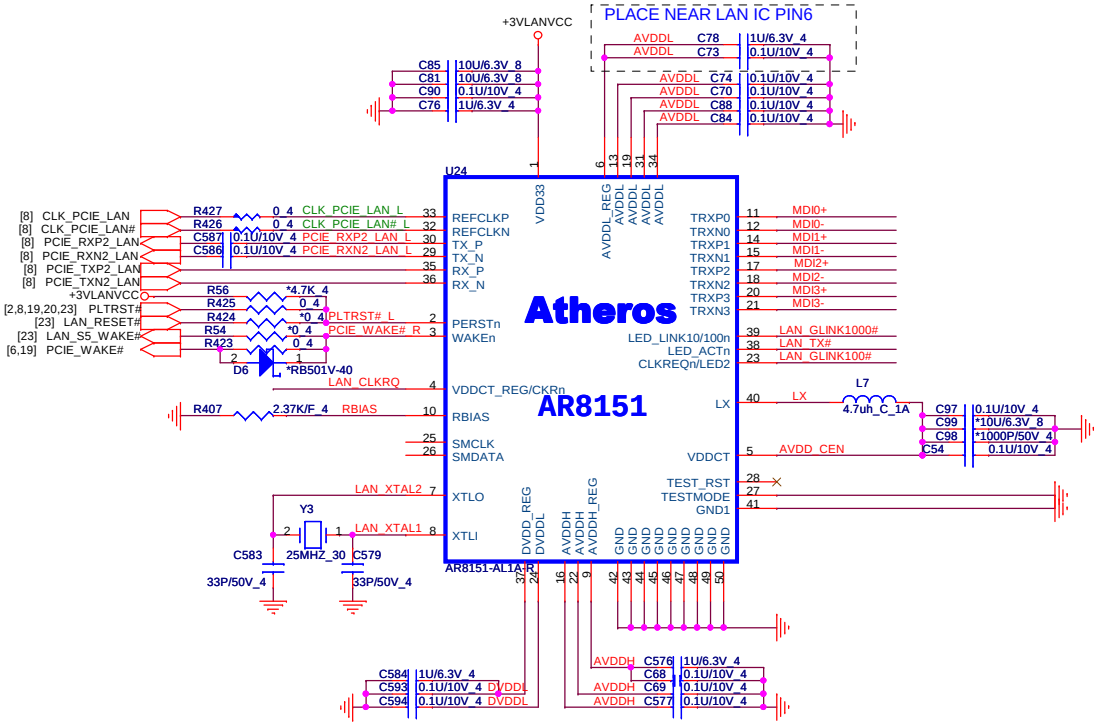
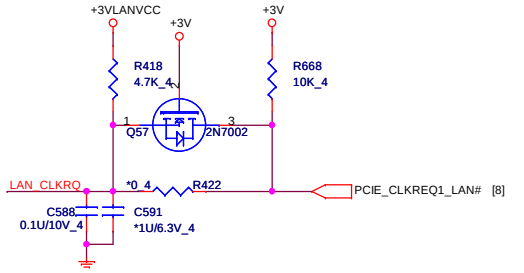
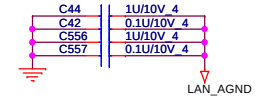
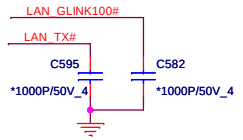
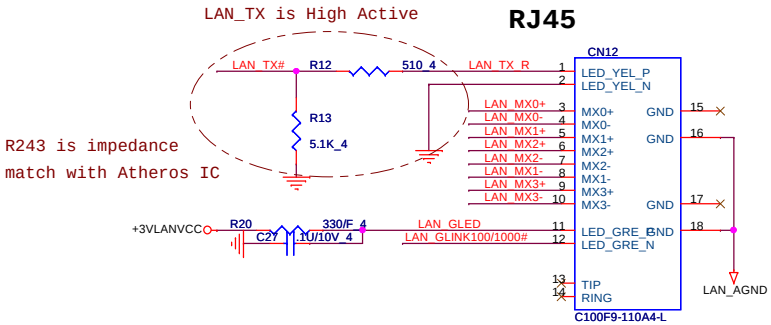


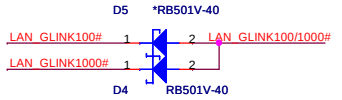


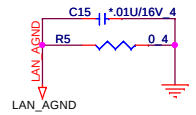




Lan Connector

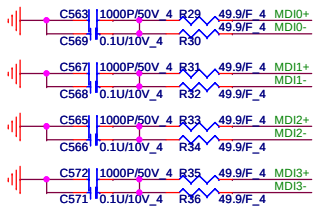


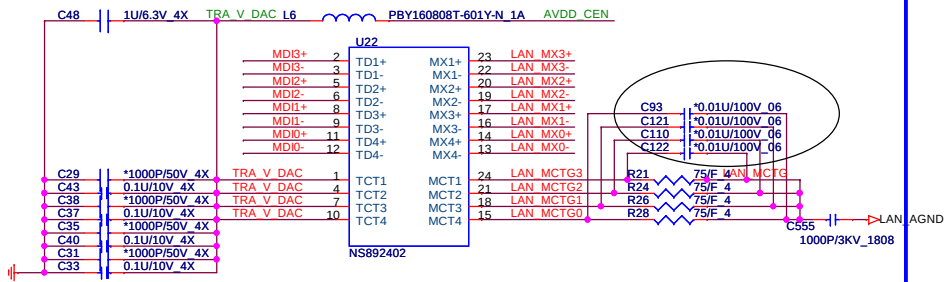




Transformer for 10/100/1000

PLACE NEAR LAN IC SIDE





for Atheros

NS892402:GIGABIT DB0AT9LAN05
NS892405:10/100 DB0ZB1LAN04

[2,6,7,8,9,10,12,13,14,15,16,17,19,20,21,22,23,26,29] +3V
[29] +3VLANVCC

PROJECT : SWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN AR8151	1A
Date: Thursday, October 28, 2010	Sheet 18 of 32	

VIA VL801

PORT1
PORT2
PORT3
PORT4

U13

USB3.0/USB2.0 COMBO

USB3.0 PORT1

USB3.0 PORT2

close USB3

close to chipset

U14 G547E2P81U

U17 W25X40BVSNIG

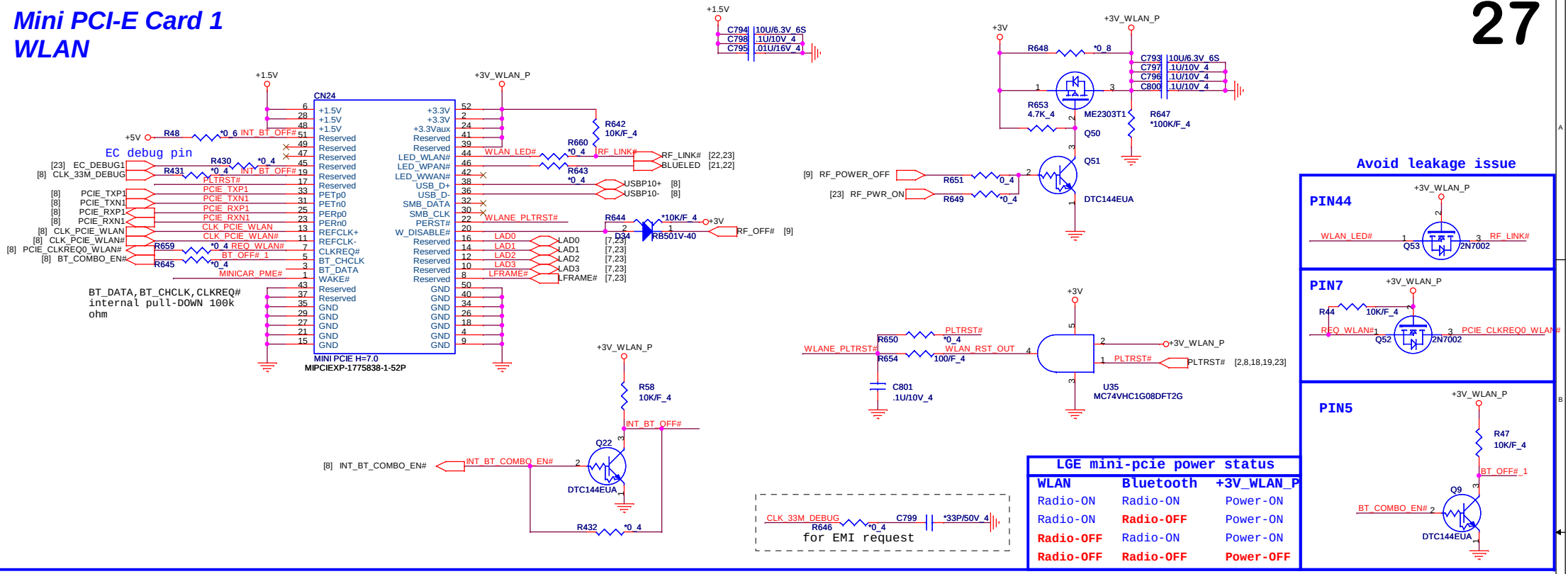
150 mils (Iout=2.5A)

Low: Enable AC Mode
High: Disable DC Mode

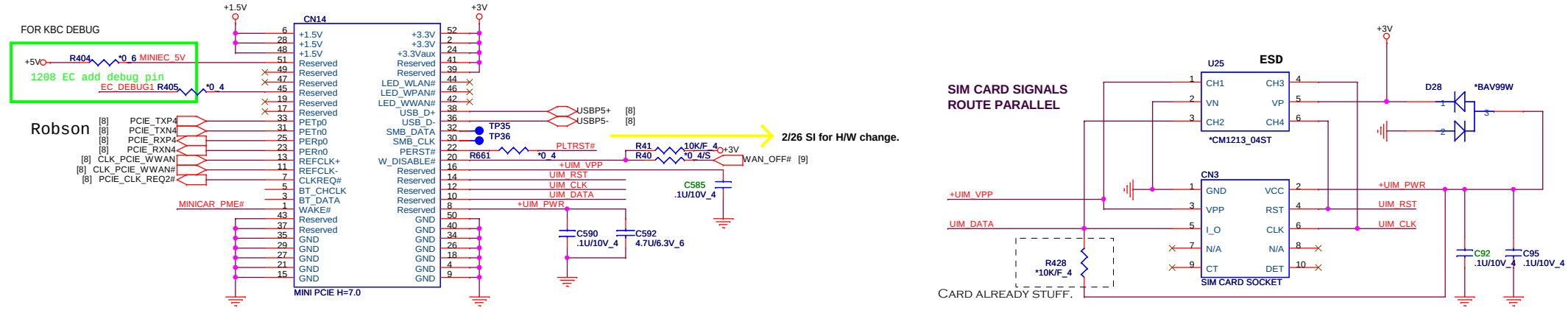
PROJECT : SWH
Quanta Computer Inc.

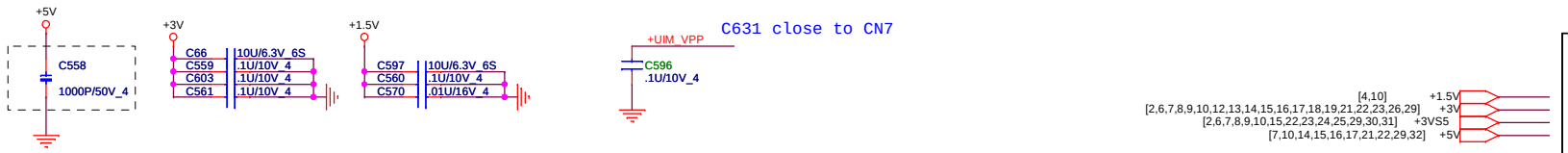
Size	Document Number	Rev
Custom	USB 3.0_VIA VL801	1A
Date: Tuesday, November 02, 2010	Sheet 19 of 32	

Mini PCI-E Card 1
WLAN



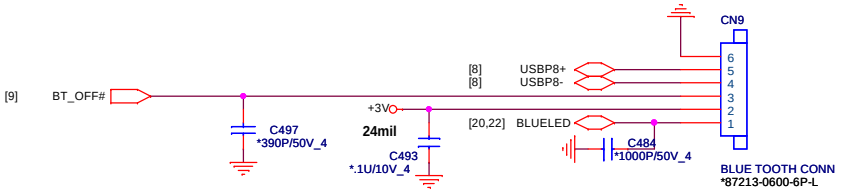
Mini PCI-E Card 2



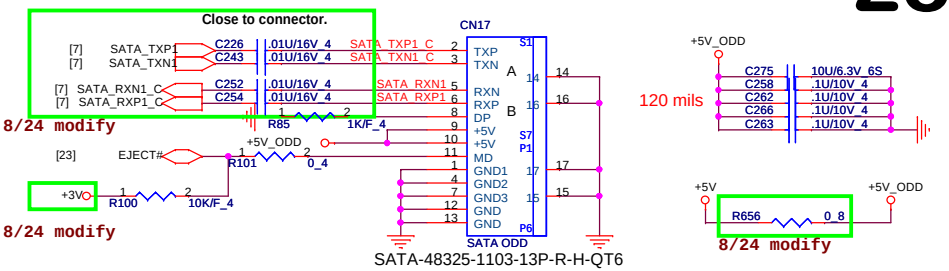


PROJECT : SWH	
Quanta Computer Inc.	
Size: Custom	Document Number: MINI PCIE CONN X2
Rev: 1A	
Date: Thursday, October 28, 2010	Sheet 20 of 32

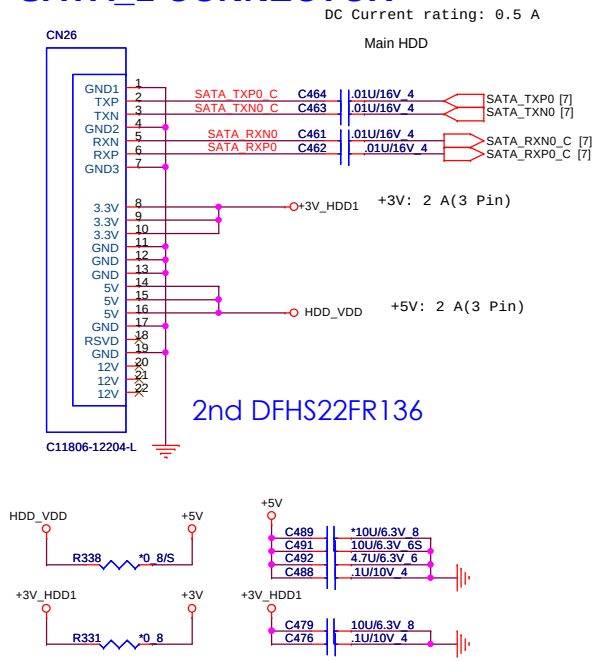
Bluetooth



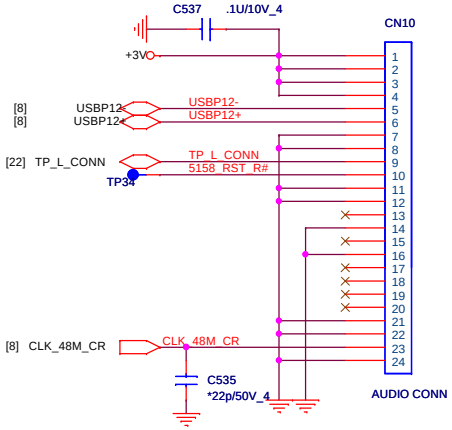
SATA ODD



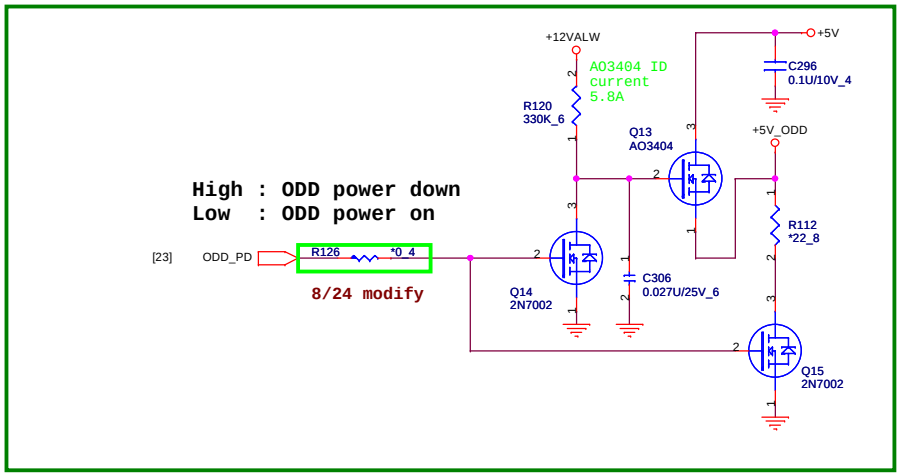
SATA_1 CONNECTOR



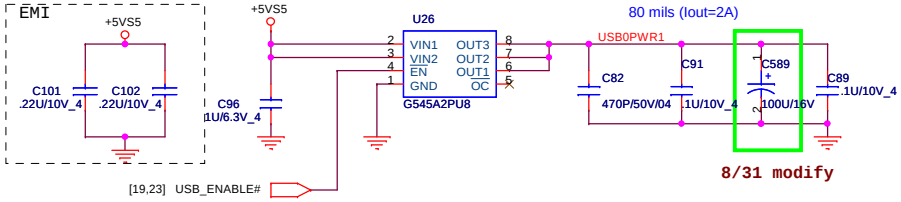
M/B to Cardreader samall board

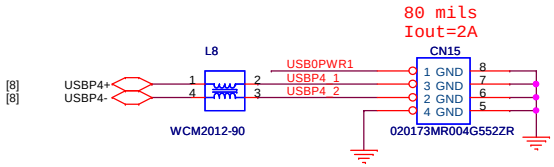


PV Change CN2 footprint 88501-2001-24p-l-nb5



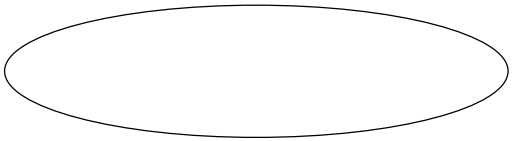
USB CONNECTOR





PQ Add ESD Protector

MDC CONNECTOR

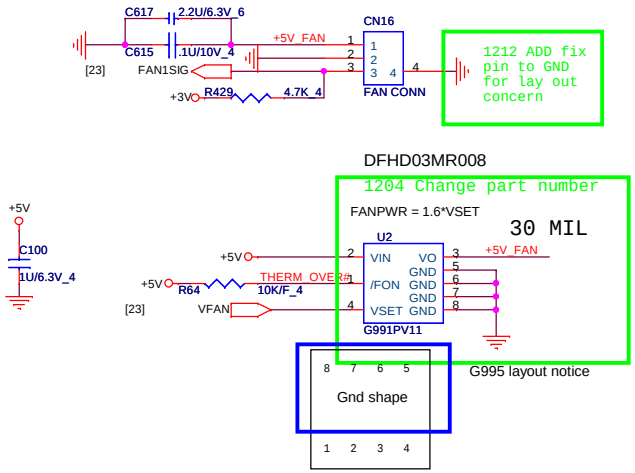


[2,6,7,8,9,10,12,13,14,15,16,17,18,19,20,22,23,26,29] +3V
[7,10,14,15,16,17,20,22,29,32] +5V
[10,19,22,24,25,26,27,28,29,30] +5VS5

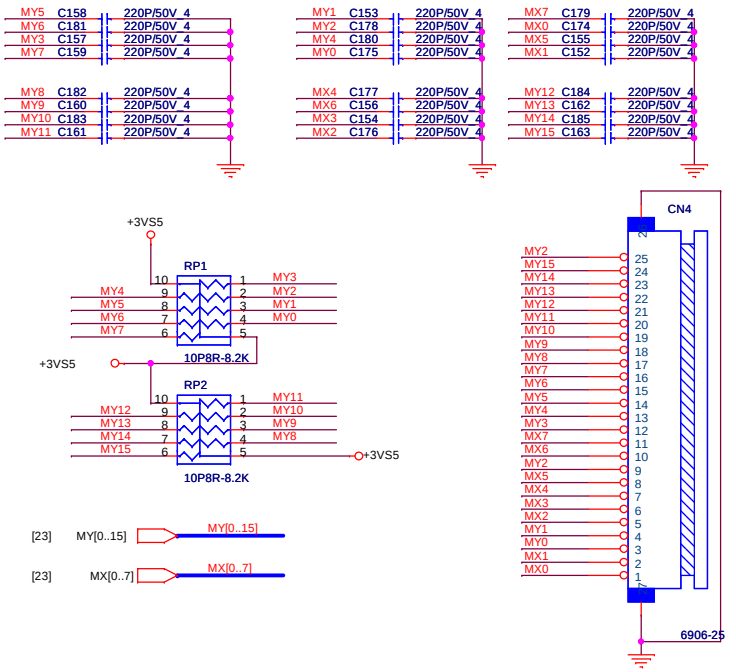
PROJECT : SWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ODD/HDD/NEW CARD/TP	1A
Date: Thursday, October 28, 2010	Sheet 21 of 32	

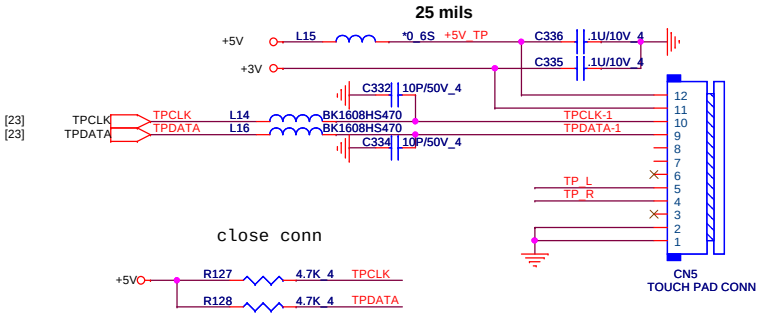
CPU FAN



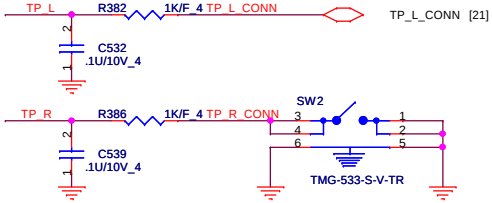
KEYBOARD Con.



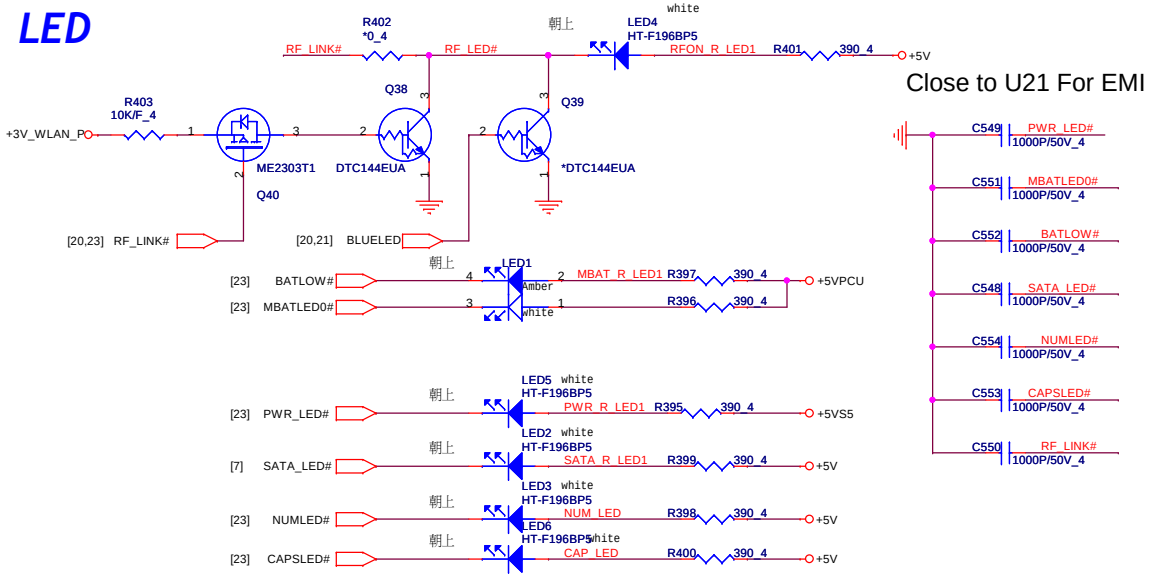
TOUCH PAD CONNECTOR



TOUCH PAD L/R SW1,SW2 in QL2 use, SW3,SW4 in SW9 use



LED



[7,10,14,15,16,17,20,21,29,32] +5V
[2,6,7,8,9,10,12,13,14,15,16,17,18,19,20,21,23,26,29] +3V
[2,6,7,8,9,10,15,23,24,25,29,30,31] +3VS5

PROJECT : SWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB/PWR/FAN/CAM/MIC	1A

Date: Thursday, October 28, 2010 Sheet 22 of 32

IT8518/BX

U18

LPC
GPIO
PS/2
SM_BUS
UART
FLASH
PWM
KBMX
WAKE UP
A/D D/A
CLOCK

IT8518E

Layout Note:
Place all capacitors close to IT8502N.

12 MILS

Select Pin

	SWH Select
LG	Ra
CB	Rb

For Battery charge/charge and cap board

For PCH SMB/DDR Thermal IC/VGA

thermal shutdown circuit

PV Change

For UMA only

Mount for Optimus

For SG/DIS

7/27:Add R399 for EC request

SPI FLASH

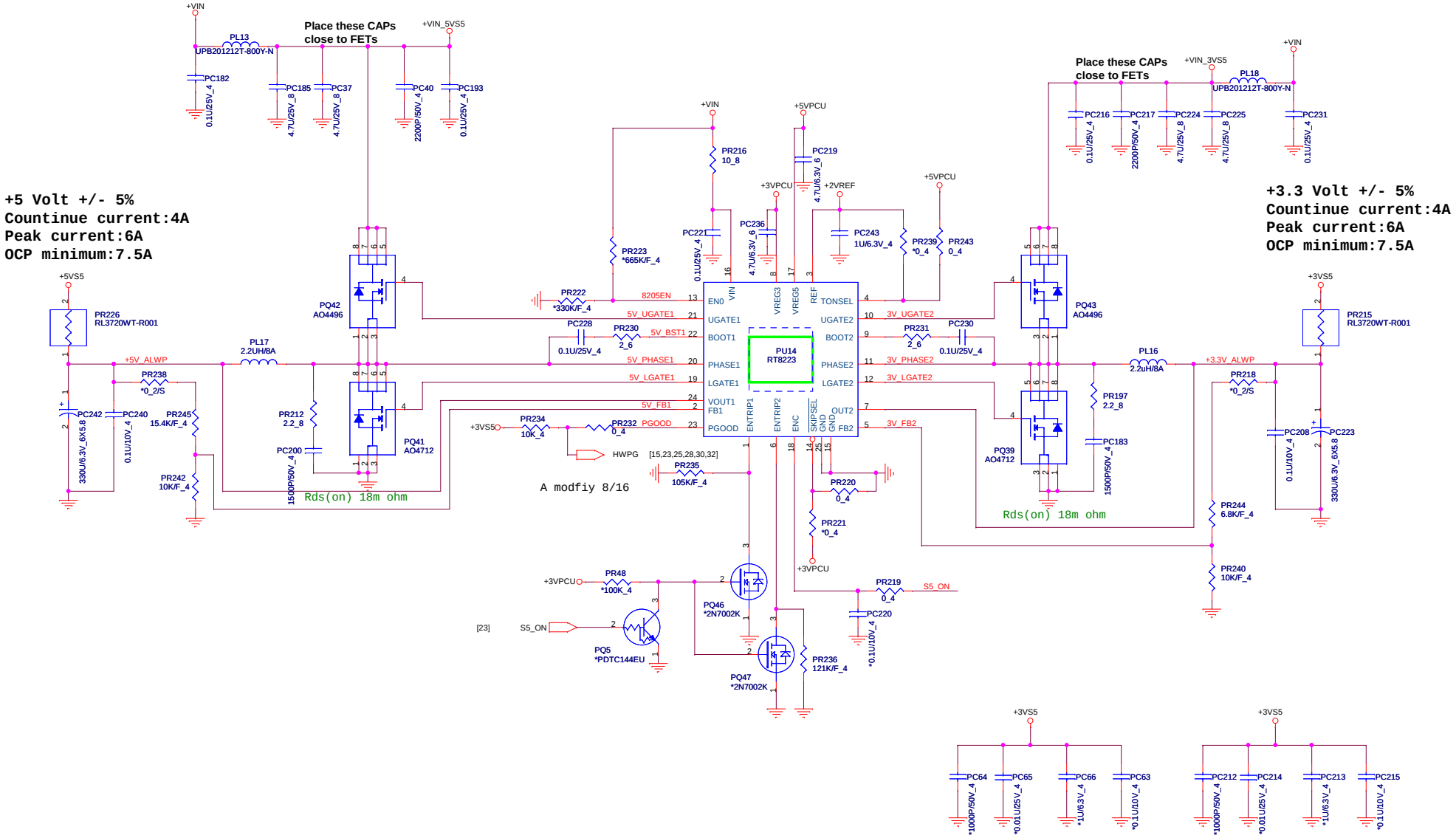
MX25L3205DM2I-12G: AKE39FP0Z00
EN25F32-100HIP: AKE39FN0Q00

Socket: DG008000031

PROJECT : SWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC (IT8502N)	1A

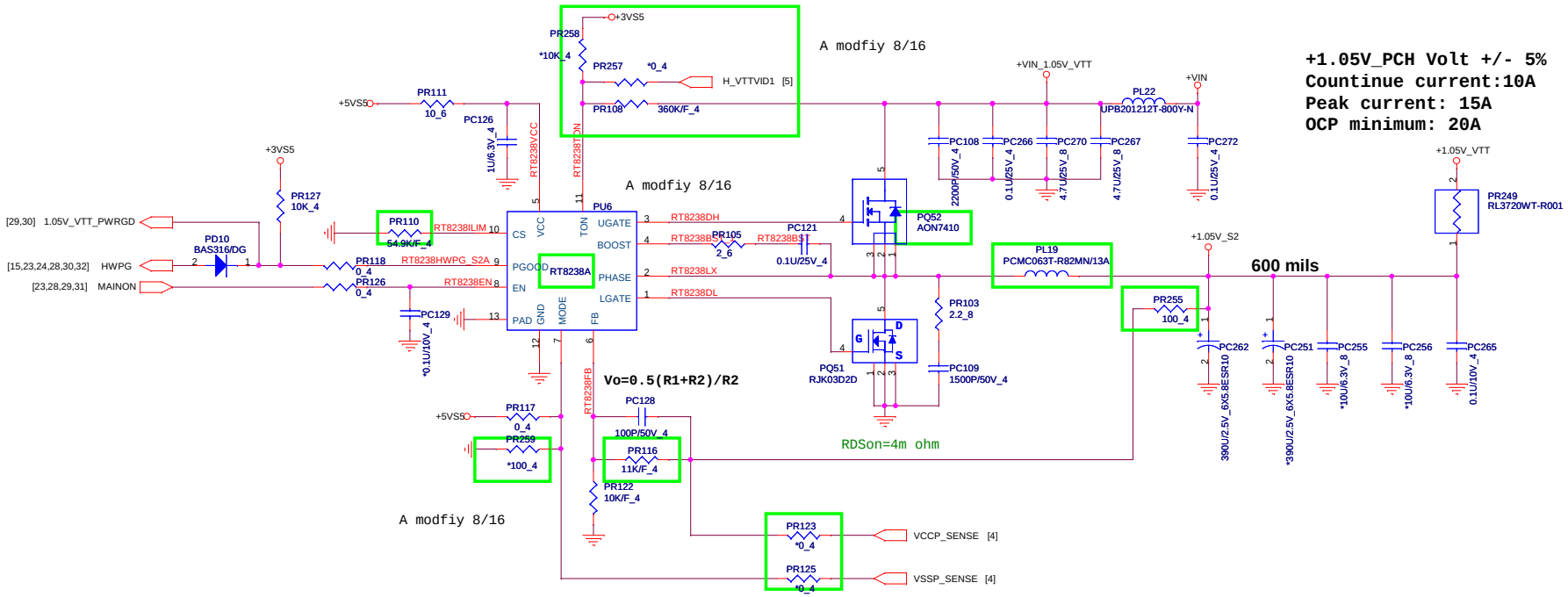
Date: Thursday, October 28, 2010 Sheet 23 of 32



PROJECT : SWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+5V/+3V (RT8206B)	1A

Date: Thursday, October 28, 2010 Sheet 24 of 32


+1.05V_PCH Volt +/- 5%
Countinue current:10A
Peak current: 15A
OCP minimum: 20A
A modfiy 8/16
A modfiy 8/16
A modfiy 8/16
PU6
RT8238A
PQ52 AON7410
PQ51 RJK03D2D
PL22 UPB201212T-800Y-N
PL19 PCMC063T-R82MN/13A
PR249 RL3720WT-R001
600 mils
Vo=0.5(R1+R2)/R2
RDSon=4m ohm
VCCP_SENSE [4]
VSSP_SENSE [4]
+1.8V +/- 5%
Countinue current:1.2A
Peak current:2A
PU15 G9661
VO=(0.8(R1+R2)/R2)
R2<120Kohm

1.Alert trace routing
between data and clock trace
2.Refer to ground
3.Keep out 20 mils

A modfiy 9/21

A modfiy 9/24

B~4350

PUT COLSE
TO VCORE
Phase 1
Inductor

SV 35W CPU
VID1=1.05V
IccMax=54A
R_LL=1.9m ohm
OCP~60A

PUT COLSE
TO VCORE
HOT SPOT

PUT COLSE
TO V_GT
HOT SPOT

PUT COLSE
TO V_GT
Inductor

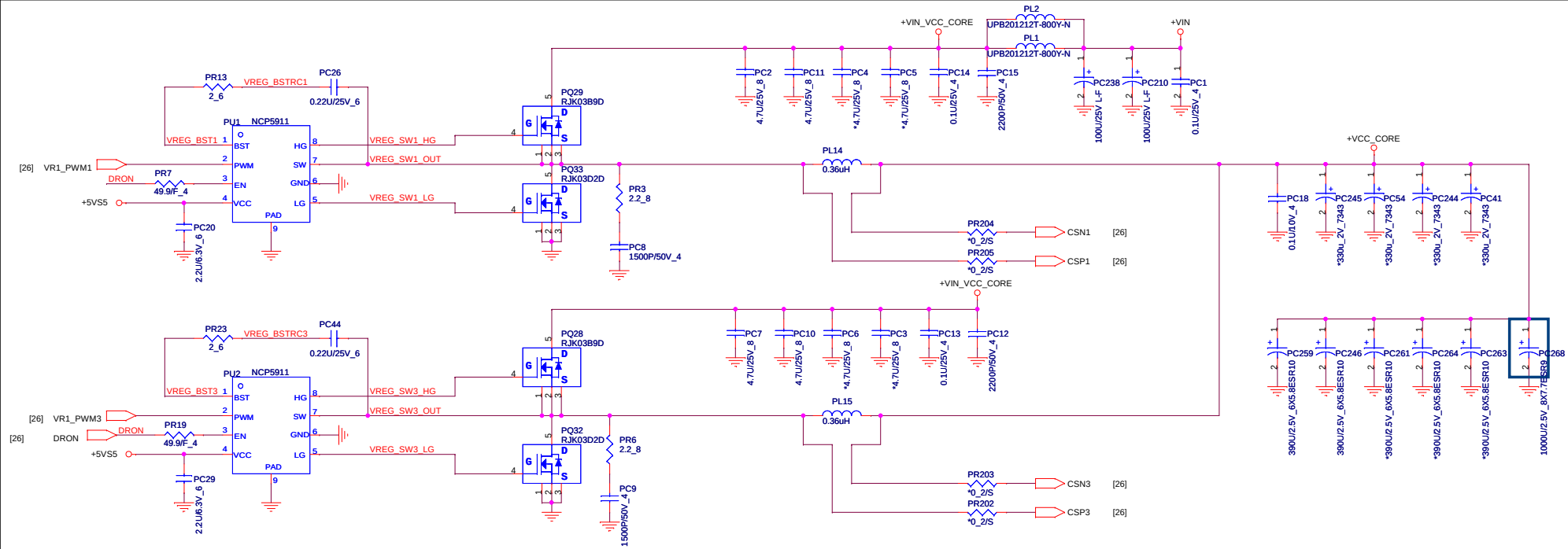
PU5
NCP6131S

ON Semiconductor

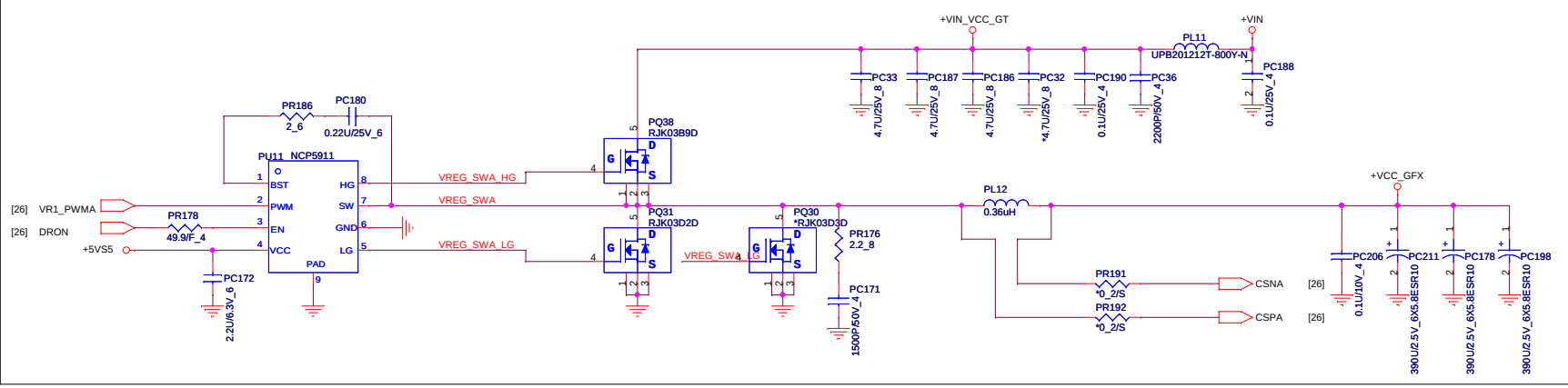
PROJECT : SWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU Core1 (NCP6131S)	1A

Date: Thursday, October 28, 2010 Sheet 26 of 32

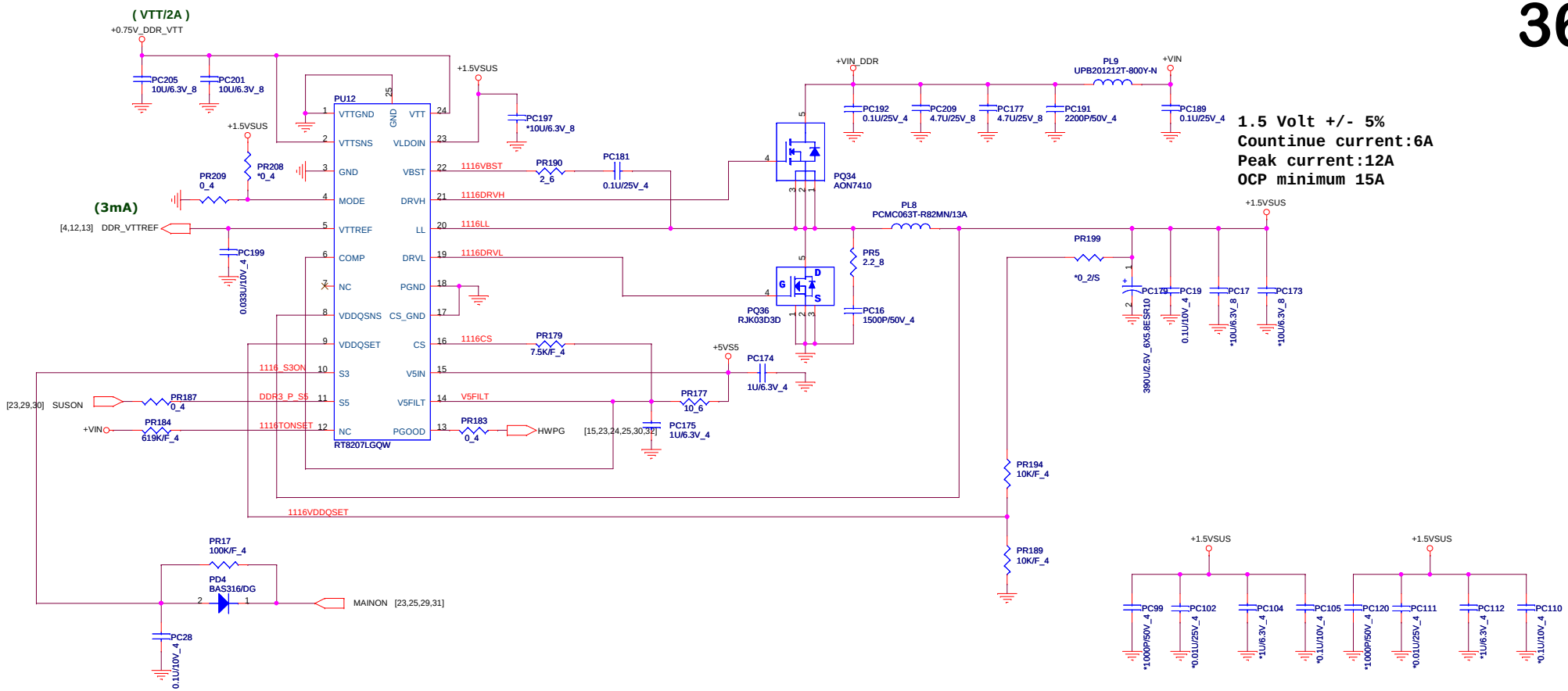


A modfiy 9/16



PROJECT : SWH
Quanta Computer Inc.

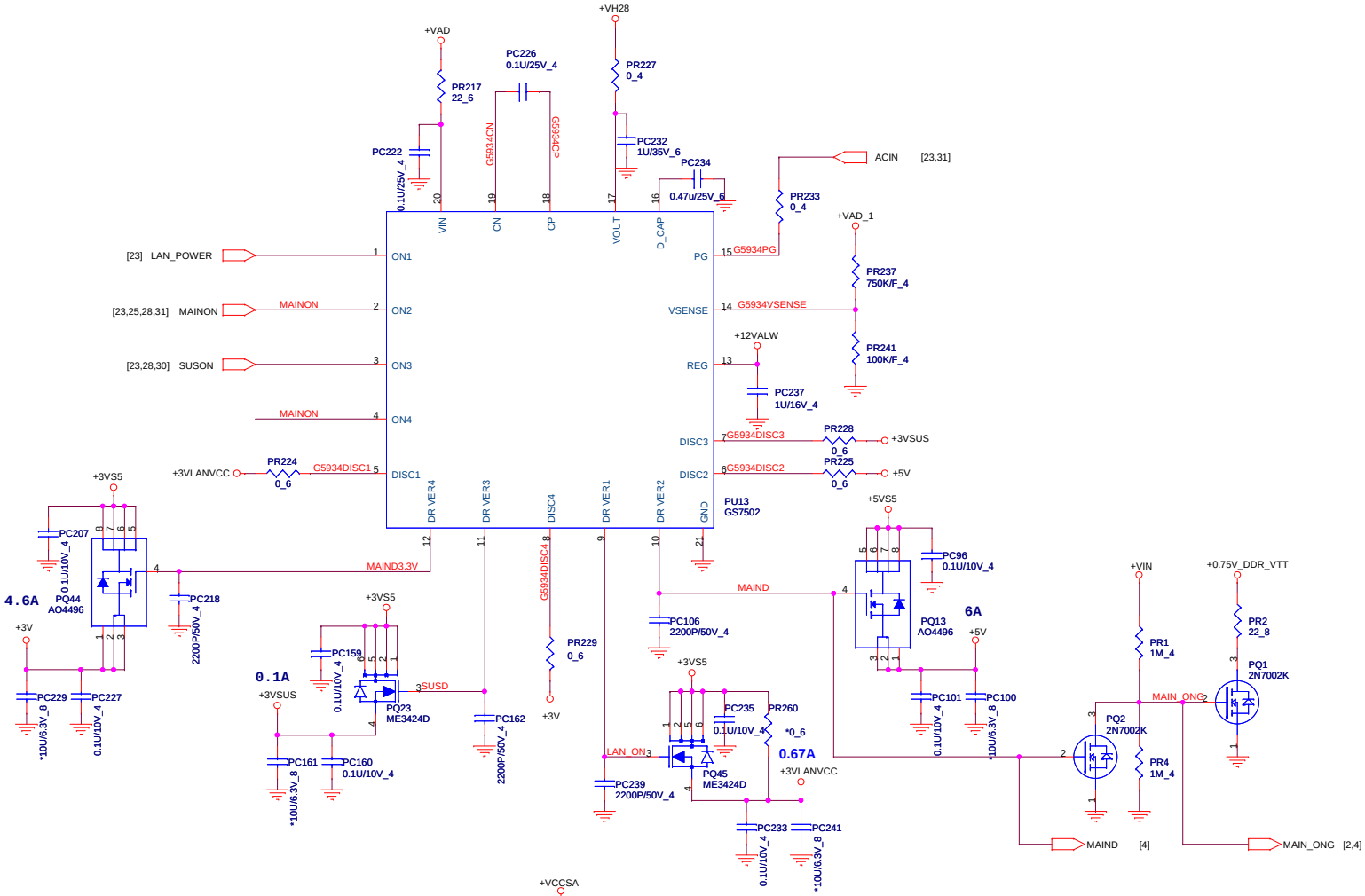
Size	Document Number	Rev
Custom	CPU Core2 (NCP5911)	1A
Date: Thursday, October 28, 2010	Sheet 27 of 32	



PROJECT : SWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (RT8207)	1A

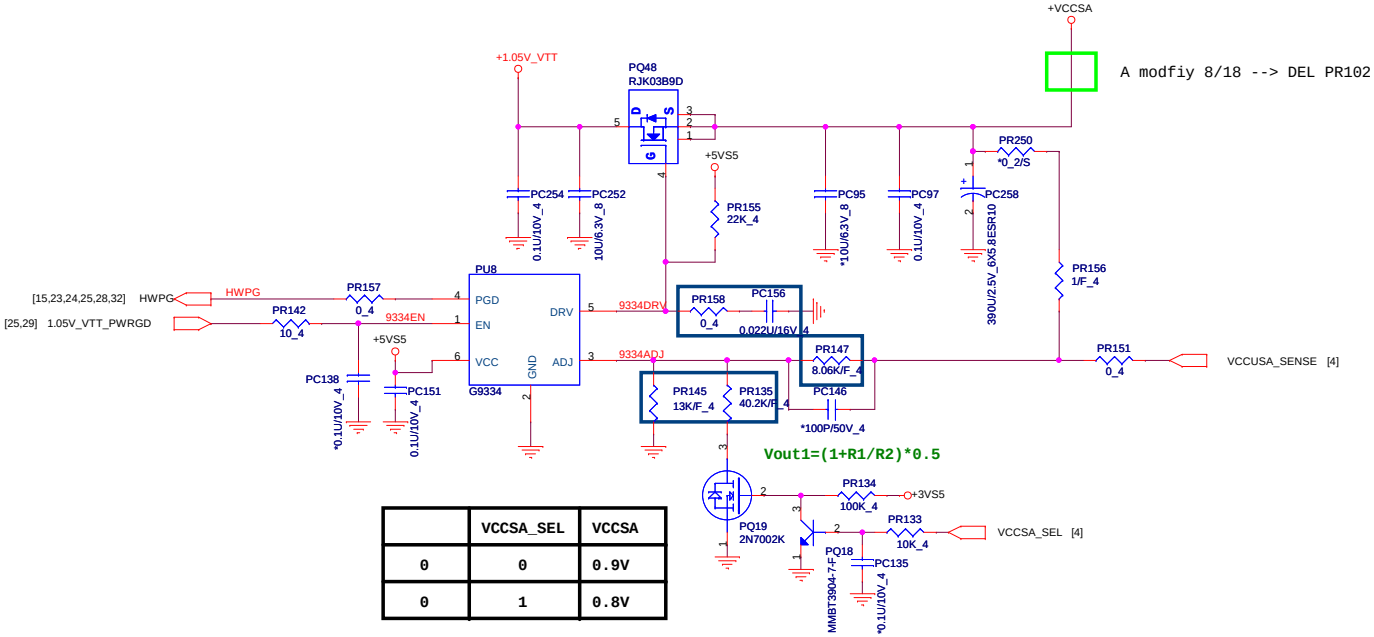
Date: Thursday, October 28, 2010 | Sheet 28 of 32



PROJECT : SWH
Quanta Computer Inc.

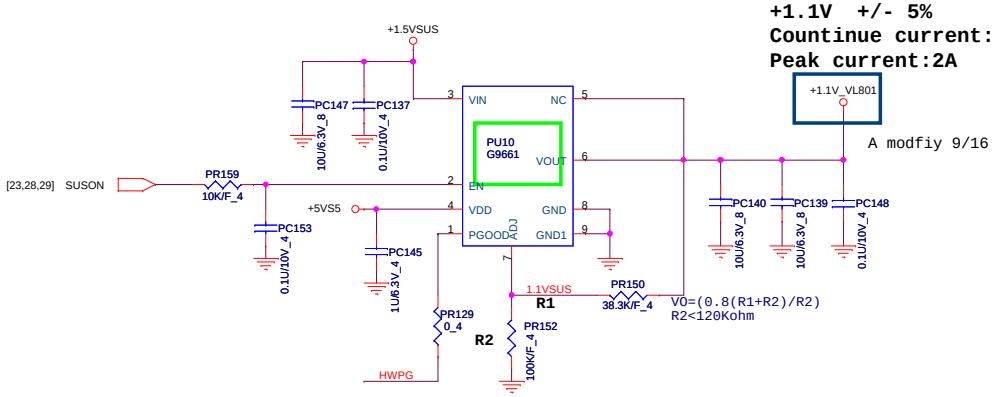
Size	Document Number	Rev
Custom	DISCHARGE/3VS5/5VS5/LAN	1A
Date: Thursday, October 28, 2010	Sheet 29 of 32	

0.85V Volt +/- 5%
Countinue current 3A~6A



	VCCSA_SEL	VCCSA
0	0	0.9V
0	1	0.8V

+1.1V +/- 5%
Countinue current:1.2A
Peak current:2A



PROJECT : SWH
Quanta Computer Inc.

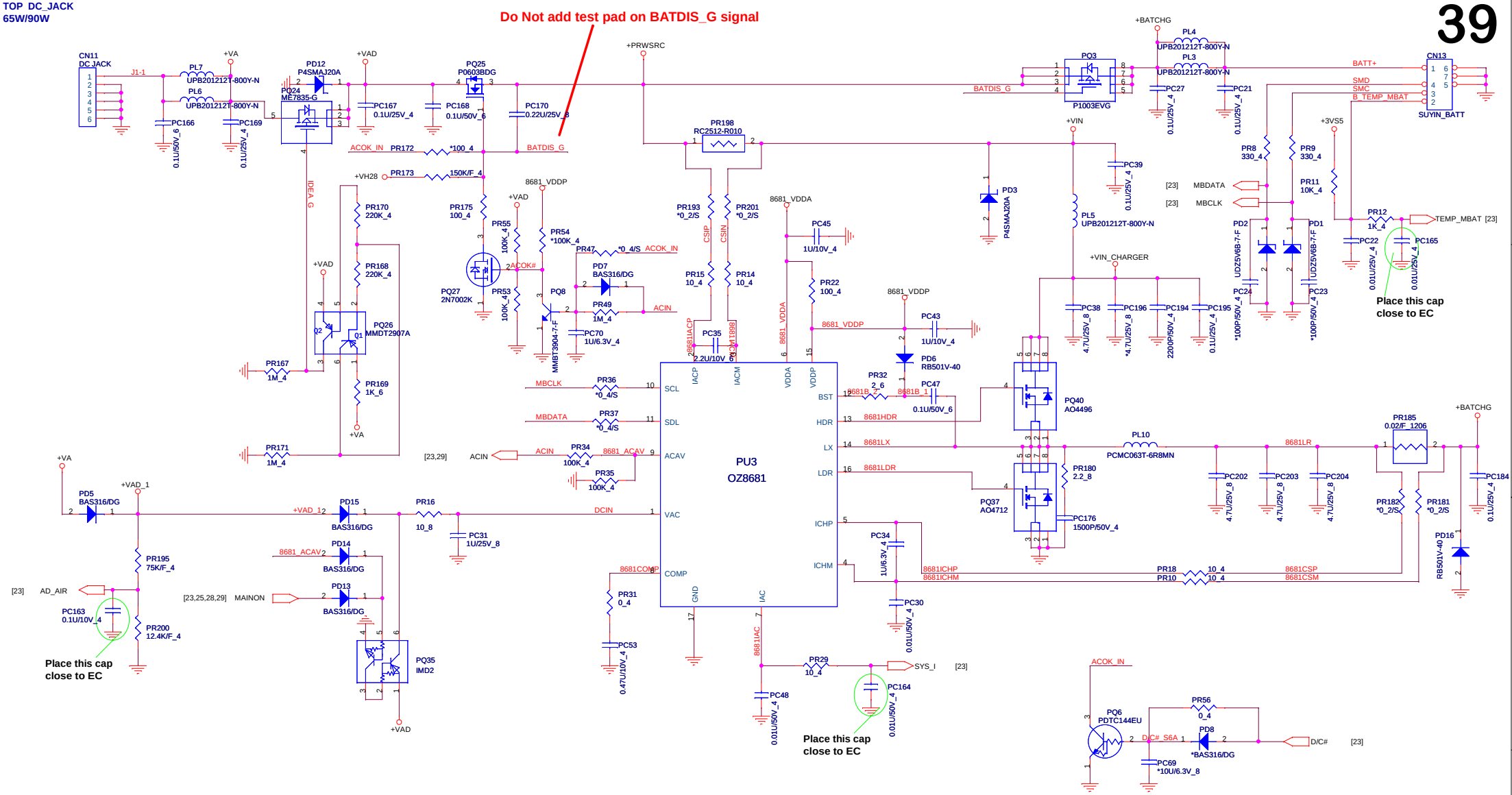
Size	Document Number	Rev
Custom	+1.05V_VTT (VT358)	1A

Date: Thursday, October 28, 2010 Sheet 30 of 32

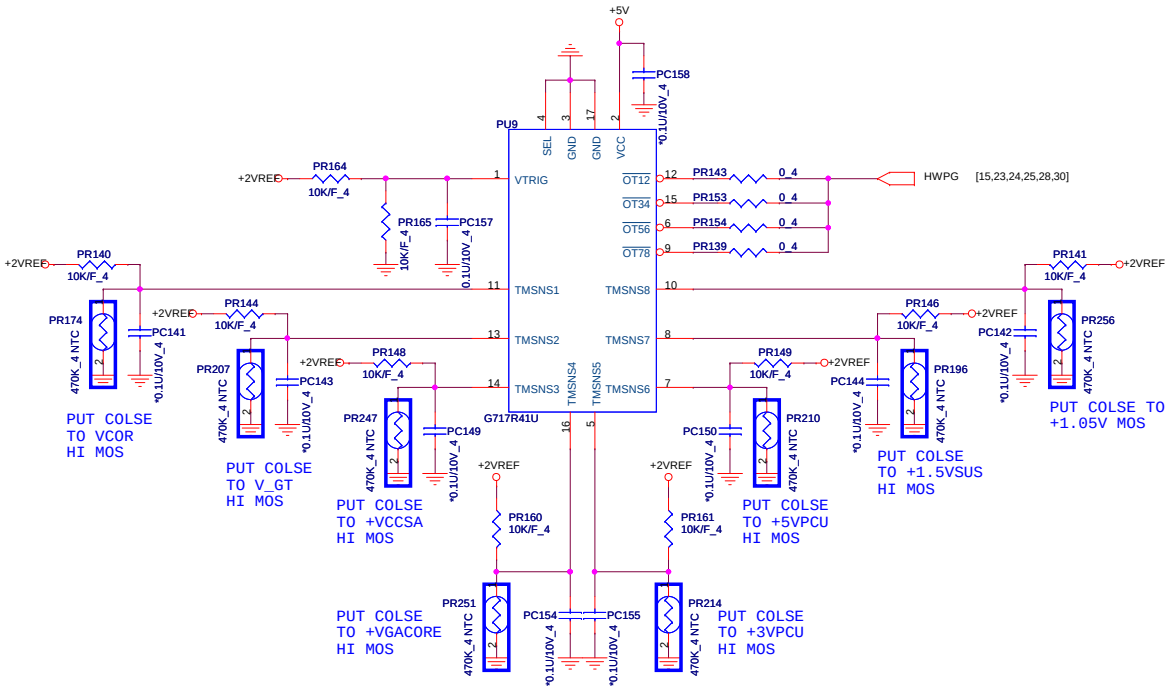
TOP DC_JACK
65W/90W

Do Not add test pad on BATDIS_G signal

39



PROJECT : SWH Quanta Computer Inc.		
Size: Custom	Document Number: Charger (OZ8681)	Rev: 1A
Date: Thursday, October 28, 2010	Sheet 31 of 32	



Vender	Size	P/N
EON	128KB	
	512KB	AKE37ZN0Q01 (EN25F40-100HIP)
Winbond	128KB	AKE35FN0N00 (W25X10BVSNIG)
	512KB	AKE37FN0N01 (W25X40BVSSIG)
Socket		DG008000031

PROJECT : SWH
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Power thermal protection	1A
Date: Thursday, October 28, 2010	Sheet 32 of 32	