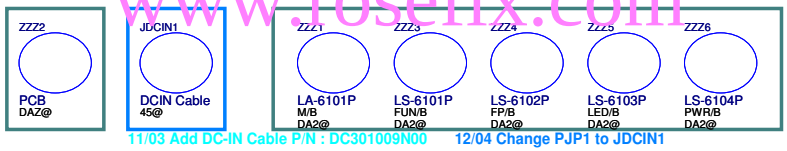

11/03 Add DC-IN Cable P/N : DC301009N00 12/04 Change PJP1 to JDCIN1

11/18 Change PCB P/N from DA60000G300 to DA60000G200

02/26 Change LA-6101P P/N from DA60000G200 to DA60000G210

02/26 Add DAZ P/N and other small board P/N

02/26 Change DAZ P/N from DAZ0D9001001 to DAZ0D900101

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NAU00 LA-6101P Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M

SV M/B

2010-03-09

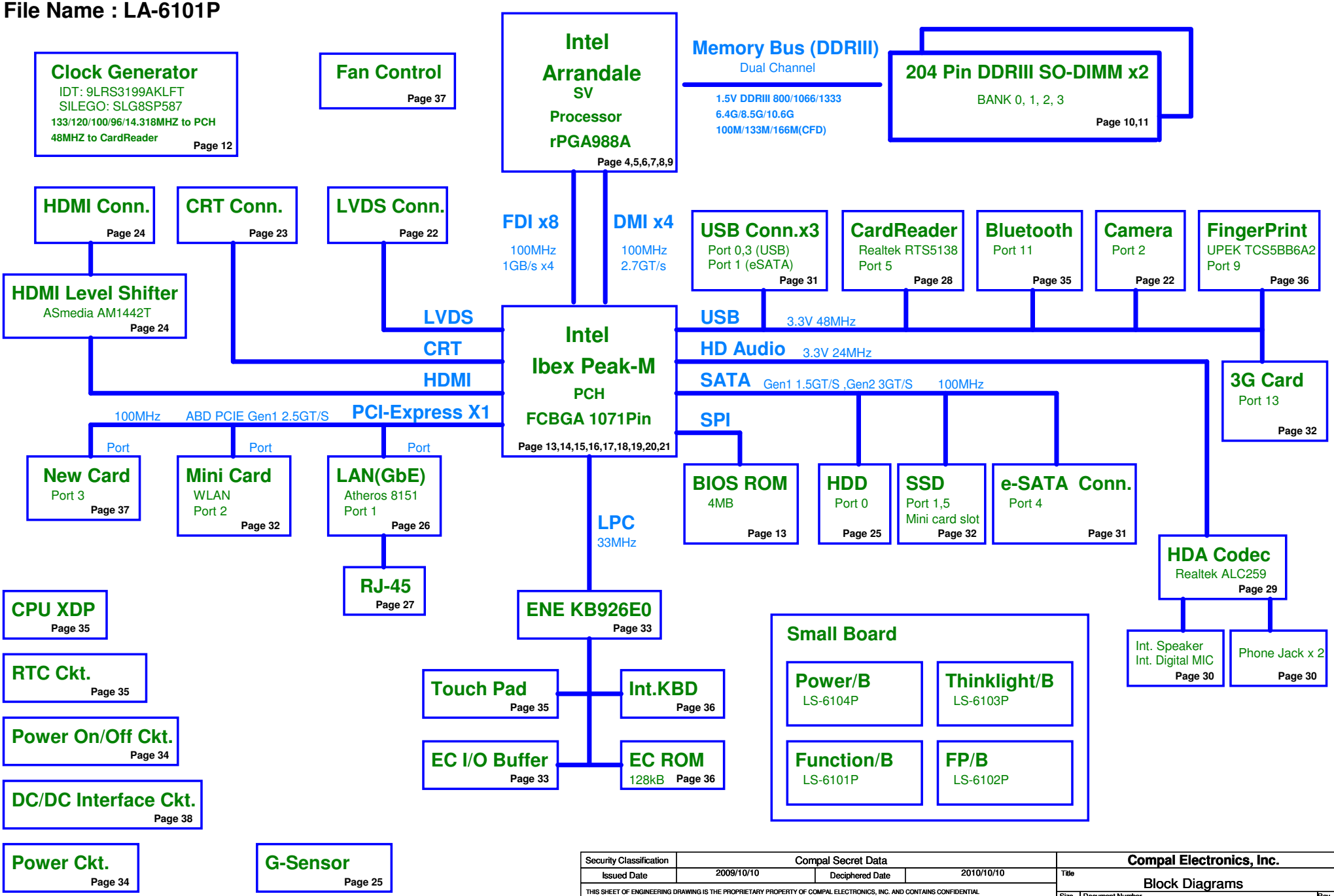
Rev : 1.0

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.		
Title: Cover Page		
Size: Custom	Document Number: NAU00 M/B LA-6101P Schematics	Rev: 1.0
Date: Tuesday, March 09, 2010	Sheet 1 of 48	

Compal Confidential

Model Name : NAU00
File Name : LA-6101P



Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.			
Title	Block Diagrams		
Size B	Document Number NAU00 M/B LA-6101P Schematics		Rev 1.0
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.1VS_VTT	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for PCH	ON	ON	ON
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+5V	5V power rail for PCH	ON	ON	ON
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
ISL90727 ISL90728	0101 1100b 0111 1100b

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
* 0	0.1
1	
2	
3	
4	
5	
6	
7	

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Compal Electronics, Inc.

Title: Notes List

Size	Document Number	Rev
B	NAU00 M/B LA-6101P Schematics	1.0

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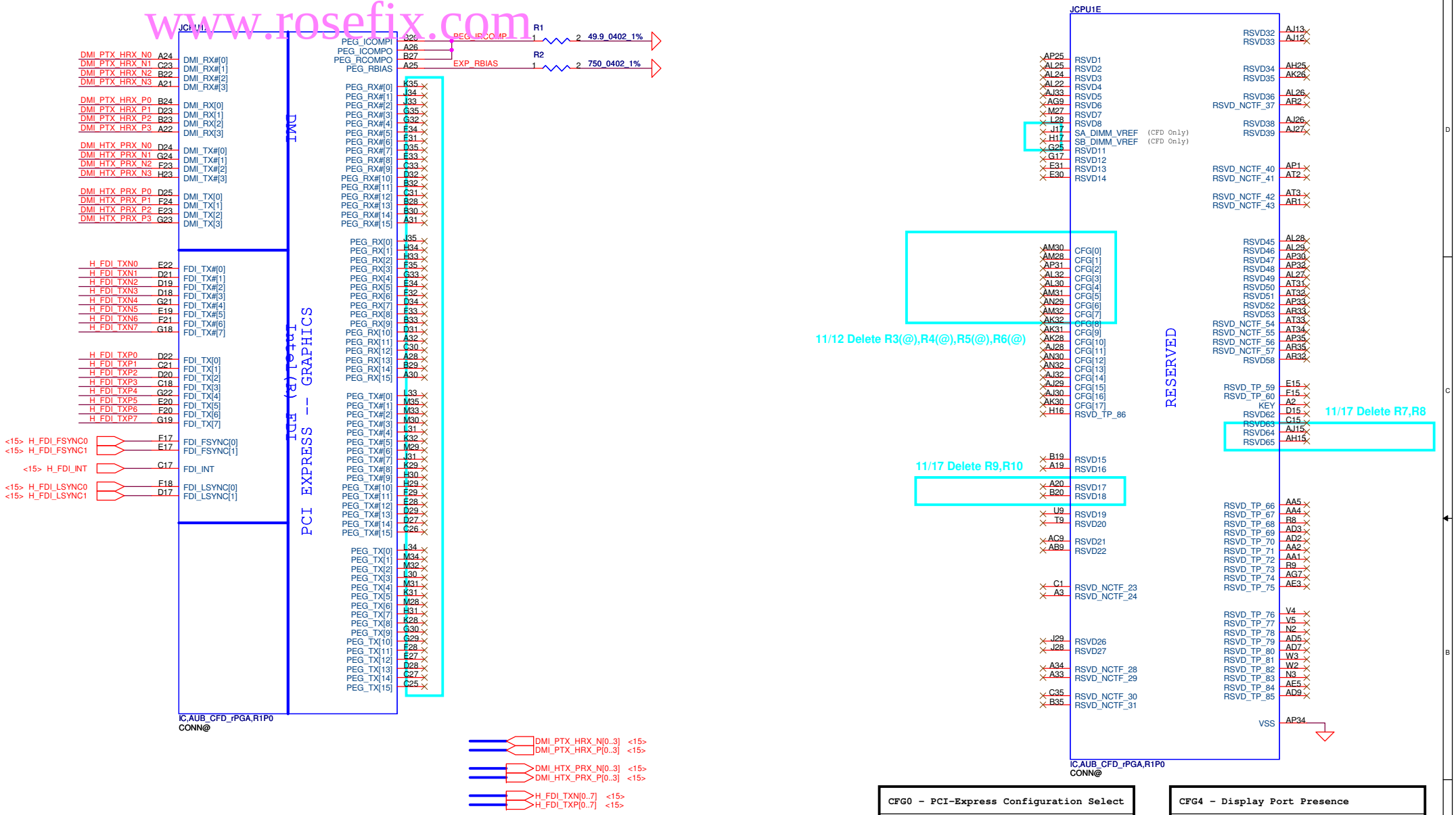

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

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Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PROCESSOR (1/6) DMI,FDI,PEG

Size	Document Number	Rev
B	NAU00 M/B LA-6101P Schematics	1.0

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11/12 Delete R11,R12,R15,R16 (Layout Spacing)

Processor CLK

Reference Input Clock	Input Frequency	Associated PLL
BCLK/BCLK#	133MHz	Processor/Memory /Graphic
PEG_CLK/ PEG_CLK#	100MHz	PCI Express/ DMI/FDI
DPLL_REF_SSCLK/ DPLL_REF_SSCLK#	120MHz	Embedded Displayport

10/21 Delete R13,R14, Add T17,T18

10/30 Delete Net : CLK_CPU_PEG_CLK/ CLK_CPU_DP#
Delete R17,R18

11/05 Delete R21(@)

11/25 Change R36 from mount to @ (Follow NIWE2)

ESD Recommend

10/28 Delete R31,R33(@),R38(@),R39
Delete Net : XDP_TDI_R,XDP_TDO_R

10/30 Add R620,R621 (Follow NIWE2)

10/21 Delete R41
Delete Net : H_PWRGD_XDP,H_PWRGD_XDP_R

10/21 Delete Net : XDP_OBS[7:0]

2009/2/4
Delete dampling resistor for power noise and Layout space issue

2009/2/4
#414044 DG
Update Rev1.11

Note: When implement S3 power reduction not to pop,R53,R44 pop U1,R45,R54

11/23 Change R44,R53 from mount to @
Change U1,R45,R54 from @ to mount

11/16 Reserve C530,C531,C532 for avoiding switching noise
11/23 Change C530,C531,C532 from @ to mount

10/21 Delete JP1,R52,R56,R57,R59,C1
Delete Net : H_CPUPWRGD,H_PWRGOOD_R, PBTN_OUT#_XDP,CLK_CPU_XDP,CLK_CPU_XDP#

Leakage Issue

10/22 Change R62 from mount to @
10/30 Change R62 from @ to mount (Follow NCQD0)
11/25 Change R62 from mount to @ (Follow NIWE2)

12/04 Change Q37 from SB000008J00 to SB000009610 (Layout Spacing)

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PROCESSOR (2/6) CLK,JTAG

Size	Document Number	Rev
B	NAU00 M/B LA-6101P Schematics	1.0

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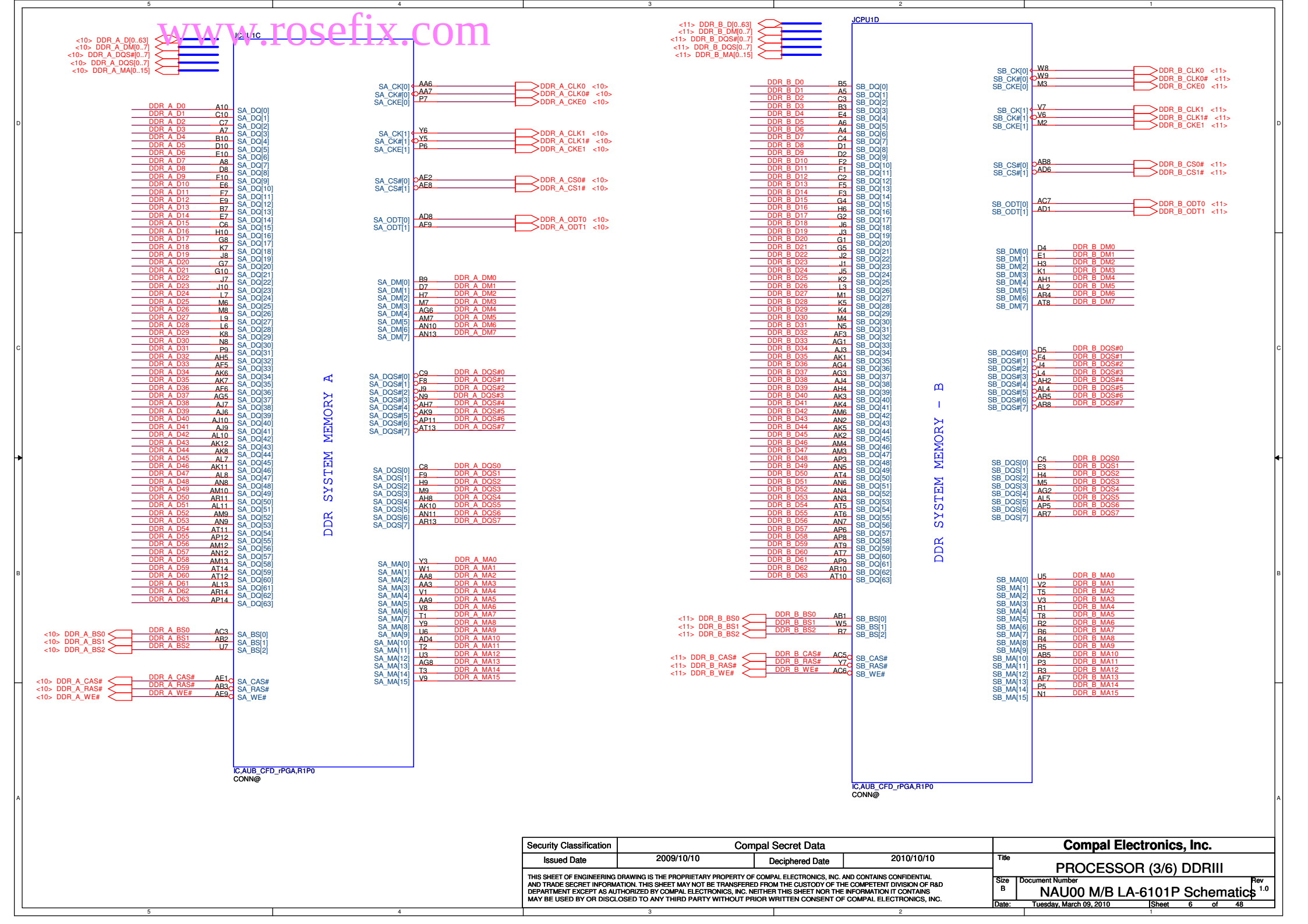

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PROCESSOR (3/6) DDRIII

Size	Document Number	Rev
B	NAU00 M/B LA-6101P Schematics	1.0

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WW15 MOW
Peak 21A
Continuous 18A

48A

+CPU_CORE

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

SENSE LINES

+1.1VS_VTT

11/25 Change C18,C19,C20 from SGA00002380 (6mohm) to SGA00002680 (9mohm)
11/25 Change C19 from mount to @
11/30 Change C20 from SGA00002680 (9mohm) to SGA00002U00 (6mohm)
11/09 Change R64,R66 from mount to @ (PWR Recommend)
11/09 Change R65,R67 from @ to mount (PWR Recommend)

(Place these capacitors between inductor and socket on Bottom)

(Place these capacitors under CPU socket, top layer)

(Place these capacitors on CPU cavity, Bottom Layer)

(Place these capacitors on CPU cavity, Bottom Layer)

CSC (Current Sense Configuration)
11/09 H_VID[6:0] => 0100100

11/17 Reserve C534,C535 for avoiding switching noise
11/17 Change C534,C535 from @ to mount

Please place C534,C535 close to PU701

VTT_SELECT = Low, 1.1V
VTT_SELECT = High, 1.05V

VTT Rail

Auburndale +1.1VS_VTT=1.05V
Clarksfield +1.1VS_VTT=1.1V

11/09 Change C42~C47 from SGA00002U00 to SGA00001Q80 (PWR Recommend)
11/11 Correct C42~C47 footprint

4 x 330uF(6m ohm@100kHz) SGA00001Q80

TOP side (under inductor)

11/25 Change R86 from mount to @ (Follow NIWE2)

Note:CRB has the VTT_SENSE connected through a "no-stuff" 0- series resistor and VSS_SENSE_VTT floating.Connect VSS_SENSE_VTT to GND or can be left floating.

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X330uF	6m ohm/4	2X330uF
MLCC 0805 X5R	16X22uF	3m ohm/12	
	16X10uF	3m ohm/16	

IC,AUB_CFD_rPGA,R1P0
CONN@

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PROCESSOR (4/6) PWR,Bypass

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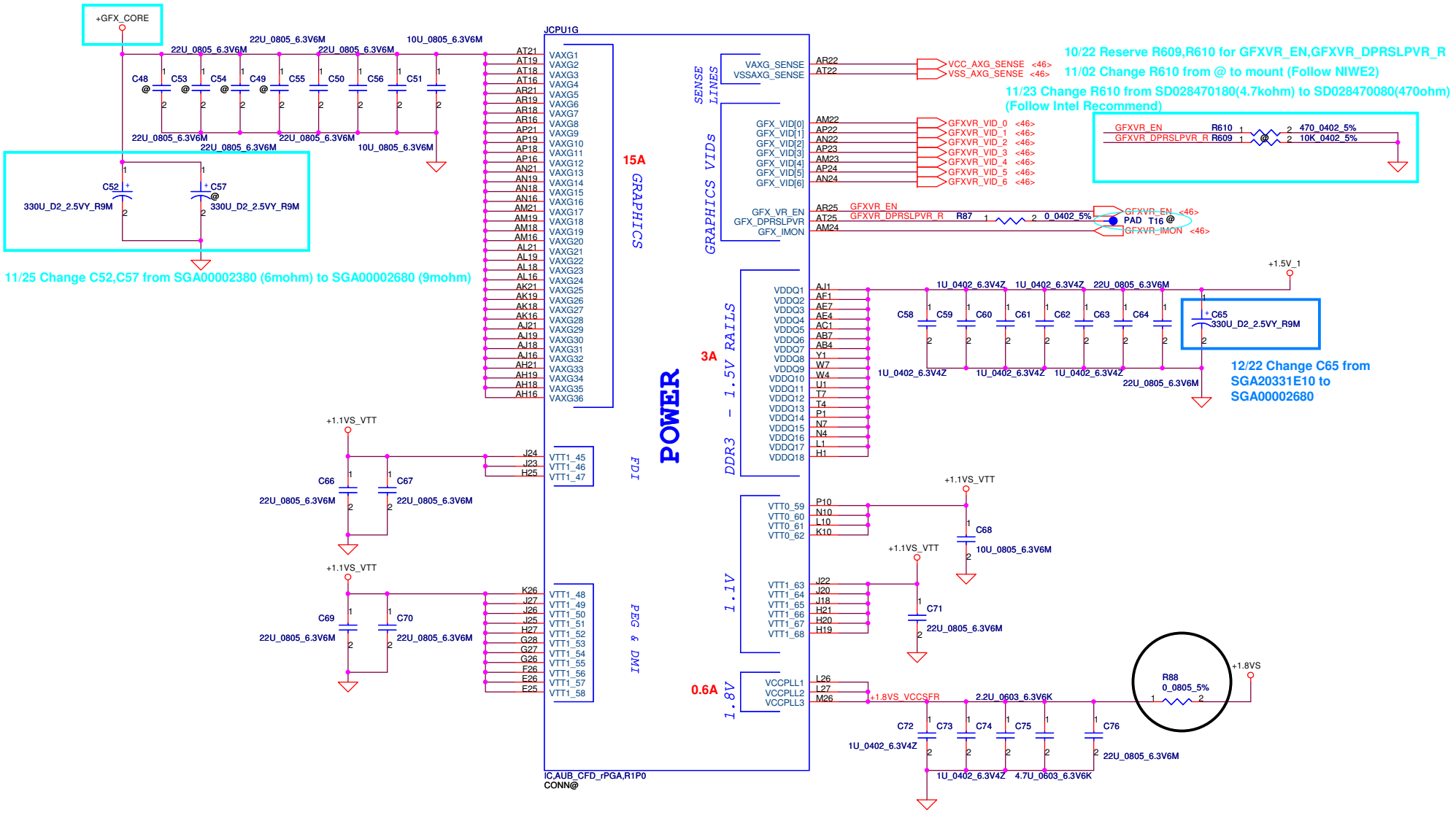

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PROCESSOR (5/6) PWR

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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JCPU1H

VSS

IC,AUB_CFD_rPGA,R1P0
CONN@

JCPU1I

VSS

IC,AUB_CFD_rPGA,R1P0
CONN@

NCTF

11/17 Delete T2,T3,T4,T5

Screw cap. Please place C520~C529 close to H1,H10,H2,H20,H3,H4,H6,H7,H8,H9

11/17 Change the power of C520,C528 from +3VS to B+
12/15 Change C520(@),C528(@) from SE070104Z80 to SE042104K80

11/10 Add C520~C529(@) (ESD Recommend)
11/13 Change C522 power from +3VS to +3VALW
11/17 Delete C521(@),C523(@)

12/15 Add C536~C540 (EMI Recommend)
12/15 Change C539,C540 from SE070104Z80 to SE042104K80

12/15 Add C541~C543 (EMI Recommend)

01/15 Add C544~C549 (EMI Recommend)
01/16 Add C550 (EMI Recommend)

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PROCESSOR (6/6) VSS

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M1 Circuit

+1.5V

R91 1K_0402_1%

+V_DDR3_DIMM_REF

R89 1K_0402_1%

<6> DDR_A_DQS[0..7]

<6> DDR_A_D[0..63]

<6> DDR_A_DM[0..7]

<6> DDR_A_DQS[0..7]

<6> DDR_A_MA[0..15]

2009/04/13
For Arrandale ,it should be use M1 Circuit
For Clarksfield ,it should be use M3 Circuit
DG V1.52

M1 Circuit

+V_DDR3_DIMM_REF

R90 0_0402_5%

+1.5V

C77 0.1U_0402_16V4Z

C78 2.2U_0603_6.3V4Z

11/10 Change C78 from SE103225Z80 to SE049225Z80

R92 @ 0_0402_5%

R93 @ 1K_0402_1%

<5> SM_DRAMRST#

Q9 BSH111_SOT23-3

DIMM_DRAMRST#

10/21 Change R93 from @ to mount

R94 100K_0402_1%

11/05 Change R94 from @ to mount (Follow NIWE2)

RST_GATE

<18> RST_GATE

C502 0.1U_0402_16V4Z

10/22 Add C502 at RST_GATE
(Intel 425302_Calpella_S3PowerReduction_WhitePaper_Rev1.0)
11/09 Change C502 from 0.047uF to 0.1uF

11/23 Change R92 from mount to @
Change Q9 from @ to mount

JDIMM1

		VREF_DQA	1	VREF_DQ	VSS1	2	
			3	VSS2	DQ4	4	DDR_A_D4
DDR_A_D0		DDR_A_D1	5	DQ0	DQ5	6	DDR_A_D5
			7	DQ1	VSS3	8	
		DDR_A_DM0	9	VSS4	DQS#0	10	DDR_A_DQS#0
			11	DM0	DQS0	12	DDR_A_DQS0
			13	VSS5	VSS6	14	
		DDR_A_D2	15	DQ2	DQ6	16	DDR_A_D6
		DDR_A_D3	17	DQ3	DQ7	18	DDR_A_D7
			19	VSS7	VSS8	20	
		DDR_A_D8	21	DQ8	DQ12	22	DDR_A_D12
		DDR_A_D9	23	DQ9	DQ13	24	DDR_A_D13
			25	VSS9	VSS10	26	
		DDR_A_DQS#1	27	DQS#1	DM1	28	DDR_A_DM1
		DDR_A_DQS1	29	DQS1	RESET#	30	DIMM_DRAMRST#
			31	VSS11	VSS12	32	
		DDR_A_D10	33	DQ10	DQ14	34	DDR_A_D14
		DDR_A_D11	35	DQ11	DQ15	36	DDR_A_D15
			37	VSS13	VSS14	38	
		DDR_A_D16	39	DQ16	DQ20	40	DDR_A_D20
		DDR_A_D17	41	DQ17	DQ21	42	DDR_A_D21
			43	VSS15	VSS16	44	
		DDR_A_DQS#2	45	DQS#2	DM2	46	DDR_A_DM2
		DDR_A_DQS2	47	DQS2	VSS17	48	
			49	VSS18	DQ22	50	DDR_A_D22
		DDR_A_D18	51	DQ18	DQ23	52	DDR_A_D23
		DDR_A_D19	53	DQ19	VSS19	54	
			55	VSS20	DQ28	56	DDR_A_D28
		DDR_A_D24	57	DQ24	DQ29	58	DDR_A_D29
		DDR_A_D25	59	DQ25	VSS21	60	
			61	VSS22	DQS#3	62	DDR_A_DQS#3
		DDR_A_DM3	63	DM3	DQS3	64	DDR_A_DQS3
			65	VSS23	VSS24	66	
		DDR_A_D26	67	DQ26	DQ30	68	DDR_A_D30
		DDR_A_D27	69	DQ27	DQ31	70	DDR_A_D31
			71	VSS25	VSS26	72	
<6> DDR_A_CKE0		DDR_A_CKE0	73	CKE0	CKE1	74	DDR_A_CKE1
			75	VDD1	VDD2	76	
			77	NC1	A15	78	DDR_A_MA15
<6> DDR_A_BS2		DDR_A_BS2	79	BA2	A14	80	DDR_A_MA14
			81	VDD3	VDD4	82	
		DDR_A_MA12	83	A12/BC#	A11	84	DDR_A_MA11
		DDR_A_MA9	85	A9	A7	86	DDR_A_MA7
			87	VDD5	VDD6	88	
		DDR_A_MA8	89	A8	A6	90	DDR_A_MA6
		DDR_A_MA5	91	A5	A4	92	DDR_A_MA4
			93	VDD7	VDD8	94	
		DDR_A_MA3	95	A3	A2	96	DDR_A_MA2
		DDR_A_MA1	97	A1	A0	98	DDR_A_MA0
			99	VDD9	VDD10	100	
<6> DDR_A_CLK0		DDR_A_CLK0	101	CK0	CK1	102	DDR_A_CLK1
<6> DDR_A_CLK0#		DDR_A_CLK0#	103	CK0#	CK1#	104	DDR_A_CLK1#
			105	VDD11	VDD12	106	
		DDR_A_MA10	107	A10/AP	BA1	108	DDR_A_BS1
<6> DDR_A_BS0		DDR_A_BS0	109	BA0	RAS#	110	DDR_A_RAS#
			111	VDD13	VDD14	112	
<6> DDR_A_WE#		DDR_A_WE#	113	WE#	S0#	114	DDR_A_CS0#
<6> DDR_A_CAS#		DDR_A_CAS#	115	CAS#	ODT0	116	DDR_A_ODT0
			117	VDD15	VDD16	118	
		DDR_A_MA13	119	A13	ODT1	120	DDR_A_ODT1
<6> DDR_A_CS1#		DDR_A_CS1#	121	S1#	NC2	122	
			123	VDD17	VDD18	124	
			125	NCTEST	VREF_CA	126	DDR_VREF_CA_DIMMA
			127	VSS27	VSS28	128	
		DDR_A_D32	129	DQ32	DQ36	130	DDR_A_D36
		DDR_A_D33	131	DQ33	DQ37	132	DDR_A_D37
			133	VSS29	VSS30	134	
		DDR_A_DQS#4	135	DQS#4	DM4	136	DDR_A_DM4
		DDR_A_DQS4	137	DQS4	VSS31	138	
			139	VSS32	DQ38	140	DDR_A_D38
		DDR_A_D34	141	DQ34	DQ39	142	DDR_A_D39
		DDR_A_D35	143	DQ35	VSS33	144	
			145	VSS34	DQ44	146	DDR_A_D44
		DDR_A_D40	147	DQ40	DQ45	148	DDR_A_D45
		DDR_A_D41	149	DQ41	VSS35	150	
			151	VSS36	DQS#5	152	DDR_A_DQS#5
		DDR_A_DM5	153	DM5	DQS5	154	DDR_A_DQS5
			155	VSS37	VSS38	156	
		DDR_A_D42	157	DQ42	DQ46	158	DDR_A_D46
		DDR_A_D43	159	DQ43	DQ47	160	DDR_A_D47
			161	VSS39	VSS40	162	
		DDR_A_D48	163	DQ48	DQ52	164	DDR_A_D52
		DDR_A_D49	165	DQ49	DQ53	166	DDR_A_D53
			167	VSS41	VSS42	168	
		DDR_A_DQS#6	169	DQS#6	DM6	170	DDR_A_DM6
		DDR_A_DQS6	171	DQS6	VSS43	172	
			173	VSS44	DQ54	174	DDR_A_D54
		DDR_A_D50	175	DQ50	DQ55	176	DDR_A_D55
		DDR_A_D51	177	DQ51	VSS45	178	
			179	VSS46	DQ60	180	DDR_A_D60
		DDR_A_D56	181	DQ56	DQ61	182	DDR_A_D61
		DDR_A_D57	183	DQ57	VSS47	184	
			185	VSS48	DQS#7	186	DDR_A_DQS#7
		DDR_A_DM7	187	DM7	DQS7	188	DDR_A_DQS7
			189	VSS49	VSS50	190	
		DDR_A_D58	191	DQ58	DQ62	192	DDR_A_D62
		DDR_A_D59	193	DQ59	DQ63	194	DDR_A_D63
			195	VSS51	VSS52	196	
			197	SA0	EVENT#	198	PM_EXTTS#0_1
			199	VDDSPD	SDA	200	D_CK_SDATA
			201	SA1	SCL	202	D_CK_SCLK
			203	VTT1	VTT2	204	+0.75VS
			205	G1	G2	206	

FOX_AS0A626-U4SN-7F
CONN@

DIMM_DRAMRST# <11>

DDR_A_CKE1 <6>

DDR_A_CLK1 <6>

DDR_A_CLK1# <6>

DDR_A_BS1 <6>

DDR_A_RAS# <6>

DDR_A_CS0# <6>

DDR_A_ODT0 <6>

DDR_A_ODT1 <6>

PM_EXTTS#0_1 <5,11>

D_CK_SDATA <11,12>

D_CK_SCLK <11,12>

+V_DDR3_DIMM_REF

R95 0_0402_5%

C79 2.2U_0603_6.3V4Z

C80 0.1U_0402_16V4Z

R96 10K_0402_5%

+3VS

C92 2.2U_0603_6.3V4Z

C93 0.1U_0402_16V4Z

R97 10K_0402_5%

Copy NTUC0

Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.5V

C81 10U_0805_6.3V6M
C82 10U_0805_6.3V6M
C83 10U_0805_6.3V6M
C84 10U_0805_6.3V6M
C85 10U_0805_6.3V6M
C86 10U_0805_6.3V6M
C87 0.1U_0402_16V4Z
C88 0.1U_0402_16V4Z
C89 0.1U_0402_16V4Z
C90 0.1U_0402_16V4Z
C91 @ 220U_D2_4VM

11/25 Change C91(@) from SGA20331E10 to SGA00000Y80

Layout Note:
Place near JDIMM1.203 & JDIMM1.204

+0.75VS

C94 1U_0603_10V4Z
C95 1U_0603_10V4Z
C96 1U_0603_10V4Z
C97 1U_0603_10V4Z
C98 10U_0805_6.3V6M

DDR3 SO-DIMM A
Standard Type
H = 4.0mm

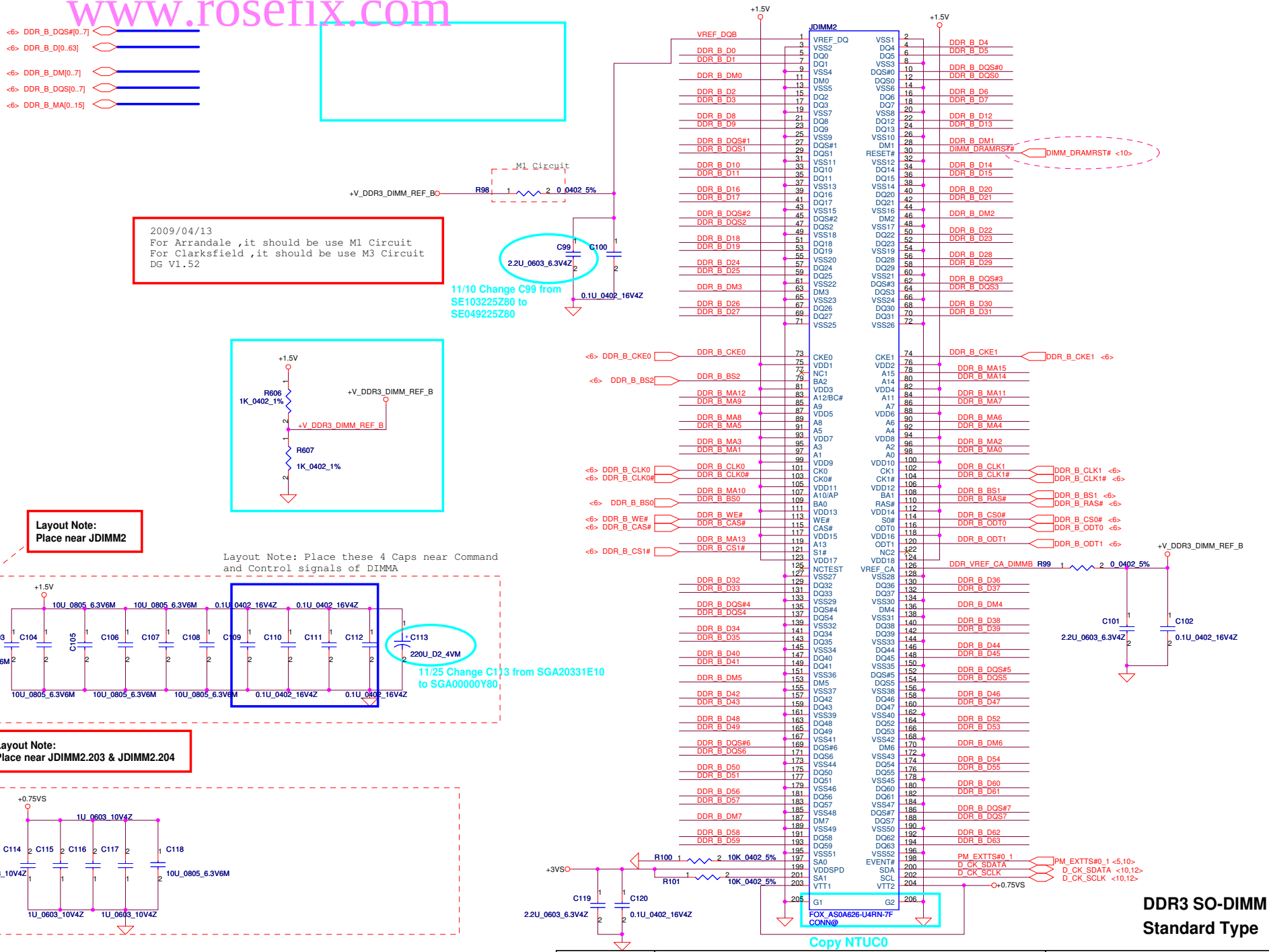
Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

Size	Document Number	Rev
Custom	NAU00 M/B LA-6101P Schematics	1.0

Date: Tuesday, March 09, 2010 Sheet 10 of 48



Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title	DDRIII-SODIMM SLOT2		
Size	Document Number	NAU00 M/B LA-6101P Schematics	Rev 1.0
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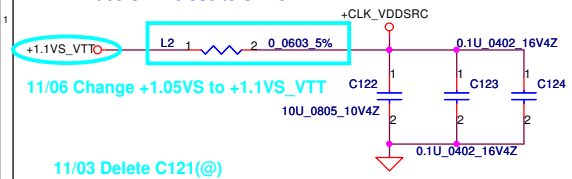
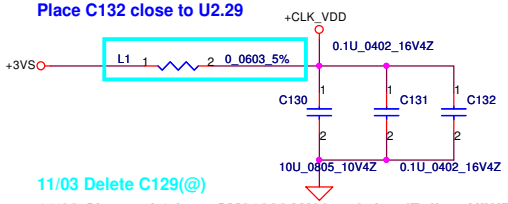
Layout note:
Place C122 close to L2
Place C123 close to U2.15
Place C124 close to U2.18



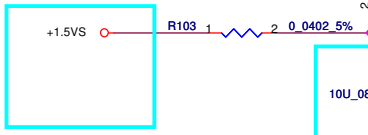
11/06 Change +1.05VS to +1.1VS_VTT
11/03 Delete C121(@)
11/03 Change L2 from SM01000AX00 to 0ohm (Follow NIWE2)

Layout note:
Place C130 close to L1
Place C131 close to U2.5
Place C132 close to U2.29



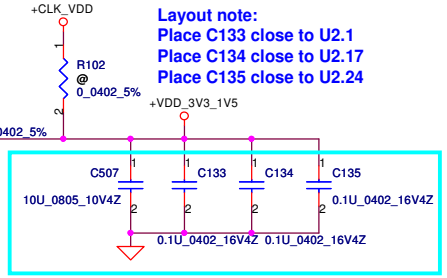
11/03 Delete C129(@)
11/03 Change L1 from SM01000AX00 to 0ohm (Follow NIWE2)

Layout note:
Place C507 close to R103



11/03 Delete L3,C126,C125(@)
10/23 Delete C127, C128, C501 on +CLK_1.5VDD

Layout note:
Place C133 close to U2.1
Place C134 close to U2.17
Place C135 close to U2.24



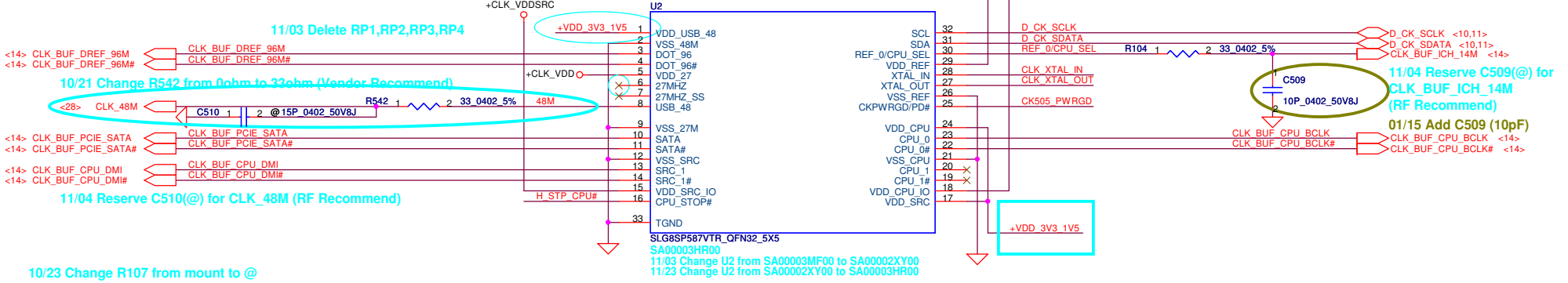
10/23 Add C1000 on +VDD_3V3_1V5
Change C133, C134, C135 from +CLK_VDD to +VDD_3V3_1V5
11/03 Change C507 from @ to mount

Type	R102	R103
Standard	Mount	@
Low Power	@	Mount

10/23 Change U2 Pin1,17,24
Net Name to +VDD_3V3_1V5

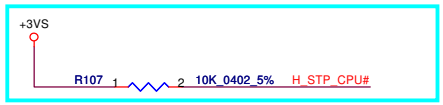
Clock Generator

11/03 Delete RP1,RP2,RP3,RP4

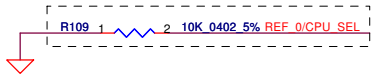


SA00003HR00
11/03 Change U2 from SA00003MF00 to SA00002XY00
11/23 Change U2 from SA00002XY00 to SA00003HR00

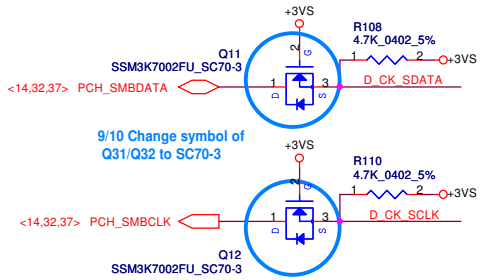
10/23 Change R107 from mount to @
11/03 Change R107 from @ to mount

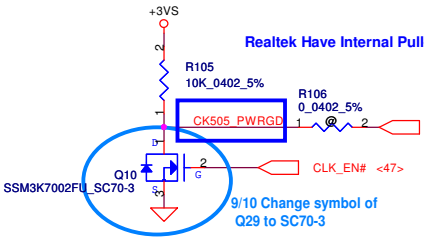


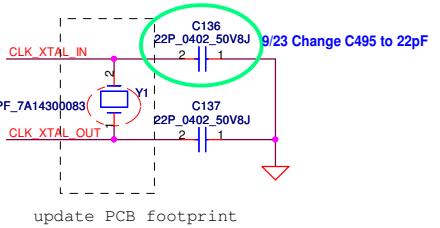
IDT& Realtek Have Internal Pull-Down



PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz







Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: Clock Generator (CK505)

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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RC Delay 13~25mS

close to RAM door

RC Delay 18~25mS

close to RAM door

12/17 Change U3 from SA00003N7B0 to SA00003N7A0
11/30 Change U3 from SA00003N720 to SA00003N7B0

PCH : SA00003N7A0

U3A REV1.0

01/21 Add U34,R652(@)

10/5 Change R223 to 330K ohm

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

HDA for AUDIO

11/04 Reserve C508(@) for BITCLK (RF Recommend)

If GPIO33 pull down, ME will not working.
For factory update ME, pull down resistor pull under door.

11/10 Delete Q13,R120,R121 (Follow NIWE2)

GPIO33 can not pull down
(manufacturing environments)

SATA for HDD

SATA for SSD

2/10 SATA2, SATA3 not support on HM55

SATA for eSATA

SATA for SSD

11/06 Change +1.05VS to +1.1VS_VTT

10/5 Change R287 to 10K ohm

Have internal PD

9/3 Remove R738

10/5 Change R734 to 0 ohm

IBEXPEAK-M_FCBGA107

PCH Pin	RefDes	PCH JTAG Pre-Production ES1	PCH JTAG Pre-Production ES2	PCH JTAG Production * MP
PCH_JTAG_TDO	R138	No Install	200ohm	No Install
	R139	No Install	100ohm	No Install
PCH_JTAG_TMS	R135	200ohm	200ohm	No Install
	R136	100ohm	100ohm	No Install
PCH_JTAG_TDI	R143	200ohm	200ohm	No Install
	R144	100ohm	100ohm	No Install
PCH_JTAG_TCK	R150	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R146	20Kohm	20Kohm	No Install
	R147	10Kohm	10Kohm	No Install

11/05 Change R135,R136,R138,R139,R143,R144,R146,R147 from mount to @ (Follow NIWE2)
11/10 Delete R134(@),R137(@),R142(@),R145(@)

11/06 Change +1.05VS to +1.1VS_VTT

11/09 Delete R148(@) (Follow NIWE2)

enable iTPM: SPI_MOSI High

11/05 Change R150 from 4.7kohm to 51ohm (Follow NIWE2)

11/23 Change R129,R131 from @ to mount
Change R132,R133 from mount to @
(Follow NIWE2)

SPI ROM Footprint 150mil

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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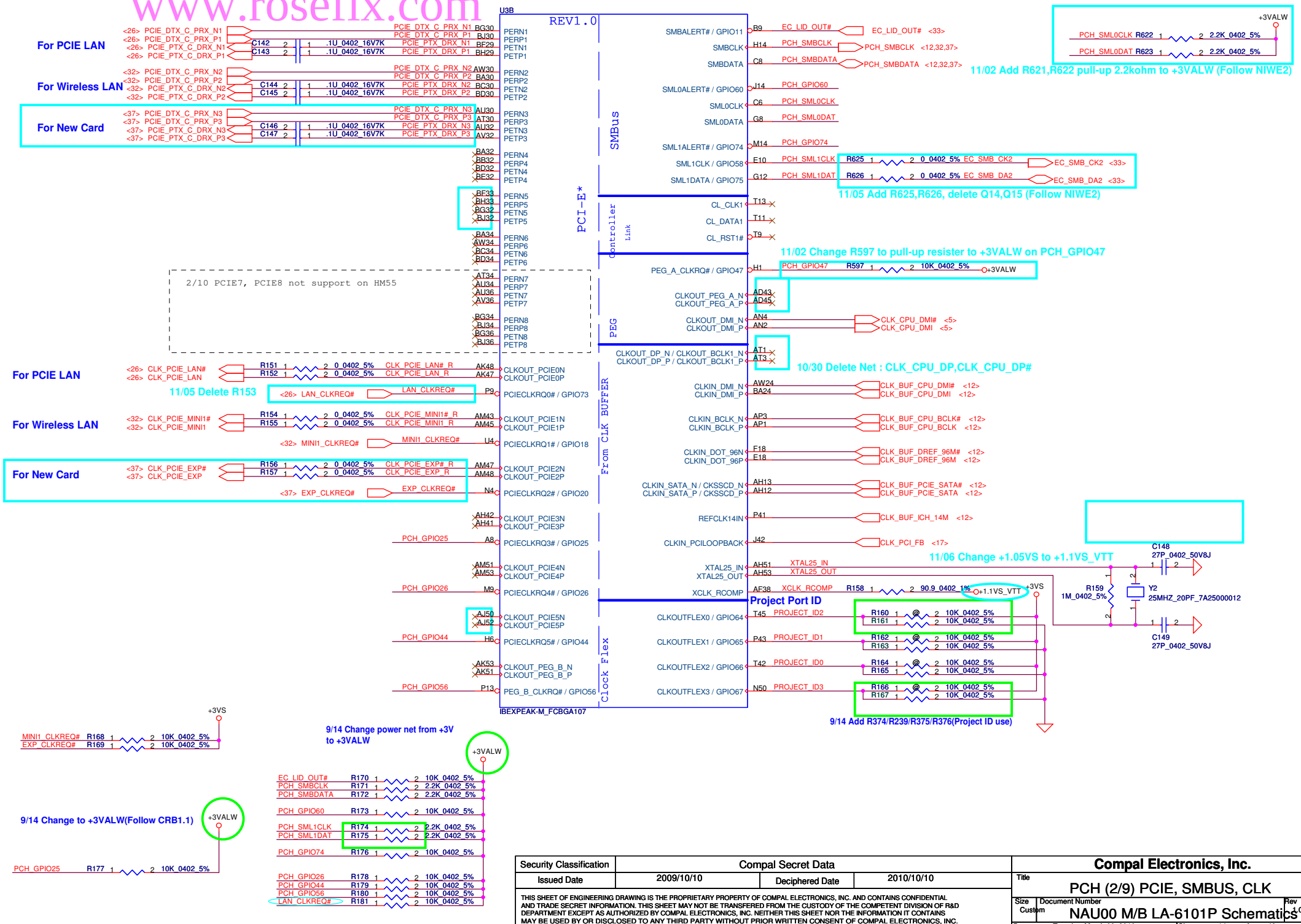


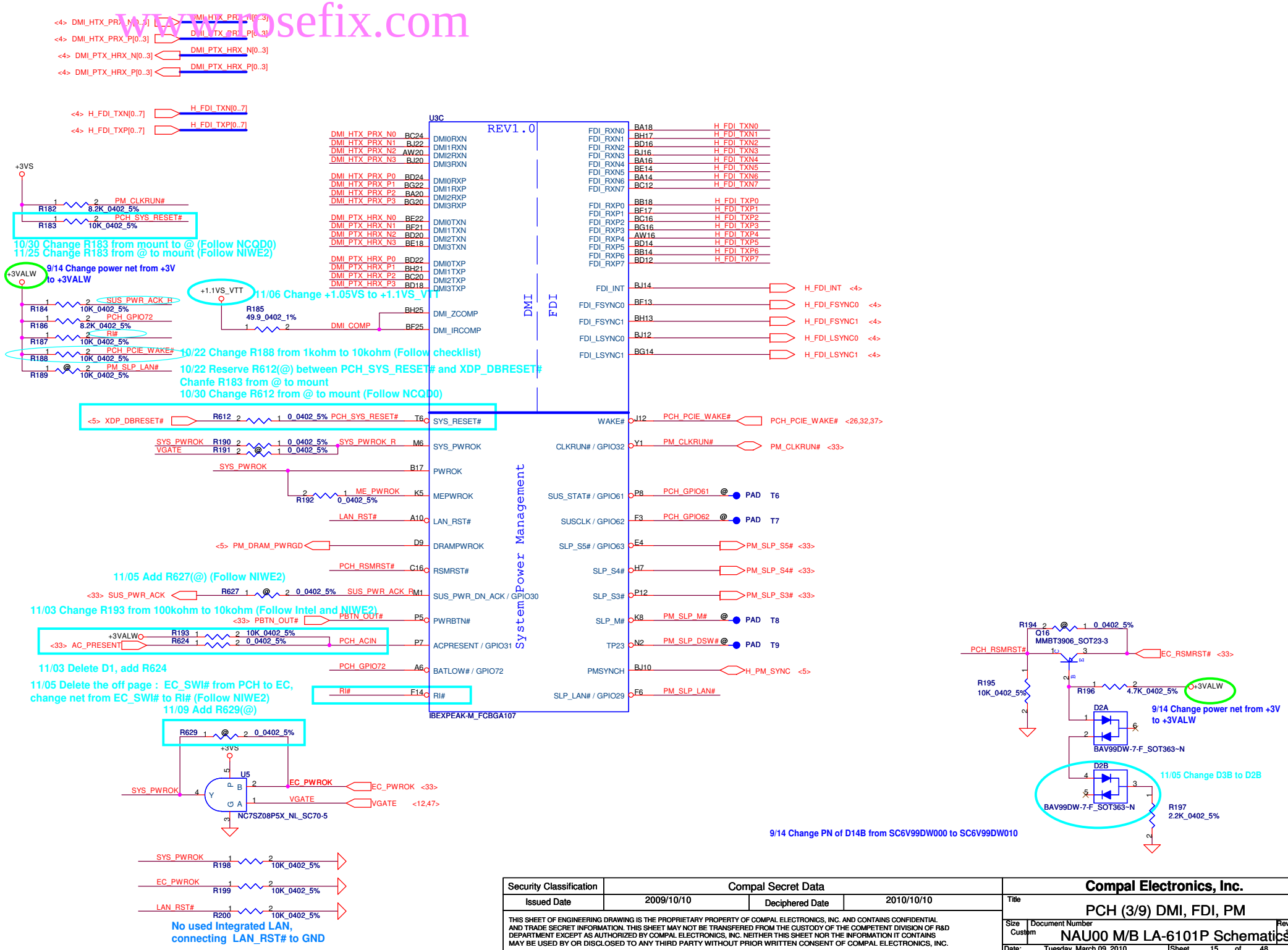
Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

Date: Tuesday, March 09, 2010 | Sheet 14 of 48



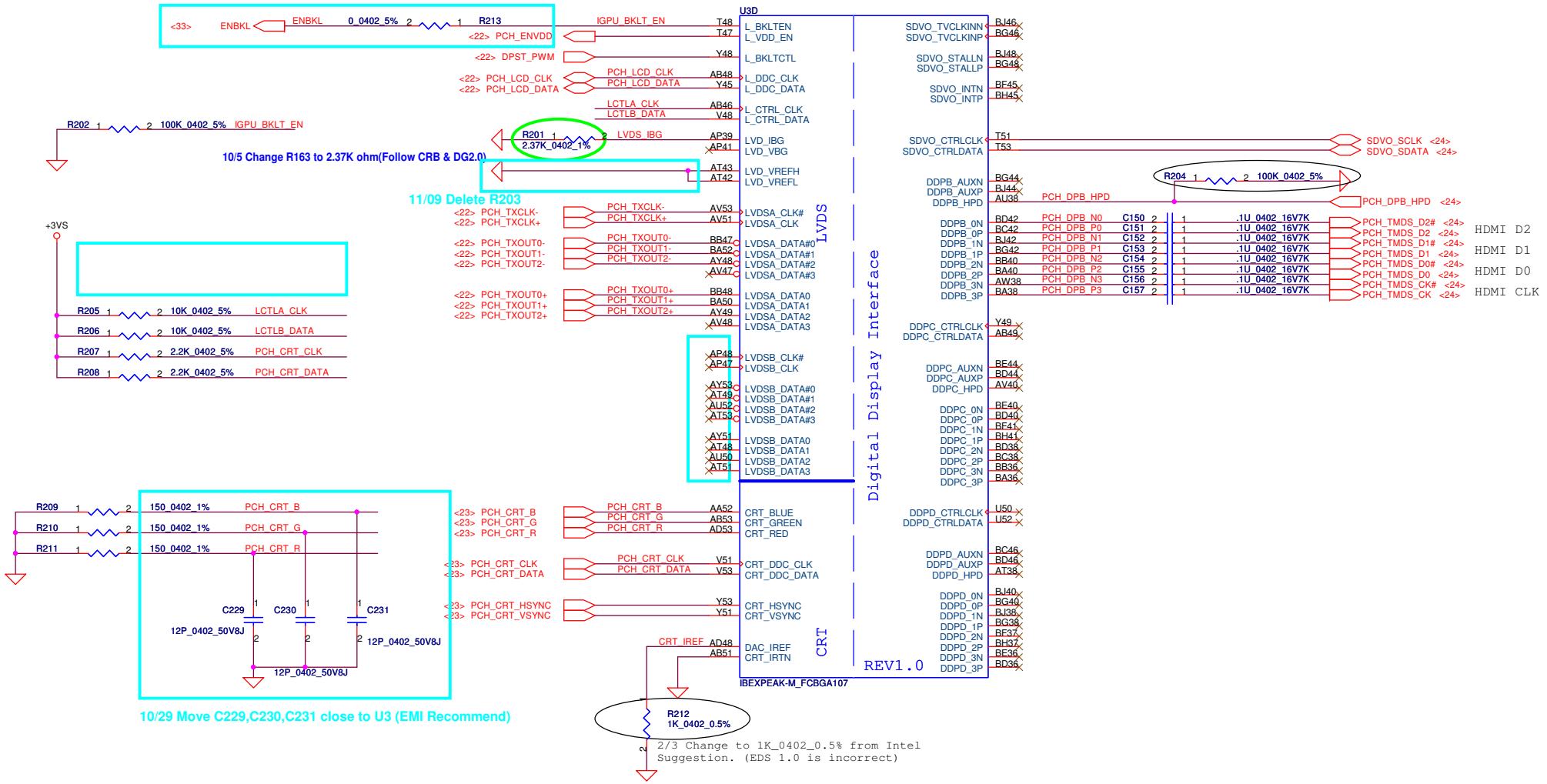
Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PCH (3/9) DMI, FDI, PM

Size	Document Number	Rev
Custom	NAU00 M/B LA-6101P Schematics	1.0

Date: Tuesday, March 09, 2010 Sheet 15 of 48



Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PCH (4/9) LVDS, CRT, DPI

Size	Document Number	Rev
Custom	NAU00 M/B LA-6101P Schematics	1.0

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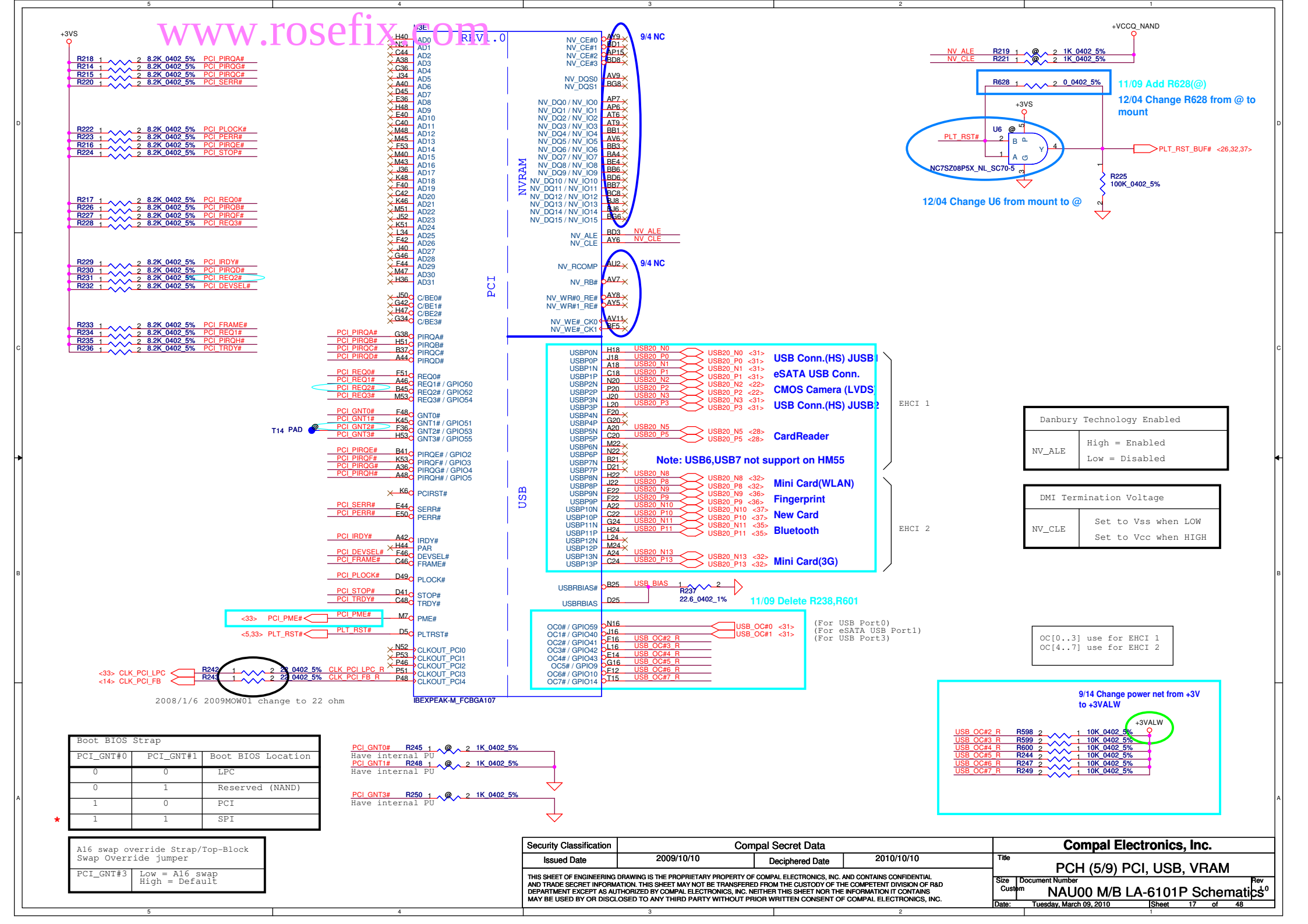


Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

★

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

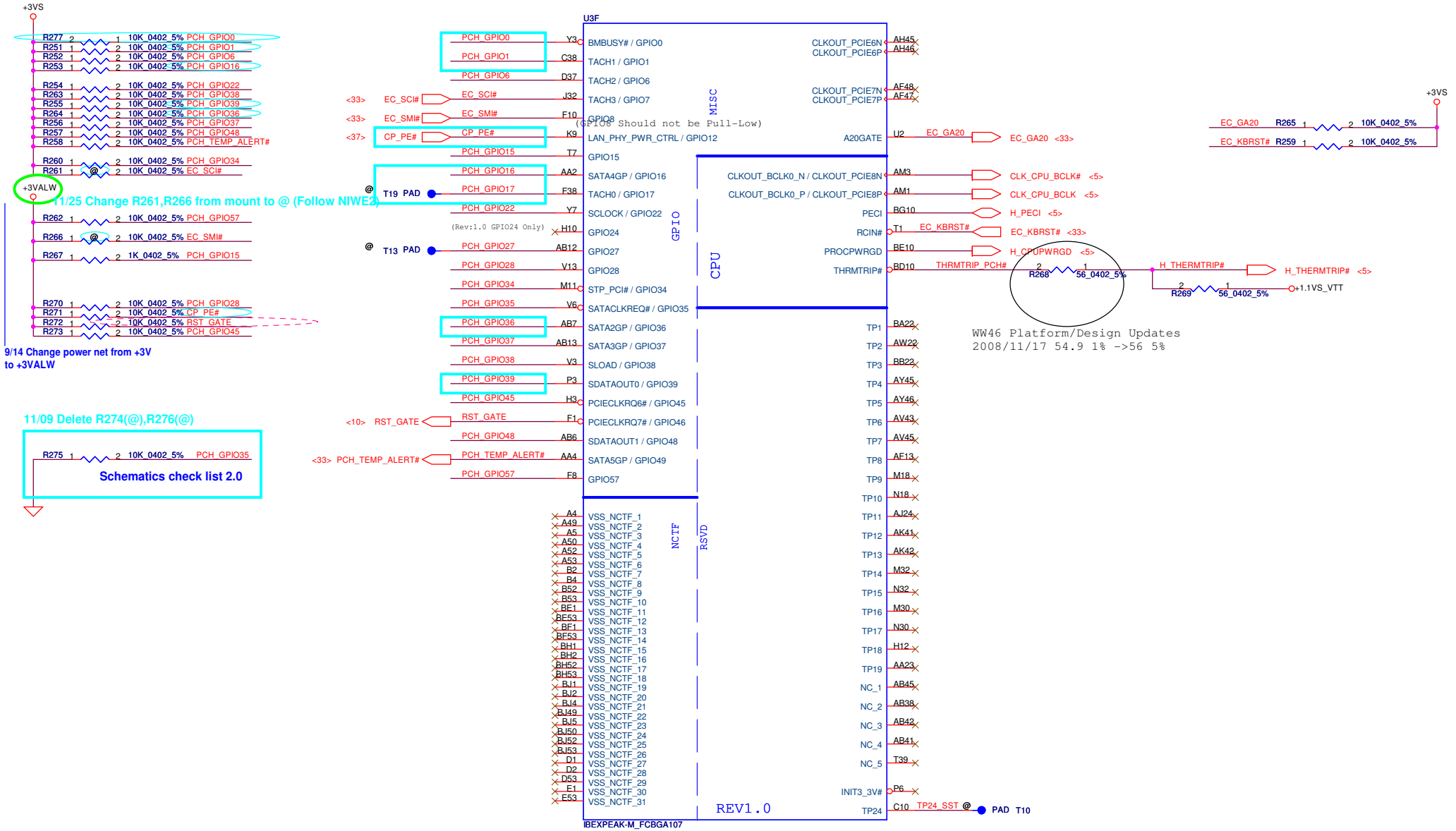
Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, VRAM

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

Date: Tuesday, March 09, 2010 | Sheet 17 of 48



Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size	Document Number	Rev
Custom	NAU00 M/B LA-6101P Schematics	1.0

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CRB 0.9 is 180 ohm @ 100MHz
DG0.8 is 600 ohm FB (Page 290)

11/06 Change +1.05VS to +1.1VS_VTT

Intel suggest follow CRB 8/21

Near AB24 Top Side

All Ibex Peak-M Power rails with netnames +1.1VS and +1.1V rails are actually +1.05VS and +1.05V rails

U3G POWER

VCC CORE 1524mA
CRT 69mA
LVDS 300mA + 59mA + 42mA
HVCMOS 3208mA
DMI 35mA + 61mA
PCI E* 156mA
NAND / SPI 85mA + 6mA
FDI
REV1.0

11/09 Delete L6(@),C166(@)

11/09 Delete L7(@),C176(@)

11/06 Change +1.05VS to +1.1VS_VTT

Near AN20 Top Side

Near AN35

Follow Intel suggestion 8/21

11/09 Delete R278(@)

Near AE50

60mA

01/18 Change L4 (SM010005500) to R649 (SD013100B80)
01/18 Change C162 from 10uF to 22uF
01/19 Add C551(@)

11/09 Change R279 from 0_0805 to 0_0603

Near AP43

L5 0.1UH_MLF1608DR10KT_10%_1608 0.1uH inductor, 200mA

Change R280,R281,R282 from 0805 to 0603 (Layout Request)
11/06 Change +1.05VS to +1.1VS_VTT
11/09 Delete R280(@),R281(@)
11/09 Change R282 from 0_0603 to 0_0402

11/09 Change R283 from 0_0805 to 0_0402

11/06 Delete R284(@)

Near AT16

11/09 Change R285 from 0_0805 to 0_0402

Near AK13

Near AM8

Near AB34

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PCH (7/9) PWR

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POWER REV1.0

U3J

11/09 Delete L8(@),C178(@),C179(@)

11/09 Delete R286(@),C190(@)

11/06 Change +1.05VS to +1.1VS_VTT

Follow Intel suggestion

All Ibex Peak-M Power rails with netnames +1.1VS and +1.1V rails are actually +1.05VS and +1.05V rails

9/14 Change power net from +3V to +3VALW

9/14 Follow CRB1.1 Change to 10 ohm

9/14 Follow CRB1.1 Change to 0.1uF

12/27 Change D4,D5 from SC1H751H010 to SCS00000Z00

Change to 1U for power sequence issue on ICH9

11/09 Delete L11(@),C203(@),C204(@)

11/09 Change R292,R293,R294,R295 from 0_0603 to 0_0402

11/09 Change R593,R594 from 0_0603 to 0_0402

IBEXPEAK-M_FCBGA107

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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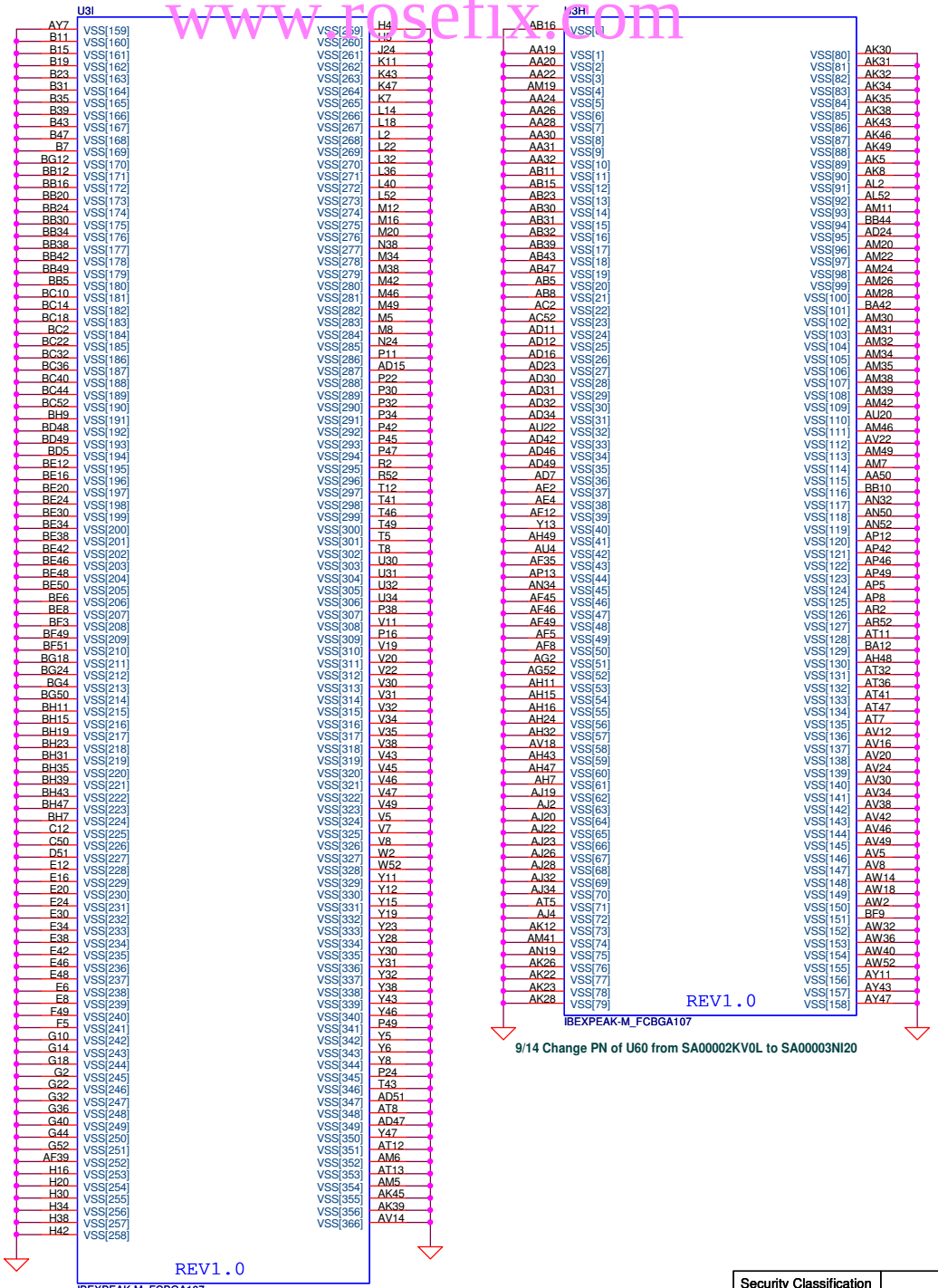

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: PCH (9/9) VSS & PCH XDP Port

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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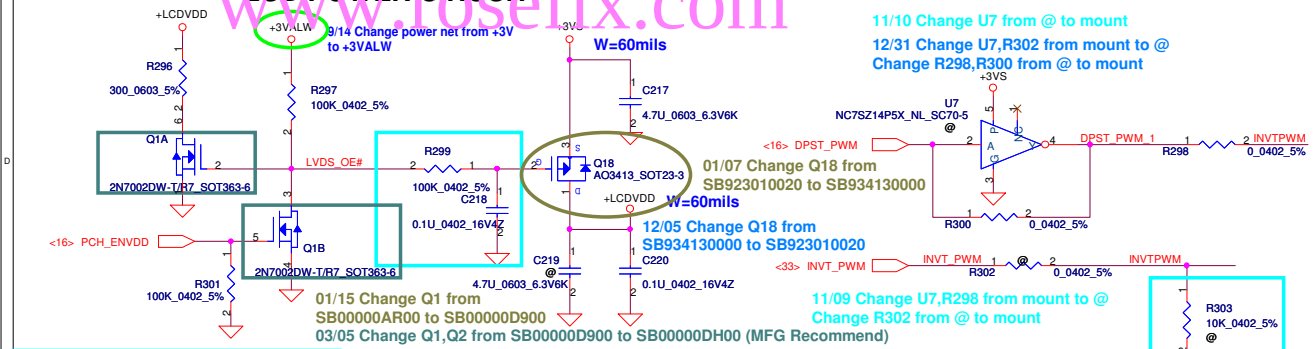
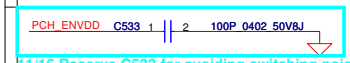
LCD POWER CIRCUIT



11/10 Change U7 from @ to mount
12/31 Change U7,R302 from mount to @
Change R298,R300 from @ to mount

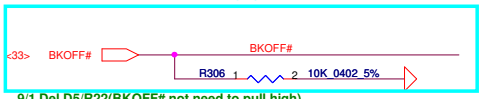
11/09 Change U7,R298 from mount to @
Change R302 from @ to mount



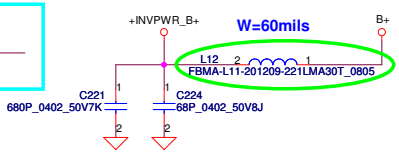
11/16 Reserve C533 for avoiding switching noise
11/23 Change C533 from @ to mount

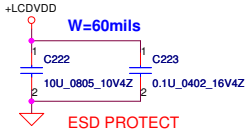
11/09 Change C218 from 0.047uf to 0.1uF
Change R299 from 1kohm to 100kohm
Change C219 from mount to @
(Follow KHLBX)

11/09 Delete R304(@) 11/10 Delete R305

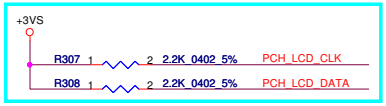


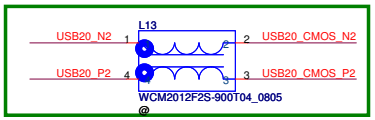
9/1 Del D5/R22(BKOFF# not need to pull high)

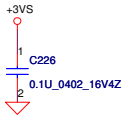


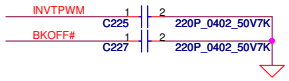


ESD PROTECT
CLOSE TO JLVDS1

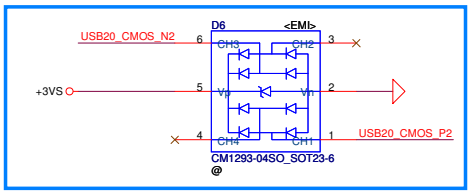


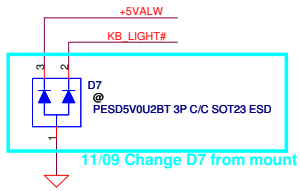






9/14 Add By Vivian(EMI suggest)

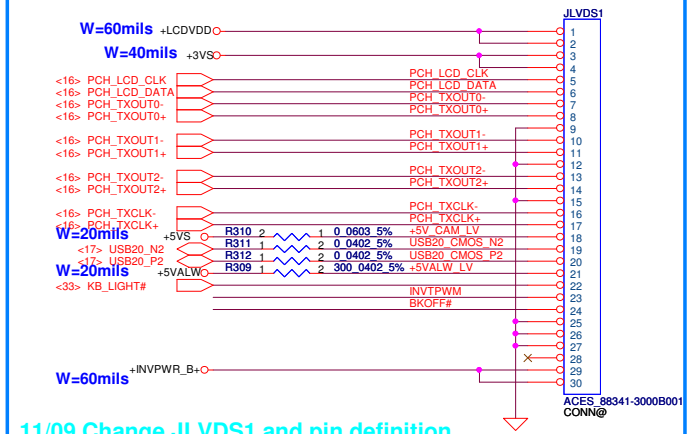




11/09 Change D7 from mount to @

LCD/PANEL BD. Conn.

Copy NAV50 Conn.



11/09 Change JLVDS1 and pin definition
12/04 Change JLVDS1 and pin definition

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: LVDS Connector

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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CRT Connector

10/29 Delete L14,L15,L16 (For layout spacing)

W=40mils

+5VS +R_CRT_VCC +CRT_VCC

D11 RB491D_SC59-3

F1 1.1A_6V_SMD1812P110TF W=40mils

C228 0.1U_0402_16V4Z

<16> PCH_CRT_R
<16> PCH_CRT_G
<16> PCH_CRT_B

PCH_CRT_R PCH_CRT_G PCH_CRT_B

10/29 Delete D8,D9,D10 (For layout spacing)

Copy KAV60

JCRT1 SUYIN_070546FR015S290ZR CONN@

L18 FCM2012CF-800T06_2P CRT_R_2
L19 FCM2012CF-800T06_2P CRT_G_2
L22 FCM2012CF-800T06_2P CRT_B_2

R313 150_0402_1%
R314 150_0402_1%
R315 150_0402_1%
150_0402_1%

C232 C233 C234 22P_0402_50V8J

C235 C236 C237 15P_0402_50V8J

Change to 12pf for DIS

C238 100P_0402_50V8J

DSUB_12 DSUB_15

C242 68P_0402_50V8J

C243 68P_0402_50V8J

0909 Change JCRT1 symbol from KAVAA

+CRT_VCC

C239 0.1U_0402_16V4Z

R317 10K_0402_5%

U8 TC7SET125FUF SC70 5P BUFFER

<16> PCH_CRT_HSYNC PCH_CRT_HSYNC CRT_HSYNC_R R540 39_0402_5% CRT_HSYNC_1

L23 BLM18AG121SN1D_2P CRT_HSYNC_2
L24 BLM18AG121SN1D_2P CRT_VSYNC_2

C240 C241 10P_0402_50V8J

11/11 Correct L23,L24 footprint

+CRT_VCC

C244 0.1U_0402_16V4Z

U9 TC7SET125FUF SC70 5P BUFFER

<16> PCH_CRT_VSYNC PCH_CRT_VSYNC CRT_VSYNC_R R541 39_0402_5% CRT_VSYNC_1

11/03 Change U8,U9 from SA411250130 to SA00000RZ00

11/10 Add C518,C519 (EMI Recommend)

+3VS

C518 680P_0402_50V7K

C519 680P_0402_50V7K

PCH DDC PU 2.2K
on Page 17

+CRT_VCC +3VS

R538 2.2K_0402_5%

R539 2.2K_0402_5%

Q2A Q2B 2N7002DW-T/R7_SOT363-6

<16> PCH_CRT_DATA PCH_CRT_DATA DSUB_12

<16> PCH_CRT_CLK PCH_CRT_CLK DSUB_15

01/15 Change Q2 from
SB00000AR00 to SB00000D900
03/05 Change Q1,Q2 from SB00000D900 to SB00000DH00 (MFG Recommend)

9/10 Change from 2N7002E-T1-E3_SOT23-3
to 2N7002DW-T/R7_SOT363-6
Michael

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: CRT Connector

Size: B | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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10/22 Change R335(1442@) from 3.3kohm to 3.4kohm (Vendor Recommend)

R335 3.4K_0402_1% 1442@
R335 1.2K_0402_1% 7318C@

10/23 Change R327 from 7318C@ from @
Change R332 from @ to 7318C@
(Vendor Recommend)

10/23 Delete R324(7318C@),R329(7318C@) for Calpella

12/22 Change R332 from 7318C@ to 1442@

12/22 Change R338 from @ to 1442@

01/20 Add R651 (Asmedia Recommend)

U10
PS8101QFN48G QFN 48P
8101@

06/25 Mirror L8,L9,L10,L11

11/09 Delete R350(@)

11/17 Change net name from +5VS to +5VS_HDMI

11/17 Add F2 (Safety Recommend)

Copy KHLB0

11/09 Delete R353

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/03/20

Compal Electronics, Inc.

Title: HDMI Level Shifter & Conn.

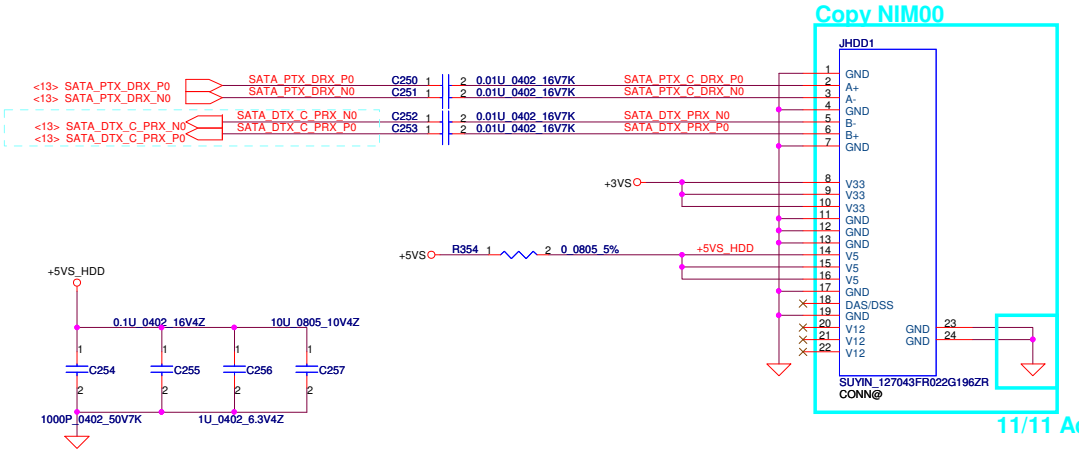
Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

Date: Tuesday, March 09, 2010 | Sheet 24 of 48

HDD

SATA HDD Conn.

Copy NIM00



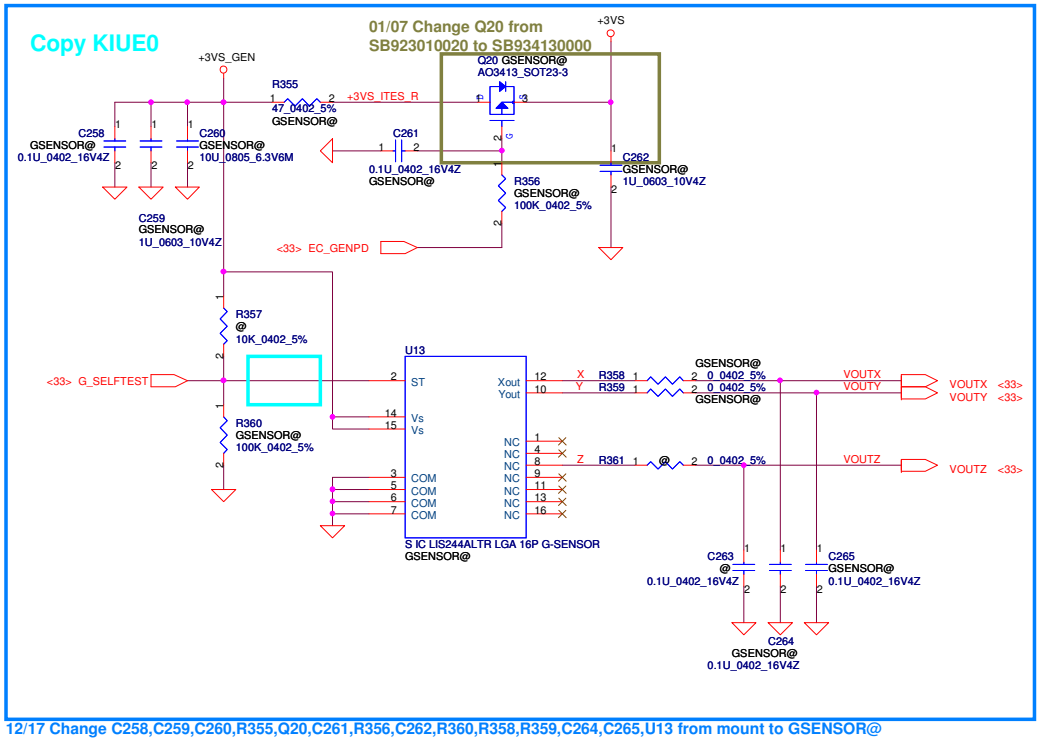
11/11 Add GND net on JHDD1.23 and JHDD1.24

G-Sensor

11/11 Correct Q20 footprint

Copy KIUE0

01/07 Change Q20 from SB923010020 to SB934130000



12/17 Change C258,C259,C260,R355,Q20,C261,R356,C262,R360,R358,R359,C264,C265,U13 from mount to GSENSOR@

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: **HDD Conn/G-Sensor**

Size	Document Number	Rev
B	NAU00 M/B LA-6101P Schematics	1.0

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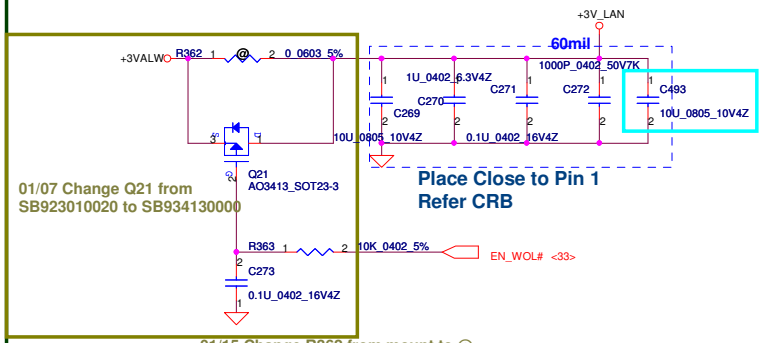
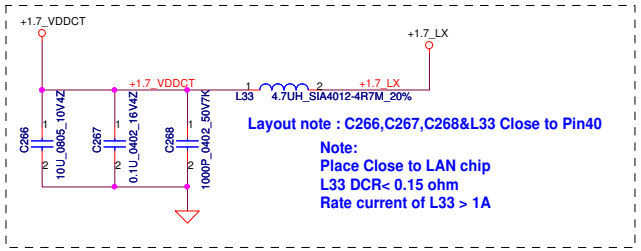
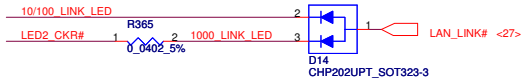
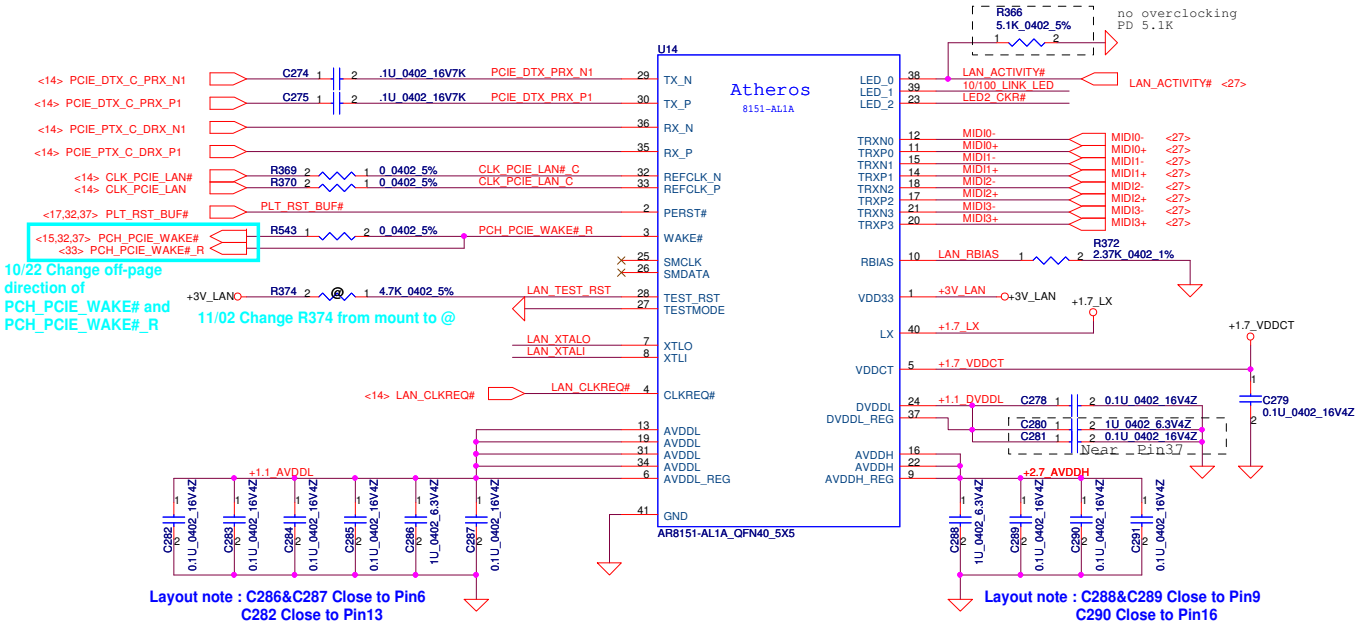
LAN Power Circuit & Refer NPUC9

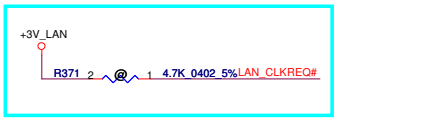




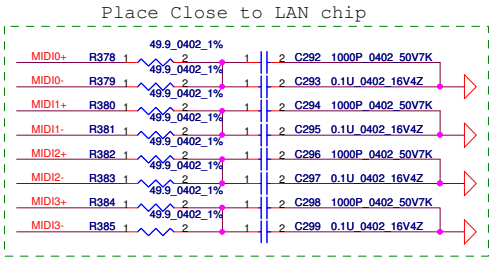
10/22 Remove R364

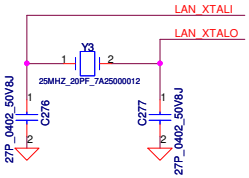






10/22 Change R376 from mount to @
11/02 Change R373 from mount to @
11/02 Delete Q3(@),R375(@),R377(@)
11/09 Delete R373(@),R376(@)





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Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: LAN AR8151

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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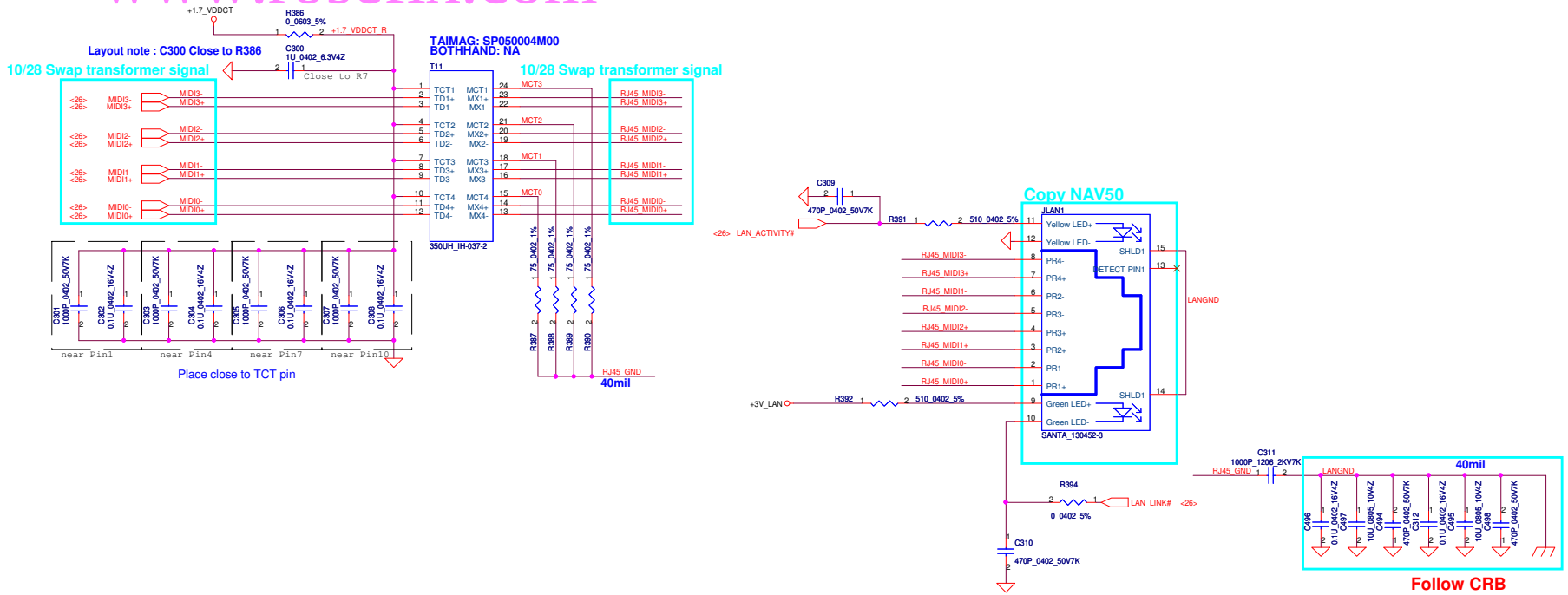

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

Size	Document Number	Rev
	NAU00 M/B LA-6101P Schematics	1.0

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CR_REFE must far away from 48MHz clock trace.

Place CR1,RR2 close to U15 Pin1

11/04 Change CR1 from SE071101J1M to SE071101J80

11/09 Delete RR1(@)

Pin1 and pin6 of U15 trace width = 20mil

11/09 Delete RR4

40mil

40mil

40mil

+V18_CR : 20mil

Place CR2,CR3 close to U15 Pin4

Place CR4,CR5 close to U15 Pin5,6

Ground pad must have 4 via

no more than 2 via on all signal trace

Pin8 and Pin15 Keep trace routing lengths as short as possible, Avoid via and layer changes

Close to U15 pin24

12/22 Mount RR7,CR6

20mil

20mil

7 in 1 Card Reader

Copy NCQF0

Close to JCR1

EMI reserved

Close to JCR1

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: **Card Reader/7-IN-1 Socket**

Size: Custom | Document Number: **NAU00 M/B LA-6101P Schematics** | Rev: 1.0

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10/29 Follow NTUC0

<33> BEEP# — R414 47K_0402_5% — C332 0.1U_0402_16V4Z — MONO_IN

<13> PCH_SPKR — R415 47K_0402_5%

R416 10K_0402_5% — C328 0.1U_0402_16V4Z

10/29 Delete C333,C334,D15,Q22,R411,R412,R413
Change R414,R415 from 560ohm to 47kohm
Change C332,C328 from 1uF to 0.1uF

+5VS — L34 FBMA-L11-201209-221LMA30T_0805 — +5VAMP — C329 0.1U_0402_16V4Z — C330 0.1U_0402_16V4Z

U16 G9191-475T1U_SOT23-5: IN, GND, SHDN, OUT, BYP — 40mil — 40mil — +VDDA — C331 2.2U_0603_6.3V6K

J3 JUMP_43X39

(output = 300 mA) 4.75V

DVT NU it.091509.

+3VS — L35 0_0603_5% — +1.5VS — L50 @ 0_0603_5% — change to +3vs — 10U_0805_10V4Z — C337 — C338 0.1U_0402_16V4Z — +1.5VS_3VS_HDIO

11/09 Change L35,L36,L50 from SM010015410 to SD013000080

+3VS — L36 0_0603_5% — 10U_0805_10V4Z — C341 @ — C342 100P_0402_50V8J — C343 0.1U_0402_16V4Z — 20mil — +3VS_HD

W=40mil — +5VS — C335 10U_0805_10V4Z — C336 0.1U_0402_16V4Z

W=40mil — +5VS — C339 10U_0805_10V4Z — C340 0.1U_0402_16V4Z

+HD_AVDD — 100P_0402_50V8J — 0.1U_0402_16V4Z — 40mil — L37 FBMA-L11-160808-800LMT_0603 — +VDDA

C344 @ — C345 0.1U_0402_16V4Z — C346 — C347 10U_0805_10V4Z

11/11 Correct L37 footprint

HDA_BITCLK_AUDIO_R — R418 22_0402_5% — C348 @ 10P_0402_50V8J

U17 ALC259-VB5-GR_QFN48_7X7

DVDD — DVDD_IO — PVDD1 — PVDD2 — AVDD1 — AVDD2

LINE1_L — LINE1_R — SPK_OUT_L+ — SPK_OUT_L- — SPKL+ — SPKL- — SPKL+ <30> — SPKL- <30>

LINE2_L — LINE2_R — SPK_OUT_R+ — SPK_OUT_R- — SPKR+ — SPKR- — SPKR+ <30> — SPKR- <30>

MIC1_L — MIC1_R — HP_OUT_L — HP_OUT_R — HP_LEFT — HP_RIGHT — HP_LEFT <30> — HP_RIGHT <30>

<30> MIC1_L_R — <30> MIC1_R_R — C465 4.7U_0603_6.3V6K — C466 4.7U_0603_6.3V6K — MIC1_L — MIC1_R

11/10 Change R465,R466 from SE053475Z80 to SE107475M80 (Realtek Recommend)

MIC2_L — MIC2_R

02/26 Change R422 from SD028000080 to SM01000CY00

+MIC1_VREFO_R — C349 @ 0.1U_0402_16V4Z — +MIC1_VREFO_L — C350 @ 0.1U_0402_16V4Z

SYNC — HDA_SYNC_AUDIO <13>

BCLK — HDA_BITCLK_AUDIO_R — R421 0_0402_5% — HDA_BITCLK_AUDIO <13>

SDATA_OUT — HDA_SDOUT_AUDIO_R — R423 0_0402_5% — HDA_SDOUT_AUDIO <13>

add it for EMI.072409.

SDATA_IN — HDA_SDIN0_R — R425 33_0402_5% — HDA_SDIN0 <13>

EAPD — R426 0_0402_5% — EC_EAPD <33>

01/07 Change C351.2 from R422.2 to R422.1

<30> DMIC_DATA_R — R420 0_0402_5% — DMIC_DATA — GPIO0/DMIC_DATA

C351 @ 10P_0402_50V8J — <30> DMIC_CLK_R — R422 FBMA-10-100505-301T-0402 — DMIC_CLK — GPIO1/DMIC_CLK

01/07 Add R648(@) to +HD_AVDD (Realtek Recommend)

<33> EC_MUTE# — R424 0_0402_5% — +HD_AVDD — R648 @ 10K_0402_5% — PD#

<13> HDA_RST#_AUDIO — C499 @ 0.01U_0402_16V7K — HDA_RST#_AUDIO — RESET#

add it.070709

<30> HP_PLUG# — R427 39.2K_0402_1% — SENSE_A

<30> MIC_PLUG# — R428 20K_0402_1%

MONO_IN — C352 @ 100P_0402_50V8J — PCBEEP

10/30 Change C352 GND from AGND to GND

SENSE_A — SENSE A

SENSE B

C353 2.2U_0402_6.3V6M — CBP

CBN

+MIC1_VREFO_L — 10mil — MIC1_VREFO_L

change pin31 and pin28

PVSS2 — PVSS1 — DVSS2 — DVSS1

MIC2_VREFO

MIC1_VREFO_R — +MIC1_VREFO_R — C492 @ 10U_0805_10V4Z

LDO_CAP — CODEC_LDO_CAP — 10mil

VREF — +CODEC_VREF — 10mil

JDREF — +CODEC_JDREF — 10mil

CPVEE — CODEC_CPVEE — 10mil

C354 @ 10U_0805_10V4Z — C355 0.1U_0402_16V4Z

C356 2.2U_0402_6.3V6M — R432 20K_0402_1%

AVSS1 — AVSS2

DGND — AGND

11/05 Add net name : CODEC_LDO_CAP,+CODEC_VREF,+CODEC_JDREF,CODEC_CPVEE

10/21 Change U17 to SA00003QR00 Symbol

03/04 Change U17 from SA00003QR00 to SA00003QR10

DGND To AGND Bypass

R431 0_0402_5% — R433 0_0402_5% — R434 0_0402_5% — R605 0_0402_5%

DGND — AGND

11/02 Change R429,R430,R431,R433,R434,R605 from 0_0603 to 0_0402 (Layout Spacing)

11/17 Delete R429,R430

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 32, 33)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 48)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 20)
	5.1K	PORT-H (PIN 47)

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: HDA Codec ALC259Q-GR

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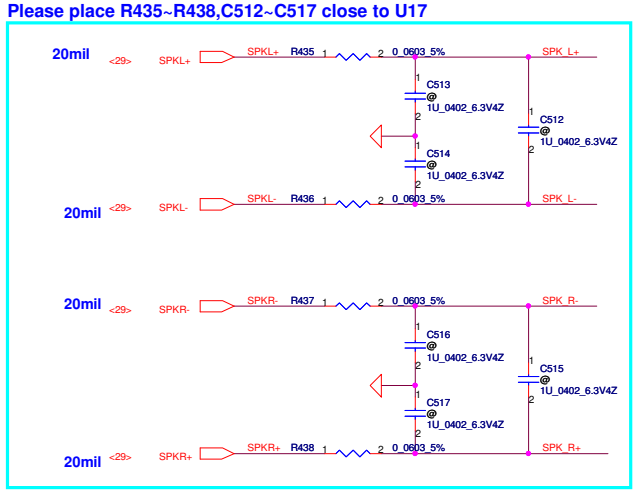
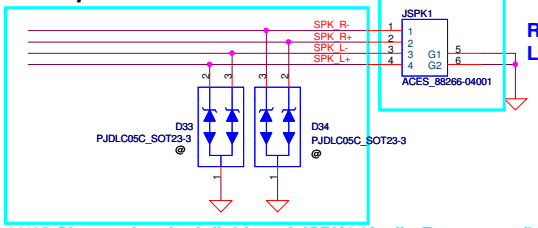
11/11 Change R435~R438 from SD010012010 to SD013000080
11/10 Add C512~C517(@) for EMI (Follow Realtek CRB)
Please place R435~R438,C512~C517 close to U17



Int. Speaker Conn.

Copy KTV00

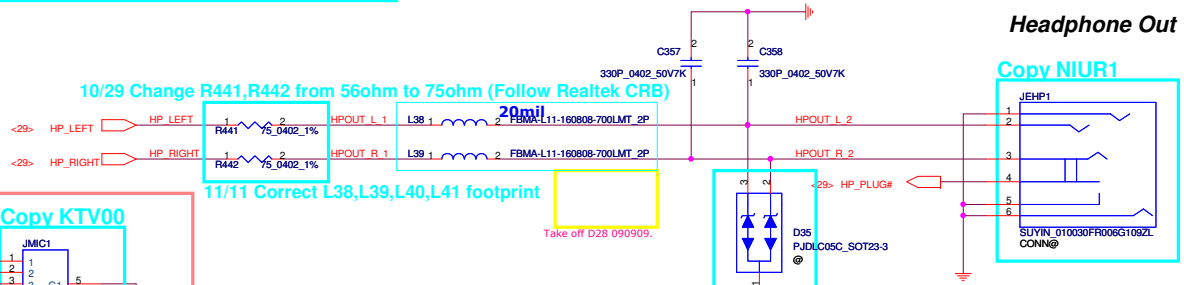


11/18 Change the pin definition of JSPK1 (Audio Recommend)
11/18 Swap D33

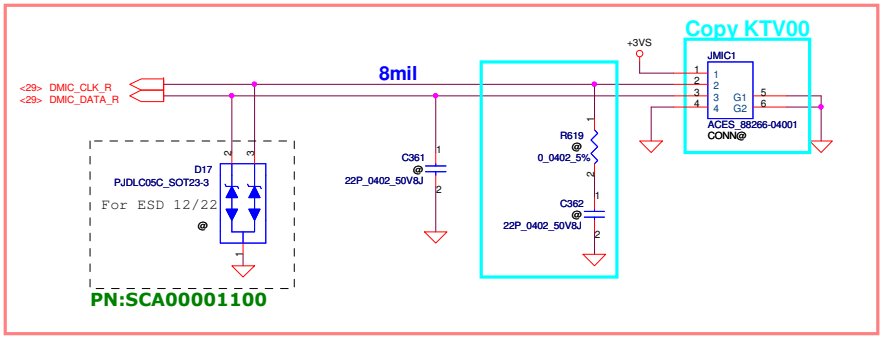
Headphone Out

Copy NIUR1

10/29 Change R441,R442 from 56ohm to 75ohm (Follow Realtek CRB)



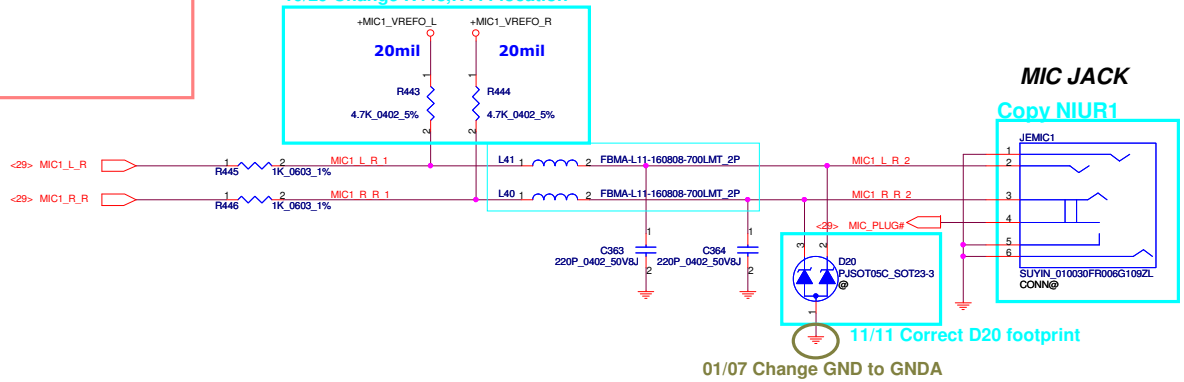
11/11 Correct L38,L39,L40,L41 footprint
Take off D28 090909.
01/07 Change GND to GNDA



10/29 Short D18,D19 (Follow Realtek CRB)
10/29 Change R443,R444 location

MIC JACK

Copy NIUR1



11/11 Correct D20 footprint
01/07 Change GND to GNDA

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Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: Audio Jack/MIC Conn/SPK Conn

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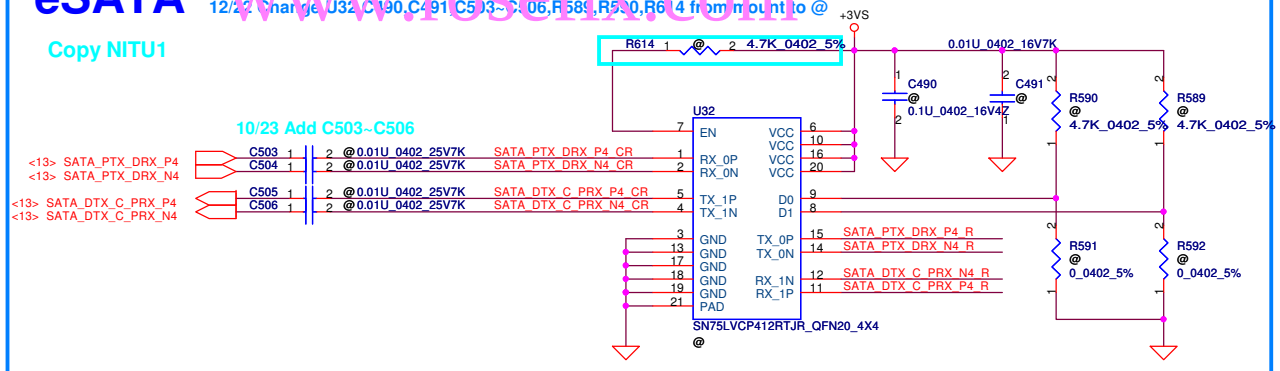
eSATA

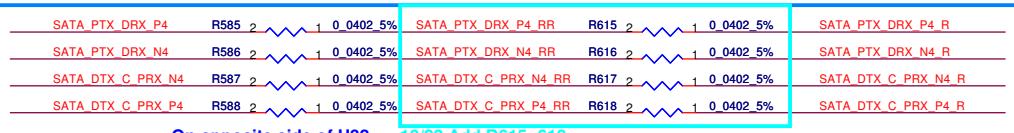
10/22 Add R614, change R590,R589 from 0ohm to 4.7kohm (Vendor Recommend)

12/22 Change U32,C490,C491,C503~C506,R585~R590,R614 from mount to @

Copy NITU1

10/23 Add C503~C506





On opposite side of U32

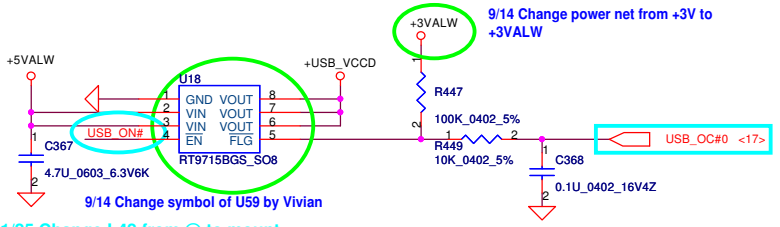
10/23 Add R615~618

12/22 Change R585~R588,R615~R618 from @ to mount

TI:D0 D1					SN75LVCP412		
EN	BA	BB			CHANNEL 0	CHANNEL 1	
0	X	X			Low-power	Low-power	
1	0	0			0dB	0dB	(Default)
1	1	0			2.5dB pre-emphasis	0dB	
1	0	1			0dB	2.5dB pre-emphasis	
1	1	1			2.5dB pre-emphasis	2.5dB pre-emphasis	

9/14 Change power net from +3V to +3VALW

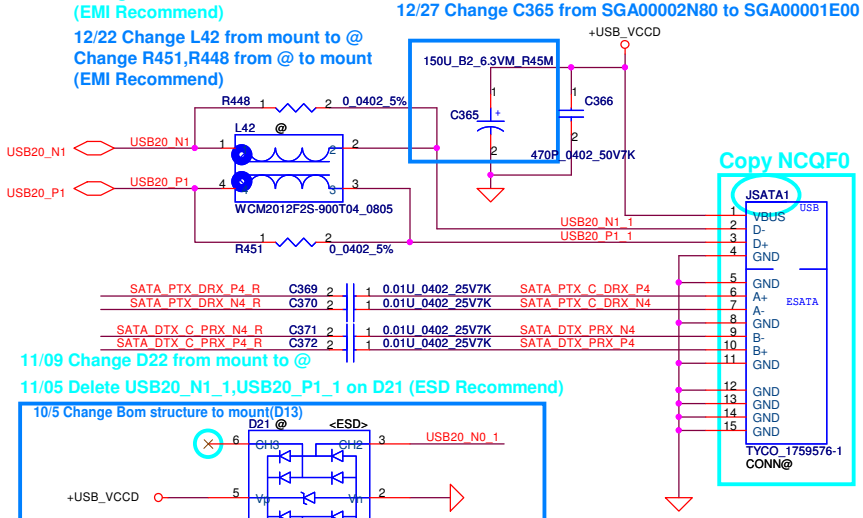
9/14 Change symbol of U59 by Vivian



11/25 Change L42 from @ to mount
Change R451,R448 from mount to @
(EMI Recommend)

12/22 Change L42 from mount to @
Change R451,R448 from @ to mount
(EMI Recommend)

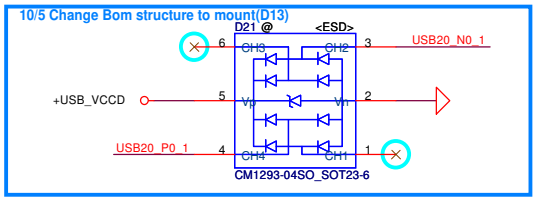
12/27 Change C365 from SGA00002N80 to SGA00001E00



11/09 Change D22 from mount to @

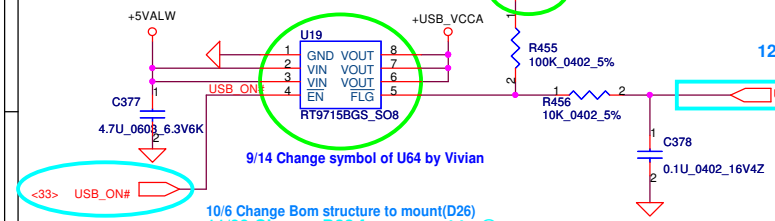
11/05 Delete USB20_N1_1,USB20_P1_1 on D21 (ESD Recommend)

10/5 Change Bom structure to mount(D13)



USB Port

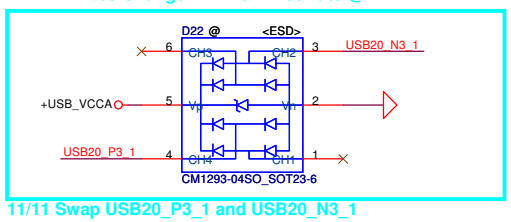
9/14 Change power net from +3V to +3VALW



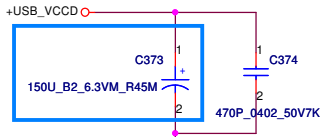
9/14 Change symbol of U64 by Vivian

10/6 Change Bom structure to mount(D26)

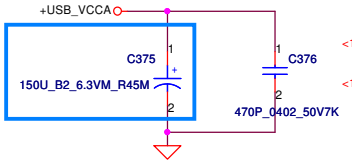
11/09 Change D22 from mount to @

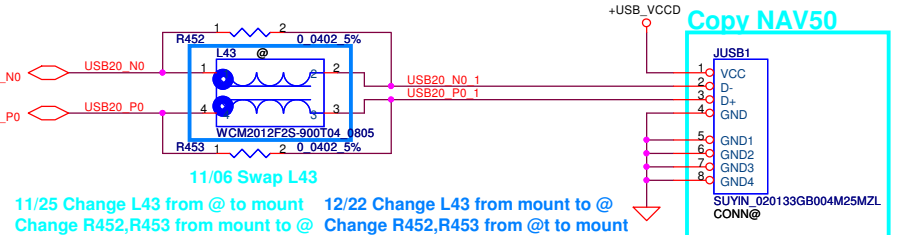


11/11 Swap USB20_P3_1 and USB20_N3_1



12/27 Change C373,C375 from SGA00002N80 to SGA00001E00

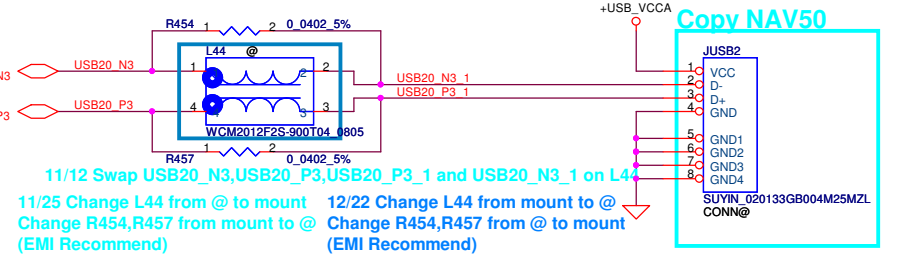




11/06 Swap L43

11/25 Change L43 from @ to mount
Change R452,R453 from mount to @
(EMI Recommend)

12/22 Change L43 from mount to @
Change R452,R453 from @t to mount
(EMI Recommend)



11/12 Swap USB20_N3,USB20_P3,USB20_P3_1 and USB20_N3_1 on L44

11/25 Change L44 from @ to mount
Change R454,R457 from mount to @
(EMI Recommend)

12/22 Change L44 from mount to @
Change R454,R457 from @ to mount
(EMI Recommend)

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: USB / BT / eSATA

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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WLAN

10/22 Add Net : BT_ACTIVE and R613, Delete T13
11/10 Add R631(@)

Copy NTUC0

11/14 Add +1.5VS

JWLAN1

R460 0_0402_5%

<15,26,37> PCH_PCIE_WAKE#
R631 @ 0_0402_5% BT_ACTIVE_R
R613 @ 0_0402_5% BT_ACTIVE_R
<35> BT_ACTIVE
<14> MINI1_CLKREQ#

<14> CLK_PCIE_MINI1#
<14> CLK_PCIE_MINI1

<14> PCIE_DTX_C_PRX_N2
<14> PCIE_DTX_C_PRX_P2

<14> PCIE_PTX_C_DRX_N2
<14> PCIE_PTX_C_DRX_P2

+3VS_WLAN

<33> EC_TX_P80_DATA
<33> EC_RX_P80_CLK

R634 100K_0402_5%

FOX_AS0B226-S40N-7F

11/10 Change net : EC_TX_P80_DATA from JWLAN1.17 to JWLAN1.49
Add R634

+3VS_WLAN R458 0_0603_5% +3VS
R459 @ 0_0603_5% +3VALW

WL_OFF# <33>
PLT_RST_BUF# <17,26,37>
R632 0_0402_5% +3VS_WLAN
R633 @ 0_0402_5% +3VALW

11/10 Add R632,R633(@)

PCH_SMBCLK <12,14,37>
PCH_SMBDATA <12,14,37>

11/17 Add GND on JWLAN1.40

USB20_N8 <17>
USB20_P8 <17>

WWAN_LED# R646 @ 0_0402_5%
WLAN_LED# R647 @ 0_0402_5%
WLAN_LED# <35>

12/16 Add R646(@),R647

10/22 Reserve pull-up resister R611(@) for WLAN_LED#
01/21 Change R611 from @ to mount
Change R461 from mount to @

+5VS (9~16mA) +3VS
R461 @ 10K_0402_5%
R611 10K_0402_5%
WLAN_LED#

+3VS_WLAN
0.1U_0402_16V4Z
C379 4.7U_0805_10V4Z
C380 0.1U_0402_16V4Z
C381

10/5 Add C13/C15/C16 by Vivian

WWAN

+3VS_WWAN R462 0_0603_5% +3VS

12/15 Reserve R642(@)
12/16 Add R643(@)

Copy NTUC0

JWWAN1

<15,26,37> PCH_PCIE_WAKE# R643 @ 0_0402_5% PCH_PCIE_WAKE#_3G

11/17 Swap SATA port5 signals

+3VS R642 @ 10K_0402_5%

<13> SATA_PTX_DRX_P5
<13> SATA_PTX_DRX_N5
C489 0.01U_0402_16V7K SATA_PTX_C_DRX_P5
C488 0.01U_0402_16V7K SATA_PTX_C_DRX_N5

<13> SATA_DTX_C_PRX_N5
<13> SATA_DTX_C_PRX_P5
C487 0.01U_0402_16V7K SATA_DTX_PRX_N5
C486 0.01U_0402_16V7K SATA_DTX_PRX_P5

<13> SATA_DTX_C_PRX_P1
<13> SATA_DTX_C_PRX_N1
C382 0.01U_0402_16V7K SATA_DTX_PRX_P1
C384 0.01U_0402_16V7K SATA_DTX_PRX_N1

<13> SATA_PTX_DRX_N1
<13> SATA_PTX_DRX_P1
C385 0.01U_0402_16V7K SATA_PTX_C_DRX_N1
C386 0.01U_0402_16V7K SATA_PTX_C_DRX_P1

+3VS_WWAN

11/17 Change SSD_DET# from JWWAN1.47 to JWWAN1.51

<33> SSD_DET#

+3VALW R469 @ 100K_0402_5%
+3VS R545 @ 100K_0402_5%

FOX_AS0B226-S40N-7F

+3VS_WWAN
+1.5VS

+UIM_PWR
UIM_DATA
UIM_CLK
UIM_RST
UIM_VPP

12/15 Add PLT_RST_BUF# on JWWAN.22
12/16 Add R644(@),R645(@)

R463 0_0402_5% WWAN_OFF# <33>
PLT_RST_BUF# R464 0_0402_5% PLT_RST_BUF# <17,26,37>
R465 @ 0_0402_5% +3VS_WWAN
+3VALW

R644 @ 0_0402_5% PCH_SMBCLK <12,14,37>
R645 @ 0_0402_5% PCH_SMBDATA <12,14,37>

USB20_N13 USB20_N13 <17>
USB20_P13 USB20_P13 <17>

WWAN_LED# WWAN_LED# <35>

R467 @ 100K_0402_5% +5VS
R468 100K_0402_5% +3VS

10/28 Change Net from USB20_N9,USB20_P9 to USB20_N13,USB20_P13

01/22 Change R468 from @ to mount
Change R467 from mount to @

Copy NTUC0

SIM Card Conn.

JSIM1

UIM_VPP
UIM_DATA
R466 @ 10K_0402_5%
+UIM_PWR

GND VPP I/O DET
VCC RST CLK
GND GND

+UIM_PWR
UIM_RST
UIM_CLK

C383 1U_0603_10V4Z

TAITW_PMPAT6-06GLBS7N14N0 CONN@

Reserve for SIM card does not meet rise time and pull-up is needed.

+3VS_WWAN
0.1U_0402_16V4Z
C552 4.7U_0805_10V4Z
C553 0.1U_0402_16V4Z
C554

01/19 Add C552,C553,C554 for +3VS_WWAN

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: WLAN/WWAN

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

Date: Tuesday, March 09, 2010 | Sheet 32 of 48

12/05 Change L48,L49 from SM010016810 to SM010005500

11/10 Change R546 from @ to mount
Change D31 from mount to @

11/10 Add R635(@)

11/02 Delete net : KB_L#DA

12/07 Change R548(@) connection from GND to +3VALW

KB926D3 : Pull-up
KB926E0 : Pull-down

KB926 SPI STRAP PIN

10/21 Reserve R608(@) for EC strap pin

11/10 Change R556 from @ to mount

11/10 Change ME_EN to ME_EN#

For ENE issue

11/02 Change net from KB_LIGHT# to KB_LIGHT#_R

11/05 Change net from KB_LIGHT#_R to KB_LED# (EC Recommend)

11/02 Delete R552

11/05 Delete net : EC_SWI# on U30.103 (Follow NIWE2)
11/12 Add R636, net : H_PROCHOT#

11/03 Delete U29

10/22 Change R561 from mount to @
Change R562 from @ to mount
11/10 Change R562 from mount to @

11/10 Delete C481(@)

11/03 Add AC_PRESENT on U30.115

11/05 Change the power of R566,R567
from +5VALW to +3VALW (Follow NIWE2)

11/05 Delete D32(@), move to close to JBATT1 (ESD Recommend)

11/03 Change R568,R569 from 2.7kohm to 2.2kohm
11/05 Change R568,R569 from mount to @ (Follow NIWE2)
11/10 Delete R568(@),R569(@),C483(@),C484(@)

11/02 Delete U31,Q36,R570

E0 Version
SA00001J5A0

10/21 Change U30 from SA00001J580 to SA00001J5A0

01/11 Change X2 from SJ100003M00 to SJ132P7KW10 (Cost down)

KB926QFA1_LQFP128

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: EC ENE-KB926

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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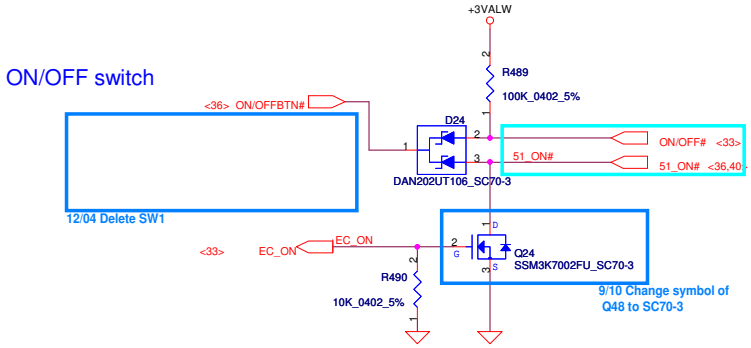
Power Button



Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: Power OK/PBN/TP Lock/LED

Size: B | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

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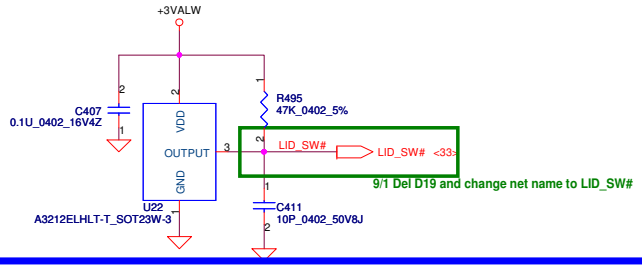
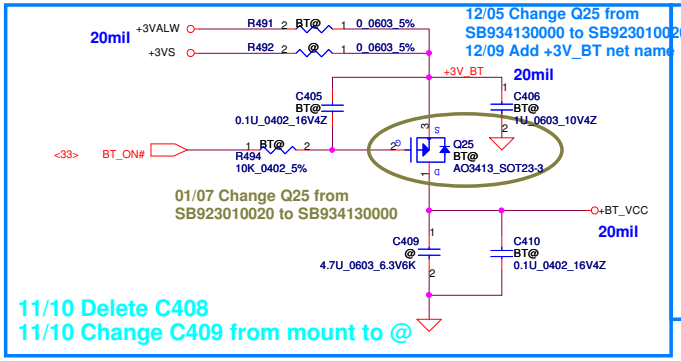
Lid Switch

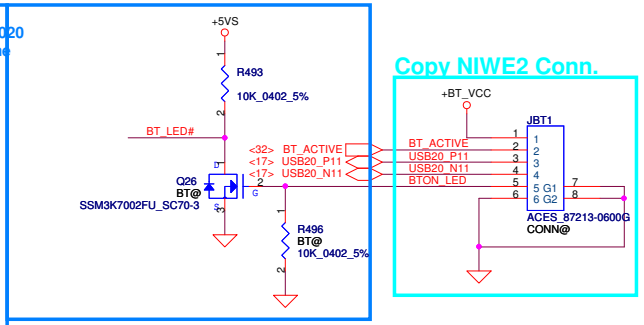
(Hall Effect Switch)



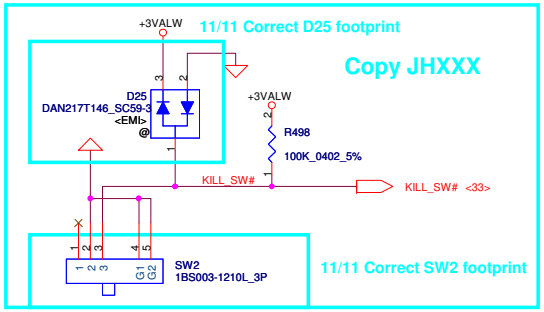
BT

12/17 Change R491,C405,R494,C406,Q25,C410,Q26,R496 from mount to BT@



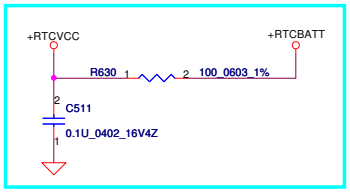


KILL Switch



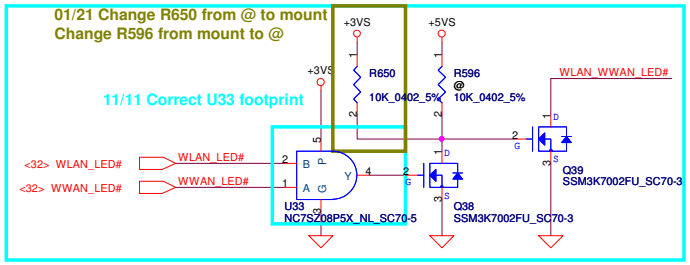
RTC

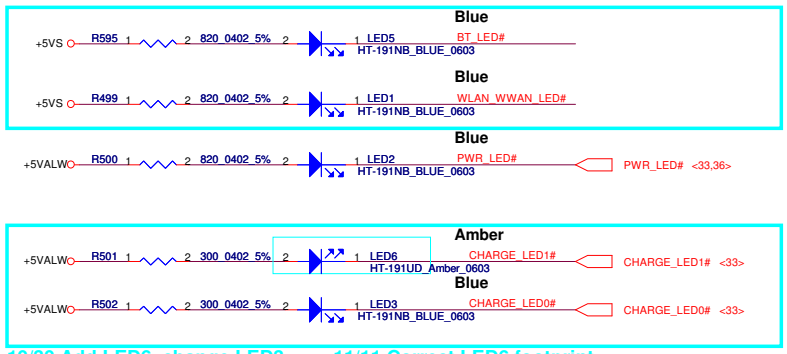
11/10 Delete D26,C412,R497, Add R630,C511 (Follow NIWE2)



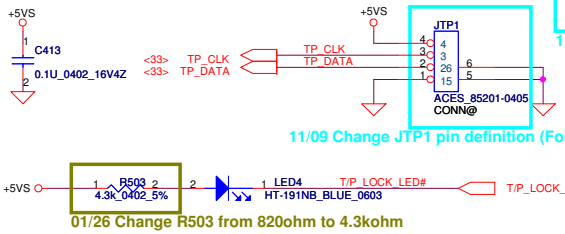
LED

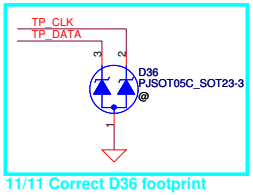
01/20 Add R650(@)





Touch Pad





Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: LID/RTC/BT/TP/KILL SW/LED

Size	Document Number	Rev
	NAU00 M/B LA-6101P Schematics	1.0

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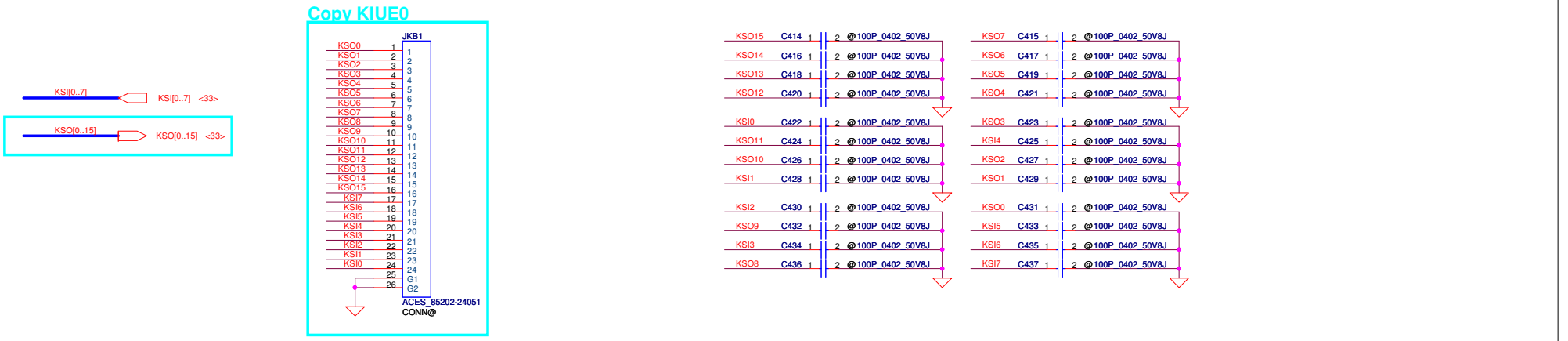
INT_KBD Conn.



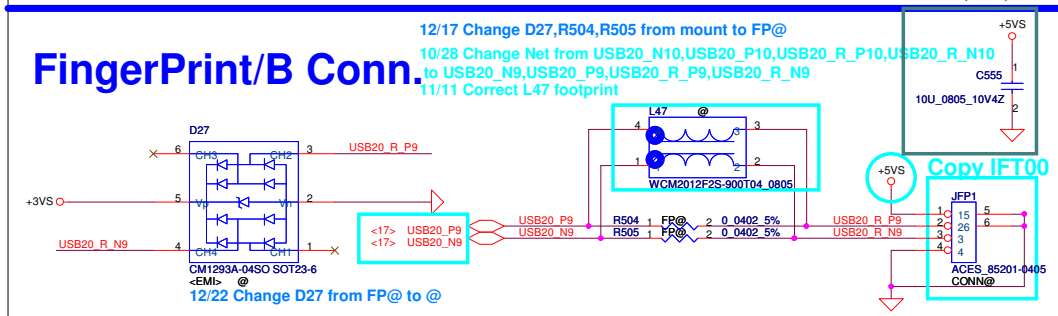
03/02 Add C555 (10uF) for FP power

FingerPrint/B Conn.

12/17 Change D27,R504,R505 from mount to FP@

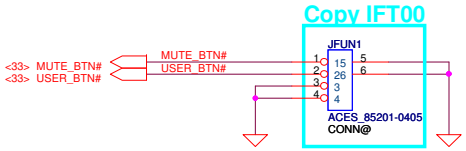
10/28 Change Net from USB20_N10,USB20_P10,USB20_R_P10,USB20_R_N10 to USB20_N9,USB20_P9,USB20_R_P9,USB20_R_N9

11/11 Correct L47 footprint

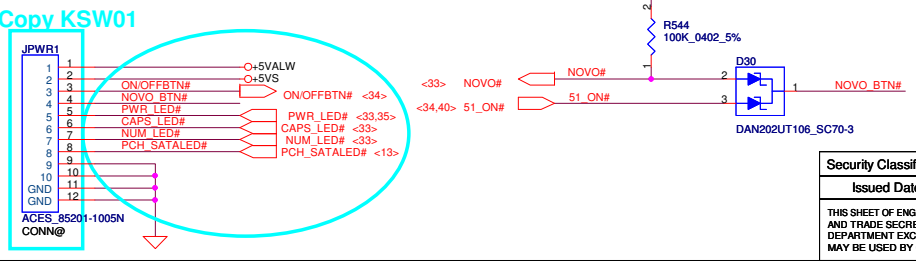


12/22 Change D27 from FP@ to @

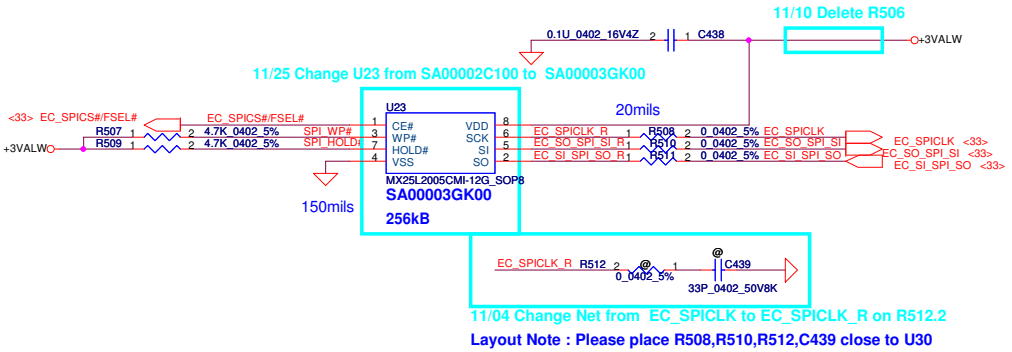
Function/B Conn.



Power/B Conn.



EC SPI ROM



Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.	
Title	BIOS/KBD/Fun_B/PWR_B/FP_B
Size B	Document Number NAU00 M/B LA-6101P Schematics
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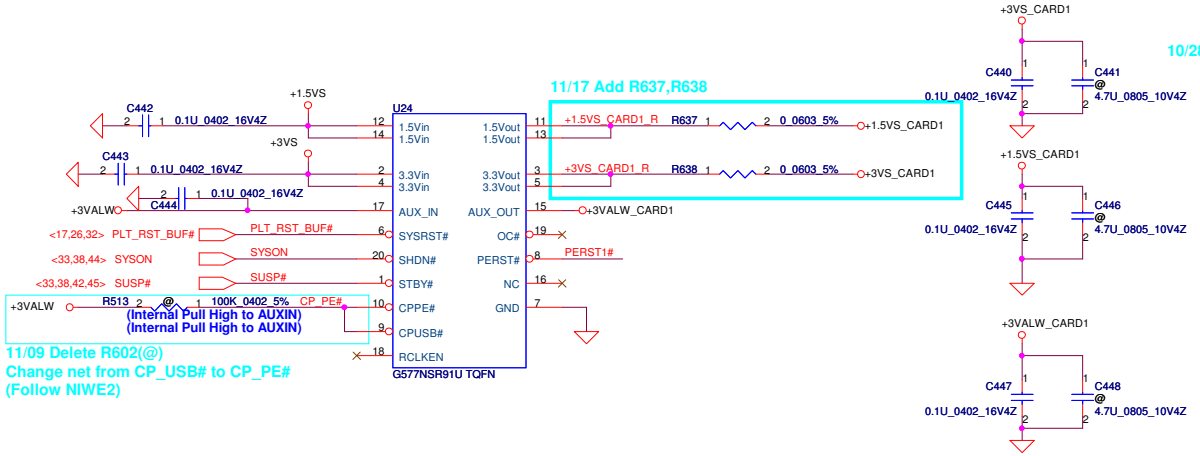
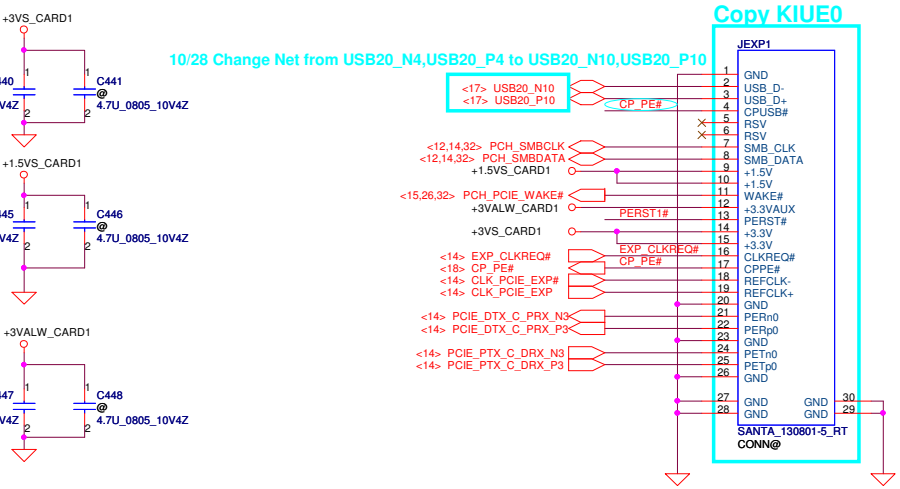
Date: Tuesday, March 09, 2010	Sheet 36 of 48

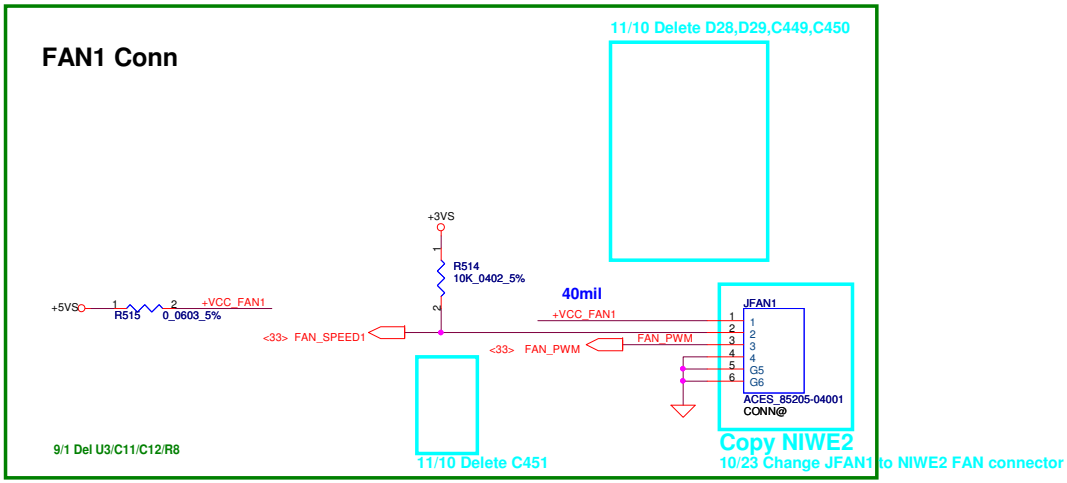
New Card Power Switch

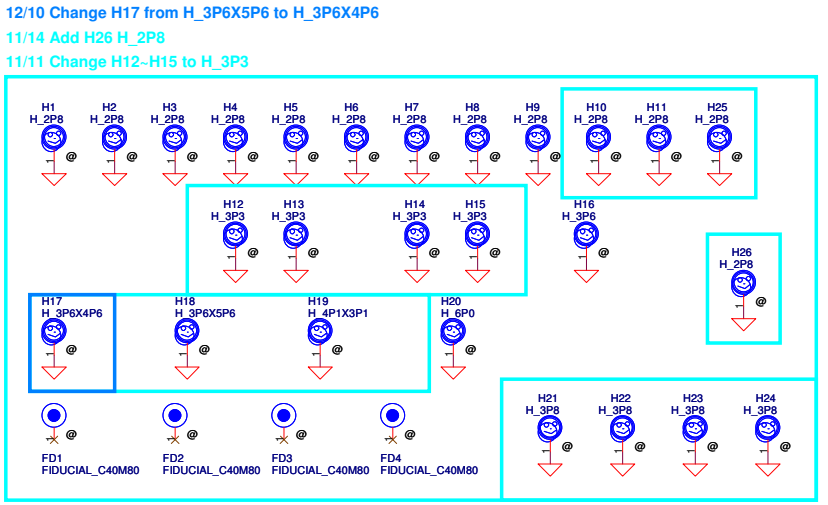


New Card Socket



FAN1 Conn





Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: FAN & Screw Hole

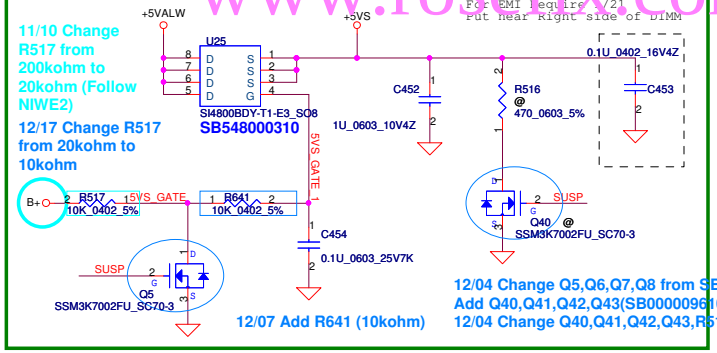
Size	Document Number	Rev
B	NAU00 M/B LA-6101P Schematics	1.0

Date: Tuesday, March 09, 2010 Sheet 37 of 48

+5VALW TO +5VS

11/10 Change R517 from 200kohm to 20kohm (Follow NIWE2)

12/17 Change R517 from 20kohm to 10kohm

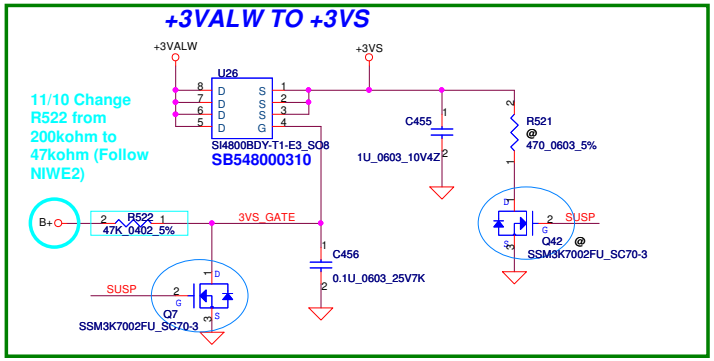


12/07 Add R641 (10kohm)

12/04 Change Q5,Q6,Q7,Q8 from SB00000AR00 to SB000009610
Add Q40,Q41,Q42,Q43(SB000009610)
12/04 Change Q40,Q41,Q42,Q43,R516,R521,R527,R518 from mount to @

+3VALW TO +3VS

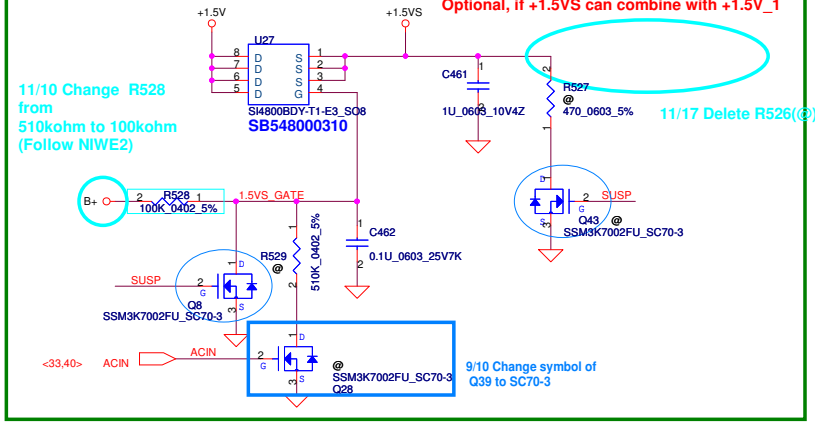
11/10 Change R522 from 200kohm to 47kohm (Follow NIWE2)



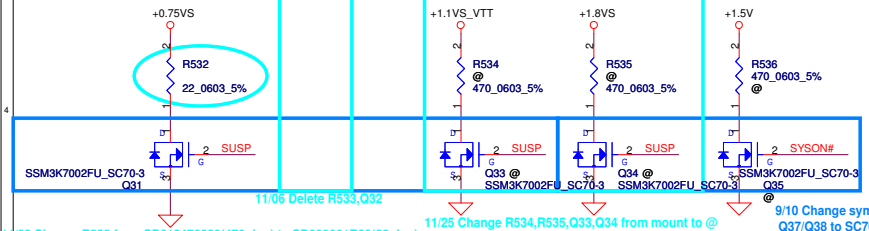
+1.5V to +1.5VS

12/18 Change U27 from SB000007O00 to SB548000310
Optional, if +1.5VS can combine with +1.5V_1

11/10 Change R528 from 510kohm to 100kohm (Follow NIWE2)



9/10 Change symbol of Q39 to SC70-3



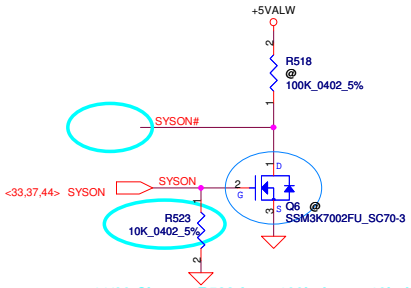
11/06 Delete R533,Q32

11/23 Change R532 from SD013470080(470ohm) to SD000001R80(22ohm) (Follow Intel Recommend)

11/25 Change R534,R535,Q33,Q34 from mount to @

9/10 Change symbol of Q37/Q38 to SC70-3

9/10 Change symbol of Q44/Q64/Q66 to SC70-3

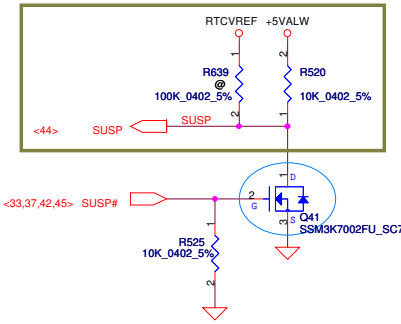


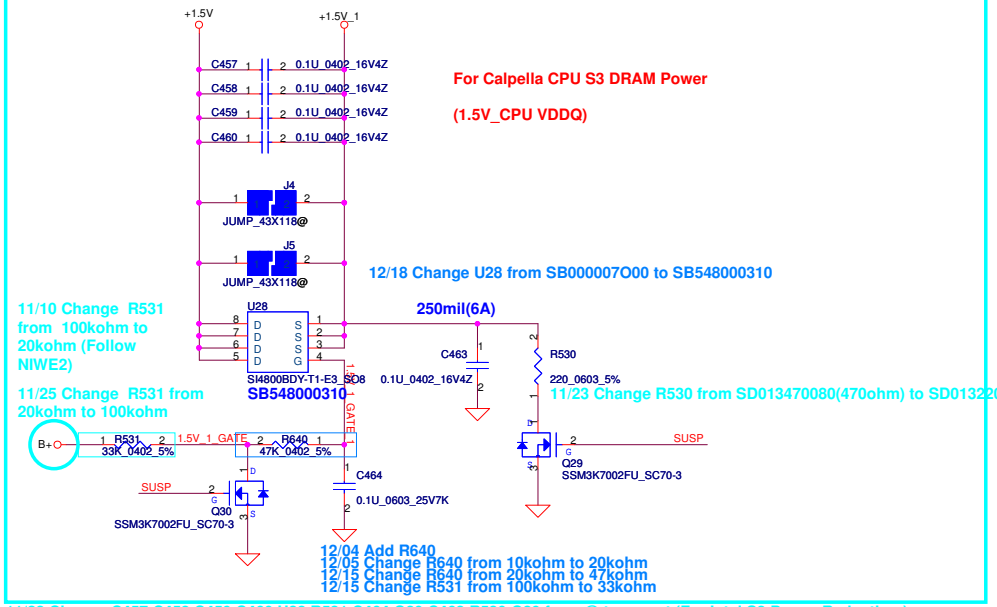
11/09 Change R523 from 100kohm to 10kohm

12/04 Add R639, Change R520 from mount to @

01/21 Change R520 from @ to mount
Change R639 from mount to @

01/21 Change R520 from 100kohm to 10kohm





11/23 Change C457,C458,C459,C460,U28,R531,C464,Q30,C463,R530,Q29 from @ to mount (For Intel S3 Power Reduction.)

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

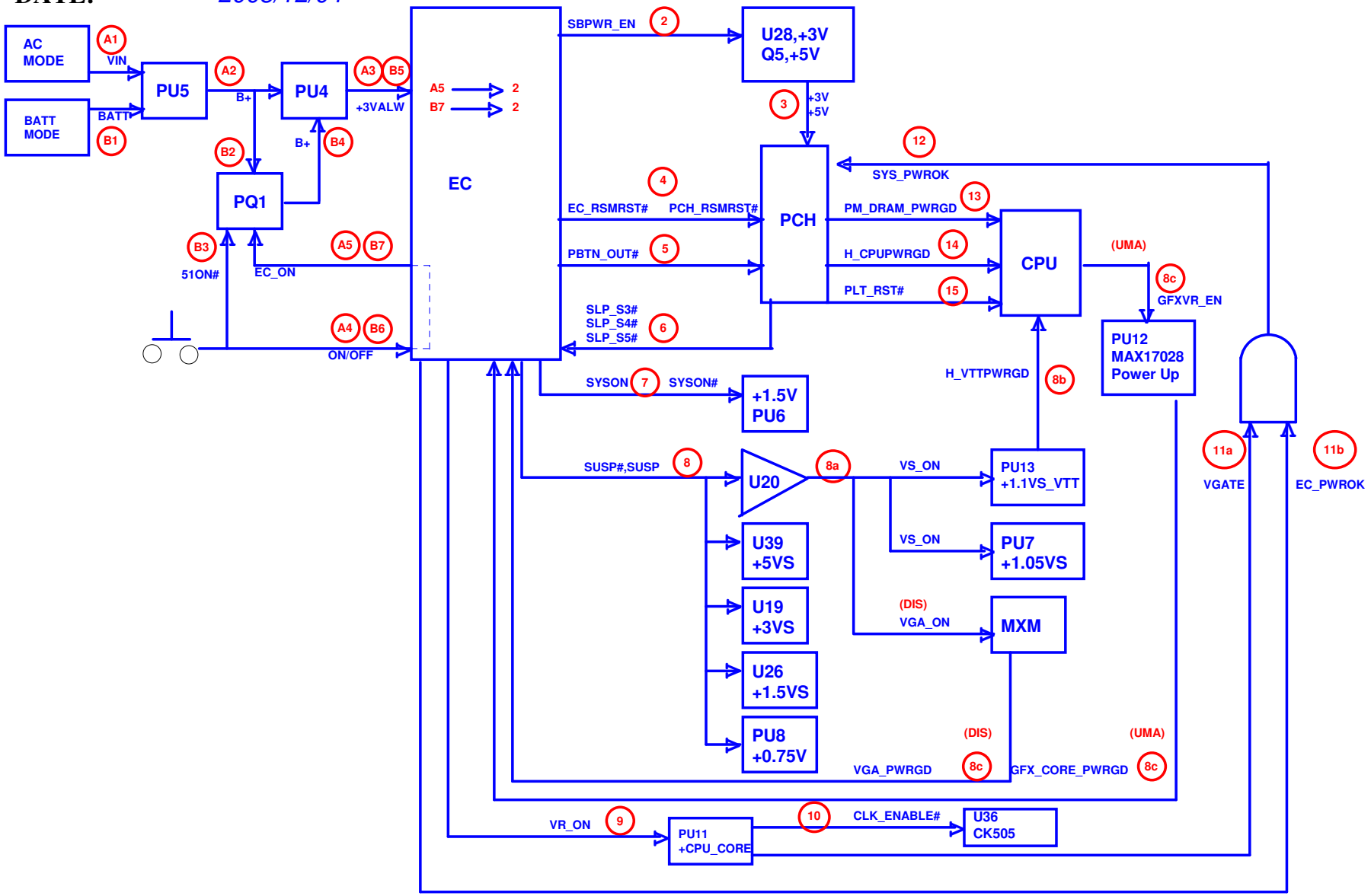
Compal Electronics, Inc.

Title: DC Interface

Size: B | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

Date: Tuesday, March 09, 2010 | Sheet 38 of 48

MODEL NAME: *KBLA0 Power Sequence Block Diagram*
PCB NAME: *LA4811P*
REVISION:
DATE: *2008/12/04*



Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/10/10

Compal Electronics, Inc.

Title: Power Sequence Block Diagram

Size: Custom | Document Number: NAU00 M/B LA-6101P Schematics | Rev: 1.0

Date: Friday, February 26, 2010 | Sheet 39 of 48

ACIN

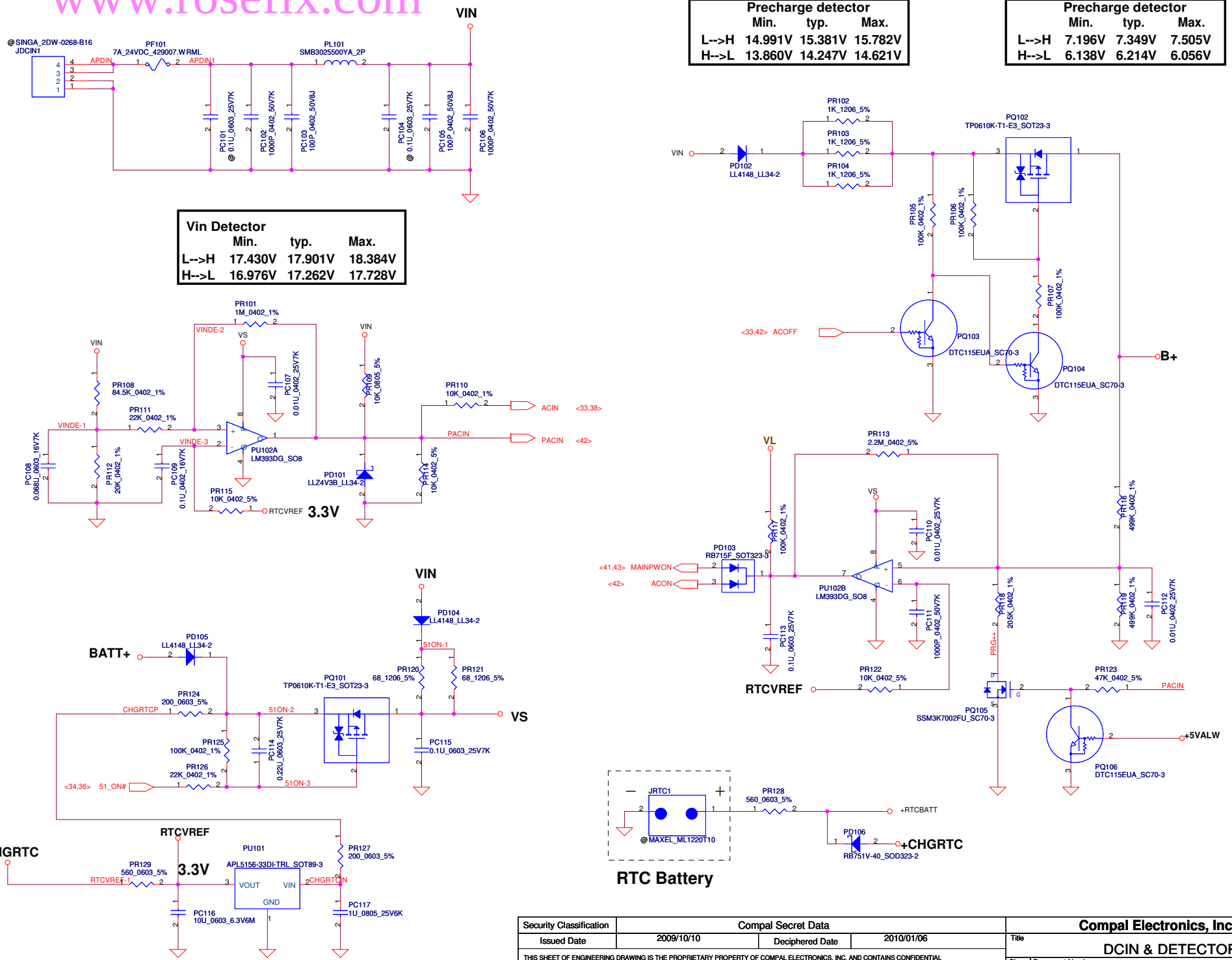
Precharge detector	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

Precharge detector	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

Vin Detector

	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V



Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size	Document Number	Rev
Custom		0.1

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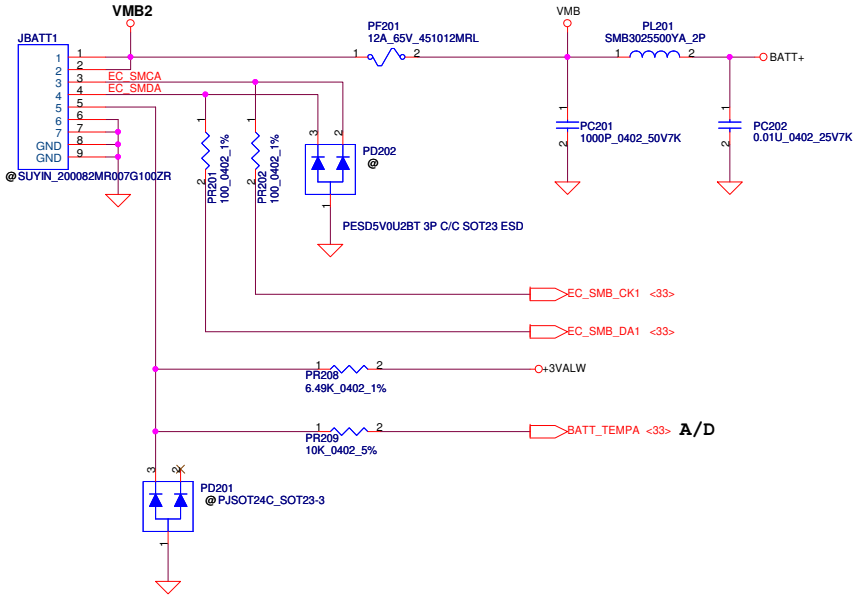
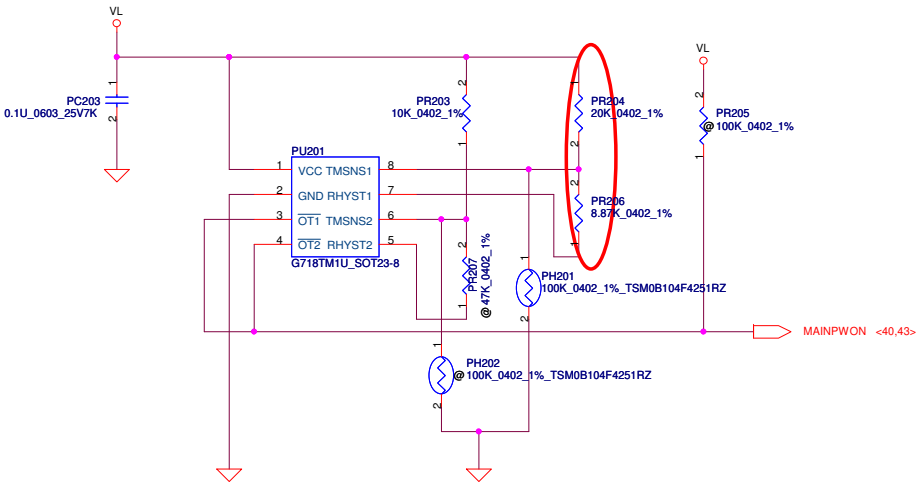
PH1 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C





Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
		0.1

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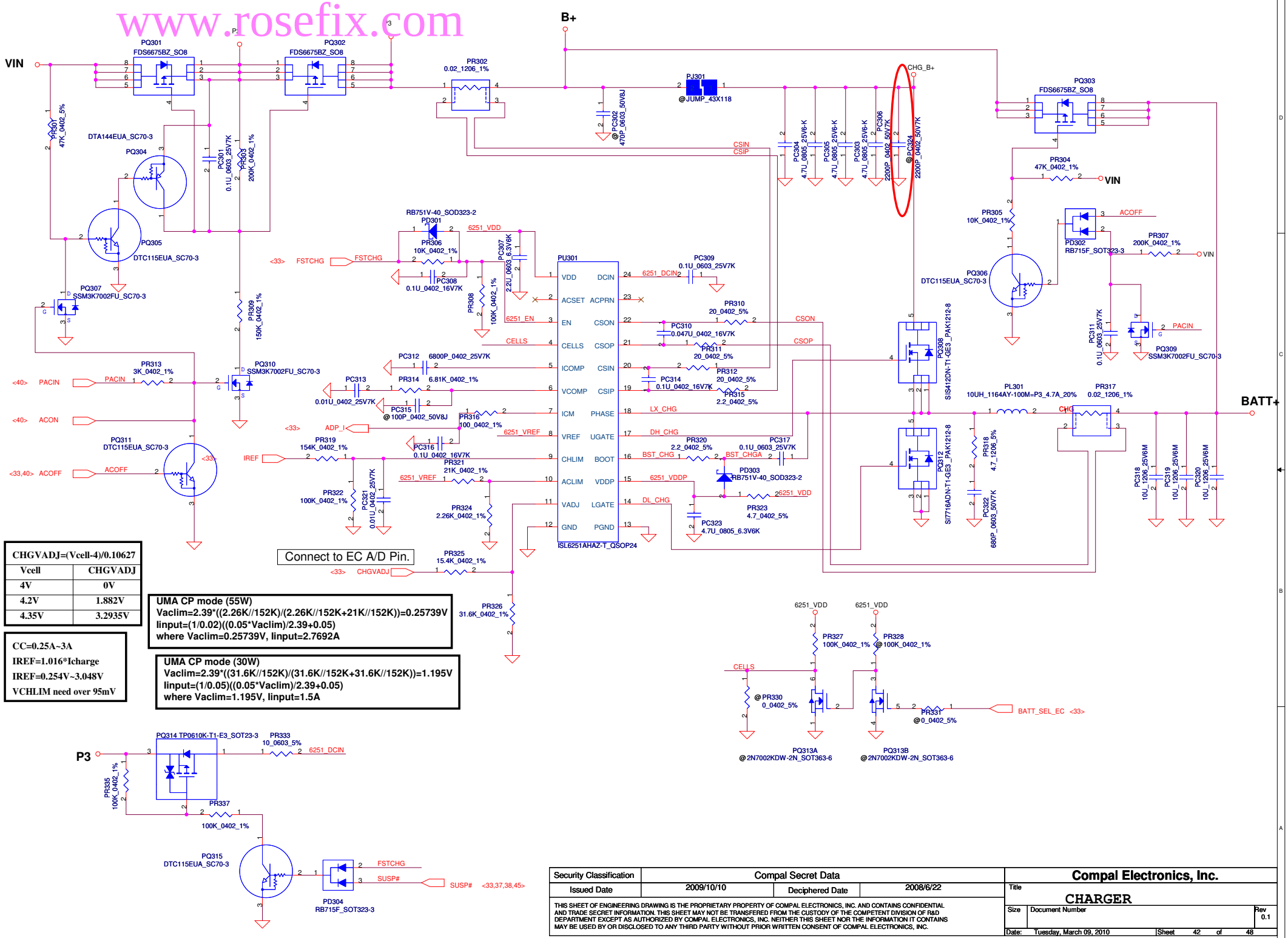

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

UMA CP mode (55W)
Vaclim=2.39*((2.26K//152K)/(2.26K//152K+21K//152K))=0.25739V
Iinput=(1/0.02)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.25739V, Iinput=2.7692A

UMA CP mode (30W)
Vaclim=2.39*((31.6K//152K)/(31.6K//152K+31.6K//152K))=1.195V
Iinput=(1/0.05)((0.05*Vaclim)/2.39+0.05)
where Vaclim=1.195V, Iinput=1.5A

Connect to EC A/D Pin.

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2008/6/22

Compal Electronics, Inc.

Title: CHARGER

Size	Document Number	Rev
		0.1

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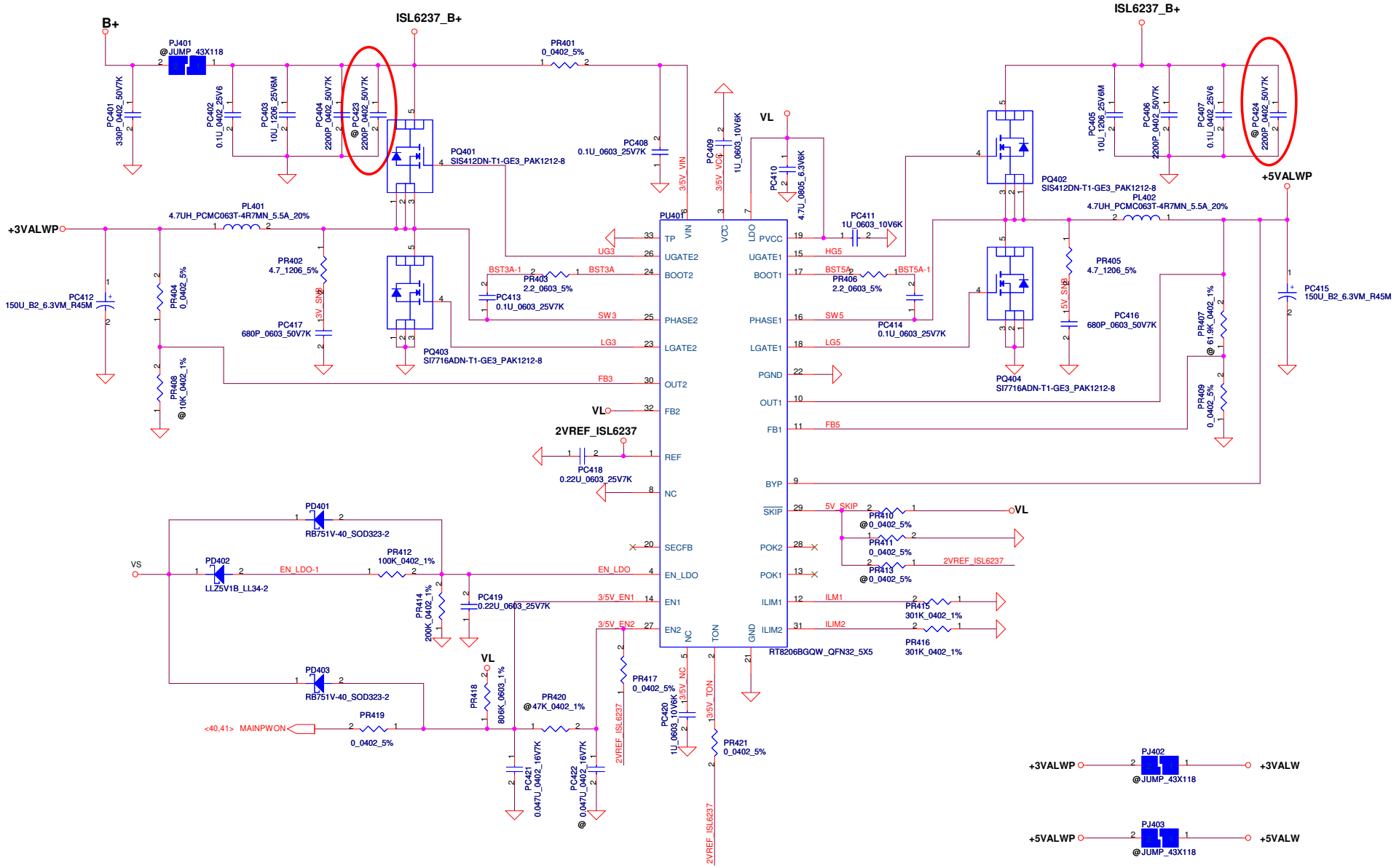


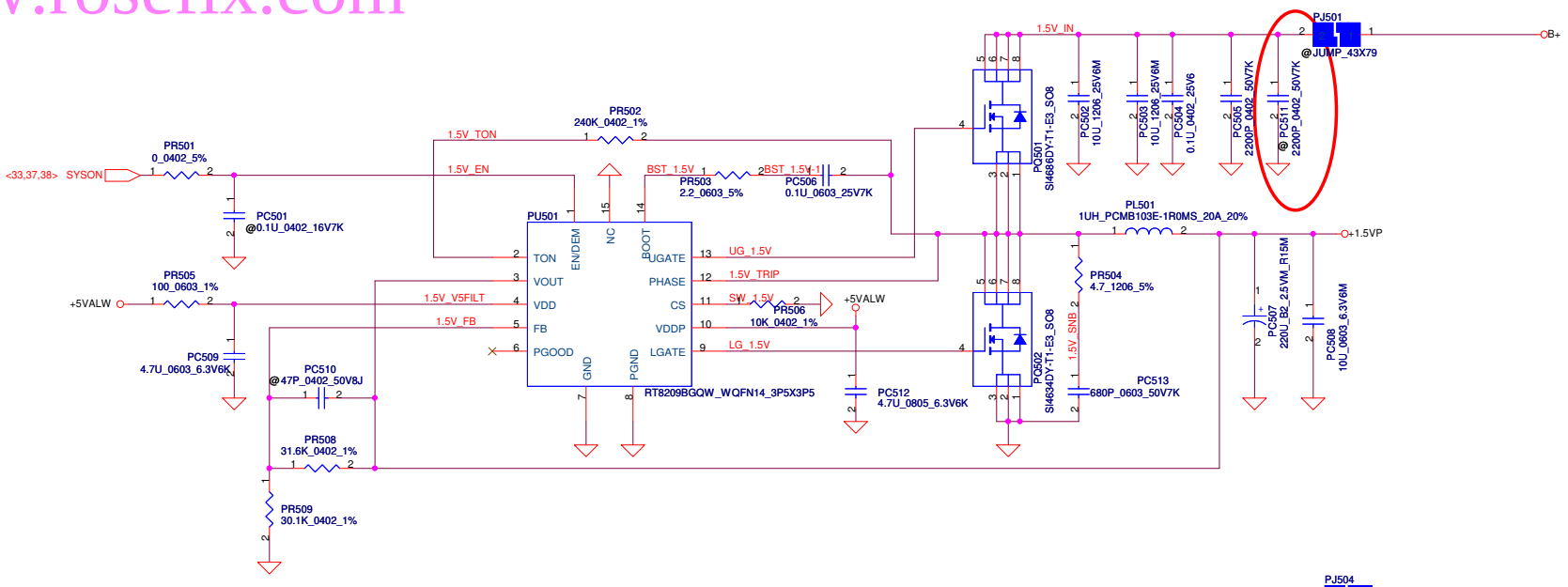
Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/01/06

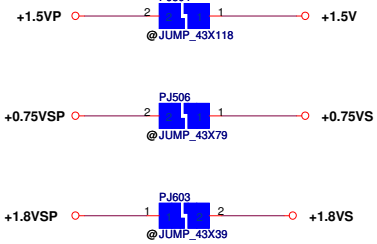
Compal Electronics, Inc.

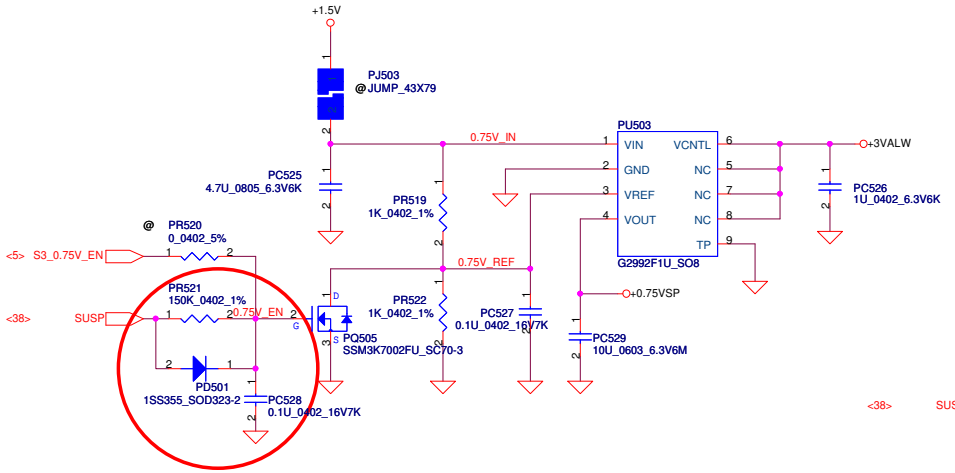
Title: 3VALW/5VALW

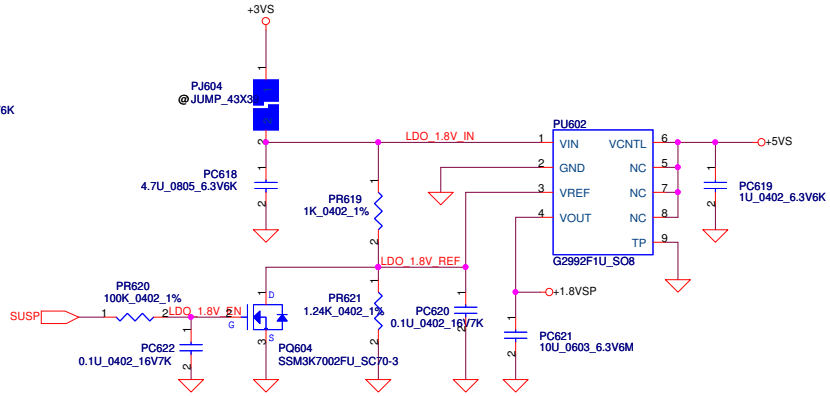
Size	Document Number	Rev
Custom		0.1

Date: Tuesday, March 09, 2010 | Sheet 43 of 48









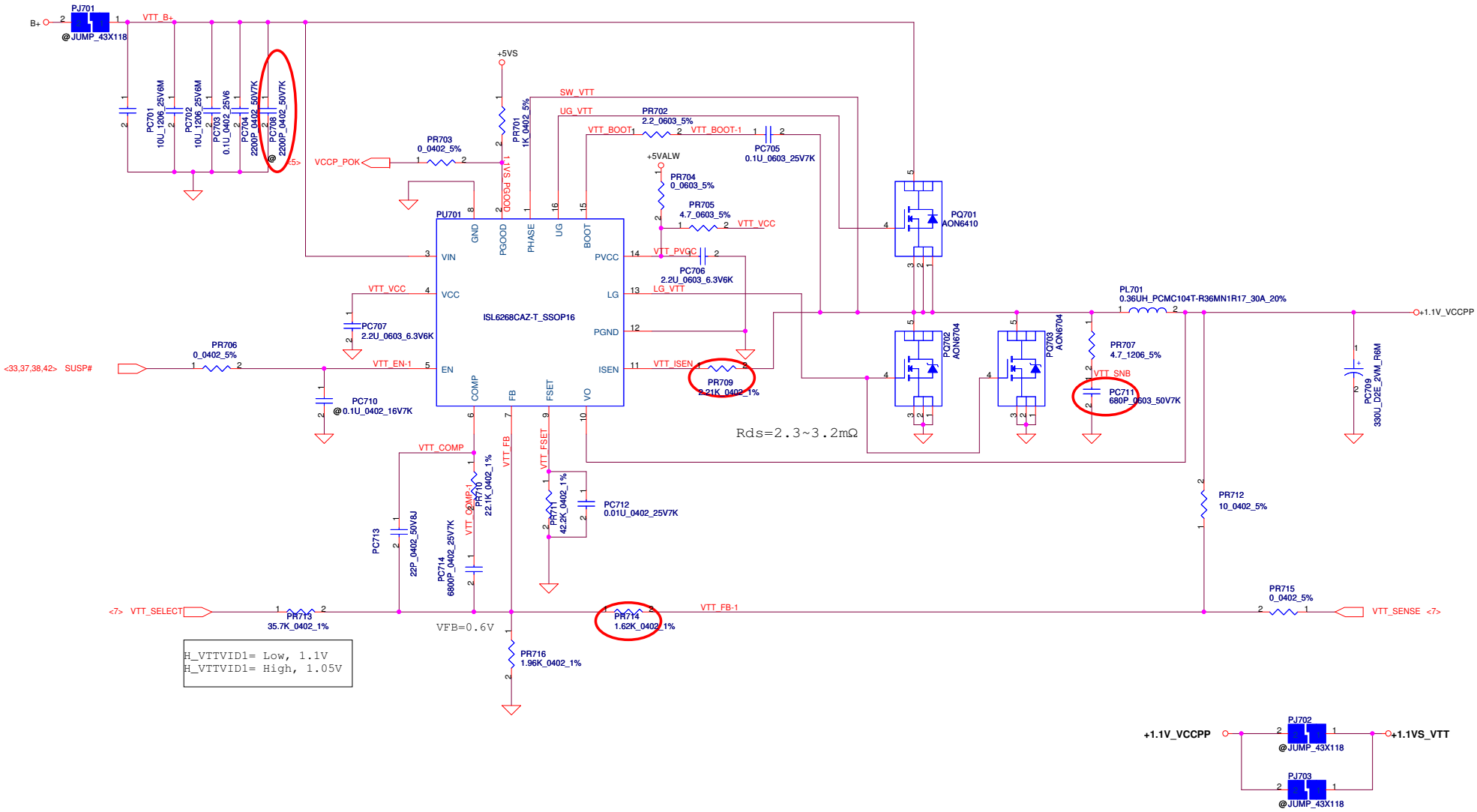
Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: 1.5V/0.75V/1.8V

Size	Document Number	Rev
		0.1

Date: Tuesday, March 09, 2010 | Sheet 44 of 48



Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/01/06

Compal Electronics, Inc.

Title: +1.1VS_VTT

Size	Document Number	Rev
Custom		0.1

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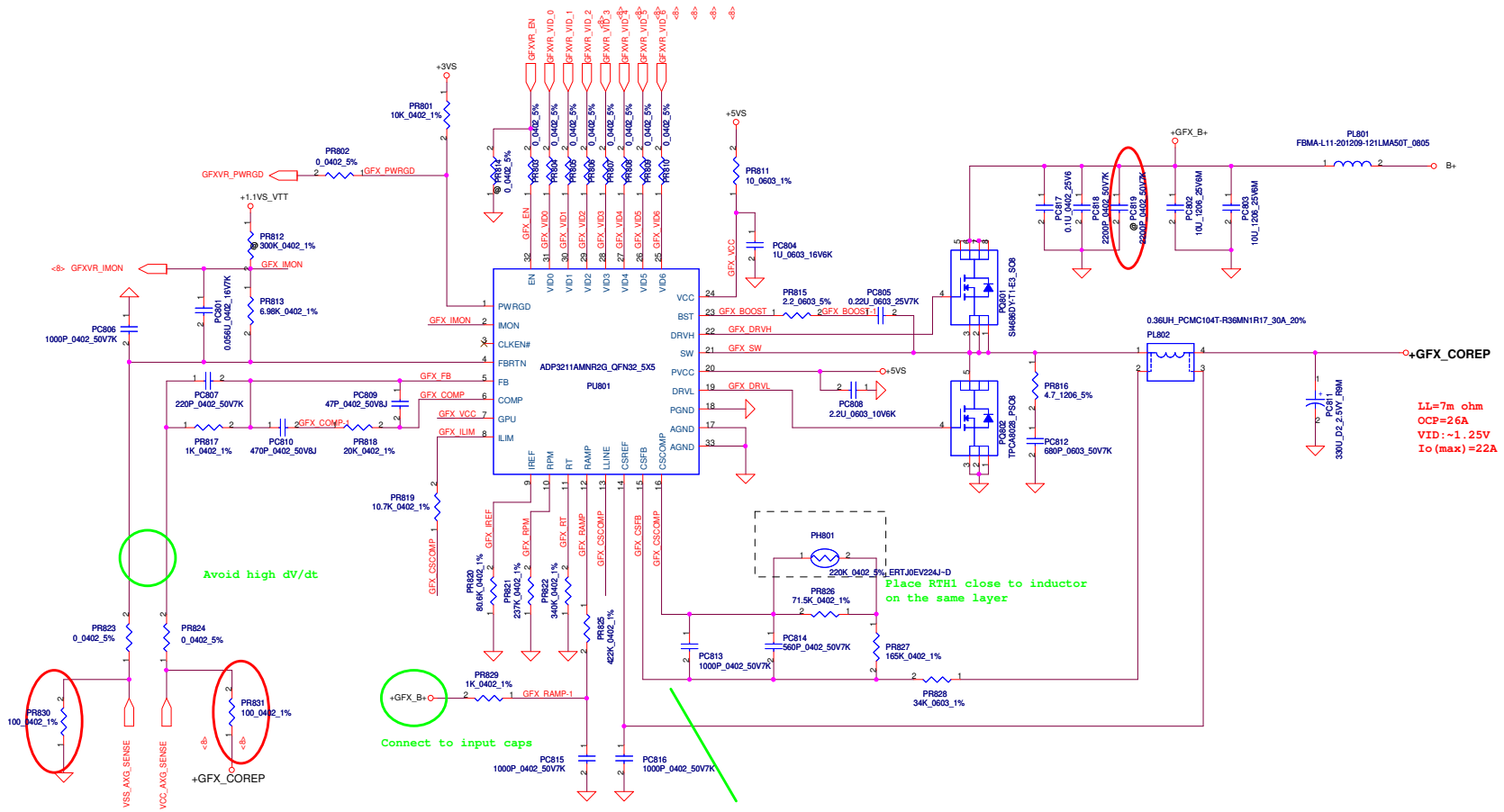
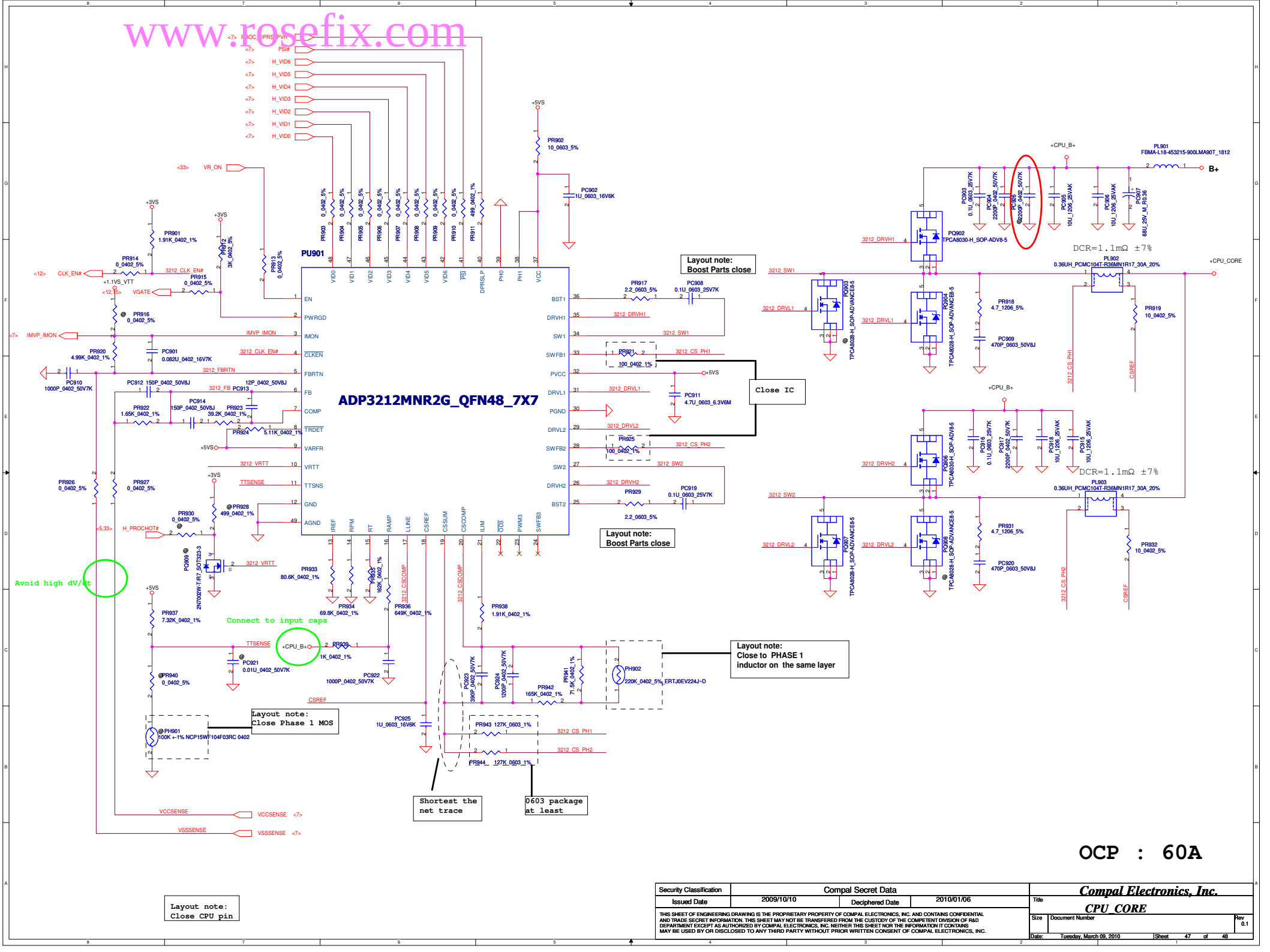
change name



Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/01/06

Compal Electronics, Inc.			
Title	GFX_CORE		
Size	Document Number		Rev 0.1
Date: Tuesday, March 09, 2010	Sheet 46 of 48		



Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2010/01/06

Compal Electronics, Inc.			
Title	CPU_CORE		
Size	Document Number		Rev 0.1
Date: Tuesday, March 09, 2010	Sheet 47 of 48		

Version change list (P.I.R. List)

for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	For ESD	P41	Add PD202	2009.11.5	EVT
2	For HW request remove +1.05V's JUMP	P41	Remove +1.05V's JUMP	2009.11.6	EVT
3	Because limited high is not enough.	P47	Change PC907 from 220uF to 68uF	2009.11.6	EVT
4	Add PR830,PR831 for GFX_CORE sence.	P46	Add PR830,PR831 for GFX_CORE sence.	2009.11.17	EVT
5	Change Battery connent footprint.	P41	Change Battery connent footprint.	2009.11.17	EVT
6	Change PR521 from 0ohm to 150Kohm. Add PC528 on BOM.	P44	HW request	2009.11.25	EVT
7	Add PD501.	P44	HW request	2009.12.16	DVT
8	Reserve Cap. on B+ for RF.		RF request	2010.1.15	PVT
9	Change PR204 from 21.5Kohm to 20Kohm. Change PR206 from 9.76Kohm to 8.87Kohm.	P41	Thermal team request to change OTP temp. change from 92 degree to 95 degree.	2010.1.22	PVT
10					
11					
12					
13					
14					
15					
16					
17				20081022	

Security Classification	Compal Secret Data		
Issued Date	2009/10/10	Deciphered Date	2009/01/06

Compal Electronics, Inc.

Title: PIR (PWR)

Size	Document Number	Rev
Custom	NAU00 M/B LA-6101P Schematics	0.1

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