DV14 CP UMA+DIS Schematics Document

Arrandale

Intel Ibex Peak-M

2011-03-18

REV : X01

DY : Nopop Component

UMA: POP for UMA option
DIS: POP for DIS option

65 BOM : Nopop for 65 BOM option

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Cover Page	
Size: A3	Document Number: DV14 CP UMA+DIS	Rev: X00
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DV14 CP Block Diagram
(UMA/DIS Co-layout)

PCB LAYER
L1: Top
L2: GND
L3: Signal
L4: Signal
L5 VCC
L6: Bottom

Project code : 91.4IU01.001
PCB P/N : 48.4IU03.0SB
Revision : 10272-SB

Clock Generator
SLG8SP595 7

VRAM gDDR3 900NHz
1GB (128x16x4)
512MB (64x16x4) 88,89

gDDR3 900MHz

AMD
Seymou PRO S3
83,84,85,86,87

100MHz/ 2.5Gbps
PCIe x 8
Bandwidth :8GB

Intel CPU
Arrandale
8,9,10,11,12,13,14

DDRIII 800/1066 Channel A
DDRIII 800/1066 Channel B

DDRIII 800/1066 Slot 0 18
DDRIII 800/1066 Slot 1 19

FDIx4 (UMA) 2.7GT/s
DMI 2.5GT/s

CRT 55
LCD 54
HDMI 57

CRT
LVDS
HDMI

Level shift 57
1.65Gbps
HDMI

SD/MMC/MS/ MS Pro 74

CardReader
Realtek RTS5138 32
USB2.0

Internal Analog MIC2 58

Azalia CODEC
IDT 92HD87 29
AZALIA 24MHz

Audio board
HP1
MIC IN
76
2CH SPEAKER
58

Intel PCH
14 USB 2.0/1.1 ports
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
PCI/PCI BRIDGE
20,21,22,23,24,25,26,27,28

SATA
SATA 3Gbps
SPI

HDD 56
ODD 56
Flash ROM 4MB 62

PCIE x 1
10/100 /1000 LOM
Realtek RTL8111E 31
RJ45 CONN 59

PCIE x 1
802.11a/b/g
Mini-Card WLAN+BT3.0 64

PCIE
100MHz
2.5Gbps

USB 2.0 x 1
CAMERA 54

USB 2.0
480Mbps

USB 2.0 x 1
M/B USB x1 (Left) 63

USB 2.0 x 2
I/O board USB x2 (Right) 76

LPC Bus
33MHz

KBC
NUVOTON
NPCE781BA0DX 37

SPI
Flash ROM 256kB 62

PS/2
Touch PAD 68

PS/2
Int. KB 68

Thermal
ENE P2800 39

ENE P2793 Fan 60

CPU DC/DC
ISL62882 47,48

INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC
RT8237AGQW 49

INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT

SYSTEM DC/DC
TPS51123RGER 46

INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW2 +3.3V_RTC_LDO +5V_ALW +3.3V_ALW +15V_ALW

SYSTEM DC/DC
RT8207LGQW 50

INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF

SYSTEM DC/DC
G9731F11U 93

INPUTS	OUTPUTS
+1.5V_SUS	+1V_GPU_PCIE

VGA
RT8208BGQW 92

INPUTS	OUTPUTS
+PWR_SRC	+VCC_GFX_CORE

MAXIM CHARGER
BQ24707RGRRG4 45

INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC

SYSTEM DC/DC
RT9025-25PSP 51

INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN

SYSTEM DC/DC
RT9025-25PSP 93

INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN_GPU

SYSTEM DC/DC
Switches 42

INPUTS	OUTPUTS
+1.5V_SUS +5V_ALW +3.3V_ALW	+1.5V_RUN +5V_RUN +3.3V_RUN

<Core Design>

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Title: Block Diagram

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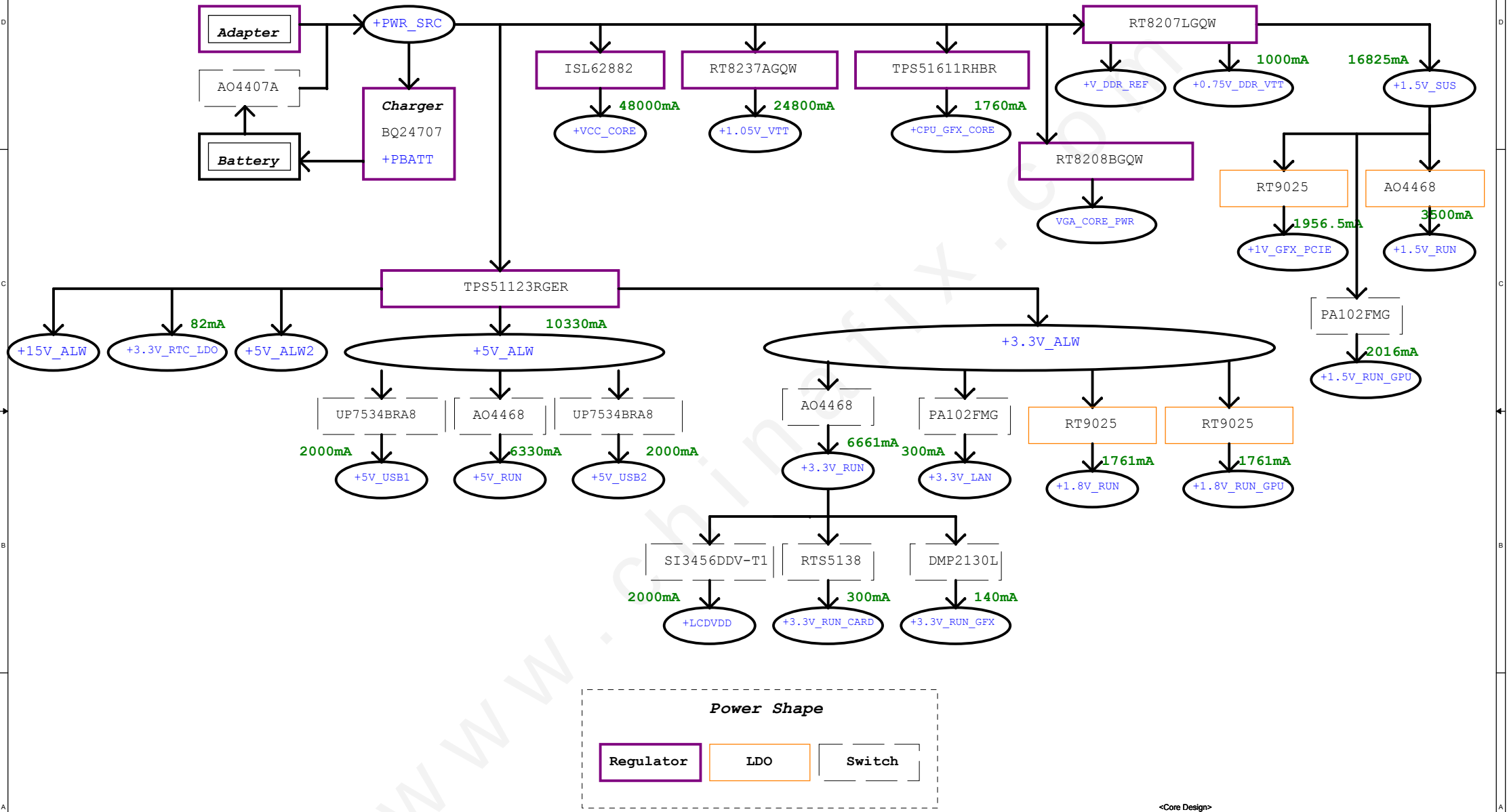

<Core Design>

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Title: Power Block Diagram

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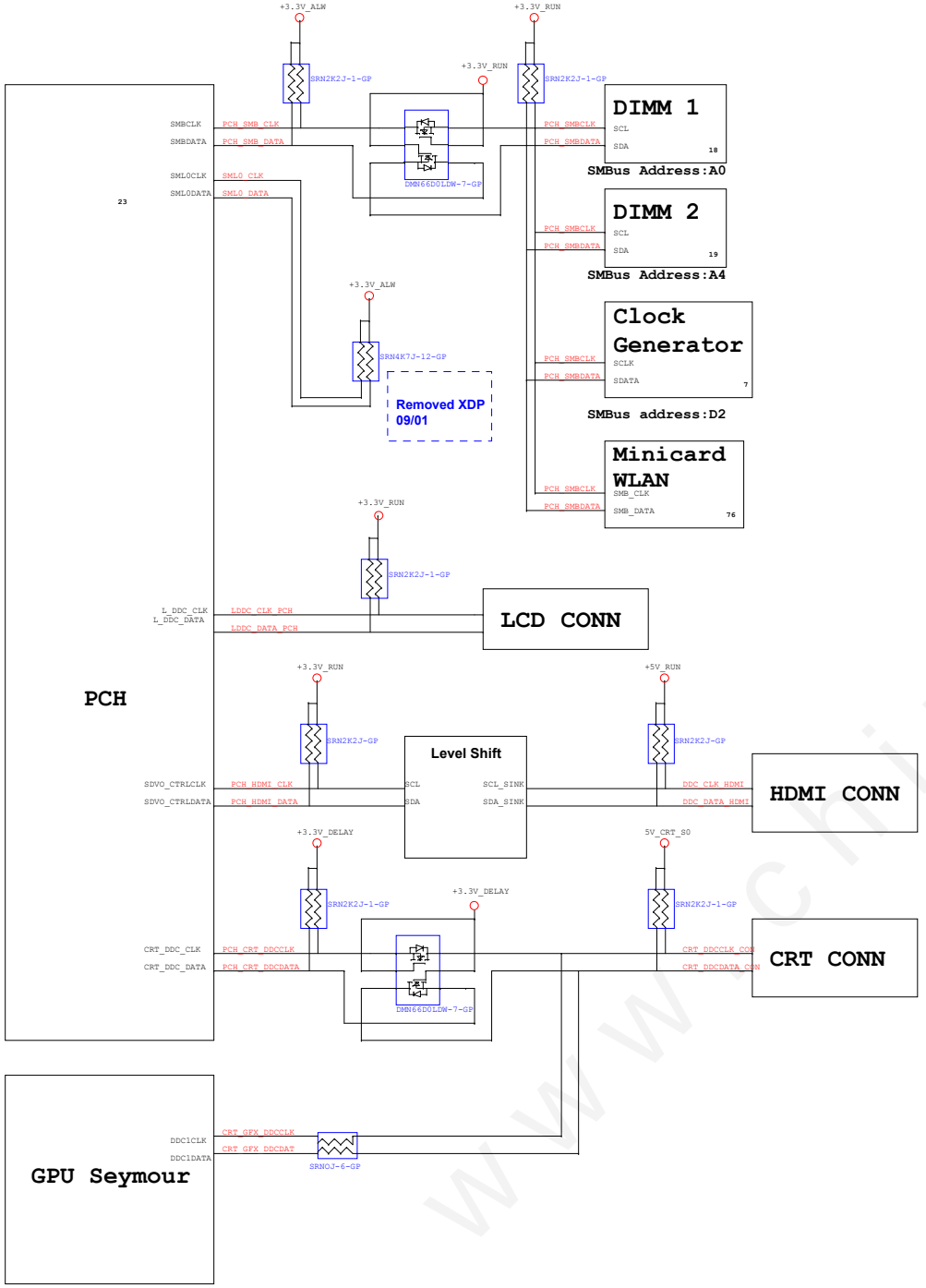
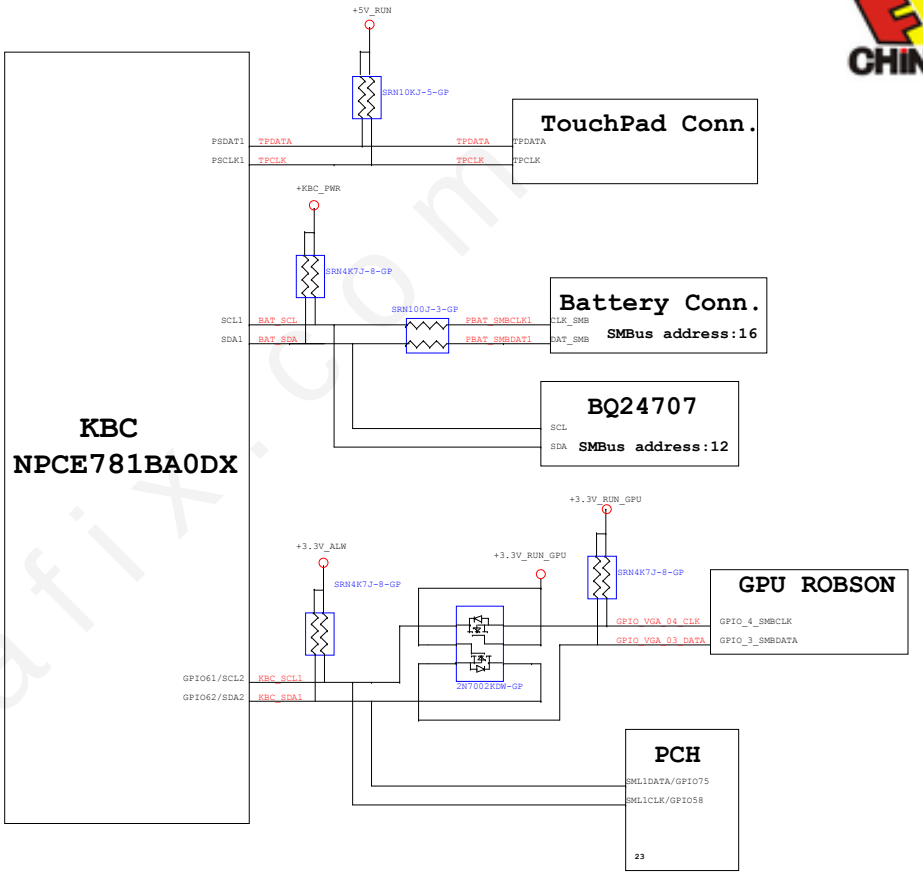
PCH SMBus Block Diagram



KBC SMBus Block Diagram



<Core Design>
Wistron Corporation
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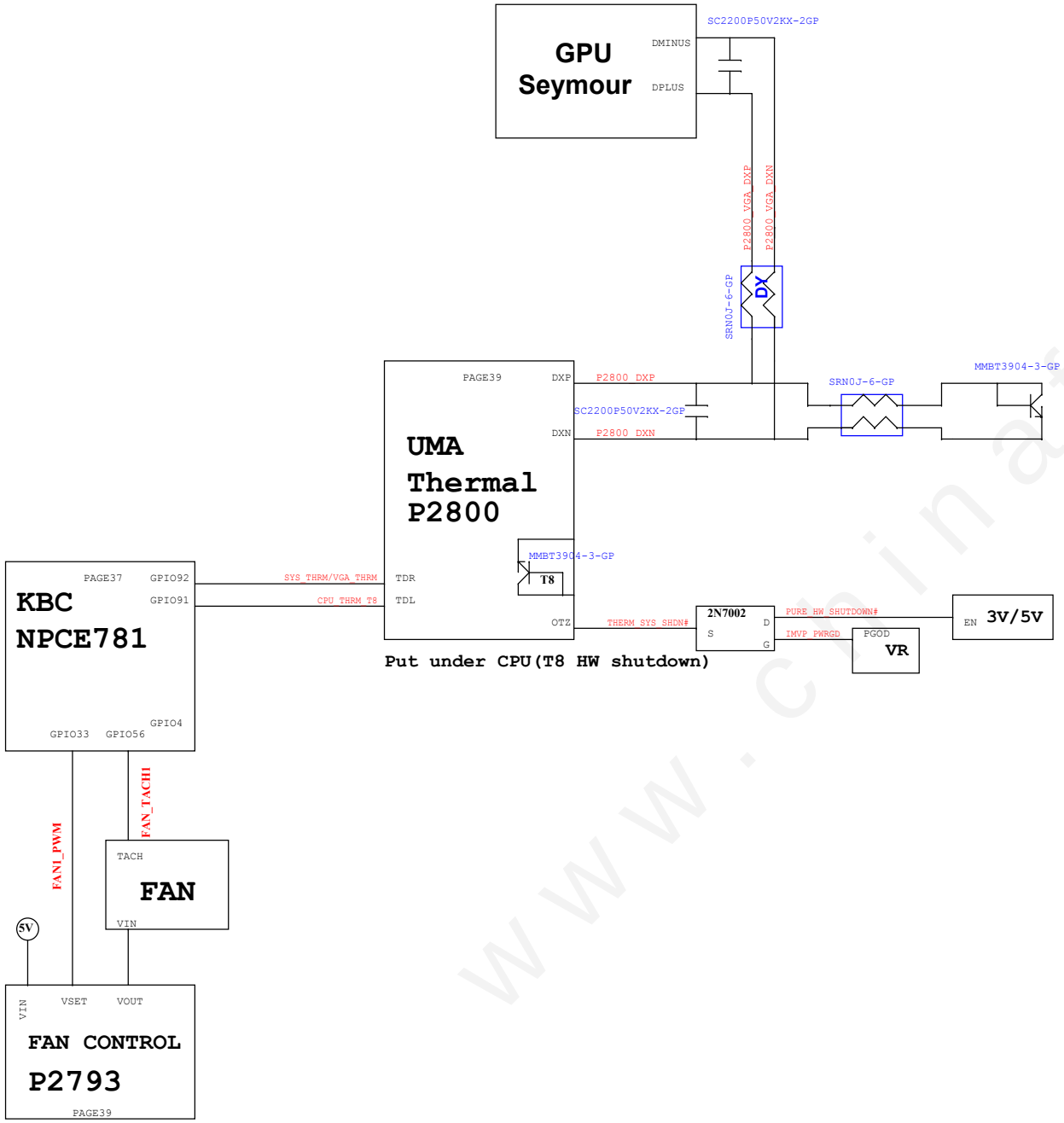
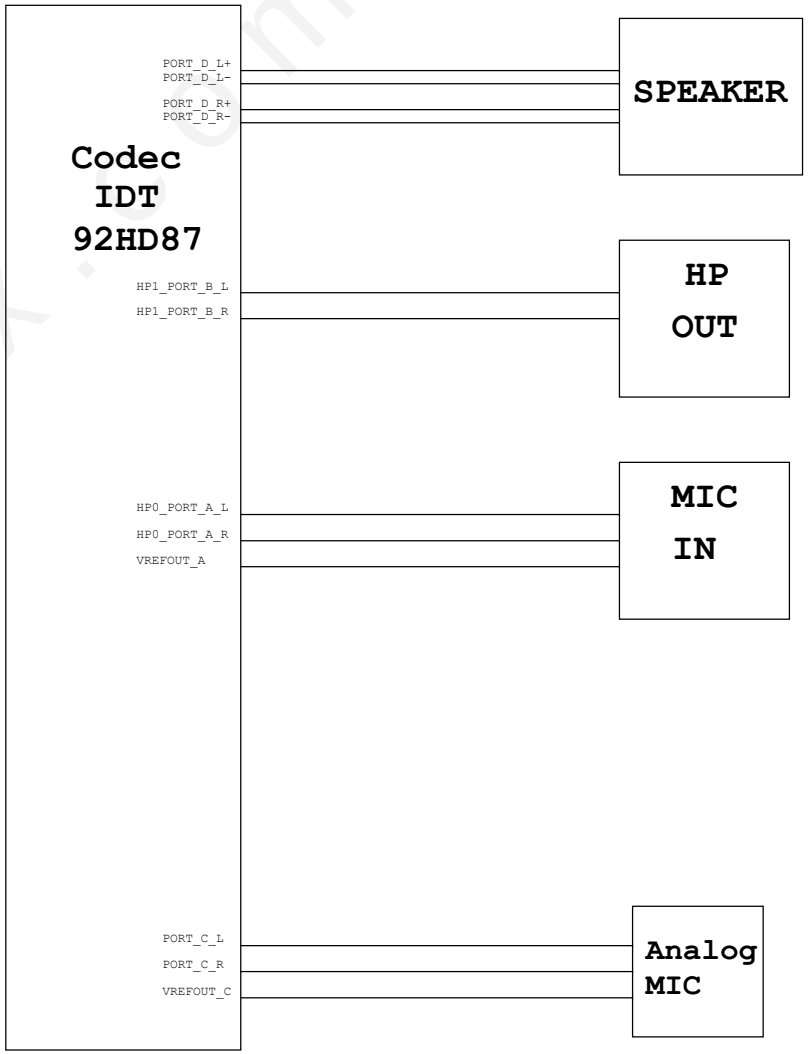
Title: SMBUS Block Diagram
Size: A2 | Document Number: DV14 CP UMA+DIS | Rev: X00
Date: Wednesday, March 09, 2011 | Sheet 4 of 100

Thermal Block Diagram



Audio Block Diagram



<Core Design>

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Title: Thermal/Audio Block Diagram

Size	Document Number	Rev
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Date: Thursday, January 06, 2011 Sheet 5 of 100

PCH Strapping

Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-k - 10-k weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-k weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#/GPIO51	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-k pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-k pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-k pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-k weak pull-up **Disable iTPM:** Signal has internal pull-up, left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-k weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

PCIE Routing

LANE2	MiniCard WLAN
LANE3	LAN

USB Table

USB	
Pair	Device
0	X
1	USB1
2	USB2
3	USB3
4	X
5	X
6	X
7	X
8	X
9	WLAN for BLUETOOTH
10	CARD READER
11	CAMERA
12	X
13	X

<Core Design>

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Title: Table of Content

Size	Document Number	Rev
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SSID = CLOCK

X01

X00 0106 Remove C705 C707 C708

BOM merge 10/05

X00-1126

Note: 595 stuff R718, 585 stuff R719

BOM merge 10/04

BOM merge 10/05

X00 09/23

X00 9/27

X01 0316
if U701 is 71.08595.003,R706 install 33ohm (63.33034.1DL);
if U701 is 2nd=71.93197.B03,R706 install 22ohm(63.22034.1DL).

71.08595.003
2nd = 71.93197.B03

1st Silego :71.08595.003
2nd IDT :71.93197.B03

82.30005.901
2nd = 82.30005.A51
3rd = 82.30005.B81

X01 0315

FSC	0	1
SPEED	133MHz (Default)	100MHz

X01 0310

84.03904.L06
2nd = 84.03904.P11

<Core Design>

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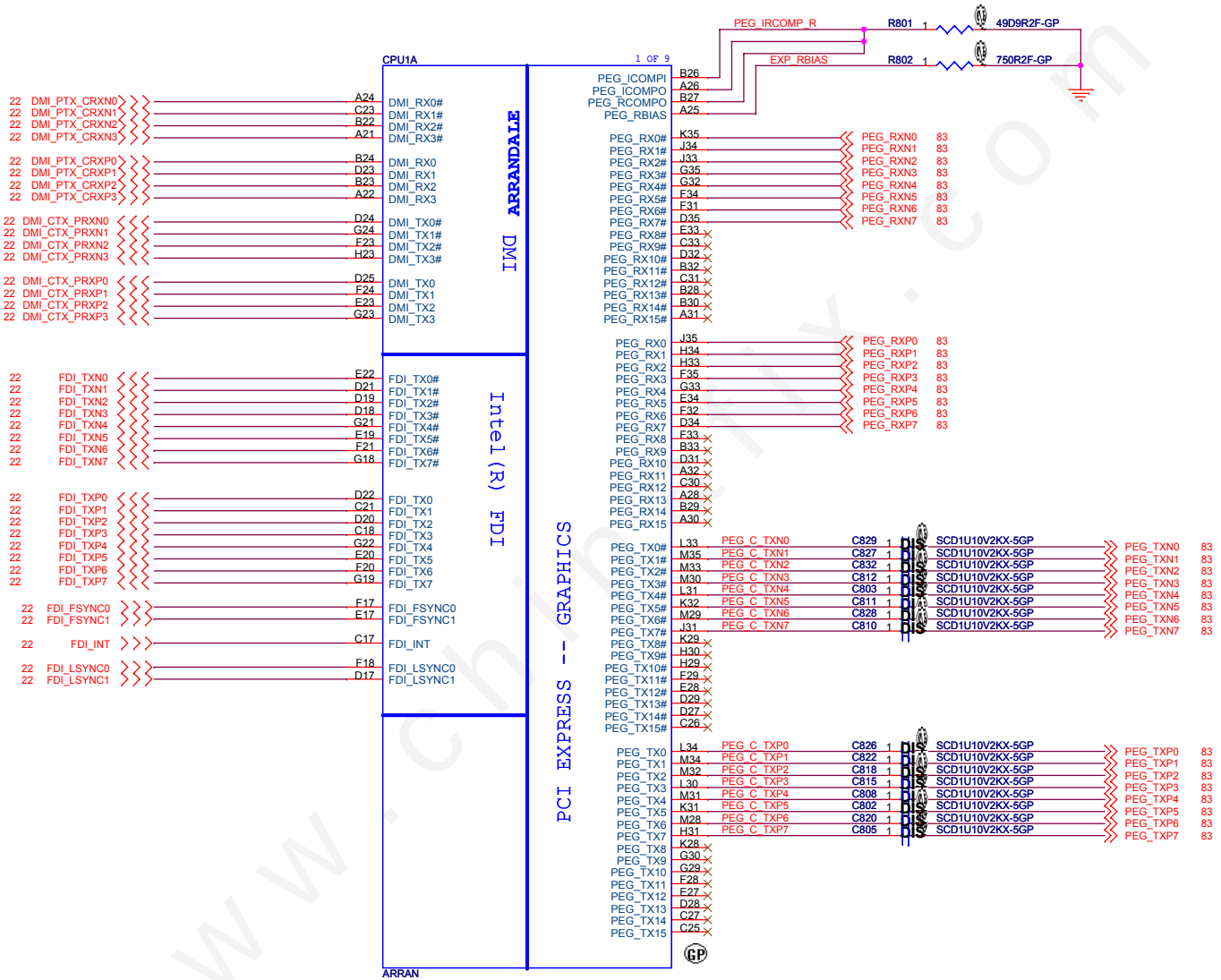
Title: Clock Generator SLG8SP585

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 7 of 100

SSID = CPU



62.10055.321

2nd = 62.10040.821

3rd = 62.10055.551

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/DMI/FDI)

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

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SSID = CPU

Processor Pullups

+1.05V_VTT

R902 1 49D9R2F-GP H_CATERR#

R933 1 68R2-GP H_PROCHOT#

R904 1 DY 68R2-GP H_CPURST#

Processor Compensation Signals

R901 1 20R2F-GP H_COMP3

R903 1 20R2F-GP H_COMP2

R905 1 49D9R2F-GP H_COMP1

R906 1 49D9R2F-GP H_COMP0

CPU1B 2 OF 9

H_COMP3 AT23 COMP3

H_COMP2 AT24 COMP2

H_COMP1 G16 COMP1

H_COMP0 AT26 COMP0

AH24 SKTOCC#

H_CATERR# AK14 CATERR#

25 H_PECI AT15 PECI

45,47 H_PROCHOT# AN26 PROCHOT#

25,42,85 H_THERMTRIP# AK15 THERMTRIP#

H_CPURST# AP26 RESET_OBS#

22 H_PM_SYNC AL15 PM_SYNC

AN14 VCCPWRGOOD_1

25,42 H_PWRGD VCCPWRGOOD AN27 VCCPWRGOOD_0

22 PM_DRAM_PWRGD VDDPWRGOOD_R AK13 SM_DRAMPWROK

49 H_VTTPWRGD AM15 VTTPWRGOOD

AM26 TAPPWRGOOD

21,31,37,64,70,83 PLT_RST# PLT_RST# R AL14 RSTIN#

ARRANDALE

MISC

THERMAL

PWR MANAGEMENT

ARRAN

X00 R908 1 2 0R0402-PAD-2-GP

R912 2 0R0402-PAD-2-GP X00

R913 1K6R2F-GP

R915 750R2F-GP

CLOCKS

BCLK A16 BCLK_CPU_P_R

BCLK# B16 BCLK_CPU_N_R

BCLK_ITP AR30

BCLK_ITP# AT30

PEG_CLK E16 PEG_CLK_R

PEG_CLK# D16 PEG_CLK# R

DPLL_REF_SSCLK A18

DPLL_REF_SSCLK# A17

X01 R916 1 2 0R0402-PAD-2-GP

R917 1 2 0R0402-PAD-2-GP

R918 1 2 0R0402-PAD-2-GP

R920 0R0402-PAD-2-GP X01

BCLK_CPU_P 25

BCLK_CPU_N 25

CLK_EXP_P 23

CLK_EXP_N 23

DDR3 MISC

SM_DRAMRST# F6 SM_DRAMRST#

SM_RCOMP0 AL1 SM_RCOMP_0

SM_RCOMP1 AM1 SM_RCOMP_1

SM_RCOMP2 AN1 SM_RCOMP_2

PM_EXT_TS0# AN15 PM_EXTTS#0_C

PM_EXT_TS1# AP15 PM_EXTTS#1_C

PM_EXTTS#0_C 53

SRN10KJ-5-GP RN905

RN906 DY SRN0J-6-GP X00

PM_EXTTS#0 18

PM_EXTTS#1 19

JTAG & BPM

PRDY# AT28

PREQ# AP27

TCK AN28

TMS AP28

TRST# AT27 XDP_TRST#

TDI AT29

TDO AR27 XDP_TDO_R

TDI_M AR29 XDP_TDI_M

TDO_M AP29 XDP_TDO_M

R914 1 2 0R0402-PAD-2-GP

DBR# AN25 H_DBR#_R

R909 0R2J-2-GP XDP_DBRESET#

XDP_DBRESET# 22

BPM0# AJ22

BPM1# AK22

BPM2# AK24

BPM3# AJ24

BPM4# AJ25

BPM5# AH22

BPM6# AK23

BPM7# AH23

GP

DDR3 Compensation Signals

SM_RCOMP_0 R907 1 100R2F-L1-GP-U

SM_RCOMP_1 R910 1 24D9R2F-L-GP

SM_RCOMP_2 R911 1 130R2F-1-GP

Clock Generator

+3.3V_RUN

U927

B VCC 5

A Y 4 VTT_PWRGD_R3

GND 3

74LVC1G08GW-1-GP

37,49,50 VTT_PWRGD

R977 2 1 1K6R2F-GP VDDPWRGOOD_R

+1.5V_RUN

DY R919 1K27R2F-L-GP

R937 750R2F-GP

73.01G08.L04

2nd = 73.7SZ08.DAH

Misc

+1.05V_VTT

RN902 1 4 XDP_TDO_R

XDP_TRST# 2 3

SRN51J-GP

+1.5V_RUN

R936 DY 1KR2J-1-GP

SM_DRAMRST#

R988 100KR2J-1-GP

DDR_RST_GATE 25

C915 SCD047U25V2KX-GP

+1.5V_SUS

R934 1KR2J-1-GP

DDR3_DRAMRST# 18,19

Q901 G D S 2N7002K-2-GP

C903 SCD1U10V2KX-5GP

84.2N702.J31

2nd = 84.2N702.031

R935 DY 0R2J-2-GP

Modified 10/7

BOM merge Change 09/09

	R919	R937	R977
S3 circuit	DY	0.75k	1.6k
Normal	1.27k	3k	DY

Remove XDP 8/22

1119

<Core Design>

Wistron Corporation

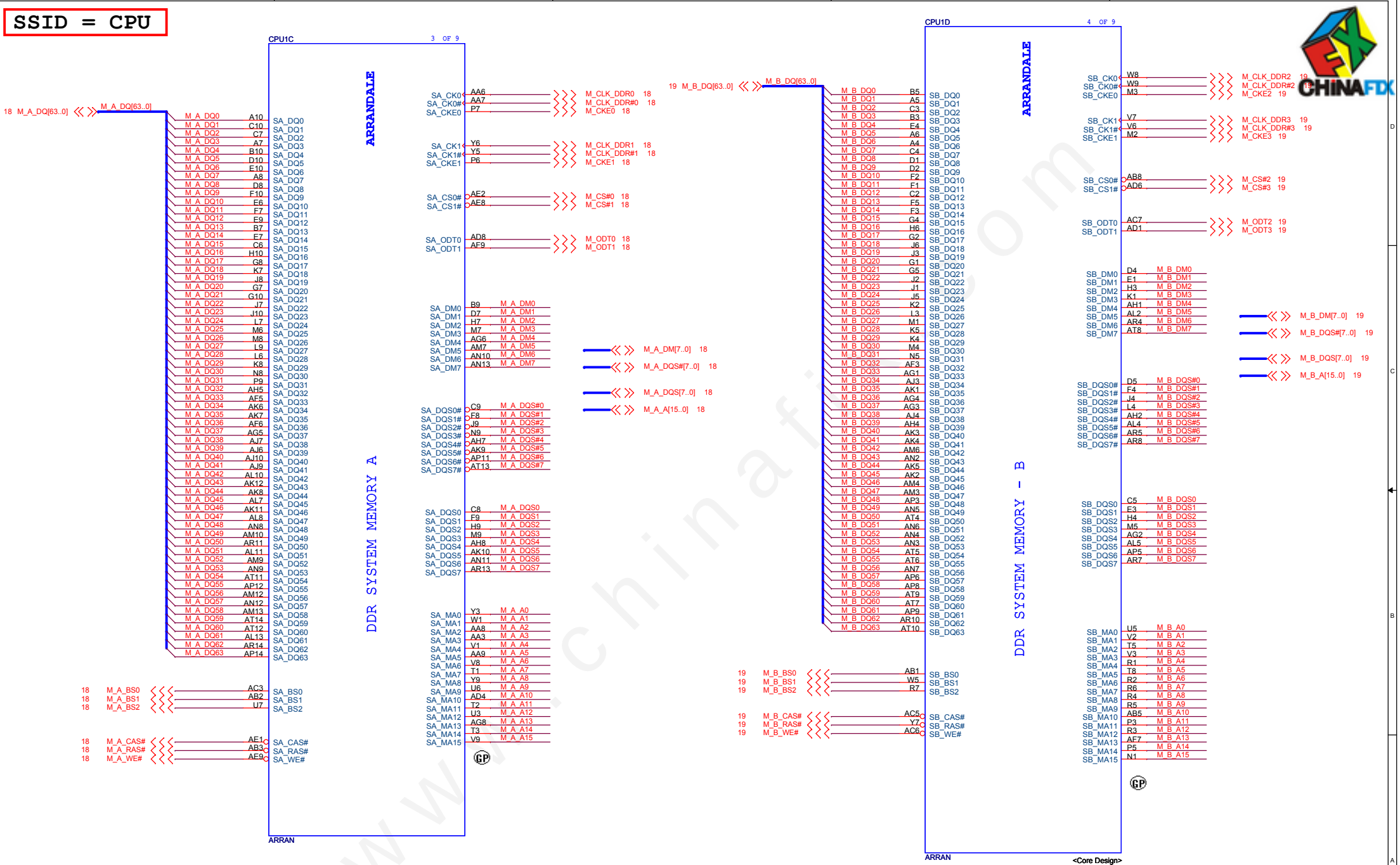
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (THERMAL/CLOCK/PM)

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

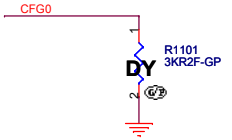
Date: Wednesday, March 23, 2011 | Sheet 9 of 100

SSID = CPU

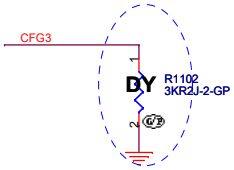


Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	CPU (DDR)	
Size: A3	Document Number: DV14 CP UMA+DIS	Rev: X00
Date: Wednesday, March 23, 2011	Sheet 10 of 100	

SSID = CPU

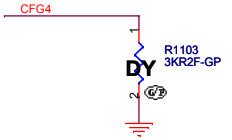


PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

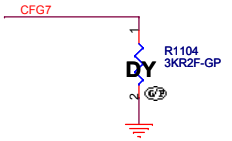


Change to Normal operation
20100202

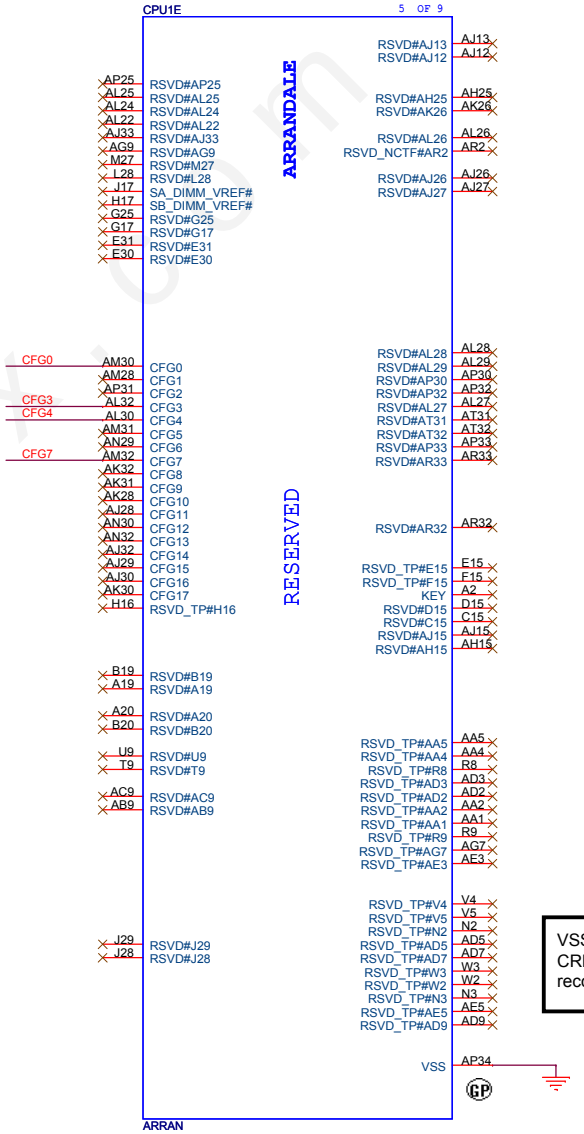
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port



CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

<Core Design>

Wistron Corporation
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Title: CPU (RESERVED)

Size	Document Number	Rev
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SSID = CPU

PROCESSOR CORE POWER

48A

+VCC_CORE

CPU1F

6 OF 9

ARRANDALE

CPU CORE SUPPLY

1.1V RAIL POWER

ARRAN

Simulation 10/07

Modified 09/09

Simulation 10/07

Merge bom 09/10

Delete 14 pcs 10U caps 9/9

The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

POWER

CPU VIDS

SENSE LINES

PSI# AN33 → PSI# 47

VID0 AK35 H_VID0
VID1 AK33 H_VID1
VID2 AK34 H_VID2
VID3 AL35 H_VID3
VID4 AL33 H_VID4
VID5 AM33 H_VID5
VID6 AM35 H_VID6
→ H_VID[6..0] 47

PROC_DPRSLPVR AM34 → PM_DPRSLPVR 47

VTT_SELECT G15 H_VTTVID1 → TP1201TPAD14-GP

H_VTTVID1 = Low, 1.1V
H_VTTVID1 = High, 1.05V

ISENSE AN35 → IMVP_IMON 47

VCC_SENSE AJ34 → VCC_SENSE 47
VSS_SENSE AJ35 → VSS_SENSE 47

VTT_SENSE B15
VSS_SENSE_VTT A15 TP_VSS_SENSE_VTT → TP1202TPAD14-GP
VTT_SENSE 49

R1201 100R2F-L1-GP-U

R1204 100R2F-L1-GP-U

<Core Design>

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_CORE)

Size: Custom | Document Number: DV14 CP UMA+DIS | Rev: X00

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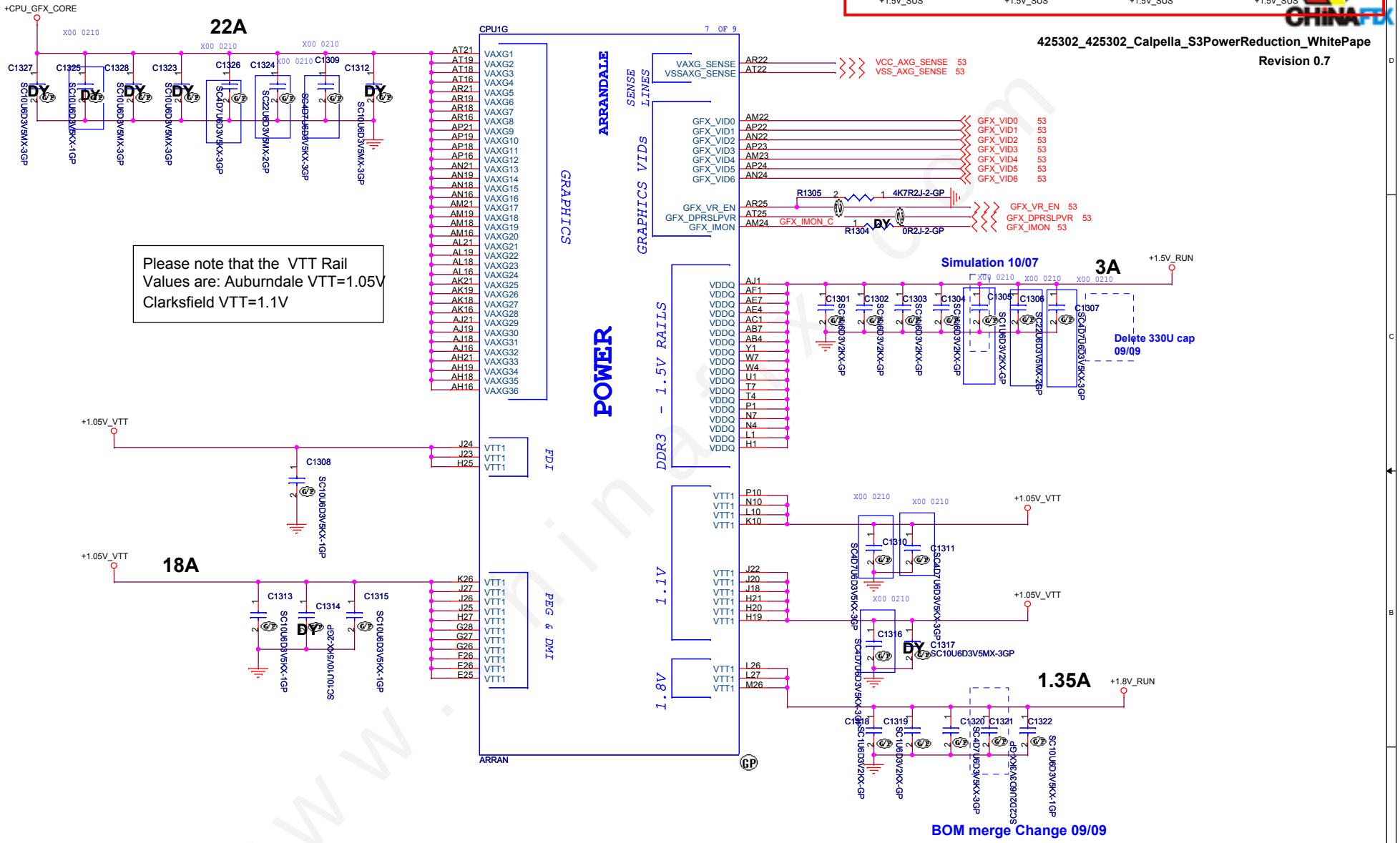
SSID = CPU



425302_425302_Calpella_S3PowerReduction_WhitePape

Revision 0.7

<Core Design>

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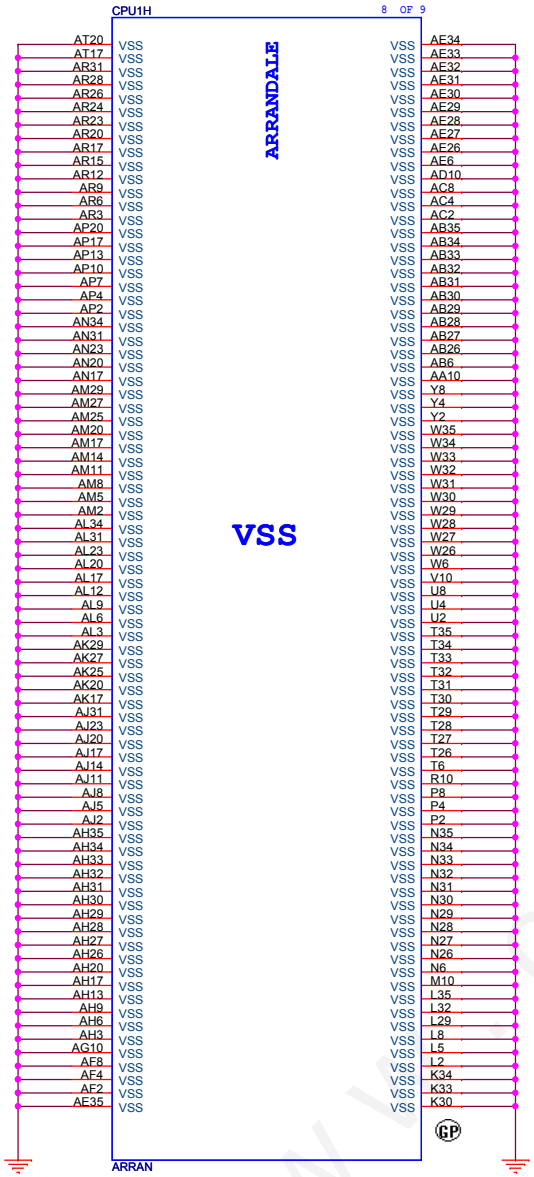
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

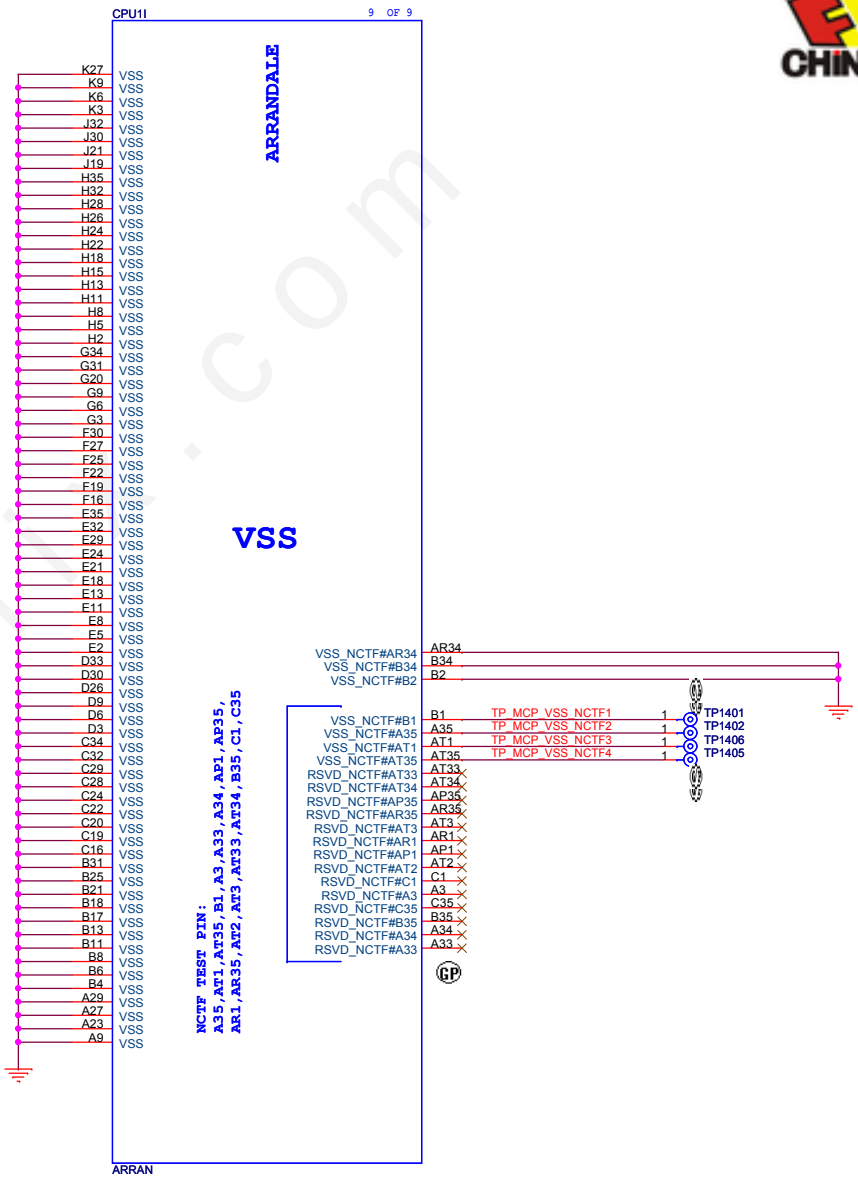
Title: CPU (VCC_GFXCORE)

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 13 of 100

SSID = CPU





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size	Document Number	Rev
A3	DV14 CP UMA+DIS	X00

Date: Monday, March 07, 2011 Sheet 14 of 100

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *DV14 CP UMA+DIS* | Rev: *X00*

Date: Thursday, January 06, 2011 | Sheet 15 of 100

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DV14 CP UMA+DIS*	*X00*

Date: Thursday, January 06, 2011 Sheet 16 of 100

(Blanking)

<Core Design>

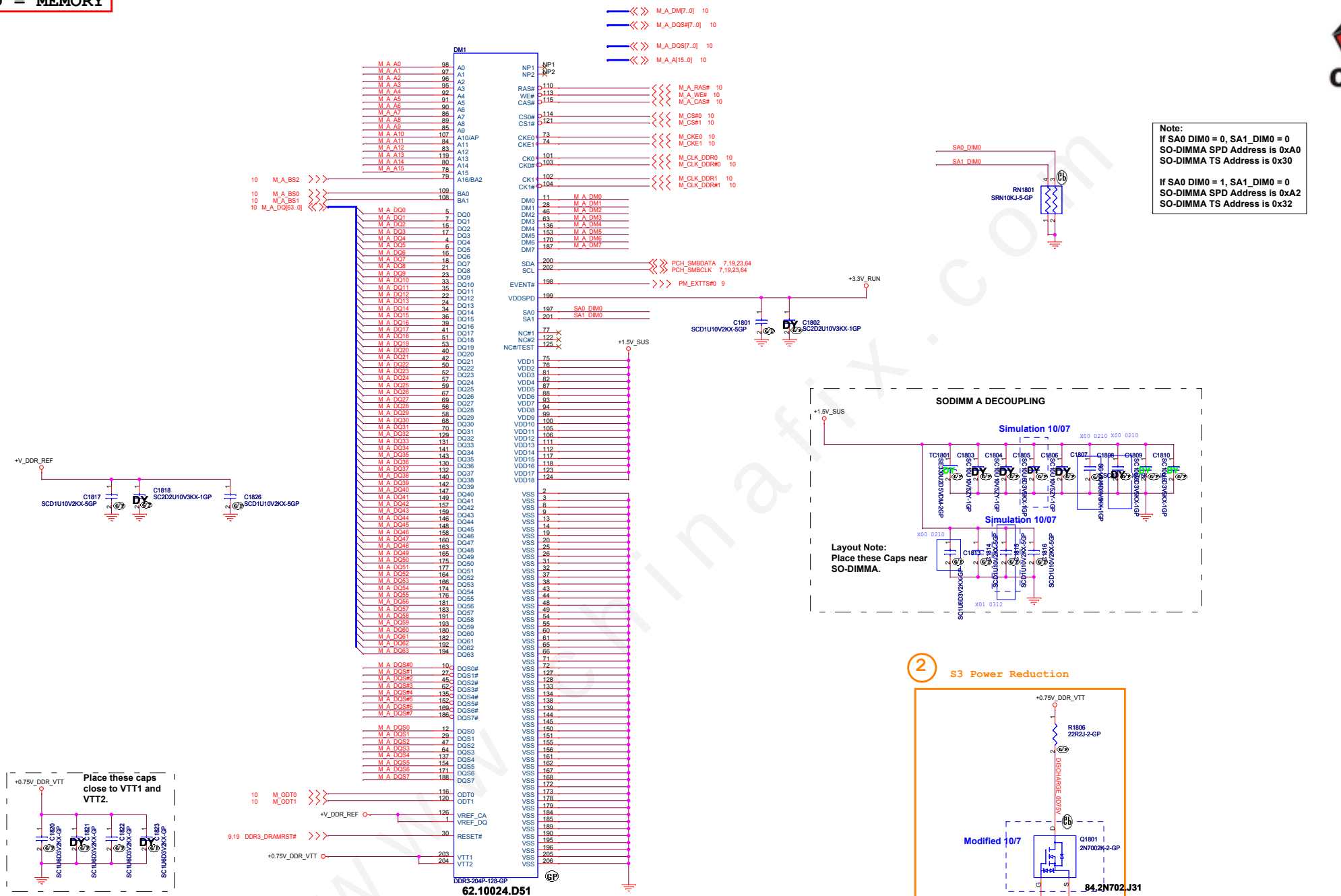
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Thursday, January 06, 2011 | Sheet 17 of 100

SSID = MEMORY



Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

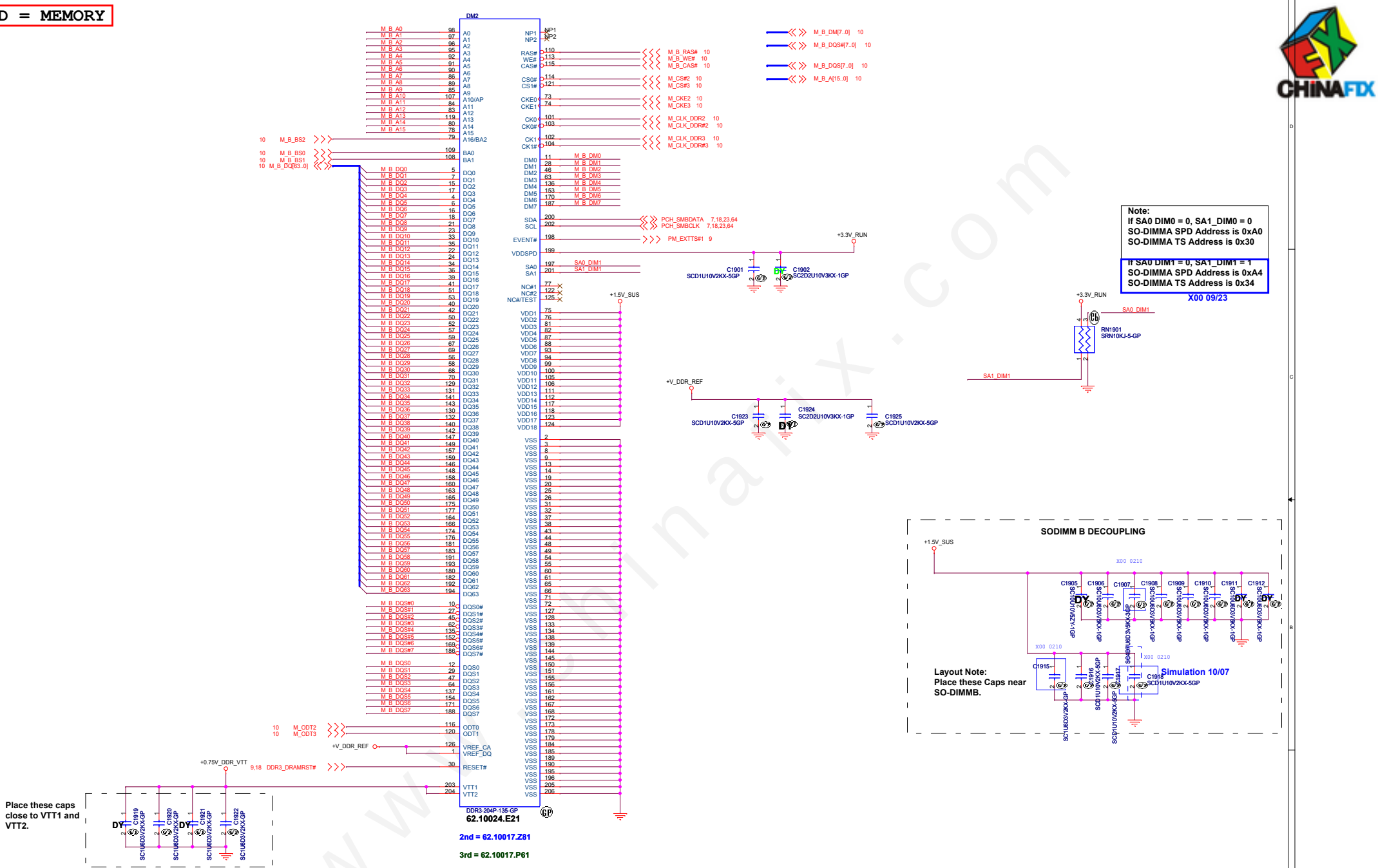
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR3-SODIMM1**

Size	Document Number	Rev
C	DV14 CP UMA+DIS	X00

Date: Wednesday, March 23, 2011 Sheet 18 of 100

SSID = MEMORY



<Core Design>

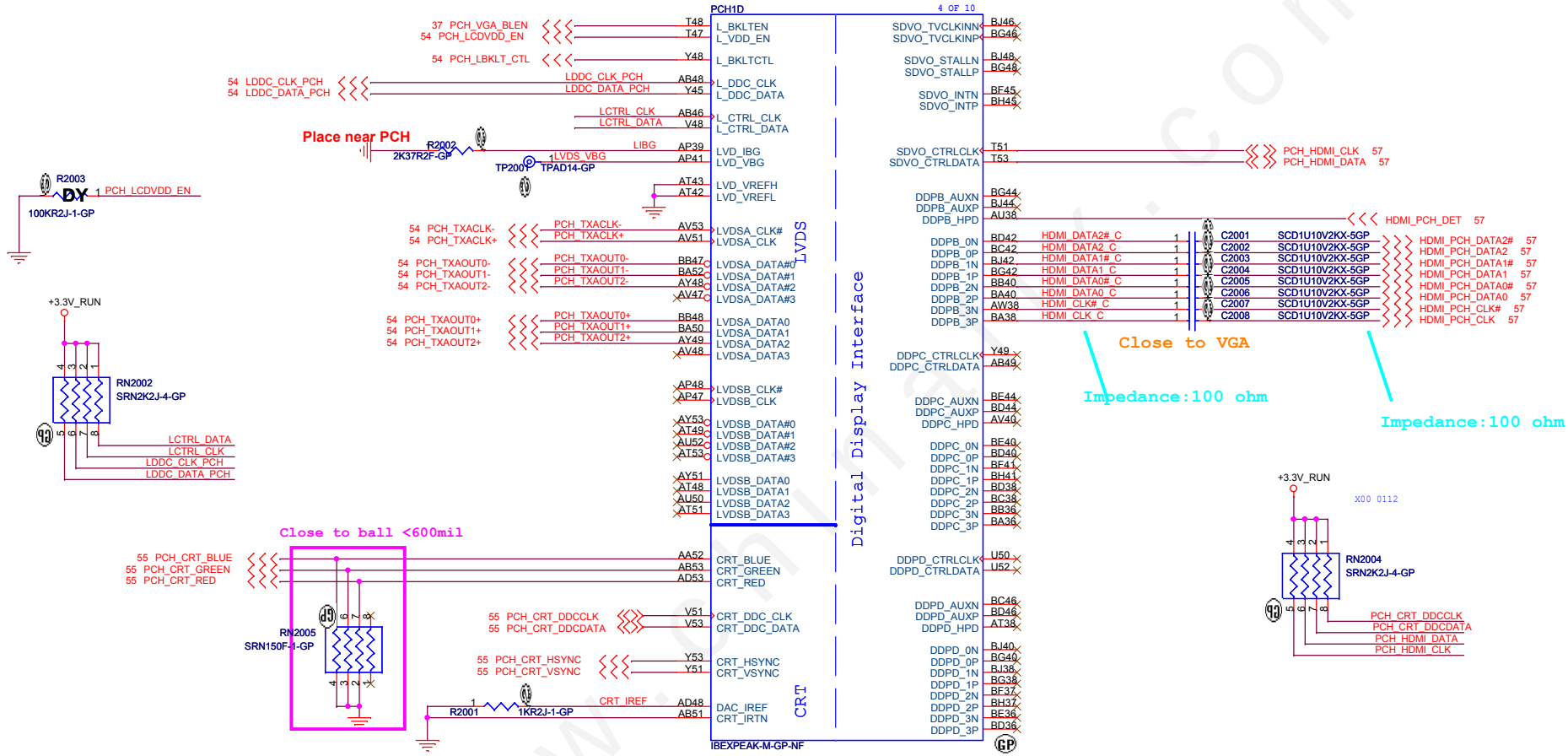
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2

Size	Document Number	Rev
	DV14 CP UMA+DIS	X00

Date: Wednesday, March 23, 2011 Sheet 19 of 100

SSID = PCH



<Core Design>

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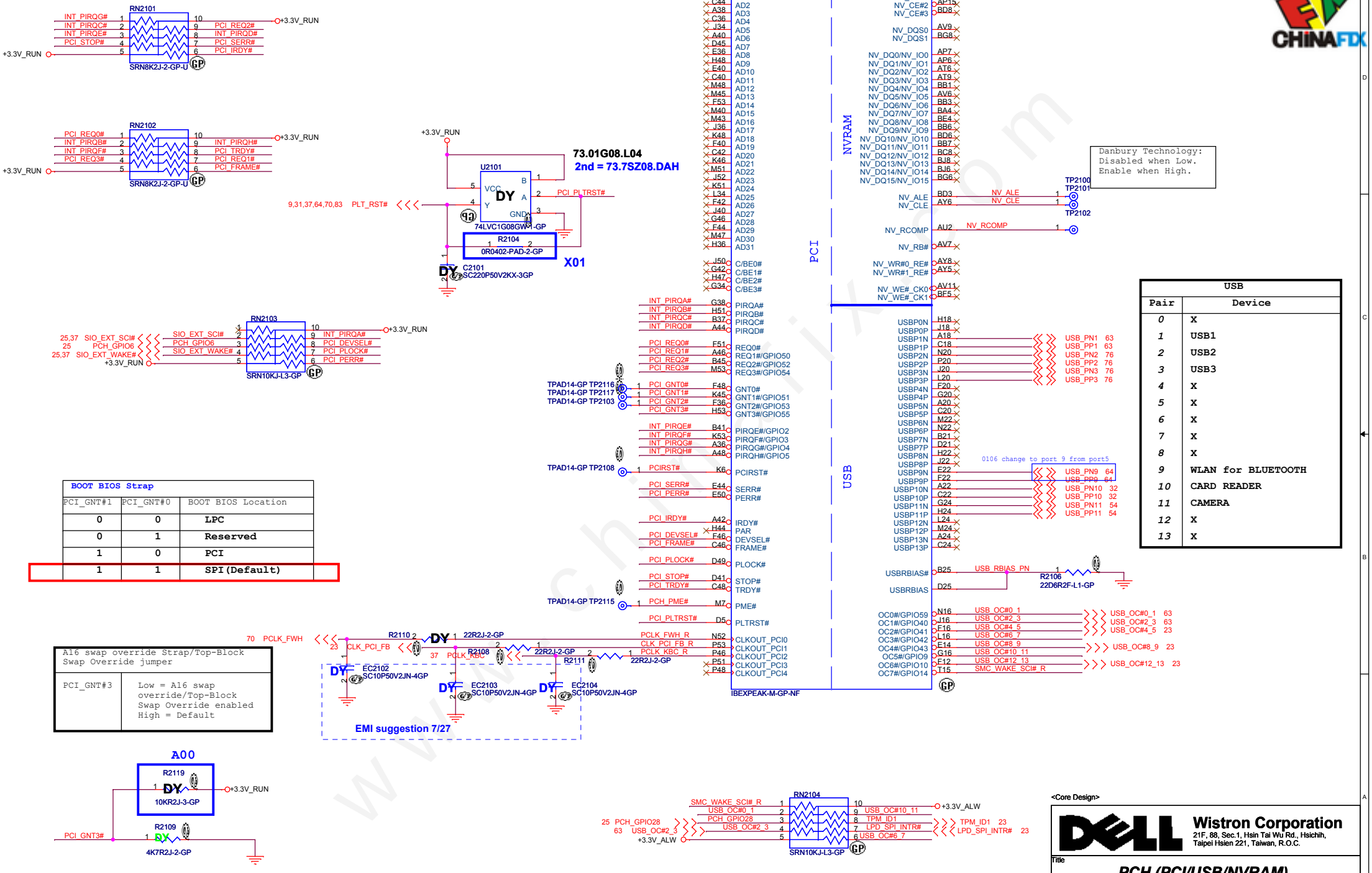
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size	Document Number	Rev
A3	DV14 CP UMA+DIS	X00

Date: Wednesday, March 23, 2011 Sheet 20 of 100

SSID = PCH



BOOT BIOS Strap		
PCI_GNT#1	PCI_GNT#0	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI (Default)

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

USB	
Pair	Device
0	X
1	USB1
2	USB2
3	USB3
4	X
5	X
6	X
7	X
8	X
9	WLAN for BLUETOOTH
10	CARD READER
11	CAMERA
12	X
13	X

<Core Design>

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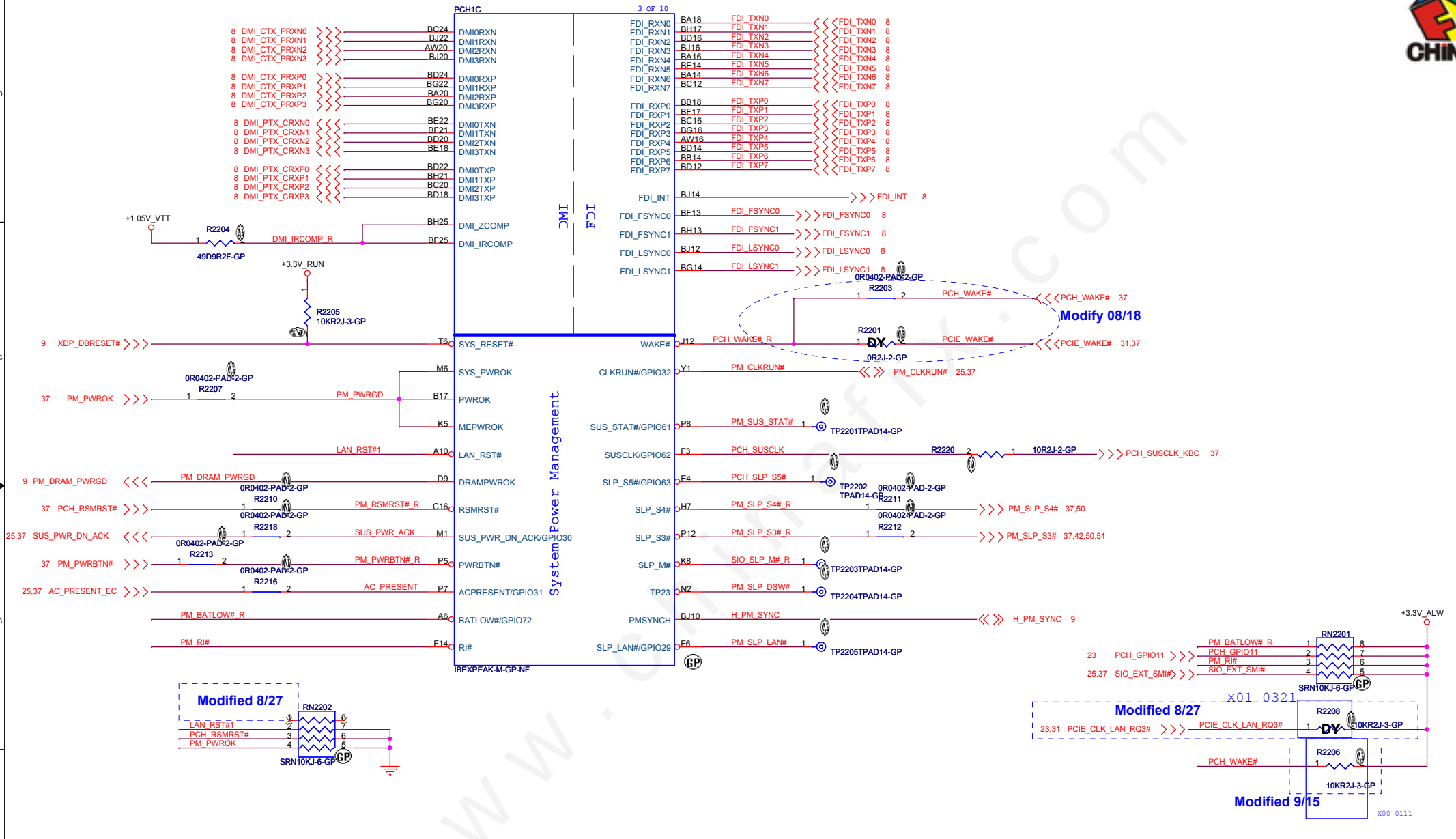
Title: PCH (PCI/USB/NVRAM)

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 21 of 100

SSID = PCH



<Core Design>

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Title	PCH (DM I/FDI/PM)	
Size A3	Document Number DV14 CP UMA+DIS	Rev X00
Date: Wednesday, March 23, 2011	Sheet 22 of 100	

SSID = PCH

PCH1B

2 OF 10

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3.3V_ALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +3.3_RUN

Add serial resistor 8/27

WLAN

LAN

X02
1118

X00 2011 0105

Add for GPU 8/10

Modified 1/5

When HDMI parts stuffed, the R2311 need DY.

X01 0228

X01 0315

82.30020.D41
2nd = 82.30020.G71
3rd = 82.30020.G61

84.2N702.A3F
2nd = 84.DM601.03F

EMI suggestion 7/27

<Core Design>

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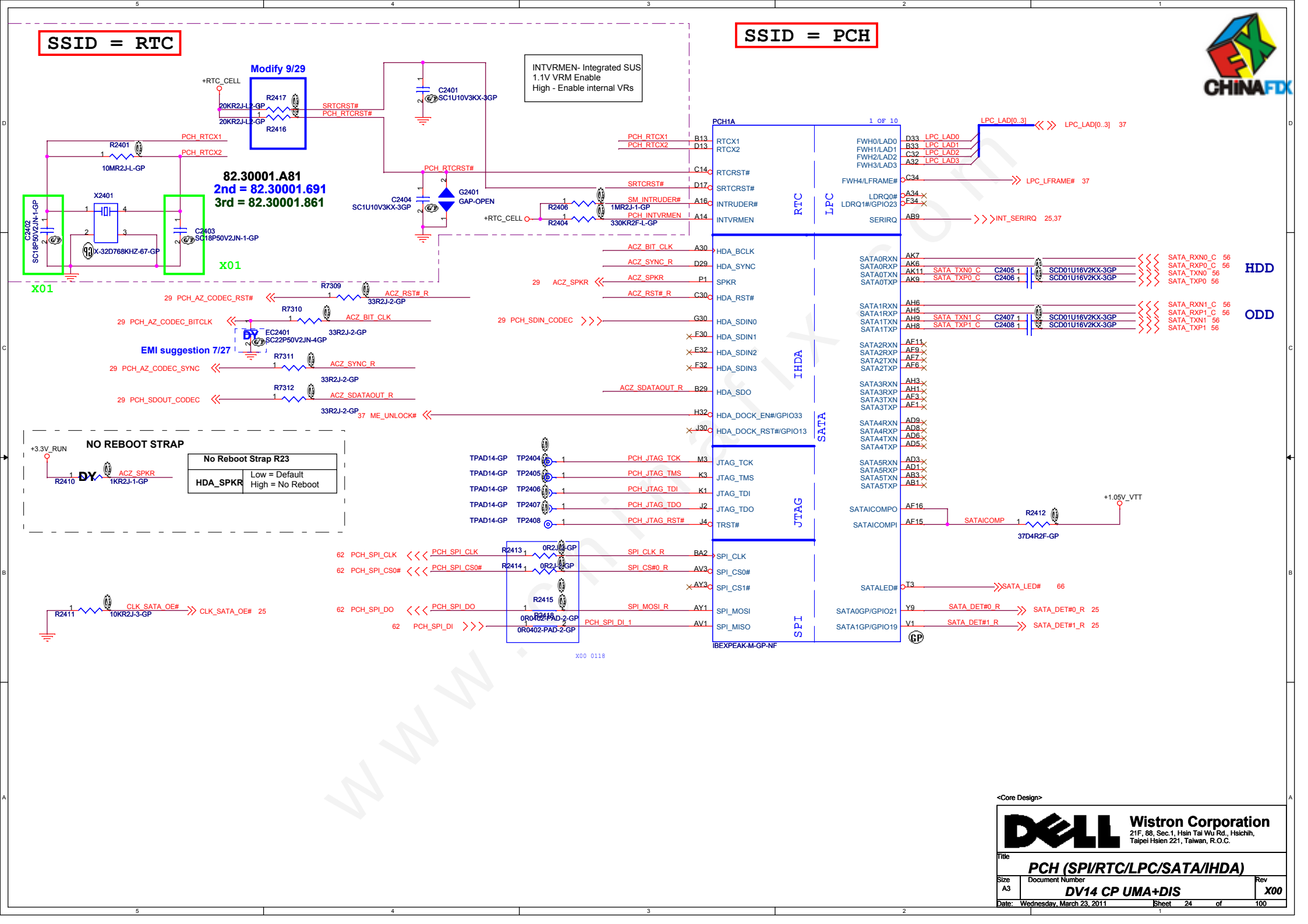
Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 23 of 100


SSID = RTC
SSID = PCH
Modify 9/29
INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs
82.30001.A81
2nd = 82.30001.691
3rd = 82.30001.861
EMI suggestion 7/27
NO REBOOT STRAP
No Reboot Strap R23
HDA_SPKR
Low = Default
High = No Reboot
PCH1A
1 OF 10
RTC
LPC
IHDA
SATA
JTAG
SPI
IBEXPEAK-M-GP-NF
HDD
ODD
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
PCH (SPI/RTC/LPC/SATA/IHDA)
Size A3
Document Number DV14 CP UMA+DIS
Rev X00
Date: Wednesday, March 23, 2011
Sheet 24 of 100

SSID = PCH

X01 0309

+3.3V_RUN

RN2508 SRN10KJ-5-GP

PCH_GPIO22 — INT_SERIRQ 24,37

PCH1F — 6 OF 10

S_GPIO — BMBUSY#/GPIO0 — Y3

21,37 SIO_EXT_SCI# — SIO_EXT_SCI# — TACH1/GPIO1 — C38

21 PCH_GPIO6 — PCH_GPIO6 — TACH2/GPIO6 — D37

21,37 SIO_EXT_WAKE# — SIO_EXT_WAKE# — TACH3/GPIO7 — J32

22,37 SIO_EXT_SMI# — SIO_EXT_SMI# — GPIO8 — F10

C2501 SC47P50V2JN-3GP DY

LAN_PHY_PWR_CTRL/GPIO12 — K9

HOST_ALTERT#1 — GPIO15 — T7

Change NET DGPU_HOLD_RST# to PE_GPIO0 to reset GPU ,09/23

83 DGPU_HOLD_RST# — SATA4GP/GPIO16 — AA2

92,93 DGPU_PWROK — TACH0/GPIO17 — F38

PCH_GPIO22 — SCLOCK/GPIO22 — Y7

C2502 SC47P50V2JN-3GP DY

TPAD14-GP TP2507 — PCH_GPIO27 — GPIO24 — H10

21 PCH_GPIO28 — PCH_GPIO28 — GPIO27 — AB12

STP_PCI# — GPIO28 — V13

+3.3V_ALW

Remove GPIO12,GPIO24 Pull high 09/10

24 CLK_SATA_OE# — CLK_SATA_OE# — STP_PCI#/GPIO34 — M11

HOST_ALTERT#1 — R2519 1KR2J-1-GP — SATACLKREQ#/GPIO35 — V6

37,93 DGPU_PWR_EN# — SATA2GP/GPIO36 — AB7

DGPU_PRSNT# — SATA3GP/GPIO37 — AB13

PCH_GPIO38 — SLOAD/GPIO38 — V3

PCH_GPIO39 — STP_PCI# — RN2509 SRN100KJ-6-GP — SDATAOUT0/GPIO39 — P3

PCH_GPIO45 — PCIECLKRQ6#/GPIO45 — H3

9 DDR_RST_GATE — DDR_RST_GATE — PCIECLKRQ7#/GPIO46 — F1

PCH_GPIO48 — SDATAOUT1/GPIO48 — AB6

37 PCH_TEMP_ALERT# — PCH_TEMP_ALERT# — R2518 X00 — SATA5GP/GPIO49 — AA4

23,62 RTC_BAT_DET# — GPIO57 — F8

+3.3V_RUN — R2508 10KR2J-3-GP UMA — DGPU_PRSNT# — R2507 10KR2J-3-GP DIS

X00 2011 0105 add R2506

+3.3V_RUN — R2504 10KR2J-3-GP UMA — DGPU_HOLD_RST# — R2503 10KR2J-3-GP DIS

+3.3V_RUN — R2505 10KR2J-3-GP DY — DGPU_PWR_EN# — R2506 10KR2J-3-GP DIS

Add PE_GPIO0 , PE_GPIO1 09/09 , pull high/low check H/L active ?

TPAD14-GP TP2510 — PCH_NCTF_1 — VSS_NCTF_1 … VSS_NCTF_31 (NCTF)

TPAD14-GP TP2511 — PCH_NCTF_2

TPAD14-GP TP2512 — PCH_NCTF_3

TPAD14-GP TP2509 — PCH_NCTF_4

IBEXPEAK-M-GP-NF

CLKOUT_PCIE6N — AH45
CLKOUT_PCIE6P — AH46
CLKOUT_PCIE7N — AF48
CLKOUT_PCIE7P — AF47
A20GATE — U2 — SIO_A20GATE# 37
CLKOUT_BCLK0_N/CLKOUT_PCIE8N — AM3 — BCLK_CPU_N 9
CLKOUT_BCLK0_P/CLKOUT_PCIE8P — AM1 — BCLK_CPU_P 9
PECI — BG10 — H_PECI 9
RCIN# — T1 — SIO_RCIN# 37
PROCPWRGD — BE10 — H_PWRGD 9,42
THRMTRIP# — BD10 — PCH_THERMTRIP_R

+1.05V_VTT — SRN56J-4-GP RN2505 — PCH_THERMTRIP_R — H_THERMTRIP# 9,42,85

Placed Within 2" from PCH

TP1 BA22 … TP24 C10 — NC_1 AB45 — NC_2 AB38 — NC_3 AB42 — NC_4 AB41 — NC_5 T39

INIT3_3V# — P6 — INIT3_3V# — TP2506TPAD14-GP

+3.3V_ALW — R2516 10KR2J-3-GP DY — PCH_GPIO45 — R2517 10KR2J-3-GP

HDMI function detect.

PCH_GPIO45	0	1
HDMI Function	YES	NO

22,37 PM_CLKRUN# — PM_CLKRUN# — PCH_GPIO38 — SATA_DET#1_R — SATA_DET#0_R — RN2507 SRN10KJ-L3-GP — S_GPIO — PCH_TEMP_ALERT# — PCH_GPIO48 — +3.3V_RUN

24 SATA_DET#1_R
24 SATA_DET#0_R

23 PEG_B_CLKRQ# — PEG_B_CLKRQ# — PCIE_CLK_RQ0# — PCIE_CLK_RQ4# — AC_PRESENT_EC — RN2506 SRN10KJ-L3-GP — DDR_RST_GATE — SUS_PWR_DN_ACK — +3.3V_ALW

23 PCIE_CLK_RQ0#
23 PCIE_CLK_RQ4#
22,37 AC_PRESENT_EC

SUS_PWR_DN_ACK 22,37

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

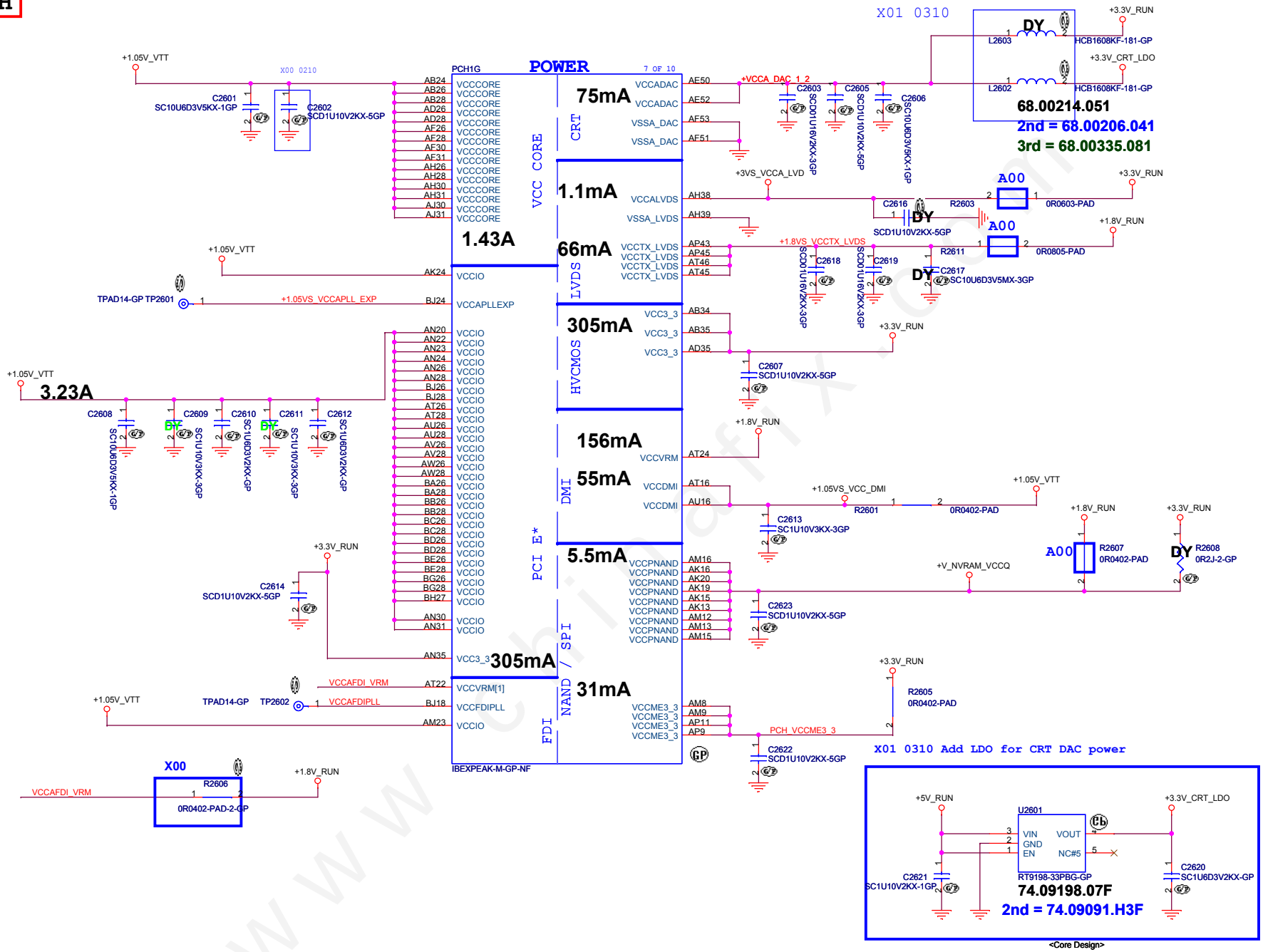
Title: PCH (GPIO/CPU)

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 25 of 100

SSID = PCH

X01 0310



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	PCH (POWER1)
Size	A3
Document Number	DV14 CP UMA+DIS
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Date:	Tuesday, March 22, 2011
Sheet	26 of 100

SSID = PCH

PCH1J

POWER

10 OF 10

Clock and Miscellaneous

USB

PCI/GPIO/LPC

SATA

CPU

RTC

HDA

IBEXPEAK-M-GP-NF

TPAD14-GP TP2515 1VCCACLK

AP51 VCCACLK
AP53 VCCACLK
AF23 VCCLAN
AF24 VCCLAN
DCPSUSBYP Y20 DCPSUSBYP
AD38 VCCME
AD39 VCCME
AD41 VCCME
AF43 VCCME
AF41 VCCME
AF42 VCCME
V39 VCCME
V41 VCCME
V42 VCCME
Y39 VCCME
Y41 VCCME
Y42 VCCME
V9 DCPRTC
AU24 VCCVRM
BB51 VCCADPLLA
BB53 VCCADPLLA
BD51 VCCADPLLB
BD53 VCCADPLLB
AH23 VCCIO
AJ35 VCCIO
AH35 VCCIO
AF34 VCCIO
AH34 VCCIO
AF32 VCCIO
V12 DCPSST
Y22 DCPSUS
P18 VCCSUS3_3
U19 VCCSUS3_3
U20 VCCSUS3_3
U22 VCCSUS3_3
V15 VCC3_3
V16 VCC3_3
Y16 VCC3_3
AT18 V_CPU_IO
AU18 V_CPU_IO
A12 VCCRTC

V24 VCCIO
V26 VCCIO
Y24 VCCIO
Y26 VCCIO
V28 VCCSUS3_3
U28 VCCSUS3_3
U26 VCCSUS3_3
U24 VCCSUS3_3
P28 VCCSUS3_3
P26 VCCSUS3_3
N28 VCCSUS3_3
N26 VCCSUS3_3
M28 VCCSUS3_3
M26 VCCSUS3_3
L28 VCCSUS3_3
L26 VCCSUS3_3
J28 VCCSUS3_3
J26 VCCSUS3_3
H28 VCCSUS3_3
H26 VCCSUS3_3
G28 VCCSUS3_3
G26 VCCSUS3_3
F28 VCCSUS3_3
F26 VCCSUS3_3
E28 VCCSUS3_3
E26 VCCSUS3_3
C28 VCCSUS3_3
C26 VCCSUS3_3
B27 VCCSUS3_3
A28 VCCSUS3_3
A26 VCCSUS3_3
U23 VCCSUS3_3
V23 VCCIO
F24 V5REF_SUS
K49 V5REF
J38 VCC3_3
L38 VCC3_3
M36 VCC3_3
N36 VCC3_3
P36 VCC3_3
U35 VCC3_3
AD13 VCC3_3
AK3 VCCSATAPLL
AK1 VCCSATAPLL
AH22 VCCIO
AT20 VCCVRM
AH19 VCCIO
AD20 VCCIO
AF22 VCCIO
AD19 VCCIO
AF20 VCCIO
AF19 VCCIO
AH20 VCCIO
AB19 VCCIO
AB20 VCCIO
AB22 VCCIO
AD22 VCCIO
AA34 VCCME
Y34 VCCME
Y35 VCCME
AA35 VCCME
L30 VCCSUSHDA

+1.05V_VTT
+3.3V_ALW
+3.3V_RUN
+5V_ALW
+5V_RUN
+1.8V_RUN
+1.05VS_VCCA_A_DPL
+1.05VS_VCCA_B_DPL
+VCCRTCEXT
+VCCSST
+1.05VALW_INT_VCCSUS
+5VALW_PCH_VCC5REFSUS
+5VS_PCH_VCC5REF
VCCSATAPLL
+3VS_+1.5VS_HDA_IO
+RTC_CELL

1.2A
88mA
88mA
133mA
1mA
1mA
1mA
6mA

Simulation 10/07
Simulation 10/07

L2702 SC10U6D3V5MX-3GP IND-10UH-218-GP 68.10050.10Y 2nd = 68.1001E.10N
L2703 IND-10UH-218-GP 68.10050.10Y 2nd = 68.1001E.10N

C2704 SC10U6D3V5KX-1GP
C2705 DY
C2706 DY SC1U6D3V2KX-GP
C2707 SCD1U10V2KX-5GP
C2708 SC1U6D3V2KX-GP
C2709 SCD1U10V2KX-5GP
C2710 DY
C2711 SC1U6D3V2KX-GP
C2712 SC1U6D3V2KX-GP
C2713 SCD1U10V2KX-5GP
C2714 SC1U6D3V2KX-GP
C2715 SC1U6D3V2KX-GP
C2716 SCD1U10V2KX-5GP
C2717 SCD1U10V2KX-5GP
C2718 SC1U6D3V2KX-GP
C2719 SC1U6D3V2KX-GP
C2720 SC1U6D3V2KX-GP
C2723 SCD1U10V2KX-5GP
C2724 SCD1U10V2KX-5GP
C2725 SC1U6D3V2KX-GP
C2726 SCD1U10V2KX-5GP
C2727 SCD1U10V2KX-5GP
C2728 SC10U6D3V5KX-1GP
C2729 SCD1U10V2KX-5GP
C2730 SC1U6D3V2KX-GP
C2731 SC1U6D3V2KX-GP
C2732 SCD1U10V2KX-5GP
C2733 SCD1U10V2KX-5GP
C2734 DY
C2735 DY

D2701 CH751H-40PT-GP
D2702 CH751H-40PT-GP
83.R0304.A8F
2nd = 83.R2004.B8F
83.R0304.A8F
2nd = 83.R2004.B8F

R2701 100R2F-L1-GP-U
R2702 100R2F-L1-GP-U
R2707 0R0402-PAD

TP2514 TPAD14-GP

X00 0210

Isolate the power supply for pin AF34,AH34,AF32 these pins can be shorted together . NOT with AH35,AJ35

X00 09/23

<Core Design>

Wistron Corporation
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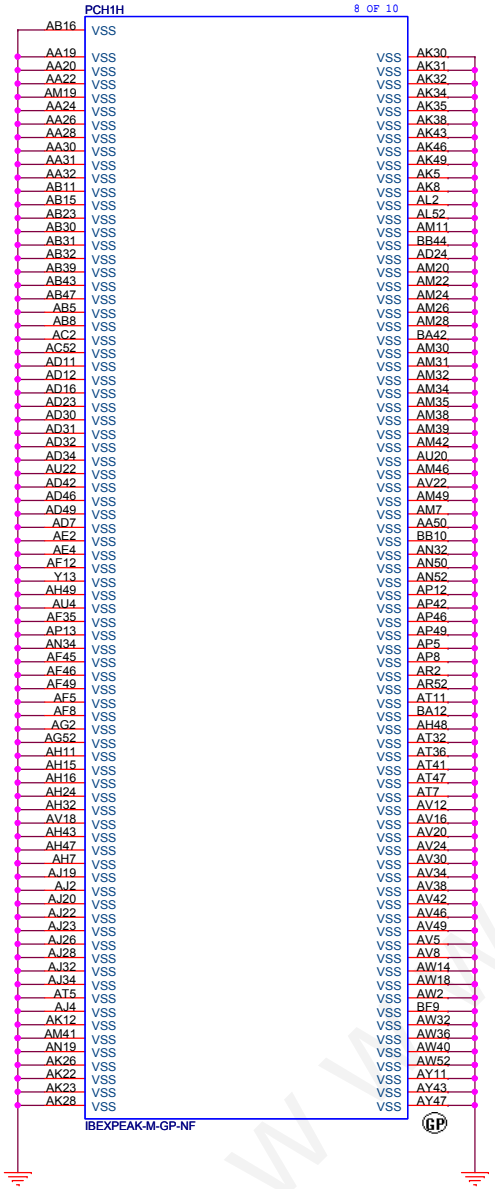
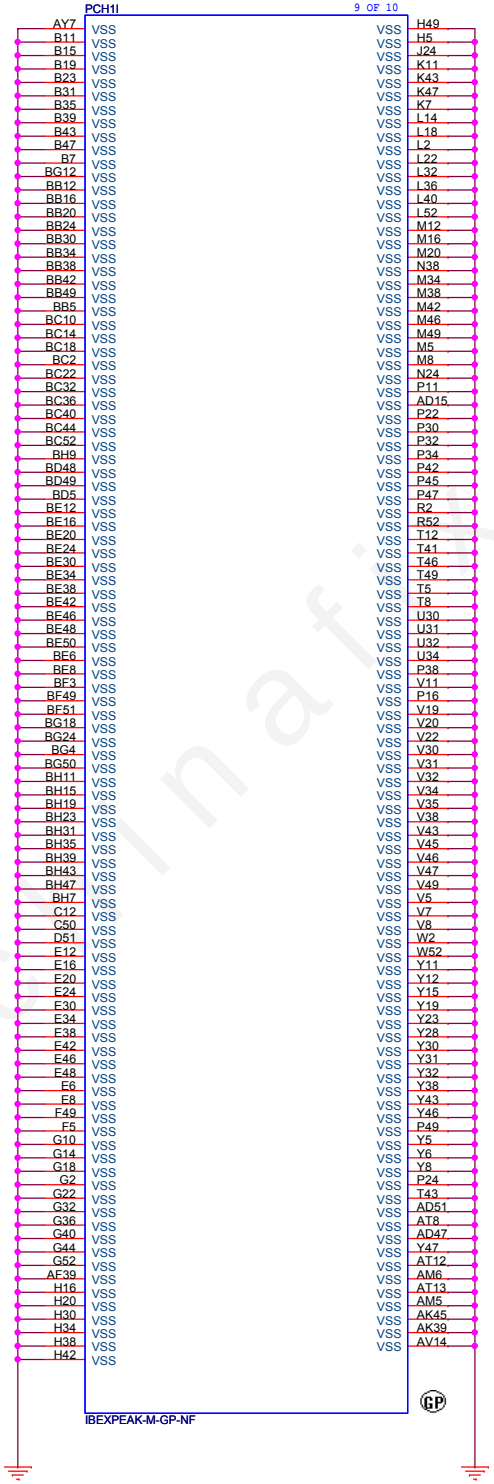
Title: PCH (POWER2)
Size: A3
Document Number: DV14 CP UMA+DIS
Rev: X00
Date: Tuesday, March 22, 2011
Sheet 27 of 100

SSID = PCH





<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (VSS)

Size	Document Number	Rev
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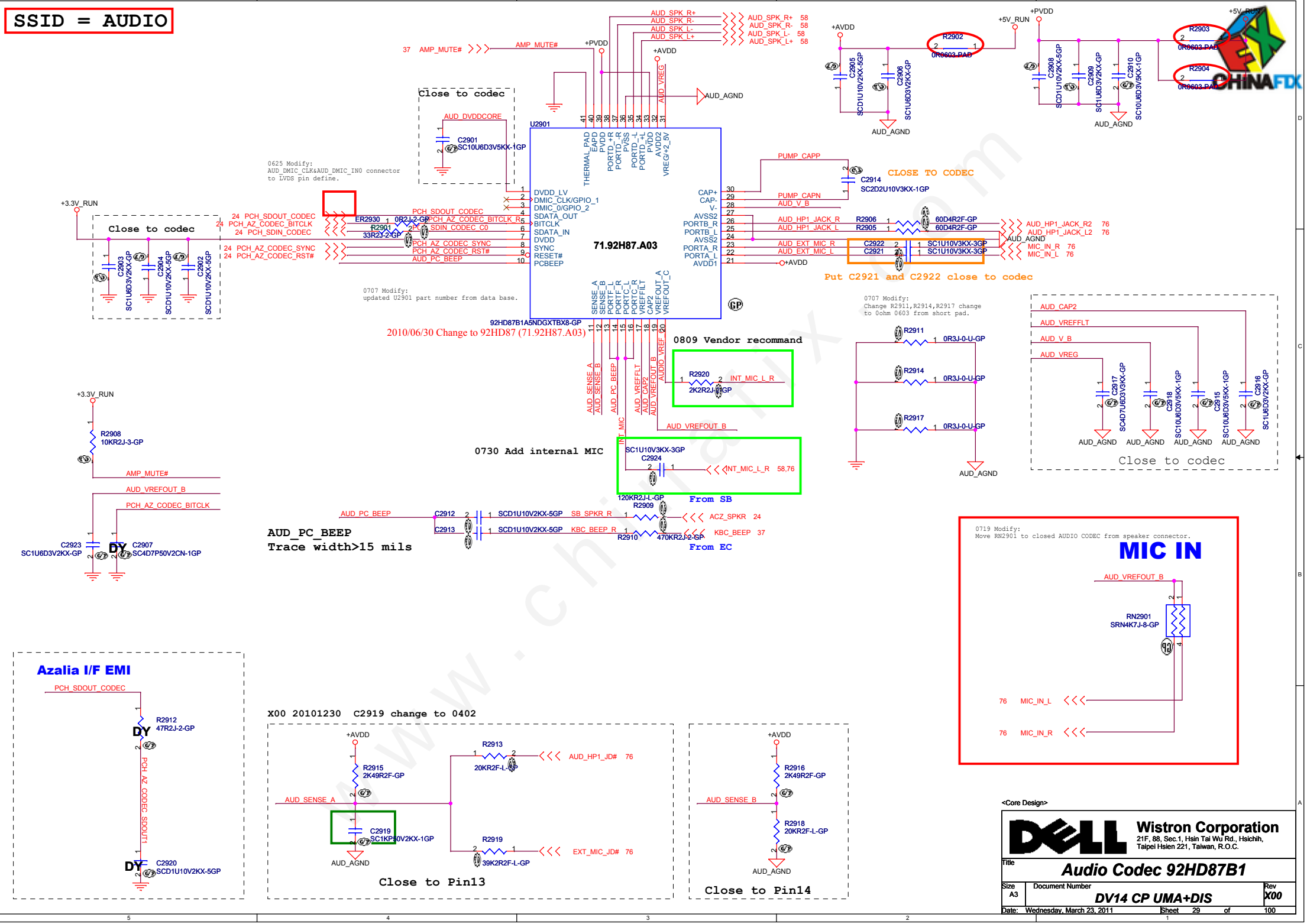
Date: Tuesday, January 25, 2011 Sheet 28 of 100

SSID = AUDIO



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec 92HD87B1

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 29 of 100

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<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

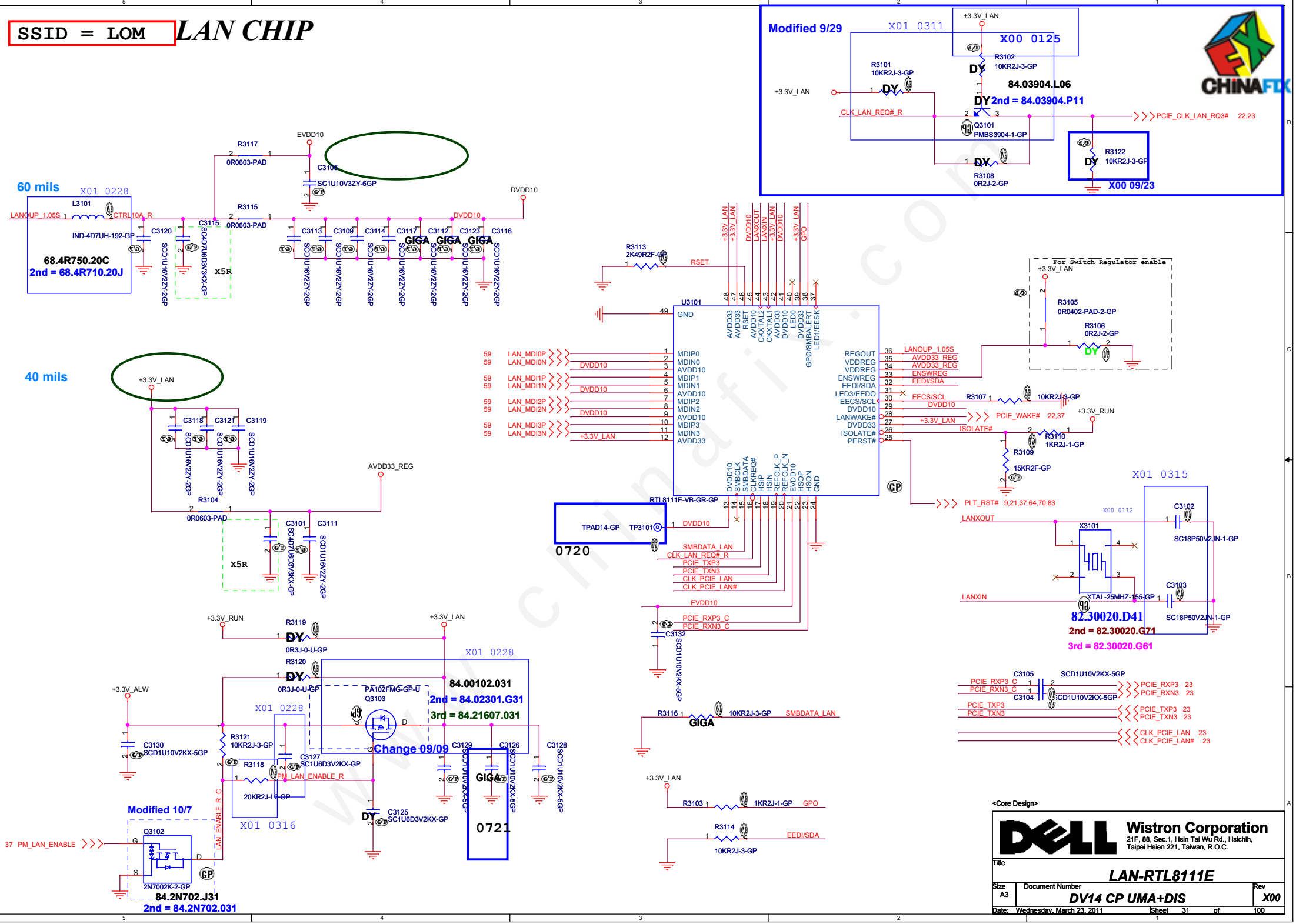
Title: *Reserved*

Size: A3 | Document Number: *DV14 CP UMA+DIS* | Rev: *X00*

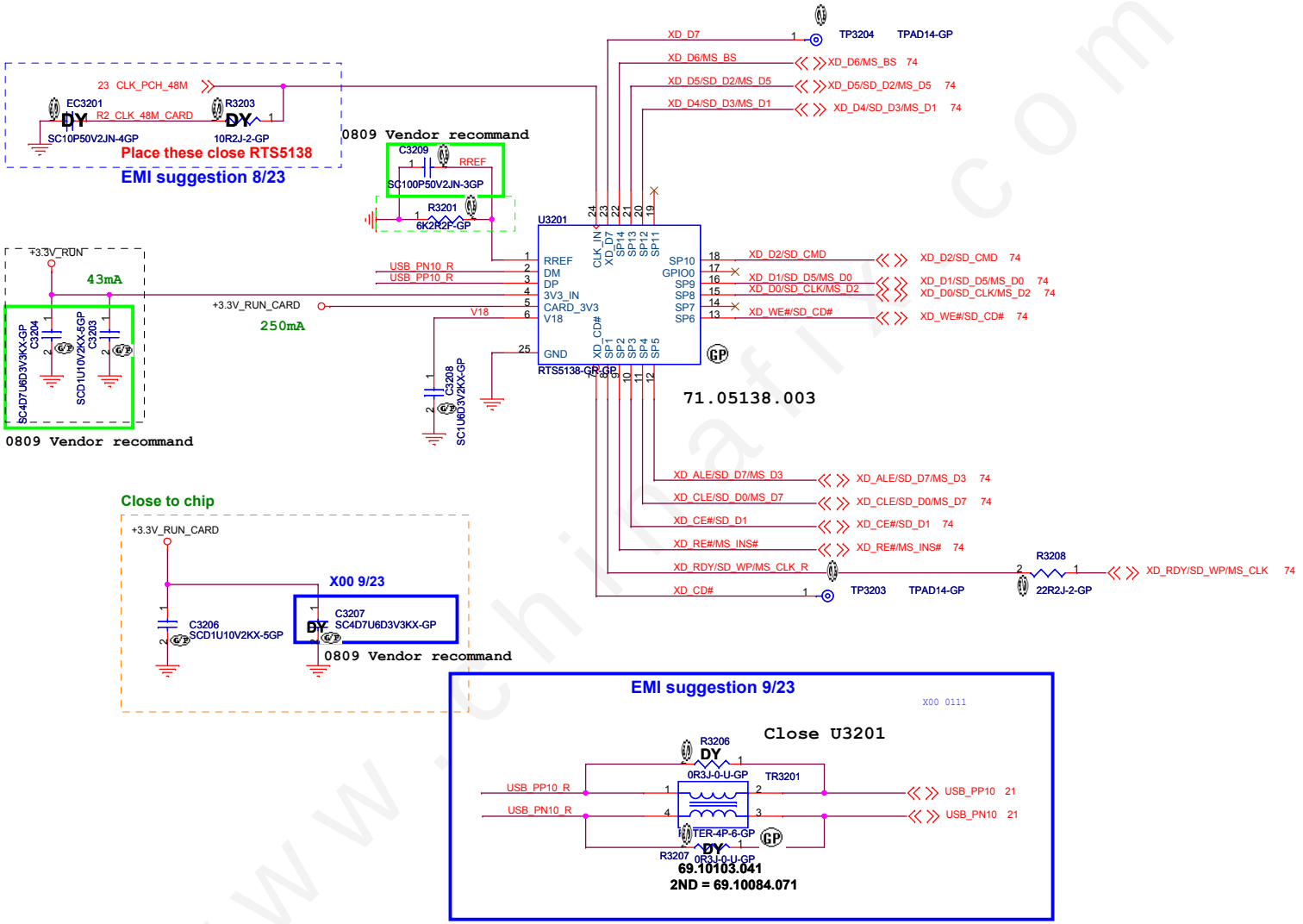
Date: Thursday, January 06, 2011 | Sheet 30 of 100

SSID = LOM

LAN CHIP



SSID = SDIO



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-RTS5138

Size	Document Number	Rev
A3	DV14 CP UMA+DIS	X00

Date: Wednesday, March 23, 2011 Sheet 32 of 100

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: Reserved

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Thursday, January 06, 2011 | Sheet 33 of 100

(Blanking)

<Core Design>

Wistron Corporation
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Title: *Reserved*

Size	Document Number	Rev
A3	*DV14 CP UMA+DIS*	*X00*

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DV14 CP UMA+DIS*	*X00*

Date: Thursday, January 06, 2011 Sheet 35 of 100

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Reserved*

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A3	*DV14 CP UMA+DIS*	*X00*

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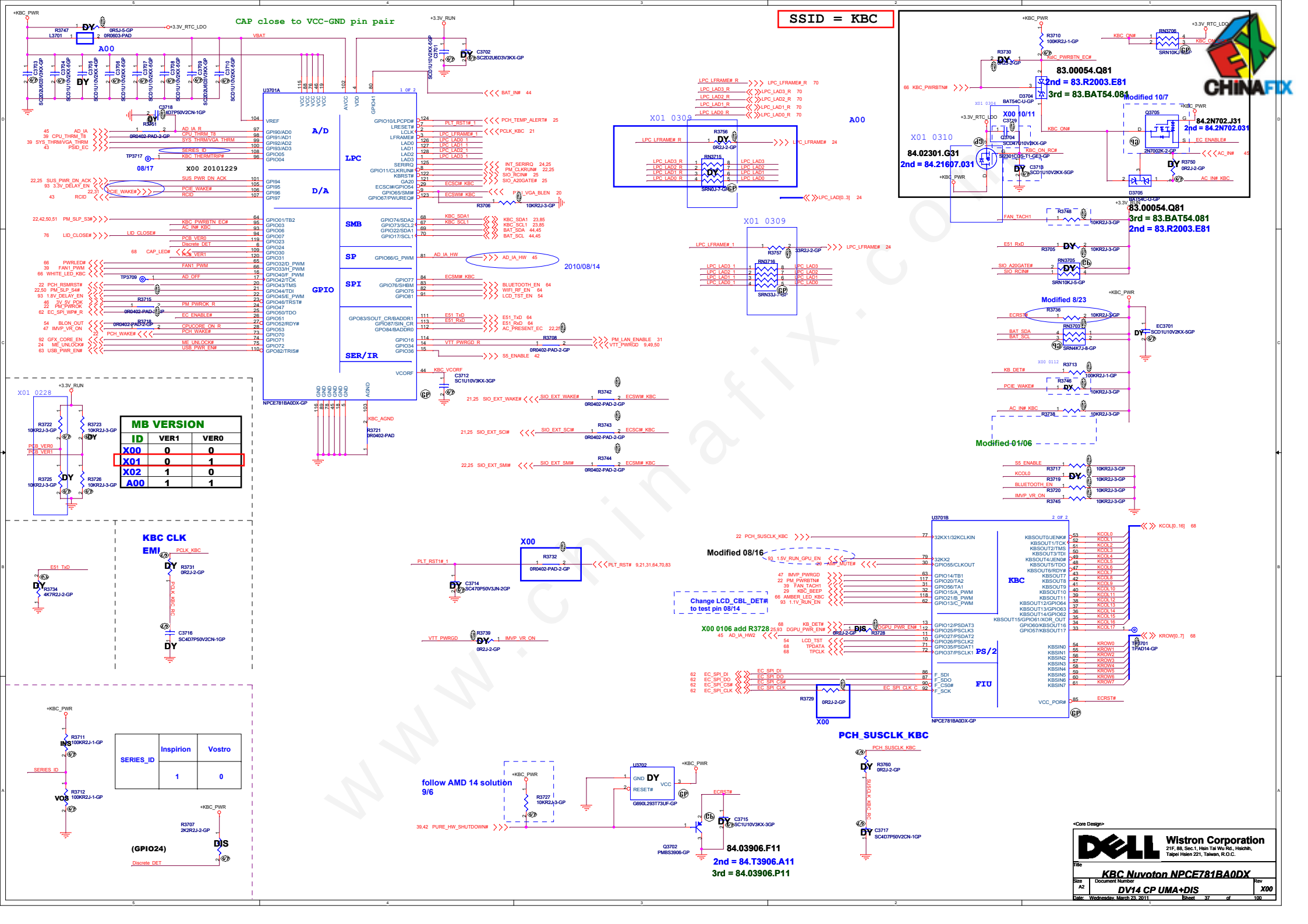
SSID = KBC
CAP close to VCC-GND pin pair
U3701A
NPCE781BA0DX-GP
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
08/17
X00 20101229
2010/08/14
MB VERSION
ID | VER1 | VER0
X00 | 0 | 0
X01 | 0 | 1
X02 | 1 | 0
A00 | 1 | 1
KBC CLK EMI
SERIES_ID
Inspirion
Vostro
(GPIO24)
follow AMD 14 solution 9/6
83.00054.Q81
2nd = 83.R2003.E81
3rd = 83.BAT54.081
Modified 10/7
84.2N702.J31
2nd = 84.2N702.031
84.02301.G31
2nd = 84.21607.031
Modified 8/23
Modified 01/06
Modified 08/16
Change LCD_CBL_DET# to test pin 08/14
X00 0106 add R3728
PCH_SUSCLK_KBC
84.03906.F11
2nd = 84.T3906.A11
3rd = 84.03906.P11
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC Nuvoton NPCE781BA0DX
DV14 CP UMA+DIS
X00
Wednesday, March 23, 2011
37
100

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Thursday, January 06, 2011 | Sheet 38 of 100

SSID = Thermal

Thermal sensor P2800

01/05 change R3903&R3904 to 0ohm.Remove C3905

+3.3V_RUN
C3901 SCD1U10V2KX-5GP

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

+3.3V_RUN
R3903 0R2J-2-GP DY
ADJ
87.1 Degree
R3904 0R2J-2-GP DY

optional
R_up 0Ω
0.1μF
Option 1: OTZ=95°C → ADJ=3.3V
Option 2: OTZ=85°C → ADJ=Floating
Option 3: OTZ=90°C → ADJ=GND
R_down 0Ω
ADJ

Very Close to CPU1

U3901 P2800EB0-GP
VCC DXP DXN OTZ TDR TDL GND ADJ
P2800_DXP_R
P2800_DXN_R
SYS_THRM/VGA_THRM 37
CPU_THRM_T8 37
THERM_SYS_SHDN# R3911 0R2J-2-GP T8_P2800

74.02800.B71
1.H/W T8 Shutdown

R(K)= 0.0012*T^2- 0.9308T+ 96.147

Fan controller P2793

X01 0303
37 FAN1_PWM
R3914 4K7R2J-2-GP
FAN1_PWM_R
C3911 SCD1U10V2KX-5GP
R3902 DY 0R2J-2-GP
+5V_RUN
FAN_VCC
Layout 10 mil
U3902 G991P11U-GP
FON# VIN VO VSET GND GND GND GND
for linear FAN
74.00991.031
2nd = 74.02793.A31

Very close to CPU1
12/15 Remove 3rd source

11/4 Vendor recommand
X01 0309 DY G709 function
R3913 470KR2J-2-GP DY
+3.3V_RUN
R3905 150R2J-1-GP DY
R3928 0R2J-2-GP DY
U3905 G709T1UF-GP
SET GND OUT# VCC HYST
ADJ_G709
G709_VCC
HYST_PH
THERM_SYS_SHDN# R3910 0R2J-2-GP DY T8_G709
R3912 24K2R2F-1-GP DY
86.9
C3908 SCD1U10V2KX-5GP DY
X01 0311
AFTP2803
AFTP2802
FAN1
37 FAN_TACH1
R3907 0R0402-PAD-2-GP
FAN_TACH1_C
Layout 15 mil
FAN_VCC
C3909 SC47U6D3V3KX-GP
D3902 CH551H-30PT-GP
C3910 SC2200P50V2KX-2GP
AFTP2801
FOX-CON3-6-GP-U
20.D0210.103
2nd = 20.D0246.103
3rd = 20.F1716.003
83.R5003.C8F
2ND = 83.R5003.H8H
3rd = 83.5R003.08F

R3908 NTC-100K-8-GP DY
Q3901 PBSS3904-1-GP
C3906 SC470P50V3JN-2GP
P2800_DXP
P2800_DXN
RN3901 SRN0J-6-GP
C3907 SC2200P50V2KX-2GP
P2800_DXP_R
P2800_DXN_R
84.03904.L06
2nd = 84.03904.P11
2.System Sensor, Put on palm rest

Modified 8/27

85 P2800_VGA_DXP
P2800_VGA_DXP
Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.
RN3902 SRN0J-6-GP DY
85 P2800_VGA_DXN
P2800_VGA_DXN

+3.3V_RUN
R3909 100KR2J-1-GP
Q3902 2N7002K-2-GP
S D G
THERM_SYS_SHDN#
37,42 PURE_HW_SHUTDOWN#
C2811 SCD1U10V2KX-2GP DY
84.2N702.J31
2ND = 84.2N702.031

EMI/ESD
FAN_VCC
EC3901 SCD1U16V2KX-3GP DY

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal P2800/Fan Controllor P2793
Size: A3
Document Number: Enrico Caruso 14
Rev: X00
Date: Wednesday, March 23, 2011
Sheet 39 of 100

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Thursday, January 06, 2011 | Sheet 40 of 100

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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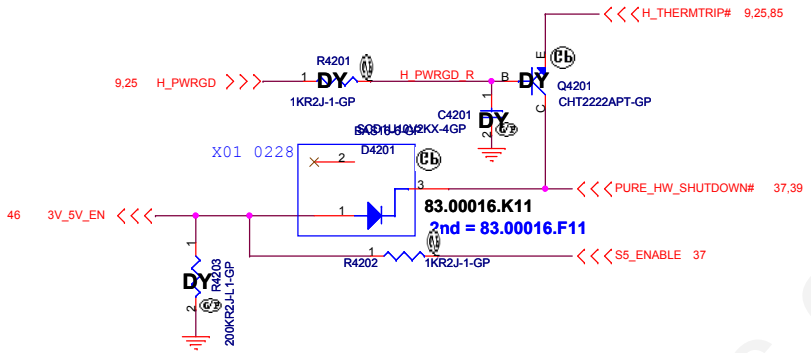
Title: *Reserved*

Size	Document Number	Rev
A3	*DV14 CP UMA+DIS*	*X00*

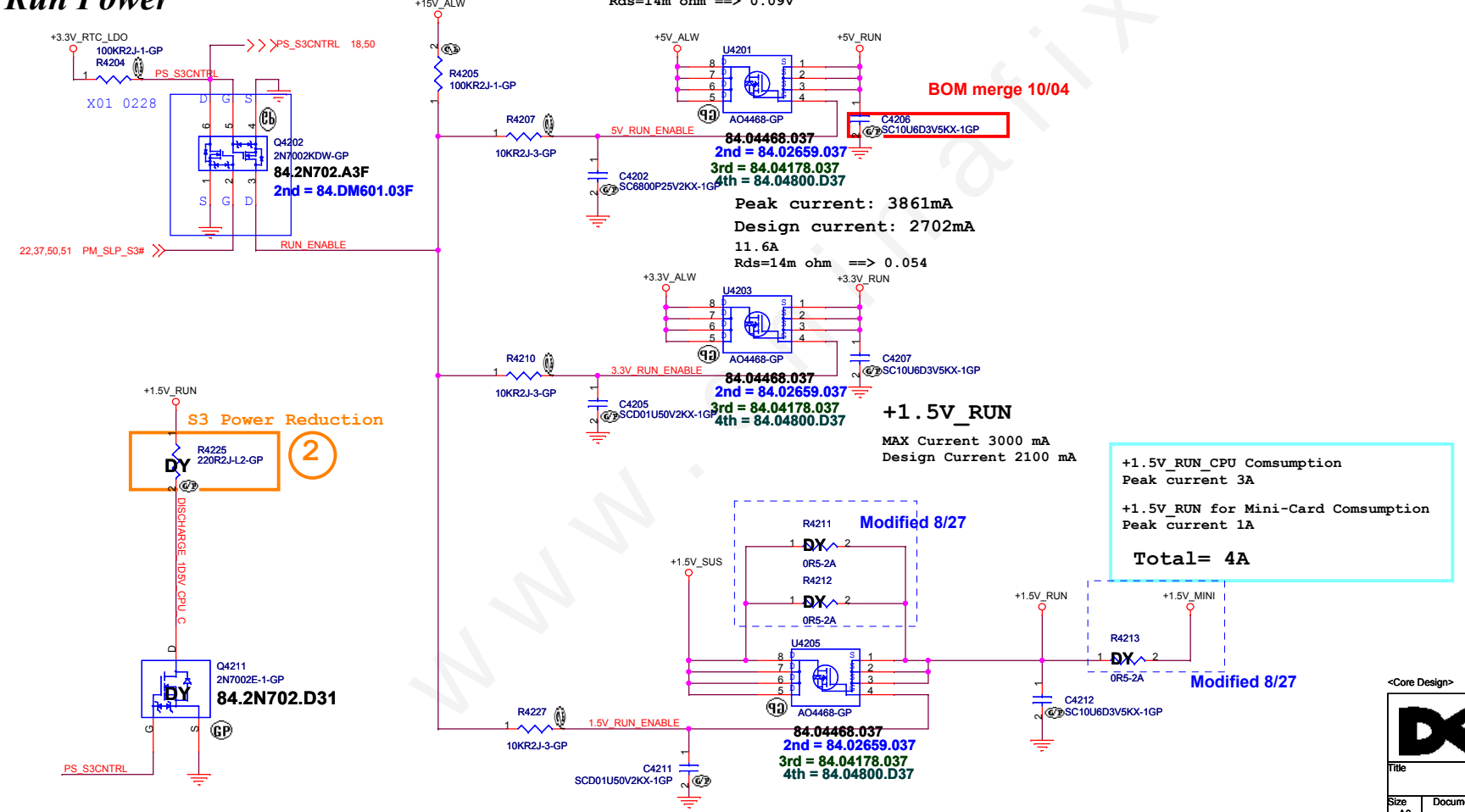
Date: Thursday, January 06, 2011 Sheet 41 of 100

SSID = Reset.Suspend



Peak current: 6370mA (HD:1100 ODD:2500)
Design current: 4459 mA
11.6A
Rds=14m ohm ==> 0.09V

Run Power



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
A3	DV14 CP UMA+DIS	X00

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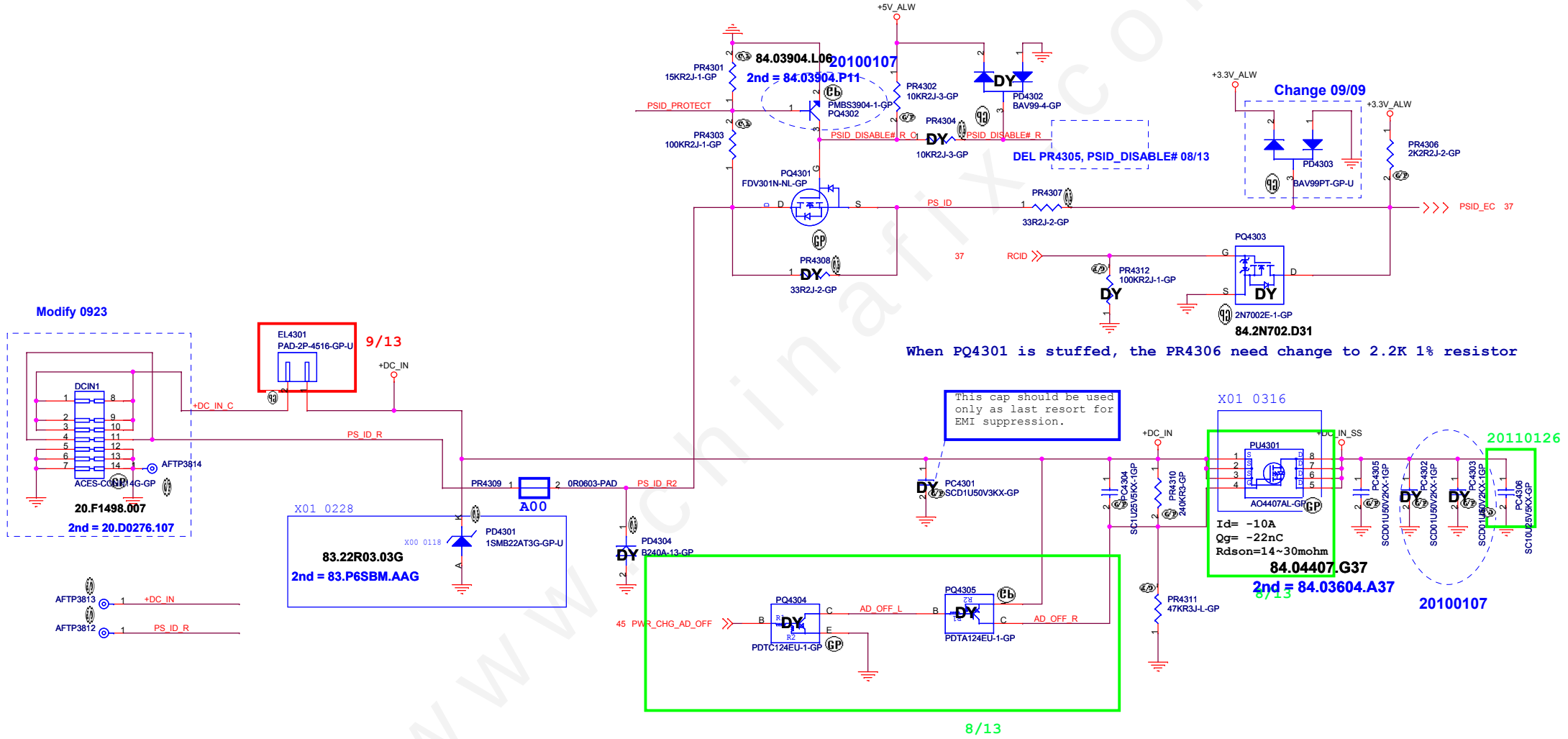
SSID = PWR.Support

DCin CONN



<Core Design>

Wistron Corporation
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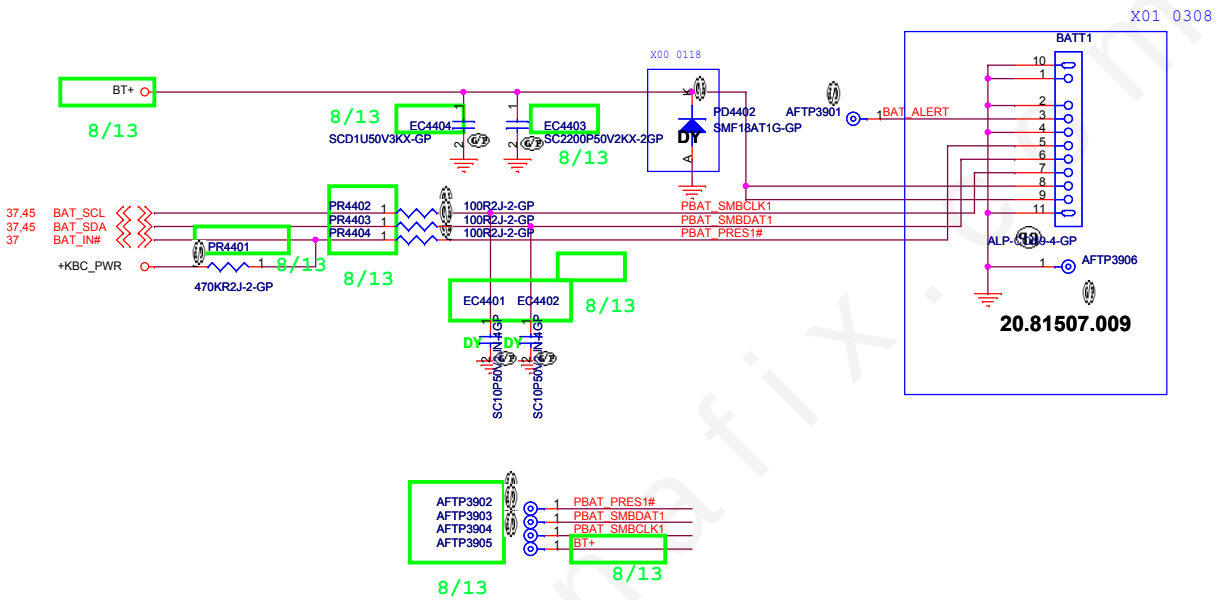
Taipei Hsien 221, Taiwan, R.O.C.

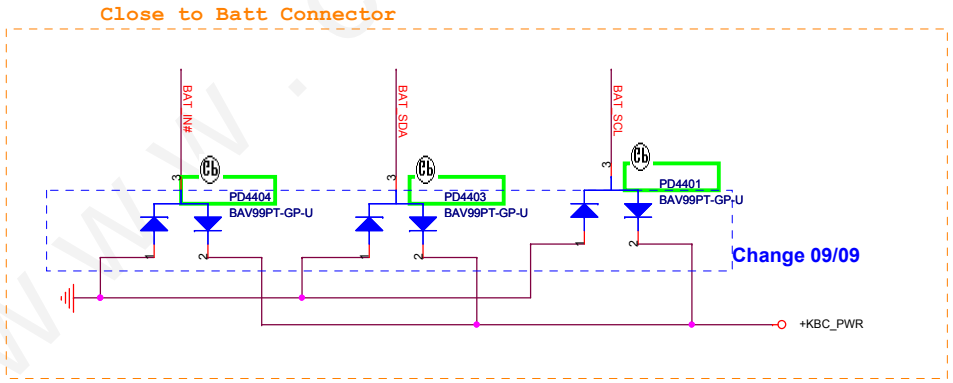
Title	DCIN Jack	
Size: A3	Document Number: DV14 CP UMA+DIS	Rev: X00
Date: Wednesday, March 23, 2011	Sheet 43 of 100	

SSID = PWR.Support

Batt Connecter



For actual location, need to be swap all pin



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

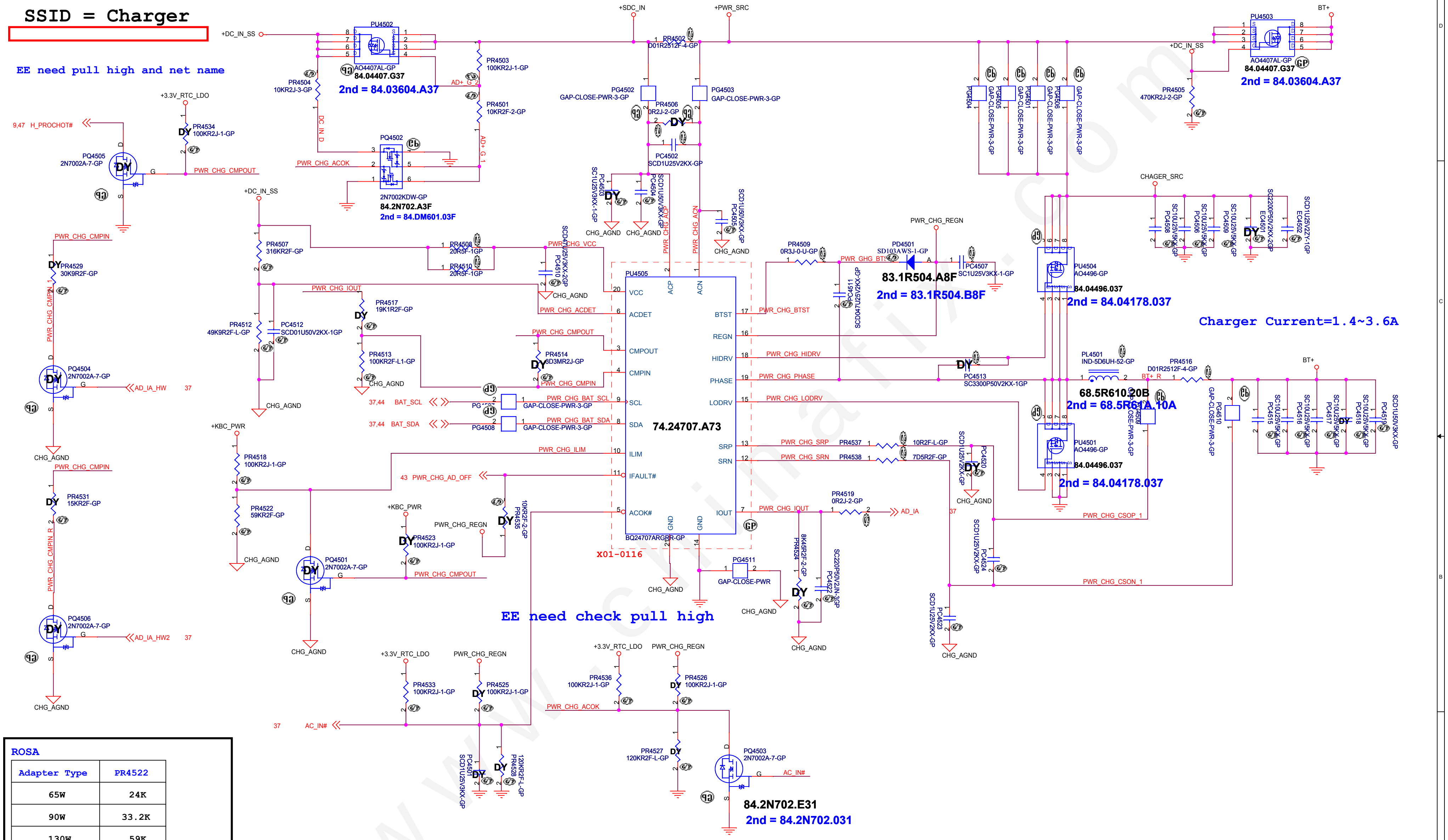
Title: BATT CONN

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 44 of 100

SSID = Charger

EE need pull high and net name



ROSA

Adapter Type	PR4522
65W	24K
90W	33.2K
130W	59K

EC code only BQ24707

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
65W	0	0
90W	1	0
130W	0	1

<Core Design>

DELL

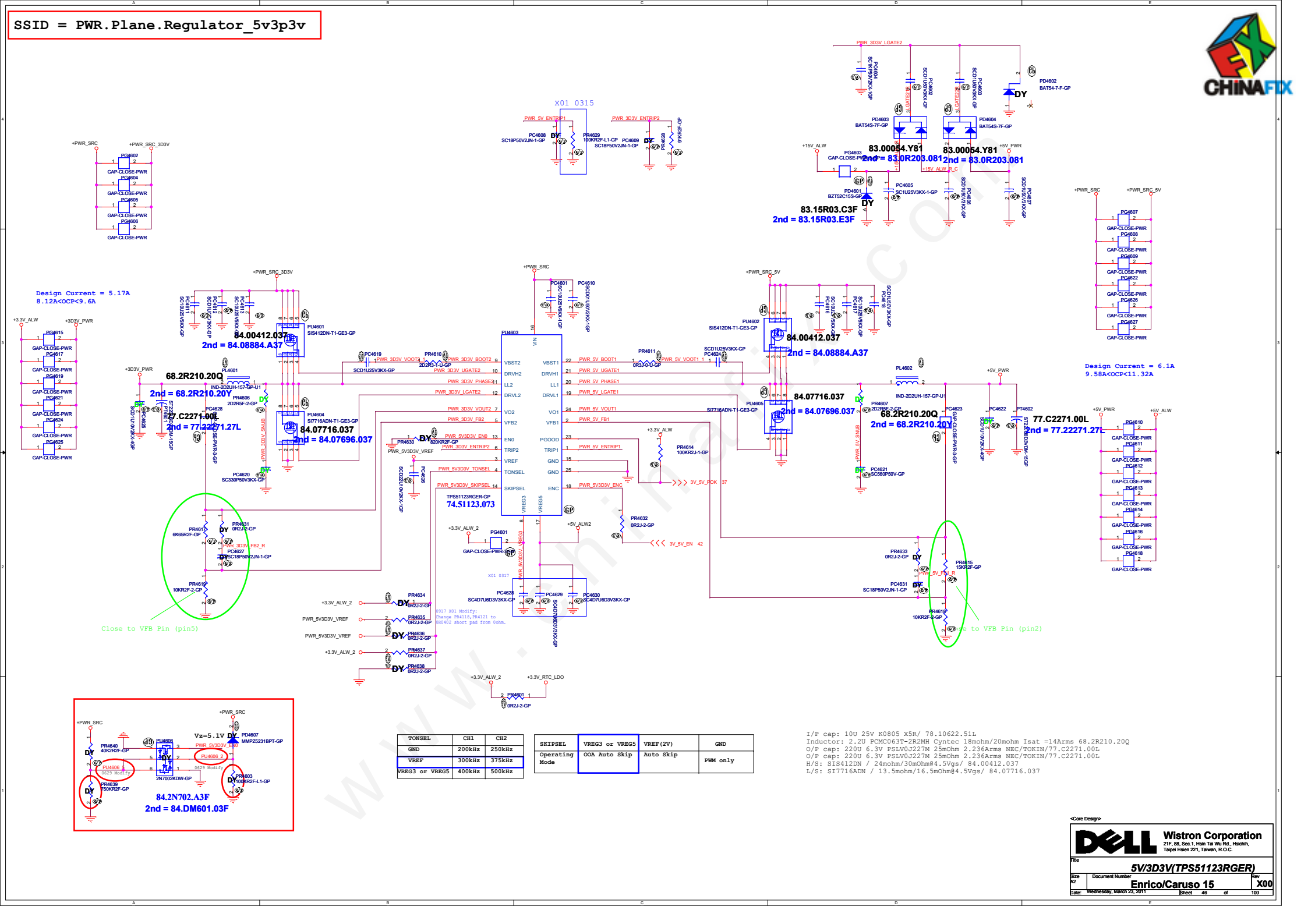
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER BQ24707**

Size: C | Document Number: **DV14 CP UMA+DIS** | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 45 of 100

SSID = PWR.Plane.Regulator_5v3p3v



TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3 or VREG5	400kHz	500kHz

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

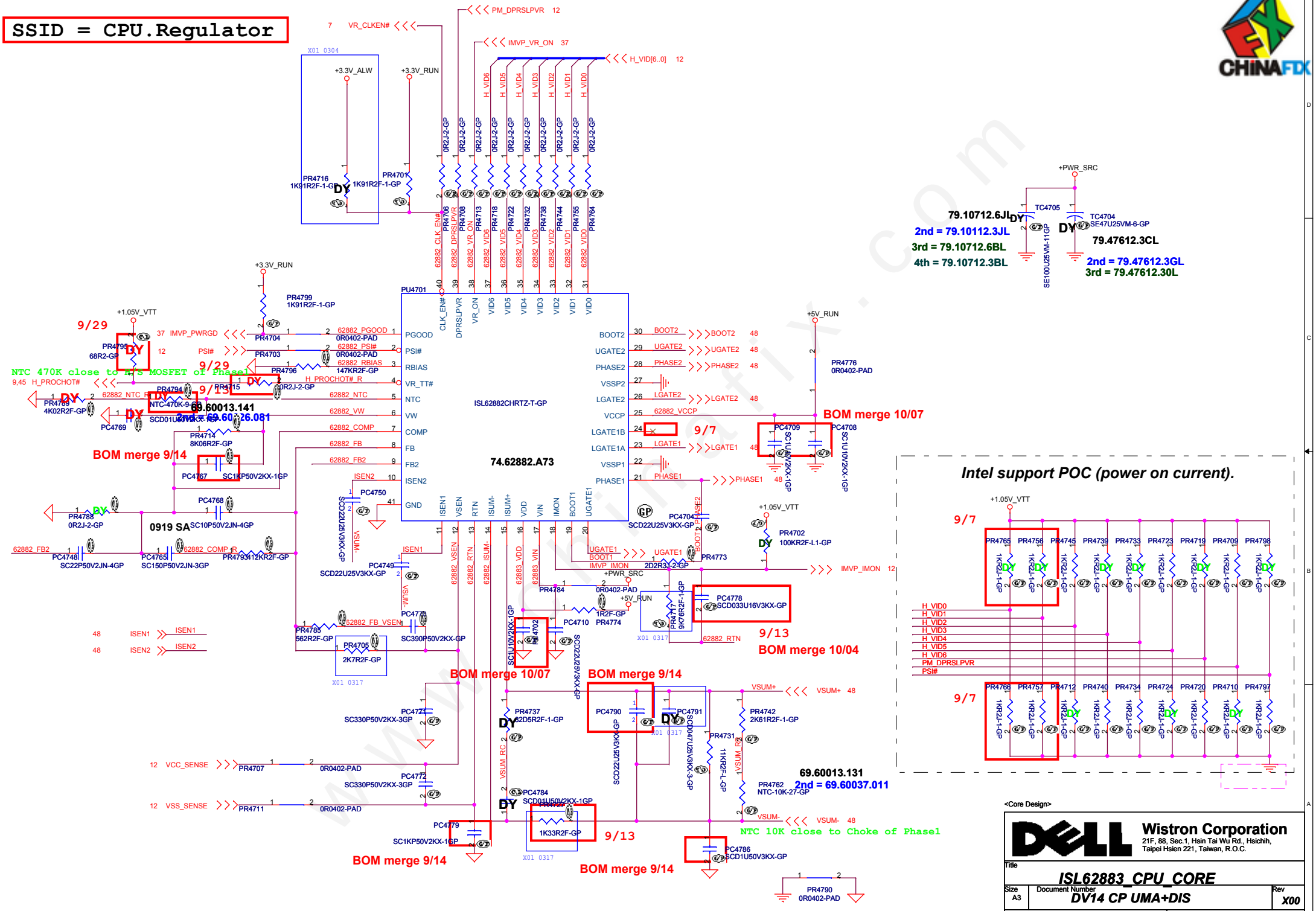
I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.2U PCMC063T-2R2MH Cyntec 18mohm/20mohm Isat =14Arms 68.2R210.20Q
O/P cap: 220U 6.3V PSLV0J227M 25mOhm 2.236Arms NEC/TOKIN/77.C2271.00L
O/P cap: 220U 6.3V PSLV0J227M 25mOhm 2.236Arms NEC/TOKIN/77.C2271.00L
H/S: SIS412DN / 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SI7716ADN / 13.5mohm/16.5mOhm@4.5Vgs/ 84.07716.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 5V/3D3V(TPS51123RGER)
Size: A2 | Document Number: Enrico/Caruso 15 | Rev: X00
Date: Wednesday, March 23, 2011 | Sheet 46 of 100

SSID = CPU.Regulator



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62883_CPU_CORE

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

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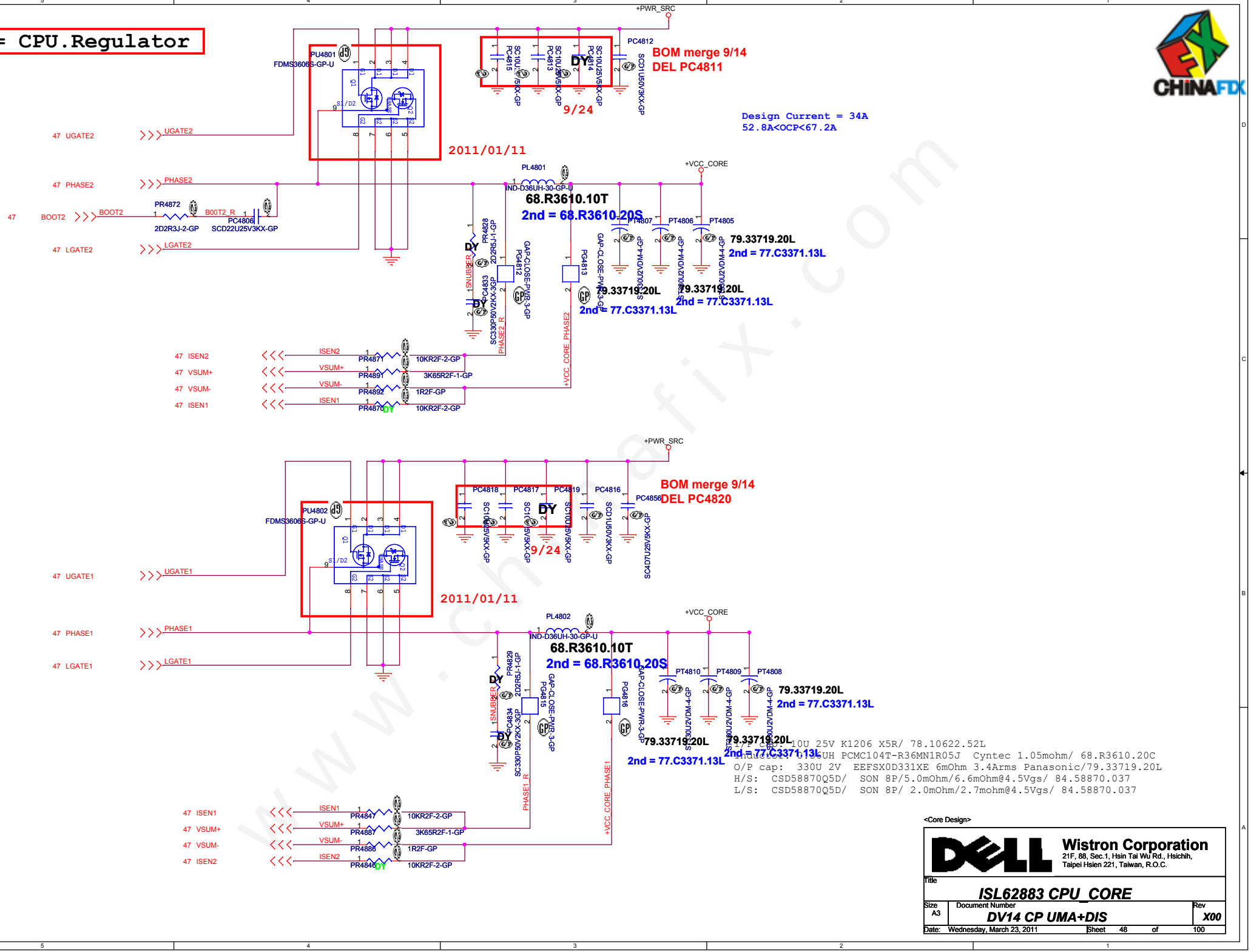
SSID = CPU.Regulator



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.36UH PCMC104T-R36MN1R05J Cyntec 1.05mohm/ 68.R3610.20C
O/P cap: 330U 2V EEFSX0D331XE 6mOhm 3.4Arms Panasonic/79.33719.20L
H/S: CSD58870Q5D/ SON 8P/5.0mOhm/6.6mOhm@4.5Vgs/ 84.58870.037
L/S: CSD58870Q5D/ SON 8P/ 2.0mOhm/2.7mohm@4.5Vgs/ 84.58870.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62883 CPU_CORE

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A3	DV14 CP UMA+DIS	X00

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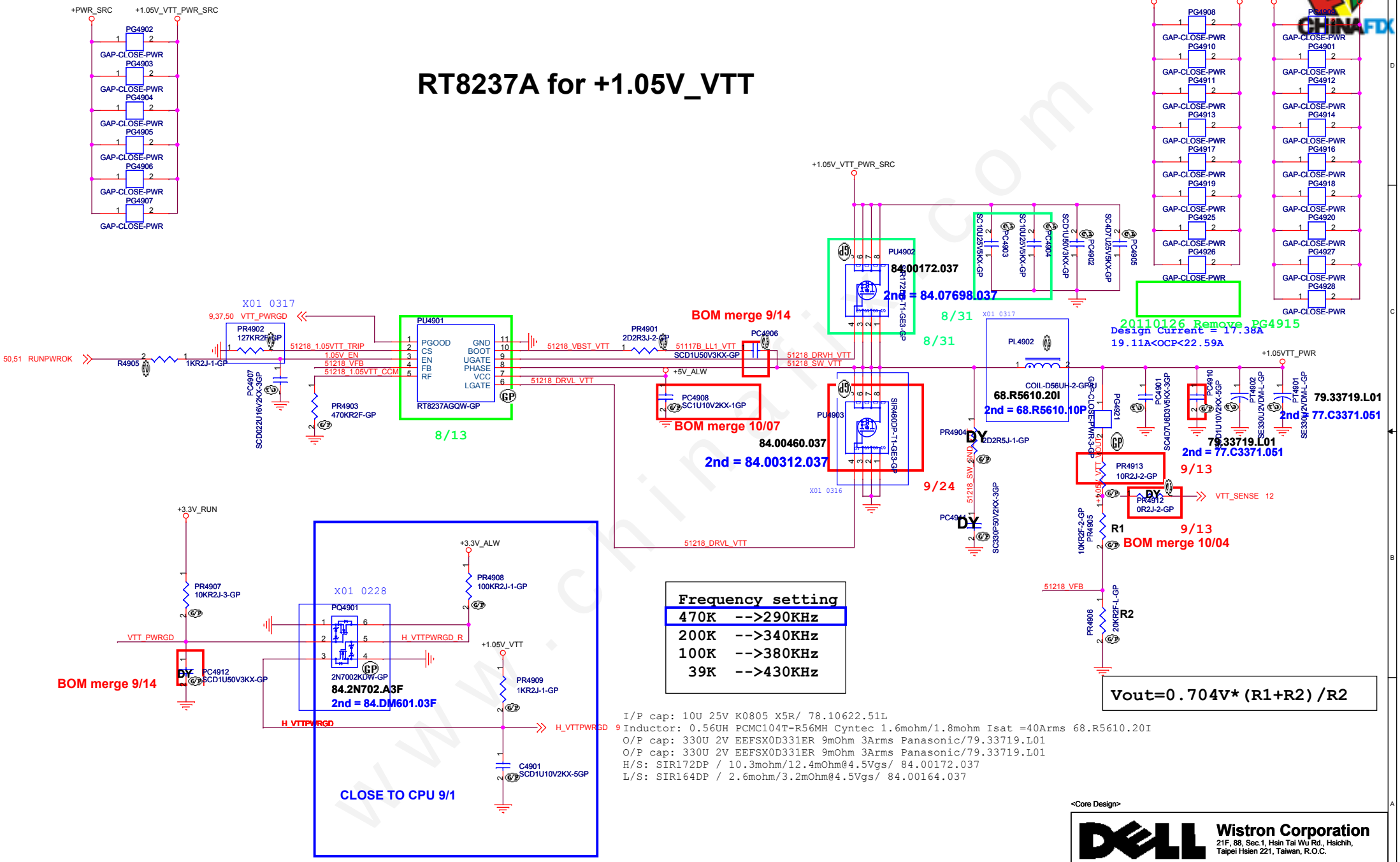
SSID = CPU.Regulator

RT8237A for +1.05V_VTT



Frequency setting
470K -->290KHz
200K -->340KHz
100K -->380KHz
39K -->430KHz

Vout=0.704V*(R1+R2)/R2

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 0.56UH PCMC104T-R56MH Cyntec 1.6mohm/1.8mohm Isat =40Arms 68.R5610.20I
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/79.33719.L01
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/79.33719.L01
H/S: SIR172DP / 10.3mohm/12.4mOhm@4.5Vgs/ 84.00172.037
L/S: SIR164DP / 2.6mohm/3.2mOhm@4.5Vgs/ 84.00164.037

<Core Design>

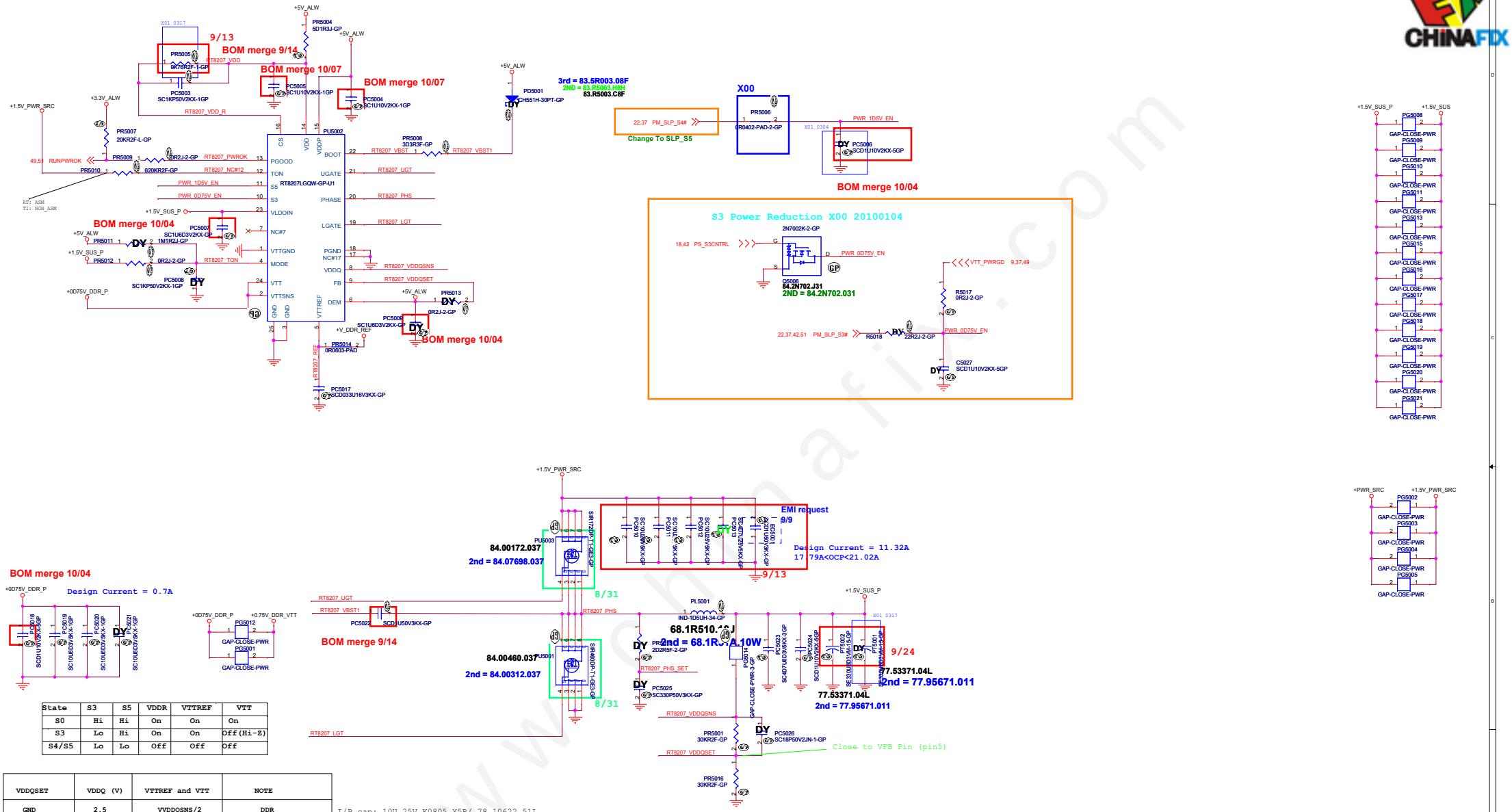
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218 +1.05V_VTT

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 49 of 100

SSID = PWR.Plane.Regulator_1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1.5U PCMC104T-1R5MH Cyntec 3.8mohm/4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U 2V EEFSX0D331ER 9mOhm 3Arms Panasonic/79.33719.L01
H/S: SIR172DP / 10.3mohm/12.4mOhm@4.5Vgs/ 84.00172.037
L/S: SIR460DP / 4.9mohm/6.1mOhm@4.5Vgs/ 84.00460.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

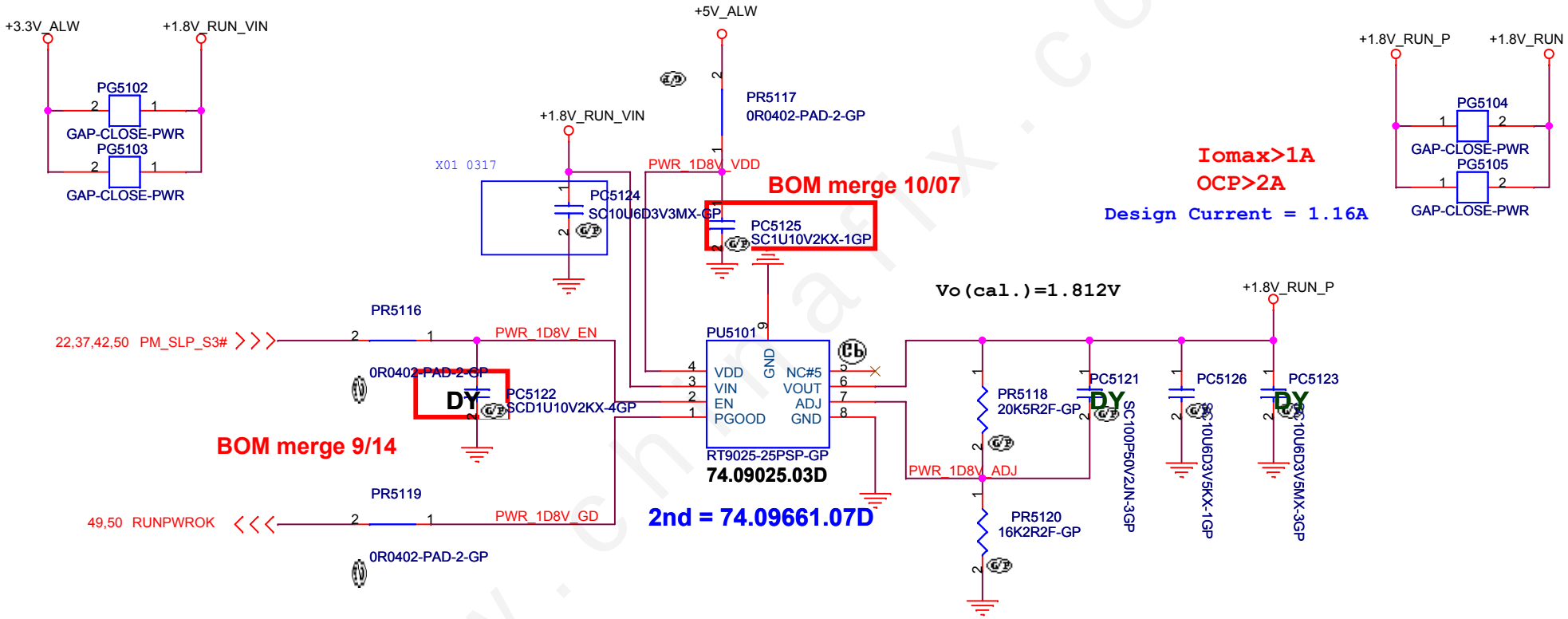
Title: RT8207 +1.5V_SUS

Size: A2 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 50 of 100

SSID = PWR.Plane.Regulator_1p8v

RT9025 for +1.8V_RUN



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT9025_+1.8V_RUN

Size	Document Number	Rev
A4	DV14 CP UMA+DIS	X00

Date: Wednesday, March 23, 2011 Sheet 51 of 100

(Blanking)

<Core Design>

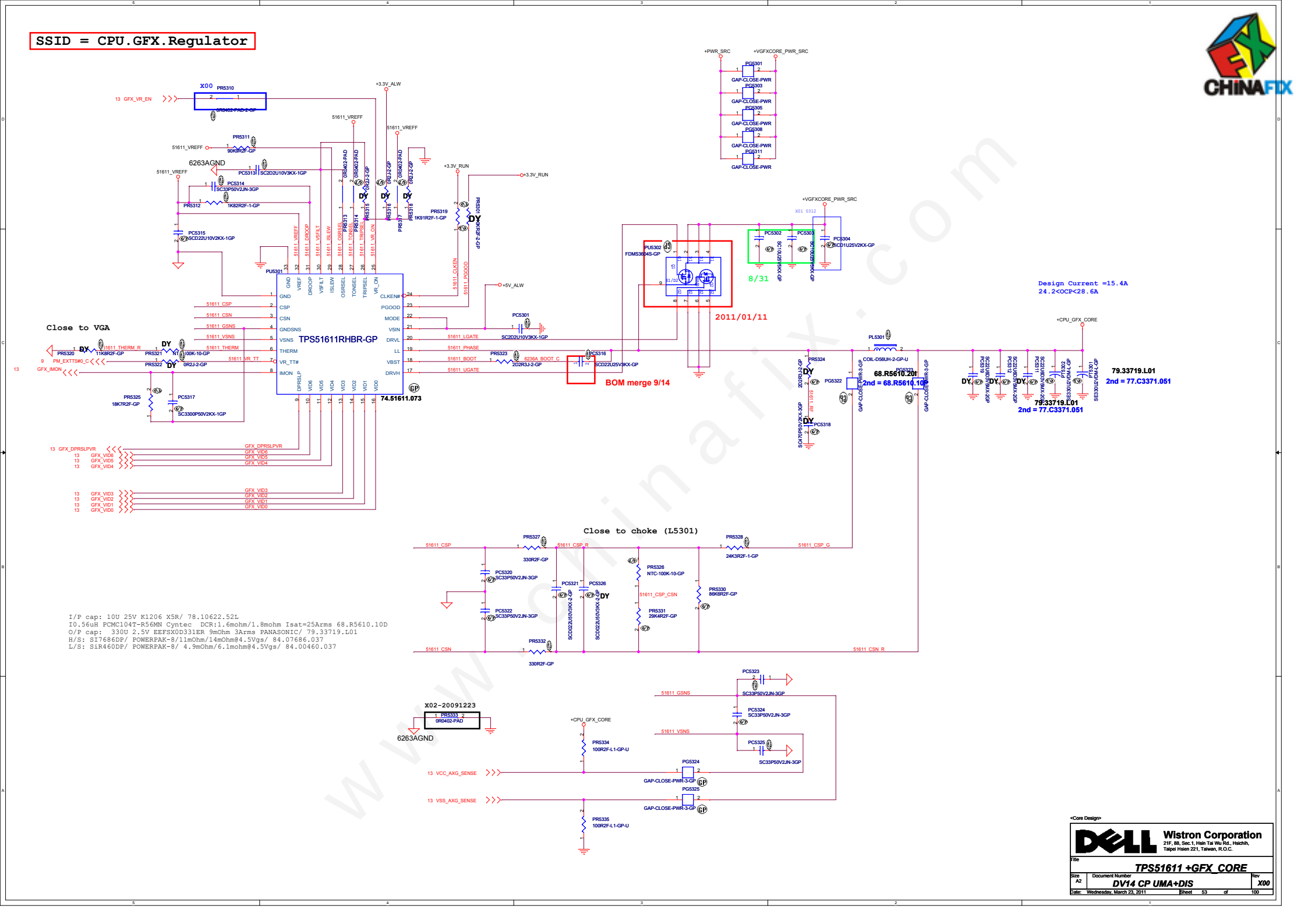
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*DV14 CP UMA+DIS*	*X00*

Date: Thursday, January 06, 2011 Sheet 52 of 100

SSID = CPU.GFX.Regulator



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51611 +GFX_CORE

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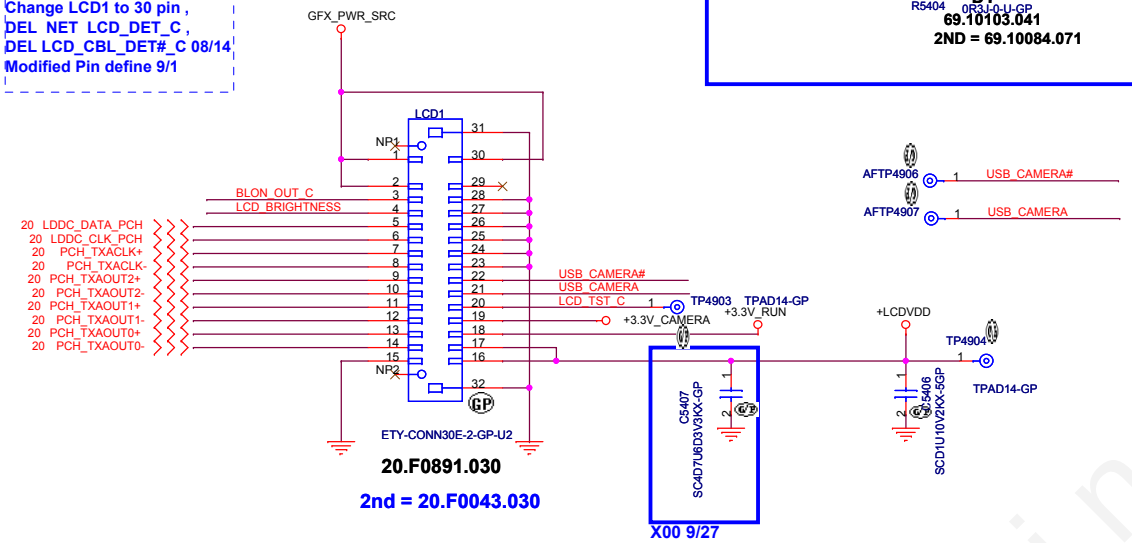
SSID = VIDEO

LVDS CONNECTOR

Change LCD1 to 30 pin ,
DEL NET LCD_DET_C ,
DEL LCD_CBL_DET#_C 08/14
Modified Pin define 9/1

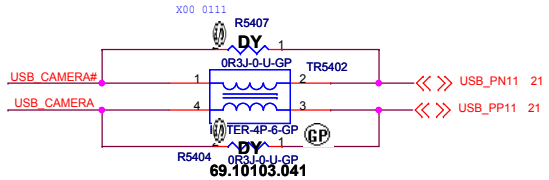


20.F0891.030

2nd = 20.F0043.030

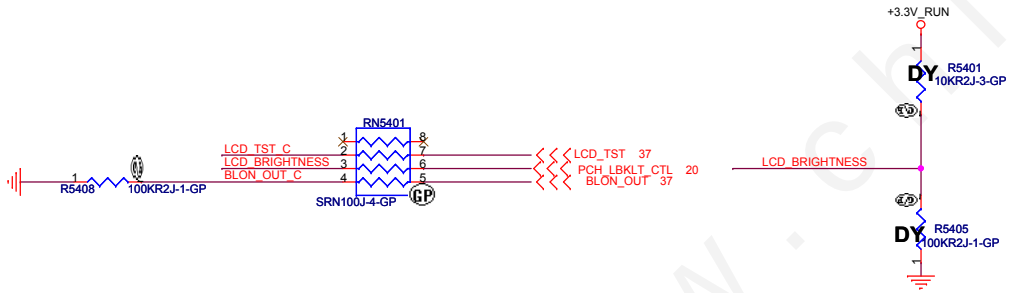
X00 9/27

EMI suggestion 9/23

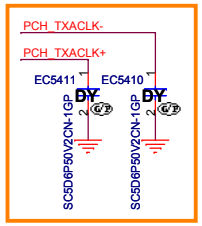


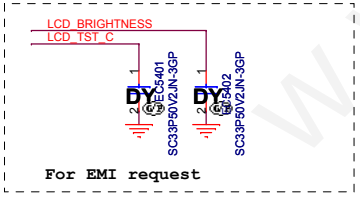
69.10103.041

2ND = 69.10084.071

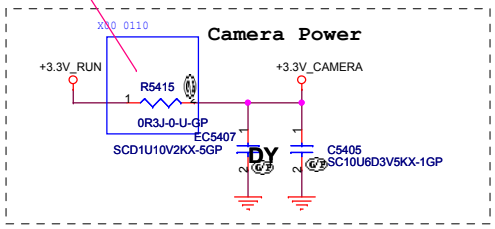


Close to LVDS connector



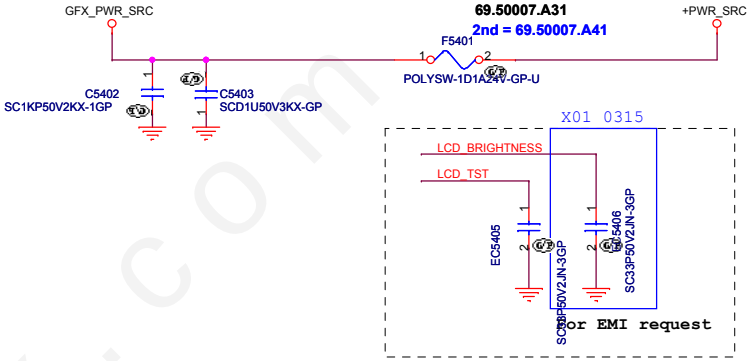


Note:R5415 cannot use short pad for safty



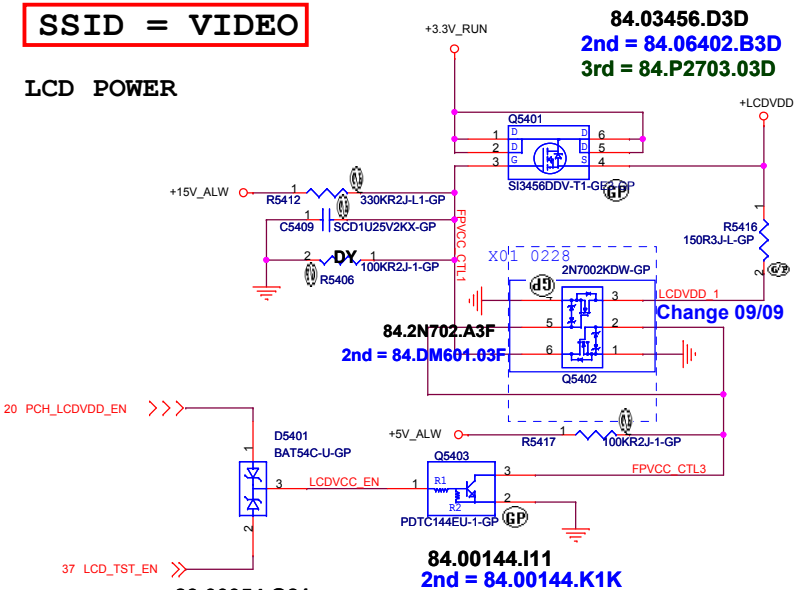
SSID = Inverter

INVERTER POWER



SSID = VIDEO

LCD POWER



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD/Inverter Connector

Size	Document Number	Rev
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SSID = VIDEO

X01 0228

+3.3V_RUN

20 PCH_CRT_DDCDATA

2N7002KDW-GP

CRT_DDCDATA_CON

Q5501

84.2N702.A3F

2nd = 84.DM601.03F

20 PCH_CRT_DDCCLK

CRT_DDCCLK_CON

5V_CRT_S0

RN5501 SRN2K2J-1-GP

CRT_DDCDATA_CON

CRT_DDCCLK_CON

C5514 SC22P50V2JN-4GP

C5513 SC22P50V2JN-4GP

5V_CRT_S0_R

X01 0308

CRT1

VCC_CRT

NC#4

NC#11

CRT_DDCDATA_CON

CRT_DDCCLK_CON

DDCDATA_ID1

DDCCLK_ID3

CHASSIS#16

CHASSIS#17

CRT_R

CRT_G

CRT_B

CRT_RED

CRT_GREEN

CRT_BLUE

GND

CRT_VSYNC_CON

CRT_HSYNC_CON

VSYNC

HSYNC

D-SUB-15-129-GP

AFTP509

20.20948.015

2nd = 20.20945.015

5V Tolerance

85 CRT_GFX_DDCDAT

85 CRT_GFX_DDCCLK

RN5506

DIS_CRT

SRN0J-6-GP

CRT_DDCDATA_CON

CRT_DDCCLK_CON

RN5507

20 PCH_CRT_BLUE

20 PCH_CRT_GREEN

20 PCH_CRT_RED

CRT_BLUE

CRT_GREEN

CRT_RED

SRN0J-7-GP

RN5505

85 CRT_GFX_R

85 CRT_GFX_G

85 CRT_GFX_B

AFTP501 5V_CRT_S0

AFTP502 CRT_DDCDATA_CON

AFTP503 CRT_DDCCLK_CON

AFTP504 CRT_R

AFTP505 CRT_G

AFTP506 CRT_B

AFTP507 CRT_HSYNC_CON

AFTP508 CRT_VSYNC_CON

C5518 SC33P50V2JN-3GP

C5517 SC33P50V2JN-3GP

Layout Note:

*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.

* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

A00

CRT_RED

CRT_GREEN

CRT_BLUE

L5501 68.00084.D61 2nd = 68.00217.991 3rd = 68.00213.021

L5502 68.00084.D61 2nd = 68.00217.991 3rd = 68.00213.021

L5503 68.00084.D61 2nd = 68.00217.991 3rd = 68.00213.021

BLM15BA330SS1D-GP

CRT_R

CRT_G

CRT_B

RN5503 SRN150F-1-GP

C5504 SC8P250V2CC-GP

C5505 SC8P250V2CC-GP

C5506 SC8P250V2CC-GP

C5507 SC10P50V2JN-4GP

C5508 SC10P50V2JN-4GP

C5509 SC10P50V2JN-4GP

X01

5V_CRT_S0

5V_CRT_S0_R

F5501 FUSE-1D1A6V-4GP-U

69.50007.691

2nd = 69.50007.771

D5502 CH551H-30PT-GP

83.R5003.C8F

2ND = 83.R5003.H8H

3rd = 83.5R003.08F

+5V_RUN

Hsync & Vsync level shift

C5512 SCD1U16V2KX-3GP

U5501A

U5501B

TSAHCT125PW-GP

CRT_HSYNC

CRT_VSYNC

HSYNC_5

VSYNC_5

RN5502 SRN33J-5-GP-U

CRT_HSYNC_CON

CRT_VSYNC_CON

X00 9/23

R5502 0R2J-2-GP

R5503 0R2J-2-GP

RN5508 SRN0J-6-GP

20 PCH_CRT_HSYNC

20 PCH_CRT_VSYNC

RN5509 SRN0J-6-GP

83,85 VGA_CRT_HSYNC

83,85 VGA_CRT_VSYNC

CLOSE TO TRANSFORMER

D5501 BAV99PT-GP-U

D5503 BAV99PT-GP-U

D5504 BAV99PT-GP-U

U5501C TSAHCT125PW-GP

U5501D TSAHCT125PW-GP

<Core Design>

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

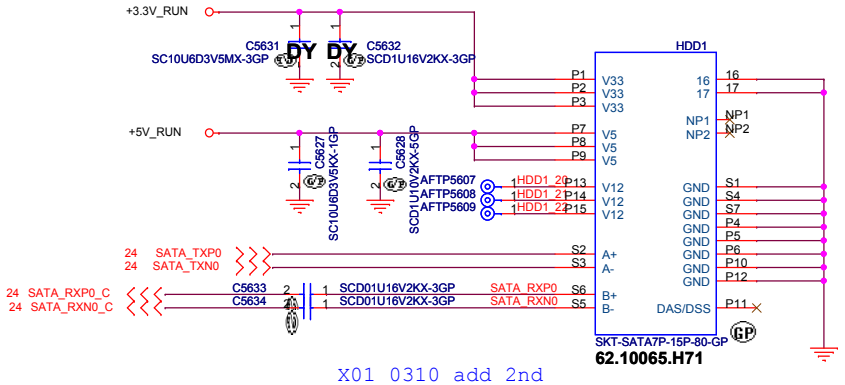
Title: CRT Connector

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 55 of 100

SSID = SATA

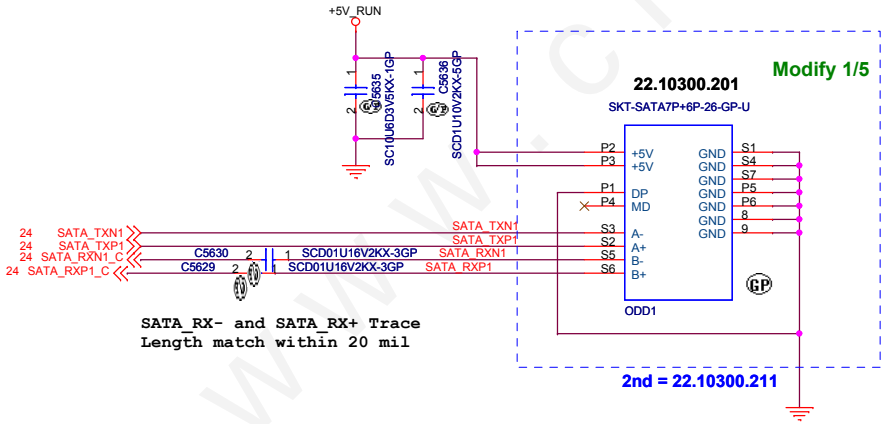
SATA HDD Connector



X01 0310 add 2nd

2nd = 62.10065.H81

SATA ODD Connector



SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

2nd = 22.10300.211

<Core Design>

Wistron Corporation
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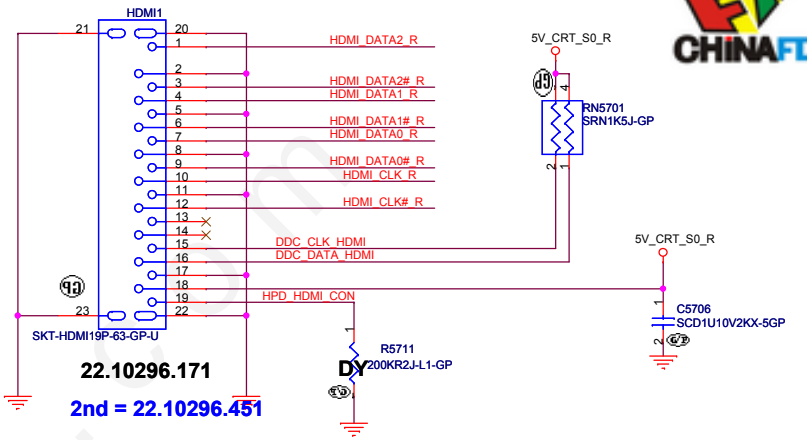
Taipei Hsien 221, Taiwan, R.O.C.

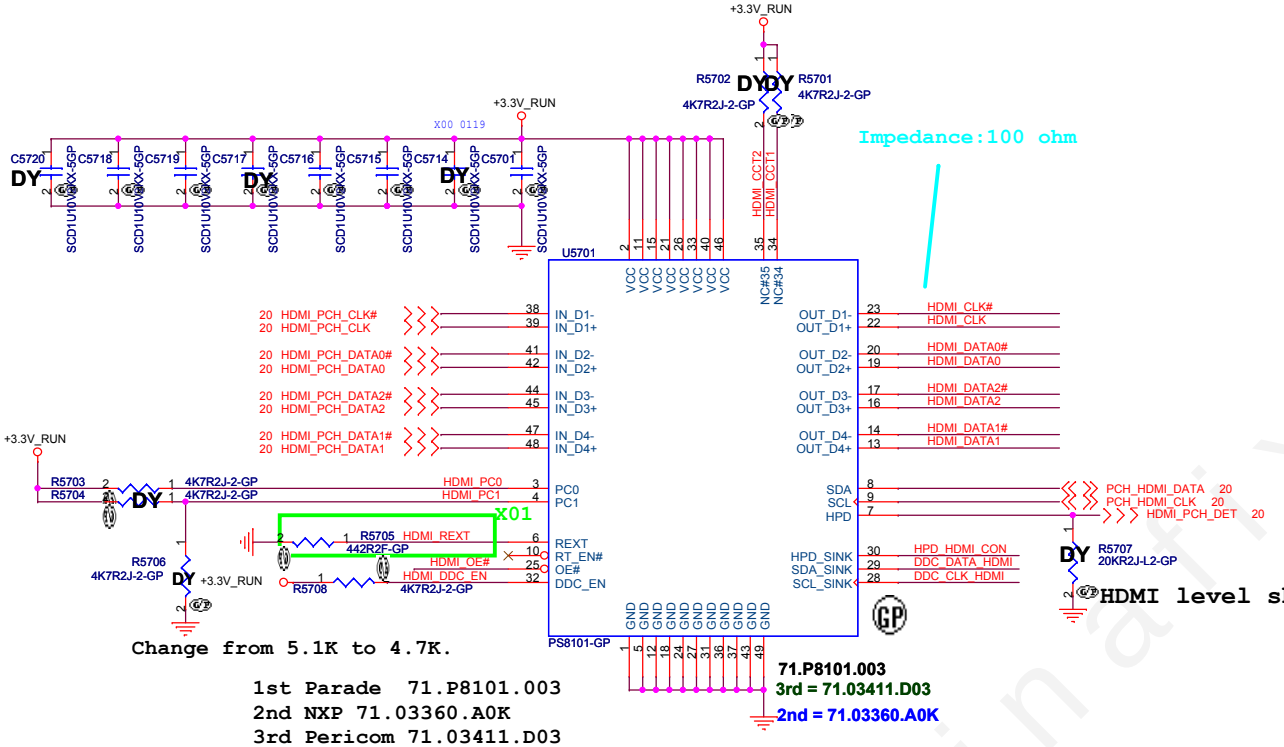
Title	HDD/ODD	
Size: A3	Document Number: DV14 CP UMA+DIS	Rev: X00
Date: Wednesday, March 23, 2011	Sheet 56 of 100	

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

HDMI CONN

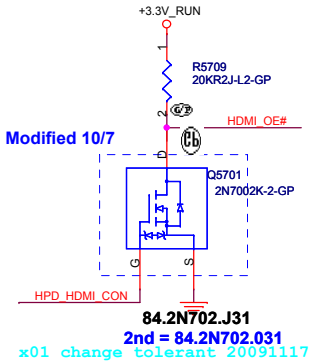


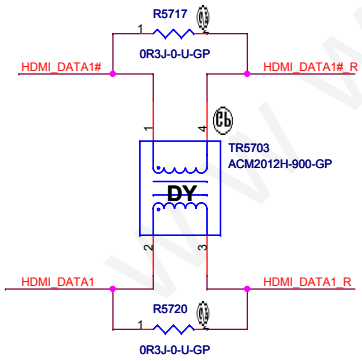


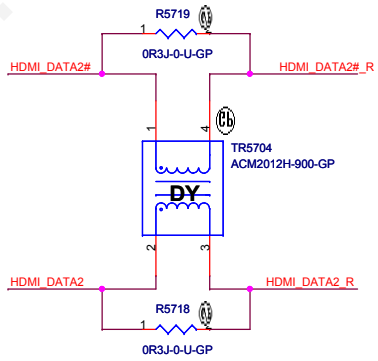
HDMI level shift circuit

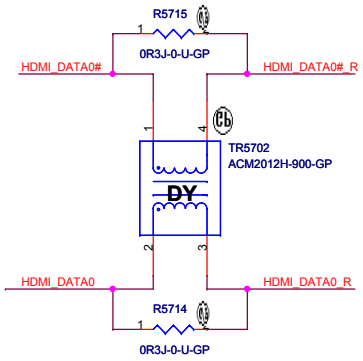
Change from 5.1K to 4.7K.

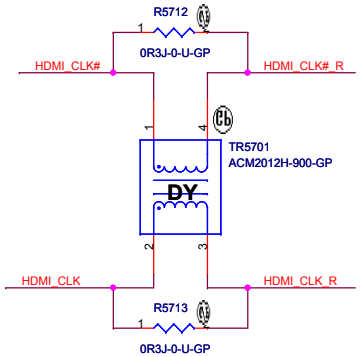
1st Parade 71.P8101.003
2nd NXP 71.03360.A0K
3rd Pericom 71.03411.D03











<Core Design>

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Title: HDMI Level Shift/ Connector

Size	Document Number	Rev
A3	DV14 CP UMA+DIS	X00

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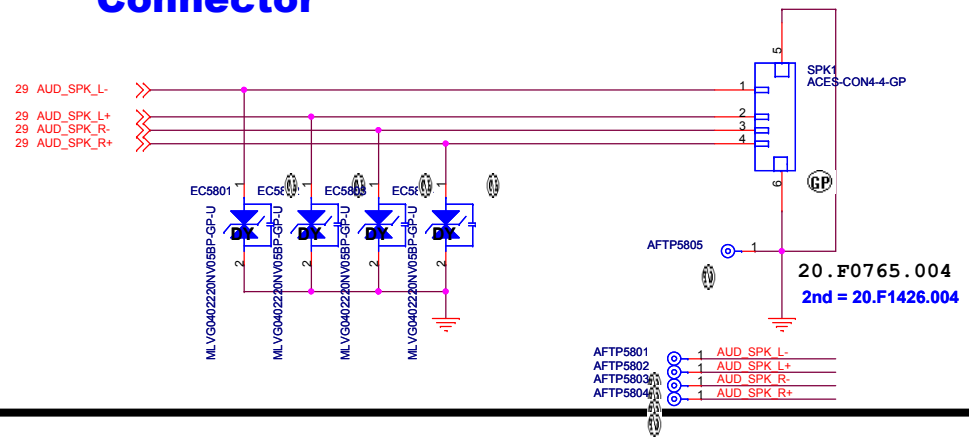
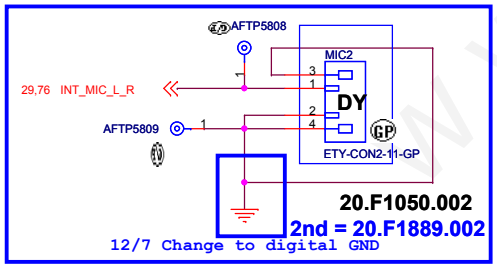
SSID = AUDIO

Speaker Connector



11/26 reserve MIC2

12/7 change MIC2 to 20.F1050.002 X01 0309



X01 0309
20.F1889.002 20.F1050.002

<Core Design>

Wistron Corporation
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Title: Audio Jack

Size	Document Number	Rev
A3	DV14 CP UMA+DIS	X00

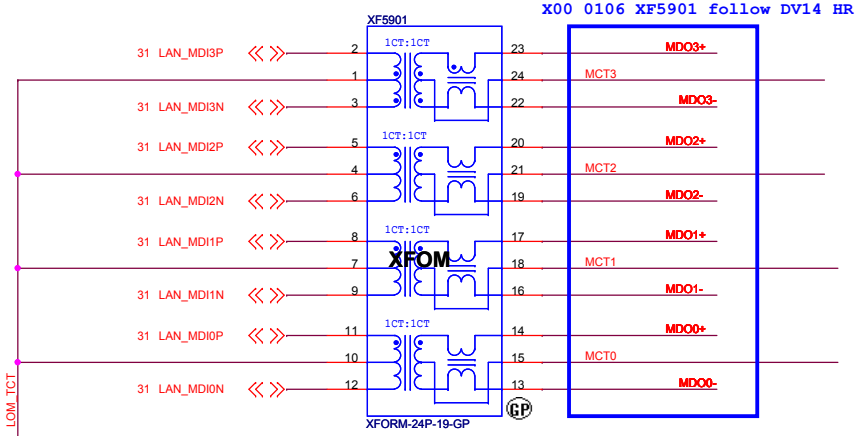
Date: Wednesday, March 23, 2011 Sheet 58 of 100

SSID = LOM

LAN TransFormer

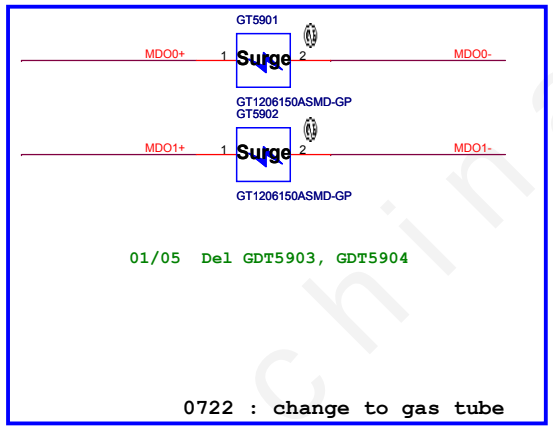
X01-0312
Add EMI solution for Surge

X00 0106 XF5901 follow DV14 HR



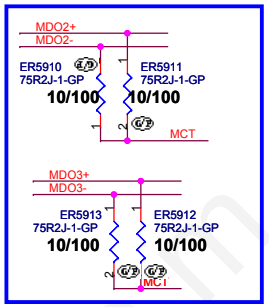
X00 0210
For GIGA LAN, use Transformer
68.IH601.301
For 10/100M LAN, use Transformer
68.HH035.301

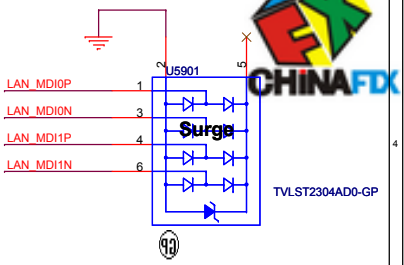
68.IH601.301
2nd = 68.05009.30A



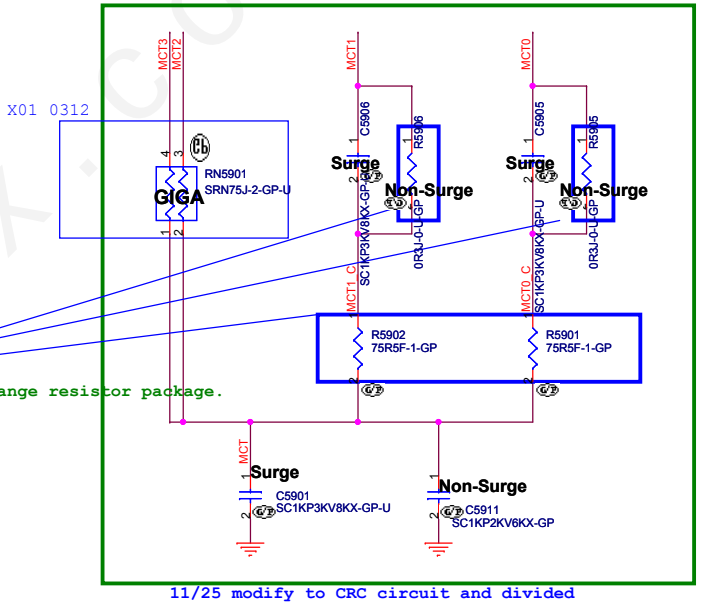
01/05 Del GDT5903, GDT5904

0722 : change to gas tube





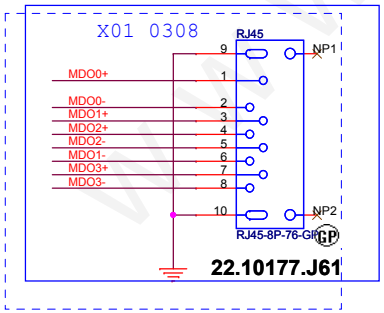
X00 20110105

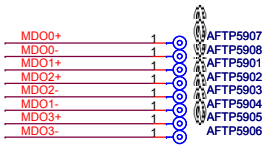


1/5 follow HR change resistor package.

11/25 modify to CRC circuit and divided resistor as EMI suggest
11/29 Change C5911 to 78.1022S.22L

RJ45





<Core Design>

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Title: LAN CONN
Size: A3
Document Number: DV14 CP UMA+DIS
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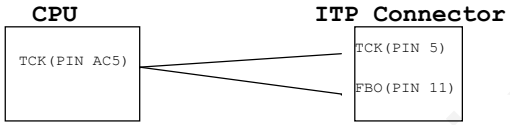
Date: Wednesday, March 23, 2011
Sheet 59 of 100

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



<Core Design>

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Title: ITP/Fan Connector

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, January 12, 2011 | Sheet 60 of 100

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<Core Design>

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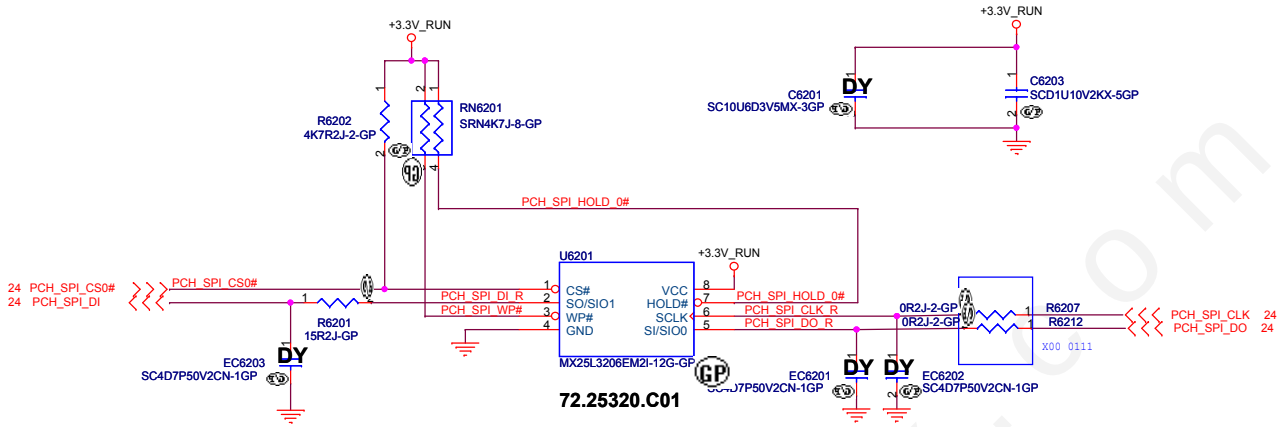
Title: *Reseved*

Size: A3 | Document Number: *DV14 CP UMA+DIS* | Rev: *X00*

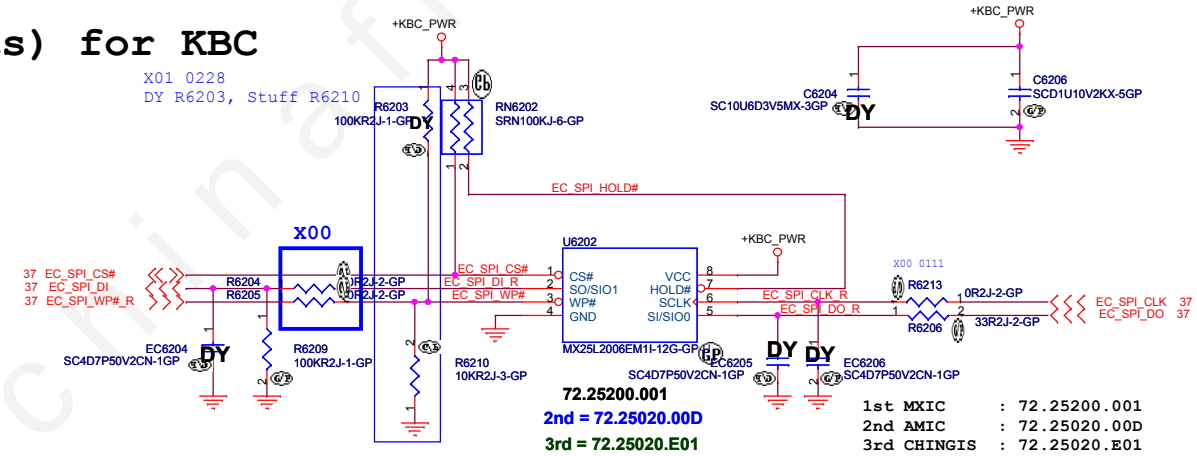
Date: Thursday, January 06, 2011 | Sheet 61 of 100

SSID = Flash.ROM

SPI FLASH ROM (32M bits) for PCH

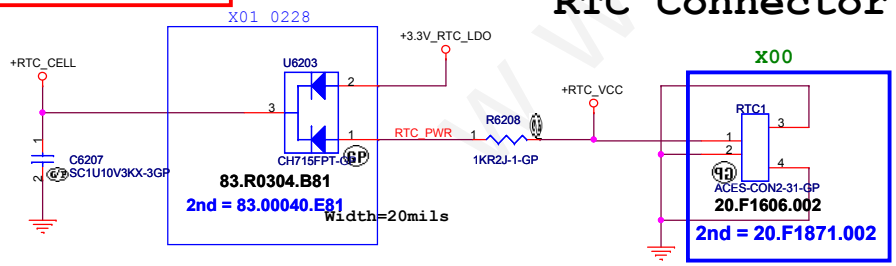


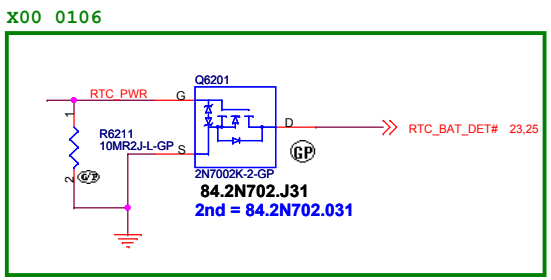
SPI FLASH ROM (2M bits) for KBC



SSID = RBATT

RTC Connector





<Core Design>

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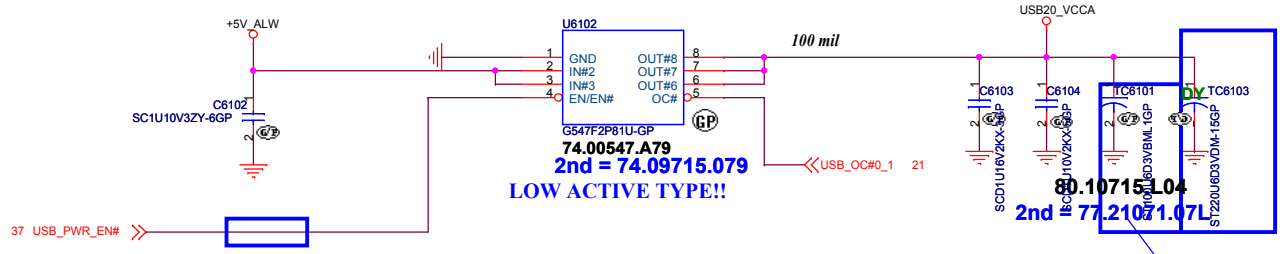
Title: Flash/RTC

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

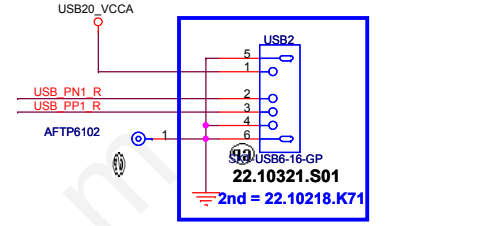
Date: Wednesday, March 23, 2011 | Sheet 62 of 100

SSID = USB

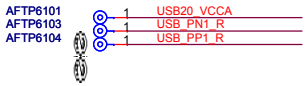


11/30 Add TC6103

12/22 change TC6101 to 100uF

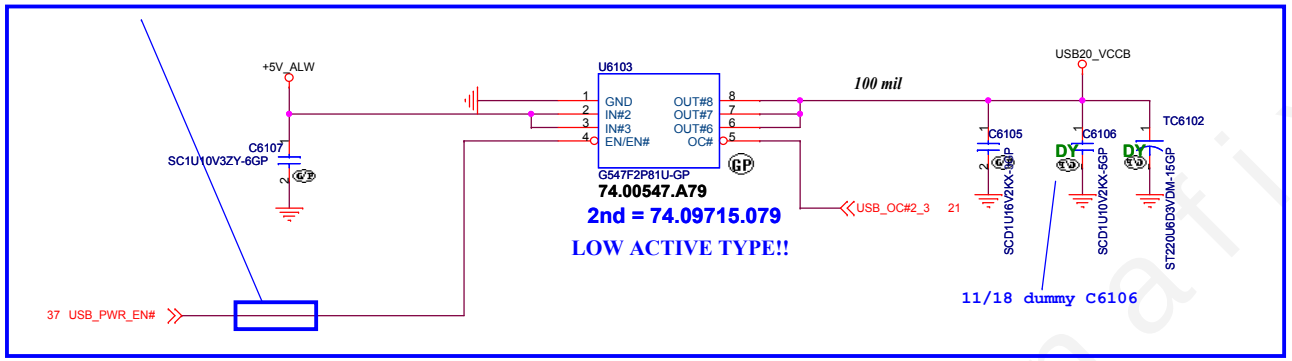


11/29 change USB2 to 22.10321.S01



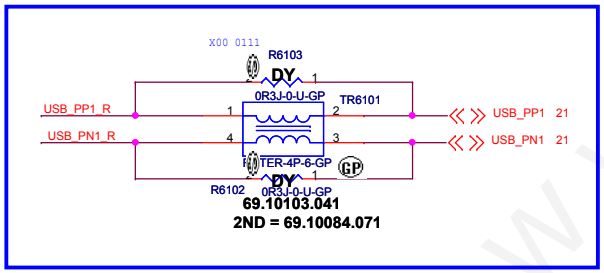
11/18 remove R6101, R6104

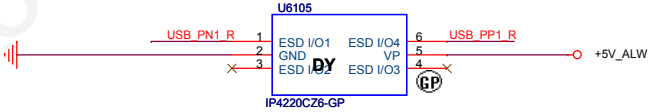
11/10 Move USB power SW to Mainboard



11/18 dummy C6106

11/1 Stuff TR6101 for EMI





<Core Design>

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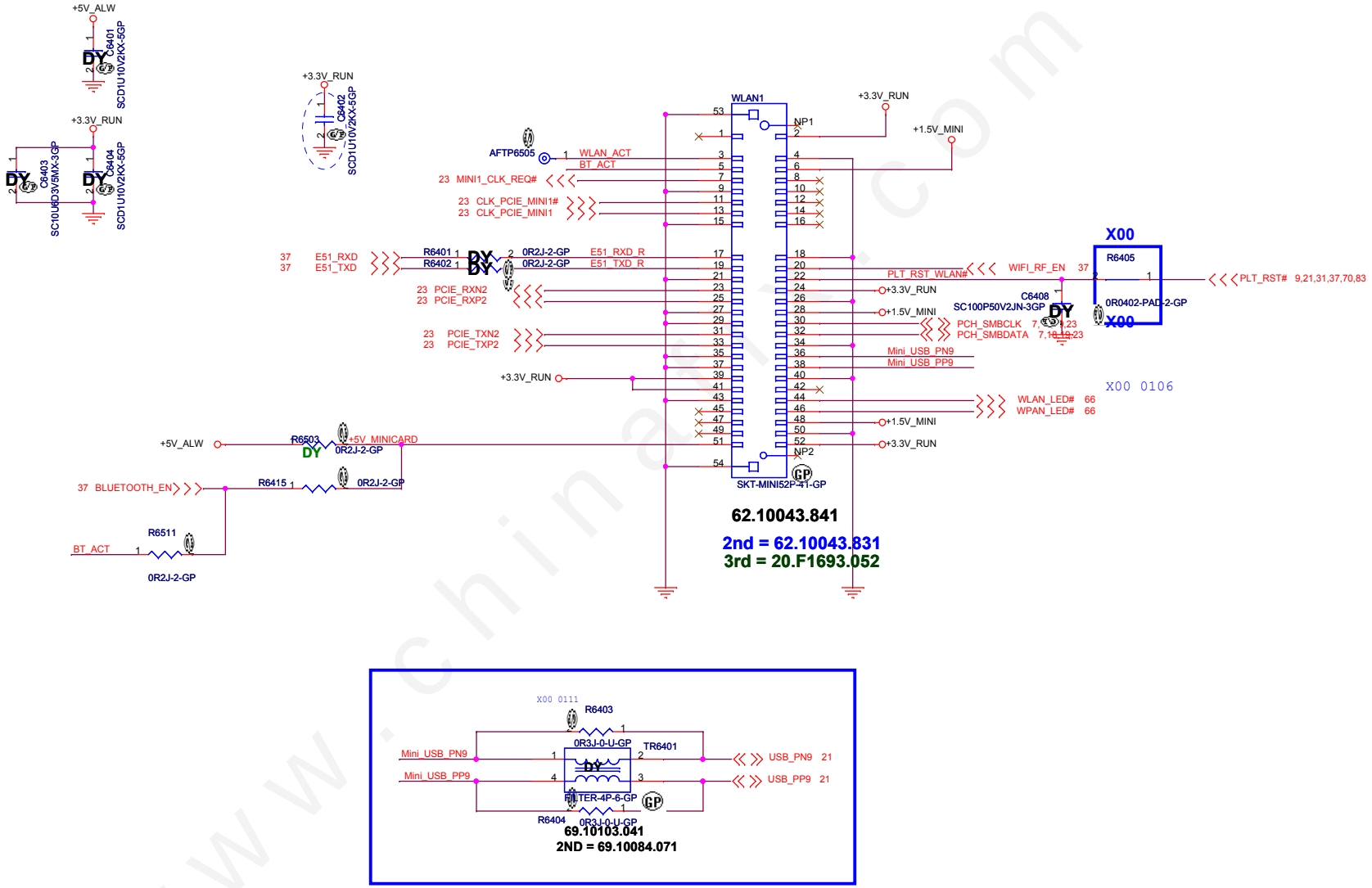
Title: USB

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 63 of 100

SSID = Wireless

Mini Card Connector(802.11a/b/g)



<Core Design>

EMI suggestion 7/27

Wistron Corporation
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Title	MINICARD	
Size A3	Document Number DV14 CP UMA+DIS	Rev X00
Date: Wednesday, March 23, 2011	Sheet 64 of 100	

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<Core Design>

Wistron Corporation
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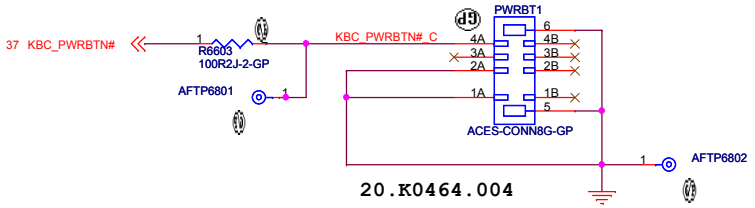
Title: Reserved

Size	Document Number	Rev
A3	DV14 CP UMA+DIS	X00

Date: Thursday, January 06, 2011 Sheet 65 of 100

SSID = User.Interface

Power BTN Connector



20.K0464.004

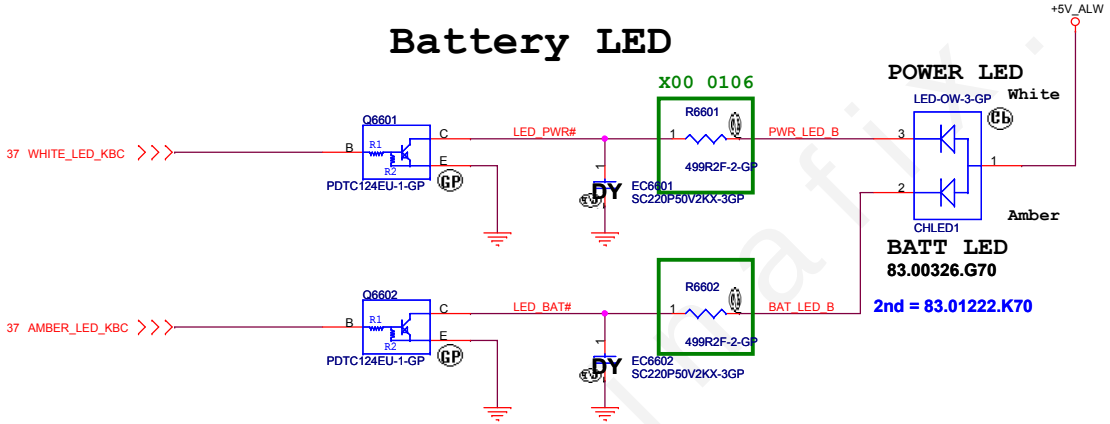
2nd = 20.K0341.004

12/10 change PWRBT1 pin define

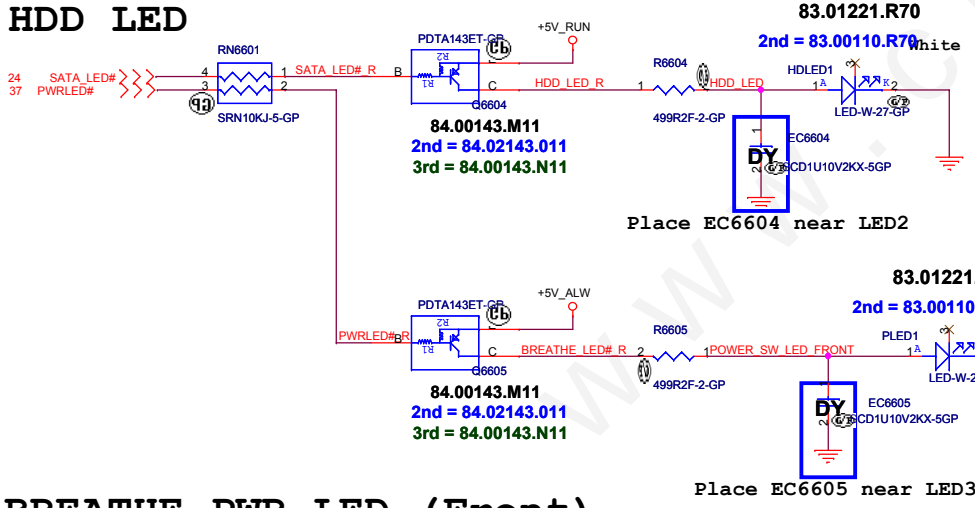
12/21 change PWRBT1 to 20.K0464.004

Modify 09/02

Battery LED

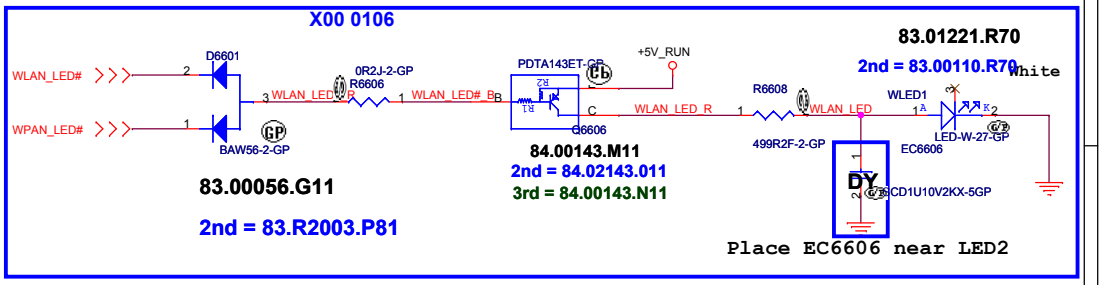


HDD LED



BREATHE PWR LED (Front)

WLAN LED



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PWR_BTN/LED	
Size A3	Document Number DV14 CP UMA+DIS	Rev X00
Date: Wednesday, March 23, 2011	Sheet 66 of 100	

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

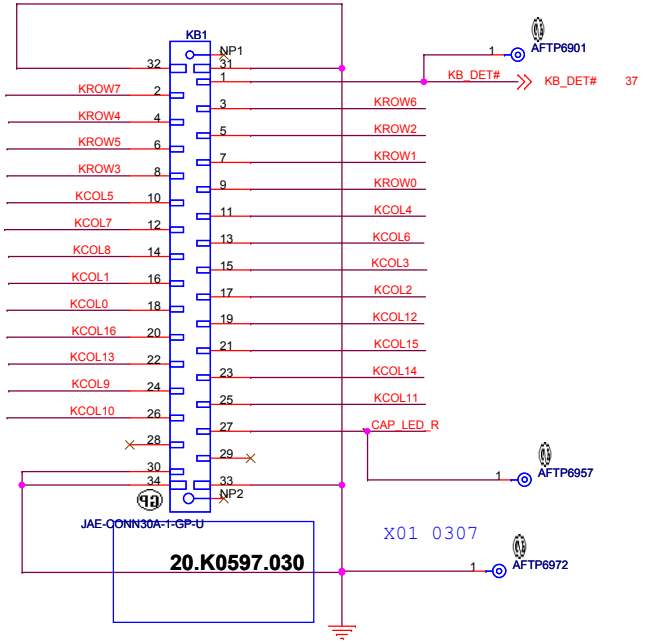
Title: Reserved

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Thursday, January 06, 2011 | Sheet 67 of 100

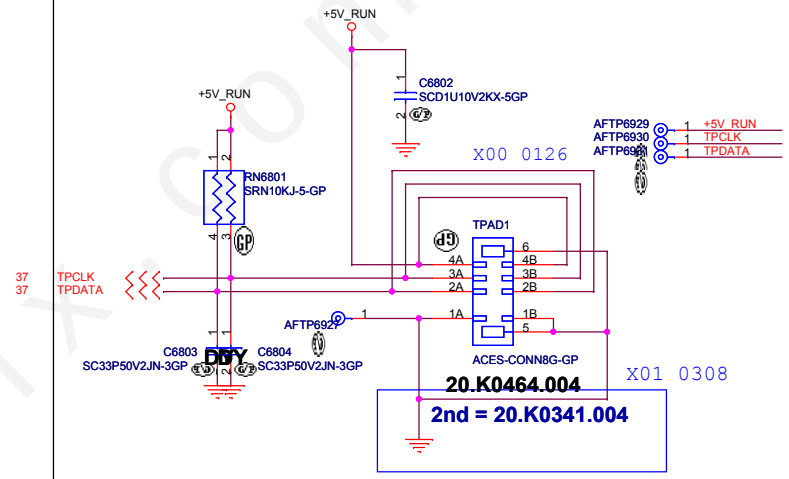
SSID = KBC

Internal KeyBoard Connector



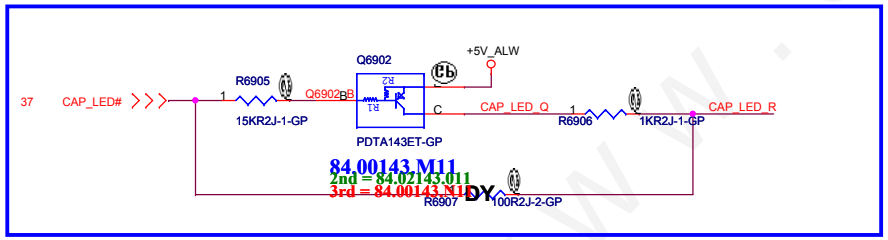
SSID = Touch.Pad

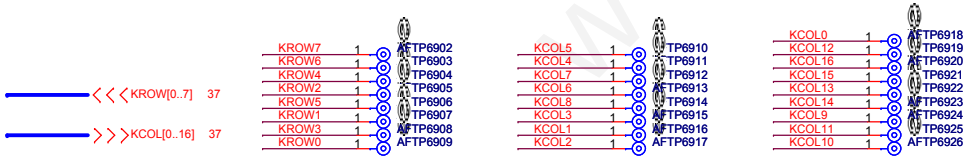
TouchPad Connector



12/8 Add Cap LED control circuit

CAP LED CONTROL





11/23 change TPAD1 to 20.K0320.004

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

Size	Document Number	Rev
A3	DV14 CP UMA+DIS	X00

Date: Wednesday, March 23, 2011 Sheet 68 of 100

SSID = User.Interface

<Core Design>

Wistron Corporation
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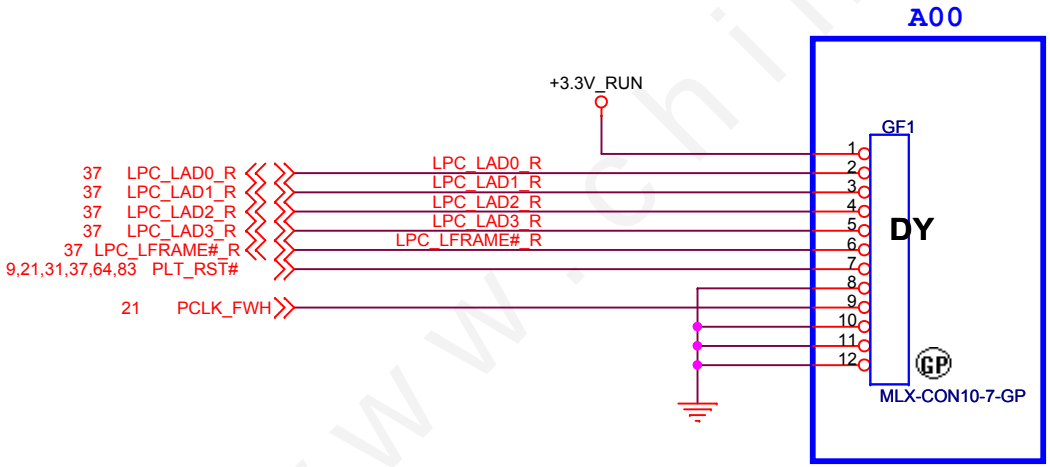
Title

Hall Sensor

Size	Document Number	Rev
A4	DV14 CP UMA+DIS	X00

Date: Monday, January 10, 2011 Sheet 69 of 100

SSID = User.Interface



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Reserved***

Size	Document Number	Rev
A4	***DV14 CP UMA+DIS***	***X00***

Date: Wednesday, March 23, 2011 Sheet 70 of 100

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *DV14 CP UMA+DIS* | Rev: *X00*

Date: Thursday, January 06, 2011 | Sheet 71 of 100

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<Core Design>

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Title: RESERVED

Size	Document Number	Rev
A3	DV14 CP UMA+DIS	X00

Date: Thursday, January 06, 2011 Sheet 72 of 100

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<Core Design>

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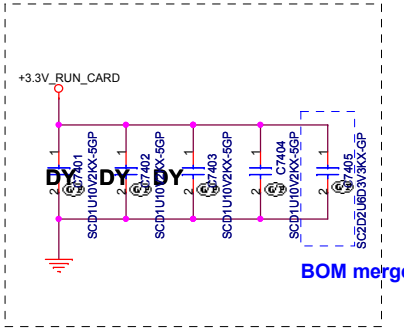
Title: *Reserved*

Size	Document Number	Rev
A3	*DV14 CP UMA+DIS*	*X00*

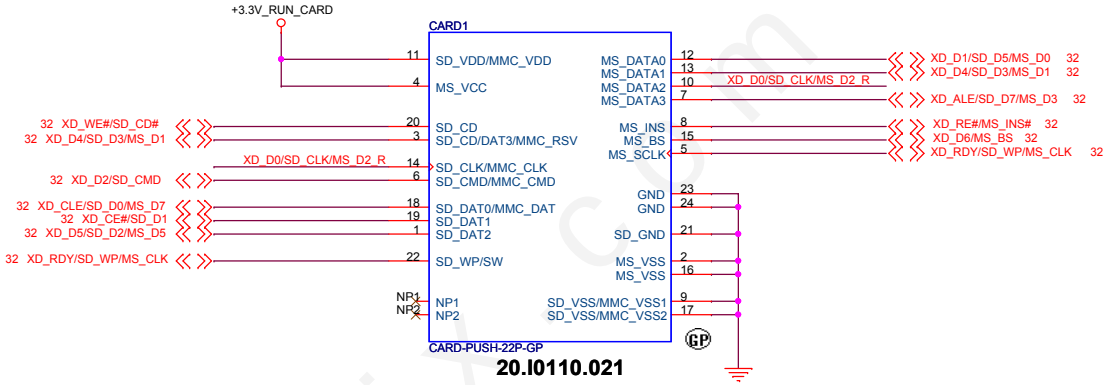
Date: Thursday, January 06, 2011 Sheet 73 of 100

SSID = SDIO

SD/XD/MS Card Reader



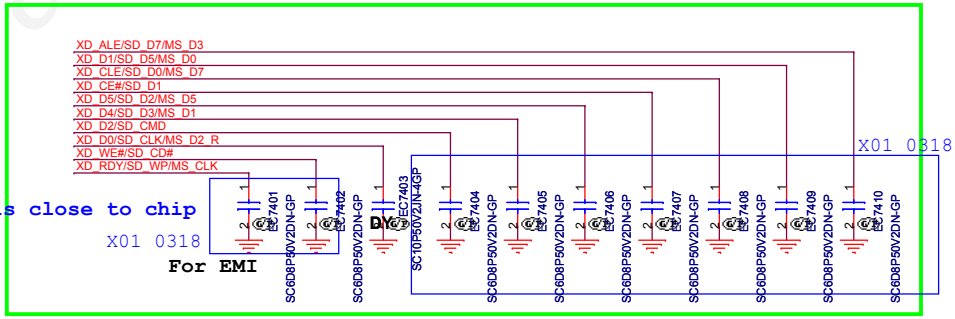
BOM merge Change 09/09

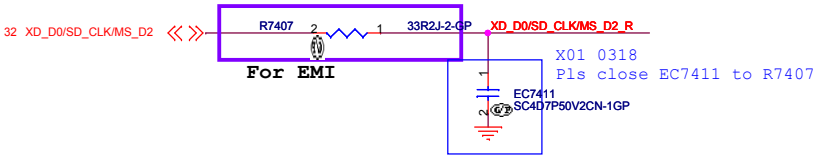


20.I0110.021

2nd = 20.I0133.001

0810 Vendor Recommand





<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title		
Reserved		
Size: A3	Document Number: DV14 CP UMA+DIS	Rev: X00
Date: Wednesday, March 23, 2011	Sheet 74 of 100	

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<Core Design>

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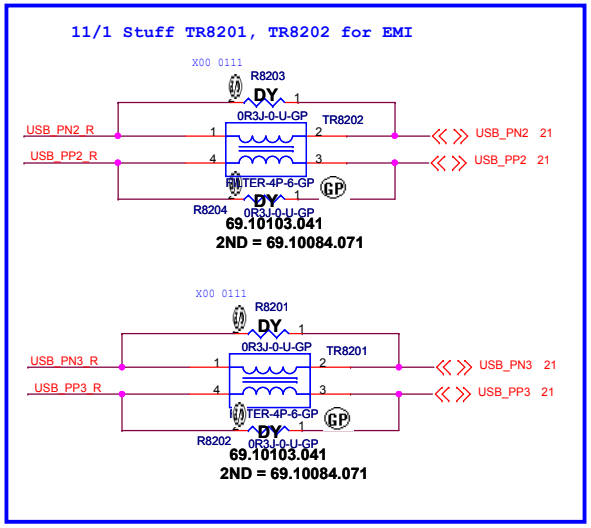
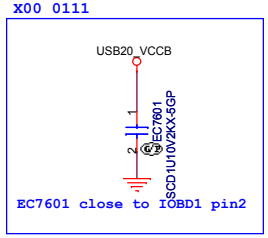
Title: Reserved

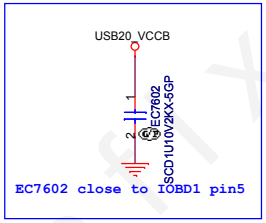
Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

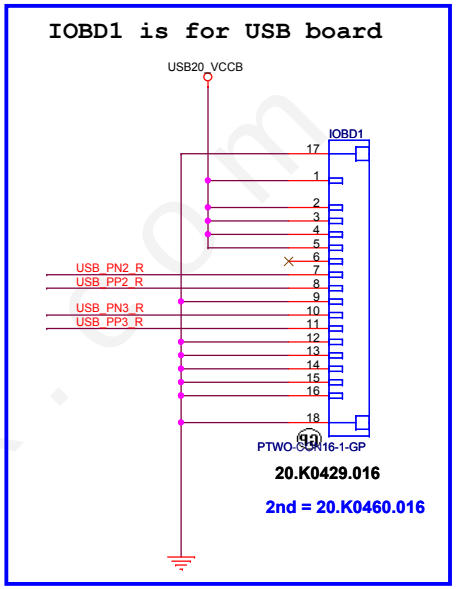
Date: Thursday, January 06, 2011 | Sheet 75 of 100

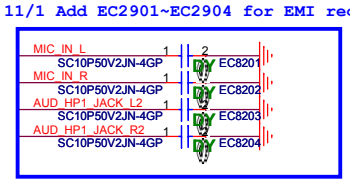
SSID = User.Interface

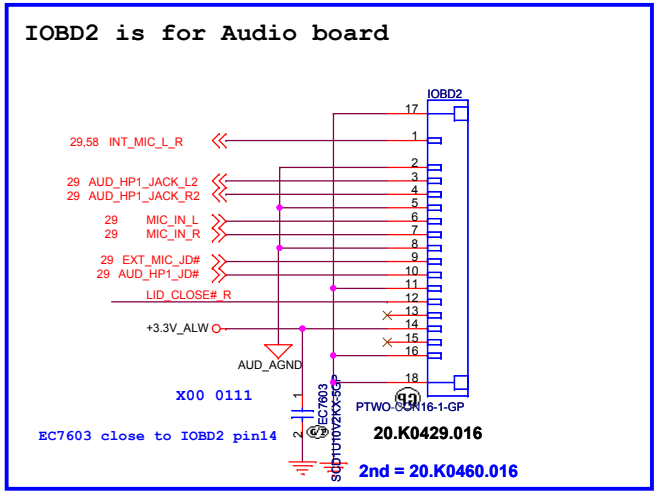


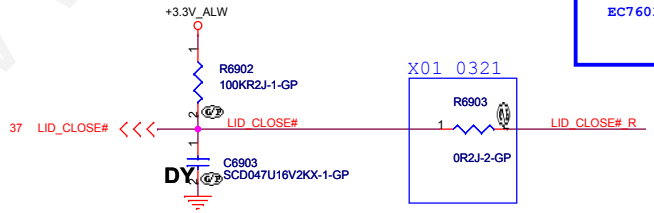












<Core Design>

Wistron Corporation
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Title: IO Board

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 76 of 100

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<Core Design>

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Title: *Reserved*

Size	Document Number	Rev
A3	*DV14 CP UMA+DIS*	*X00*

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<Core Design>

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Title: *Reserved*

Size: A3 | Document Number: *DV14 CP UMA+DIS* | Rev: *X00*

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SSID = Mechanical

H1 HT85BE85R29-U-5-GP
H2 HOLE256R115-GP
H3 HT85BE85R29-U-5-GP
H4 HT85BE85R29-U-5-GP
H5 HT85BE85R29-U-5-GP
H6 HT85BE85R29-U-5-GP
H7 HT85B95X975R29-S-GP

X01 0316
SPR4 SPRING-13-GP-U
34.43E24.001

For CPU BRACKET
H8 HOLE197R166-1-GP
H9 HOLE197R166-1-GP
H10 HOLE197R166-1-GP

VGA Stand-Off
H11 STF237R117H83-1-GP DIS
34.4CK01.001

PCH Stand-Off
H12 STF237R117H83-1-GP
H13 STF237R117H83-1-GP
X01 0308
34.4CK01.001
34.4CK01.001

X01 0315
SPR1 SPRING-58-GP
34.4B312.002
SPR2 SPRING-62-GP
34.39S07.003

X00 0126
+1.05V_VTT +3.3V_ALW +3.3V_ALW +3.3V_ALW +3.3V_ALW +3.3V_ALW +3.3V_ALW +3.3V_ALW +3.3V_ALW +3.3V_ALW +3.3V_ALW +5V_ALW +5V_ALW
DY EC7970 SCD1U10V2KX-5GP
DY EC7971 SCD1U10V2KX-5GP
DY EC7972 SCD1U10V2KX-5GP
DY EC7973 SCD1U10V2KX-5GP
DY EC7974 SCD1U10V2KX-5GP
DY EC7975 SCD1U10V2KX-5GP
DY EC7976 SCD1U10V2KX-5GP
DY EC7977 SCD1U10V2KX-5GP
DY EC7978 SCD1U10V2KX-5GP
DY EC7979 SCD1U10V2KX-5GP
DY EC7980 SCD1U10V2KX-5GP
DY EC7981 SCD1U10V2KX-5GP
X01 0312

Add 9/27
EC7964 DY SCD1U10V2KX-5GP AUD_AGND
EC7965 DY SCD1U10V2KX-5GP AUD_AGND
EC7966 DY SCD1U10V2KX-5GP AUD_AGND
X01 0312
+PWR_SRC EC7965 SCD1U25V2KX-GP

Modified 8/24
Add 9/16
X01 0312
+PWR_SRC EC7901 SCD1U25V2KX-GP
EC7902 SCD1U25V2KX-GP
EC7903 SCD1U25V2KX-GP
EC7904 SCD1U25V2KX-GP
EC7905 SCD1U25V2KX-GP
EC7906 SCD1U25V2KX-GP
EC7907 SCD1U25V2KX-GP
EC7929 SCD1U25V2KX-GP
EC7930 SCD1U25V2KX-GP
EC7931 SCD1U25V2KX-GP
EC7932 SCD1U25V2KX-GP
EC7933 SCD1U25V2KX-GP
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EC7940 SCD1U25V2KX-GP
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EC7942 SCD1U25V2KX-GP
EC7943 SCD1U25V2KX-GP
EC7944 SCD1U25V2KX-GP
EC7945 SCD1U25V2KX-GP
EC7946 SCD1U25V2KX-GP
EC7947 SCD1U25V2KX-GP

+5V_RUN +5V_RUN +5V_RUN +5V_RUN +5V_RUN +5V_RUN
DY EC7908 SCD1U10V2KX-5GP
DY EC7909 SCD1U10V2KX-5GP
DY EC7910 SCD1U10V2KX-5GP
DY EC7911 SCD1U10V2KX-5GP
DY EC7982 SCD1U10V2KX-5GP
DY EC7983 SCD1U10V2KX-5GP
X00 0126

Add 9/16
+1.5V_SUS +1.5V_SUS +1.5V_SUS +1.5V_SUS +1.5V_SUS +1.5V_SUS +1.5V_SUS +1.5V_SUS +1.5V_SUS +1.5V_SUS +1.5V_SUS +1.5V_SUS
DY EC7952 SCD1U10V2KX-5GP
DY EC7953 SCD1U10V2KX-5GP
DY EC7954 SCD1U10V2KX-5GP
DY EC7955 SCD1U10V2KX-5GP
DY EC7956 SCD1U10V2KX-5GP
DY EC7957 SCD1U10V2KX-5GP
EC7958 SCD1U10V2KX-5GP
EC7959 SCD1U10V2KX-5GP
DY EC7960 SCD1U10V2KX-5GP
EC7961 SCD1U10V2KX-5GP
X01 0312

Add 9/23
+1.5V_SUS
DY EC7966 SCD1U10V2KX-5GP
+1.5V_SUS EC7987 SCD1U10V2KX-5GP
X01 0312
EC7985 near 5969.49 5620.99

Add 9/16
+3.3V_RUN +3.3V_RUN +3.3V_RUN +3.3V_RUN +3.3V_RUN +3.3V_RUN +3.3V_RUN +3.3V_RUN +3.3V_RUN +3.3V_RUN
DY EC7912 SCD1U10V2KX-5GP
DY EC7913 SCD1U10V2KX-5GP
DY EC7914 SCD1U10V2KX-5GP
DY EC7915 SCD1U10V2KX-5GP
DY EC7916 SCD1U10V2KX-5GP
DY EC7917 SCD1U10V2KX-5GP
DY EC7918 SCD1U10V2KX-5GP
DY EC7919 SCD1U10V2KX-5GP
DY EC7920 SCD1U10V2KX-5GP
DY EC7962 SCD1U10V2KX-5GP

+3.3V_RUN
DY EC7984 SCD1U10V2KX-5GP
X00 0126

Add 9/16
+1.05V_VTT +1.05V_VTT +1.05V_VTT +1.05V_VTT
DY EC7948 SCD1U10V2KX-5GP
DY EC7949 SCD1U10V2KX-5GP
DY EC7950 SCD1U10V2KX-5GP
DY EC7951 SCD1U10V2KX-5GP

+1.5V_SUS
EC7986 SCD1U10V2KX-5GP
X01 0312
EC7985 near 5270.66 5222.88

+1.5V_SUS
EC7988 SCD1U10V2KX-5GP
X01 0312
EC7985 near 6101.25 5812.89

+3.3V_ALW +5V_ALW +5V_ALW +5V_ALW +5V_ALW +5V_ALW +5V_ALW +DC_IN
DY EC7921 SCD1U10V2KX-5GP
DY EC7922 SCD1U10V2KX-5GP
DY EC7923 SCD1U10V2KX-5GP
DY EC7924 SCD1U10V2KX-5GP
DY EC7925 SCD1U10V2KX-5GP
DY EC7926 SCD1U10V2KX-5GP
DY EC7927 SCD1U10V2KX-5GP
DY EC7928 SCD1U25V2KX-GP

Modified 8/24

Add 9/16
+3.3V_ALW +3.3V_ALW
DY EC7963 SCD1U10V2KX-5GP
DY EC7964 SCD1U10V2KX-5GP

+1.5V_SUS
EC7985 SCD1U10V2KX-5GP
X01 0312
EC7985 near 6167.13 5283.03

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: UNUSED PARTS/EMI Capacitors
Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00
Date: Tuesday, March 22, 2011 | Sheet 79 of 100

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Reserved*

Size	Document Number	Rev
A3	DV14 CP UMA+DIS	X00

Date: Thursday, January 06, 2011 Sheet 80 of 100

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<Core Design>

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Title: Reserved

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Thursday, January 06, 2011 | Sheet 81 of 100

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<Core Design>

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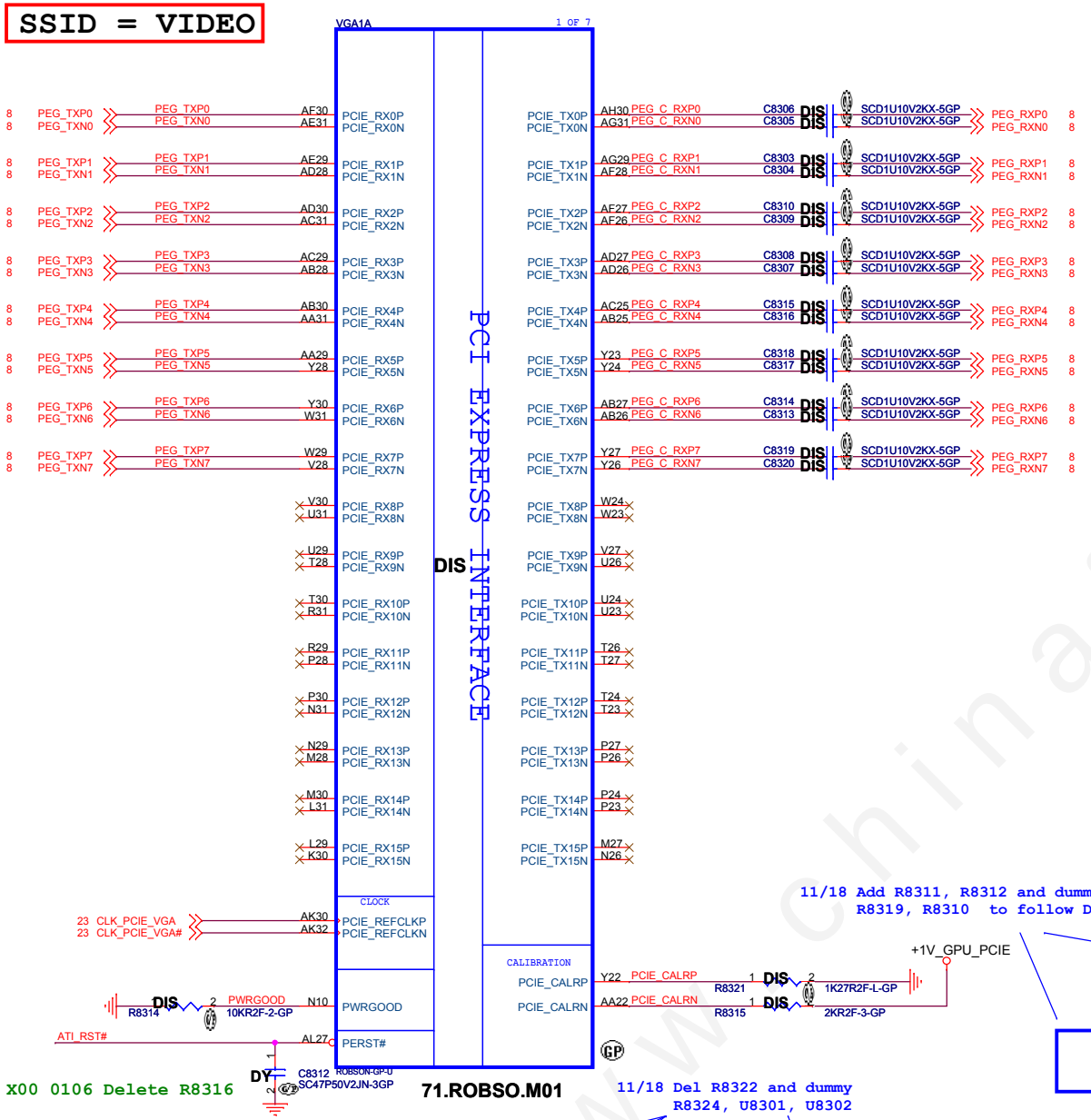
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: DV14 CP UMA+DIS | Rev: X00

Date: Thursday, January 06, 2011 | Sheet 82 of 100

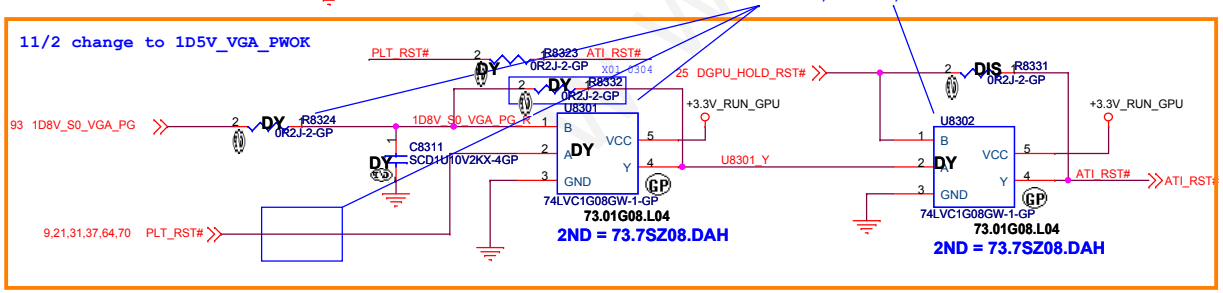
SSID = VIDEO



X00 0106 Delete R8316

11/18 Add R8311, R8312 and dummy R8319, R8310 to follow DN13

11/18 Del R8322 and dummy R8324, U8301, U8302



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

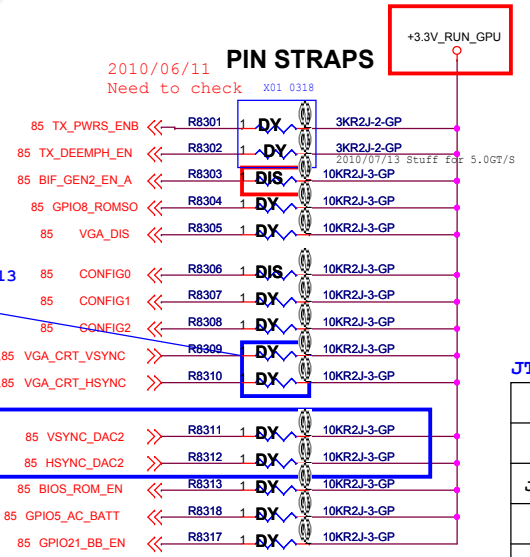
RECOMMENDED SETTINGS:
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

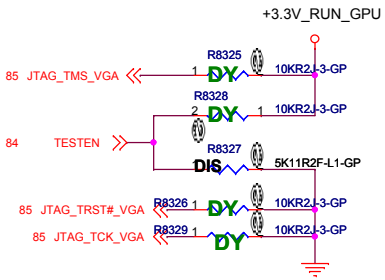
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND SETTING: PLATFORM	RECOMMEND SETTING: ASIC
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
GPIO8_ROMSO	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
GPIO21_BB_EN	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

2010/06/11

PIN STRAPS

2010/06/11 Need to check X01 0318





JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC

PE_GPIO0	
dGPU mode	H
IGPU	L
IGPU with BACO	H

<Core Design>

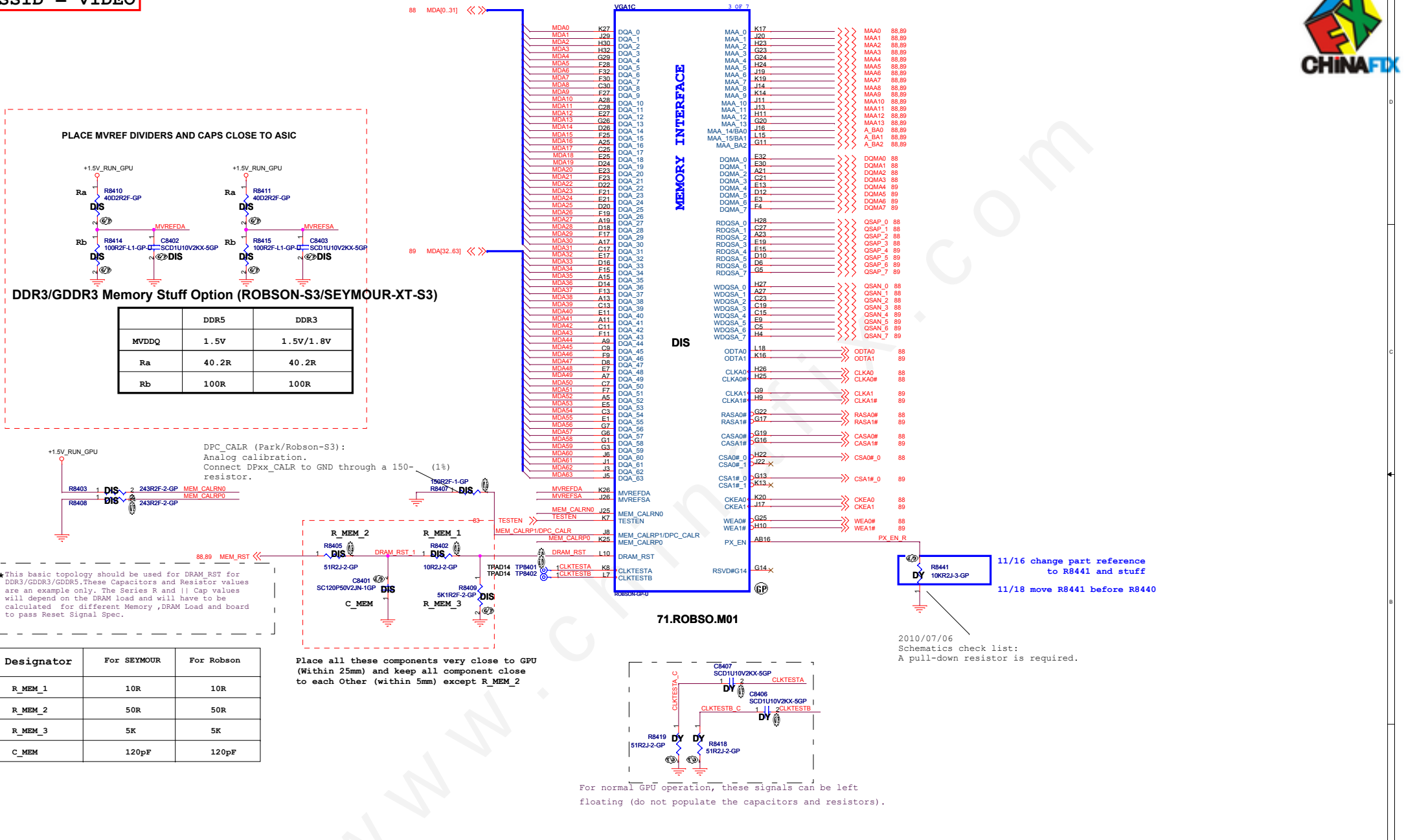
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU_PCIE/STRAPPING(1/5)

Size: A3 | Document Number: Enrico Caruso 14 | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 83 of 100

SSID = VIDEO



** This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Designator	For SEYMOUR	For Robson
R_MEM_1	10R	10R
R_MEM_2	50R	50R
R_MEM_3	5K	5K
C_MEM	120pF	120pF

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except R_MEM_2

For normal GPU operation, these signals can be left floating (do not populate the capacitors and resistors).

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU Memory(2/5)
Size: Custom | Document Number: Enrico Caruso 14 | Rev: X00
Date: Wednesday, March 23, 2011 | Sheet 84 of 100

MEMORY ID Table

DVPDATA[3:0]	Description
0000	DDR3 SAMSUNG-K4W1G1646G-BC11(900MHz)64M*16
0001	DDR3 Hynix-H5TQ1G63DFR-11C (900MHz) 64M*16
0010	DDR3 SAMSUNG K4W2G1646C-HC11 (900MHz) 128M*16
0011	DDR3 Hynix-H5TQ2G63BFR-11C (900MHz) 128M*16

DVPDATA[0:3] Default:Pull down

X00 2011 0105 DY R8526 R8525 Q8501

For Seymour,
DPC_PVDD is DPC_VDD18
DPC_PVSS and all DPC_VSSR are DP_VSSR

2010/06/11

SSID = VIDEO

LVDS Interface

0923 Modify for DV14 Config

MEM_ID Control

2010/06/11

2010/07/07 Remove TP8517,TP8518,TP8506,TP8519,TP8512

Vendor suggest to reserve test point 09/06

11/18 Del C8529 to follow DN13

2010/07/07
Change to RSVD based on DS v3.05

12/17 dummy R8523 for panel interface unused.

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

12/20 NC R-,G-,B- on SSI and try to co-layout with Rosbson in PT stage

12/20 Add R8504 for Robson.

12/9 chnage R8501 to ROB

0820

12/16 change R8507, R8505 and R8513 to ROB

0723 Add SMBUS

AUXP PD 100K
AUXN PD 100K
Draw on EDP circuit page

Change to DY 9/20

X00 9/23
Voltage Swing:1.8V

2010/07/06
Schematics check list: X00 20101230 DY
A 1~M ohm resistor must be connected between XTALIN and XTALOUT when a crystal is used.

Clock Input Configuraiton -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

Seymou XT S3 PN:71.SEYMR.M01

71.ROBSO.M01

71.ROBSO.M01

Modified 9/1

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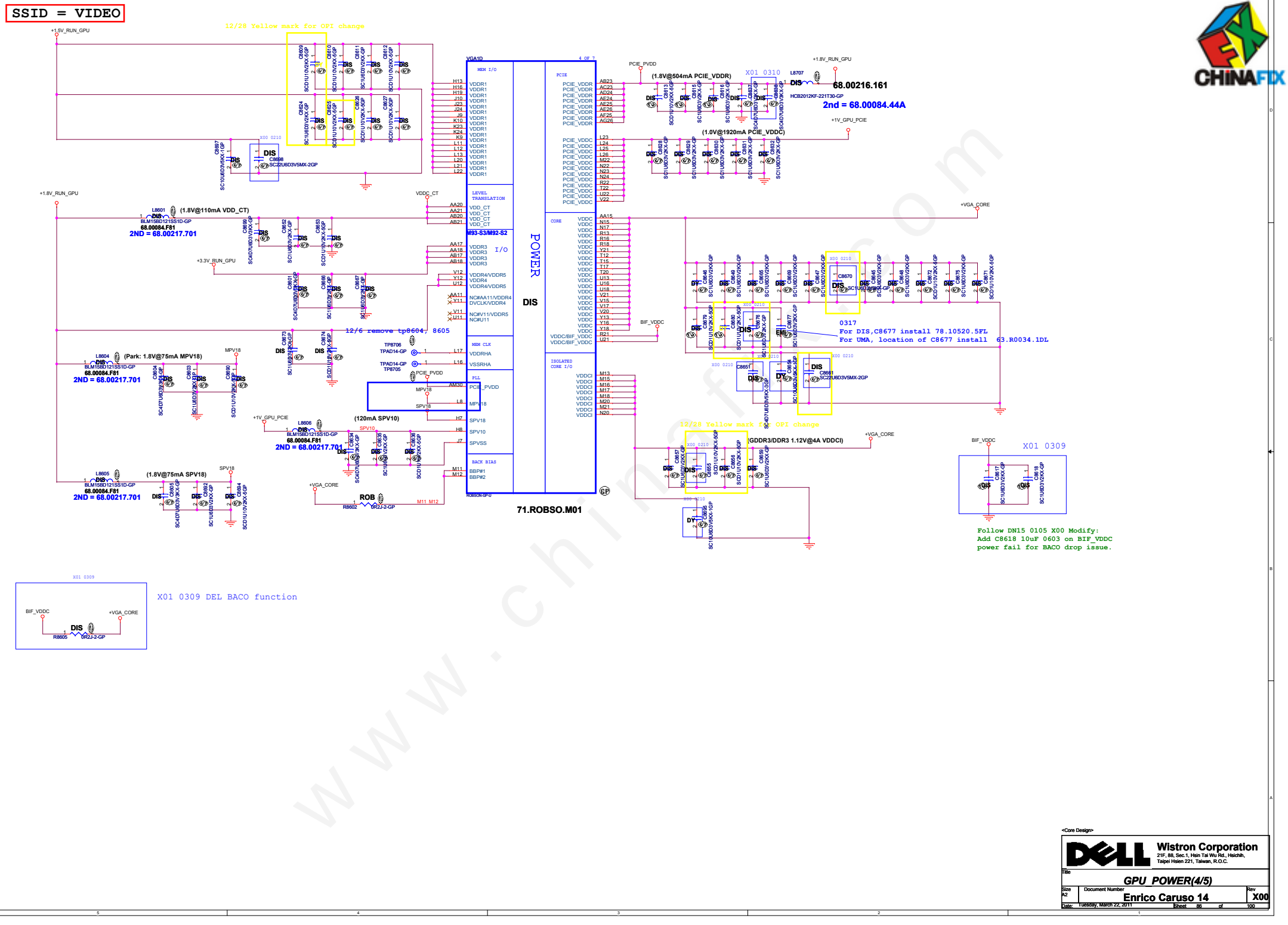
Title: GPU_DP/LVDS/CRT/GPIO(3/5)
Size: A2 | Document Number: X00 | Rev:
Date: Wednesday, March 23, 2011 | Sheet 85 of 109

Enrico Caruso 14


SSID = VIDEO
12/28 Yellow mark for OPI change
POWER
DIS
71.ROBSO.M01
(1.8V@504mA PCIE_VDDR)
X01 0310
68.00216.161
2nd = 68.00084.44A
(1.0V@1920mA PCIE_VDDC)
(1.8V@110mA VDD_CT)
2ND = 68.00217.701
(Park: 1.8V@75mA MPV18)
2ND = 68.00084.F81
(120mA SPV10)
(1.8V@75mA SPV18)
12/6 remove tp8604, 8605
(GDDR3/DDR3 1.12V@4A VDDCI)
0317
For DIS,C8677 install 78.10520.5FL
For UMA, location of C8677 install 63.R0034.1DL
X01 0309
X01 0309 DEL BACO function
Follow DN15 0105 X00 Modify:
Add C8618 10uF 0603 on BIF_VDDC
power fail for BACO drop issue.
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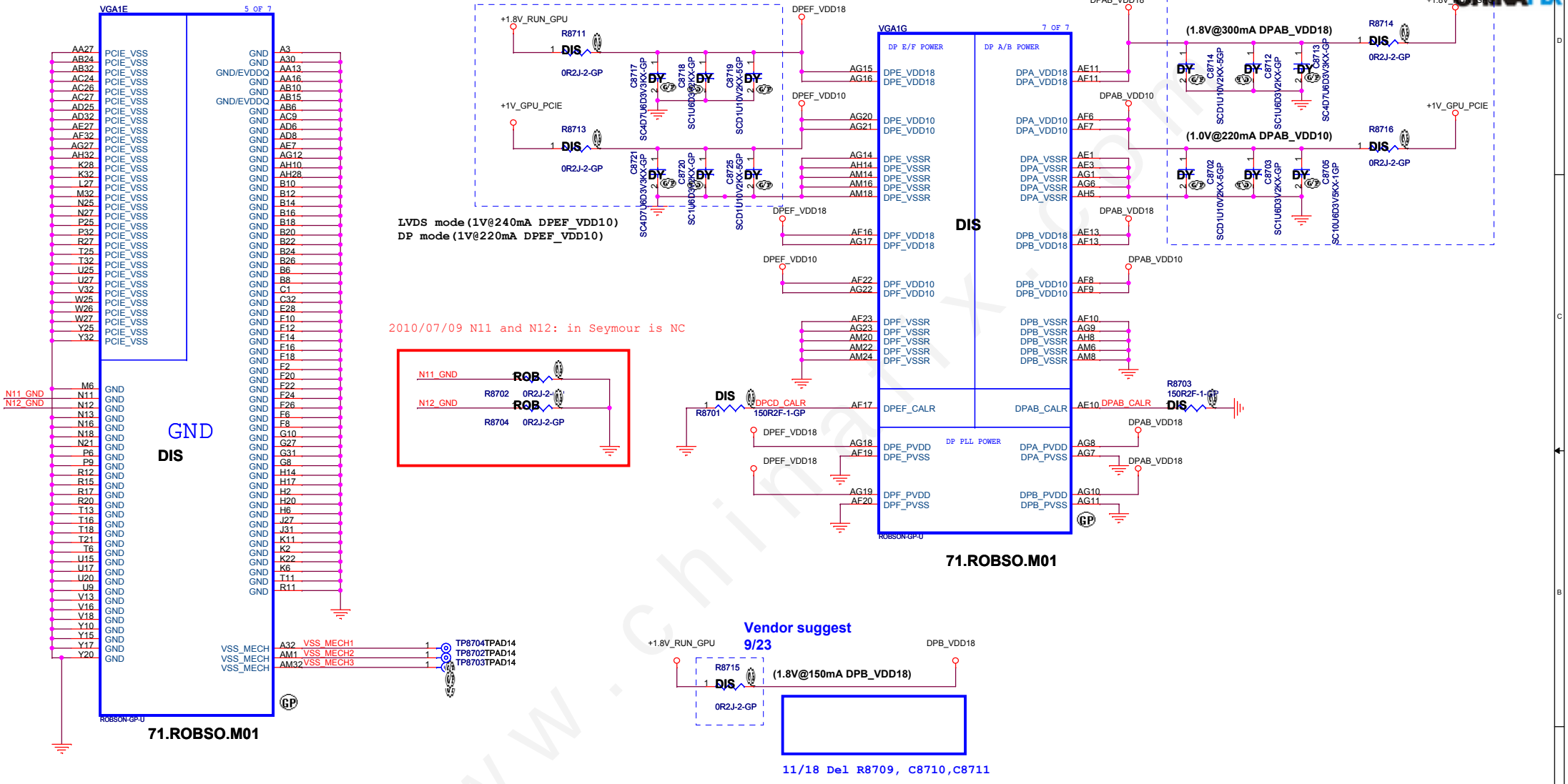
GPU_POWER(4/5)
Enrico Caruso 14
X00
Tuesday, March 22, 2011

SSID = VIDEO



<Core Design>

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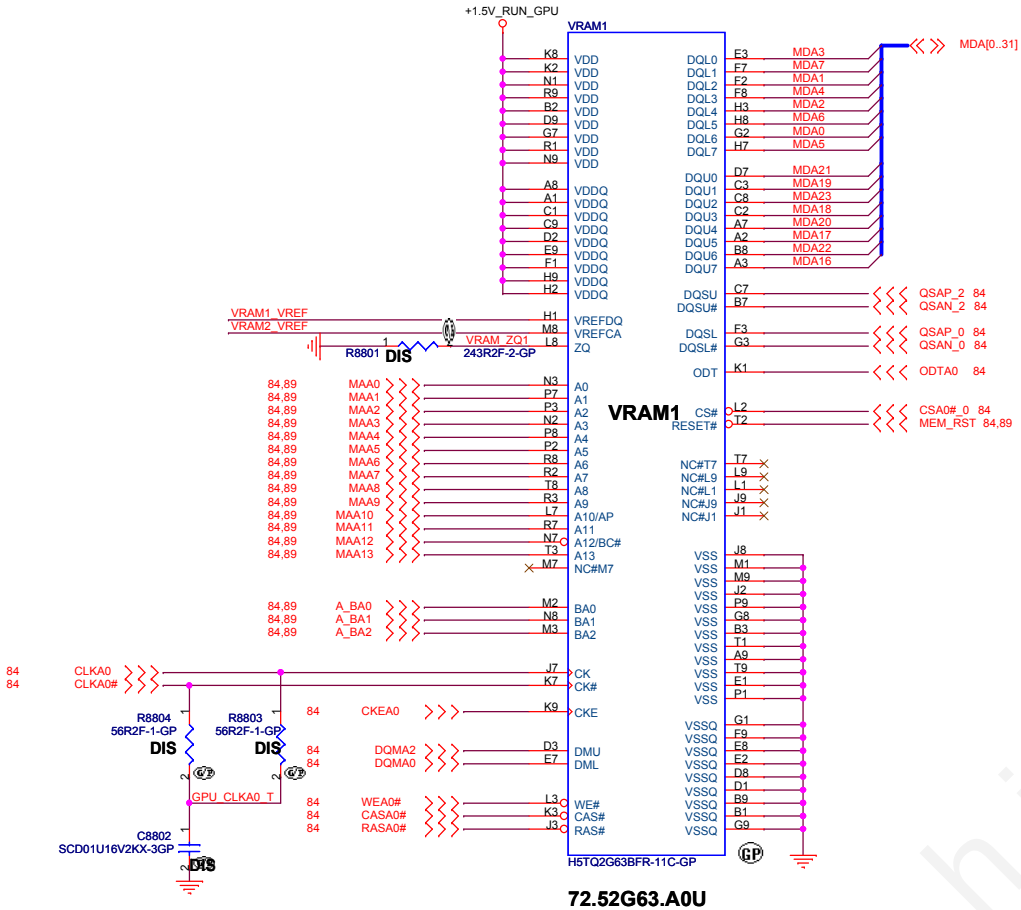
Title: GPU_DPPWR/GND(5/5)

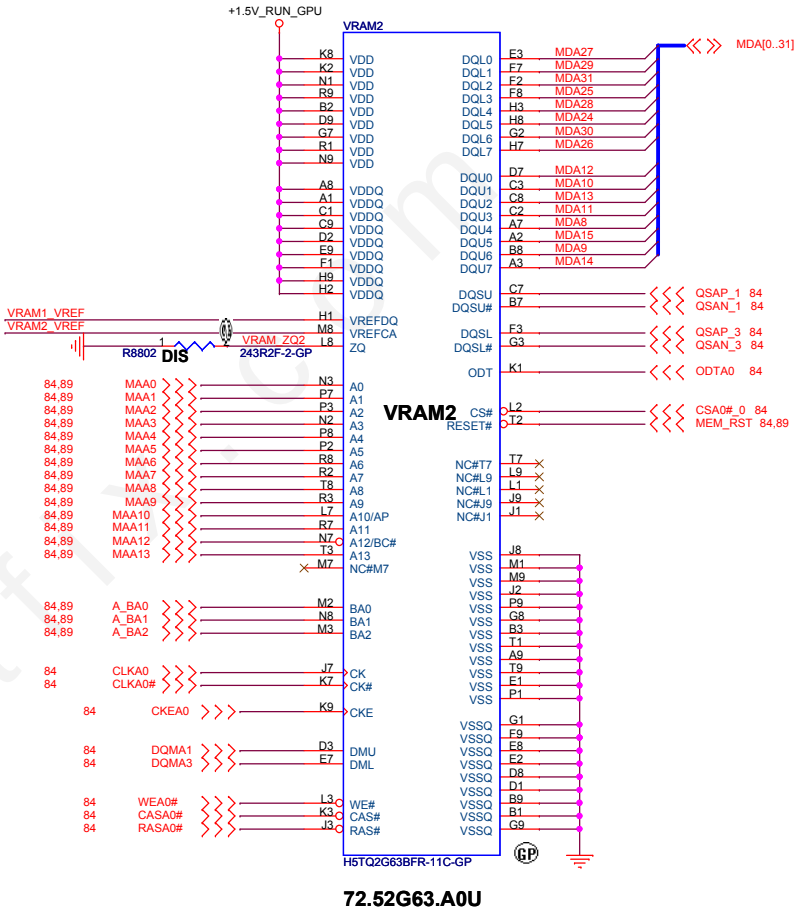
Size	Document Number	Rev
A3	Enrico Caruso 14	X00

Date: Tuesday, March 22, 2011 Sheet 87 of 100

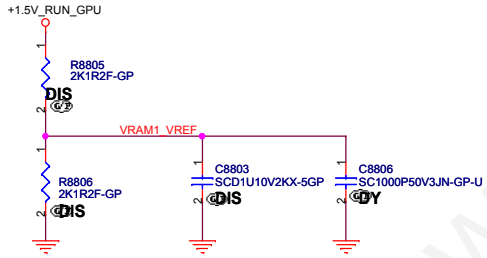
SSID = VIDEO

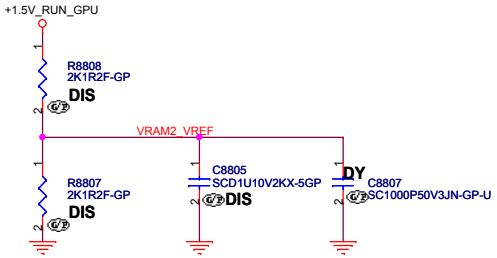


72.52G63.A0U



72.52G63.A0U





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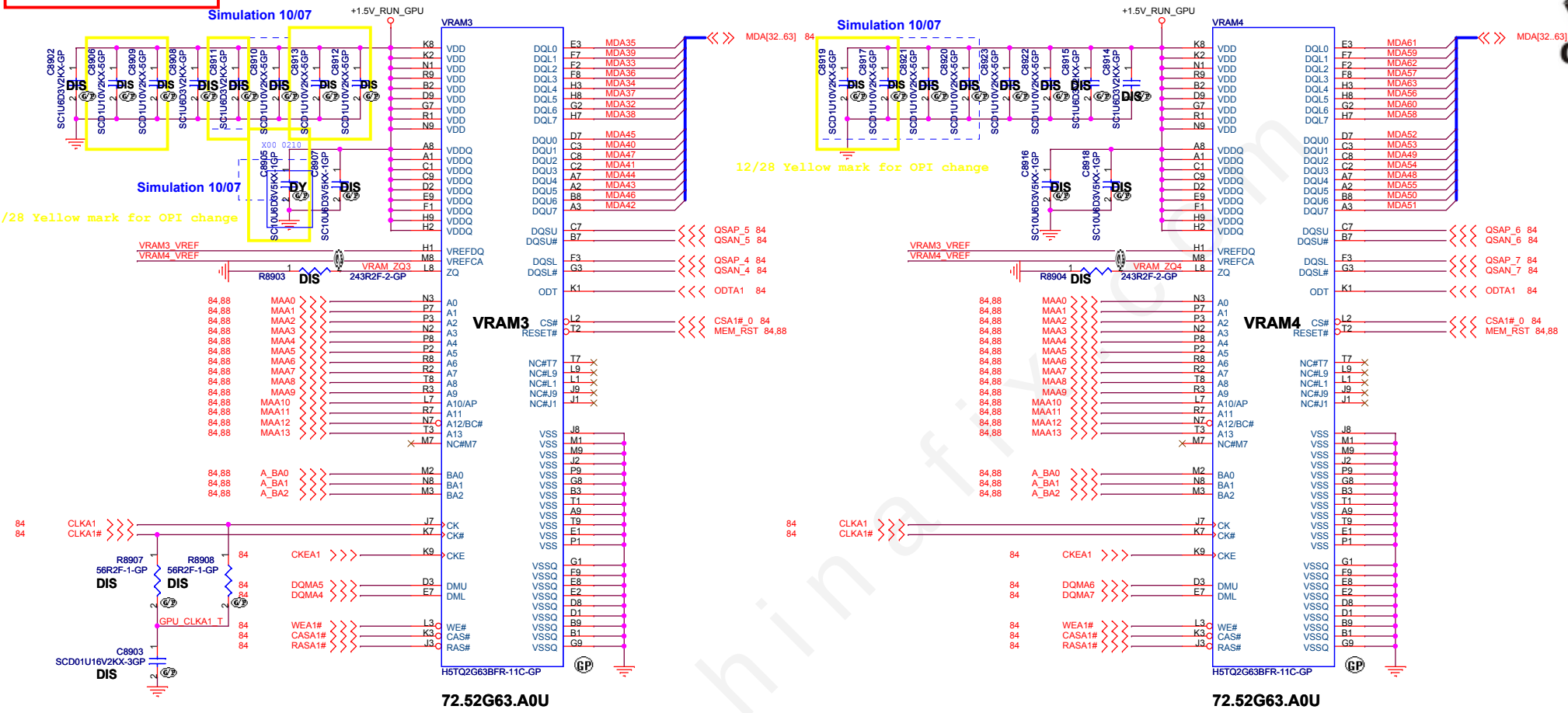
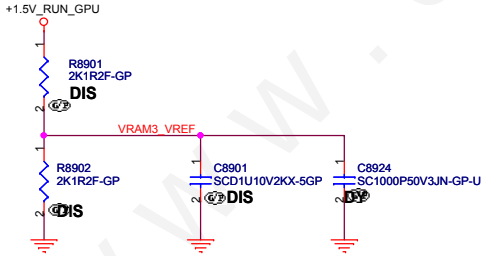
Title: GPU-VRAM1,2 (1/4)

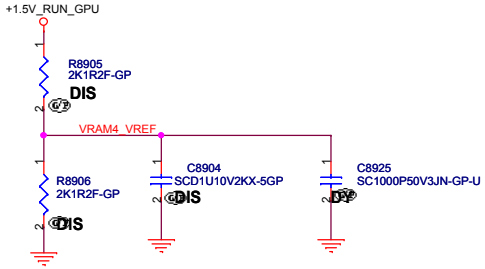
Size: Custom | Document Number: Enrico Caruso 14 | Rev: X00

Date: Wednesday, March 23, 2011 | Sheet 88 of 100

SSID = VIDEO







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Title: GPU-VRAM3,4 (2/4)

Size	Document Number	Rev
Custom	Enrico Caruso 14	X00

Date: Wednesday, March 23, 2011 Sheet 89 of 100

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Title: GPU-VRAM5,6 (3/4)

Size: A3 | Document Number: Enrico Caruso 14 | Rev: X00

Date: Thursday, January 06, 2011 | Sheet 90 of 100

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Title: GPU-VRAM7,8 (4/4)

Size: A3 | Document Number: Enrico Caruso 14 | Rev: X00

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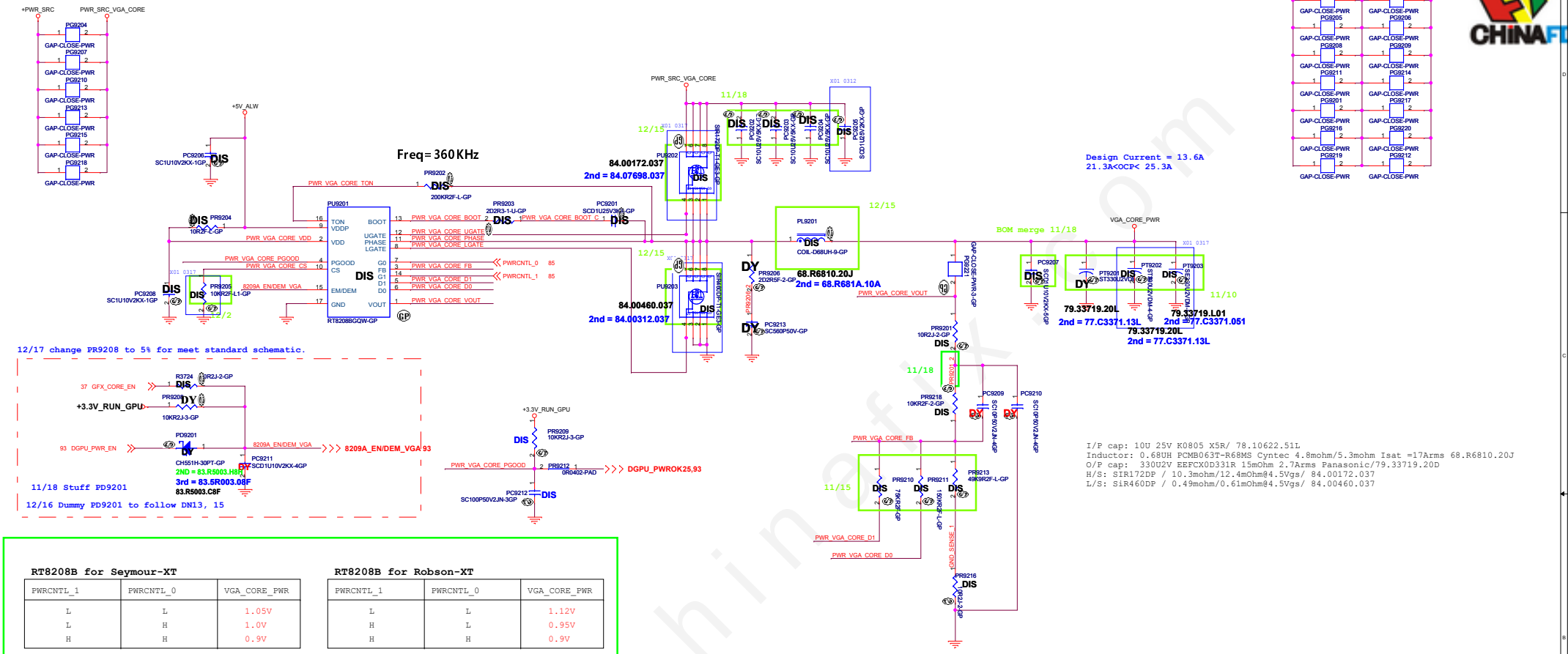
SSID = PWR.Plane.Regulator_VGACORE



RT8208B for Seymour-XT

PWRCNTL_1	PWRCNTL_0	VGA_CORE_PWR
L	L	1.05V
L	H	1.0V
H	H	0.9V

RT8208B for Robson-XT

PWRCNTL_1	PWRCNTL_0	VGA_CORE_PWR
L	L	1.12V
H	L	0.95V
H	H	0.9V

For Robson:
PR9218=10K
PR9213=49.9K
PR9211=150K
PR9210=44.2K

Vout=0.75V*(R1+R2)/R2

<Core Design>

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Title: RT8208B +VGA_CORE

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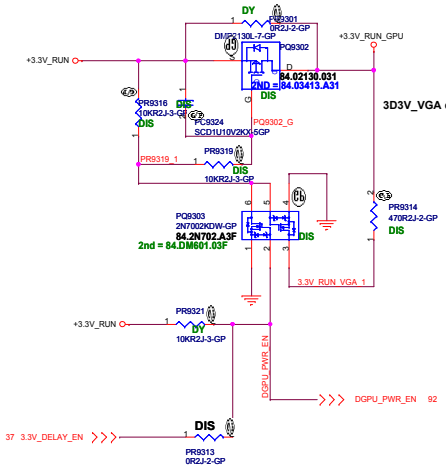
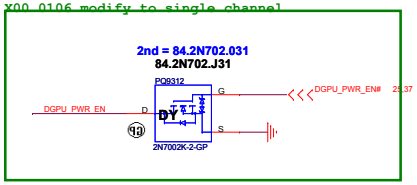
3D3V_S0 to 3D3V_VGA_S0 Transfer

Change DUMMY Reference Name to PX_BACO



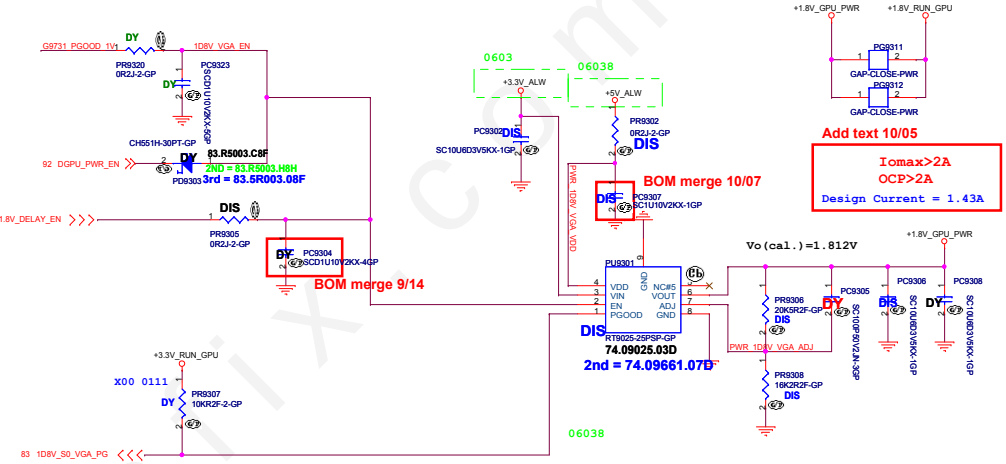
	DGPU_PWR_EN#
dGPU mode	L
IGPU	H
IGPU with BACO	L

X00 0106 modify to single channel



11/18 Merge PQ9803 PQ9804 to PQ9312

+1.8V_RUN_GPU



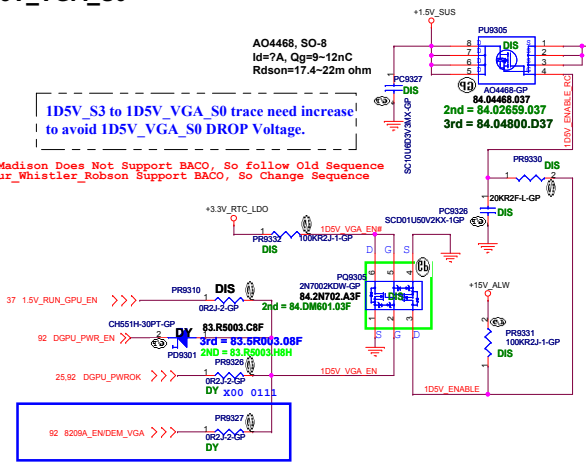
1D5V_VGA_S0

change low Rds(on) MOSFET

AO4468, SO-8
Id=7A, Qg=9~12nC
Rdson=17.4~22m ohm

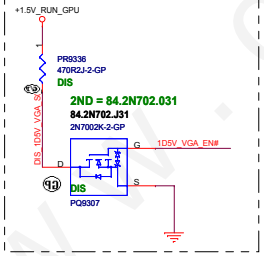
1D5V_S3 to 1D5V_VGA_S0 trace need increase to avoid 1D5V_VGA_S0 DROP Voltage.

Park_Madison Does Not Support BACO, So follow Old Sequence
Seymour_Whistler_Robson Support BACO, So Change Sequence



11/18 Add PR9327 for 8209A_EN/DEM_VGA turn on 1D5V_VGA_S0 power.

Discharge Circuit



G9731 for 1V_VGA_S0

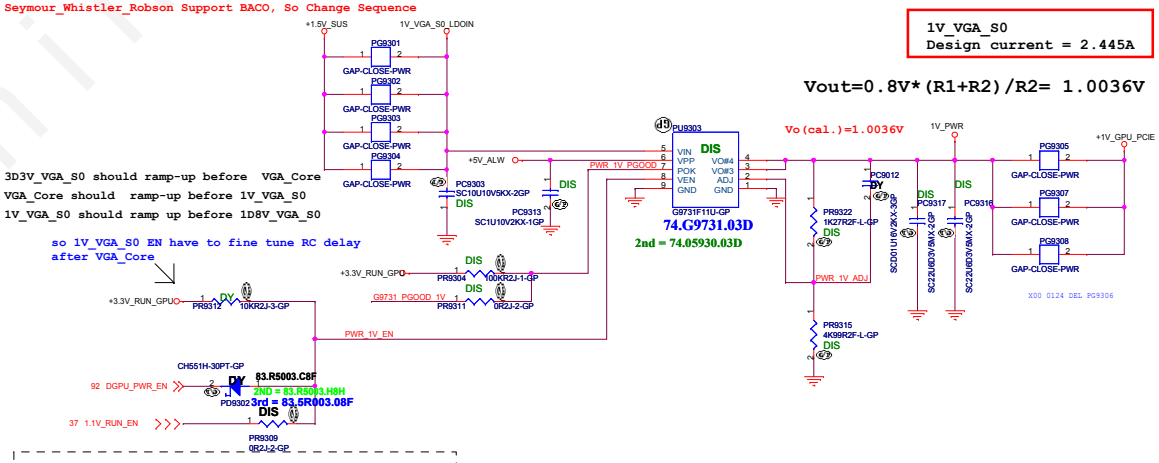
Park_Madison Does Not Support BACO, So follow Old Sequence
Seymour_Whistler_Robson Support BACO, So Change Sequence

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0

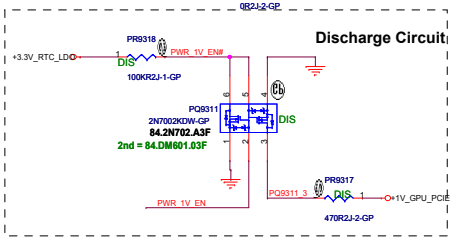
so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

1V_VGA_S0
Design current = 2.445A

Vout=0.8V*(R1+R2)/R2= 1.0036V



Discharge Circuit



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DELL	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	DISCRETE VGA POWER	
Size A2	Document Number: Enrico Caruso 14	Rev: X00
Date: Wednesday, March 23, 2011	Sheet 93 of 100	

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Title: *Reserved*

Size: A3 | Document Number: *DV14 CP UMA+DIS* | Rev: *X00*

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Title: *Reserved*

Size: A3 | Document Number: *DV14 CP UMA+DIS* | Rev: *X00*

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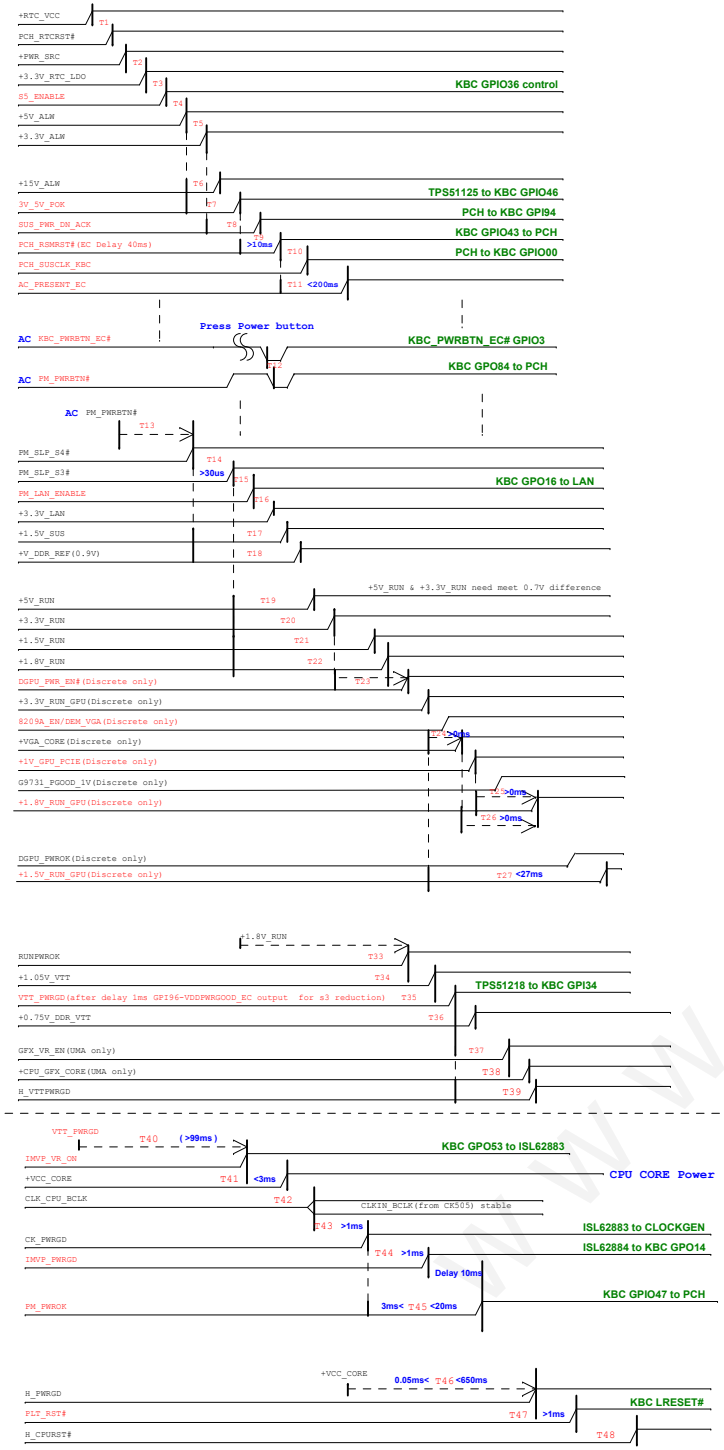
DV14 Calpella UMA&DIS Power Up Sequence

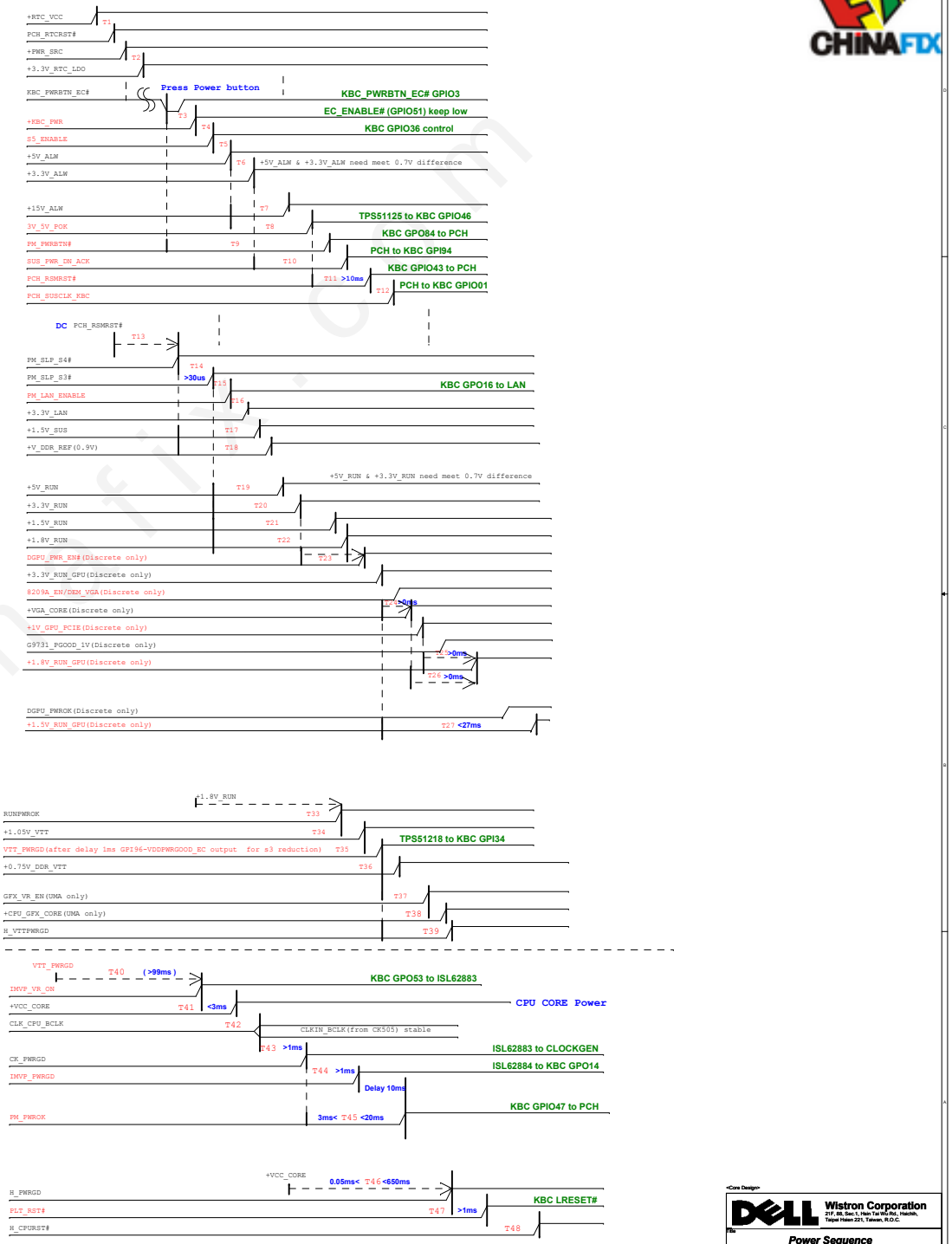
(AC mode)

red word: KBC GPIO



(DC mode)

red word: KBC GPIO



<Core Design>
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Title: Power Sequence
Size: A1 | Document Number: DV14 CP UMA+DIS | Rev: X00
Date: Monday, February 28, 2011 | Sheet 98 of 100

<Core Design>

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Title: Change History

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A3	DV14 CP UMA+DIS	X00

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Title: Change History

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A3	DV14 CP UMA+DIS	X00

Date: Thursday, January 06, 2011 Sheet 98 of 100

<Core Design>

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Title: Change History

Size	Document Number	Rev
A3	DV14 CP UMA+DIS	X00

Date: Thursday, January 06, 2011 Sheet 99 of 100

<Core Design>

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Title: Change History

Size	Document Number	Rev
A3	DV14 CP UMA+DIS	X00

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