Compal Confidential

PIQY1 M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
nVIDIA N12P-GT1

2010-10-05

REV:0.2

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.		
Title: *Cover Page*		
Size: Custom	Document Number: *LA-6882P*	Rev: 0.2
Date: Wednesday, October 06, 2010	Sheet 1 of 63	

POWER & BOARD
CAP SENSOR BOARD
I/O BOARD

ZZZ1
LA6882P

NVidia N12P-GT1
VRAM 64*16 GDDR5*8

PCI-E X16

Intel Sandy Bridge
Socket-rPGA988B
37.5mm*37.5mm

DDR3-SO-DIMM X2
BANK 0, 1, 2, 3
UP TO 8G

Dual Channel
DDR3-1066(1.5V)
DDR3-1333(1.5V)

100MHz 2.7GT/s
FDI *8
DMI *4

HDMI CONN
Passive level shift
CRT Connector
optimus 1.0
LVDS Connector
optimus 1.0

Intel Cougar Point
FCBGA 951
25mm*25mm

AZALIA
Audio Codec
RealTek
ALC272/ALC5503
2Channel Speaker
Array Digital MIC
Audio Jacks
Stereo
HeadPhone Output
Microphone Input

PCI Express Mini card Slot 1
WLAN/WiMAX
USB (WiMAX)
PCI-E (WLAN)

PCI Express Mini card Slot 2
SSD
SATA (SSD)
USB (WWAN)

6*PCI-E BUS

14*USB2.0
BlueTooth CONN
CMOS Camera
USB PORT 2.0 x2(Right)
Option3.0 x2
A-COVET Light
WLAN/WiMAX
USB PORT 2.0 x1(Left)
TV
IR

6*SATA serial
(port0,1 support SATA3)

USB3.0 Controller 2 PORT

SPI ROM BIOS

LPC BUS

EC
ENE KB930

PCI Express Mini card Slot 3
TV
PCI-E
USB

Card Reader
Jmicro JMB389
SD/MMC/MS/MS Pro/XD

Realtek
BCM7780/57781
GIGA LAN
RJ45 CONN

Int.KBD
Touch Pad
SPI ROM

ESATA HDD AND USB CONN (Left)
SATA3.0 HDD CONN
SATA3.0 HDD (SSD)
SATA ODD CONN

WLAN/WiMAX

TV

Thermal Sensor
EMC1403

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Issued Date	2008/03/24	Deciphered Date	2008/04/

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Title: MB Block Diagram
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Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	10K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	
0	0	0 V	0 V	0 V	EVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	DVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	PVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	MP
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

SMBUS Control Table

	SOURCE	VGA	BATT	KE930	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB930 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB930 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port
EHCI1	UHCI0	0	USB Port (Left Side)
		1	USB Port (Left Side)
	UHCI1	2	USB Port (Right Side)
		3	USB Port (Right Side)
	UHCI2	4	Camera(3D)
		5	Camera
	UHCI3	6	
		7	
EHCI2	UHCI4	8	IR
		9	Mini Card(WLAN)
	UHCI5	10	A Cover Light
		11	
	UHCI6	12	Mini Card(TV)
		13	Blue Tooth

PCIE PORT LIST

Port	Device
1	LAN
2	WLAN
3	
4	USB3.0
5	Card Reader
6	TV
7	
8	

BOM Structure Table

BOM Structure	BTO Item
OPTI@	OPTIMUS part
DIS@	Discrete part
UMA@	UMA part
DIS_ONLY@	Discrete only part
HDMI@	HDMI part (DIS and UMA)
UMA_HDMI@	HDMI part (UMA)
DIS_HDMI@	HDMI part (DIS)
USB20@	USB20 option (Right side 2 ports)
USB30@	USB30 option (Right side 2 ports)
USB30_SUB@	USB30 part at sub-board
TV@	TV module part
TV_SW@	TV module power swith part
NO_TVSW@	No TV module power swith part
USB_CHG@	USB charger part
NO_CHG@	No USB charger part
272@	ALC272 audio codec part
5503@	ALC5503 audio codec part
57780@	BCM57780 LAN part
57781@	BCM57781 LAN part
ACOVER@	A cover light part
BT@	Blue Tooth part
CMOS@	CMOS Camera part
ESATA@	E-SATA part
VENTURA@	NVDIA VENTURA function part
X76@	X76 Level part
S1G@	Samsun VRAM 1G part
S2G@	Samsun VRAM 2G part
H1G@	Hynix VRAM 1G part
ME@	ME part
@	Unpop

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb
Thermal Sensor EMC1402-1	100_1100 b

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

SKU

OPTIMUS	UMA@+DIS@+OPTI@
Discrete only	DIS@+DIS_ONLY@

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Title: *Notes List*

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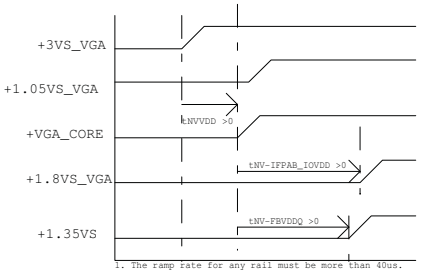
VGA and GDDR5 Voltage Rails (N12Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	N/A	
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	Thermal Alert
GPIO10	OUT	-	Memory VREF Control
GPIO11	I/O	N/A	
GPIO12	IN		AC Power Detect Input (10K pull low)
GPIO13	OUT	N/A	
GPIO14	OUT	N/A	
GPIO15	IN		Hot Plug Detect for IFPE
GPIO16	OUT	N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	



1. The ramp rate for any rail must be more than 40us.
2. +VGA_CORE <= +3VS_VGA +0.5V
3. +1.5VS_VGA <= +3VS_VGA +0.5V
4. Optimus follows power sequencing rules specified in discrete GPU design guide.

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N12P-GT1 64bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_VGA	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]

GPIO5 GPIO6

	Device ID
N12P-GT1 (40nm)	0x0DEB

GPU_VID0	GPU_VID1	VGA_CORE	P-State
0	0	0.825V	Deep P12
0	1	0.825V	P8
1	1	1.075V	P0

GPU	FB Memory (GDDR5)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N12P-GT1	Samsung 1800MHz (defaul)	K4G10325FE-HC04						
		32Mx32	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K
	Hynix 1600MHz	H5GQ1H24AFR-T2L						
		32Mx32	PD 10K	PD 15K	PD 15K	PU 20K	PD 35K	PU 45K
					X76			

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Title: VGA Notes List

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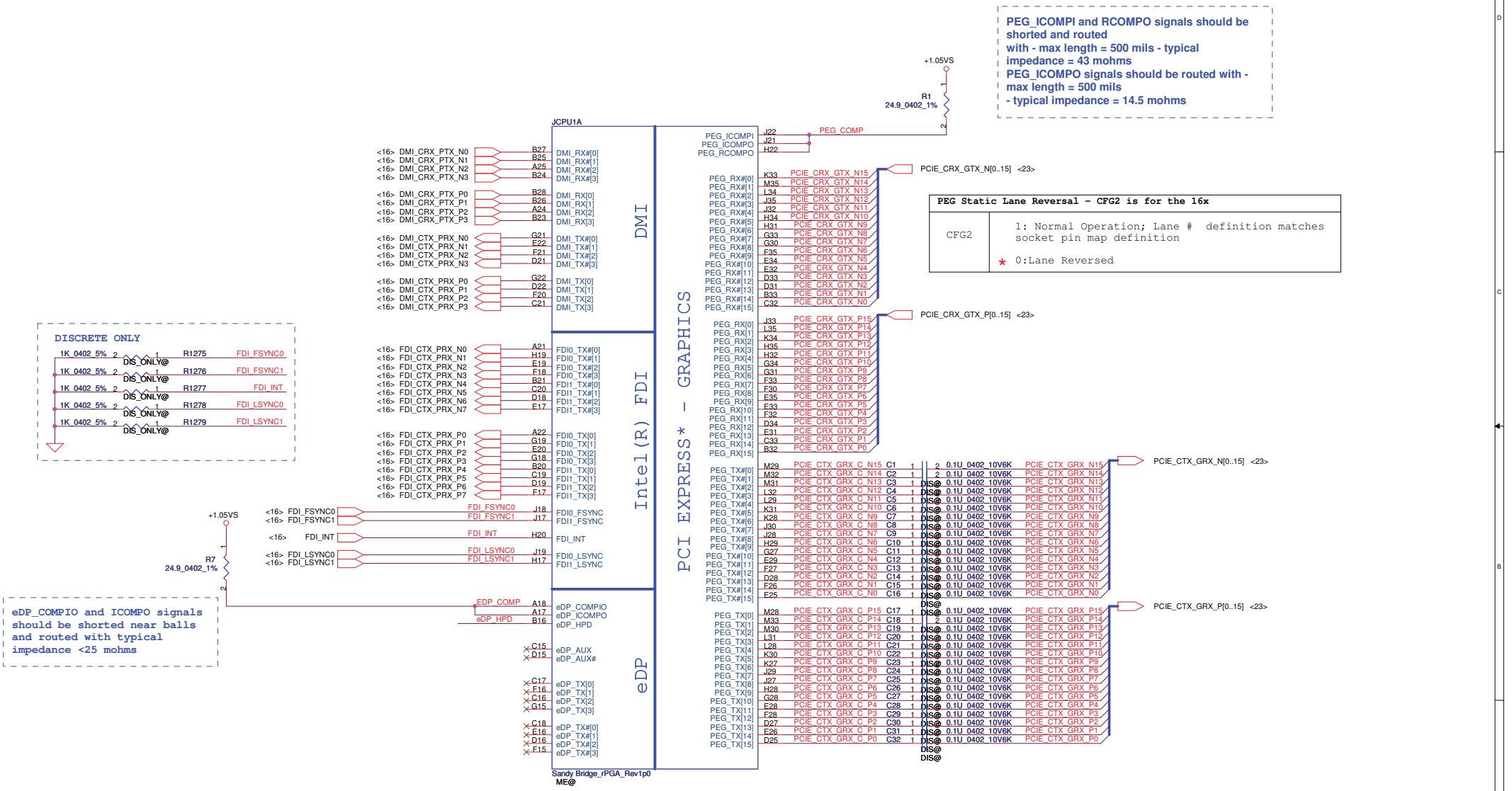

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Title: PROCESSOR(1/7) DMI,FDI,PEG

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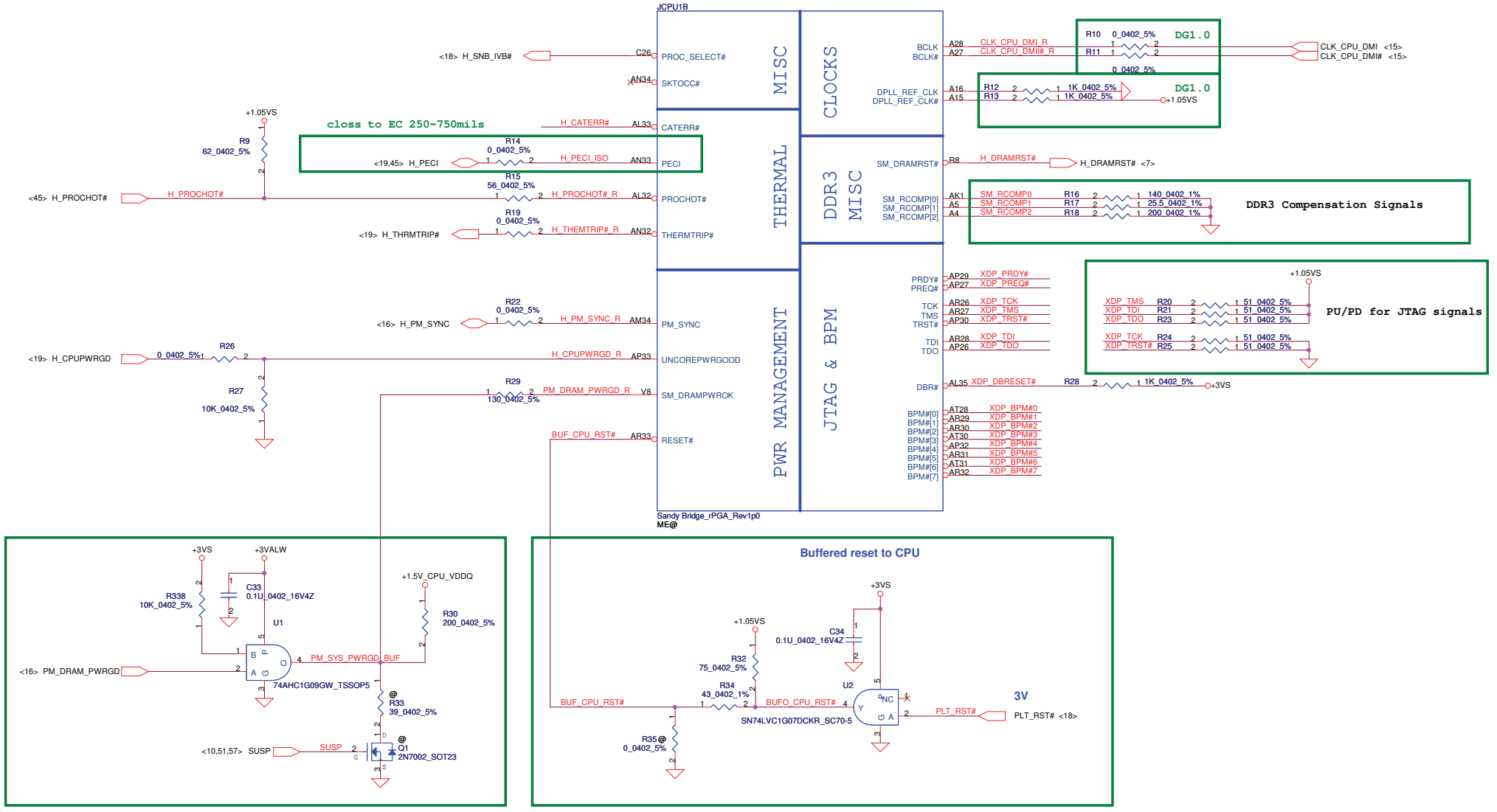

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Title	Compal Electronics, Inc.		
	PROCESSOR(2/7) PM,XDP,CLK		
Size: Custom	Document Number: LA-6882P		Rev: 0.2
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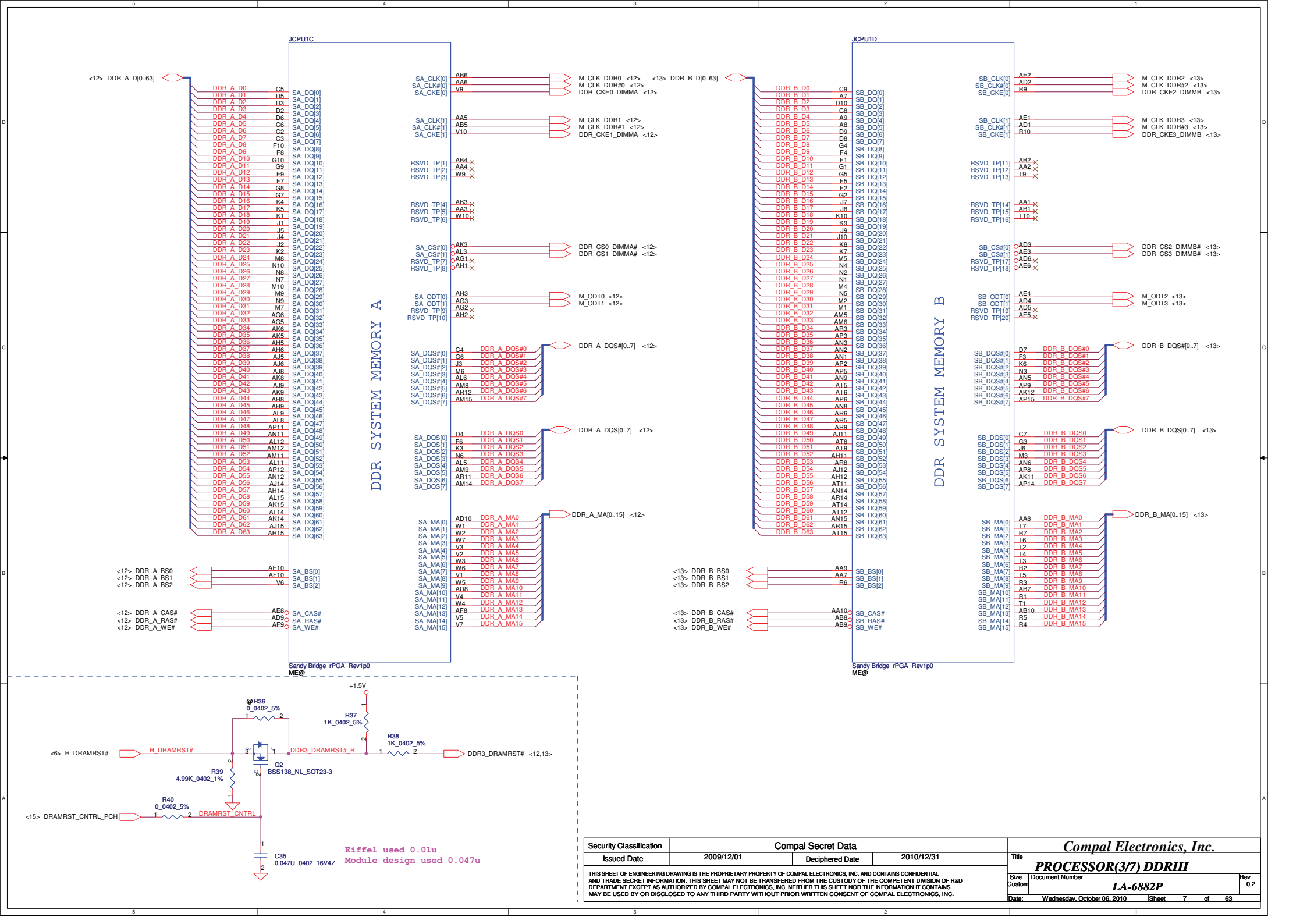

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Title: PROCESSOR(3/7) DDRIII

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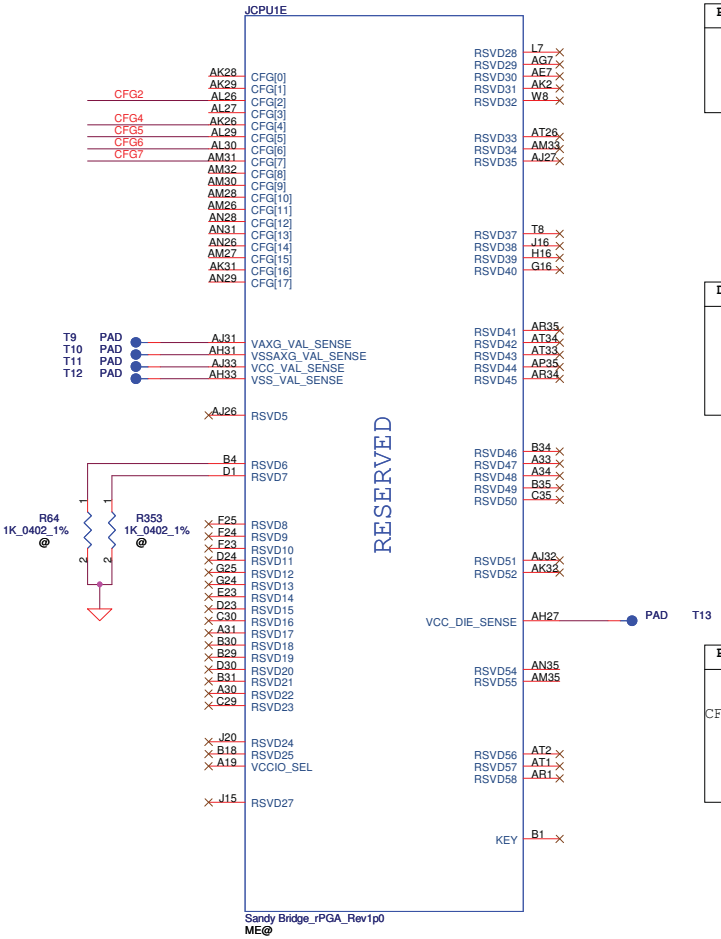
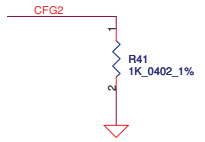
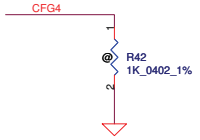
CFG Straps for Processor

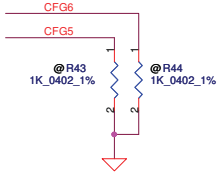




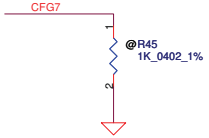
PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(4/7) RSVD,CFG

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POWER

JCPU1F

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

+CPU_CORE

(6/16 change 10uF_0603_6.3V)*5

QC=94A
DC=53A

C36 10U_0805_6.3V6M
C37 10U_0805_6.3V6M
C38 10U_0805_6.3V6M
C39 10U_0805_6.3V6M
C40 10U_0805_6.3V6M
C48 10U_0603_6.3V6M
C49 10U_0603_6.3V6M
C50 10U_0603_6.3V6M
C51 10U_0603_6.3V6M
C52 10U_0603_6.3V6M
C53 10U_0603_6.3V6M @

+CPU_CORE

(22uF_0805_6.3V)*16

C66 22U_0805_6.3V6M
C67 22U_0805_6.3V6M
C68 22U_0805_6.3V6M
C70 22U_0805_6.3V6M
C71 22U_0805_6.3V6M
C74 22U_0805_6.3V6M
C75 22U_0805_6.3V6M
C76 22U_0805_6.3V6M
C77 22U_0805_6.3V6M
C78 22U_0805_6.3V6M
C79 22U_0805_6.3V6M
C80 22U_0805_6.3V6M
C81 22U_0805_6.3V6M
C82 22U_0805_6.3V6M
C83 22U_0805_6.3V6M
C84 22U_0805_6.3V6M
C85 22U_0805_6.3V6M @
C86 22U_0805_6.3V6M @
C87 22U_0805_6.3V6M @

+CPU_CORE

(330uF)*4

C88 330U_X_2VM_R8M
C89 330U_X_2VM_R8M
C90 330U_X_2VM_R8M
C91 330U_X_2VM_R8M

Cap quantity follow HR_PDDG_Rev07
22uF*7 NO-STUFF

18A

(22uF_0805_6.3V)*13

+1.05VS

C41 C42 C43 C44 C54 C45 C46 C55 C56 C47 22U_0805_6.3V6M

C57 C58 C59 @ C60 @ C61 @ C62 @ C63 @ C64 @ C65 @ 22U_0805_6.3V6M

C922 330U_2.5V_M
C288 330U_2.5V_M
C69 @ 330U_D2_2.5VY_R9M
C72 330U_D2_2.5VY_R9M
C73 @ 330U_D2_2.5VY_R9M

OSCAN
(330U 2.5V M 6.3X5.5 R15M)*1=(SF000002000)

+1.05VS

R46 75_0402_5%

VR_SVID_CLK series-resistors close to VR

VIDALERT# AJ29 H_CPU_SVIDALRT# R47 43_0402_5% VR_SVID_ALRT# <60>
VIDSCLK AJ30 H_CPU_SVIDCLK R48 0_0402_5% VR_SVID_CLK <60>
VIDSOUT AJ28 H_CPU_SVIDDAT R49 0_0402_5% VR_SVID_DAT <60>

R50 130_0402_5% +1.05VS

VCC_SENCE 100ohm +-1% pull-up to VCC near processor

+CPU_CORE

R51 100_0402_1%

VCC_SENSE AJ35 VCCSENSE_R R52 0_0402_5% VCCSENSE <60>
VSS_SENSE AJ34 VSSSENSE_R R53 0_0402_5% VSSSENSE <60>

R1294 10_0402_1% +1.05VS

VCCIO_SENSE B10 VCCIO_SENSE <58>
VSSIO_SENSE A10 VSSIO_SENSE

R54 100_0402_1%
R1295 @ 27.4_0402_1%
R1296 @ 27.4_0402_1%
R1297 10_0402_1%

VSS_SENCE 100ohm +-1% pull-down to GND near processor

Sandy Bridge_rPGA_Rev1.0
ME@

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Title: PROCESSOR(5/7) PWR,BYPASS

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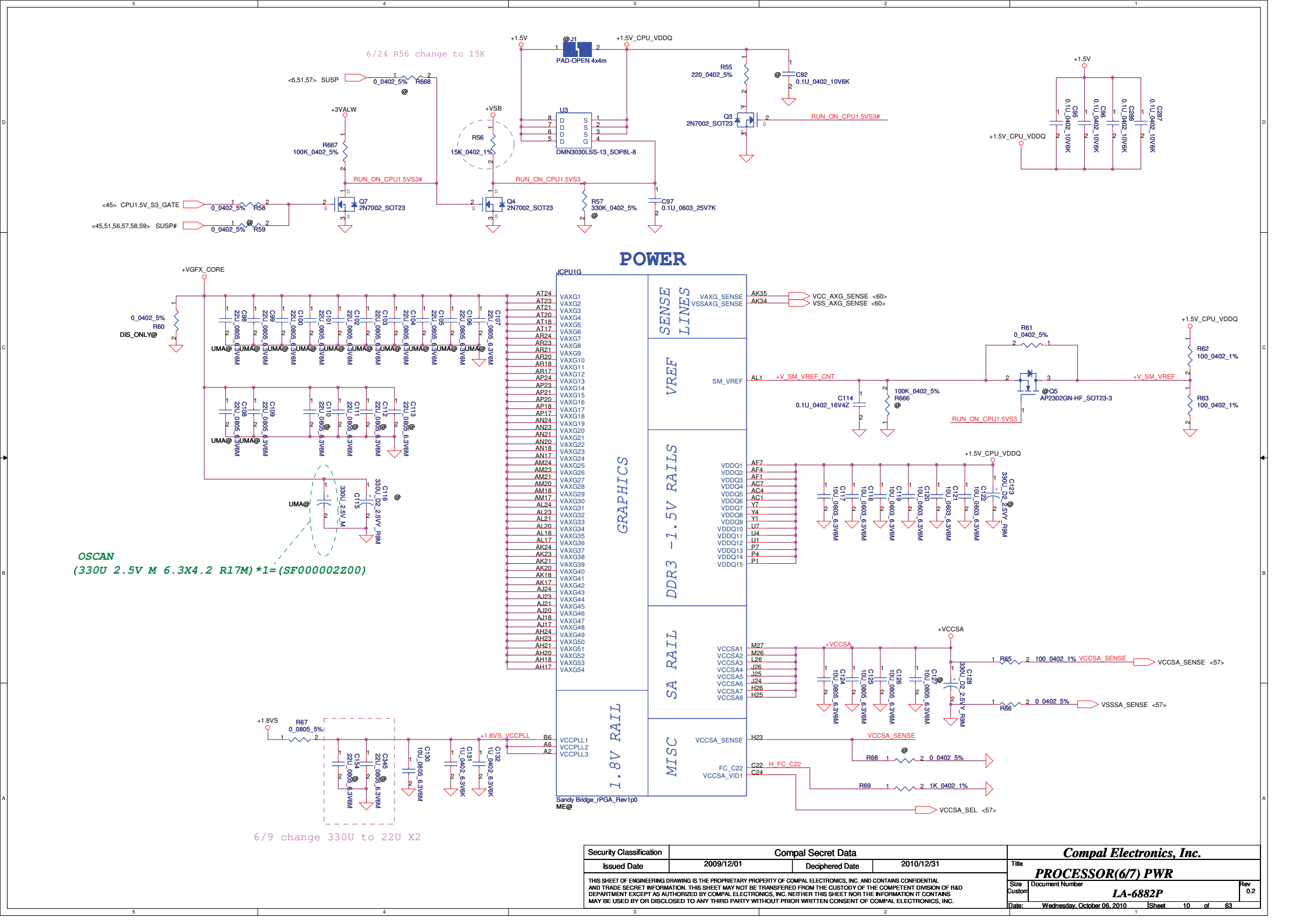
6/24 R56 change to 15K
POWER
JCPU1G
SENSE LINES
VREF
GRAPHICS
DDR3 -1.5V RAILS
SA RAIL
1.8V RAIL
MISC
Sandy Bridge_rPGA_Rev1p0
ME@
OSCAN
(330U 2.5V M 6.3X4.2 R17M)*1=(SF000002Z00)
6/9 change 330U to 22U X2
PAD-OPEN 4x4m
DMN3030LSS-13_SOP8L-8
2N7002_SOT23
AP2302GN-HF_SOT23-3
VCC_AXG_SENSE <60>
VSS_AXG_SENSE <60>
VCCSA_SENSE <57>
VSSSA_SENSE <57>
VCCSA_SEL <57>
RUN_ON_CPU1.5VS3#
RUN_ON_CPU1.5VS3
+V_SM_VREF_CNT
+V_SM_VREF
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Compal Secret Data
Issued Date
2009/12/01
Deciphered Date
2010/12/31
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PROCESSOR(6/7) PWR
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Custom
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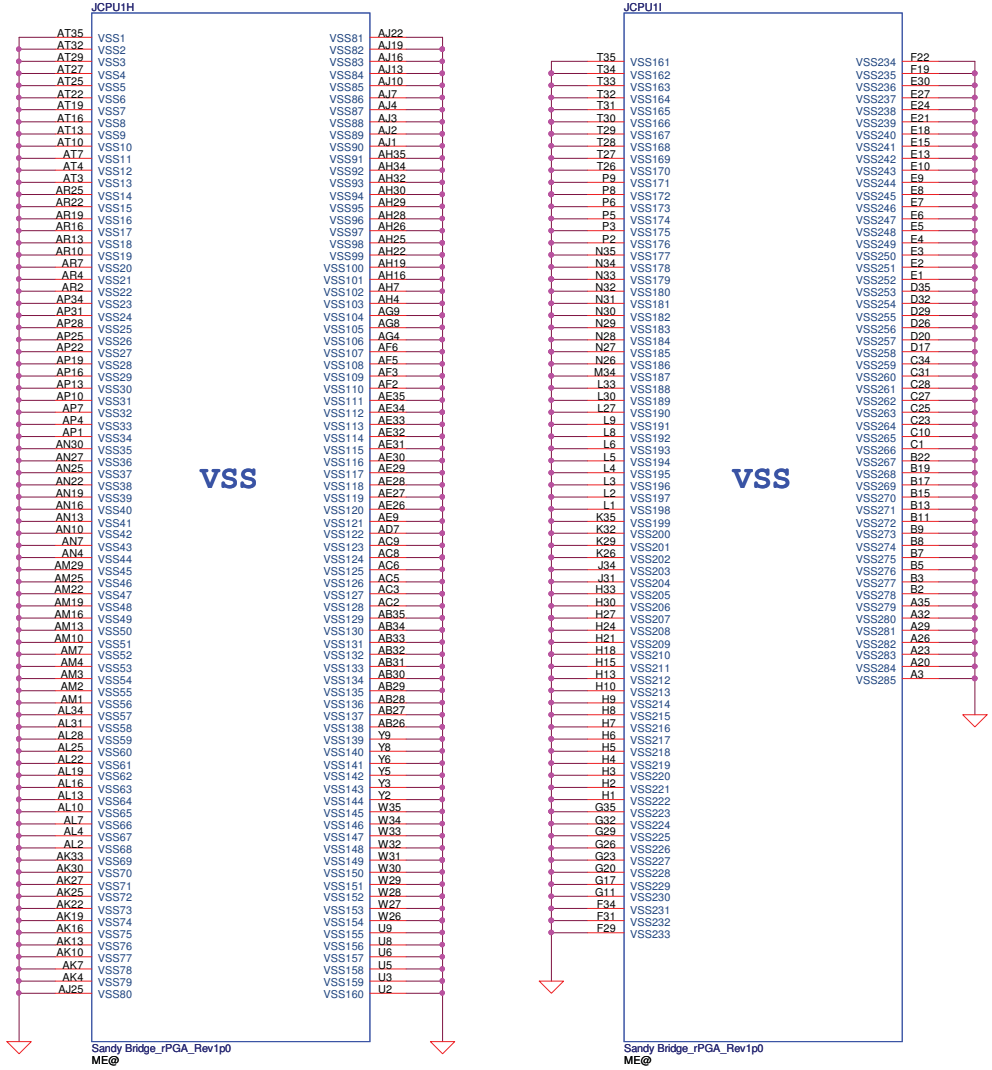

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Compal Electronics, Inc.

Title: PROCESSOR(7/7) VSS

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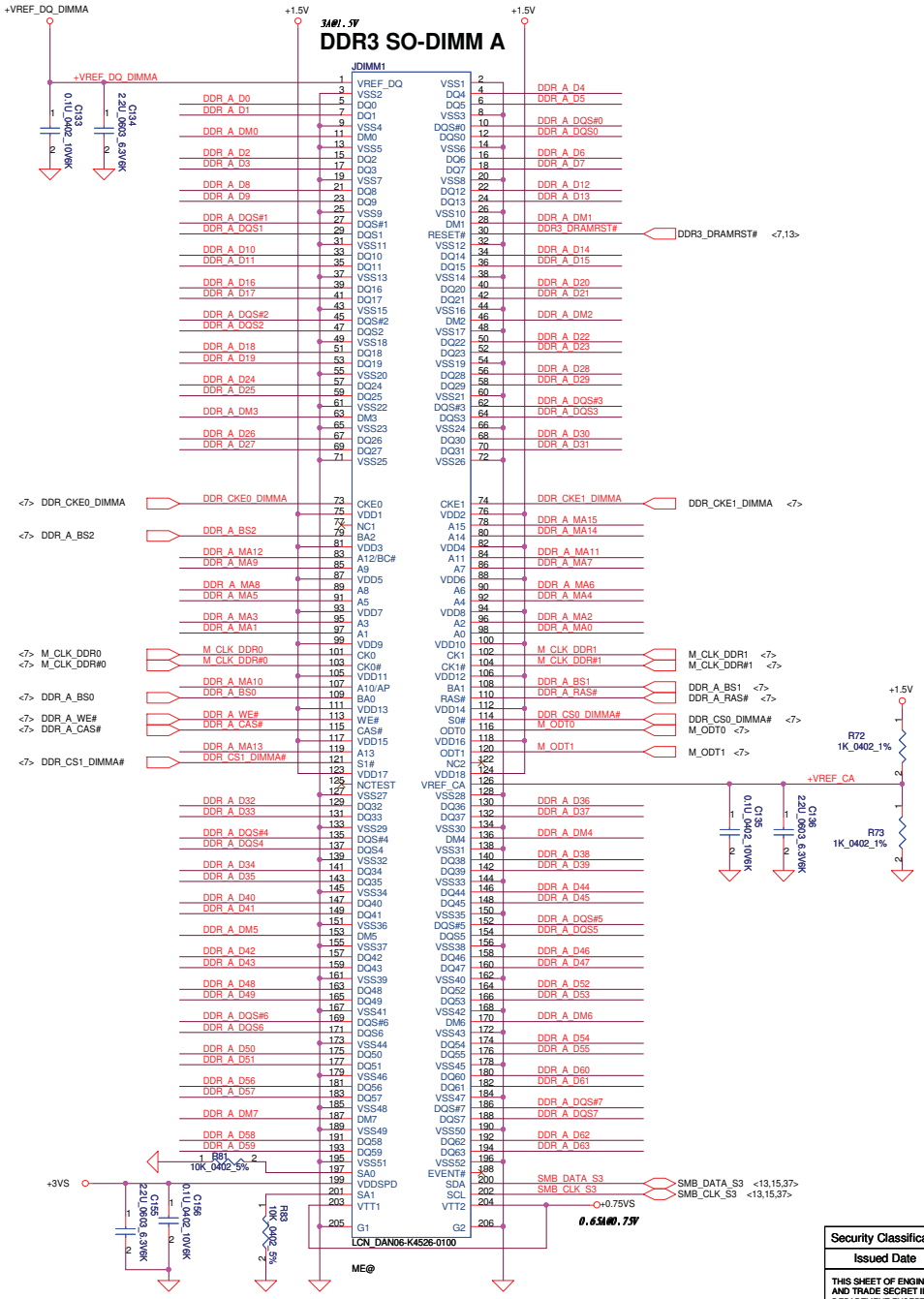
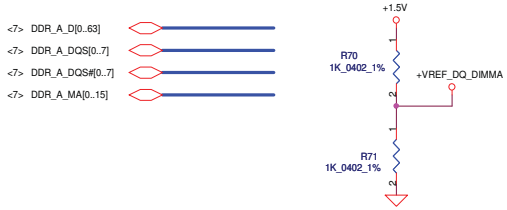
DDR3 SO-DIMM A



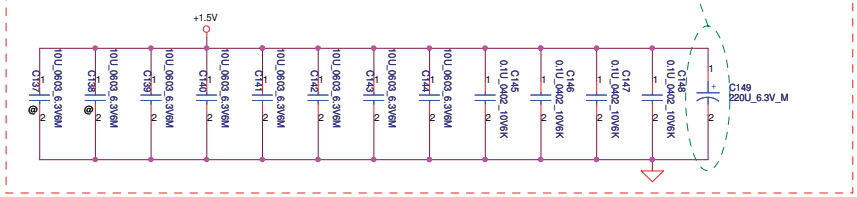


OSCAN (220uF_6.3V_5.9L_ESR15m)*1=(SF000001500)

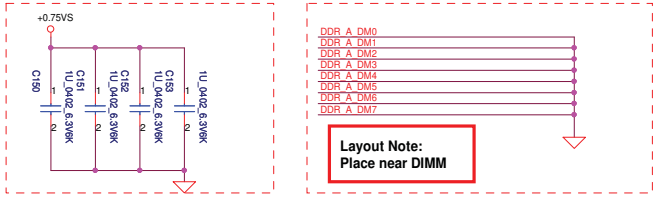
(10uF_0603_6.3V)*8

(0.1uF_402_10V)*4

Layout Note:
Place near DIMM



Layout Note:
Place near DIMM



Layout Note:
Place near DIMM

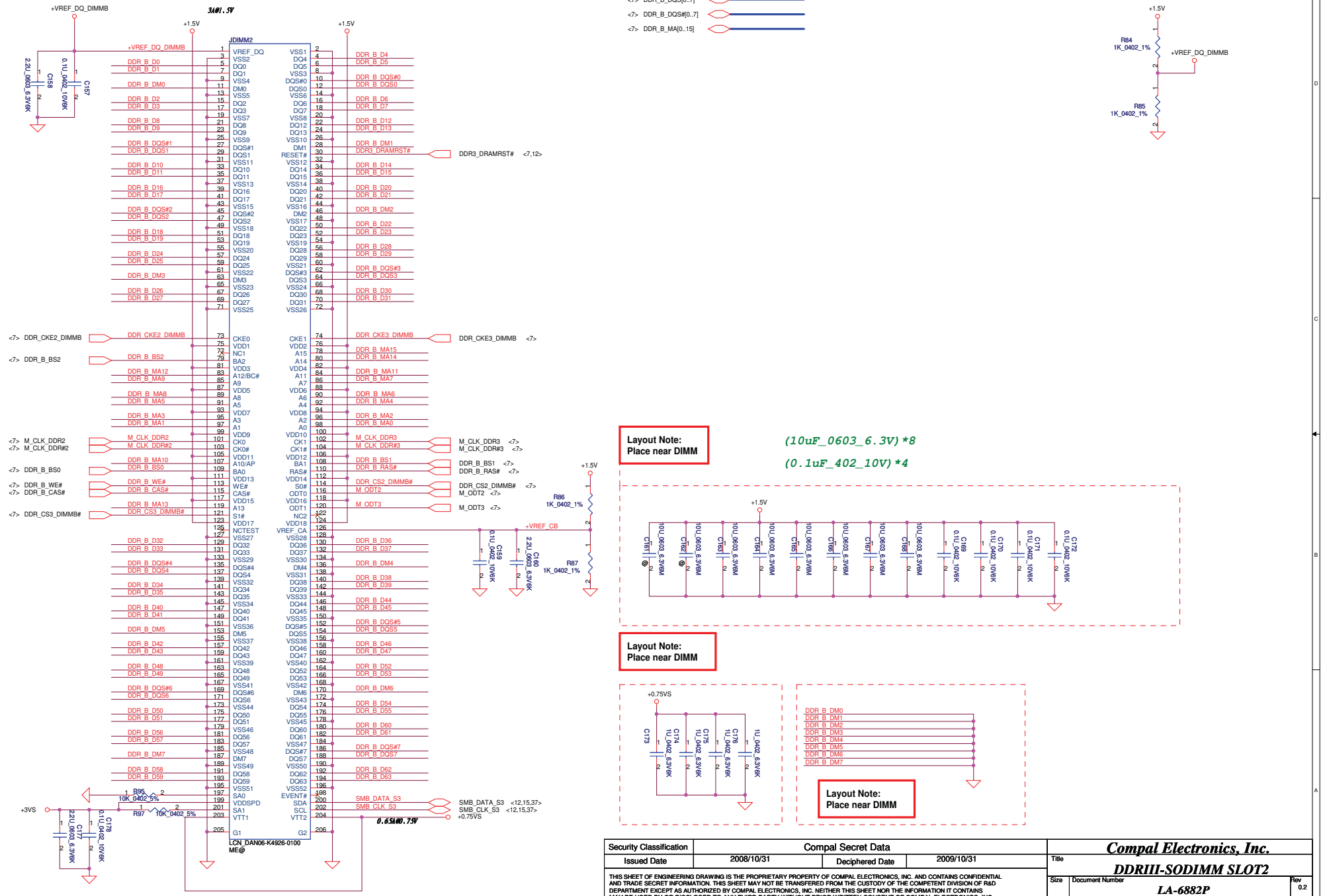
Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT1**

Size: Custom | Document Number: **LA-6882P** | Rev: 0.2

Date: Wednesday, October 06, 2010 | Sheet 12 of 63



Security Classification	Compal Secret Data		
Issued Date	2008/10/31	Deciphered Date	2009/10/31

Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT2**

Size	Document Number	Rev
	LA-6882P	0.2

Date: Wednesday, October 06, 2010 | Sheet 13 of 63

W=20mils W=20mils
+RTCVCC +RTCBATT
R99 1K_0402_5%
C179 1U_0603_10V4Z
CLRP1 SHORT PADS

+RTCVCC
R101 1M_0402_5% SM_INTRUDER#
R102 330K_0402_5% PCH_INTVRMEN
R1330 330K_0402_5%
INTVRMEN
* H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)

+3VS
R105 1K_0402_5% HDA_SPKR
* HIGH= Enable (No Reboot)
LOW= Disable (Default)

+3VALW
R106 1K_0402_5% HDA_SDOUT
* Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]

+3VALW
R108 1K_0402_5% HDA_SYNC
This signal has a weak internal pull-down

* On Die PLL VR Select is supplied by
1.5V when smapled high
1.8V when sampled low
Needs to be pulled High for Huron River platfrom

R112 33_0402_5% HDA_BIT_CLK
R114 33_0402_5% HDA_SYNC_R
R116 33_0402_5% HDA_RST#
R118 33_0402_5% HDA_SDOUT
<42> HDA_BITCLK_AUDIO
<42> HDA_SYNC_AUDIO
<42> HDA_RST_AUDIO#
<42> HDA_SDOUT_AUDIO

+3VALW
R121 200_0402_5% PCH_JTAG_TDO
R122 200_0402_5% PCH_JTAG_TMS
R123 200_0402_5% PCH_JTAG_TDI
R125 100_0402_1%
R126 100_0402_1%
R128 100_0402_1%
DPDG1.1

6/30 update R121, R122, R123

R98 10M_0402_5%
PCH_RTCX1 PCH_RTCX2
Y1 32.768KHZ_12.5PF_9H03200413
C180 18P_0402_50V8J
C181 18P_0402_50V8J
CMOS

+RTCVCC
C183 1U_0603_10V4Z
R103 20K_0402_5%
R100 20K_0402_5%
C182 1U_0603_10V4Z
CLRP2 SHORT PADS
CLRP3 SHORT PADS

U4A
PCH_RTCX1 A20 RTCX1
PCH_RTCX2 C20 RTCX2
PCH_RTCRST# D20 RTCRST#
PCH_SRTCRST# G22 SRTCRST#
SM_INTRUDER# K22 INTRUDER#
PCH_INTVRMEN C17 INTVRMEN
RTC

LPC
FWH0 / LAD0 C38 LPC_AD0
FWH1 / LAD1 A38 LPC_AD1
FWH2 / LAD2 B37 LPC_AD2
FWH3 / LAD3 C37 LPC_AD3
FWH4 / LFRAME# D36 LPC_FRAME#
LDRQ0# E36
LDRQ1# / GPIO23 K36
SERIRQ V5
LPC_AD0 <37,45>
LPC_AD1 <37,45>
LPC_AD2 <37,45>
LPC_AD3 <37,45>
LPC_FRAME# <37,45>
SERIRQ <45>
R104 10K_0402_5% +3VS
EC and Mini card debug port

HDA_BIT_CLK N34 HDA_BCLK
HDA_SYNC L34 HDA_SYNC
HDA_SPKR T10 SPKR
HDA_RST# K34 HDA_RST#
HDA_SDIN0 E34 HDA_SDIN0
G34 HDA_SDIN1
C34 HDA_SDIN2
A34 HDA_SDIN3
IHDA
<42> HDA_SPKR
<42> HDA_SDIN0

R109 0_0402_5%
ME_FLASH HDA_SDOUT A36 HDA_SDO
<45> ME_FLASH
R107 1K_0402_1% PCH_GPIO33 C36 HDA_DOCK_EN# / GPIO33
Kill_SW# N32 HDA_DOCK_RST# / GPIO13
<49> Kill_SW#

R110 51_0402_5%
PCH_JTAG_TCK J3 JTAG_TCK
PCH_JTAG_TMS H7 JTAG_TMS
PCH_JTAG_TDI K5 JTAG_TDI
PCH_JTAG_TDO H1 JTAG_TDO
JTAG

SPI_CLK_PCH T3 SPI_CLK
SPI_SB_CS0# Y14 SPI_CS0#
SPI_SB_CS1# T1 SPI_CS1#
SPI_SI V4 SPI_MOSI
SPI_SO_R U3 SPI_MISO
SPI

SATA
SATA0RXN AM3
SATA0RXP AM1
SATA0TXN AP7
SATA0TXP AP5
SATA_ITX_C_DRX_N0 0.01U_0402_16V7K C184
SATA_ITX_C_DRX_P0 0.01U_0402_16V7K C185
SATA_DTX_C_IRX_N0
SATA_DTX_C_IRX_P0
SATA_ITX_DRX_N0
SATA_ITX_DRX_P0
SATA_DTX_C_IRX_N0 <37>
SATA_DTX_C_IRX_P0 <37>
SATA_ITX_DRX_N0 <37>
SATA_ITX_DRX_P0 <37>
SSD

SATA1RXN AM10
SATA1RXP AM8
SATA1TXN AP11
SATA1TXP AP10
SATA_ITX_C_DRX_N1 0.01U_0402_16V7K C273
SATA_ITX_C_DRX_P1 0.01U_0402_16V7K C272
SATA_DTX_C_IRX_N1
SATA_DTX_C_IRX_P1
SATA_ITX_DRX_N1
SATA_ITX_DRX_P1
SATA_DTX_C_IRX_N1 <41>
SATA_DTX_C_IRX_P1 <41>
SATA_ITX_DRX_N1 <41>
SATA_ITX_DRX_P1 <41>
HDD

SATA2RXN AD7
SATA2RXP AD5
SATA2TXN AH5
SATA2TXP AH4
SATA_ITX_C_DRX_N2 0.01U_0402_16V7K C186
SATA_ITX_C_DRX_P2 0.01U_0402_16V7K C187
SATA_DTX_C_IRX_N2
SATA_DTX_C_IRX_P2
SATA_ITX_DRX_N2_CONN
SATA_ITX_DRX_P2_CONN
SATA_DTX_C_IRX_N2 <41>
SATA_DTX_C_IRX_P2 <41>
SATA_ITX_DRX_N2_CONN <41>
SATA_ITX_DRX_P2_CONN <41>
ODD

SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1

SATA4RXN Y7
SATA4RXP Y5
SATA4TXN AD3
SATA4TXP AD1
ESATA@
SATA_ITX_C_DRX_N4 0.01U_0402_16V7K C188
SATA_ITX_C_DRX_P4 0.01U_0402_16V7K C189
SATA_DTX_C_IRX_N4
SATA_DTX_C_IRX_P4
SATA_ITX_DRX_N4
SATA_ITX_DRX_P4
SATA_DTX_C_IRX_N4 <48>
SATA_DTX_C_IRX_P4 <48>
SATA_ITX_DRX_N4 <48>
SATA_ITX_DRX_P4 <48>
ESATA

SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1

SATAICOMPO Y11
SATAICOMPI Y10
R111 37.4_0402_1% +1.05VS_VCC_SATA
SATA_COMP

SATA3RCOMPO AB12
SATA3COMPI AB13
R113 49.9_0402_1% +1.05VS_SATA3
SATA3_COMP

SATA3RBIAS AH1
RBIAS_SATA3 R115 750_0402_1%

SATALED# P3
R117 10K_0402_5% +3VS
HDD_LED# <50>

SATA0GP / GPIO21 V14
PCH_GPIO21 R119 10K_0402_5% +3VS

SATA1GP / GPIO19 P1
SATA_DET# <37>
R316 10K_0402_5% +3VS

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+3VS
Q10 BSS138_NL_SOT23-3
@R325 0_0402_5%
6/17 follow module design

4MB SPI ROM FOR ME & Non-share ROM.
For Fast Boot

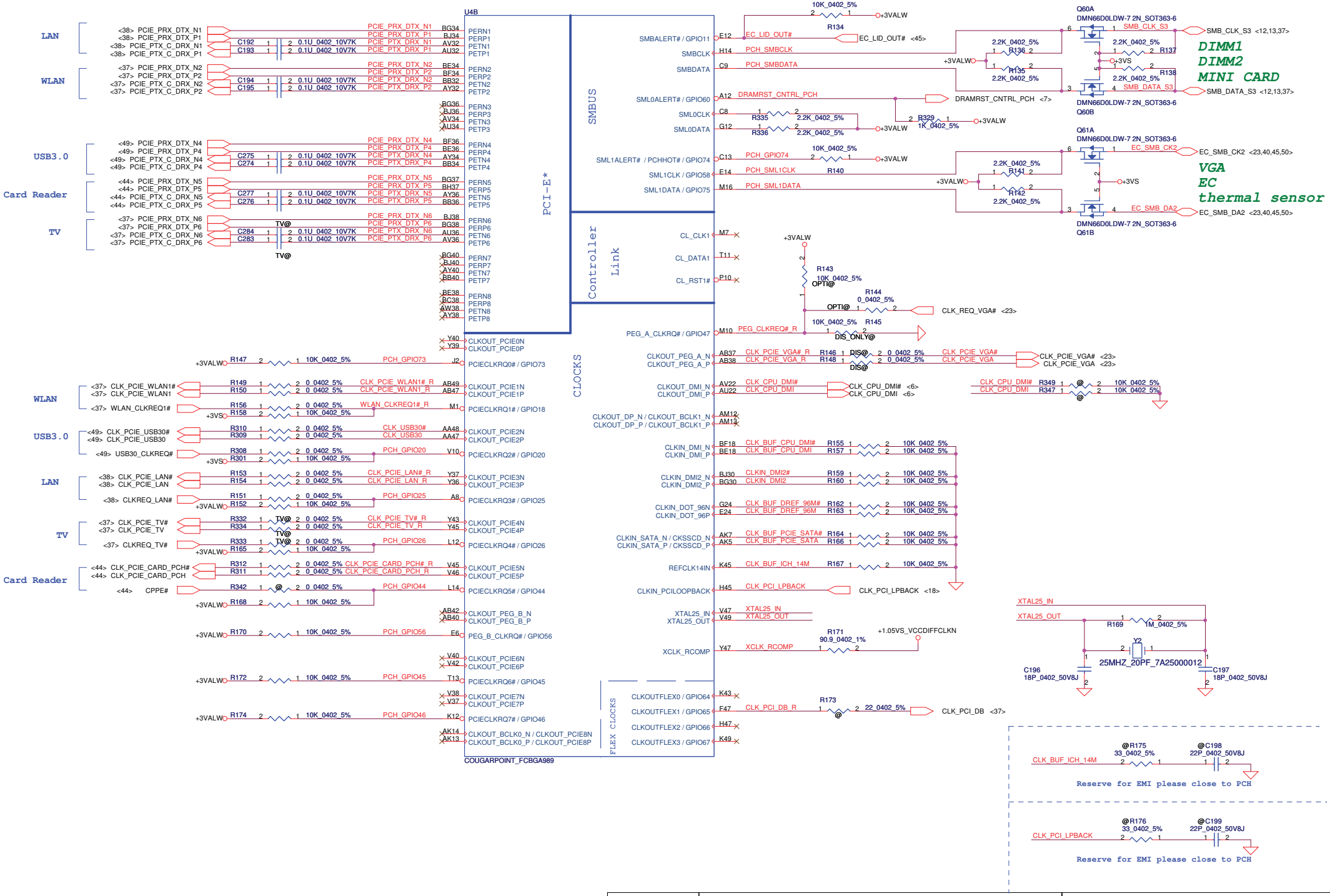
+3VS
R1334 3.3K_0402_5% SPI_WP#_1
R1335 3.3K_0402_5% SPI_HOLD#_1
@R1337 0_0402_5%
SPI_SB_CS1# SPI_SB_CS1#_R
SPI_SO_R SPI_SO_L1 SPI_WP#_1
@33_0402_5% R1338
U61
CS# VCC
SO HOLD#
WP# SCLK
GND SI
S IC FL 32M W25Q32BVSSIG SOIC 8P
C923 0.1U_0402_16V4Z
SPI_HOLD#_1 33_0402_5% R1340 SPI_CLK_PCH
SPI_CLK_PCH_1
SPI_SI_R1 SPI_SI
33_0402_5% R1339

+3VS
@ R1346 10K_0402_5%
SPI_SB_CS1#_R
<45> SPI_SB_CS0#_R
SPI_SB_CS0#_R
Q134 2N7002_SOT23-3

4MB SPI ROM FOR ME & Non-share ROM.
SPI_CLK_PCH
R124 33_0402_5% @
C190 22P_0402_50V8J @
+3VS
R127 3.3K_0402_5% SPI_WP#
R129 3.3K_0402_5% SPI_HOLD#
C191 0.1U_0402_16V4Z
R130 0_0402_5%
SPI_SB_CS0# SPI_SB_CS0#_R
SPI_SO_R SPI_SO_L SPI_WP#
33_0402_5% R131
U5
CS# VCC
SO HOLD#
WP# SCLK
GND SI
S IC FL 32M W25Q32BVSSIG SOIC 8P
SPI_HOLD# 33_0402_5% R1342 SPI_CLK_PCH
SPI_CLK_PCH
SPI_SI_R SPI_SI
33_0402_5% R133

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.
Title: PCH (1/8) SATA,HDA,SPI, LPC, XDP
Size: Custom | Document Number: LA-6882P | Rev: 0.2
Date: Wednesday, October 06, 2010 | Sheet 14 of 63



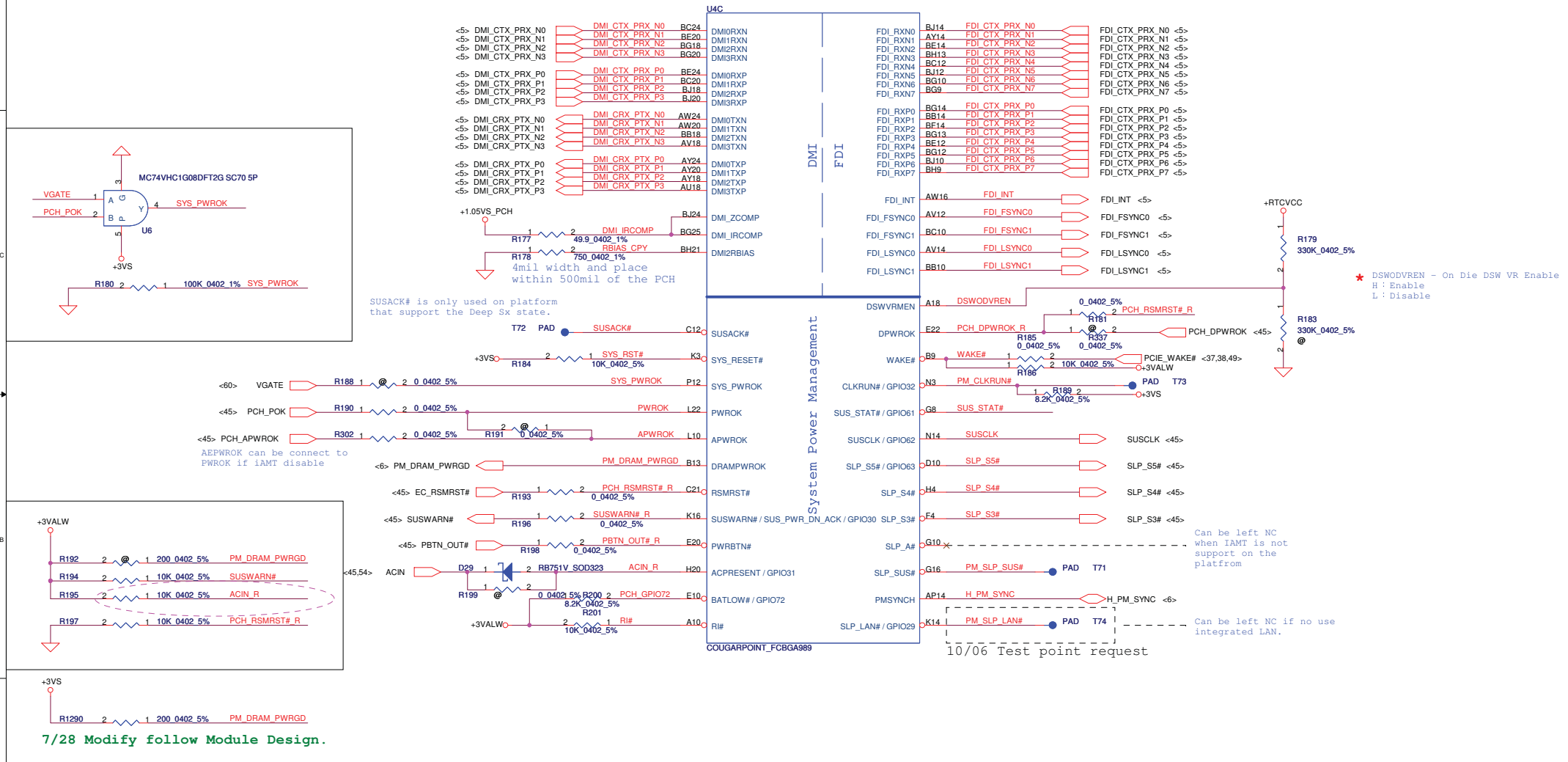
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

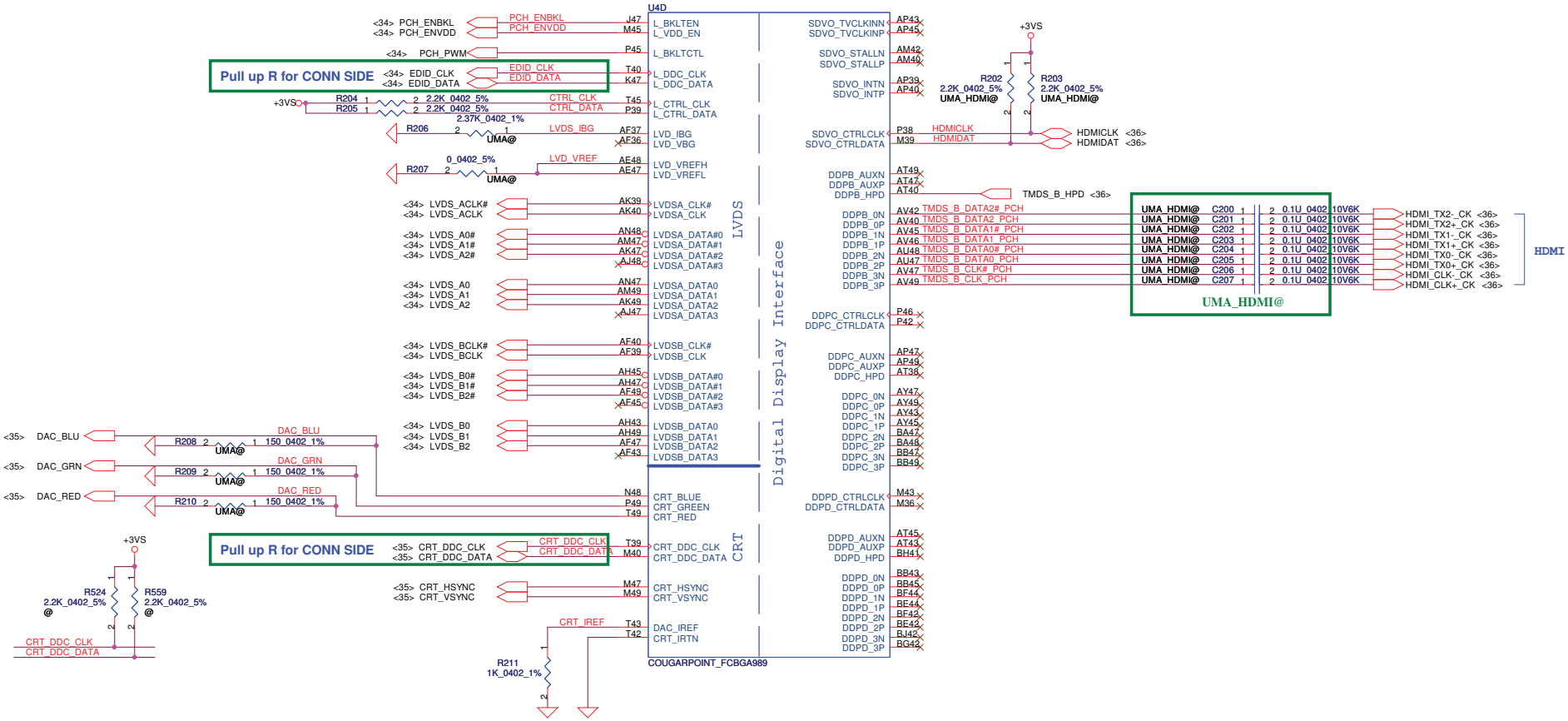
Size	Document Number	Rev
Custom	LA-6882P	0.2

Date: Wednesday, October 06, 2010 Sheet 15 of 63



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.		
Title	PCH (3/8) DMI,FDI,PM,	
Size: Custom	Document Number: LA-6882P	Rev: 0.2
Date: Wednesday, October 06, 2010	Sheet 16 of 63	



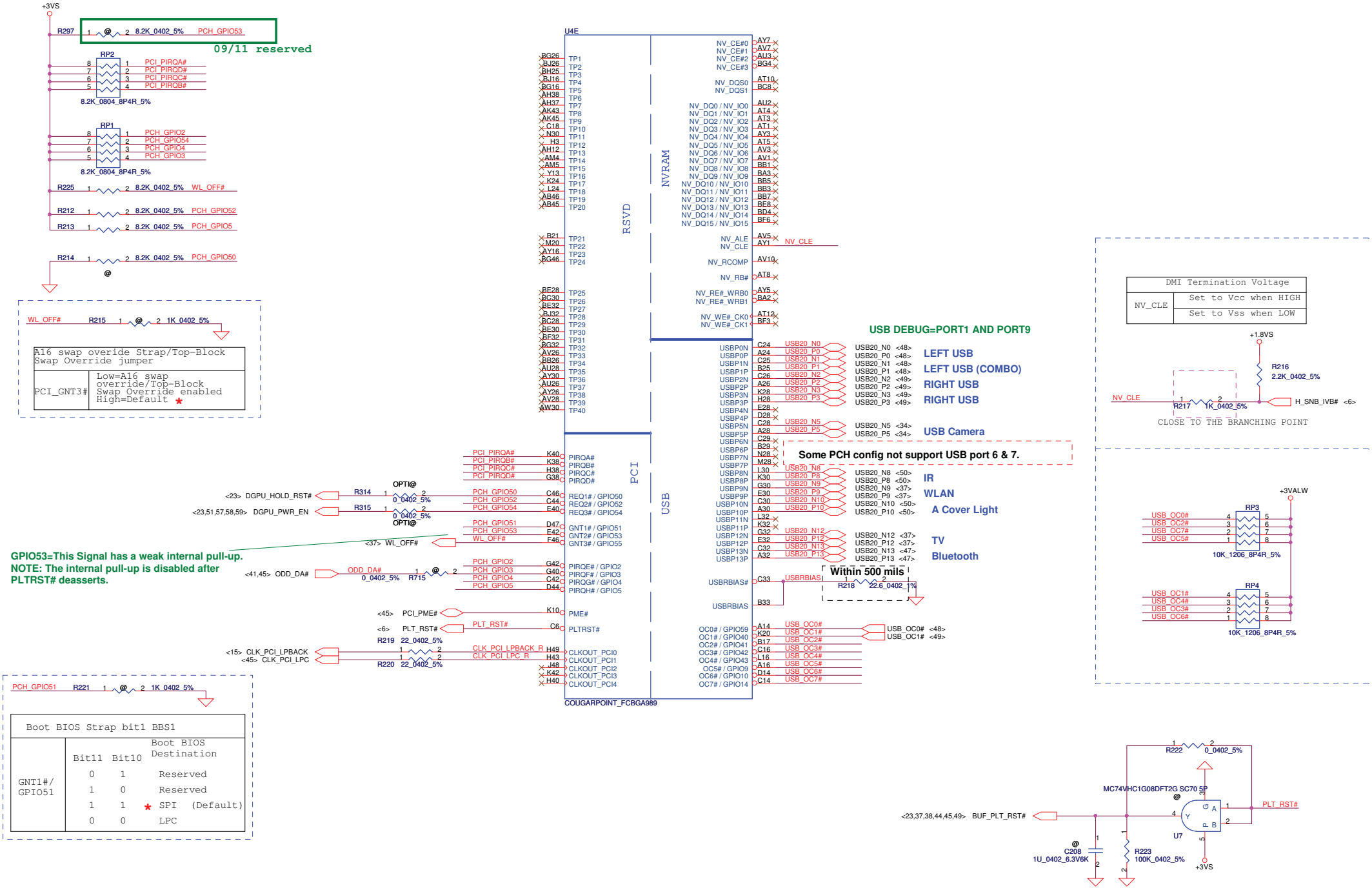
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size	Document Number	Rev
Custom	LA-6882P	0.2

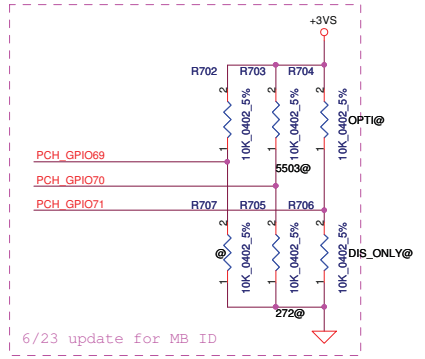
Date: Wednesday, October 06, 2010 Sheet 17 of 63



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.			
Title	PCH (5/9) PCI, USB		
Size: Custom	Document Number: LA-6882P		Rev: 0.2
Date: Wednesday, October 06, 2010	Sheet 18 of 63		

GPIO69	GPIO70	GPIO71
14": Low 15": Hi	ALC272: Low ALC5503: Hi	DIS ONLY: Low OPTIMUS: Hi
1	0	0
1	0	1
1	1	0
1	1	1



6/24 Change to @ follow module design
and double check on module design meeting

ICC_EN#
Integrated Clock Chip Enable
H ; Disable
L ; Enable
R235 1 @ 2 1K_0402_5% EC_SMI#
Weak internal pull-high

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable
R240 1 @ 2 1K_0402_5% PCH_GPIO28

PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable
R245 1 @ 2 10K_0402_5% PCH_GPIO27

+3VS R250 1 @ 2 200_0402_5% PCH_GPIO36
R264 1 2 10K_0402_5%

<48> ESATA_DET# 1 2 R340 0_0402_5% @ ESATA_DET_RR#
7/29 update for ESATA detect

+3VS R233 1 2 10K_0402_5% PCH_GPIO0
<48> ESATA_DET# 1 2 R303 0_0402_5%
R227 1 2 10K_0402_5% ESATA_DET_R#
+3VS R228 1 2 10K_0402_5% DEVICE_RST#
<37,38,44> DEVICE_RST#
<45> EC_SCI# EC_SCI#
<45> EC_SMI# EC_SMI#
+3VALW R229 1 @ 2 10K_0402_5% PCH_GPIO12
R230 1 @ 2 1K_0402_5% SMIB
<49> SMIB
+3VS R231 1 2 10K_0402_5% ESATA_DET_RR#
R232 1 @ 2 10K_0402_1%
<23,59> VGA_PGOOD 1 2 R339 0_0402_5% VGA_PGOOD_R
+3VS R238 1 2 10K_0402_5% BT_DISABLE
<37> BT_DISABLE
<41> ODD_EN ODD_EN
+3VALW
R241 1 2 10K_0402_5% PCH_GPIO27
<37,47> BT_OFF# 1 @ 2 R242 10K_0402_5% PCH_GPIO28
+3VS BT_OFF#
R243 1 2 10K_0402_5% PCH_GPIO35
R259 1 2 10K_0402_5% PCH_GPIO36
+3VS R244 1 @ 2 10K_0402_5% PCH_GPIO37
R246 1 2 10K_0402_5% PCH_GPIO38
R247 1 2 10K_0402_5% PCH_GPIO39
R248 1 2 10K_0402_5% PCH_GPIO48
+3VS R249 1 2 10K_0402_5% PCH_GPIO49
+3VALW R251 1 2 10K_0402_5% PCH_GPIO57
NO_VENTURA@
R1345 1 2 10K_0402_5%
VENTURA@

U4F

T7	BMBUSY# / GPIO0	TACH4 / GPIO68	C40 PCH_GPIO68
A42	TACH1 / GPIO1	TACH5 / GPIO69	B41 PCH_GPIO69
H36	TACH2 / GPIO6	TACH6 / GPIO70	C41 PCH_GPIO70
E38	TACH3 / GPIO7	TACH7 / GPIO71	A40 PCH_GPIO71
C10	GPIO8		
C4	LAN_PHY_PWR_CTRL / GPIO12		
G2	GPIO15	A20GATE	P4 GATEA20 <45>
U2	SATA4GP / GPIO16	PECI	AU16 PCH_PECI_R 0_0402_5% R237 H_PECI <6,45>
D40	TACH0 / GPIO17	RCIN#	P5 KB_RST# KB_RST# <45>
T5	SCLOCK / GPIO22	PROCPWRGD	AY11 H_CPUPWRGD <6>
E8	GPIO24 / MEM_LED	THRMTRIP#	AY10 PCH_THRMTRIP#_R R239 390_0402_5% H_THRMTRIP# H_THRMTRIP# <6>
E16	GPIO27	INIT3_3V#	T14 PCH_THRMTRIP#_R <23>
P8	GPIO28		
K1	STP_PCI# / GPIO34	NC_1	AH8
K4	GPIO35	NC_2	AK11
V8	SATA2GP / GPIO36	NC_3	AH10
M5	SATA3GP / GPIO37	NC_4	AK10
N2	SLOAD / GPIO38	NC_5	P37
M3	SDATAOUT0 / GPIO39		
V13	SDATAOUT1 / GPIO48	VSS_NCTF_15	BG2 VSS_NCTF_15
V3	SATA5GP / GPIO49	VSS_NCTF_16	BG48 VSS_NCTF_16
D6	GPIO57	VSS_NCTF_17	BH3 VSS_NCTF_17
		VSS_NCTF_18	BH47 VSS_NCTF_18
A4	VSS_NCTF_1	VSS_NCTF_19	BJ4 VSS_NCTF_19
A44	VSS_NCTF_2	VSS_NCTF_20	BJ44 VSS_NCTF_20
A45	VSS_NCTF_3	VSS_NCTF_21	BJ45 VSS_NCTF_21
A46	VSS_NCTF_4	VSS_NCTF_22	BJ46 VSS_NCTF_22
A5	VSS_NCTF_5	VSS_NCTF_23	BJ5 VSS_NCTF_23
A6	VSS_NCTF_6	VSS_NCTF_24	BJ6 VSS_NCTF_24
B3	VSS_NCTF_7	VSS_NCTF_25	C2 VSS_NCTF_25
B47	VSS_NCTF_8	VSS_NCTF_26	C48 VSS_NCTF_26
BD1	VSS_NCTF_9	VSS_NCTF_27	D1 VSS_NCTF_27
BD49	VSS_NCTF_10	VSS_NCTF_28	D49 VSS_NCTF_28
BE1	VSS_NCTF_11	VSS_NCTF_29	E1 VSS_NCTF_29
BE49	VSS_NCTF_12	VSS_NCTF_30	F49 VSS_NCTF_30
BF1	VSS_NCTF_13	VSS_NCTF_31	F1 VSS_NCTF_31
BF49	VSS_NCTF_14	VSS_NCTF_32	F49 VSS_NCTF_32

GPIO | CPU/MISC | NCTF

COUGARPOINT_FCBGA989

+3VS R236 10K_0402_5%

PCH_GPIO68 R224 1 2 10K_0402_5%
KB_RST# R226 1 2 10K_0402_5%

INIT3_3V
This signal has weak internal PU, can't pull low

Intel schematic reviwe recommand.

Change VSS_NCTF pin form TEST point to Trace for layout SPACE reducing..

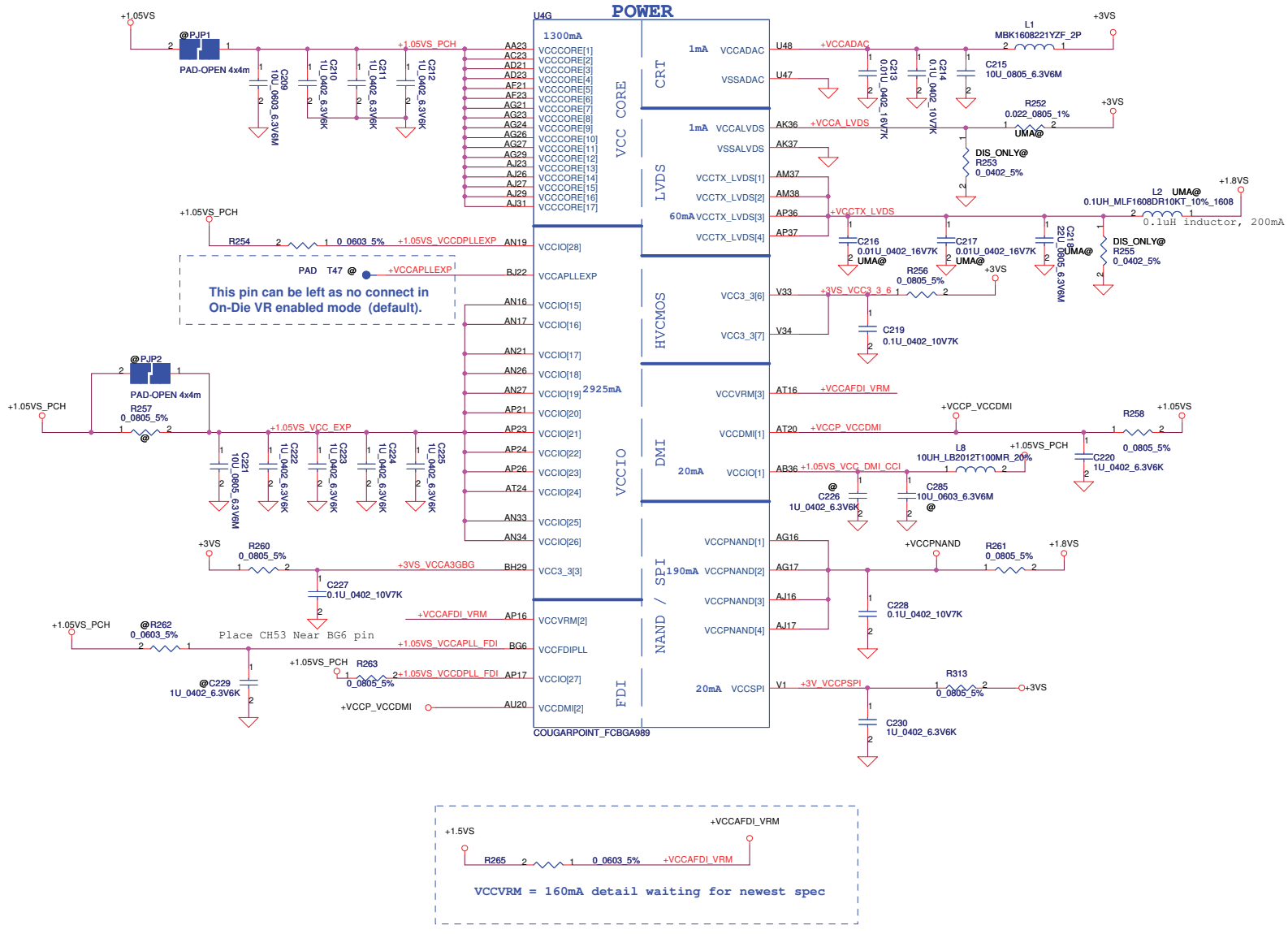
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: LA-6882P | Rev: 0.2

Date: Wednesday, October 06, 2010 | Sheet 19 of 63



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: LA-6882P | Rev: 0.2

Date: Wednesday, October 06, 2010 | Sheet 20 of 63

Have internal VRM

VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

POWER

U4J

OSCAN
SF000001500
(220U 6.3V M V LESR15M VL H5.9)*2

COUGARPOINT_FCBGA989

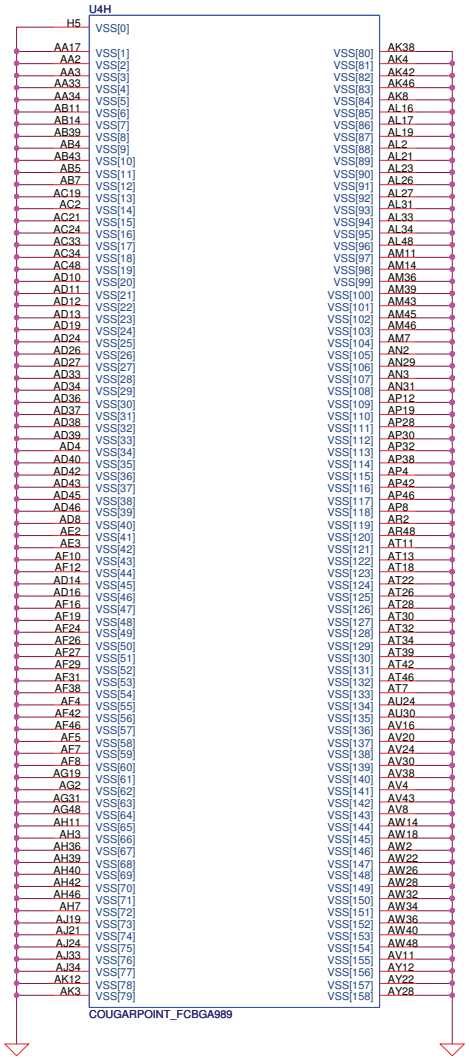
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

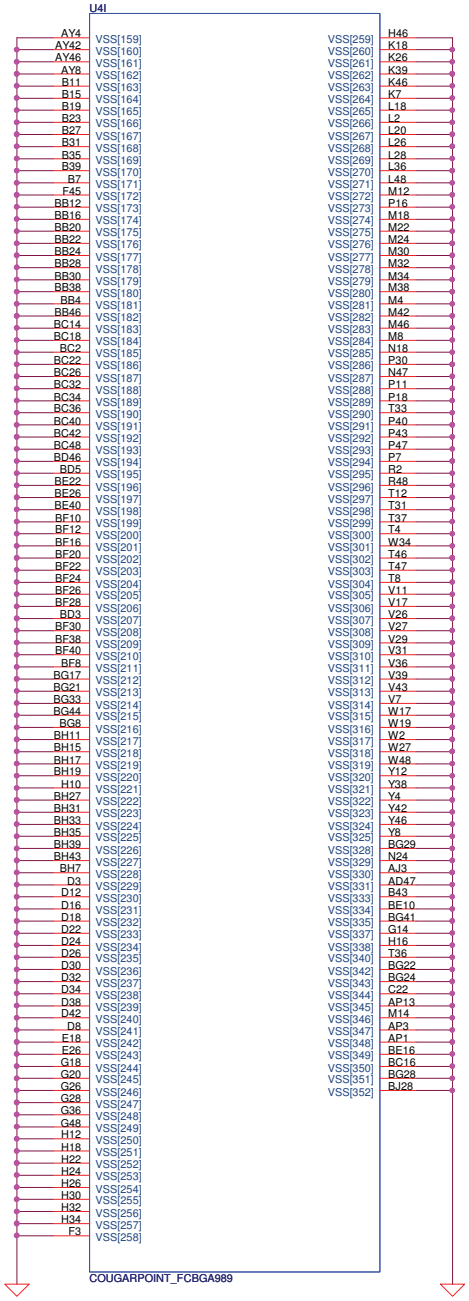
Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size: Custom | Document Number: LA-6882P | Rev: 0.2

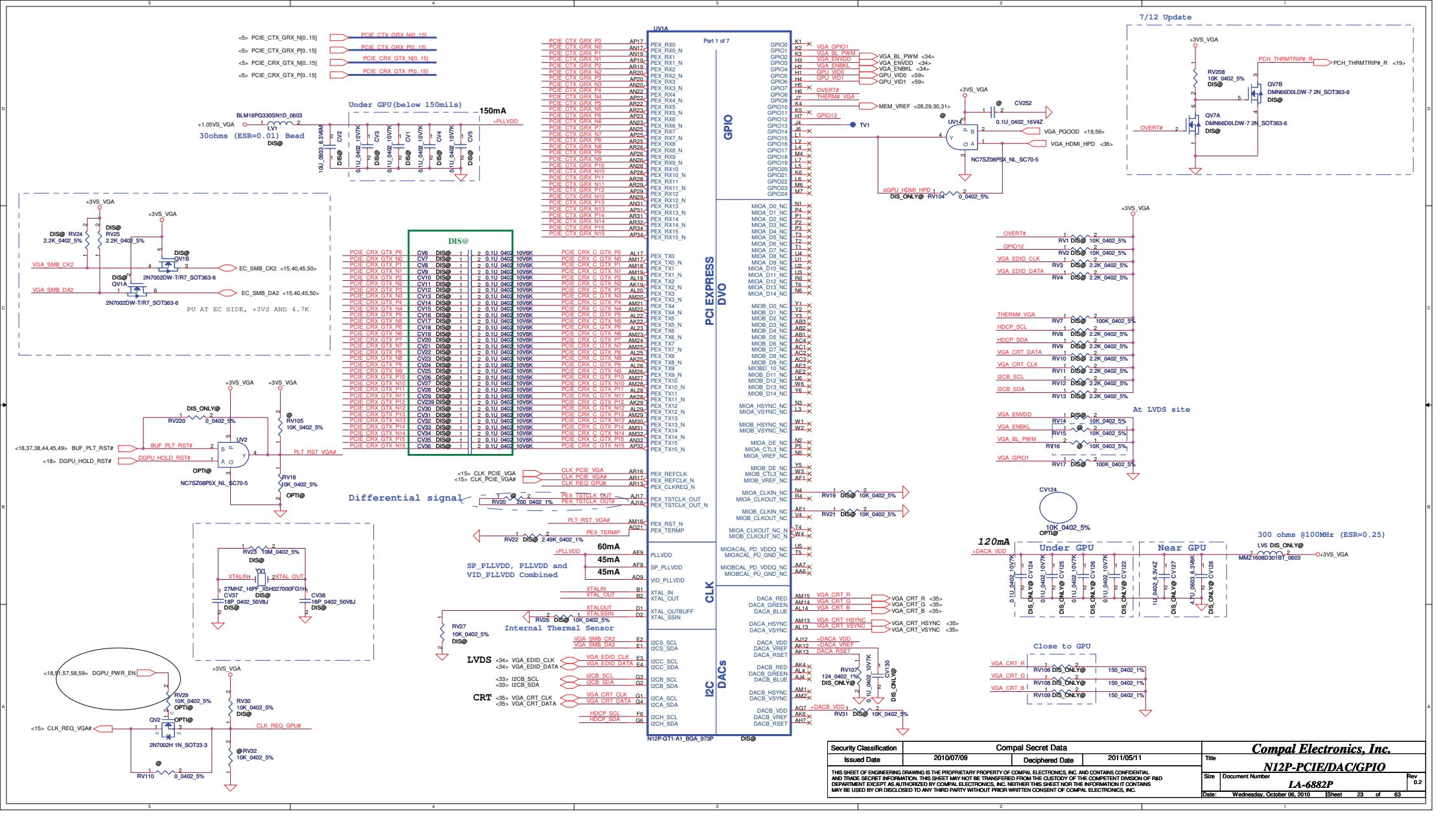
Date: Wednesday, October 06, 2010 | Sheet 21 of 63





Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.			
Title	PCH (9/9) VSS		
Size: Custom	Document Number: LA-6882P		Rev: 0.2
Date: Wednesday, October 06, 2010	Sheet 22 of 63		



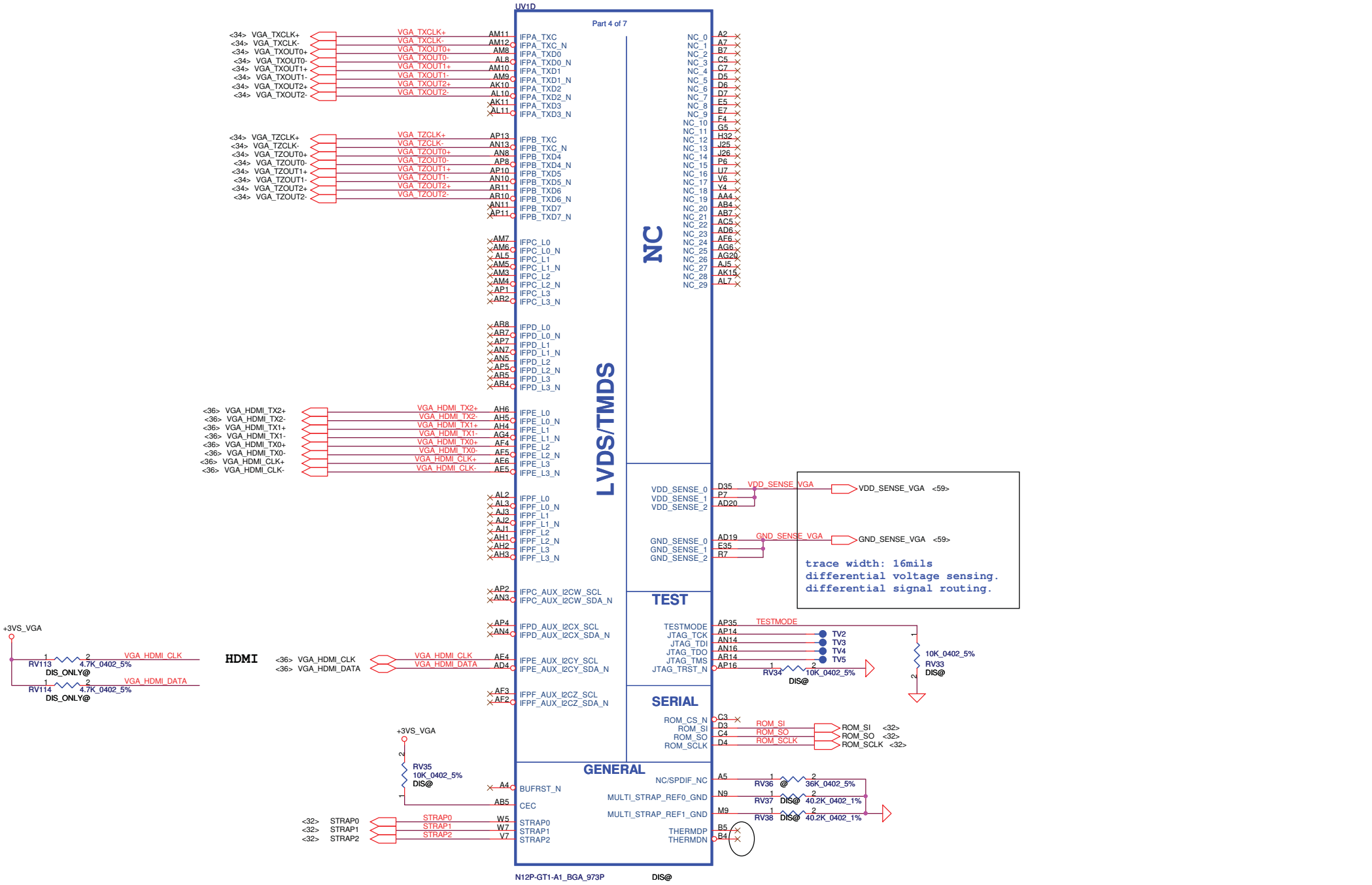
Security Classification	Compal Secret Data		
Issued Date	2010/07/09	Deciphered Date	2011/05/11

Compal Electronics, Inc.

Title: N12P-PCIE/DAC/GPIO

Size	Document Number	Rev
	LA-6882P	0.2

Date: Wednesday, October 06, 2010 | Sheet 23 of 63



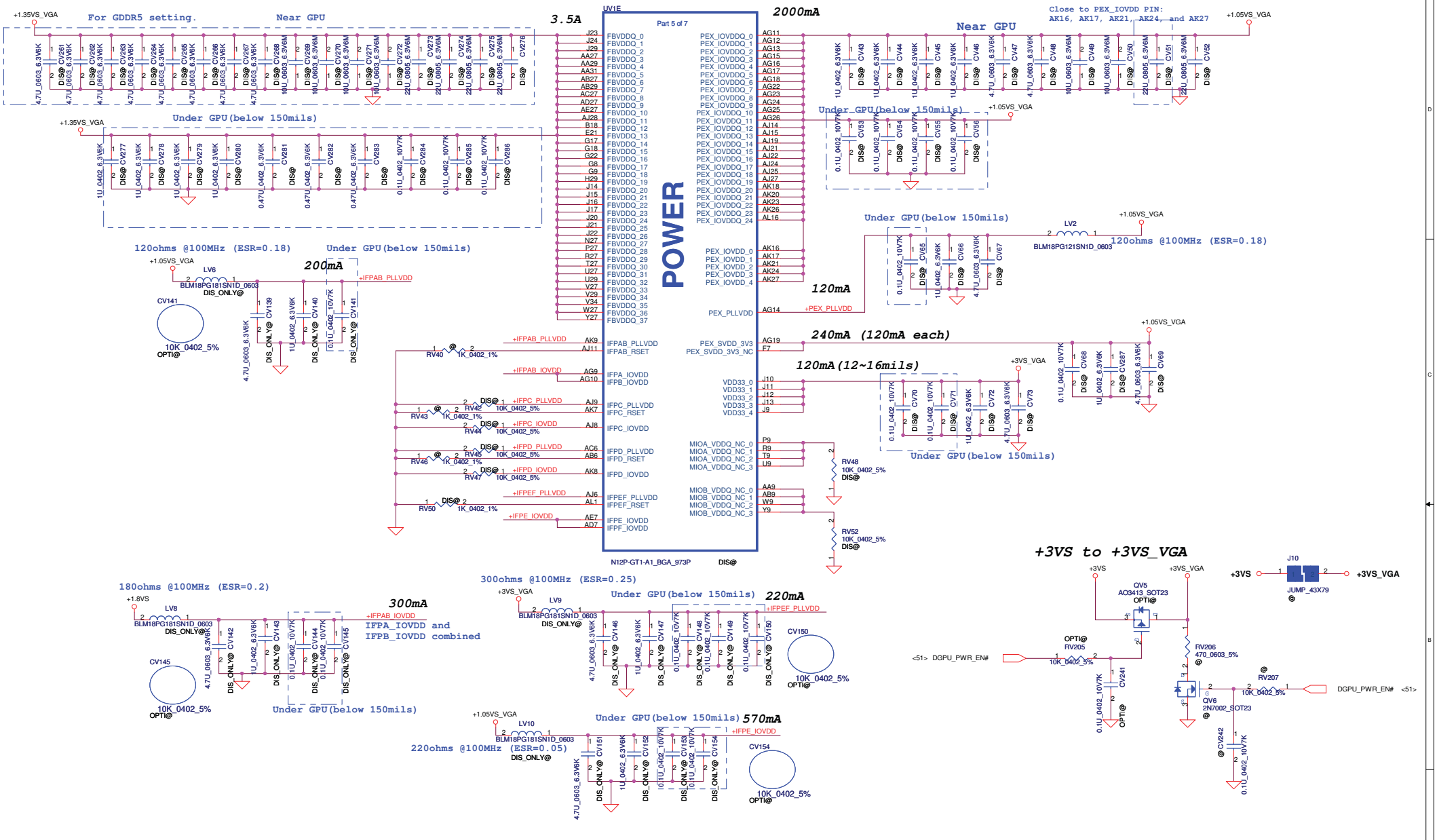
Security Classification	Compal Secret Data		
Issued Date	2010/07/09	Deciphered Date	2011/05/11

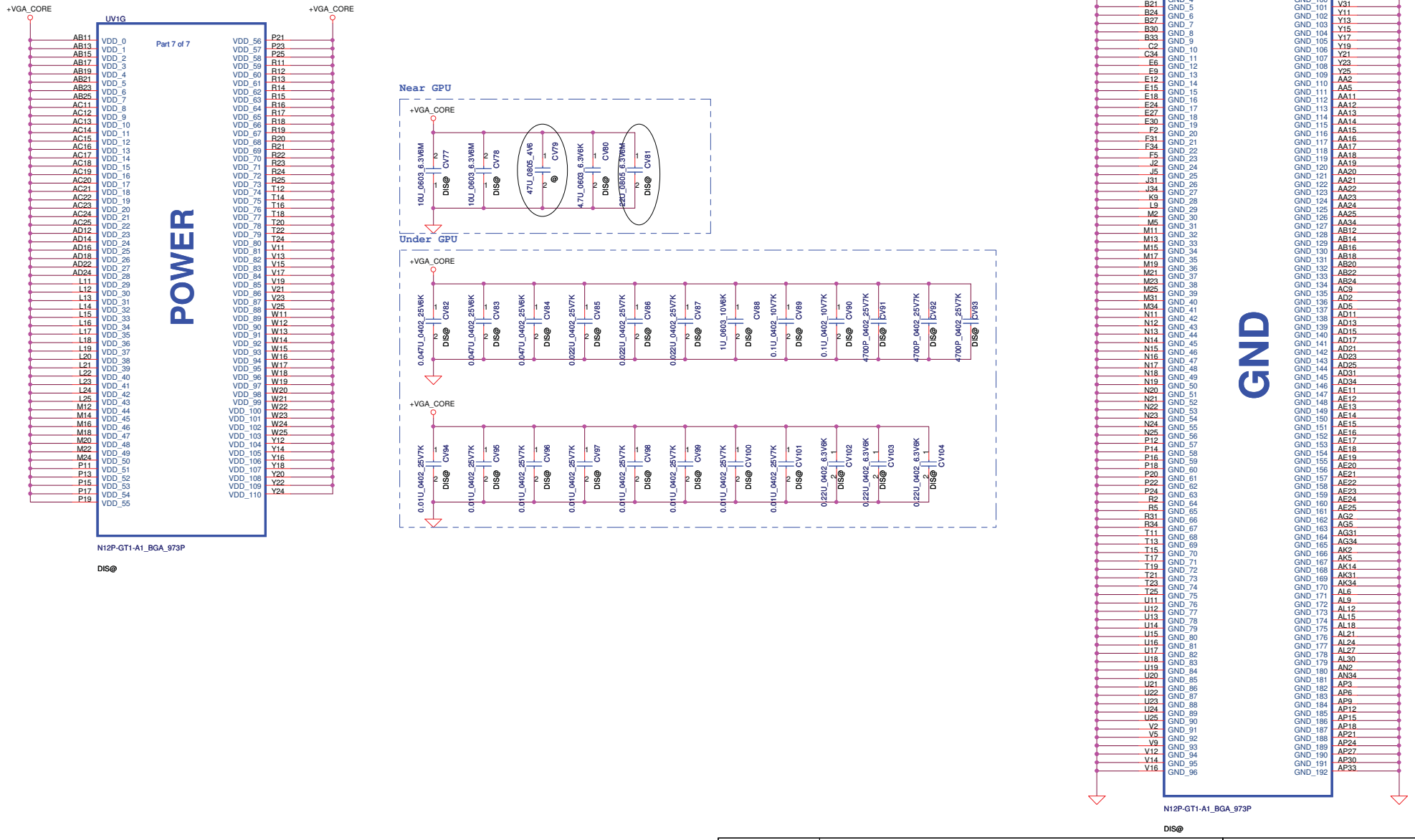
Compal Electronics, Inc.

Title: **N12P-LVDS/HDMI/DP/THM**

Size	Document Number	Rev
	LA-6882P	0.2

Date: Wednesday, October 06, 2010 | Sheet 24 of 63


POWER
UV1E
Part 5 of 7
N12P-GT1-A1_BGA_973P
DIS@
3.5A
2000mA
Near GPU
Close to PEX_IOVDD PIN:
AK16, AK17, AK21, AK24, and AK27
Under GPU(below 150mils)
For GDDR5 setting.
120ohms @100MHz (ESR=0.18)
200mA
120mA
240mA (120mA each)
120mA(12~16mils)
180ohms @100MHz (ESR=0.2)
300mA
IFPA_IOVDD and
IFPB_IOVDD combined
300ohms @100MHz (ESR=0.25)
220mA
220ohms @100MHz (ESR=0.05)
570mA
+3VS to +3VS_VGA
+1.35VS_VGA
+1.05VS_VGA
+3VS_VGA
+1.8VS
+3VS
+PEX_PLLVDD
+IFPAB_PLLVDD
+IFPAB_IOVDD
+IFPC_PLLVDD
+IFPC_IOVDD
+IFPD_PLLVDD
+IFPD_IOVDD
+IFPEF_PLLVDD
+IFPE_IOVDD
<51> DGPU_PWR_EN#
DGPU_PWR_EN# <51>
Security Classification
Compal Secret Data
Issued Date
2010/07/09
Deciphered Date
2011/05/11
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.
Compal Electronics, Inc.
Title
N12P-POWER
Size
Document Number
LA-6882P
Rev
0.2
Date: Wednesday, October 06, 2010
Sheet 25 of 63



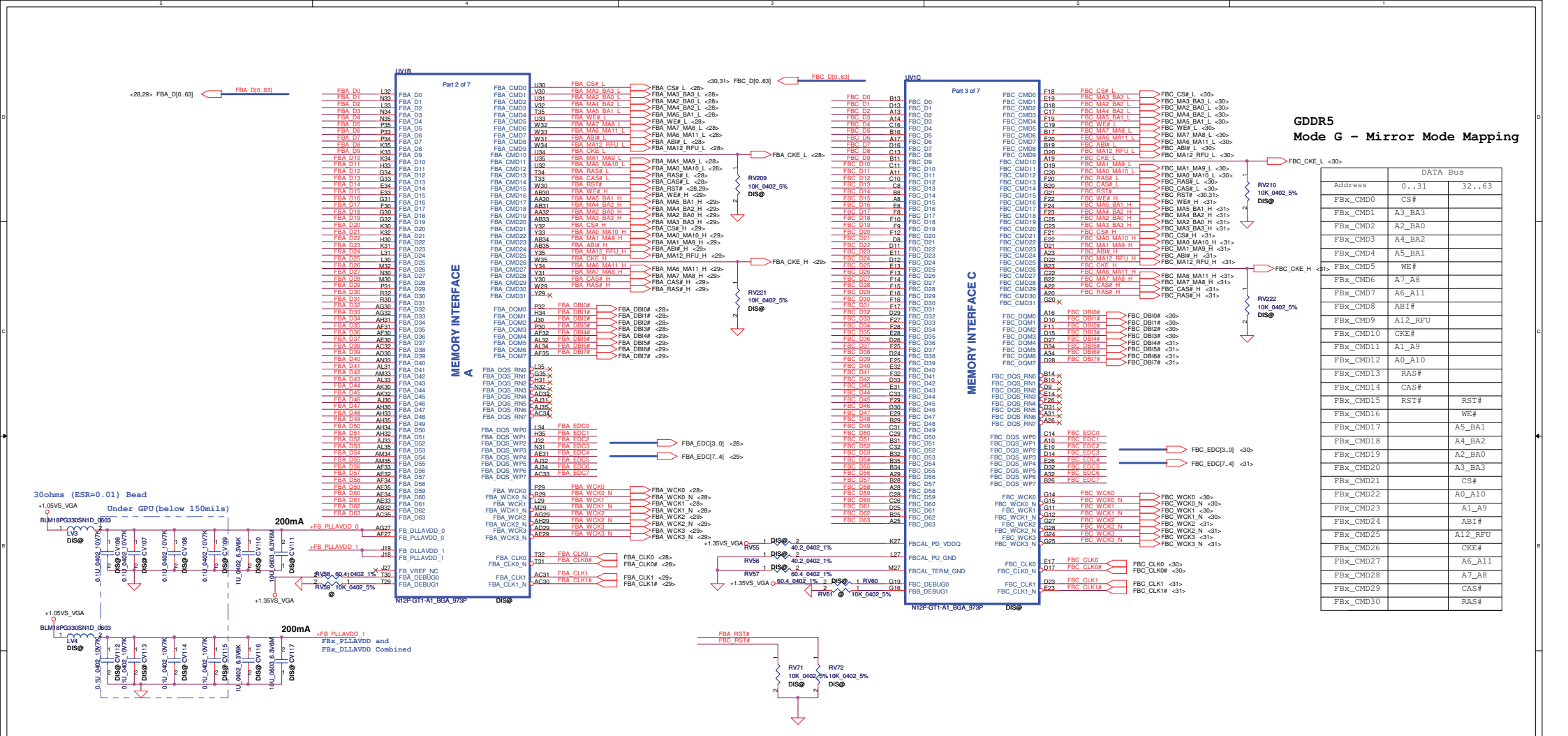
Security Classification	Compal Secret Data		
Issued Date	2010/07/09	Deciphered Date	2011/05/11

Compal Electronics, Inc.

Title: **N12P-VGA CORE, GND**

Size	Document Number	Rev
	LA-6882P	0.2

Date: Wednesday, October 06, 2010 | Sheet 26 of 63



Security Classification	Compal Secret Data		
Issued Date	2010/07/09	Deciphered Date	2011/05/11

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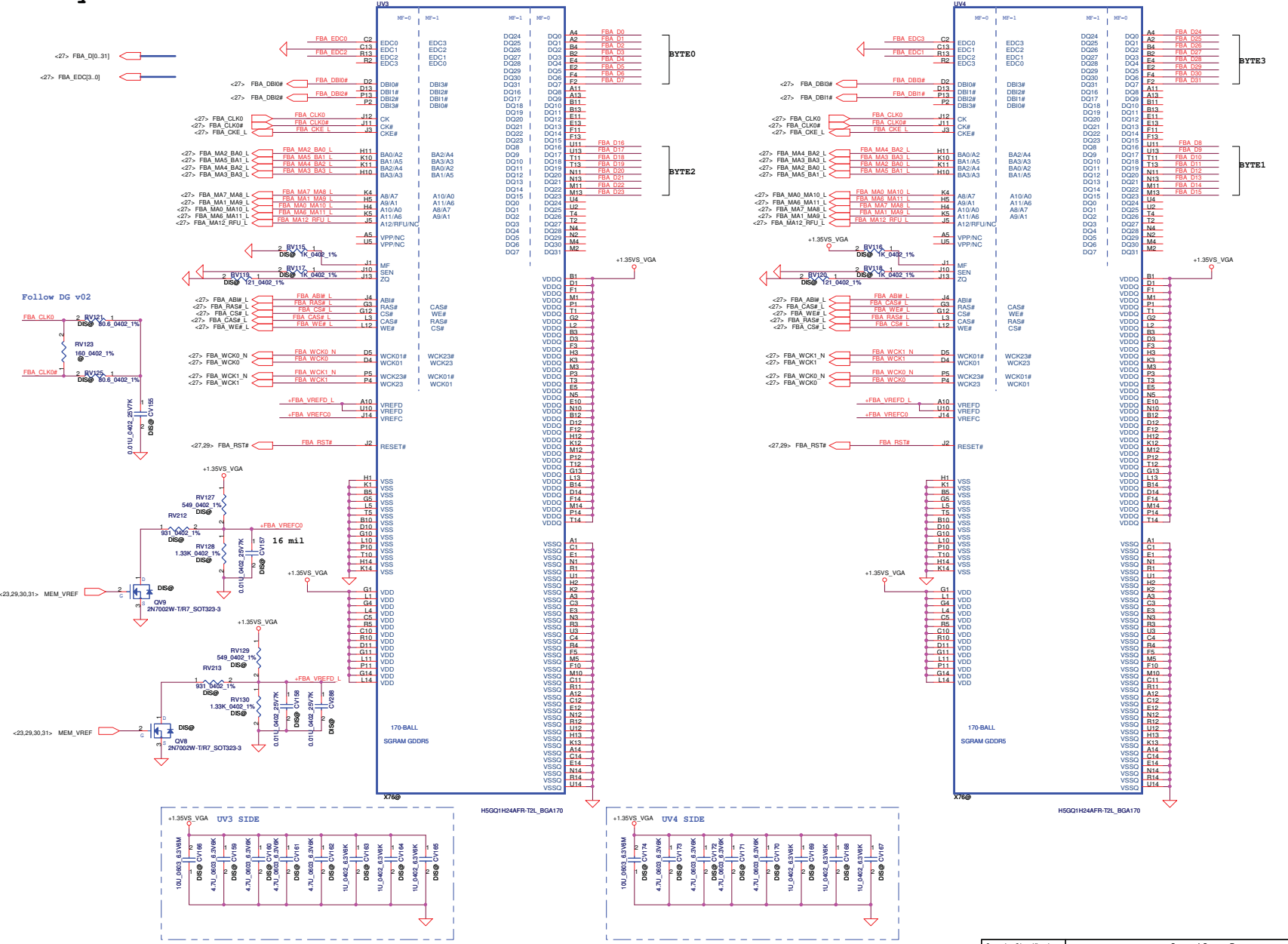
Compal Electronics, Inc.

Title: **N12P-MEM Interface**

Size: | Document Number: **LA-6882P** | Rev: 0.2

Date: Wednesday, October 06, 2010 | Sheet 27 of 63

Memory Partition A - Lower 32 bits



GDDR5
Mode G - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	CKE#	
FBx_CMD11	A1_A9	
FBx_CMD12	A0_A10	
FBx_CMD13	RAS#	
FBx_CMD14	CAS#	
FBx_CMD15	RST#	RST#
FBx_CMD16		WE#
FBx_CMD17		A5_BA1
FBx_CMD18		A4_BA2
FBx_CMD19		A2_BA0
FBx_CMD20		A3_BA3
FBx_CMD21		CS#
FBx_CMD22		A0_A10
FBx_CMD23		A1_A9
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		CKE#
FBx_CMD27		A6_A11
FBx_CMD28		A7_A8
FBx_CMD29		CAS#
FBx_CMD30		RAS#

Security Classification	Compal Secret Data		
Issued Date	2010/07/09	Deciphered Date	2011/05/11

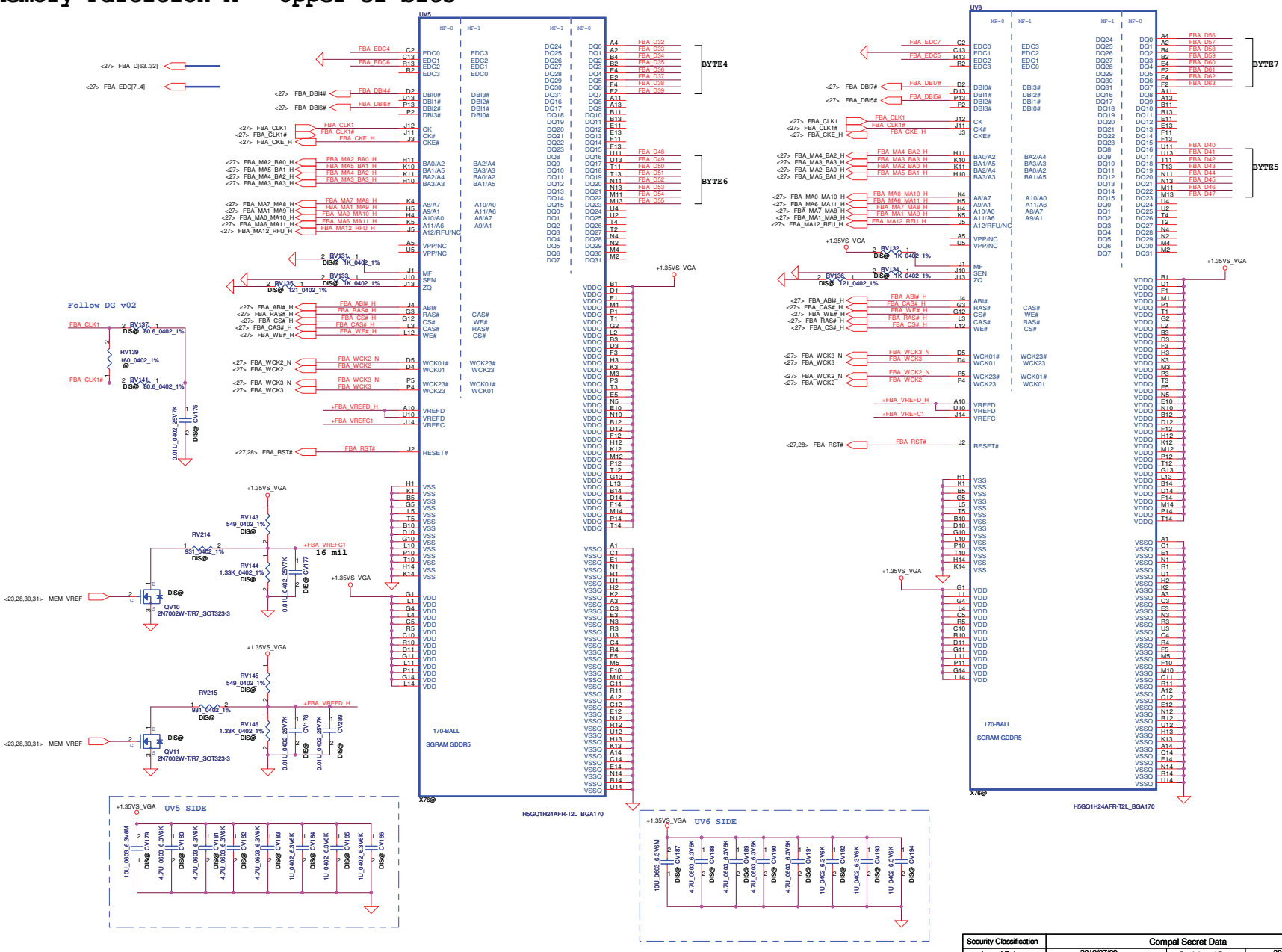
Compal Electronics, Inc.

Title: N12P-VRAM A Lower

Size: | Document Number: LA-6882P | Rev: 0.2

Date: Wednesday, October 06, 2010 | Sheet 28 of 83

Memory Partition A - Upper 32 bits



GDDR5
Mode G - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	CKE#	
FBx_CMD11	A1_A9	
FBx_CMD12	A0_A10	
FBx_CMD13	RAS#	
FBx_CMD14	CAS#	
FBx_CMD15	RST#	RST#
FBx_CMD16		WE#
FBx_CMD17		A5_BA1
FBx_CMD18		A4_BA2
FBx_CMD19		A2_BA0
FBx_CMD20		A3_BA3
FBx_CMD21		CS#
FBx_CMD22		A0_A10
FBx_CMD23		A1_A9
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		CKE#
FBx_CMD27		A6_A11
FBx_CMD28		A7_A8
FBx_CMD29		CAS#
FBx_CMD30		RAS#

Compal Electronics, Inc.

Title: N12P-VRAM A Upper

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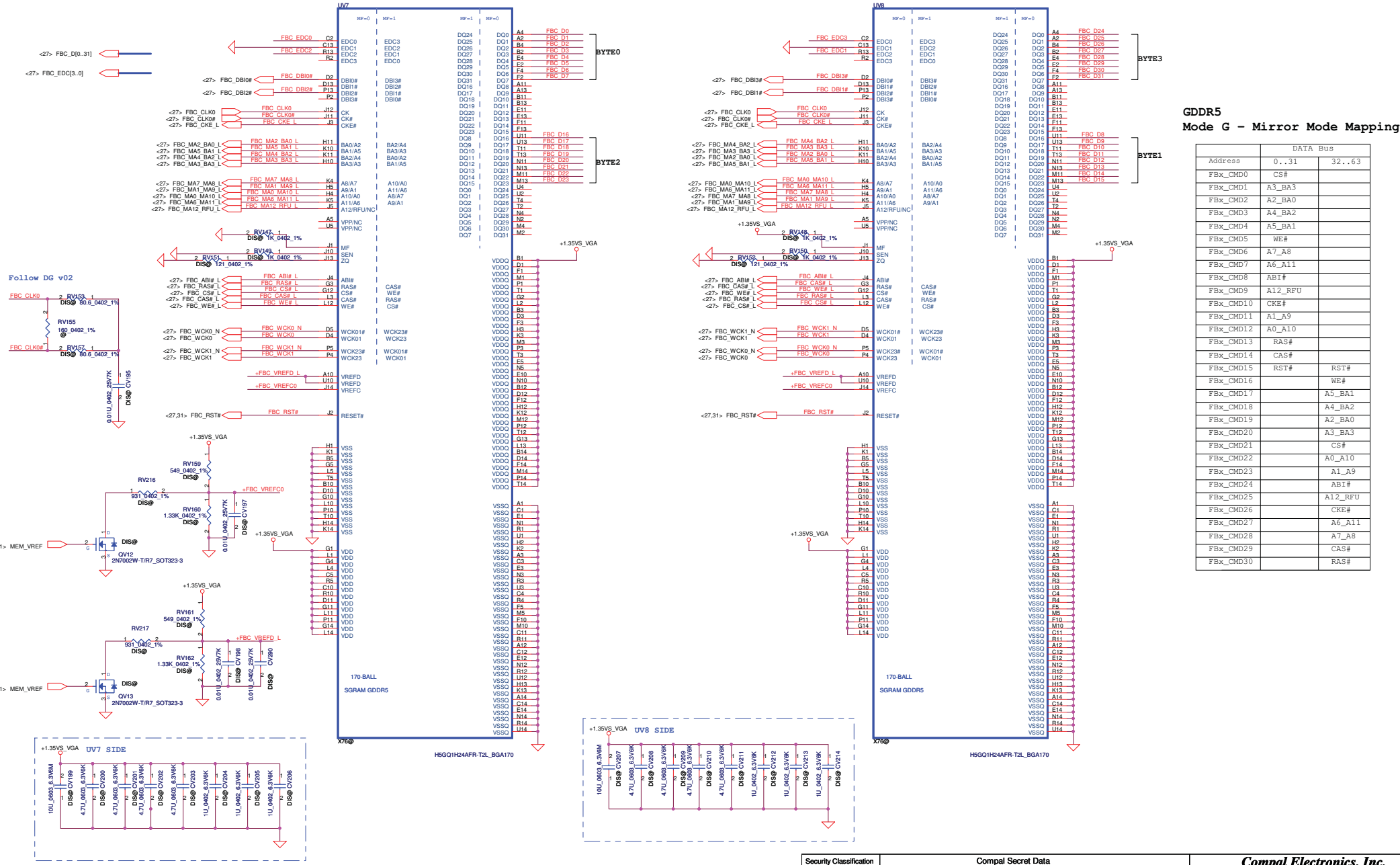
Date: Wednesday, October 06, 2010 | Sheet 29 of 83

Memory Partition C - Lower 32 bits



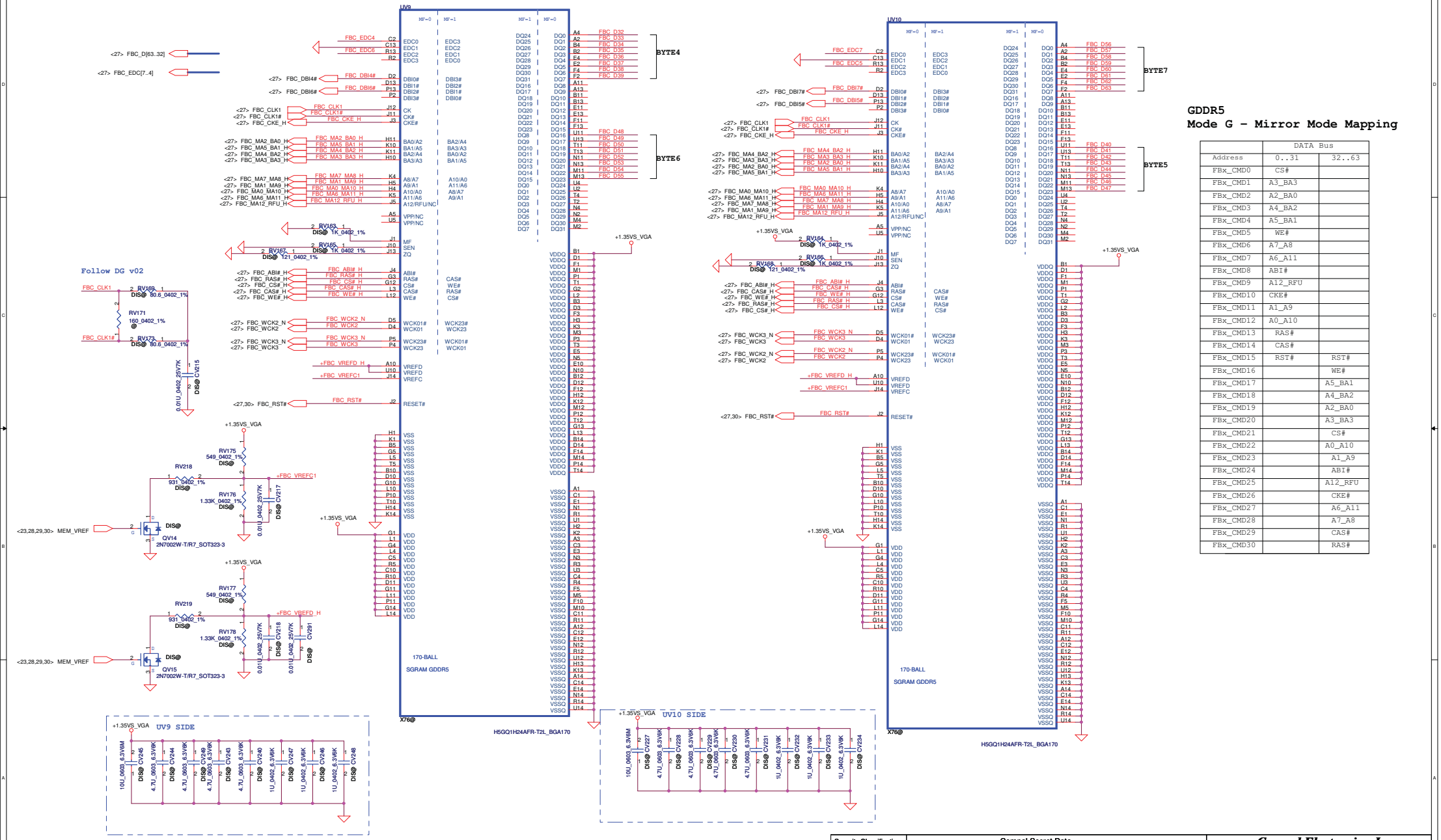
GDDR5
Mode G - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	CKE#	
FBx_CMD11	A1_A9	
FBx_CMD12	A0_A10	
FBx_CMD13	RAS#	
FBx_CMD14	CAS#	
FBx_CMD15	RST#	RST#
FBx_CMD16		WE#
FBx_CMD17		A5_BA1
FBx_CMD18		A4_BA2
FBx_CMD19		A2_BA0
FBx_CMD20		A3_BA3
FBx_CMD21		CS#
FBx_CMD22		A0_A10
FBx_CMD23		A1_A9
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		CKE#
FBx_CMD27		A6_A11
FBx_CMD28		A7_A8
FBx_CMD29		CAS#
FBx_CMD30		RAS#

Security Classification	Compal Secret Data		
Issued Date	2010/07/09	Deciphered Date	2011/05/11

Compal Electronics, Inc.		
Title: N12P-VRAM C Lower		
Size: Custom	Document Number: LA-6882P	Rev: 0.2
Date: Wednesday, October 06, 2010	Sheet 30 of 63	

Memory Partition C – Upper 32 bits



GDDR5
Mode G – Mirror Mode Mapping

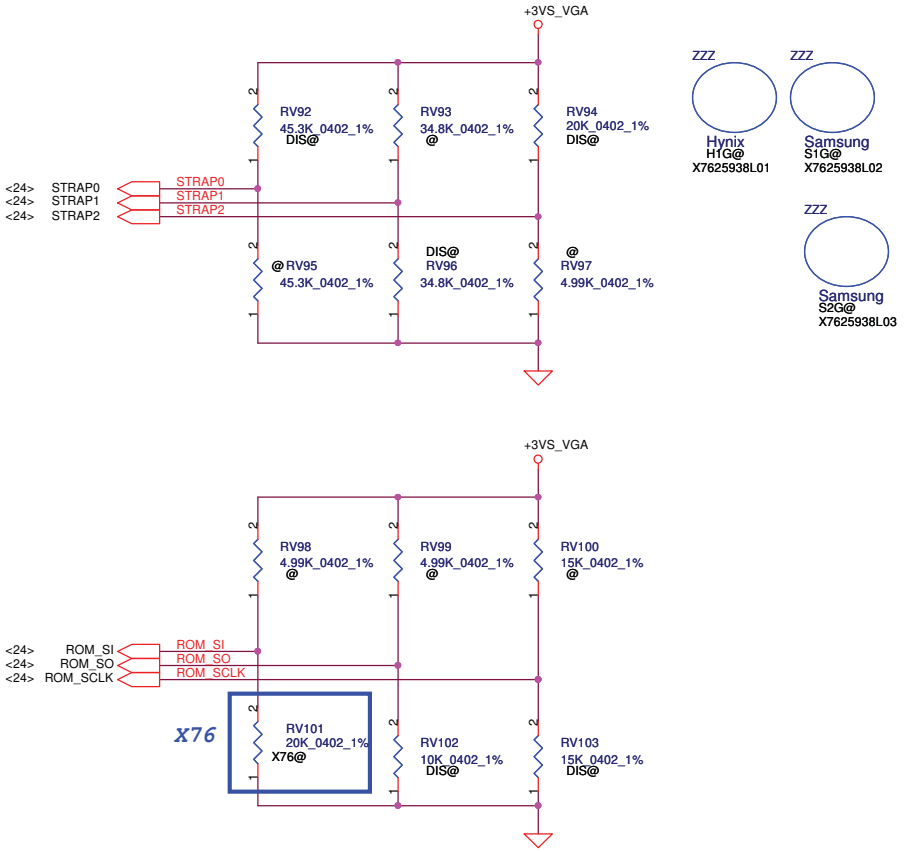
	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	CKE#	
FBx_CMD11	A1_A9	
FBx_CMD12	A0_A10	
FBx_CMD13	RAS#	
FBx_CMD14	CAS#	
FBx_CMD15	RST#	RST#
FBx_CMD16		WE#
FBx_CMD17		A5_BA1
FBx_CMD18		A4_BA2
FBx_CMD19		A2_BA0
FBx_CMD20		A3_BA3
FBx_CMD21		CS#
FBx_CMD22		A0_A10
FBx_CMD23		A1_A9
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		CKE#
FBx_CMD27		A6_A11
FBx_CMD28		A7_A8
FBx_CMD29		CAS#
FBx_CMD30		RAS#

Compal Electronics, Inc.

Title: N12P-VRAM C Upper

Size: Custom | Document Number: LA-6882P | Rev: 0.2

Date: Wednesday, October 06, 2010 | Sheet 31 of 63



ZZZ
Hynix
H1G@
X7625938L01

ZZZ
Samsung
S1G@
X7625938L02

ZZZ
Samsung
S2G@
X7625938L03

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_VGA	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

GPU	FB Memory (GDDR5)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N12P-GT1	Samsung 1800MHz (defaul)	K4G10325FE-HC04						
		32Mx32	PD 10K	PD 15K	PD 20K	PU 20K	PD 35K	PU 45K
	Hynix 1600MHz	H5GQ1H24AFR-T2L						
		32Mx32	PD 10K	PD 15K	PD 15K	PU 20K	PD 35K	PU 45K
					X76			

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XCLK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

Security Classification	Compal Secret Data		
Issued Date	2010/07/09	Deciphered Date	2011/05/11

Compal Electronics, Inc.

Title: N12P_MISC

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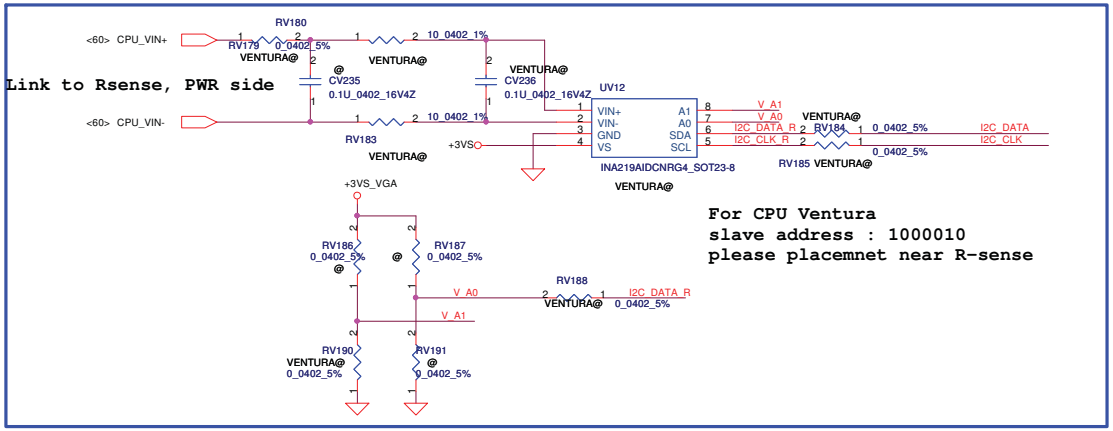
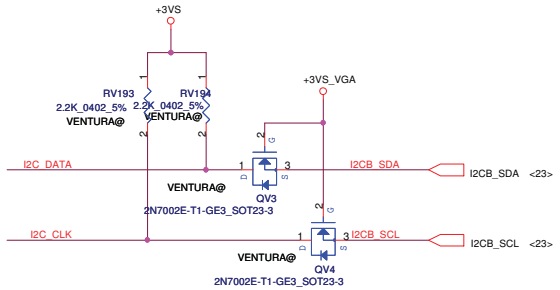
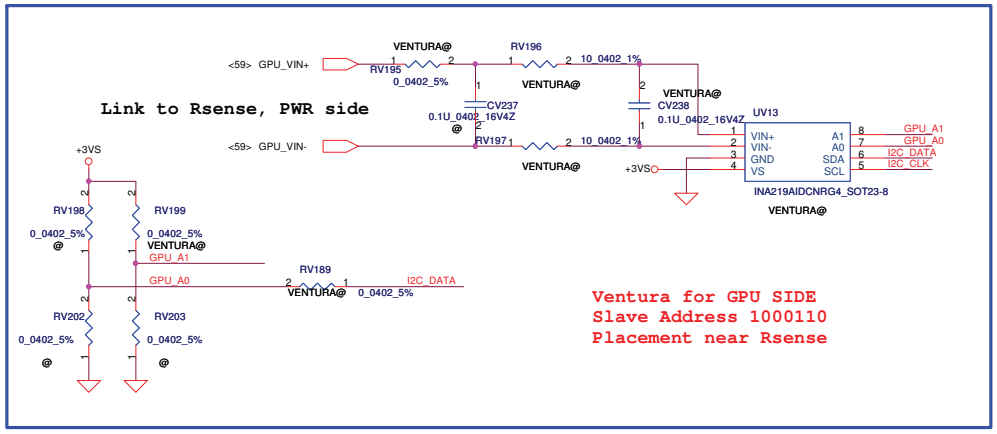
TOP side (under inductor)







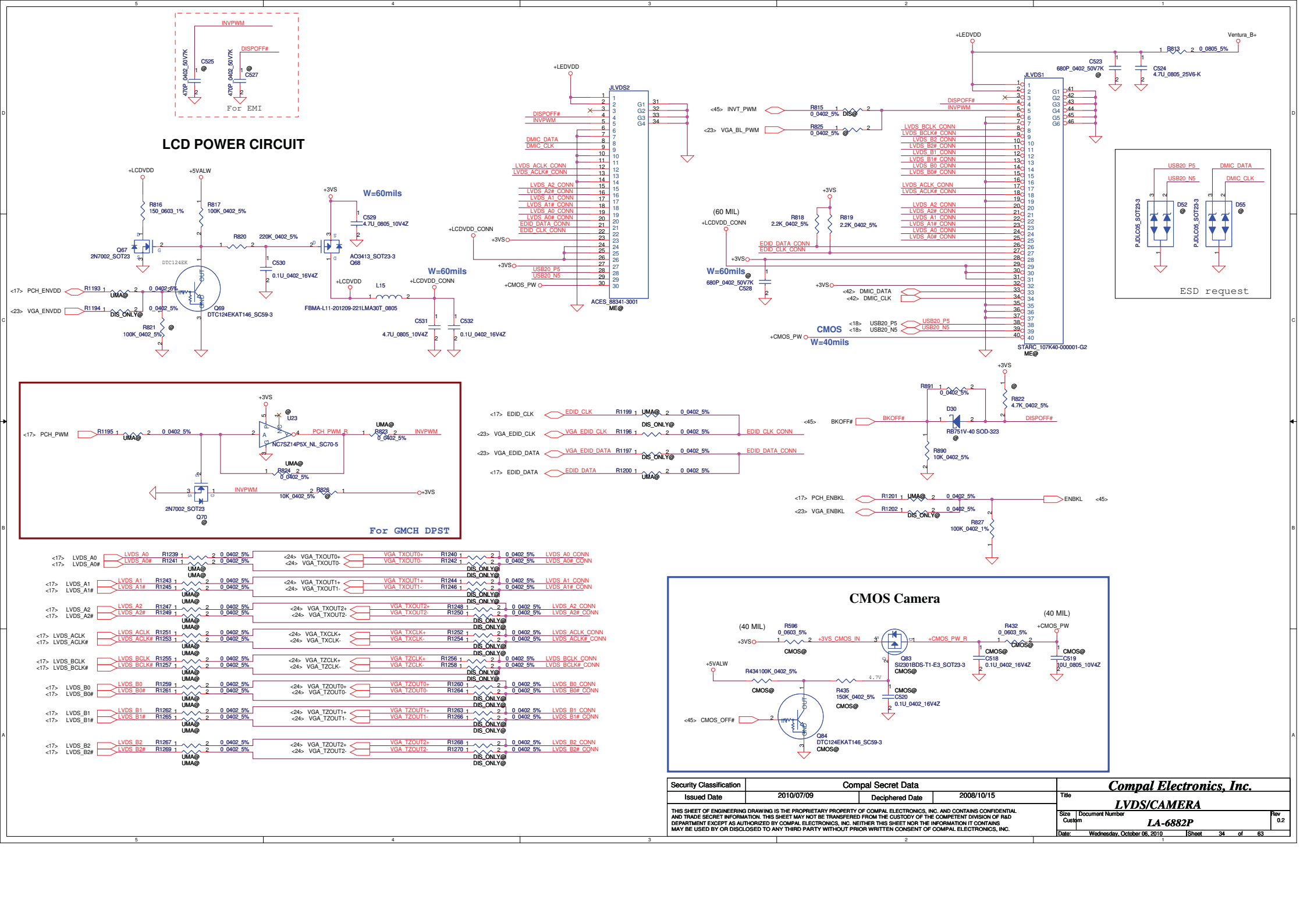
Security Classification	Compal Secret Data		
Issued Date	2010/07/09	Deciphered Date	2011/05/11

Compal Electronics, Inc.

Title: **VENTURA Interface**

Size	Document Number	Rev
	LA-6882P	0.2

Date: Wednesday, October 06, 2010 | Sheet 33 of 63



Security Classification	Compal Secret Data		
Issued Date	2010/07/09	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **LVDS/CAMERA**

Size	Document Number	Rev
Custom	LA-6882P	0.2

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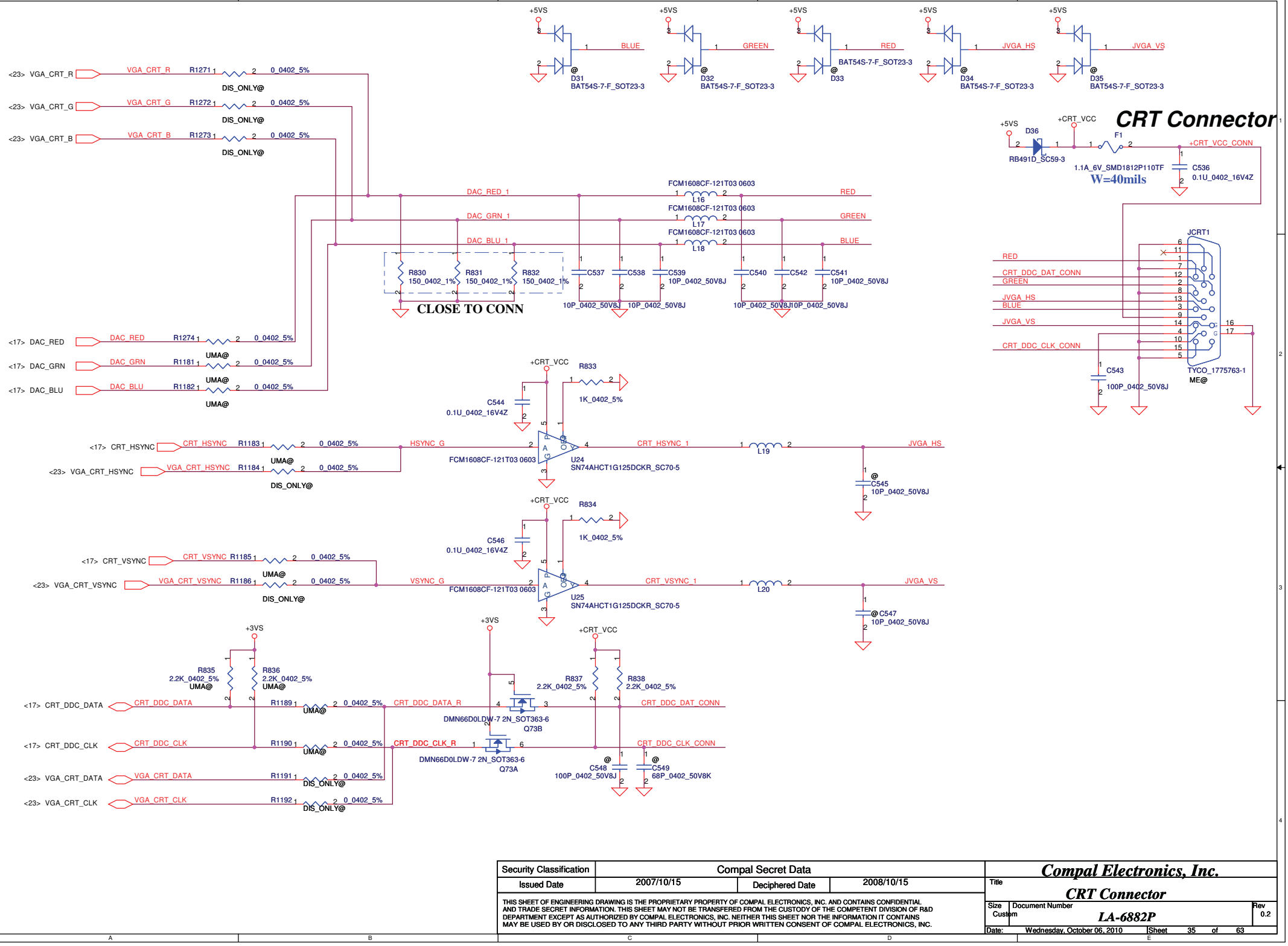
CRT Connector



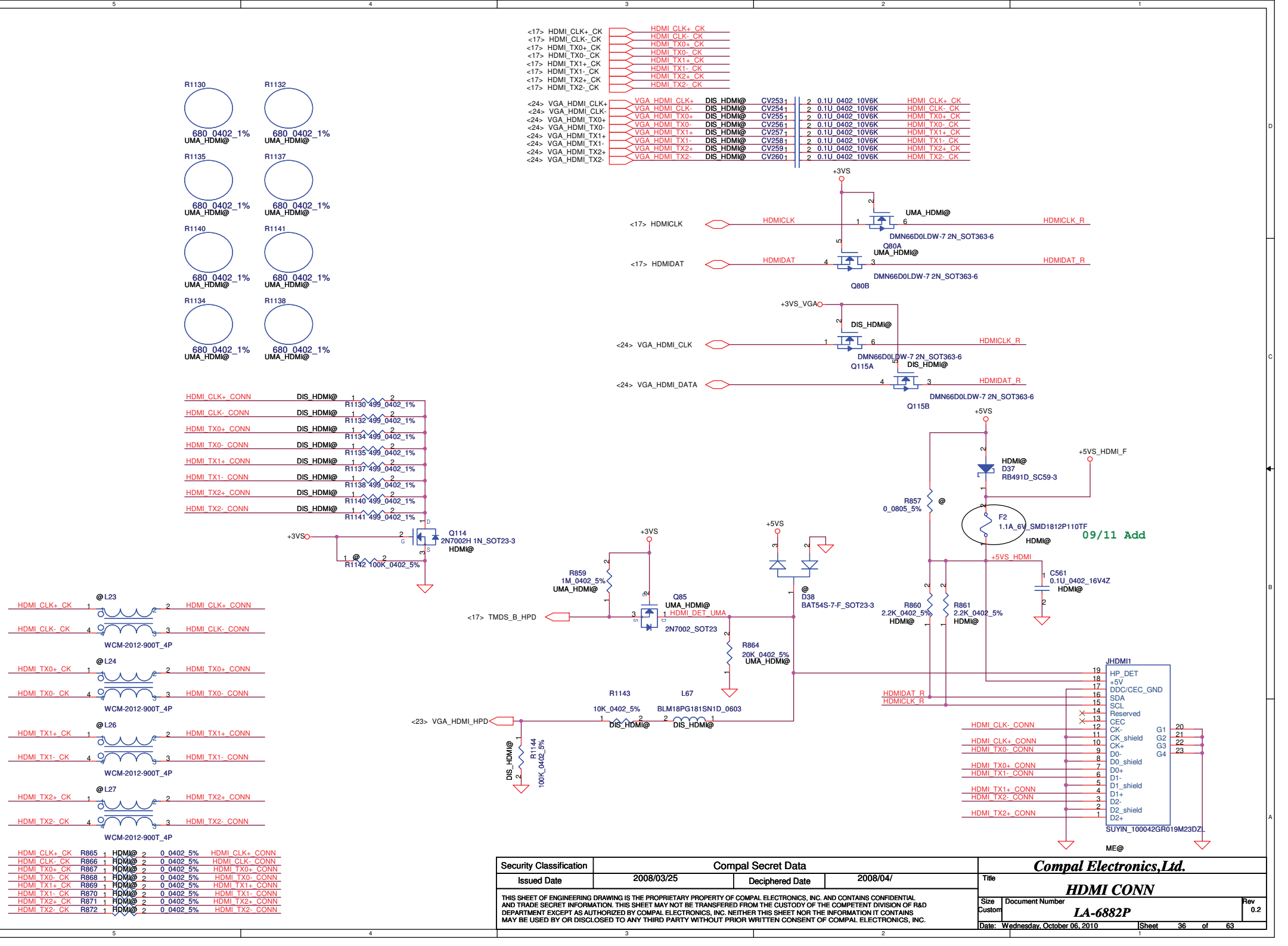
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: CRT Connector

Size: Custom | Document Number: LA-6882P | Rev: 0.2

Date: Wednesday, October 06, 2010 | Sheet 35 of 63


R1130 680_0402_1% UMA_HDMI@
R1132 680_0402_1% UMA_HDMI@
R1135 680_0402_1% UMA_HDMI@
R1137 680_0402_1% UMA_HDMI@
R1140 680_0402_1% UMA_HDMI@
R1141 680_0402_1% UMA_HDMI@
R1134 680_0402_1% UMA_HDMI@
R1138 680_0402_1% UMA_HDMI@
<17> HDMI_CLK+_CK
<17> HDMI_CLK-_CK
<17> HDMI_TX0+_CK
<17> HDMI_TX0-_CK
<17> HDMI_TX1+_CK
<17> HDMI_TX1-_CK
<17> HDMI_TX2+_CK
<17> HDMI_TX2-_CK
HDMI_CLK+_CK
HDMI_CLK-_CK
HDMI_TX0+_CK
HDMI_TX0-_CK
HDMI_TX1+_CK
HDMI_TX1-_CK
HDMI_TX2+_CK
HDMI_TX2-_CK
<24> VGA_HDMI_CLK+
<24> VGA_HDMI_CLK-
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<24> VGA_HDMI_TX0-
<24> VGA_HDMI_TX1+
<24> VGA_HDMI_TX1-
<24> VGA_HDMI_TX2+
<24> VGA_HDMI_TX2-
VGA_HDMI_CLK+ DIS_HDMI@ CV253 0.1U_0402_10V6K HDMI_CLK+_CK
VGA_HDMI_CLK- DIS_HDMI@ CV254 0.1U_0402_10V6K HDMI_CLK-_CK
VGA_HDMI_TX0+ DIS_HDMI@ CV255 0.1U_0402_10V6K HDMI_TX0+_CK
VGA_HDMI_TX0- DIS_HDMI@ CV256 0.1U_0402_10V6K HDMI_TX0-_CK
VGA_HDMI_TX1+ DIS_HDMI@ CV257 0.1U_0402_10V6K HDMI_TX1+_CK
VGA_HDMI_TX1- DIS_HDMI@ CV258 0.1U_0402_10V6K HDMI_TX1-_CK
VGA_HDMI_TX2+ DIS_HDMI@ CV259 0.1U_0402_10V6K HDMI_TX2+_CK
VGA_HDMI_TX2- DIS_HDMI@ CV260 0.1U_0402_10V6K HDMI_TX2-_CK
+3VS
<17> HDMICLK
HDMICLK
UMA_HDMI@
DMN66D0LDW-7 2N_SOT363-6
HDMICLK_R
Q80A
<17> HDMIDAT
HDMIDAT
HDMIDAT_R
DMN66D0LDW-7 2N_SOT363-6
Q80B
+3VS_VGA
DIS_HDMI@
<24> VGA_HDMI_CLK
HDMICLK_R
DMN66D0LDW-7 2N_SOT363-6
Q115A
DIS_HDMI@
<24> VGA_HDMI_DATA
HDMIDAT_R
DMN66D0LDW-7 2N_SOT363-6
Q115B
+5VS
HDMI_CLK+_CONN DIS_HDMI@ R1130 499_0402_1%
HDMI_CLK-_CONN DIS_HDMI@ R1132 499_0402_1%
HDMI_TX0+_CONN DIS_HDMI@ R1134 499_0402_1%
HDMI_TX0-_CONN DIS_HDMI@ R1135 499_0402_1%
HDMI_TX1+_CONN DIS_HDMI@ R1137 499_0402_1%
HDMI_TX1-_CONN DIS_HDMI@ R1138 499_0402_1%
HDMI_TX2+_CONN DIS_HDMI@ R1140 499_0402_1%
HDMI_TX2-_CONN DIS_HDMI@ R1141 499_0402_1%
+3VS
Q114 2N7002H 1N_SOT23-3 HDMI@
@ R1142 100K_0402_5%
HDMI@ D37 RB491D_SC59-3
+5VS_HDMI_F
R857 @ 0_0805_5%
F2 1.1A_6V_SMD1812P110TF HDMI@
09/11 Add
+5VS_HDMI
C561 0.1U_0402_16V4Z HDMI@
R859 1M_0402_5% UMA_HDMI@
Q85 UMA_HDMI@ 2N7002_SOT23
HDMI_DET_UMA
<17> TMDS_B_HPD
@ D38 BAT54S-7-F_SOT23-3
R860 2.2K_0402_5% HDMI@
R861 2.2K_0402_5% HDMI@
R864 20K_0402_5% UMA_HDMI@
@L23
HDMI_CLK+_CK HDMI_CLK+_CONN
HDMI_CLK-_CK HDMI_CLK-_CONN
WCM-2012-900T_4P
@L24
HDMI_TX0+_CK HDMI_TX0+_CONN
HDMI_TX0-_CK HDMI_TX0-_CONN
WCM-2012-900T_4P
@L26
HDMI_TX1+_CK HDMI_TX1+_CONN
HDMI_TX1-_CK HDMI_TX1-_CONN
WCM-2012-900T_4P
@L27
HDMI_TX2+_CK HDMI_TX2+_CONN
HDMI_TX2-_CK HDMI_TX2-_CONN
WCM-2012-900T_4P
R1143 10K_0402_5% DIS_HDMI@
L67 BLM18PG181SN1D_0603 DIS_HDMI@
<23> VGA_HDMI_HPD
DIS_HDMI@ R1144 100K_0402_5%
JHDMI1
HP_DET
+5V
DDC/CEC_GND
SDA
SCL
Reserved
CEC
CK-
CK_shield
CK+
D0-
D0_shield
D0+
D1-
D1_shield
D1+
D2-
D2_shield
D2+
G1 G2 G3 G4
SUYIN_100042GR019M23DZL
ME@
HDMIDAT_R
HDMICLK_R
HDMI_CLK-_CONN
HDMI_CLK+_CONN
HDMI_TX0-_CONN
HDMI_TX0+_CONN
HDMI_TX1-_CONN
HDMI_TX1+_CONN
HDMI_TX2-_CONN
HDMI_TX2+_CONN
HDMI_CLK+_CK R865 HDMI@ 0_0402_5% HDMI_CLK+_CONN
HDMI_CLK-_CK R866 HDMI@ 0_0402_5% HDMI_CLK-_CONN
HDMI_TX0+_CK R867 HDMI@ 0_0402_5% HDMI_TX0+_CONN
HDMI_TX0-_CK R868 HDMI@ 0_0402_5% HDMI_TX0-_CONN
HDMI_TX1+_CK R869 HDMI@ 0_0402_5% HDMI_TX1+_CONN
HDMI_TX1-_CK R870 HDMI@ 0_0402_5% HDMI_TX1-_CONN
HDMI_TX2+_CK R871 HDMI@ 0_0402_5% HDMI_TX2+_CONN
HDMI_TX2-_CK R872 HDMI@ 0_0402_5% HDMI_TX2-_CONN
Security Classification
Compal Secret Data
Issued Date
2008/03/25
Deciphered Date
2008/04/
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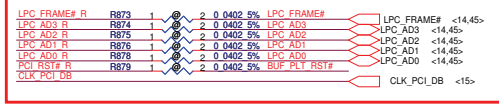
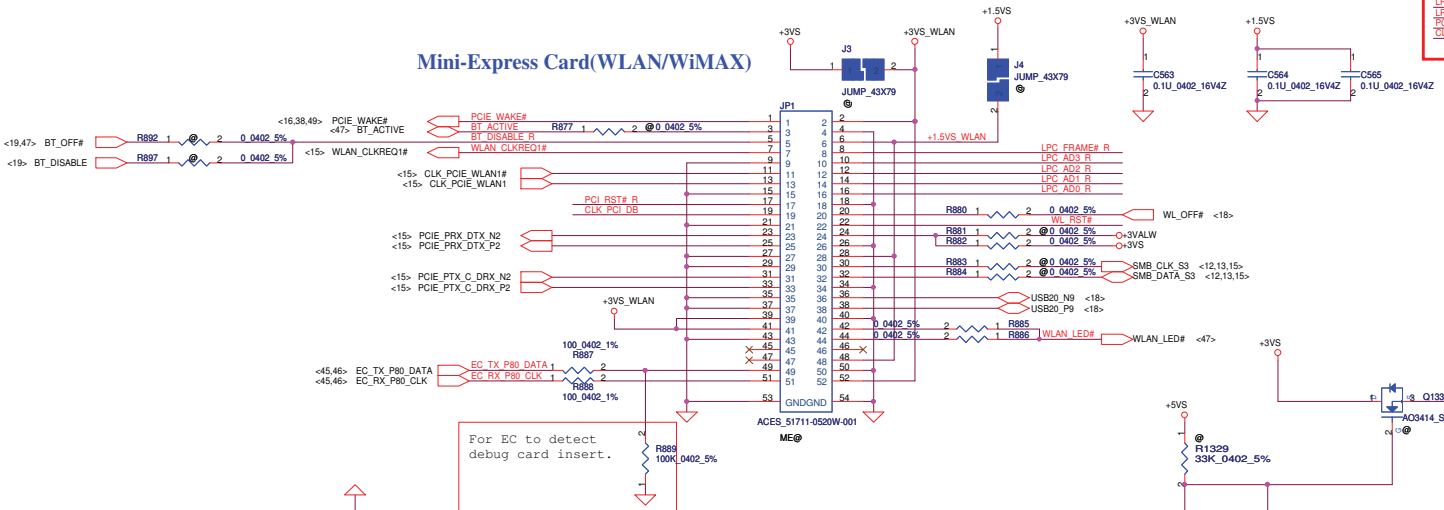
Compal Electronics,Ltd.
Title
HDMI CONN
Size
Custom
Document Number
LA-6882P
Rev
0.2
Date: Wednesday, October 06, 2010
Sheet 36 of 63

Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for SSD(Full)

Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

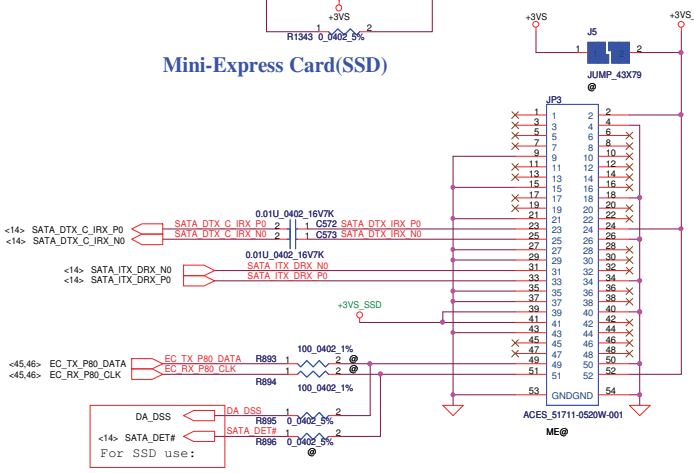


Mini-Express Card(WLAN/WiMAX)

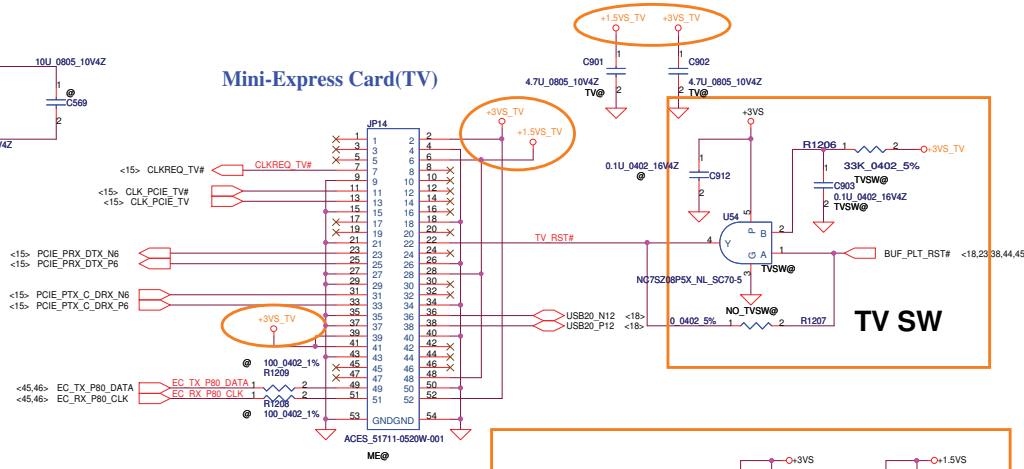


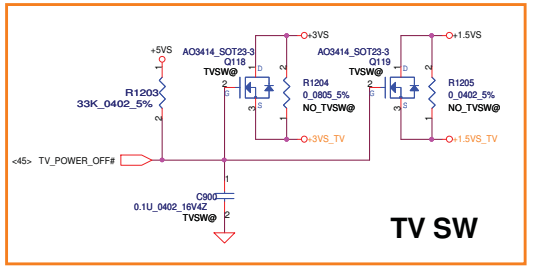
SSD Active:4.5W(1.5A)

Mini-Express Card(SSD)



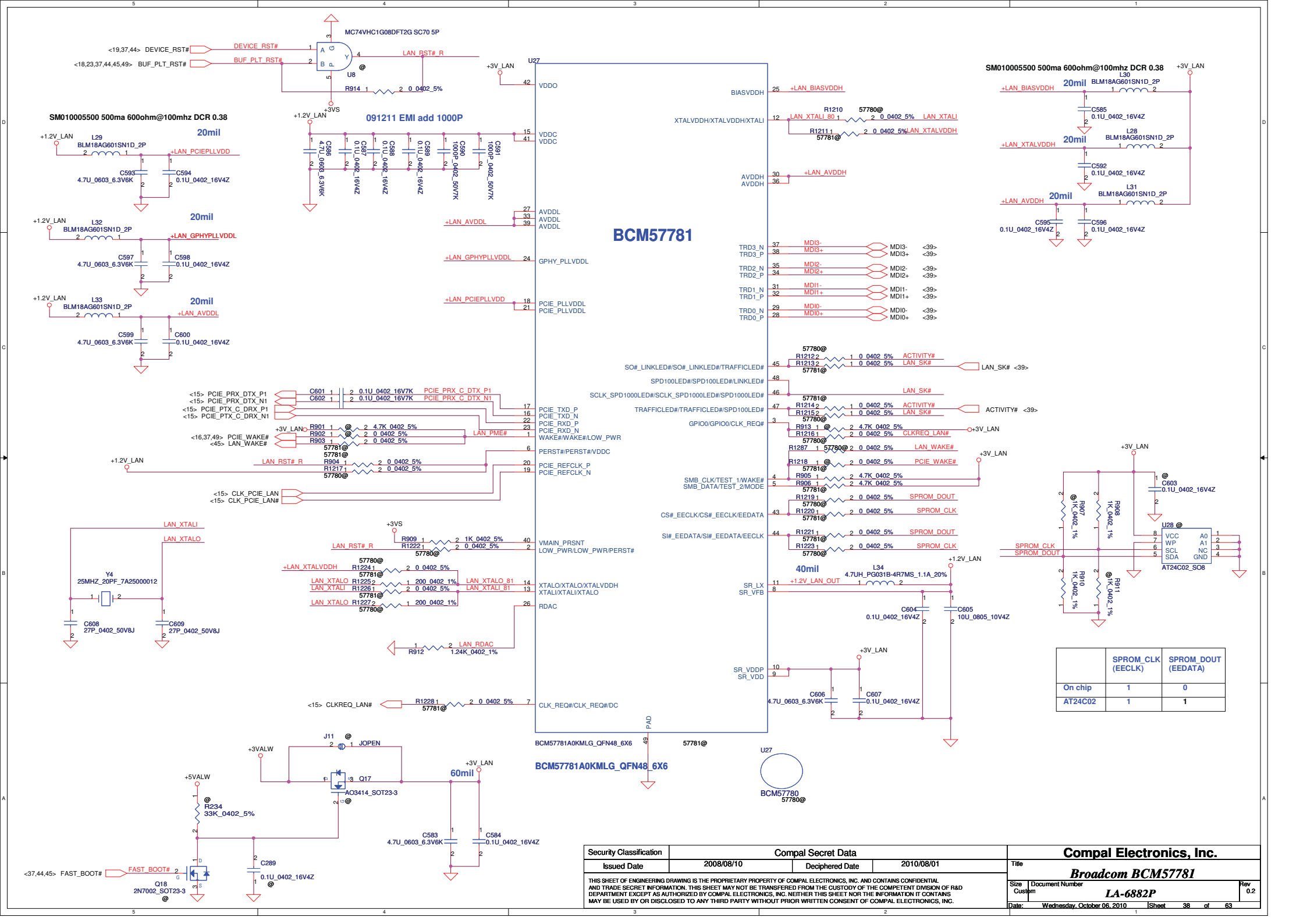
Mini-Express Card(TV)





Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: Mini-Card			
Size	Document Number: LA-6882P		Rev: 0.2
Date: Wednesday, October 06, 2010	Sheet 37 of 63		



	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

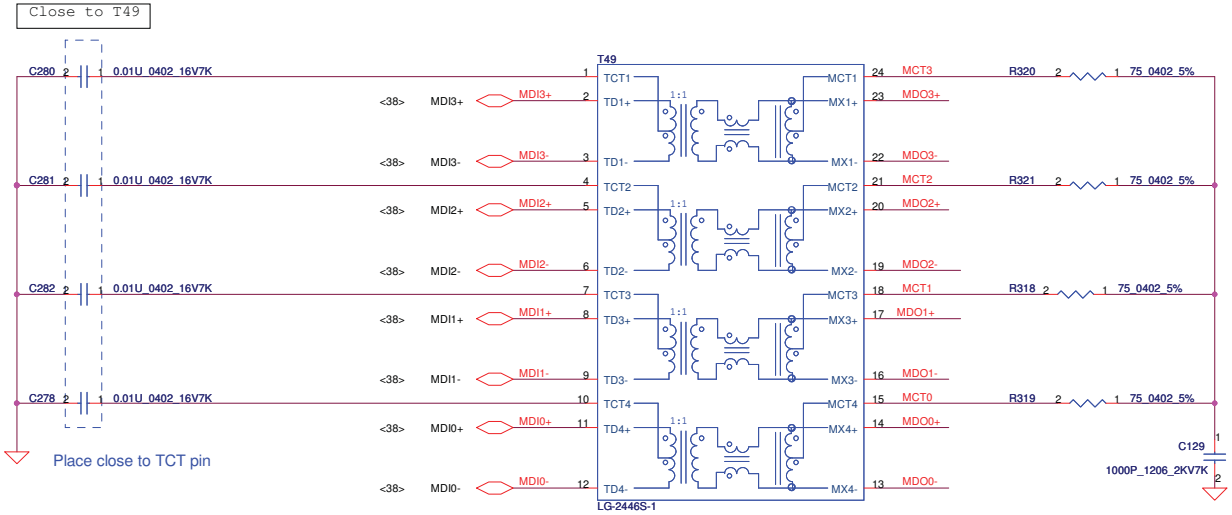
Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

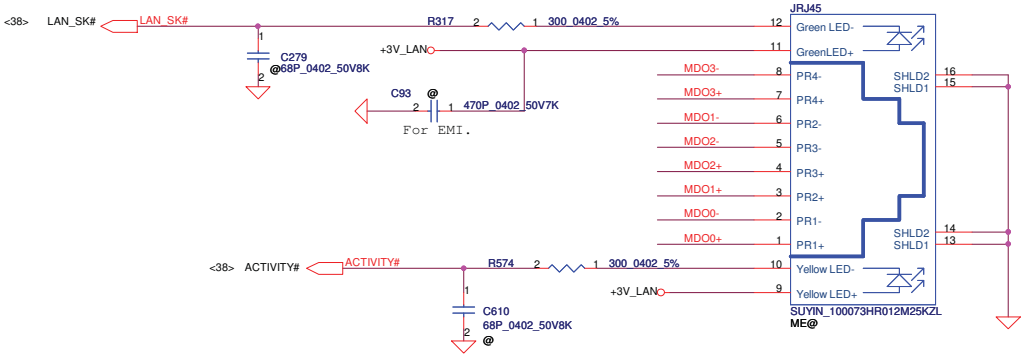
Title: *Broadcom BCM57781*

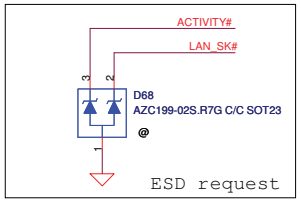
Size: Custom | Document Number: *LA-6882P* | Rev: 0.2

Date: Wednesday, October 06, 2010 | Sheet 38 of 63



RJ45 Conn.





Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: **LAN Magnetic & RJ45**

Size	Document Number	Rev
Custom	LA-6882P	0.2

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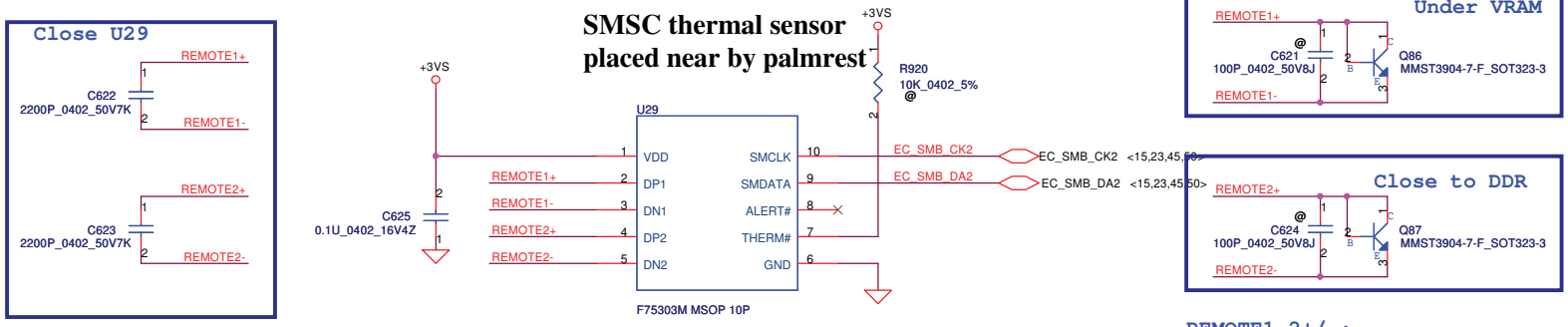
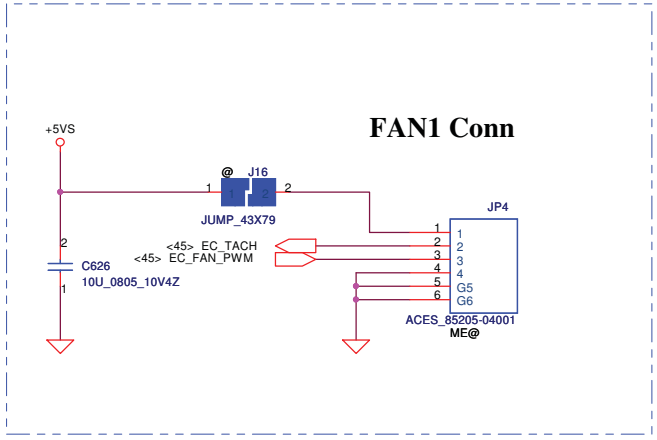


Address 1001_101xb

REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: **EMC1403_Thermal sensor/FAN**

Size	Document Number	Rev
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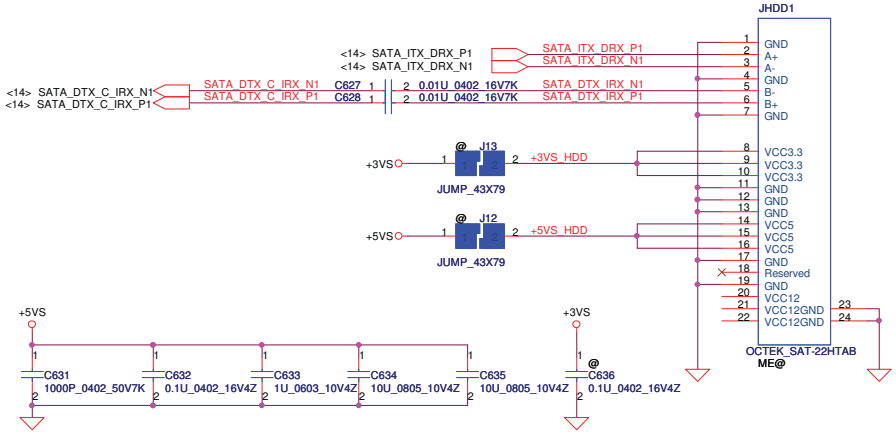
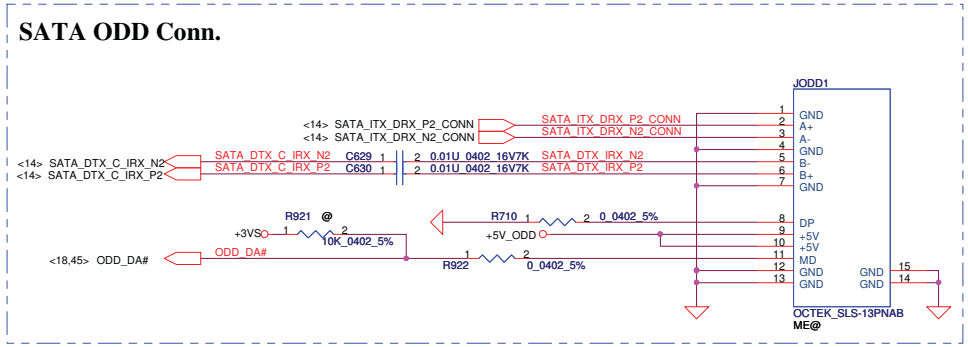
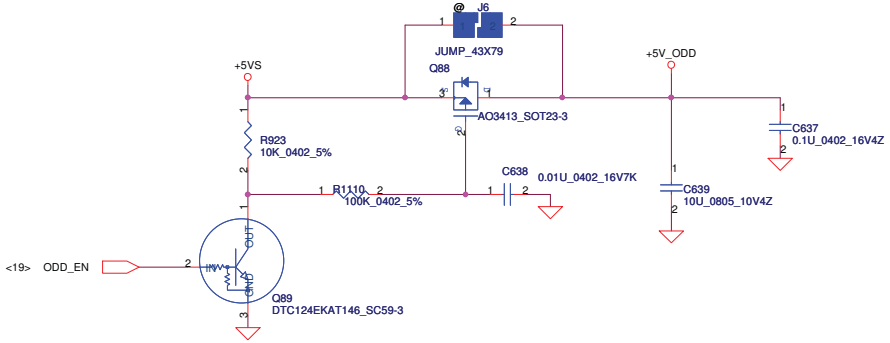
SATA HDD Conn.



SATA ODD Conn.



ODD Power Control



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: HDD/ODD Connector			
Size: B	Document Number: LA-6882P		Rev: 0.2
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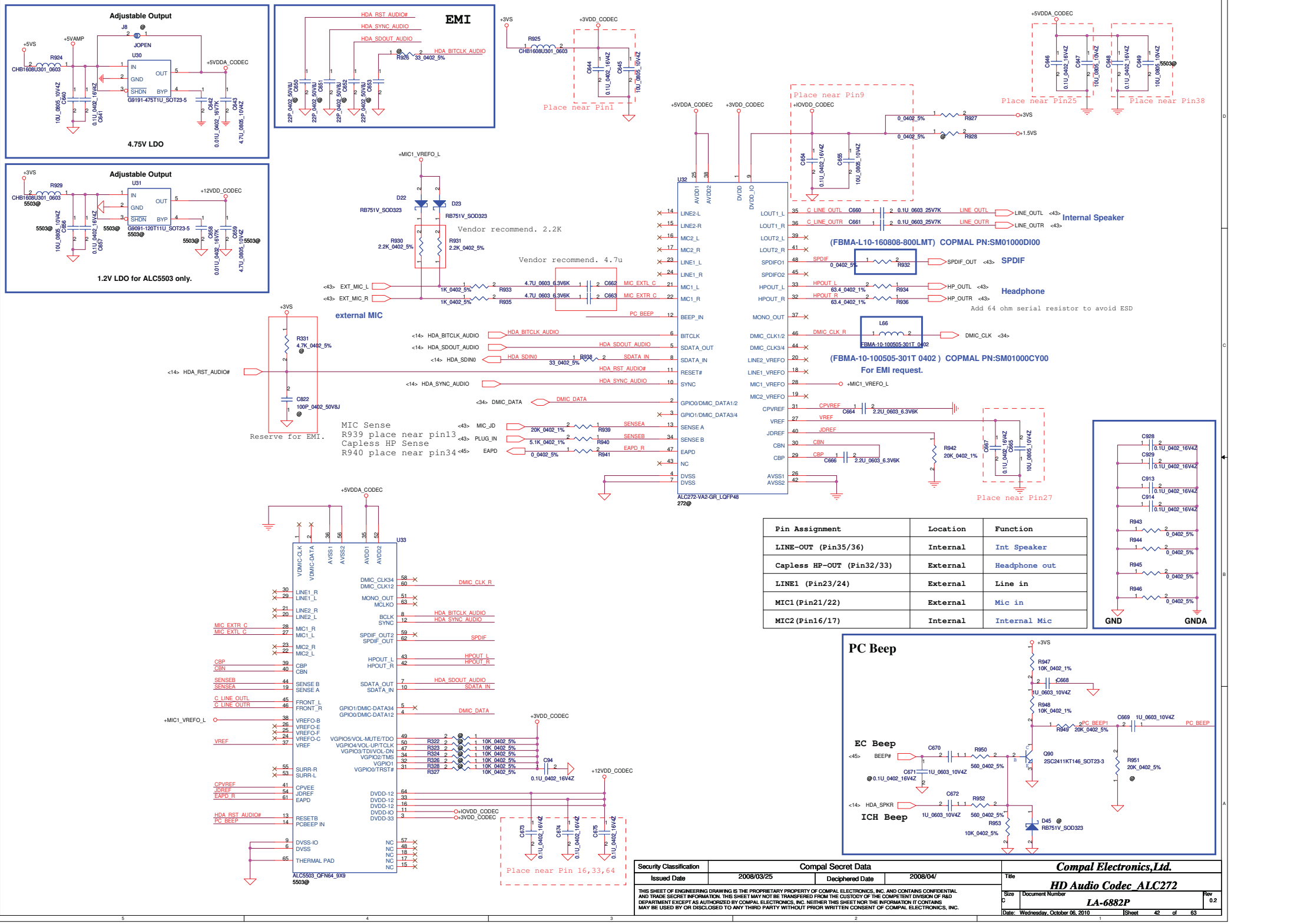

Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	Line in
MIC1(Pin21/22)	External	Mic in
MIC2(Pin16/17)	Internal	Internal Mic

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

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Compal Electronics,Ltd.

Title: HD Audio Codec ALC272

Size: C | Document Number: LA-6882P | Rev: 0.2

Date: Wednesday, October 06, 2010 | Sheet 42 of 63

wide 25MIL

SPK_R1- 1 R1280 2 0_0805_5% SPK_R1-_CONN
SPK_R2+ 1 R1281 2 0_0805_5% SPK_R2+_CONN
SPK_L1- 1 R1282 2 0_0805_5% SPK_L1-_CONN
SPK_L2+ 1 R1283 2 0_0805_5% SPK_L2+_CONN

C678 @ 1000P_0402_50V7K
C679 @ 1000P_0402_50V7K
C680 @ 1000P_0402_50V7K
C681 @ 1000P_0402_50V7K

JSPK1
1 2 3 4 GND GND
ACES_87212-04G0
ME@

SPK_R1-_CONN
SPK_R2+_CONN
SPK_L1-_CONN
SPK_L2+_CONN
HP_OUTR
HP_OUTL

D59 @ PACDN042Y3R_SOT23-3
D60 @ PACDN042Y3R_SOT23-3
D61 @ PACDN042Y3R_SOT23-3

Reserve for ESD request.

EXT_MIC_L-2
EXT_MIC_R-2
D69 @ ZEN ROW PJDLC05C 3P C/A SOT23
ESD request

Audio Jack
MIC IN

<42> EXT_MIC_L
EXT_MIC_L
L37 FBMA-L10-160808-121LMT_2P
EXT_MIC_L-2
C676 47P_0402_50V8J
@C677 10P_0402_50V8J
GNDA

<42> EXT_MIC_R
EXT_MIC_R
L40 FBMA-L10-160808-121LMT_2P
EXT_MIC_R-2
C682 47P_0402_50V8J
@C683 10P_0402_50V8J
GNDA

<42> MIC_JD
MIC_JD
10P_0402_50V8J C684 @
GNDA

JMIC1
GND GND GND GND
SUYIN_010168FR006G576ZL
ME@

220P_0402_50V7K C685
220P_0402_50V7K C686

Headphone

@R954 1K_0402_5%
@R955 1K_0402_5%
GNDA

<42> HP_OUTR
HP_OUTR
L41 FBMA-L10-160808-121LMT_2P
PR-OUT

<42> HP_OUTL
HP_OUTL
L42 FBMA-L10-160808-121LMT_2P
PL-OUT

JHP1

<42> PLUG_IN
PLUG_IN

+5VS
DRIVE IC

<42> SPDIF_OUT
SPDIF_OUT
C688 220P_0402_50V7K
C687 0.1U_0402_16V4Z

GND GND
SINGA_2SJ-A373-H03
ME@

GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

+5VAMP
W=40mil
+3VALW

U34
VDD PVDD PVDD
GAIN0
GAIN1
LIN-
RIN-
LIN+
RIN+
BYPASS
NC
SHUTDOWN
LOUT-
ROUT-
LOUT+
ROUT+
GND GND GND GND GND
TPA6017A2PWPR_TSSOP20

R956 10K_0402_5% @
AMP_OFF#
R957 0_0402_5%
EC_MUTE#
EC_MUTE# <45>

SPK_L1-
SPK_R1-
SPK_L2+
SPK_R2+
20mil

<42> LINE_OUTL
LINE_OUTL C926 0.033U_0402_16V7K LIN
<42> LINE_OUTR
LINE_OUTR C927 0.033U_0402_16V7K RIN

R960 @ 10K_0402_5%
R961 @ 10K_0402_5%
C691 0.1U_0603_25V7K
C692 0.1U_0603_25V7K
C695 4.7U_0805_10V4Z

+5VAMP
R962 @ 100K_0402_1%
GAIN0
R965 100K_0402_1%
+5VAMP
R963 100K_0402_1%
GAIN1
R966 100K_0402_1% @

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: AMP,Audio speaker CONN

Size: Custom | Document Number: LA-6882P | Rev: 0.2

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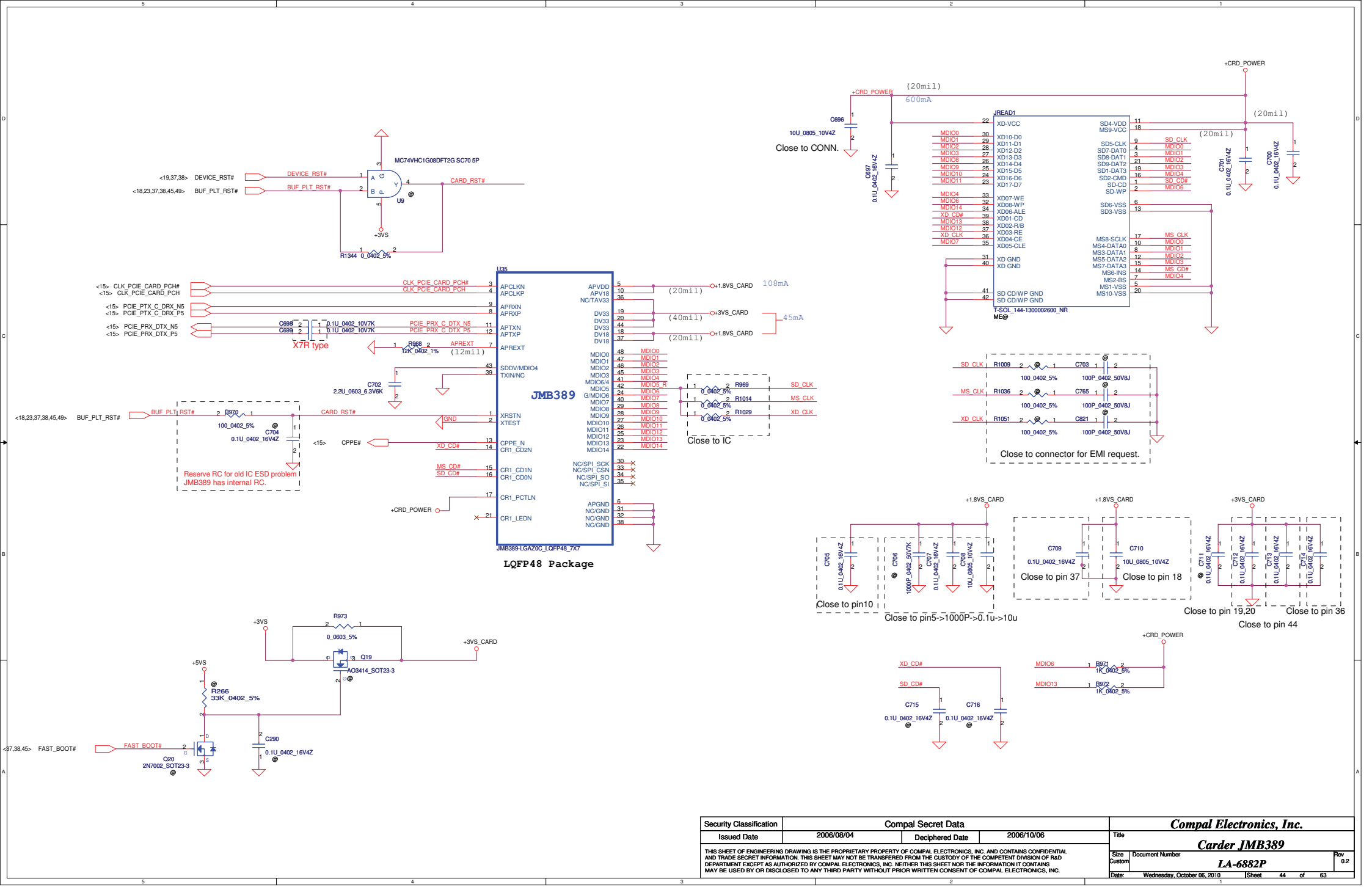


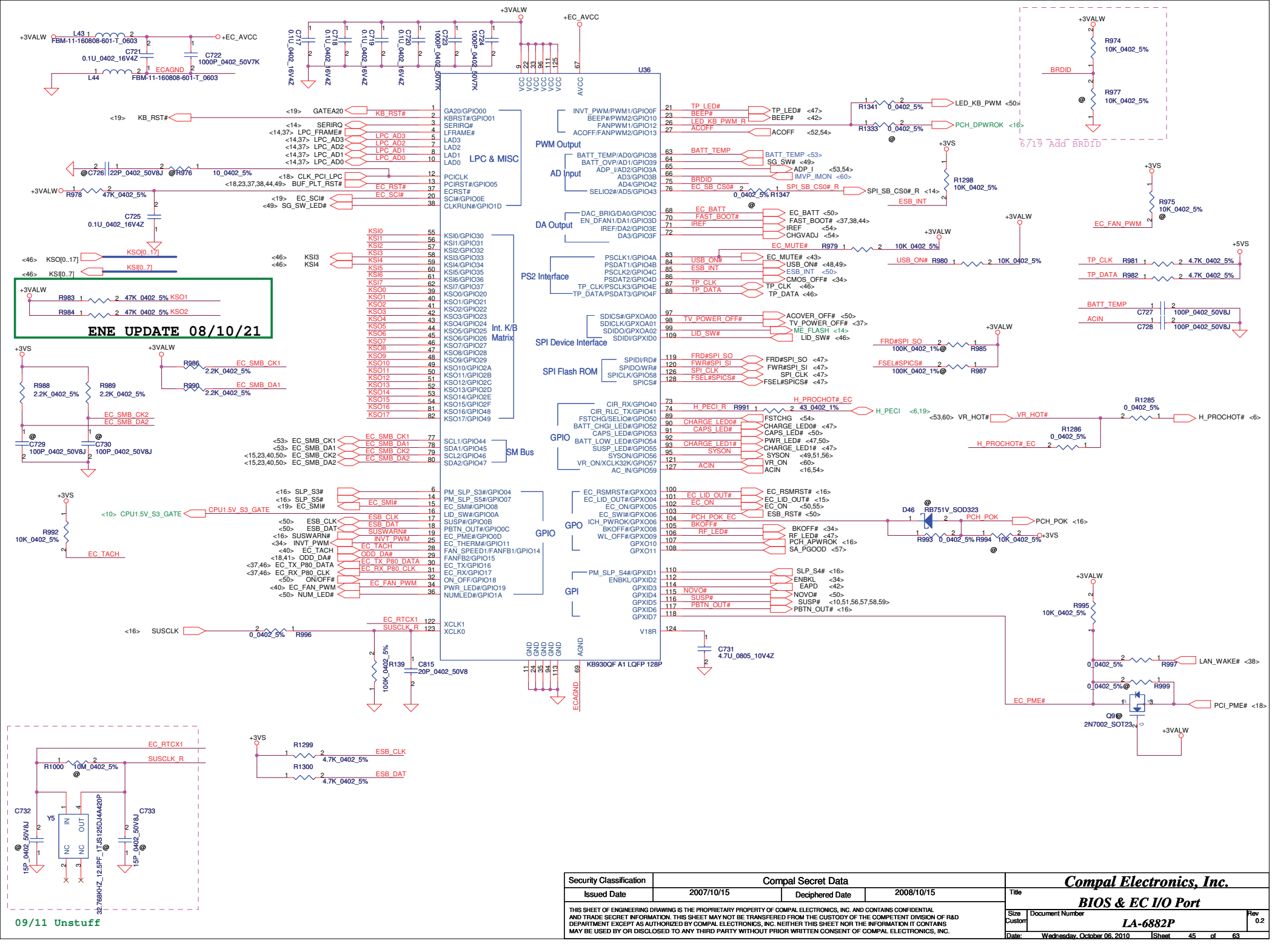
Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2006/10/06

Compal Electronics, Inc.

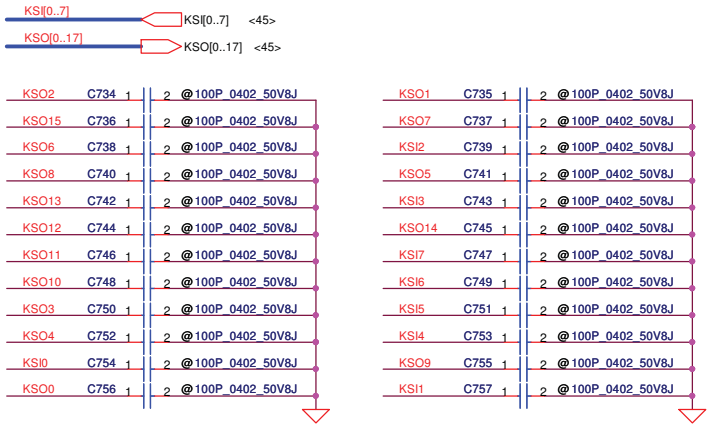
Title: **Carder JMB389**

Size	Document Number	Rev
Custom	LA-6882P	0.2

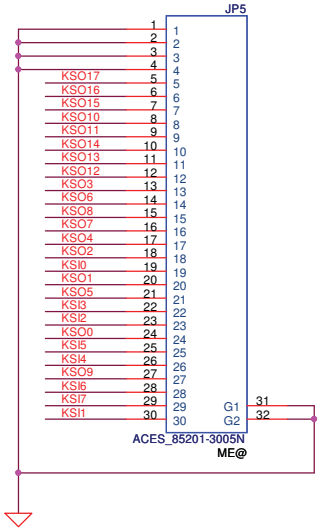
Date: Wednesday, October 06, 2010 | Sheet 44 of 63


U36
KB930QF A1 LQFP 128P
ENE UPDATE 08/10/21
09/11 Unstuff
6/19 Add BRDID
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
Compal Secret Data
Compal Electronics, Inc.
BIOS & EC I/O Port
LA-6882P
Issued Date 2007/10/15
Deciphered Date 2008/10/15
Wednesday, October 06, 2010

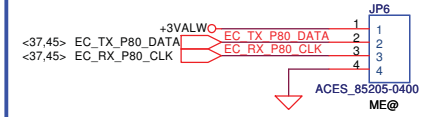
INT_KBD Conn.



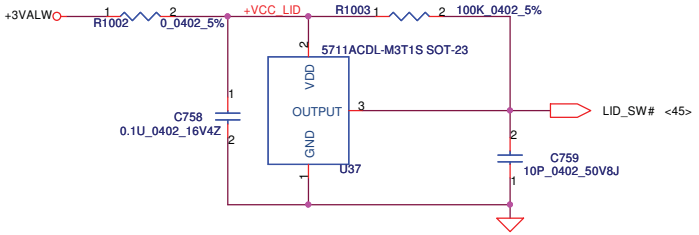
CONN PIN define need double check



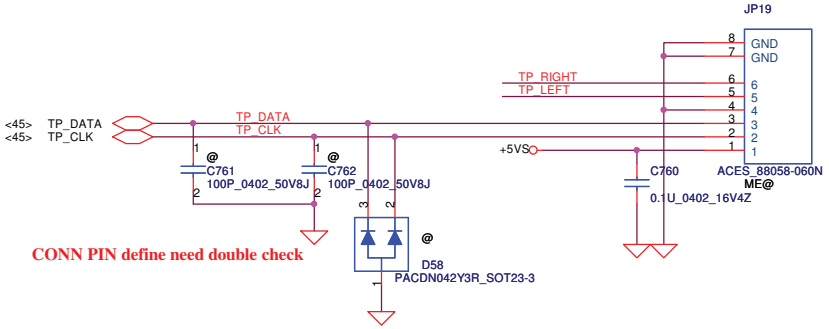
EC DEBUG PORT



Lid Switch

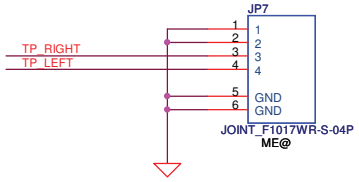


To TP/B Conn.



CONN PIN define need double check

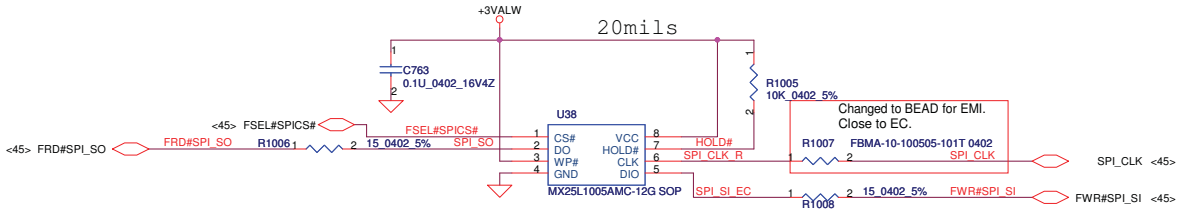
To TP Button/B Conn.

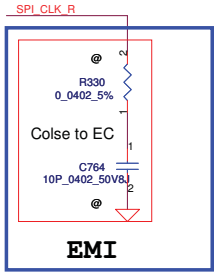


Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

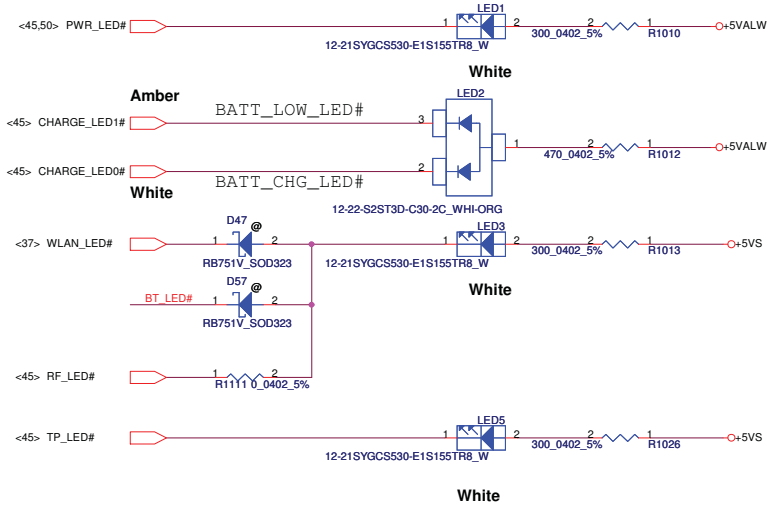
Compal Electronics, Inc.			
Title: KB /SW /LPC Debug Conn.			
Size: B	Document Number: LA-6882P		Rev: 0.2
Date: Wednesday, October 06, 2010	Sheet 46 of 63		

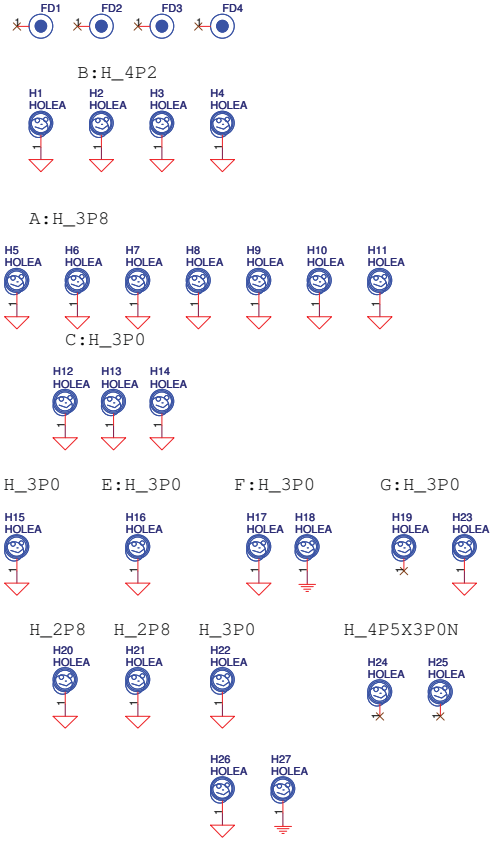
FOR EC 128KB SPI ROM
(150mil PACKAGE)
P/N : SA00002C100



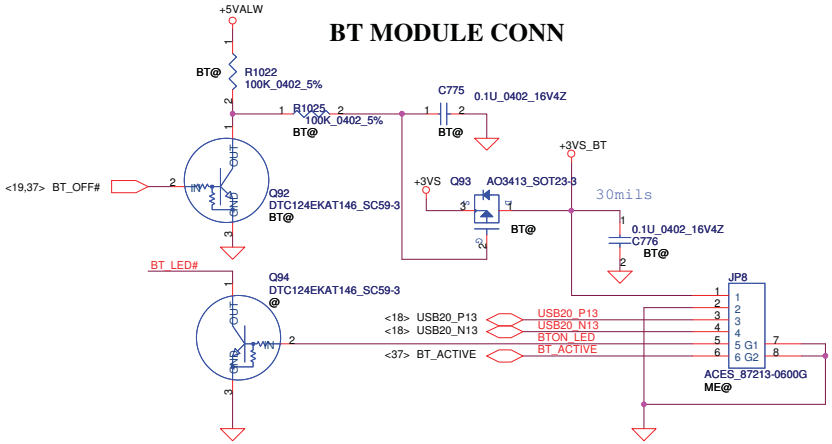


LED





BT MODULE CONN



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **LED/EC SPI ROM/BT**

Size	Document Number	Rev
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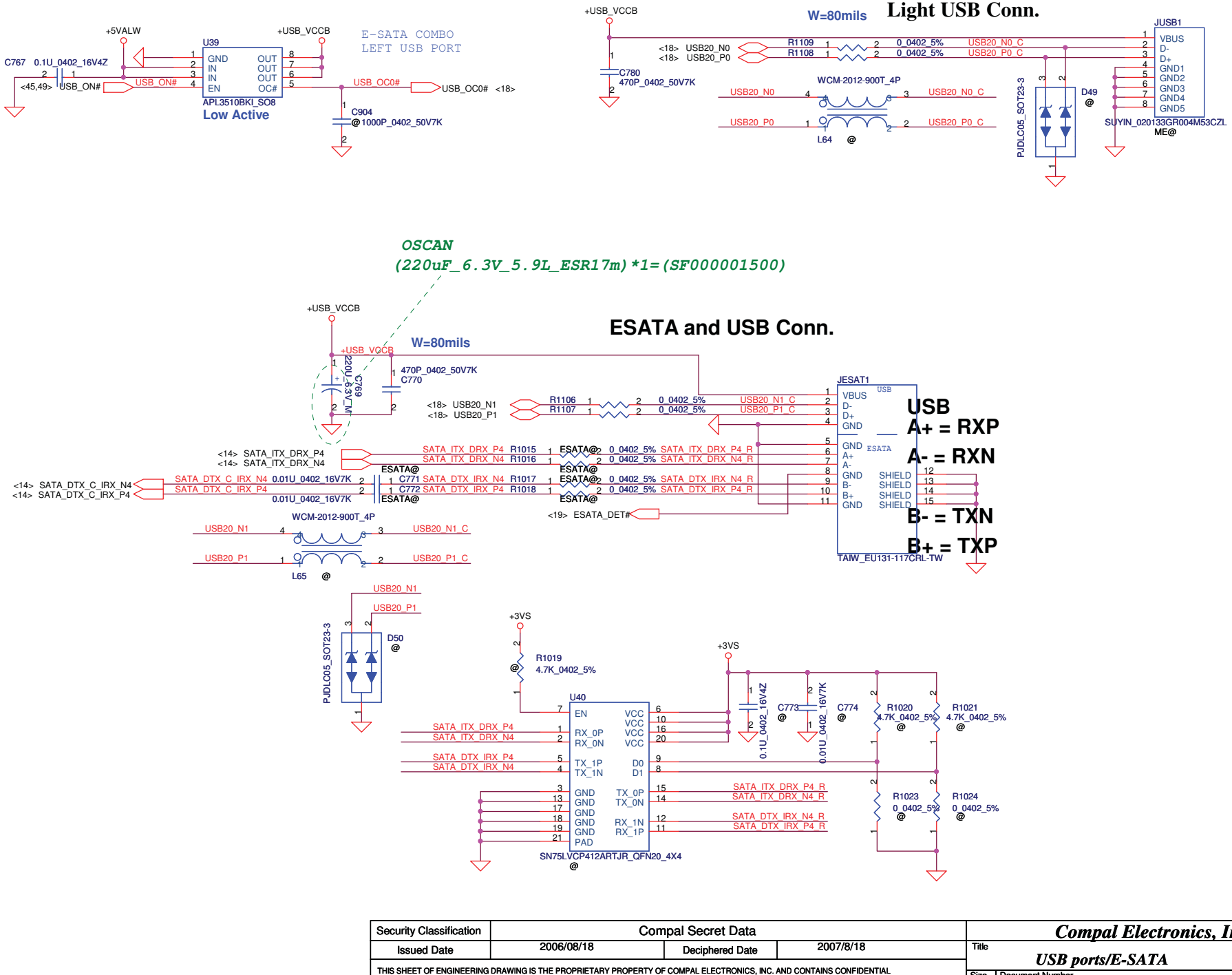


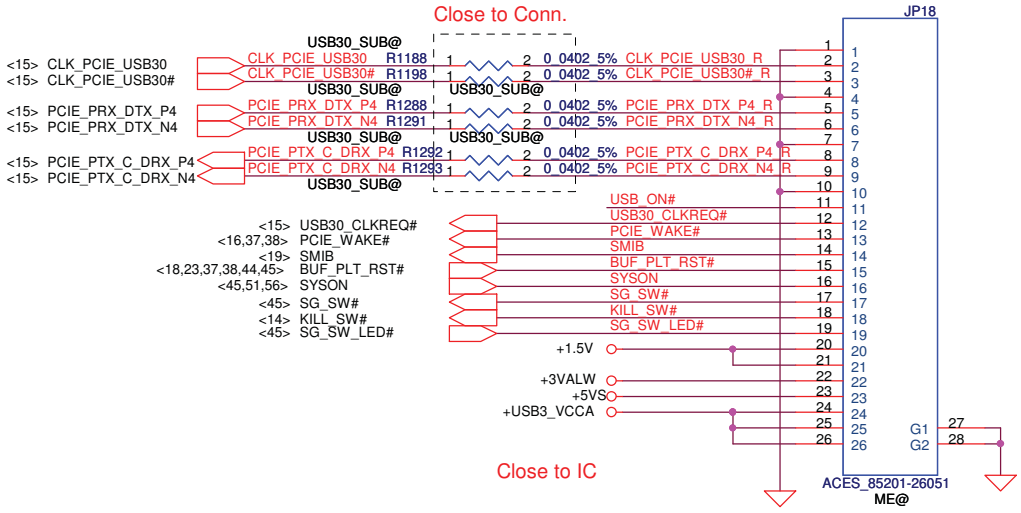
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: *USB ports/E-SATA*

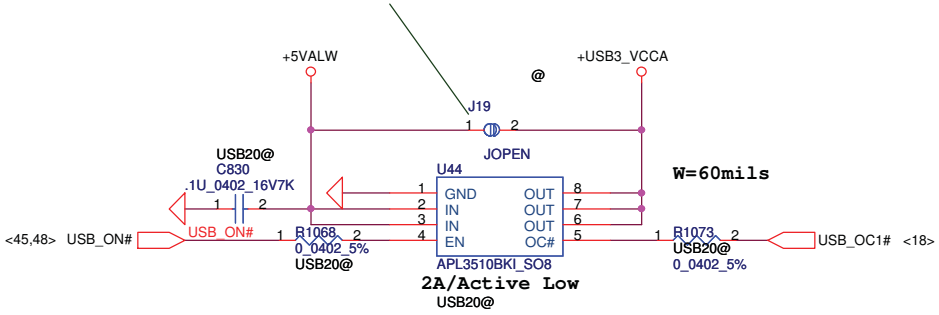
Size: Custom | Document Number: *LA-6882P* | Rev: 0.2

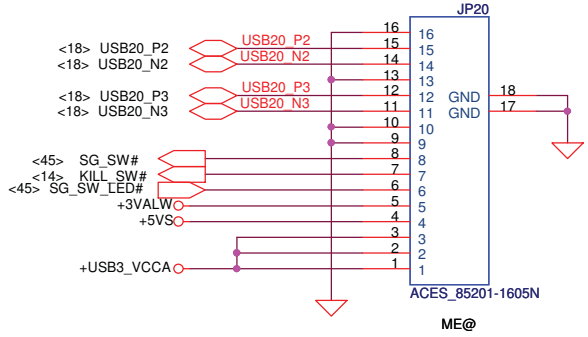
Date: Wednesday, October 06, 2010 | Sheet 48 of 63



09/30 Delete USB3.0 controller

10/04 Short J19 with JP18.





Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2008/1/15

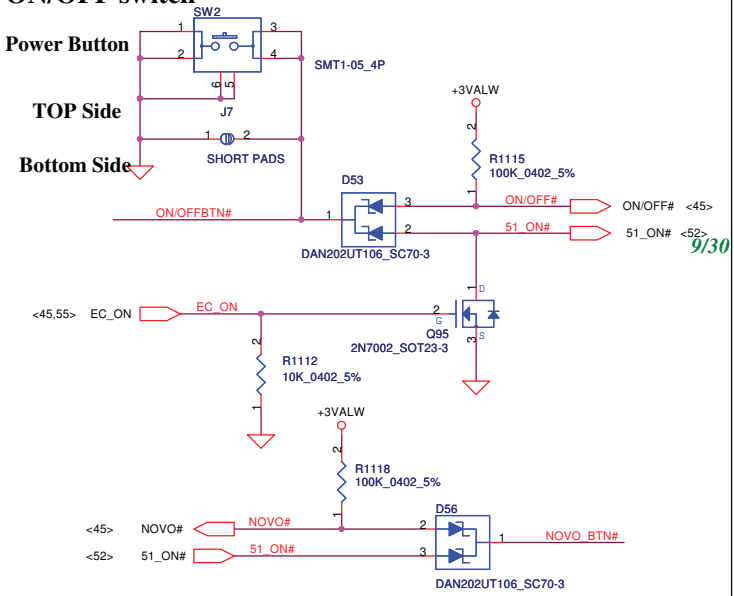
Compal Electronics, Inc.

Title: **USB Right Ports/ USB Brd Conn.**

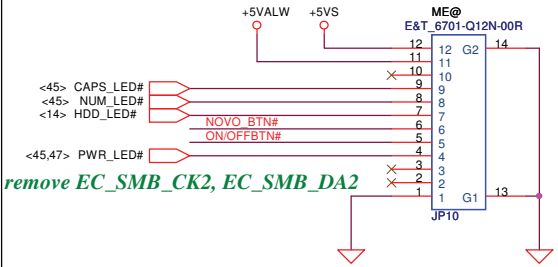
Size	Document Number	Rev
Custom	LA-6882P	0.2

Date: Wednesday, October 06, 2010 | Sheet 49 of 63

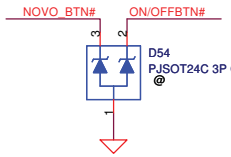
ON/OFF switch



Power Button Board Conn. 10pin



9/30 remove EC_SMB_CK2, EC_SMB_DA2

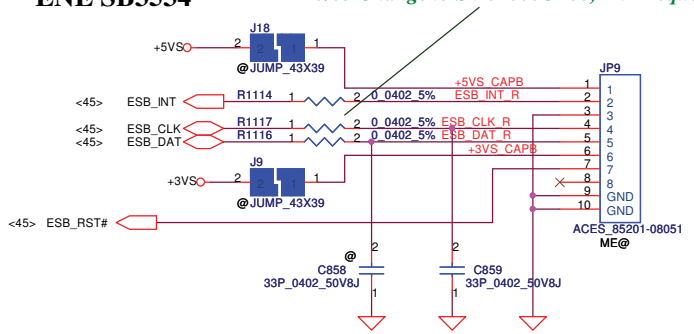


EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

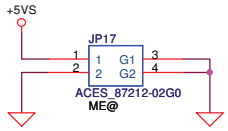
Cap Sensor Board Conn. 8pin

ENE SB3534

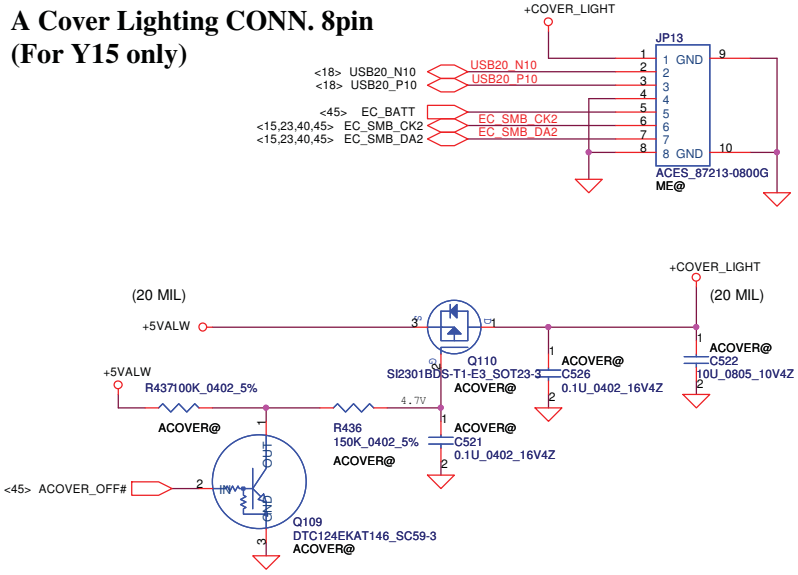
10/05 Change to SM01000CY00, EMI request



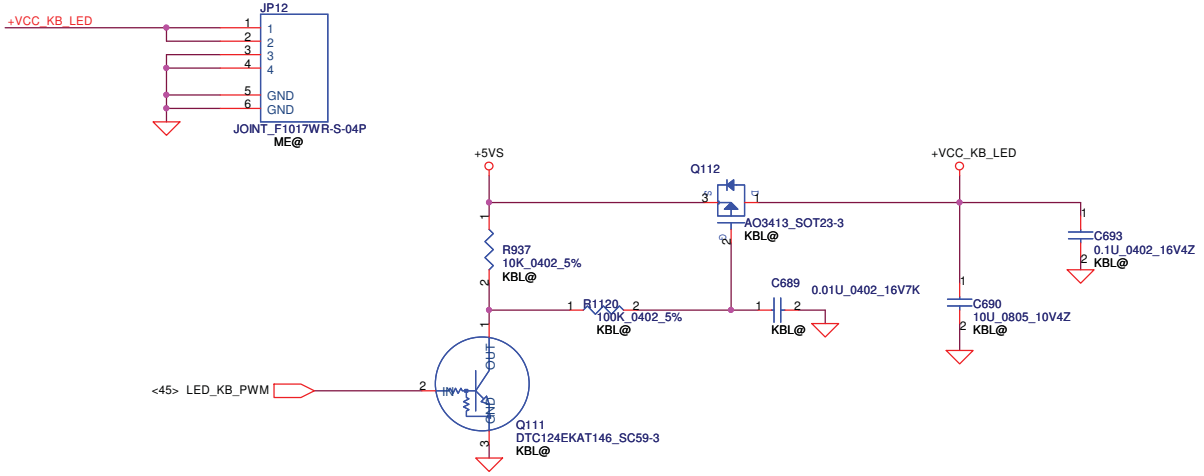
FAN Lighting Conn. 2pin (For Y15 only)



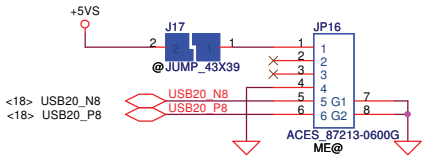
A Cover Lighting CONN. 8pin (For Y15 only)



KB Lighting CONN.4pin



IR CONN. 6pin (For Y15 only)



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: **other IO connector**

Size	Document Number	Rev
Custom	LA-6882P	0.2

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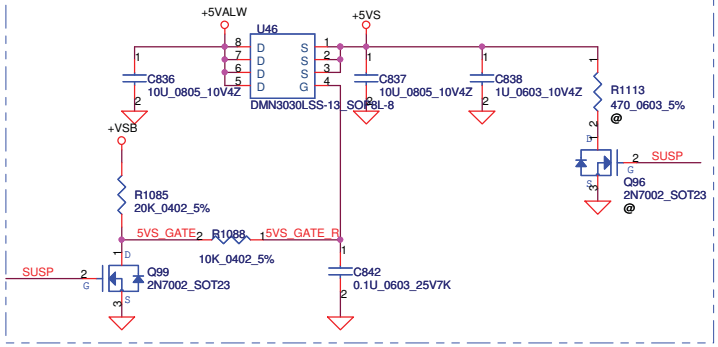
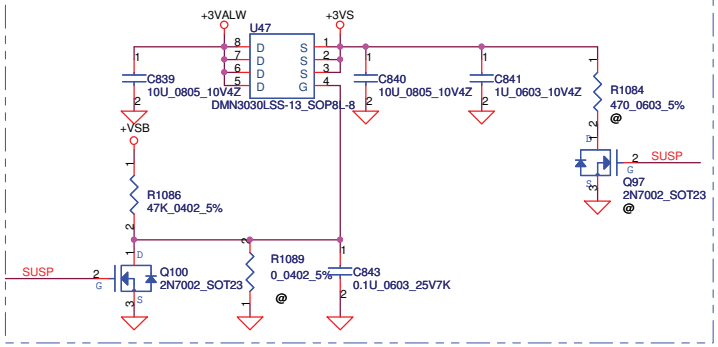
+5VALW TO +5VS

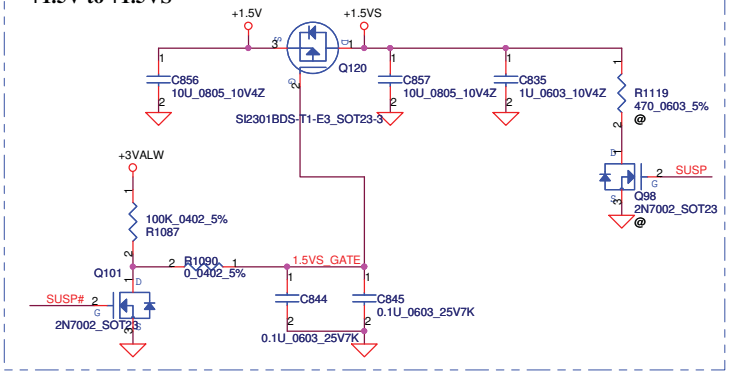


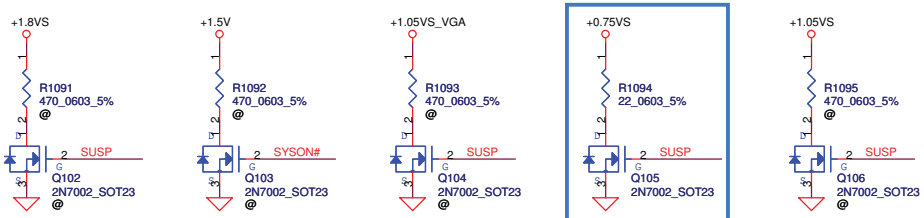
+3VALW TO +3VS



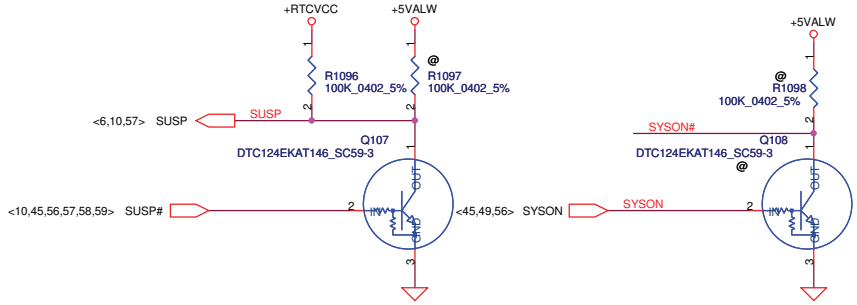
+1.5V to +1.5VS

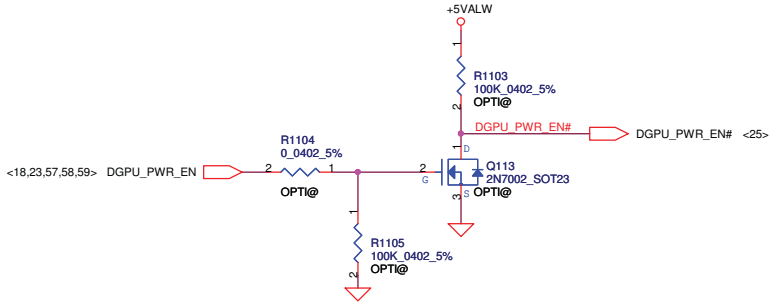
7/26 change SI4800 to SI2301





For Intel S3 Power Reduction.





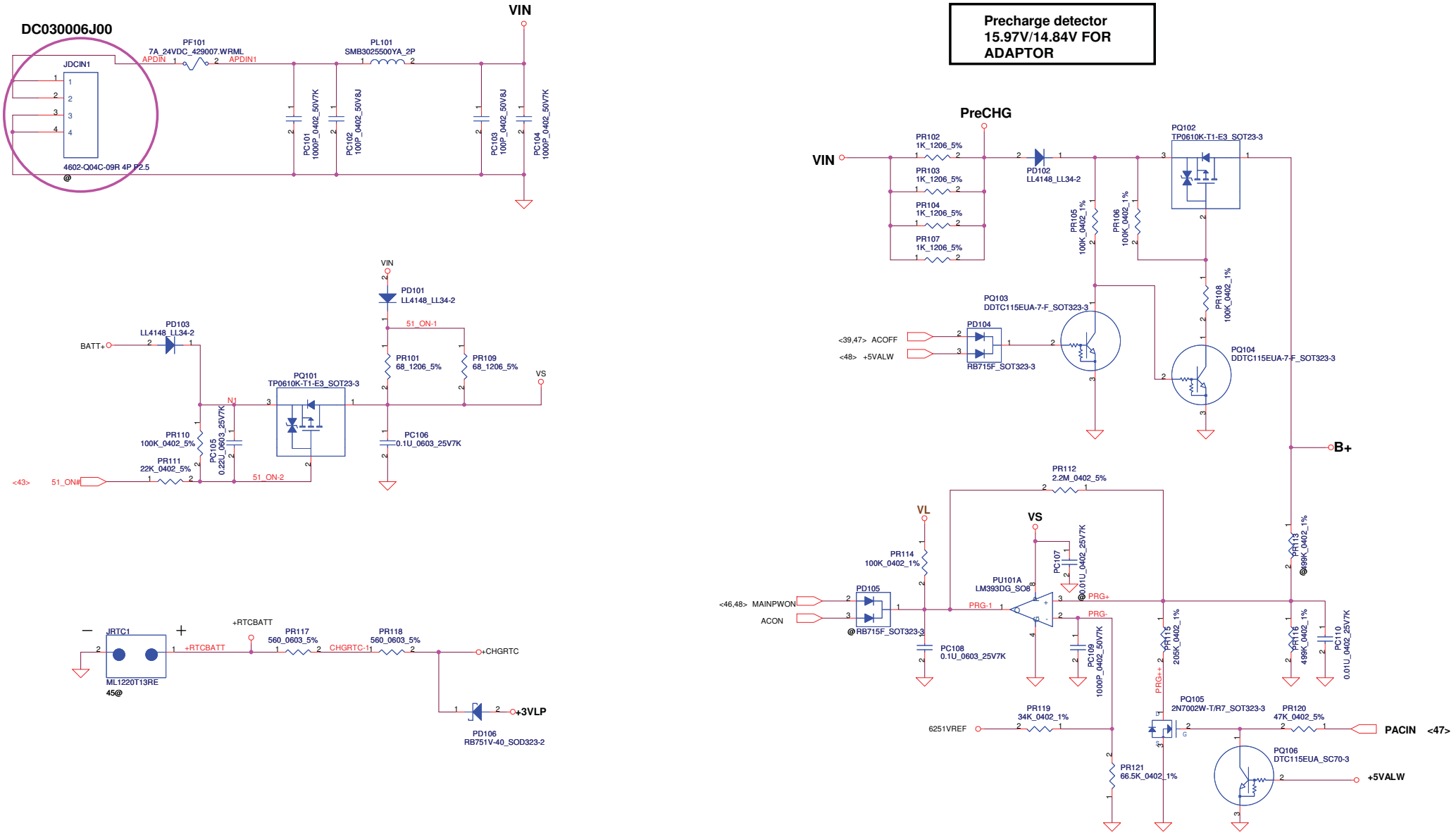
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: **DC Interface**

Size	Document Number	Rev
Custom	LA-6882P	0.2

Date: Wednesday, October 06, 2010 | Sheet 51 of 63



ACIN

Precharge detector	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

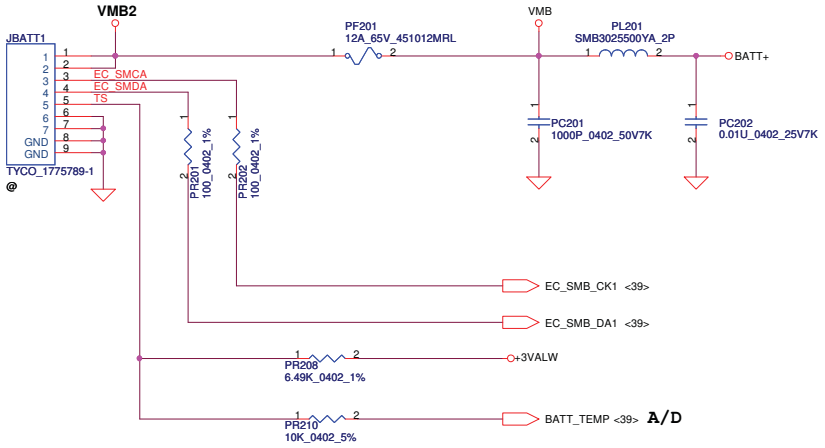
BATT ONLY

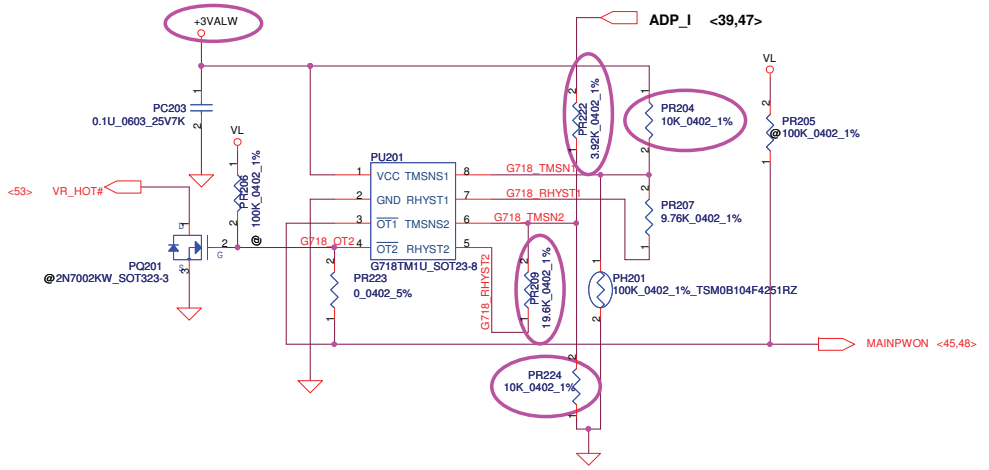
Precharge detector	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

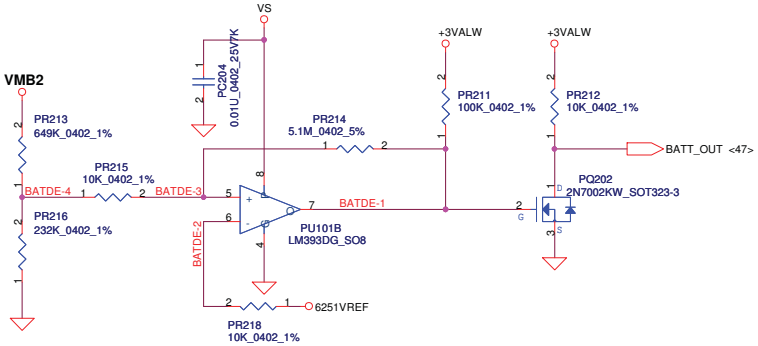
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

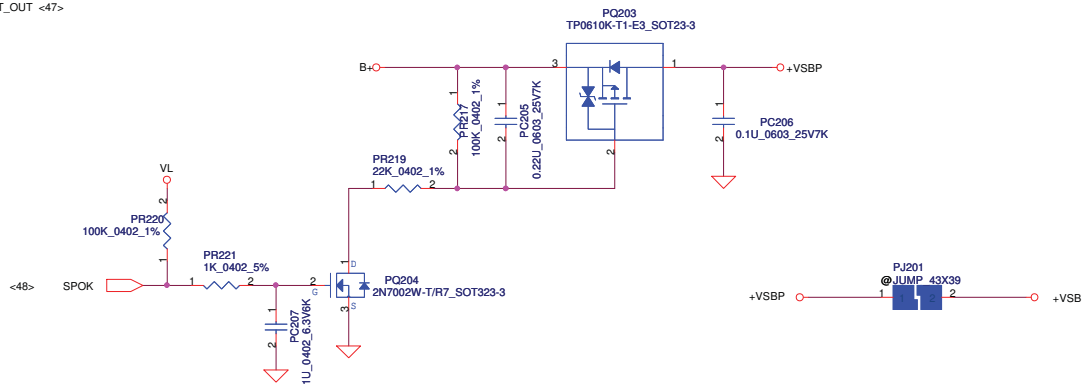
Compal Electronics, Inc.	
Title	PWR DCIN / Vin Detector /Pre-charge
Size: Custom	Document Number: PIQY0/Y1
Rev	0.1
Date: Wednesday, October 06, 2010	Sheet 52 of 63

PH201 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



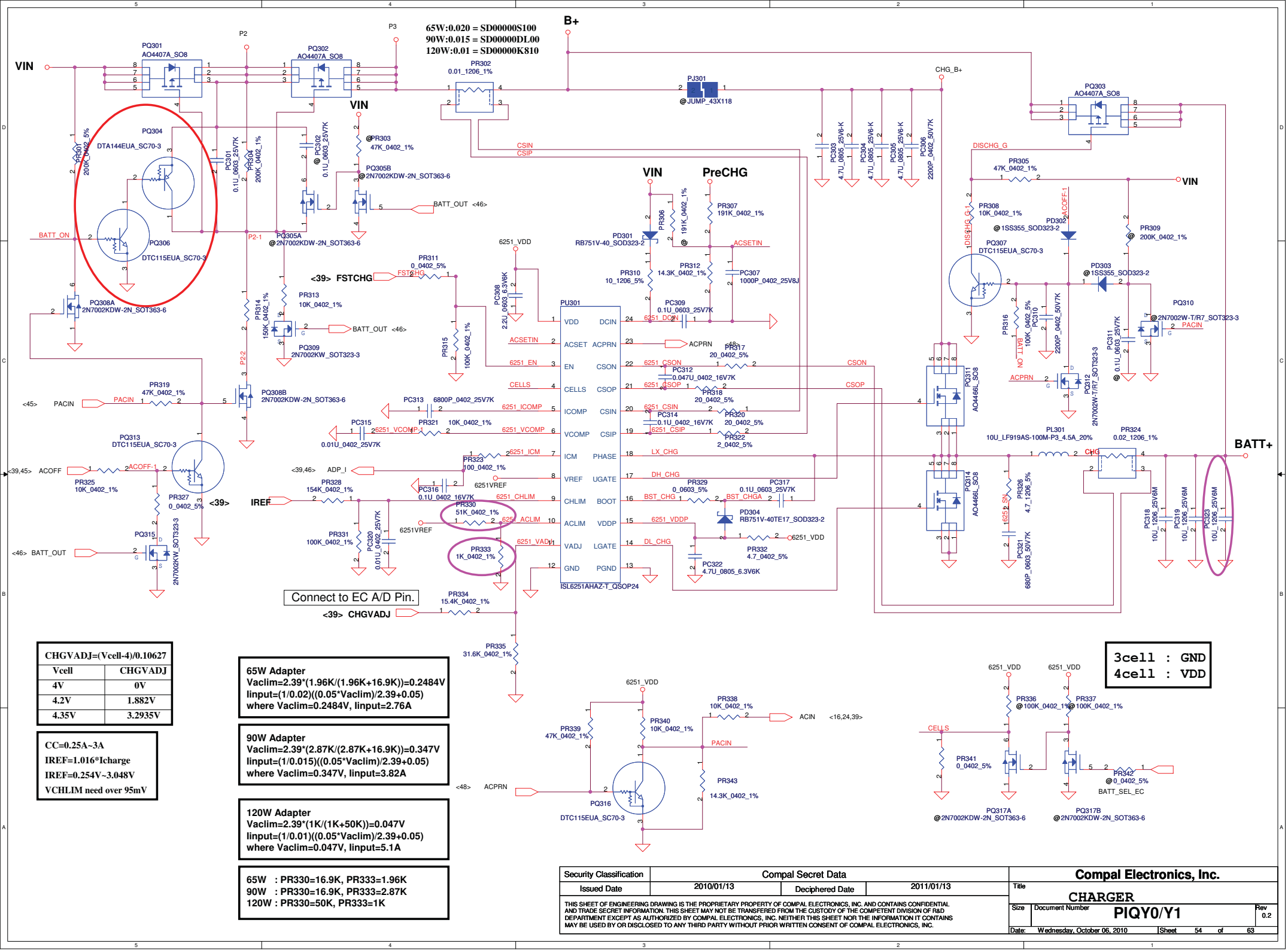






Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.			
Title	PWR-BATTERY CONN/OTP		
Size	Document Number	PIQY0/Y1	Rev 0.1
Custom			
Date:	Wednesday, October 06, 2010	Sheet	53 of 63



CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

65W Adapter
Vaclim=2.39*(1.96K/(1.96K+16.9K))=0.2484V
linput=(1/0.02)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.2484V, linput=2.76A

90W Adapter
Vaclim=2.39*(2.87K/(2.87K+16.9K))=0.347V
linput=(1/0.015)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.347V, linput=3.82A

120W Adapter
Vaclim=2.39*(1K/(1K+50K))=0.047V
linput=(1/0.01)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.047V, linput=5.1A

65W : PR330=16.9K, PR333=1.96K
90W : PR330=16.9K, PR333=2.87K
120W : PR330=50K, PR333=1K

3cell : GND
4cell : VDD

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

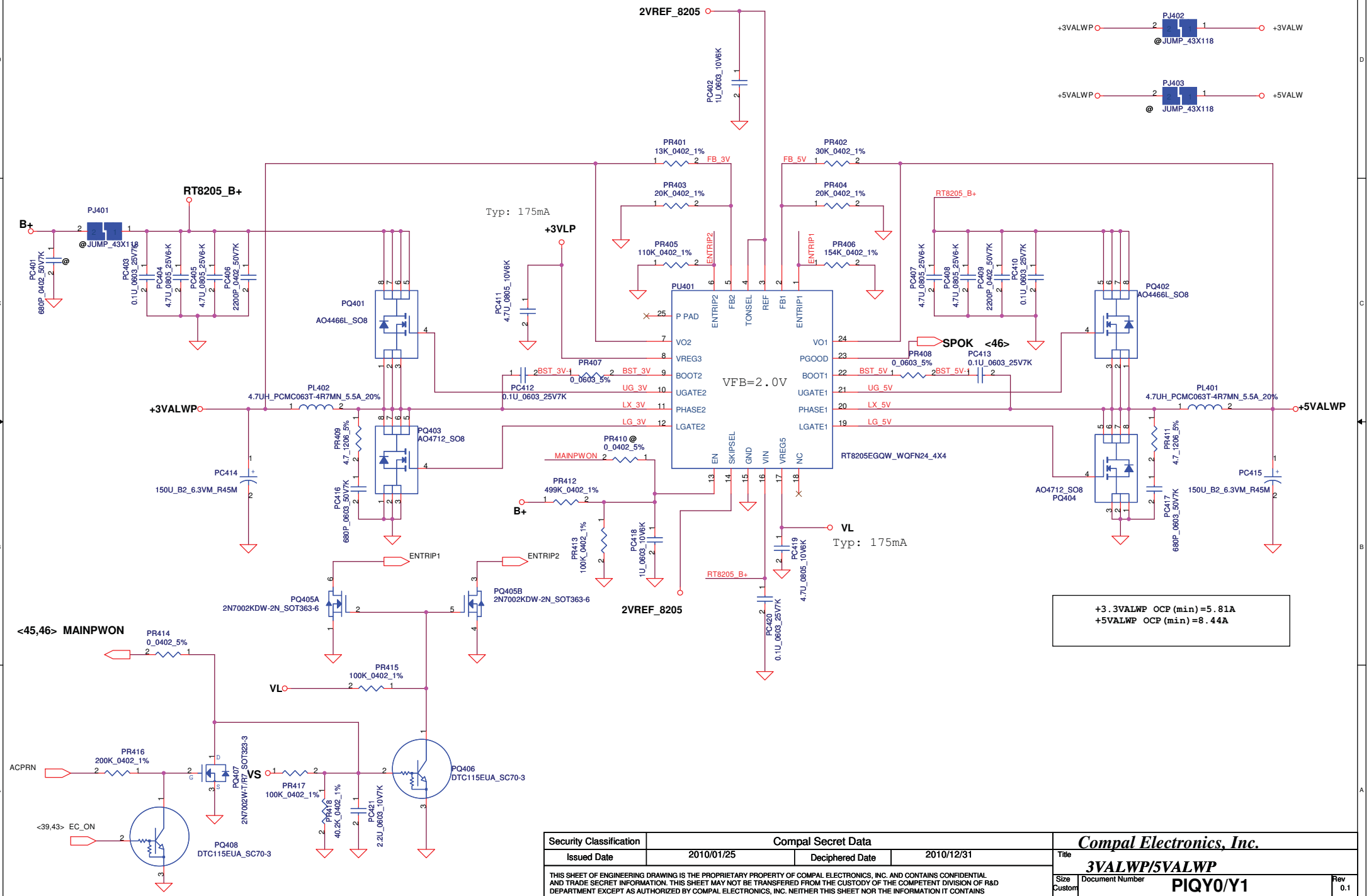
Compal Electronics, Inc.

Title: CHARGER

Size	Document Number	Rev
	PIQY0/Y1	0.2

Date: Wednesday, October 06, 2010 Sheet 54 of 63

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



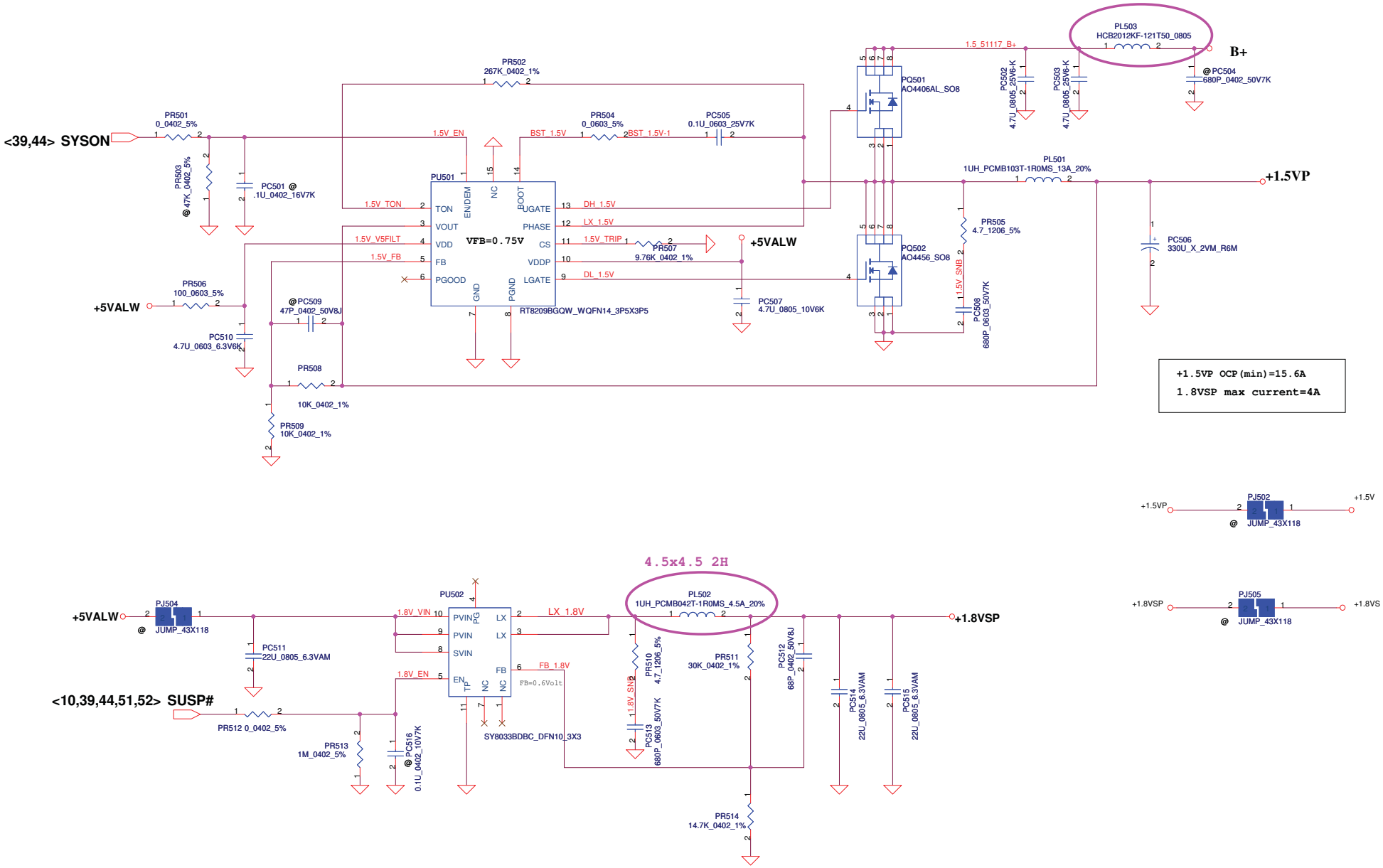
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size	Document Number	Rev
Custom	PIQY0/Y1	0.1

Date: Wednesday, October 06, 2010 Sheet 55 of 63



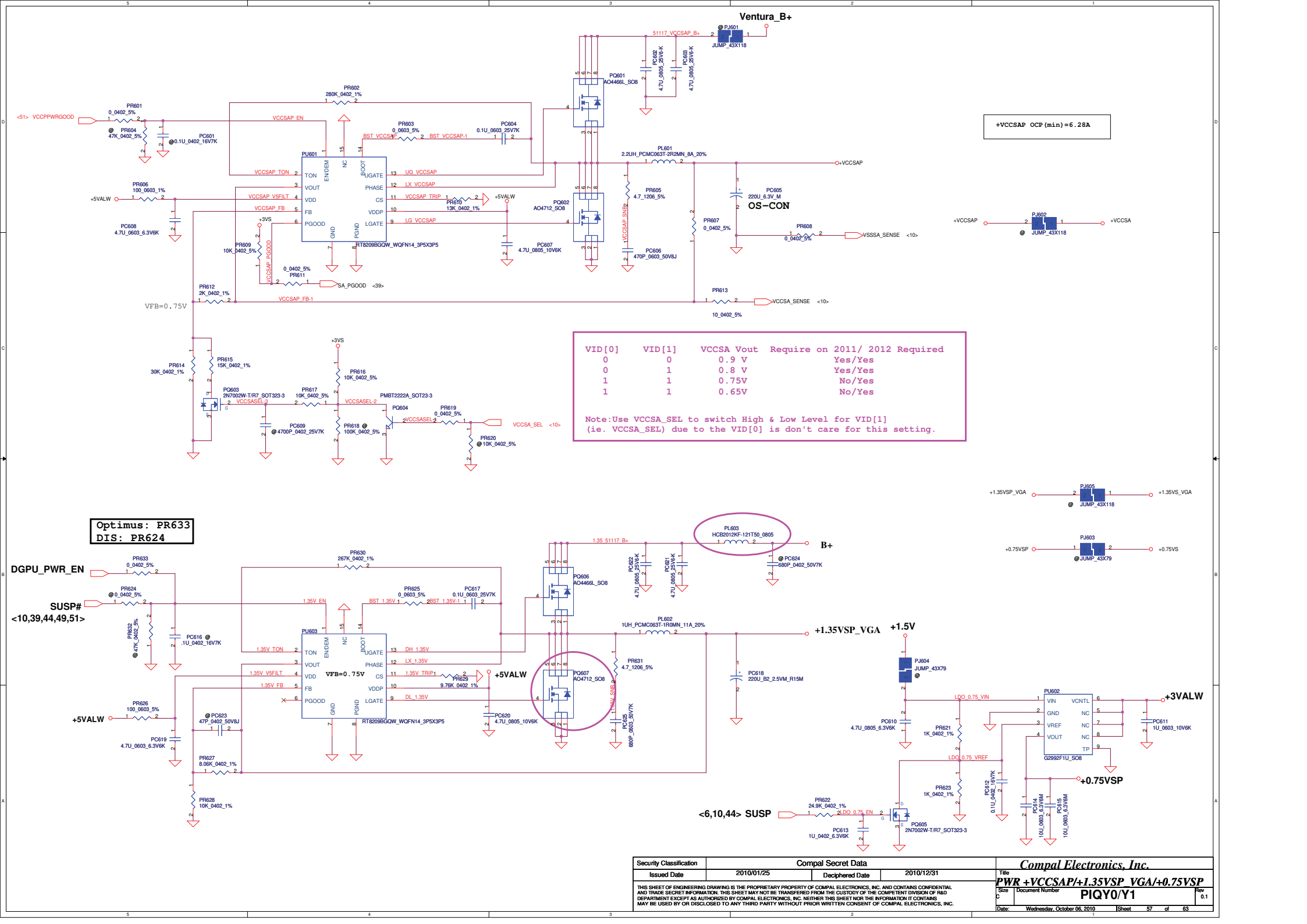
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: *PWR-+1.5VP/+1.8VSP*

Size: Custom | Document Number: PIQY0/Y1 | Rev: 0.1

Date: Wednesday, October 06, 2010 | Sheet 56 of 63


Ventura_B+
+VCCSAP OCP(min)=6.28A
VID[0] VID[1] VCCSA Vout Require on 2011/ 2012 Required
0 0 0.9 V Yes/Yes
0 1 0.8 V Yes/Yes
1 1 0.75V No/Yes
1 1 0.65V No/Yes
Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.
Optimus: PR633
DIS: PR624
DGPU_PWR_EN
SUSP#
<10,39,44,49,51>
B+
+1.35VSP_VGA
+1.5V
+3VALW
+0.75VSP
+5VALW
+VCCSAP
+VCCSA
+1.35VSP_VGA
+0.75VS
<6,10,44> SUSP
VFB=0.75V
OS-CON
RT8209BGQW_WQFN14_3P5X3P5
G2992F1U_SO8
Security Classification
Compal Secret Data
Issued Date
2010/01/25
Deciphered Date
2010/12/31
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Compal Electronics, Inc.
Title
PWR +VCCSAP/+1.35VSP_VGA/+0.75VSP
Size C
Document Number PIQY0/Y1
Rev 0.1
Date: Wednesday, October 06, 2010
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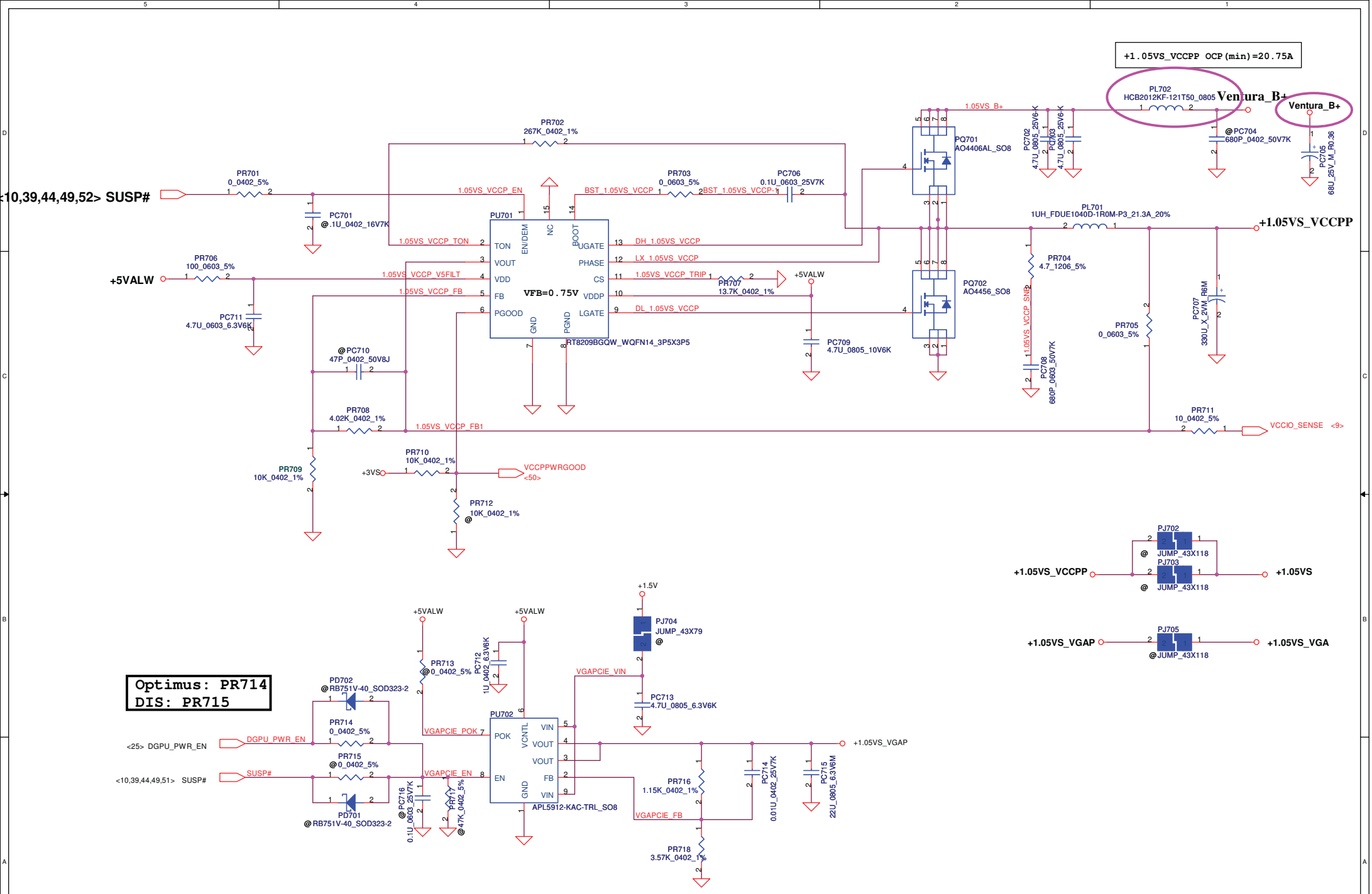


Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR +1.05VS_VCCPP/1.05VS_VGA

Size: Custom | Document Number: PIQY0/Y1 | Rev: 0.1

Date: Wednesday, October 06, 2010 | Sheet 58 of 63

N12P-GS

GPIO6	GPIO5	
GPU_VID1	GPU_VID0	VGA_CORE
0	0	1.0V
0	1	0.975V
1	1	0.825V

N12P-GT/GT1

GPIO6	GPIO5	
GPU_VID1	GPU_VID0	VGA_CORE
0	0	1.075V
0	1	0.925V
1	1	0.825V

Optimus: PR801
DIS: PR802

GS: PR840,PR845,PR847,PR853
GT/GT1:PR843,PR844.PR846,PR854

PU801 ISL6264CRZ-T_QFN40_6X6

PQ807 2N7002KW_SOT323-3
PQ806 2N7002KW_SOT323-3
PQ801 TPCA8030-H_SOP-ADV8-5
PQ802 TPCA8028-H_SOP-ADVANCE8-5
PQ803 TPCA8030-H_SOP-ADV8-5
PQ804 TPCA8028-H_SOP-ADVANCE8-5

PL801 HCB4532KF-800T90_1812
PL802 0.36UH_PCMC104T-R36MN1R17_30A_20%
PL803 0.36UH_PCMC104T-R36MN1R17_30A_20%

PH801 10K_0603_5% TSM1A103J4302RE

B value=4300K

Security Classification	Compal Secret Data
Issued Date	2006/12/12
Deciphered Date	2007/12/12

Compal Electronics, Inc.

Title: **Power-VGA_CORE**

Size: Custom | Document Number: **PIQY0/Y1** | Rev: 0.1

Date: Wednesday, October 06, 2010 | Sheet 59 of 63

Alert# PU resister need close CPU,
so the PU resister in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resister in POWER schematic.

Parallel and tune length

change from 43P to 47P
for shortage problem
2010-03-15

PR956
QC:19.1K
DC:19.6K

PR956
QC:3.724K
DC:2.15K

PR959
QC:1.54K=120A
DC:887=70A

QC: PC935
DC: PC933

PR943
0 ohm =>98A (Vboot=0v)
590 ohm=>91A (Vboot=0v)

B value=4700K

B value=4700K

B value=4250K

Choke PN:SH00000JX00
DCR=1.33~1.396m ohm

Choke PN:SH00000JX00
DCR=1.33~1.396m ohm

Choke PN:SH00000JX00
DCR=1.33~1.396m ohm

Choke PN:SH00000JX00
DCR=1.33~1.396m ohm

*Iccmax in Turbo Mode for SV (35W) is 53A

+CPU_CORE

Icc-max=53A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)10U_0805_4V *10
(2)22U_0805_6.3V *15
(3)470U_D2_2V *4(ESR=4.5m ohm)

*OCP setting value=71.5A

+VGFX_COREP

Ipeak=26A , Imax=18.2A , 1.2Ipeak=31.2A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)22U_0805_6.3V *12
(2)470U_D2_2V *2(ESR=4.5m ohm)

*OCP setting value=37A

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR +CPU_CORE/+VGFX_CORE

Size: Custom | Document Number: PIQY0/Y1 | Rev: 0.1

Date: Wednesday, October 06, 2010 | Sheet 60 of 63

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Compal Electronics, Inc.

Title: PIR (PWR)

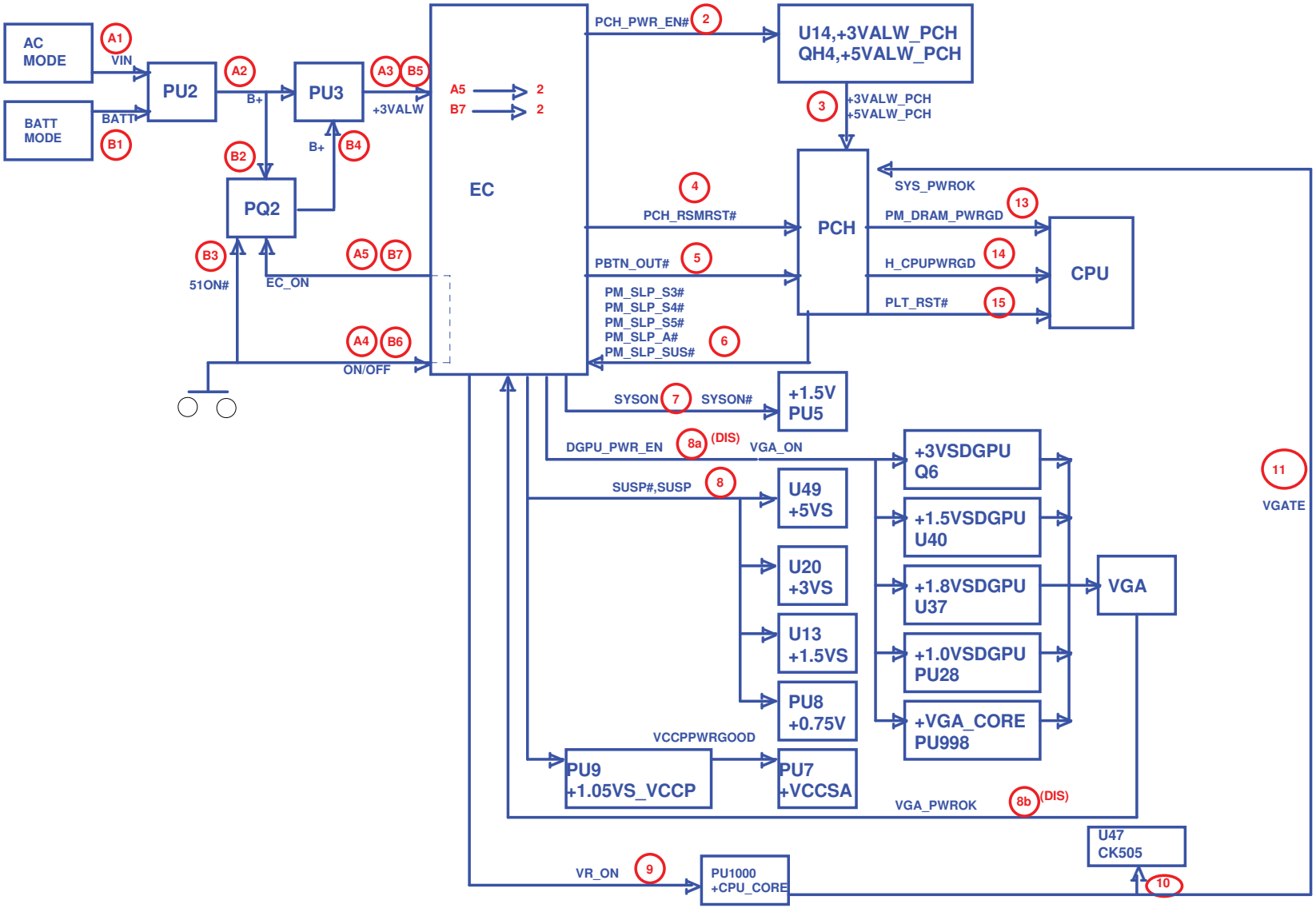
Size: Custom | Document Number: PIQY0/Y1 | Rev: 0.1

Date: Wednesday, October 06, 2010 | Sheet 61 of 63

PIQY1 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
				EVT TO DVT
1		P18	Reserve R297	Reserve pull down for PCH GPIO53.
2		P18	Exchange SATA port0 & port1	For fast boot function.
3		P50	Change KB light control circuit	Change KB light control from PWM to on/off.
4		P36	Add F2 (poly-fuse)	For HDMI port diode protection.
5		P19	Stuff R303, unstuff R340	Change ESATA_DET# to GPIO1.
6		P49	Stuff R1068, reserve R1071,R1072,R1099,Q121	Reserve USB3.0 power swicth control inverter circuit.
7		P48	Add R1154	For CHG_ON# pull down.
8		P45	Stuff R996,R139,C815, unstuff R1000,C732,C733,Y5	Change EC CLK from crystal to SUSCLK.
9		P37	Add U60, Q132, C921, R1329, Q133, R1328	Add WLAN power switch circuit
10		P09	Add C922	Add C922 to place at CPU sdie.
11		P21	Add R1330	Add for INTVREN control
12		P47	Modify LED1,LED2,LED3,LED5	Change LED type
13		P45	Modify TP_LED#, PCH_DPWROK and LED_KB_PWM link	Change LED_KB_PWM to U36. pin26 GPIO12.
14		P18	Delete EN_CARD_PW#, EN_WOL#	Add FAST_BOOT# to replace EN_CARD_PW# and EN_WOL#
15		P48	Delete USB charger circuit	Remove USB charger function
16		P47	Modify H5,H6,H7 size	From H_3P0 to H_3P8
17		P42	Change C660, C661 from 3300p to 0.1u	For 100Hz High Pass filter
18		P43	Replace R958, R959 to C926, C927 0.033u	For 100Hz High Pass filter
19		P50	Remove EC_SMB_CK2, EC_SMB_DA2 link to JP13	Remove light sensor function
20		P42	Add C928, C929	EMI Request
21		P49	Add J19	for USB30, USB20 colayout design
			Modify J18, J20	for USB30, USB20 colayout design
22		P14	Add Q134, R1347, R1346	Add for Fast boot SPI ROM selection by EC.
23		P37, P44	Add R1344,R1343	Added for WLAN and CARD reader Reset signal.
24		P19	Add R1345	Added for VENTURA detection.

Compal Electronics, Inc.		
Title: PIR (HW)		
Size: Custom	Document Number: LA-6882P	Rev: 0.2
Date: Wednesday, October 06, 2010	Sheet 62 of 63	



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: Power sequence

Size	Document Number	Rev
Custom	LA-6361P	0.1

Date: Wednesday, October 06, 2010 Sheet 63 of 63