



# Compal Confidential

## DIS M/B Schematics Document

Haswell with DDRIII + Lynx Point PCH

MARS XT / SUN PRO

2012-08-06

LA-9641P

REV: 0.1

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# Shark Bay

**AMD MARS XT M2 128 bits / SUN PRO M2 64 bits**

VRAM 512MB/1GB/2GB  
MARS XT : DDR3 x 8  
SUN PRO : DDR3 x 4

page 23~32

PEG 8x Gen2 / Gen3

**Intel Processor Haswell**

rPGA946  
37.5mm x 37.5mm

page 5,~11

Memory Bus Dual Channel

**204pin DDRIII-SO-DIMM X2**  
BANK 0, 1, 2

page 12,13

DDR3L 1600MHz  
DDR3L 1333MHz

**LVDS Conn.**  
page 31

**LVDS Translator**  
RTD2132R(Single)

page 33

**HDMI Conn.**  
page 36

FDI \*2  
2.7GT/s

DMI2 \*4  
5GT/s

**CRT Conn.**  
page 35

**RJ45 Conn.**  
page 39

**LAN**  
Atheros AR8162/QCA8172 (10/100)

page 38

PCIe x1

**PCIe Mini Card WiMax**  
USB20 Port 10

page 28

**PCIe Mini Card WLAN**  
PCIe Port 0

page 28

PCIe x1

USB20 x1

**Intel PCH Lynx Point**

FCBGA 695Balls  
20mm x 20mm

USB30 x2

**Left USB3.0 x2**  
USB30 Port 0,1

page 46

**Right USB2.0**  
USB20 Port 9

page 46

**Int. Camera**  
USB20 Port 3

page 33

USB20 x6

**Touch Screen**  
USB20 Port 2

**Card Reader**  
Realtek RTS5170  
USB20 Port 11

page 44

SATA Gen3

**HDD Conn.**  
SATA Port 4

page 41

SATA

**ODD Conn.**  
SATA Port 5

page 41

AZALIA

**Audio Codec**  
CONEXANT CX20757

page 42

**Int. MIC Conn.**

page 42

**Int. Speaker Conn.**

page 42

**Audio Combo Jacks**  
HP & MIC

page 42

**SPI ROM**  
2MB + 4MB

page 17

**EC**  
ENE KB9012

page 44

**Thermal Sensor**

page 40

**Touch Pad**

page 44

**Int. KBD**

page 44

Sub-board

**15"**

**14"**

**Power/B LSXXXP**  
page 44

**LED/B LSXXXP**  
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**USB/B LSXXXP**  
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**CR/B LSXXXP**  
page 44

**ODD/B LSXXXP**  
page 44

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				Block Diagram
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### Voltage Rails

power plane	+B	+5VALW	+1.35V	+5VS
		+3VALW		+3VS
State				+VCC_CORE
				+VGA_CORE
				+1.5VS
				+0.675VS
				+1.05VS
S0	○	○	○	○
S3	○	○	○	X
S5 S4/AC	○	○	X	X
S5 S4/ Battery only	○	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

### EC SM Bus1 address

### EC SM Bus2 address

Device	Address
Smart Battery	0001 011X b

Device	Address
Thermal Sensor	1001_100xb

### PCH SM Bus address

### AMD-GPU SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

Device	Address
Internal thermal sensor	1000_001xb

Device	Address
RTD2132R	1101 010Xb

### BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF



### Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%					
Ra/Rc/Re	100K +/- 5%					
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max	Project	Phase
0	0	0 V	0 V	0 V	G-series	MP
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	G-series	PVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	G-series	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	G-series	EVT

### USB Port Table

USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0
		1
		2
	UHCI1	3
		4
		5
		6
EHCI2	UHCI3	7
		8
	UHCI4	9
		10
	UHCI5	11
		12
	UHCI6	13

### BOM Structure Table

BTO Item	BOM Structure
DIS	PX@
MARS XT	MARS@
SUN PRO	SUN@
HDMI	HDMI@
Deep S3	DS3@
NO Deep S3	NODS3@
8162 LAN	8162@
8172 LAN	8172@
LAN LDO MODE	LDO@
LAN SWR MODE	SWR@
LAN Surge	GAS@
USB30	USB30@
Camera	CMOS@
LAN Switch mode	SWR@
Touch screen	TS@
GREEN CLOCK	GCLK@
DIS GREEN CLOCK	GCLK304@
UMA GREEN CLOCK	GCLK244@
NO GREEN CLOCK	NOGCLK@
14"	14@
15"	15@
45 LEVEL	45@
X76 LEVEL	X76@
Unpop	@
AUDIO PART	MIC@
Connector	ME@

VRAM BOM STRUCTURE Refer P4. VGA NOTE

### SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH	RTD2132
SMB_EC_CK1	KB9012	X	V	X	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW						
SMB_EC_CK2	KB9012	X	X	X	X	X	X	+3VS	+3VS
SMB_EC_DA2	+3VALW								
SMBCLK	PCH	X	X	X	V	V	X	X	X
SMBDATA	+3VALW				+3VS	+3VS			
SML0CLK	PCH	X	X	X	X	X	X	X	X
SML0DATA	+3VALW								
SML1CLK	PCH	V	X	V	X	X	V	X	V
SML1DATA	+3VALW	+3VS		+3VS			+3VS		+3VS

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### Power-Up/Down Sequence

"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD\_CT have ramped up.
- VDDC and VDD\_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD\_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.

#### Mars XT VRAM STRAP

	<b>x76@</b>	<b>x76@</b>	<b>x76@</b>	<b>x76@</b>	<b>x76@</b>	<b>x76@</b>
	Vendor UV5, UV6, UV7, UV8 UV9, UV10, UV11, UV12	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV20	R_pd RV27
ZZZ4 MS2G@ 2GBytes	Samsung 2048Mbits SA000068U00 128Mx16 K4W2G1646E-BC1A	0	0	0	NC	4.75K
ZZZ5 MM2G@ 2GBytes	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	0	0	1	8.45K	2K
ZZZ6 MH2G@ 2GBytes	Hynix 2048Mbits TBD H5TQ2G63DFR-NOC	0	1	0	4.53K	2K
ZZZ7 MS1G@ 1GBytes	Samsung 1028Mbits SA00004GS00 64Mx16 K4W1G1646G-BC11	0	1	1	6.98K	4.99K
ZZZ8 MH1G@ 1GBytes	Hynix 1024Mbits SA000041SB0 64Mx16 H5TQ1G63EFR-11C	1	1	1	4.75K	NC



VDDR3(3.3VGS)

PCIE\_VDDC(0.95VGSV)

VDDR1(1.5VGS)

VDDC/VDDCI(1.12V)

VDD\_CT(1.8V)

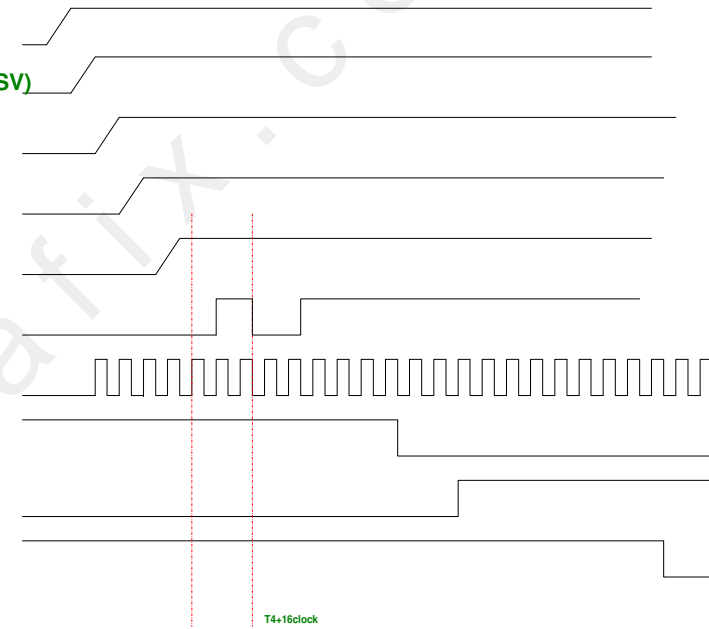
PERSTb

REFCLK

Straps Reset

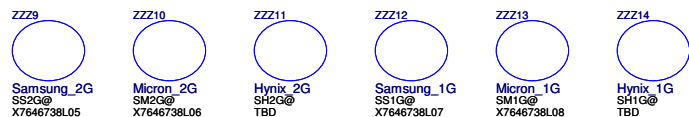
Straps Valid

Global ASIC Reset

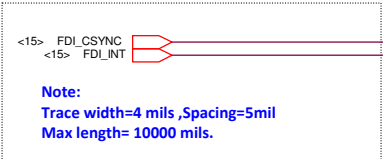
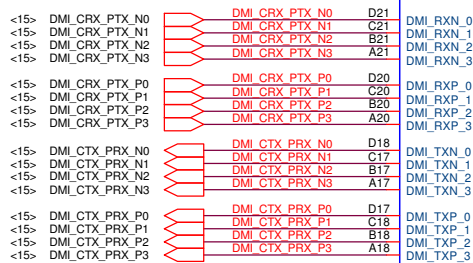
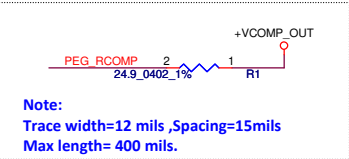
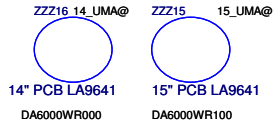
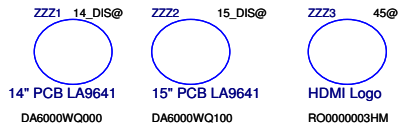


#### Sun PRO VRAM STRAP

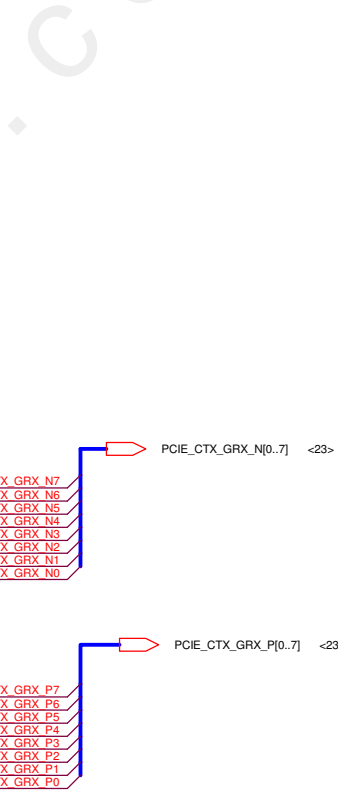
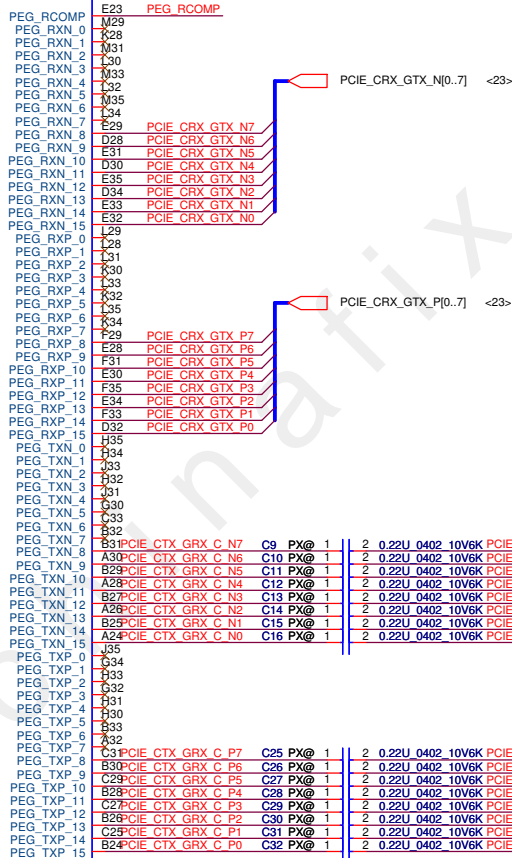
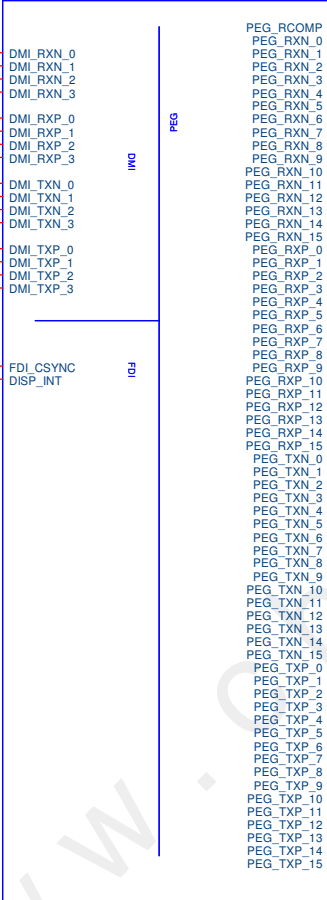
	<b>x76@</b>	<b>x76@</b>	<b>x76@</b>	<b>x76@</b>	<b>x76@</b>	<b>x76@</b>
	Vendor UV9, UV10, UV11, UV12	PS_3[3]	PS_3[2]	PS_3[1]	R_pu RV20	R_pd RV27
ZZZ9 SS2G@ 2GBytes	Samsung 4096Mbits SA000068R00 256Mx16 K4W4G1646B-HC11	0	0	0	NC	4.75K
ZZZ10 SM2G@ 2GBytes	Micron 4096Mbits SA000065D00 256Mx16/1866 MT41K256M16HA-109G:E	0	0	1	8.45K	2K
ZZZ11 SH2G@ 2GBytes	Hynix 4096Mbits SA00006DG00 256MX16 H5TQ4G63MFR-11C	0	1	0	4.53K	2K
ZZZ12 SS1G@ 1GBytes	Samsung 2048Mbits SA000068U00 128Mx16 K4W2G1646E-BC1A	0	1	1	6.98K	4.99K
ZZZ13 SM1G@ 1GBytes	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	1	1	0	3.4K	10K
ZZZ14 SH1G@ 1GBytes	Hynix 2048Mbits TBD H5TQ2G63DFR-NOC	1	1	1	4.75K	NC



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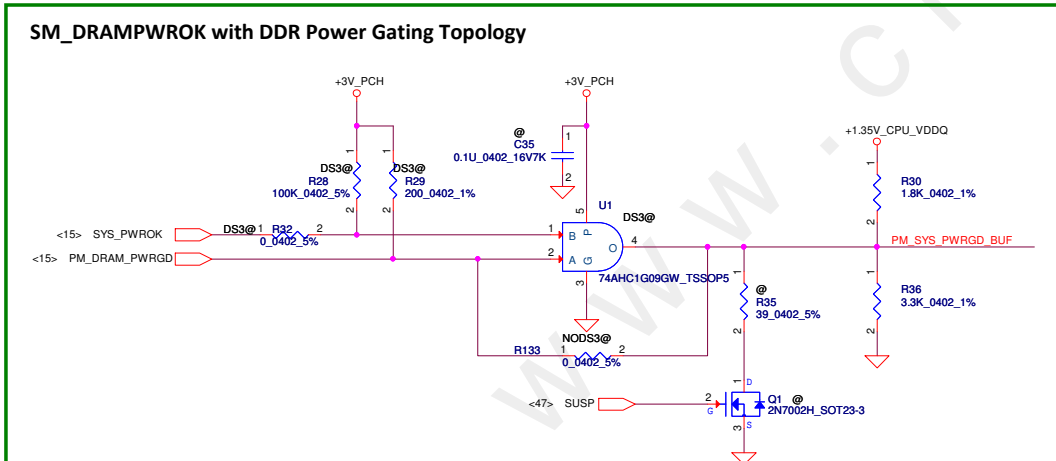
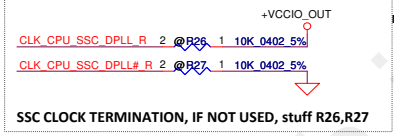
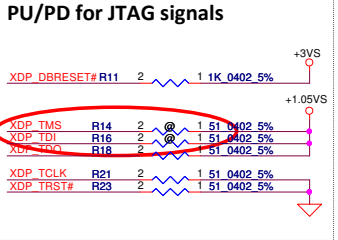
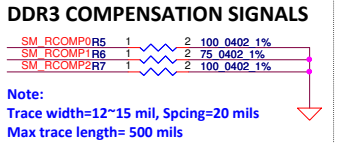
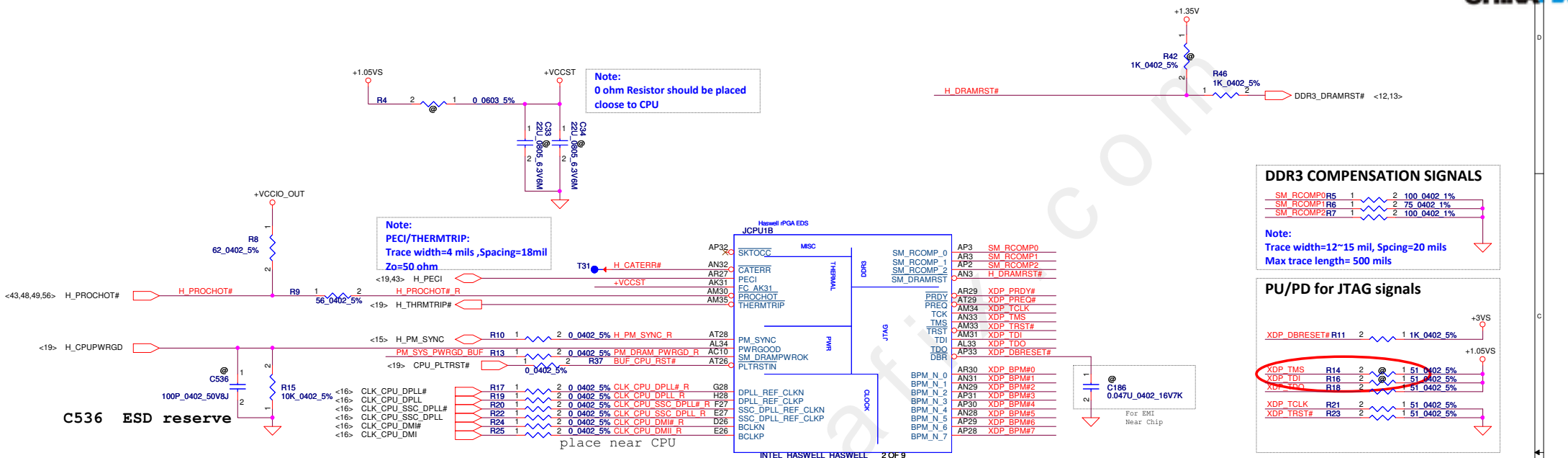
Haswell iPGA EDS  
JCPU1A

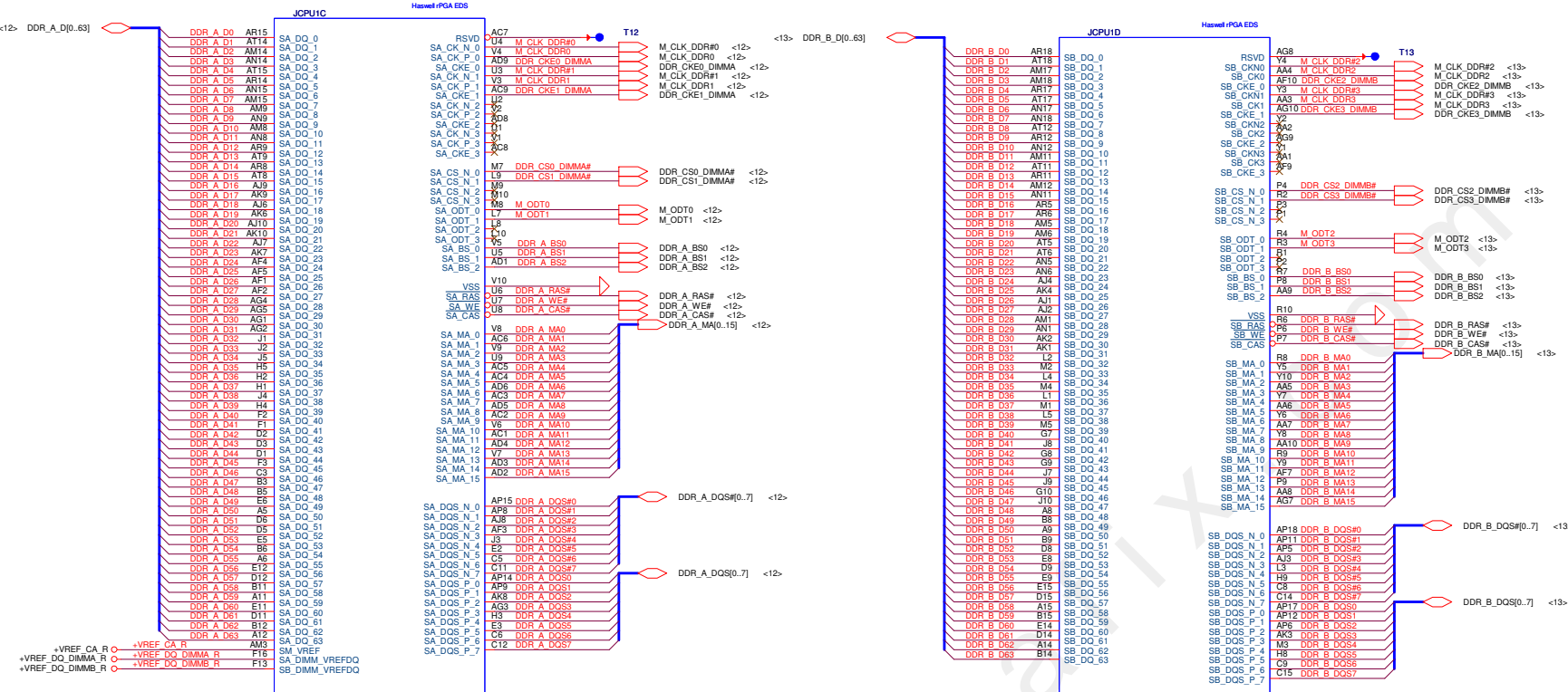


INTEL\_HASWELL\_HASWELL 1 OF 9

ME@

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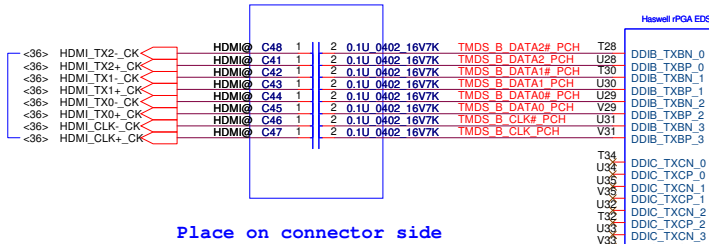
INTEL\_HASWELL\_HASWELL 3 OF 9 INTEL\_HASWELL\_HASWELL 4 OF 9

CPI DRIVER VREF PATH IS DEFAULT

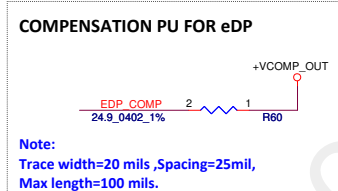
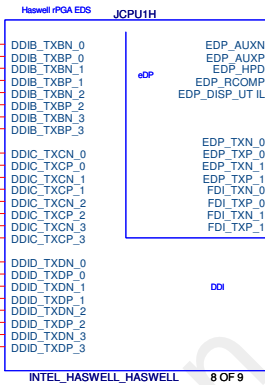
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HDMI D2  
HDMI D1  
HDMI D0  
HDMI CLK

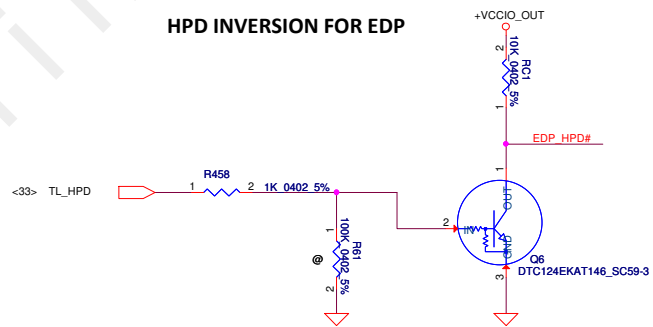
HDMI



Place on connector side



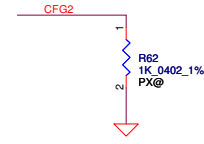
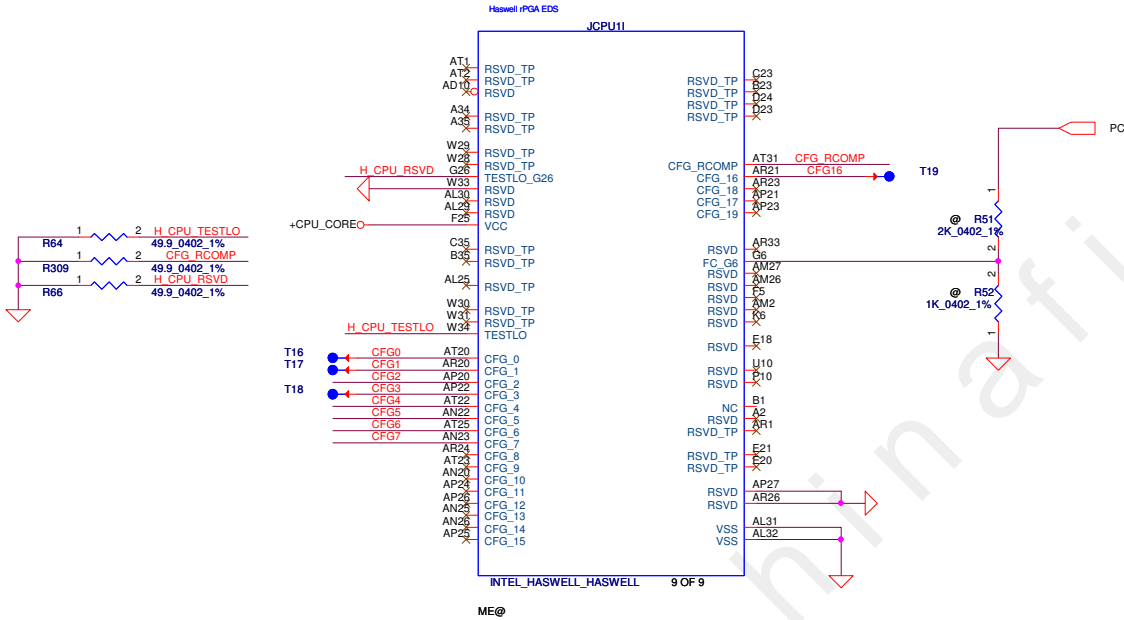
### HPD INVERSION FOR EDP



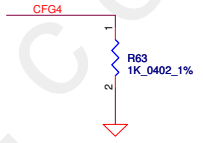
HPD is a active high signal from device. The HPD processor input is a low voltage active signal.



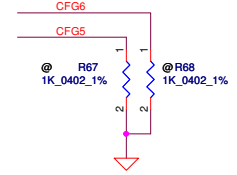
### CFG Straps for Processor



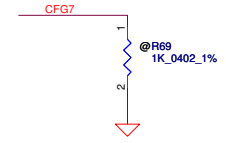
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed



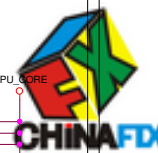
Embedded Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



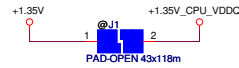
PCIe Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

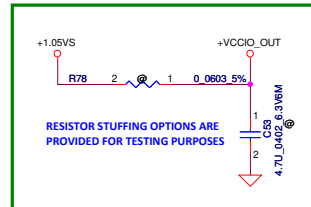
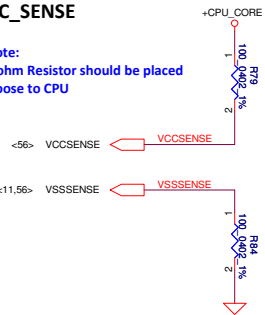


### +1.35V\_CPU\_VDDQ Source

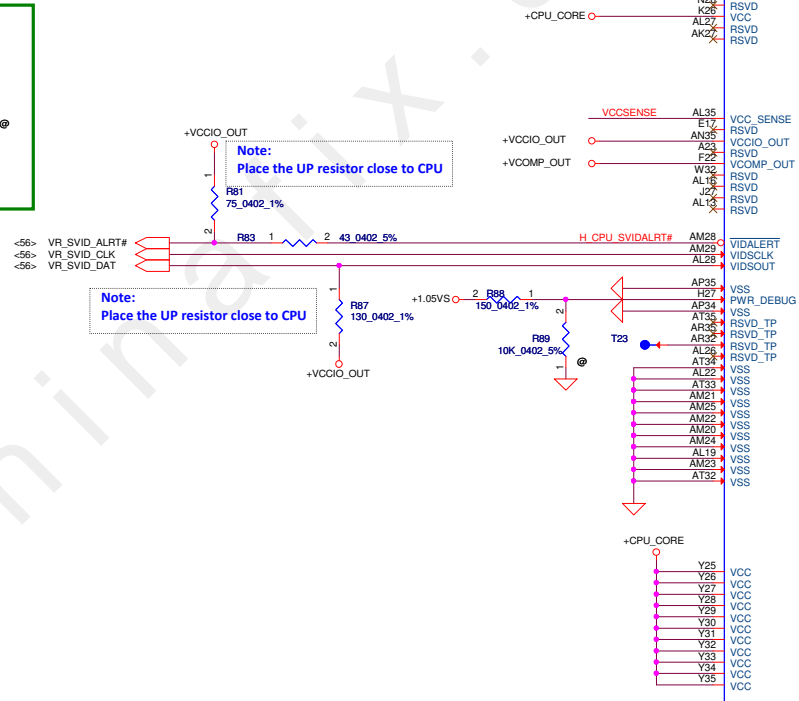


### VCC\_SENSE

Note:  
0 ohm resistor should be placed close to CPU



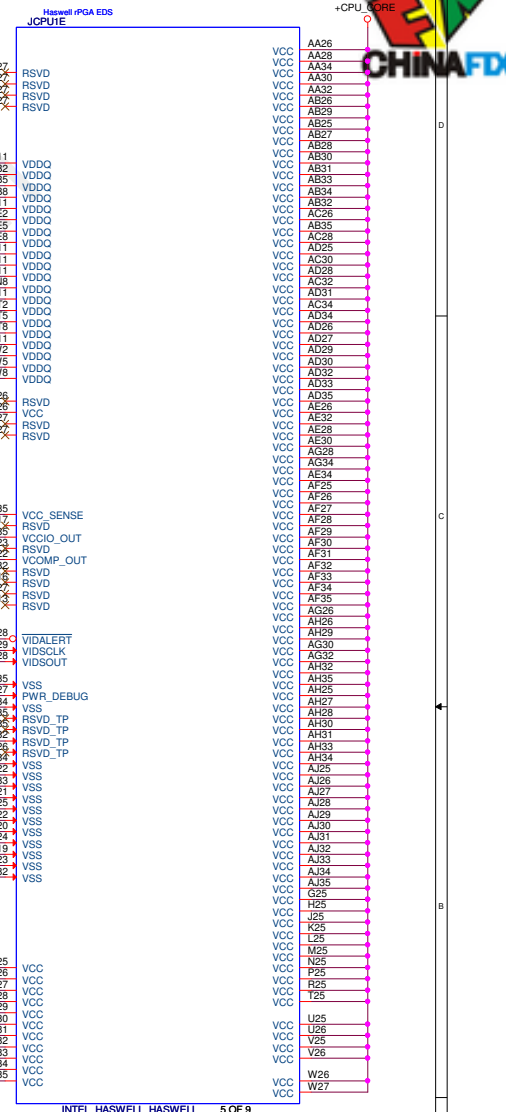
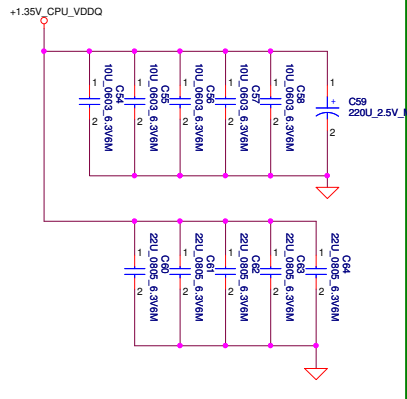
RESISTOR STUFFING OPTIONS ARE PROVIDED FOR TESTING PURPOSES



Note:  
Place the UP resistor close to CPU

Note:  
Place the UP resistor close to CPU

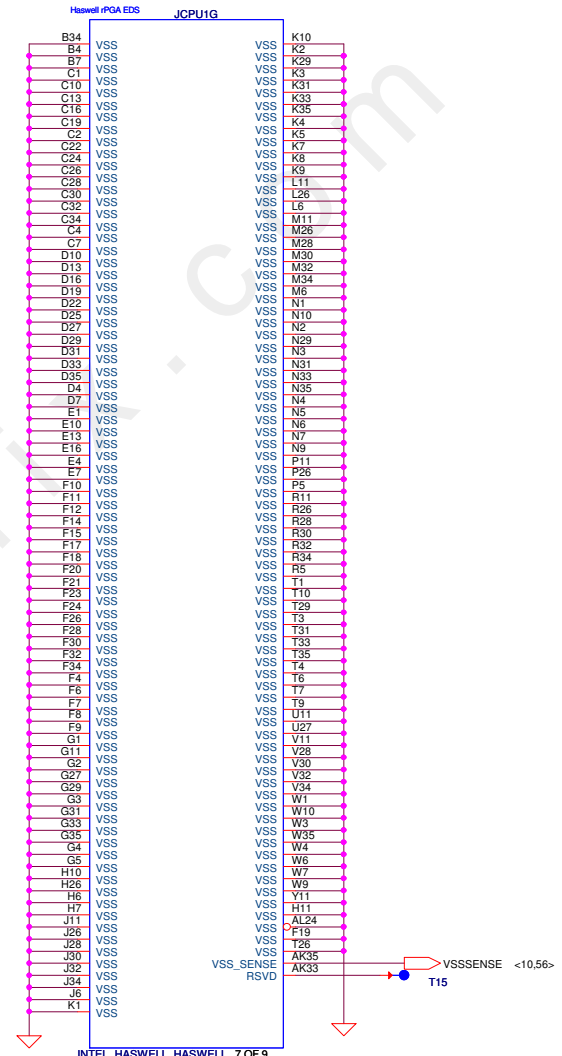
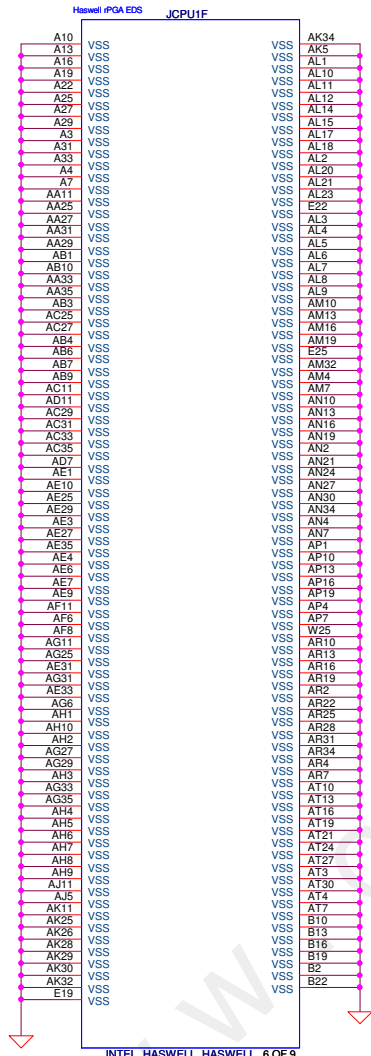
### VDDQ DECOUPLING



INTEL\_HASWELL\_HASWELL 5 OF 9

ME@

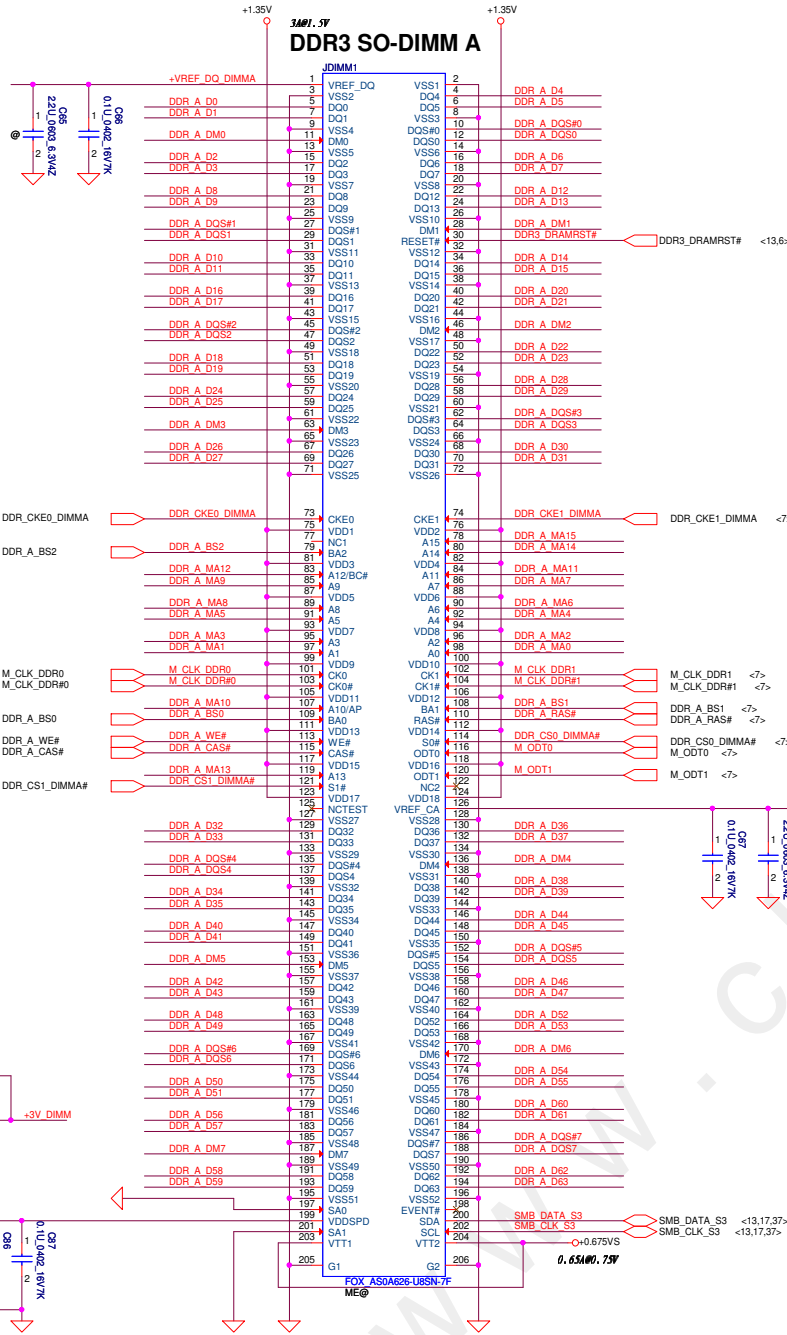
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Issued Date	2011/06/15	Deciphered Date	2012/07/11
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			Rev 0.1 Sheet 10 of 60



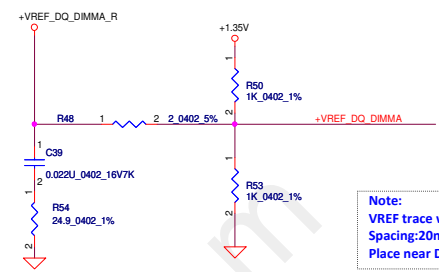
Security Classification	Compal Secret Data		Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Compal Electronics, Inc.
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				Rev 0.1
				Sheet 11 of 60



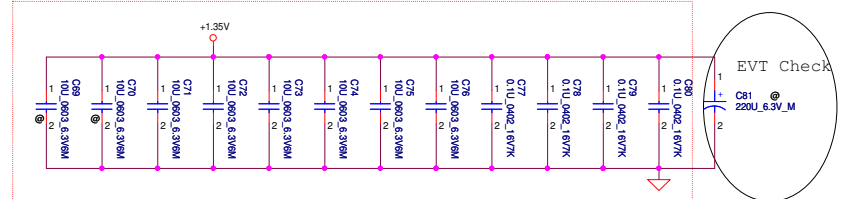
### DDR3 SO-DIMM A



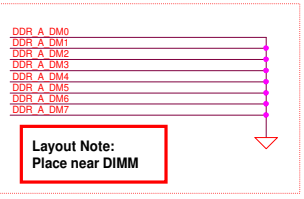
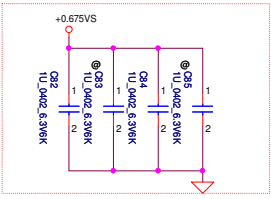
- <-> DDR\_A\_D[0..63]
- <-> DDR\_A\_DQS[0..7]
- <-> DDR\_A\_DQS# [0..7]
- <-> DDR\_A\_MA [0..15]



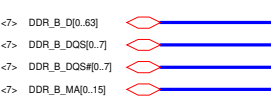
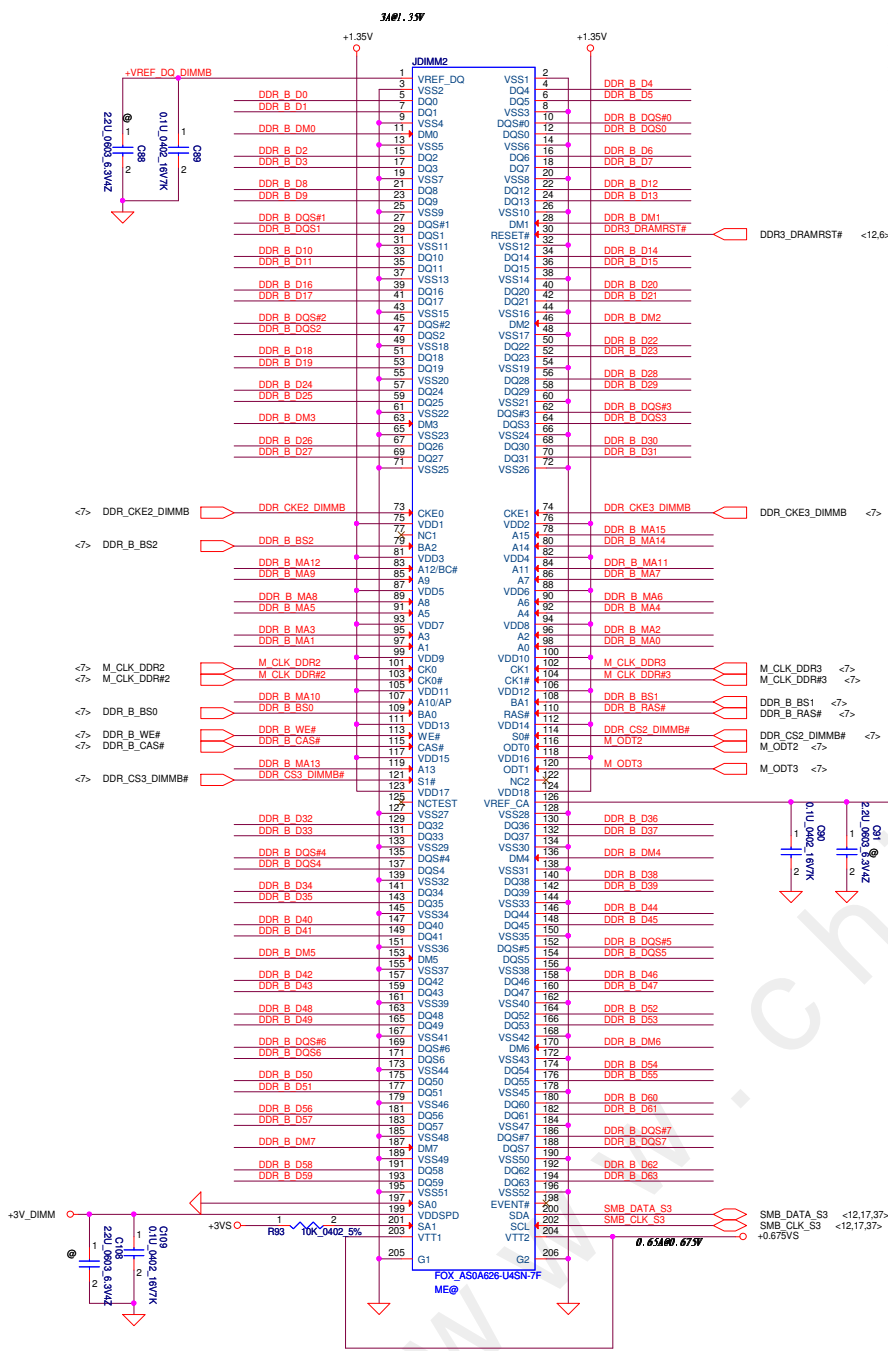
Layout Note: Place near DIMM



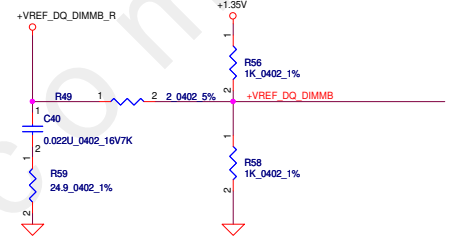
Layout Note: Place near DIMM



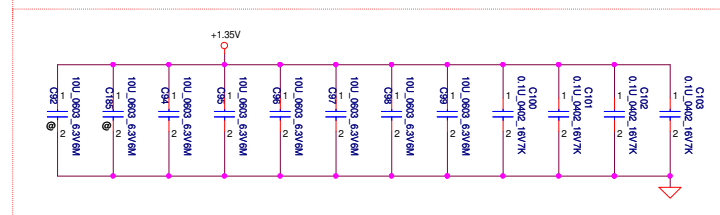
Security Classification	Compal Secret Data		Title	<b>Compal Electronics, Inc.</b>	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	<b>DDR3-SODIMM SLOT1</b>	
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Doc No	LA-7981P	Sheet	12 of 60		
Date:	Thursday, October 11, 2012	ISheet			



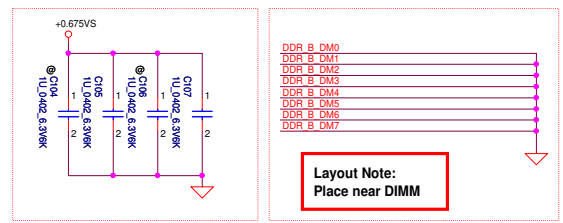
Note:  
VREF trace width: 20 mils at least  
Spacing: 20mils to other signal/planes



Layout Note:  
Place near DIMM

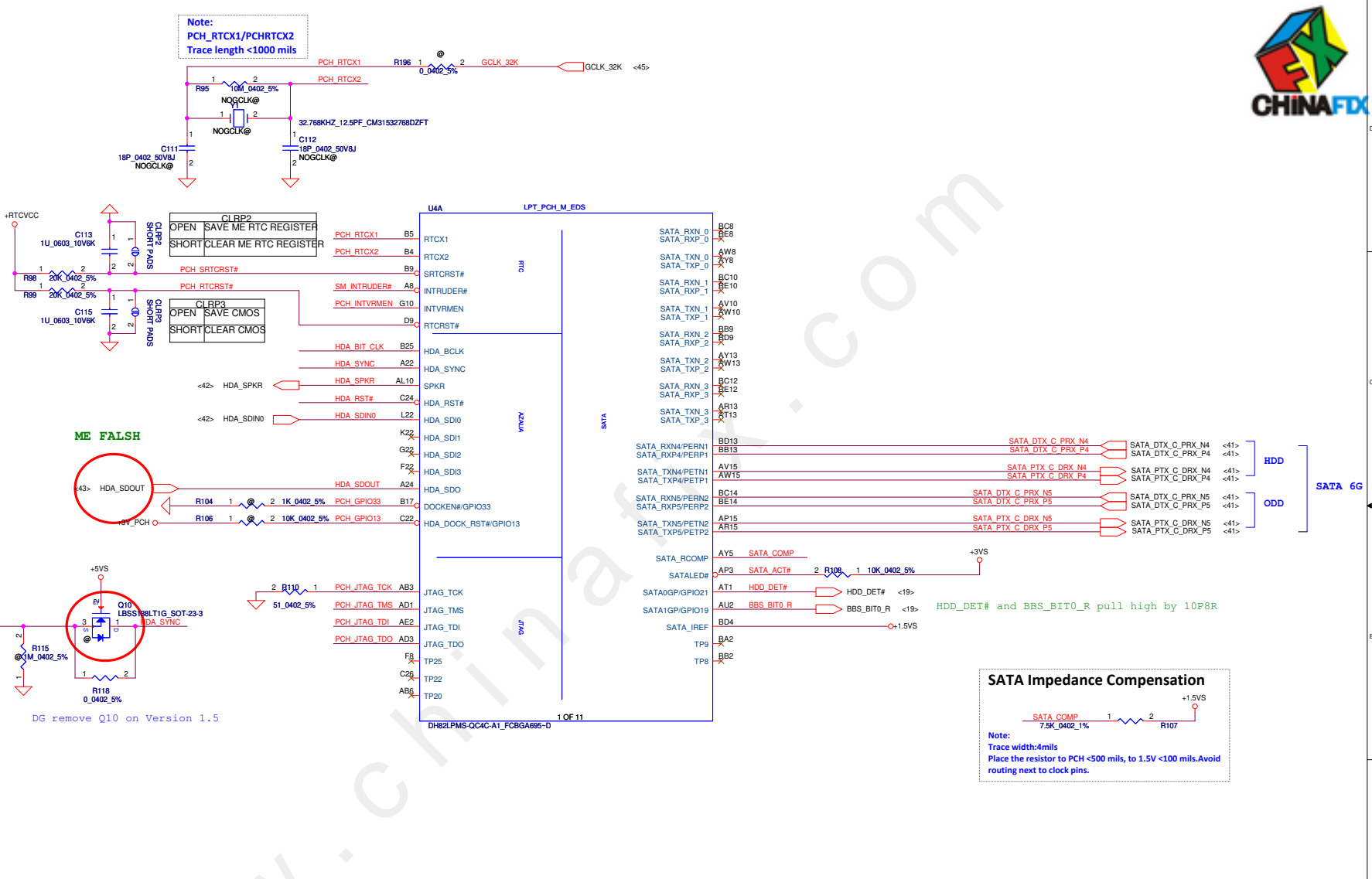
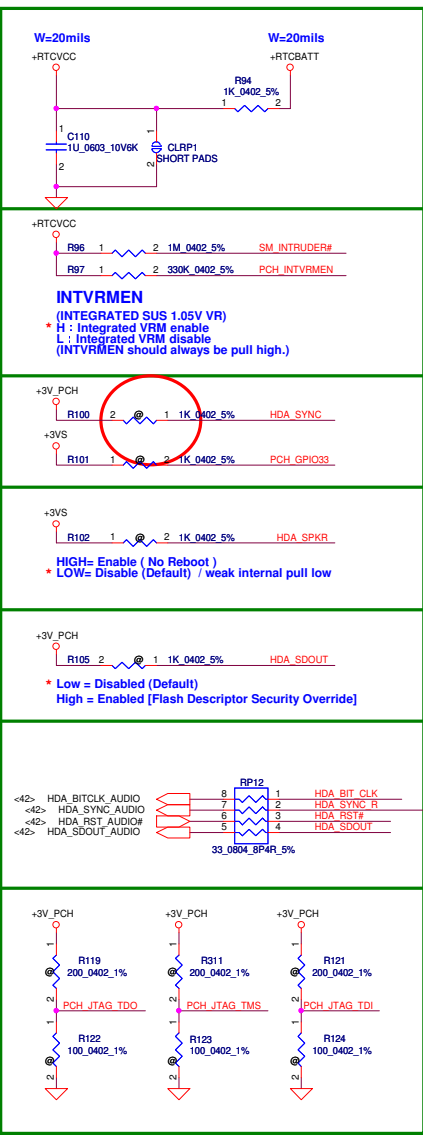


Layout Note:  
Place near DIMM

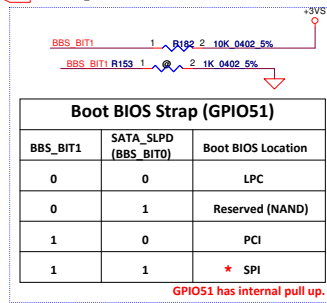
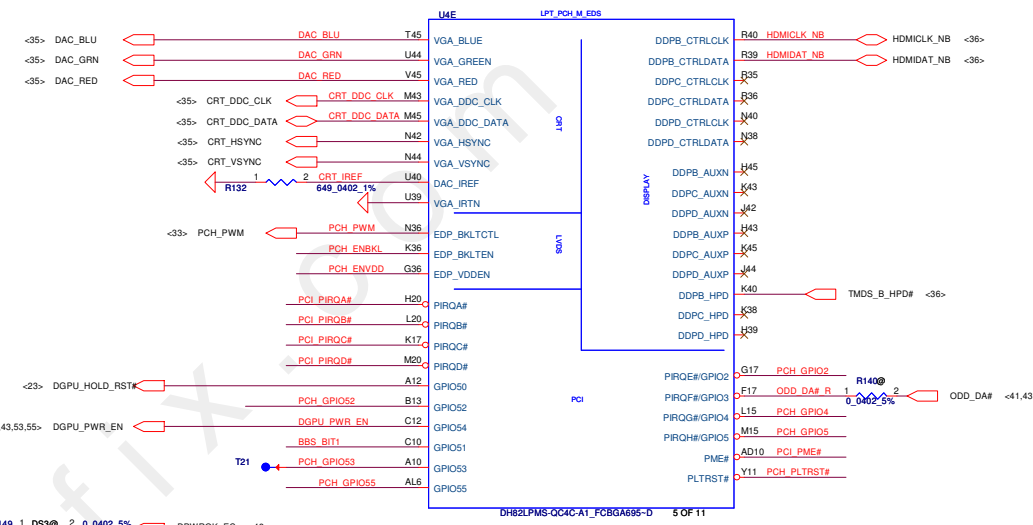
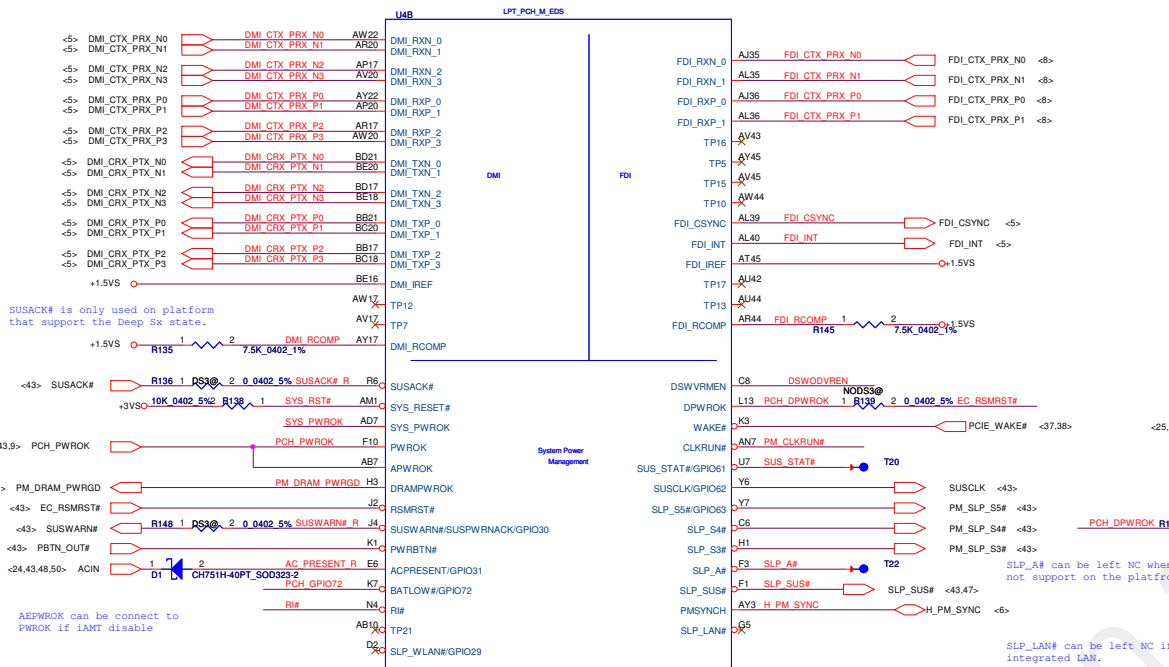


Layout Note:  
Place near DIMM

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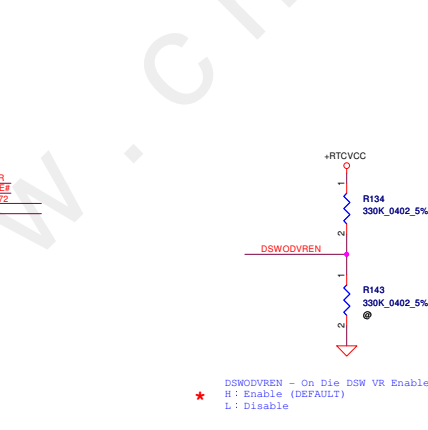
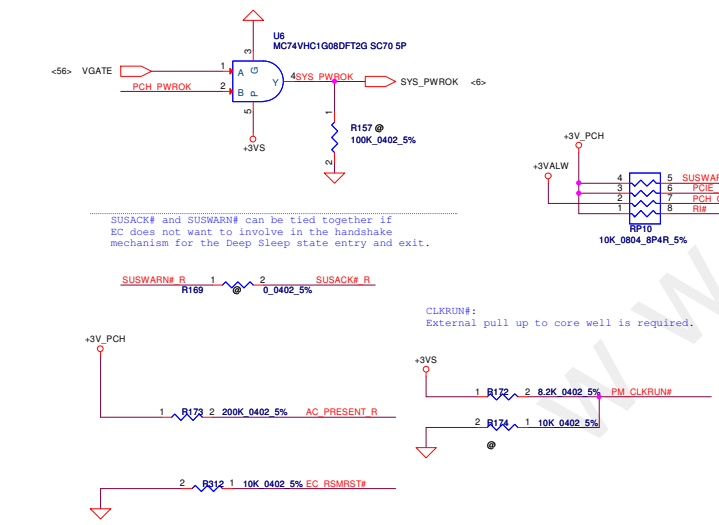
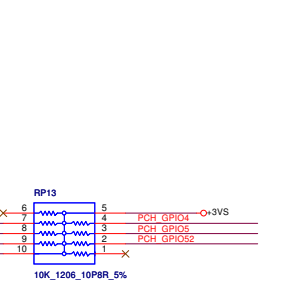
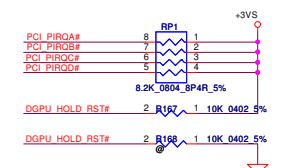
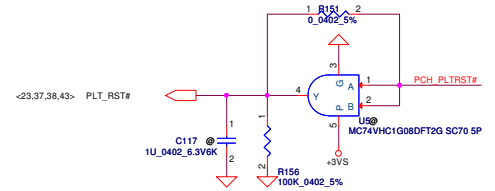
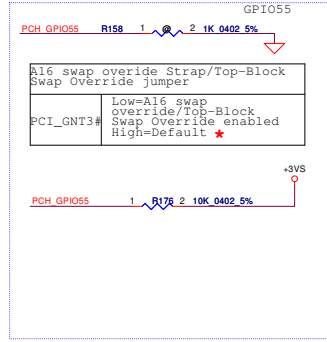


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Size	Document Number	Rev	Date	
Custom	LA-9641P	0.1	Thursday, October 11, 2012	
			Sheet	14 of 60

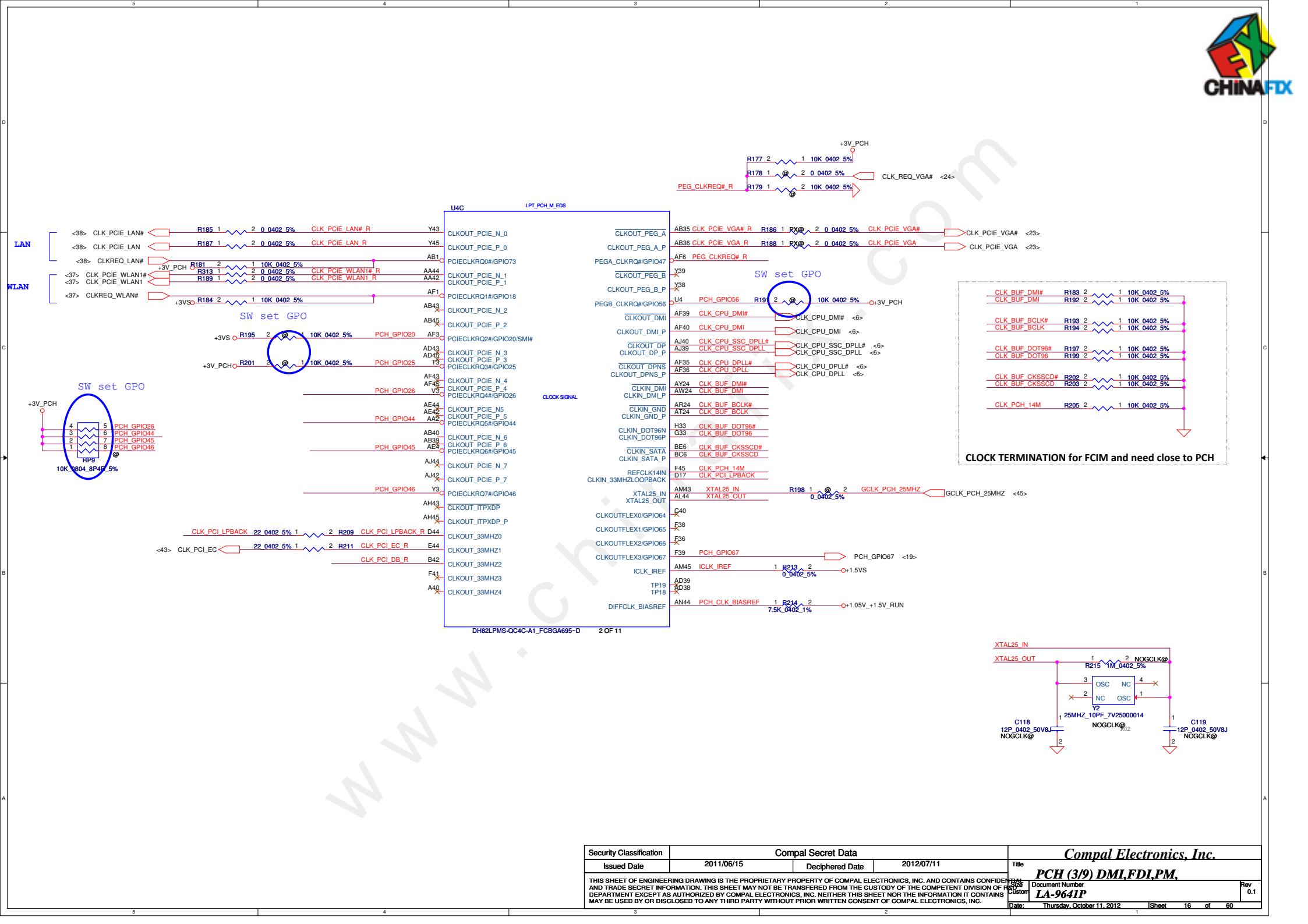


BBS_BIT1	SATA_SLPD (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	* SPI

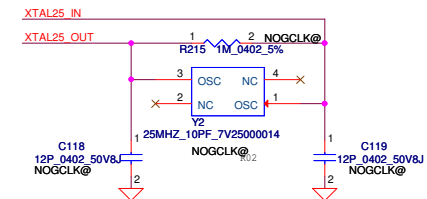
**GPIO51 has internal pull up.**





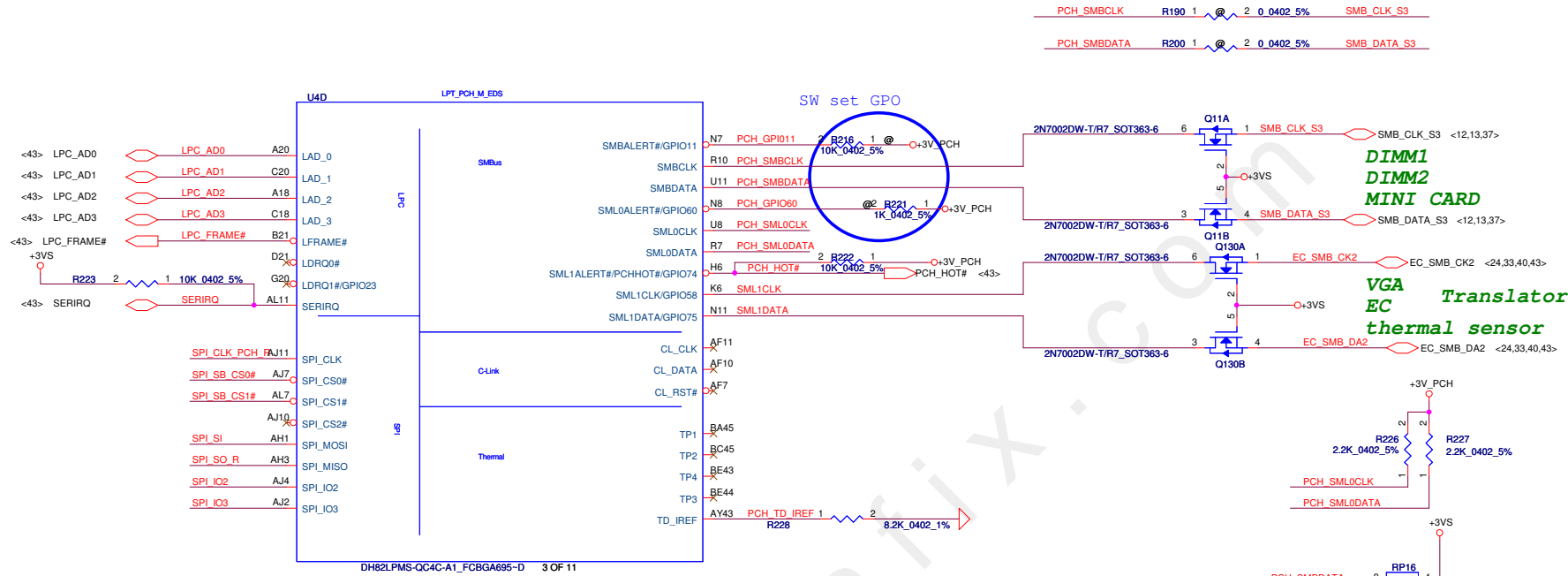


**CLOCK TERMINATION for FCIM and need close to PCH**

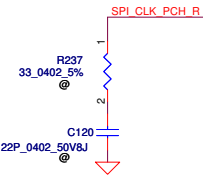
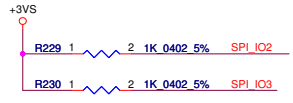


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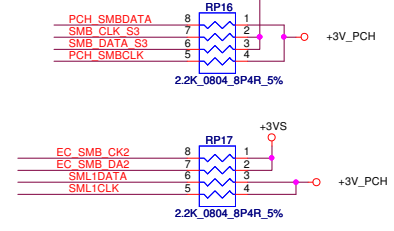
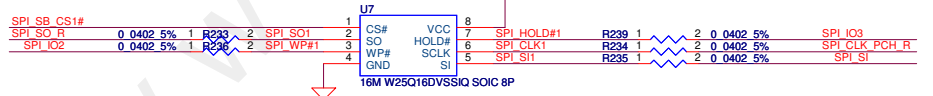
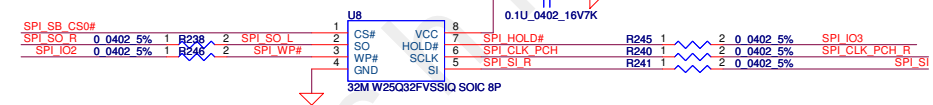




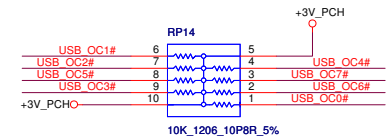
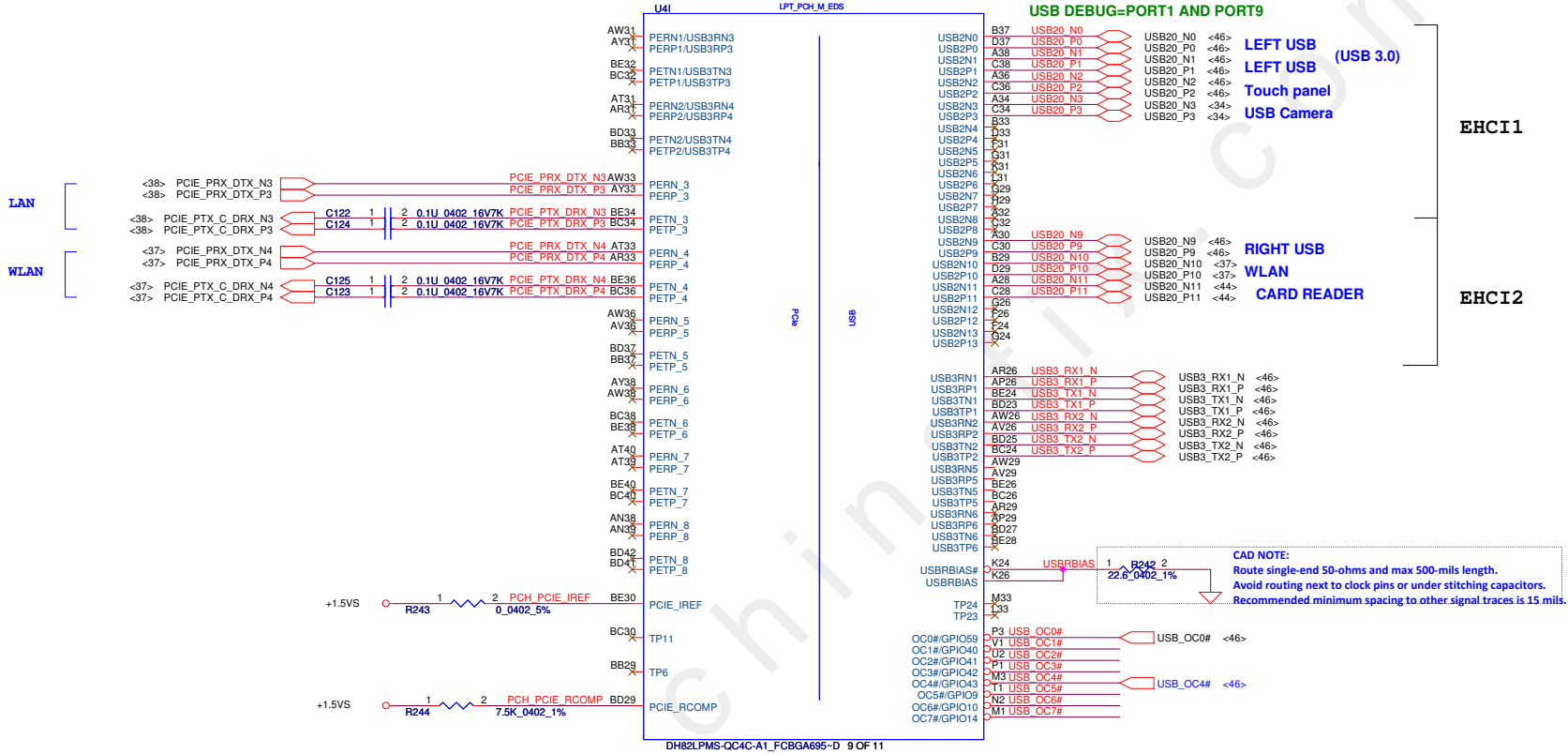
**8MB SPI ROM FOR ME & Non-share ROM.**



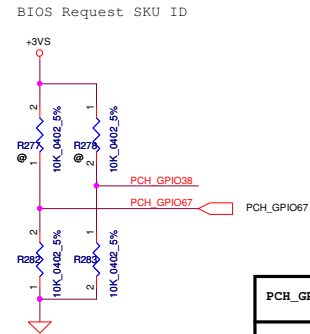
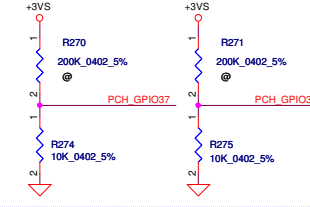
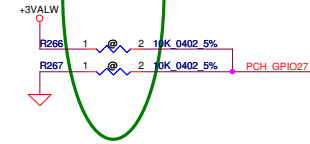
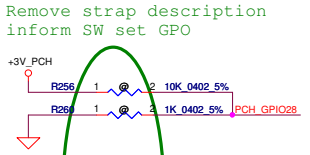
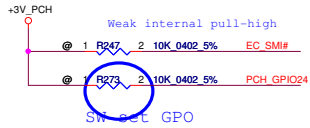
R124;c190 close to U4.T3 pin



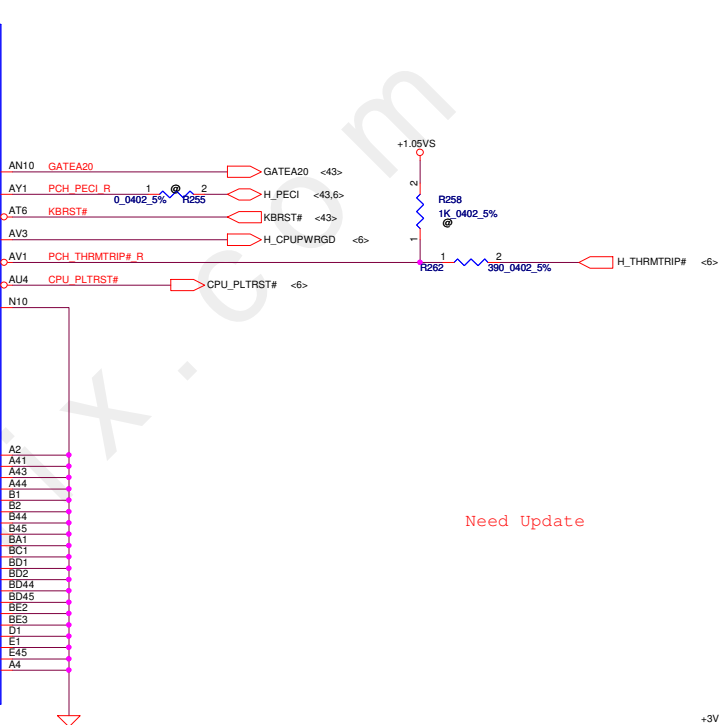
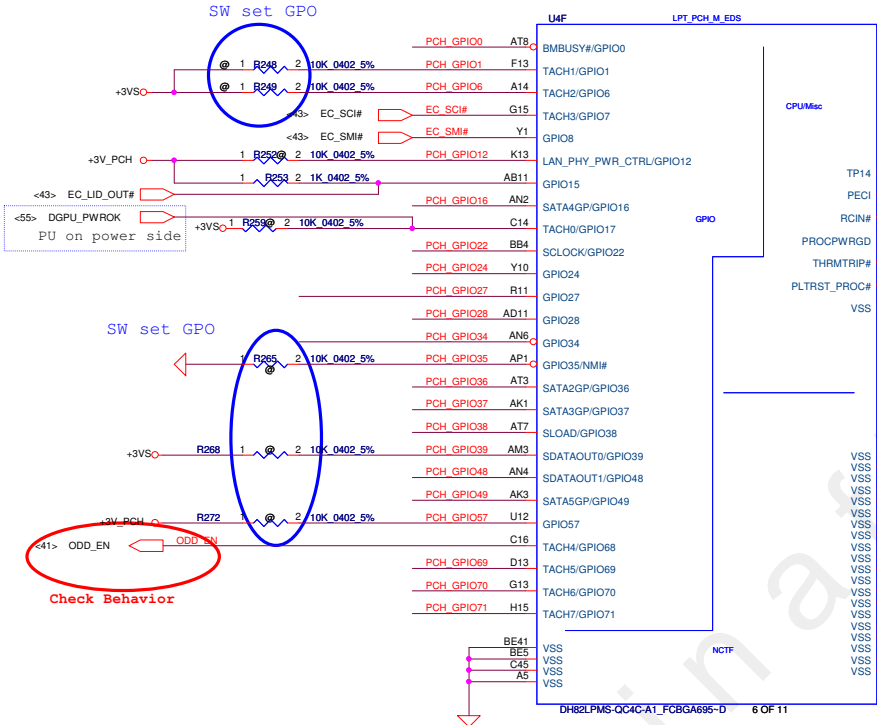
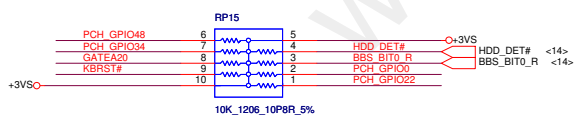
Security Classification		Compal Secret Data		Title	
Issued Date		2011/06/15		PCH (4/9) LVDS,CRT,DP,HDMI	
		Deciphered Date		2012/07/11	
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Issued Date	2011/06/15	Deciphered Date	2012/07/11	PCH (5/9) PCI, USB	
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PCH_GPIO38	PCH_GPIO67	Function
0	0	MUXLESS
0	1	Reserved
1	0	UMA
1	1	DIS



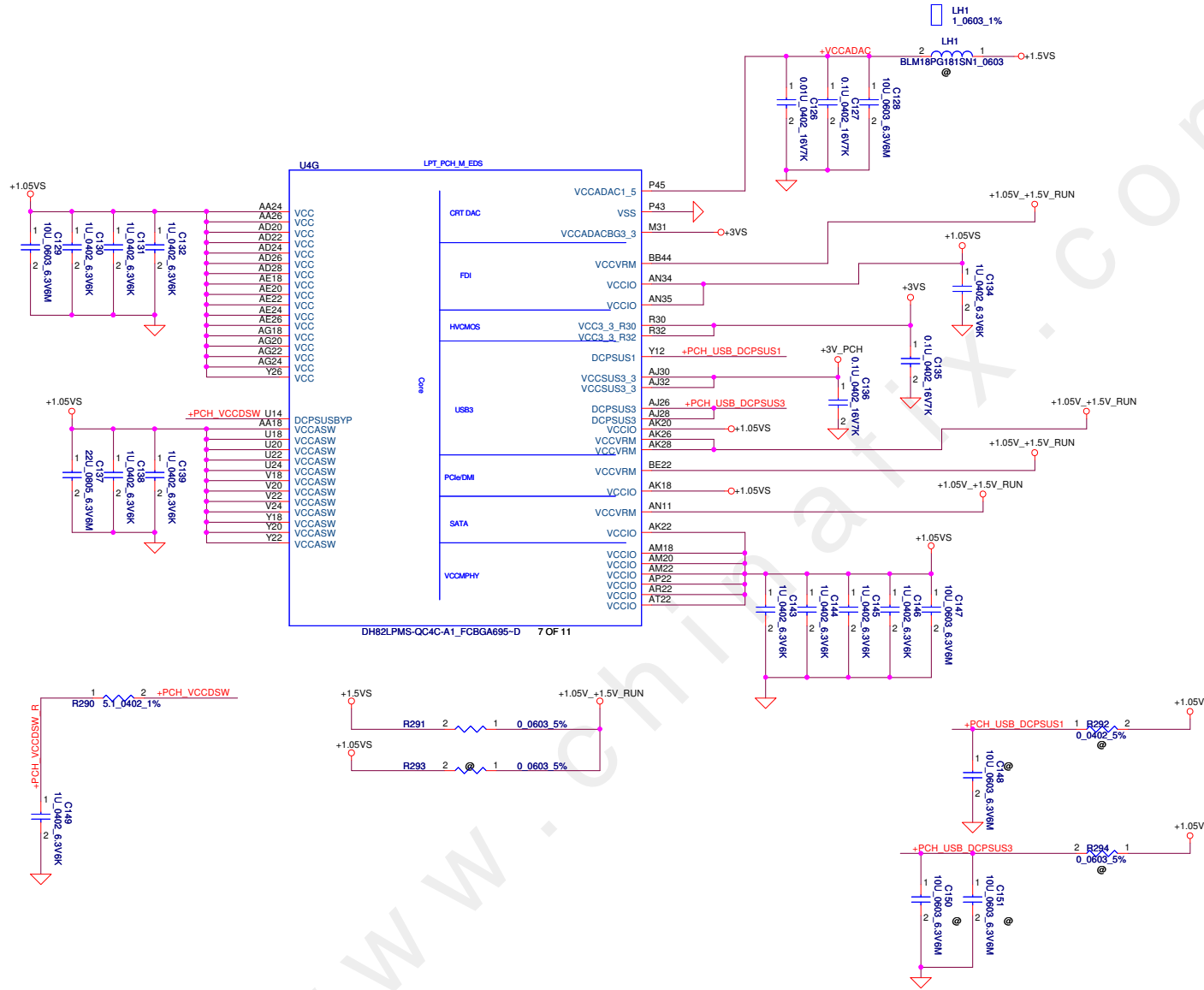
Need Update

Config	GPIO16 & 49
USB3.0 x4, PCIE x8, SATA x6	11
USB3.0 x6, PCIE x8, SATA x4	01

Fixed Signals				Muxed Signals				Fixed Signals				Muxed Signals				Fixed Signals									
USB3_1	USB3_2	USB3_5	USB3_6	PCIE_1	PCIE_2	PCIE_3	PCIE_4	PCIE_5	PCIE_6	PCIE_7	PCIE_8	SATA_1	SATA_2	SATA_3	SATA_4	SATA_5	SATA_6	PCIE_1	PCIE_2	SATA_1	SATA_2	SATA_3	SATA_4	SATA_5	SATA_6
(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(00)	(01)	(01)	(01)	(01)	(01)	(01)	(01)	(01)

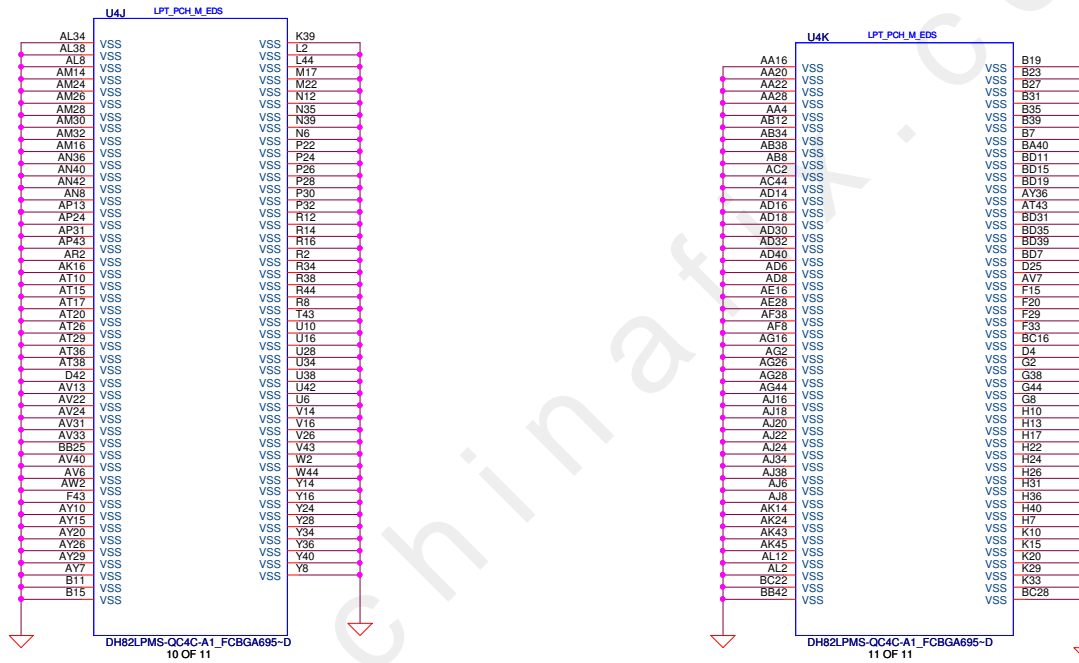
PCH_GPIO69	Function
0	
1	

PCH_GPIO70	Function
0	
1	
PCH_GPIO71	
0	SUN PRO
1	Mars XT

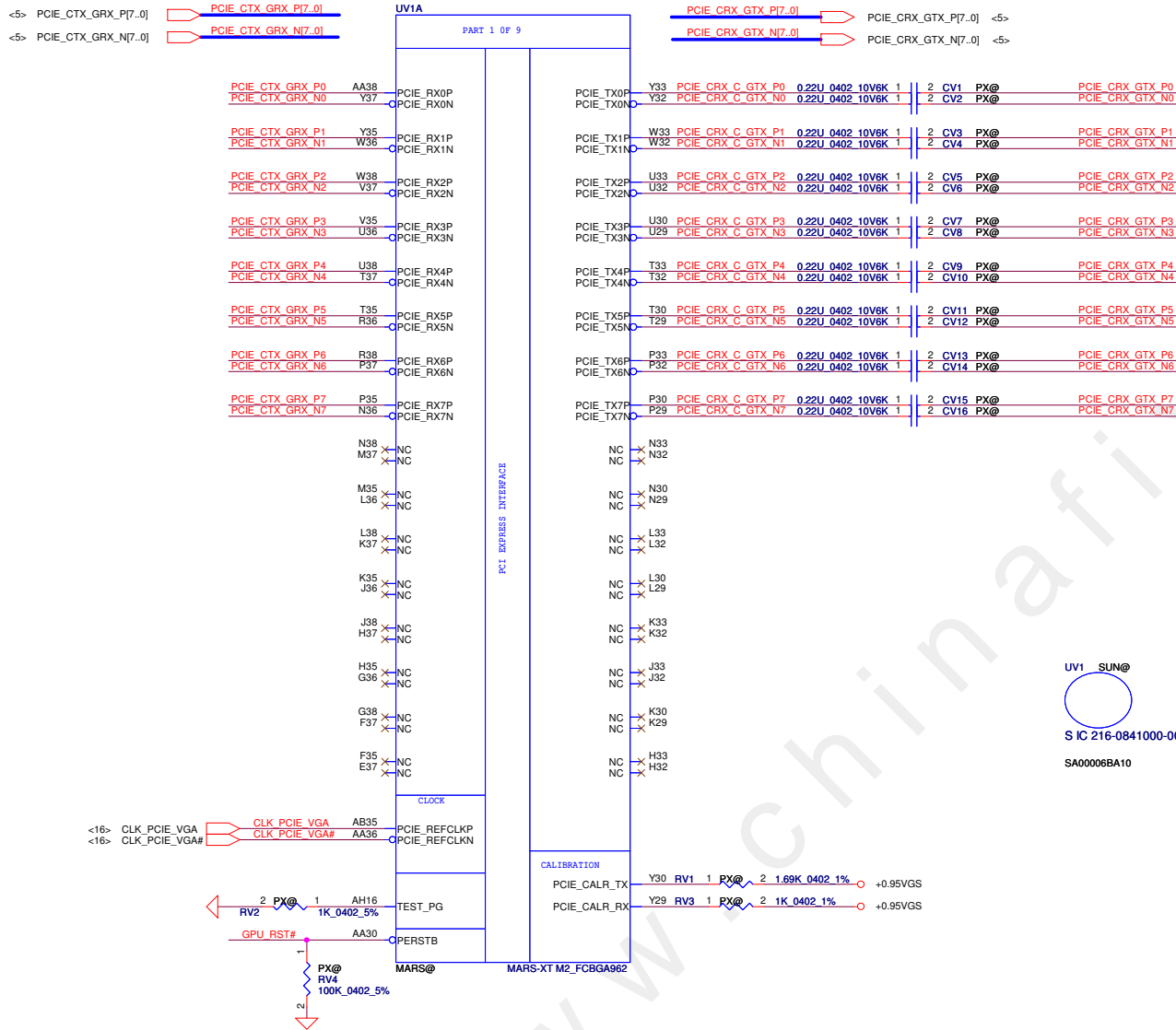


PCH Power Rail Table		
Voltage Rail	Voltage	50 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCDAC1_5	1.5V	0.070 A
VCCDAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCDSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A

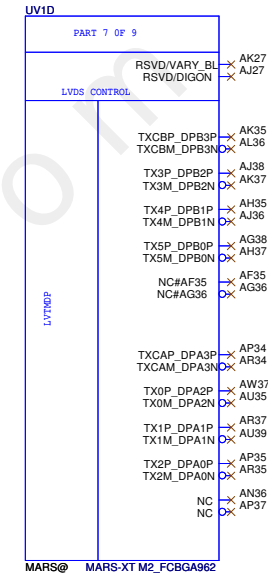




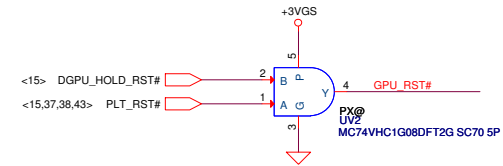
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### LVDS Interface



UV1 SUN@  
  
 S IC 216-0841000-00 A0 SUN PRO M2 FCBGA 962P C38  
 SA00006BA10



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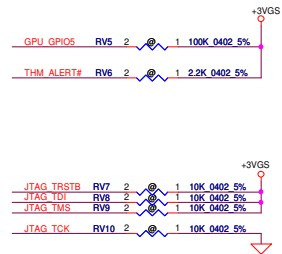
### CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS  
 0= DO NOT INSTALL RESISTOR  
 1= INSTALL 10K RESISTOR  
 X= DESIGN DEPENDANT  
 NA= NOT APPLICABLE

STRAPS	MLPS	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRNS_ENB	PS_1[4]	Transmitter Power Savings Enable 0:50% Tx output swing 1:Full Tx output swing	1
TX_DEEMPH_EN	PS_1[5]	PCIe Transmitter De-emphasis Enable 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	0
BIF_GEN3_EN_A	PS_1[1]	PCIe Gen3 Enable (NOTE:RESERVED for Thames/Seymour and should be strapped to 0) 0:GEN3 not support at power-on 1:GEN3 supported at power-on	1
BIF_VGA_DIS	PS_2[4]	VGA control 0:VGA controller capacity enabled 1:VGA controller capacity disabled (for multi-GPU)	0
ROMIDCFQ[2:0]	PS_0[3..1]	Serial ROM type or Memory Aperture Size Select If PS_2[3]=0, defines memory aperture size If PS_2[3]=1, defines ROM type 100- 512Kbit M2SP05A (ST) 101- 1Mbit M2SP10A (ST) 101- 2Mbit M2SP20 (ST) 101- 4Mbit M2SP40 (ST) 101- 8Mbit M2SP80 (ST) 100- 512Kbit Pm2SLV010 (Chingis) 101- 1Mbit Pm2SLV010 (Chingis)	000
BIOS_ROM_EN	PS_2[3]	Enable external BIOS ROM device 0:Disabled 1:Enabled	0
AUD[1]	NA	00- No audio function 01- Audio for DP only 10- Audio for DP and HDMI if dongle is detected 11- Audio for both DP and HDMI	XX
AUD[0]	NA	HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	
CEC_DIS	PS_0[4]	Reserved for future ASIC	1
RESERVED	PS_1[3]	Reserved	0
RESERVED	PS_1[2]	Reserved	0
RESERVED	NA	Reserved	0
RESERVED	NA	Reserved (for Thames/Whistler/Seymour only)	0
AUD_PORT_CONN_PINSTRAP[2]	PS_3[5]	STRAPS TO INDICATE THE NUMBER OF AUDIO CAPABLE DISPLAY OUTPUTS 111 = 0 usable endpoints 110 = 1 usable endpoints 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	XXX
AUD_PORT_CONN_PINSTRAP[1]	PS_3[4]		
AUD_PORT_CONN_PINSTRAP[0]	PS_3[5]		

### STRAPS



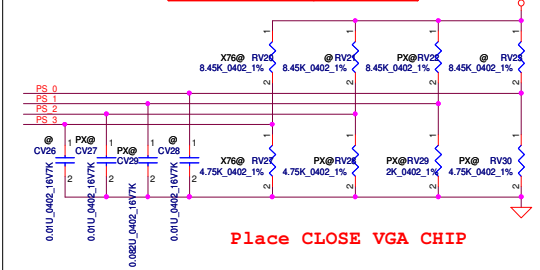
AVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

VDD1DI	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

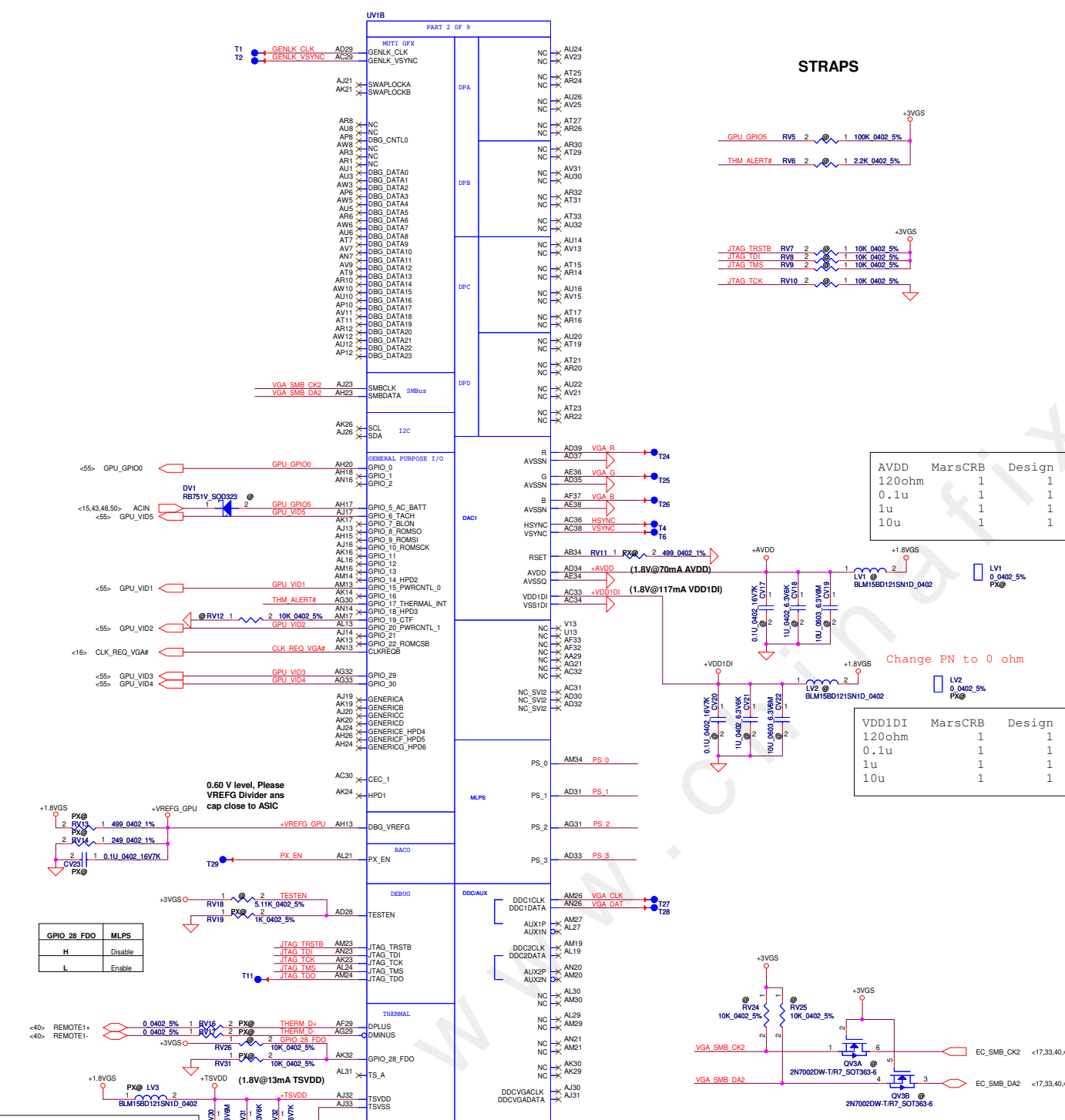
### MLPS Strap

Bits[5:1]	Bits[3:1]	Capacitor	R_pu	R_pd
PS_0[5:1]	1 1 000	NC	NC	4.75K
PS_1[5:1]	01 0 0 1	82 nF	8.45K	2K
PS_2[5:1]	10 0 0 0 0	10 nF	NC	4.75K
PS_3[5:1]	1 1	X X X	X	X

Mapping to VRAM type please refer to page 4



Place CLOSE VGA CHIP



GPIO 28 FDO	MLPS
H	Disable
L	Enable

TSVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

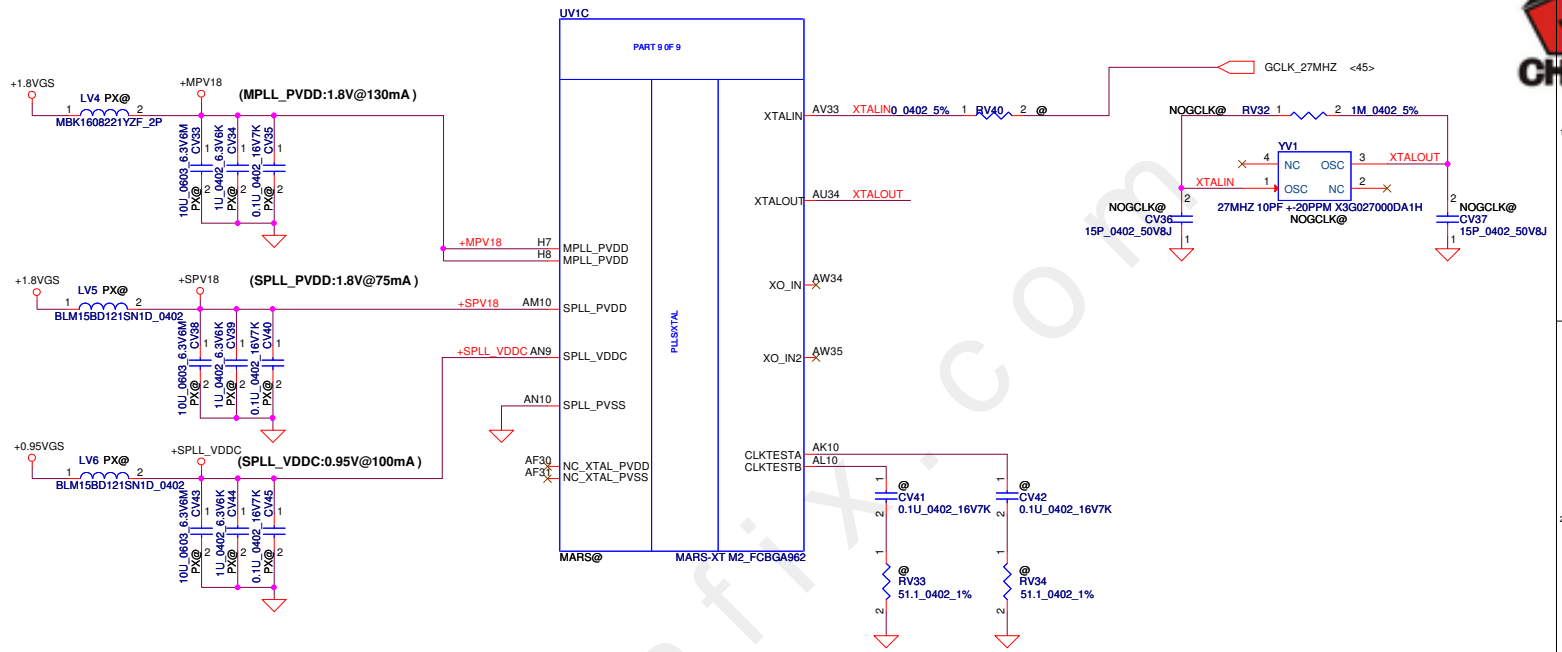




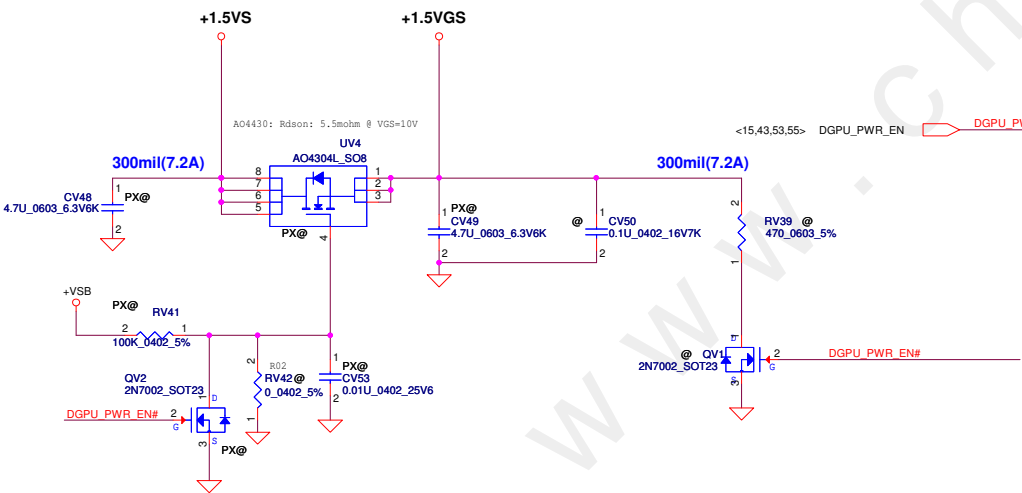
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

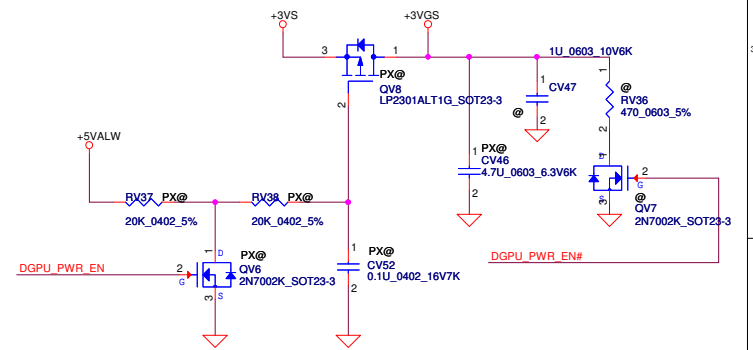
SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



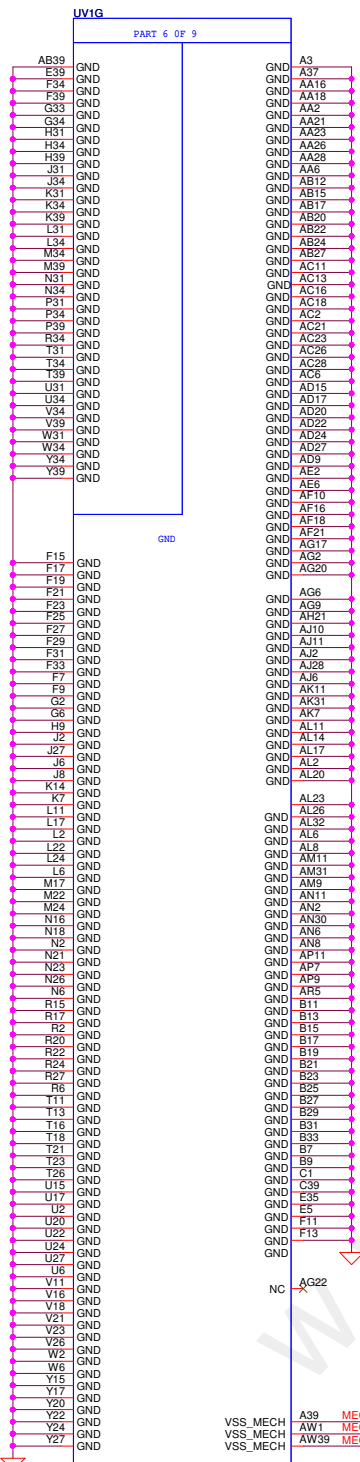
**+1.5VS to +1.5VGS Transfer**



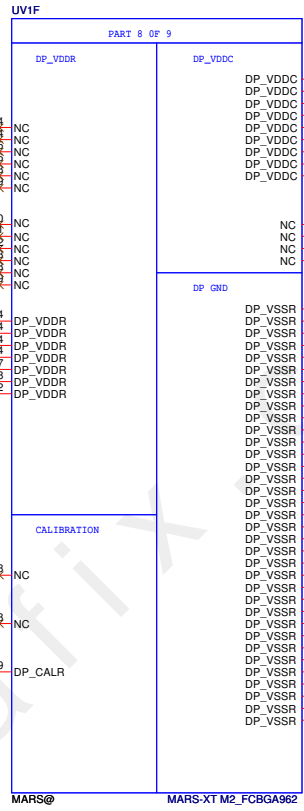
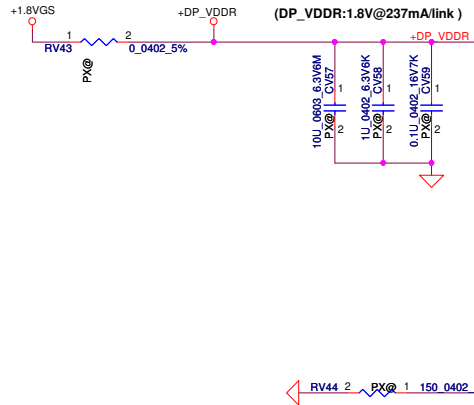
**<+3VS TO +3VGS> Need OPEN**



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Date: Thursday, October 11, 2012						Sheet 25 of 60



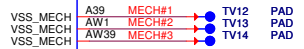
DP_VDDR	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1



DP_VDDC	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1

(DP\_VDDC:0.95V@280mA/link)

+0.95VGS

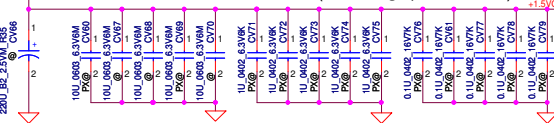


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Date:	Thursday, October 11, 2012	Sheet	26	Rev 0.1				



**For GDDR5, MVDDQ = 1.5V**

(VDDR1:1.5V@3A,GDDR5:1125MHz)

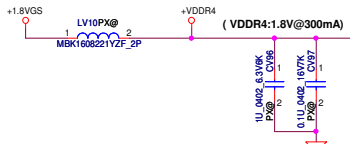
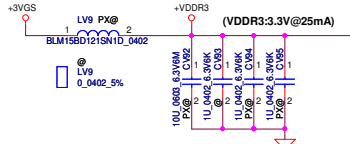
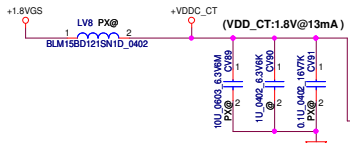


VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1

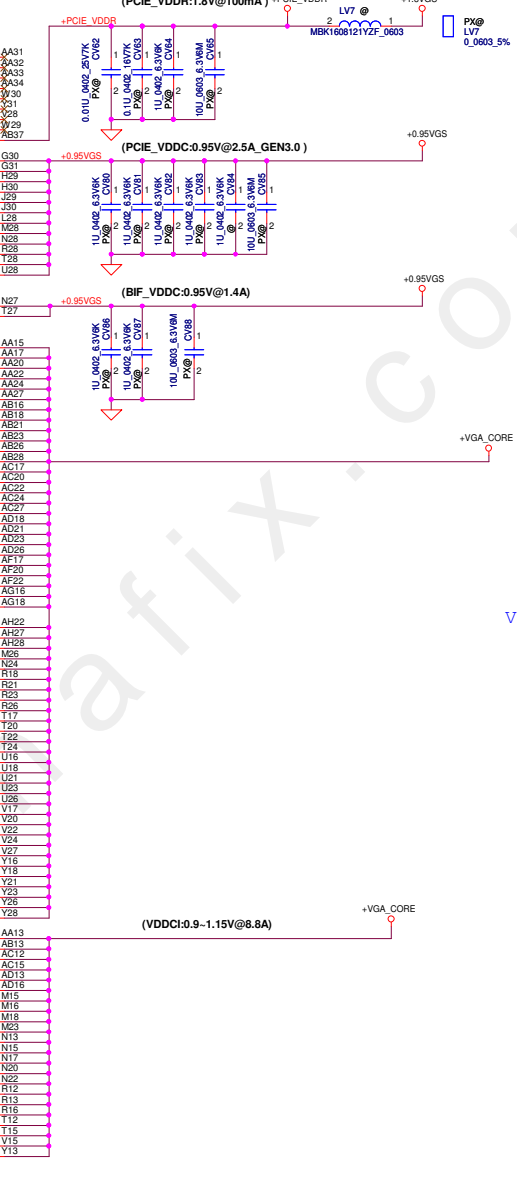
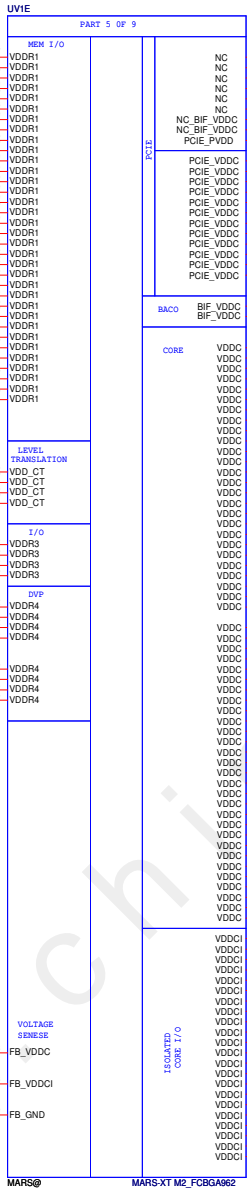
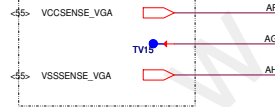
VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1

VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1

VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0



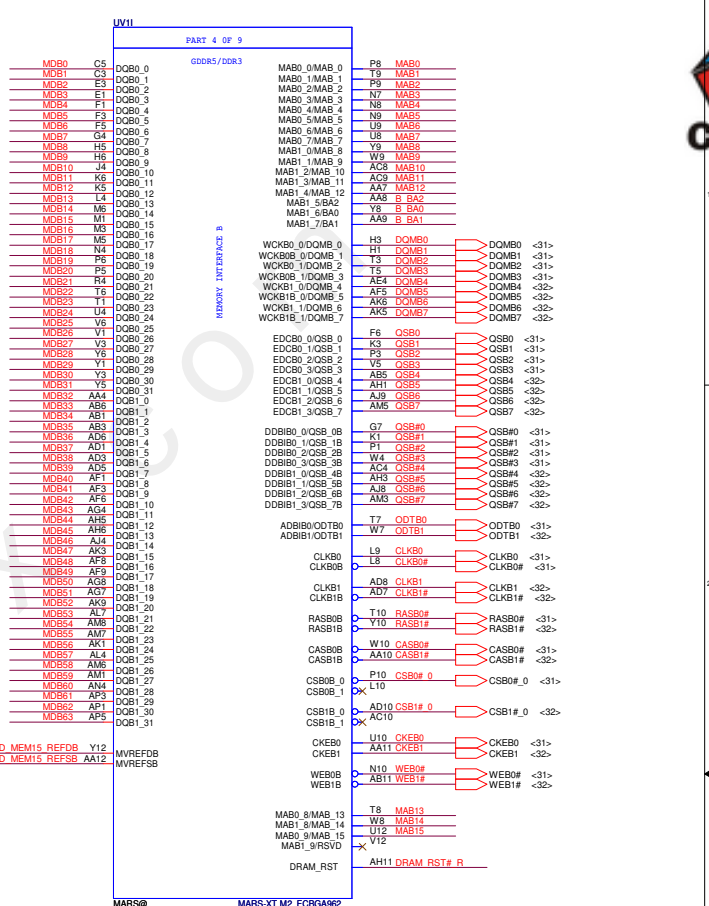
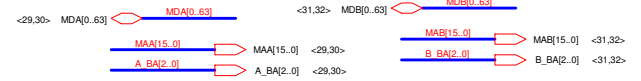
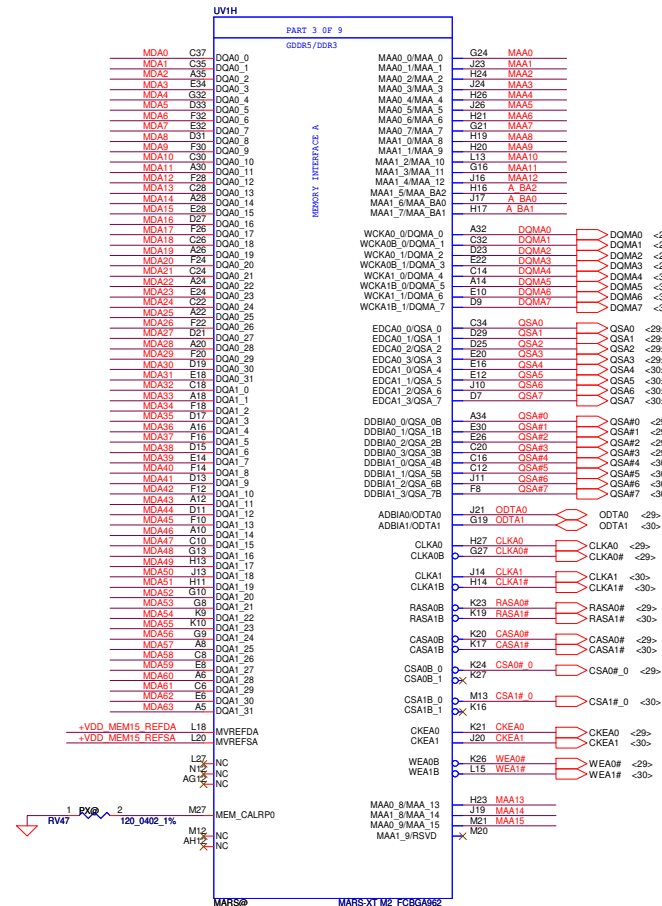
Route as differential pair



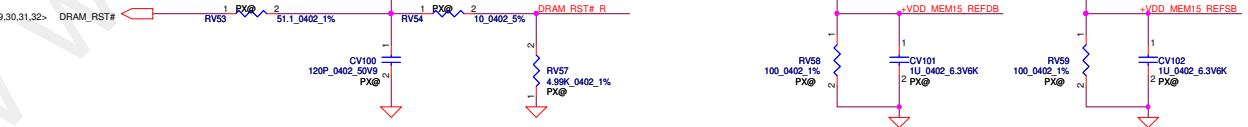
PCIE_VDDR	MarsCRB	Design
0.1u	0	2
1u	2	3
10u	1	1

PCIE_VDDC	MarsCRB	Design
1u	7	5
10u	2	1

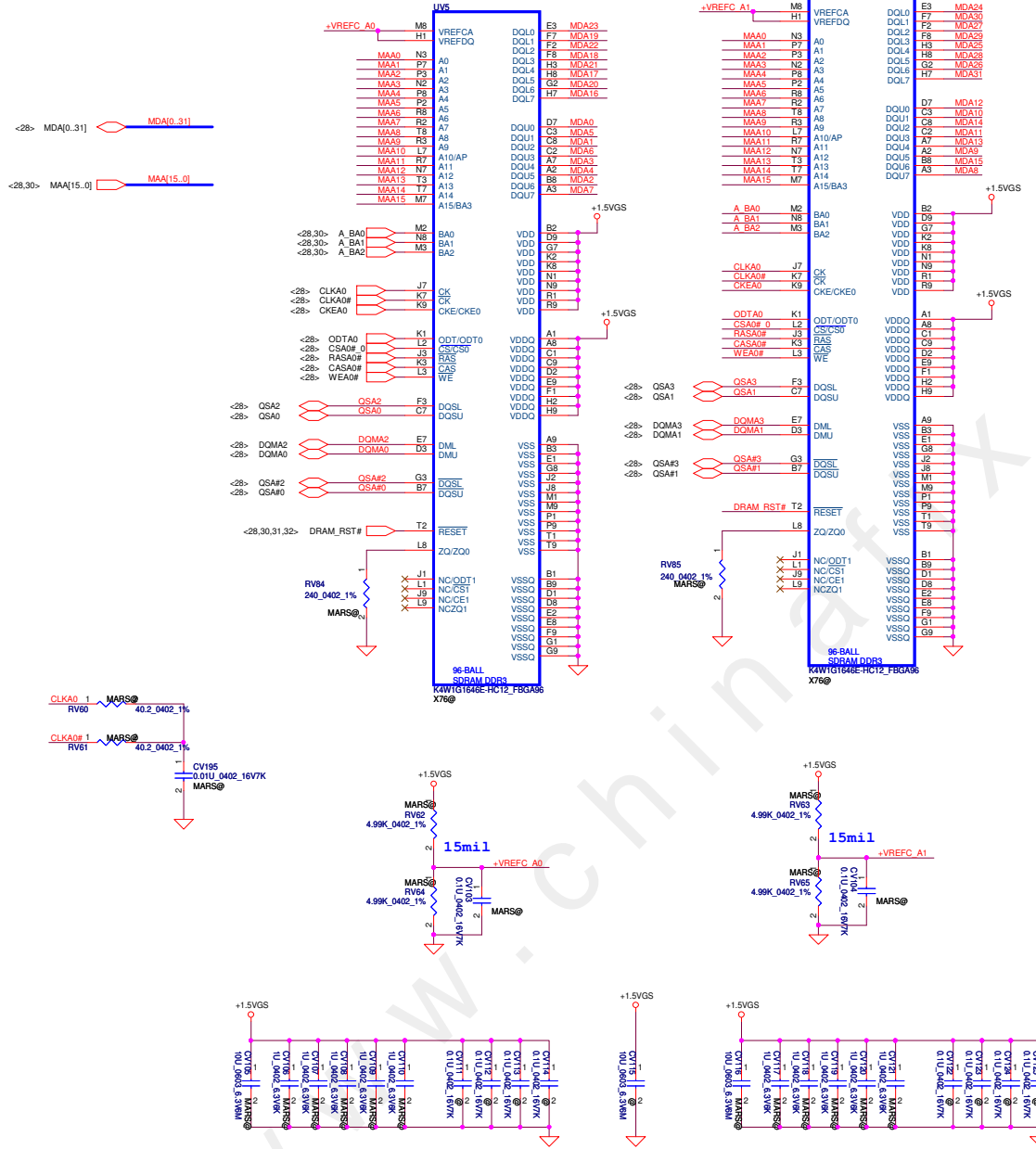
VGA\_CORE Cap in power side sheet

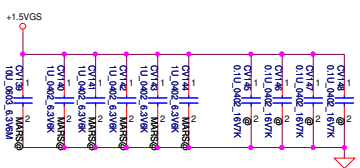
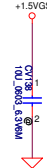
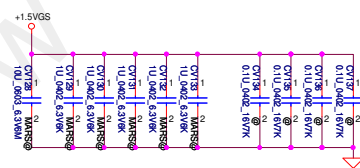
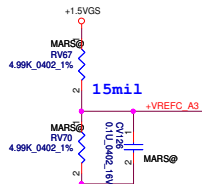
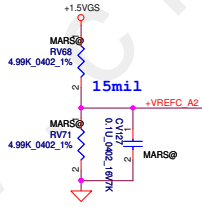
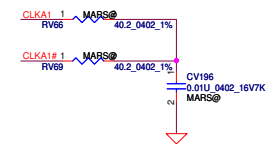
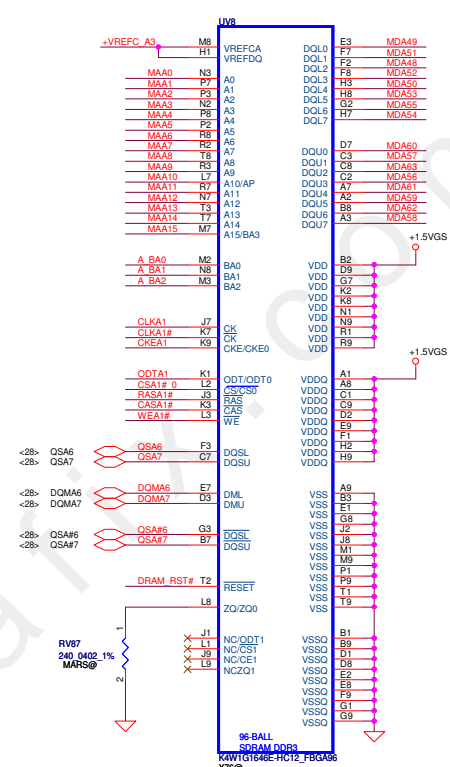
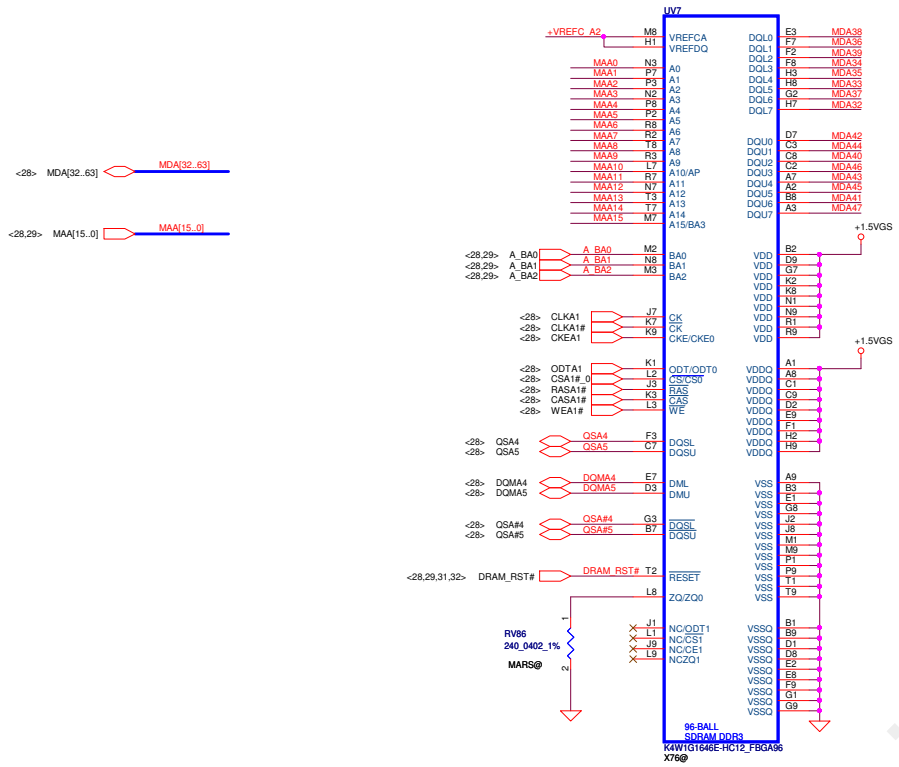


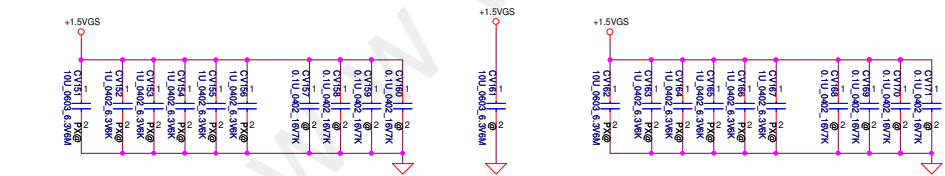
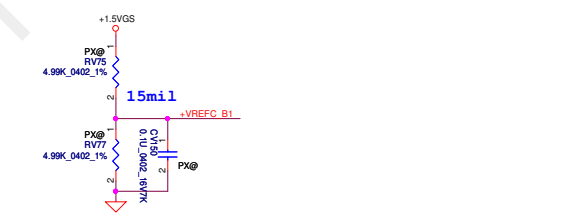
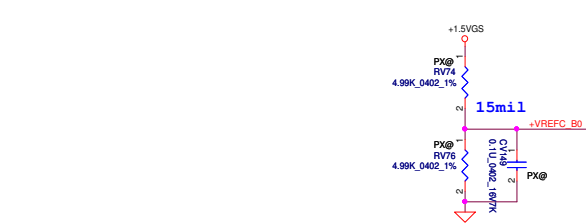
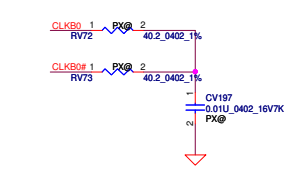
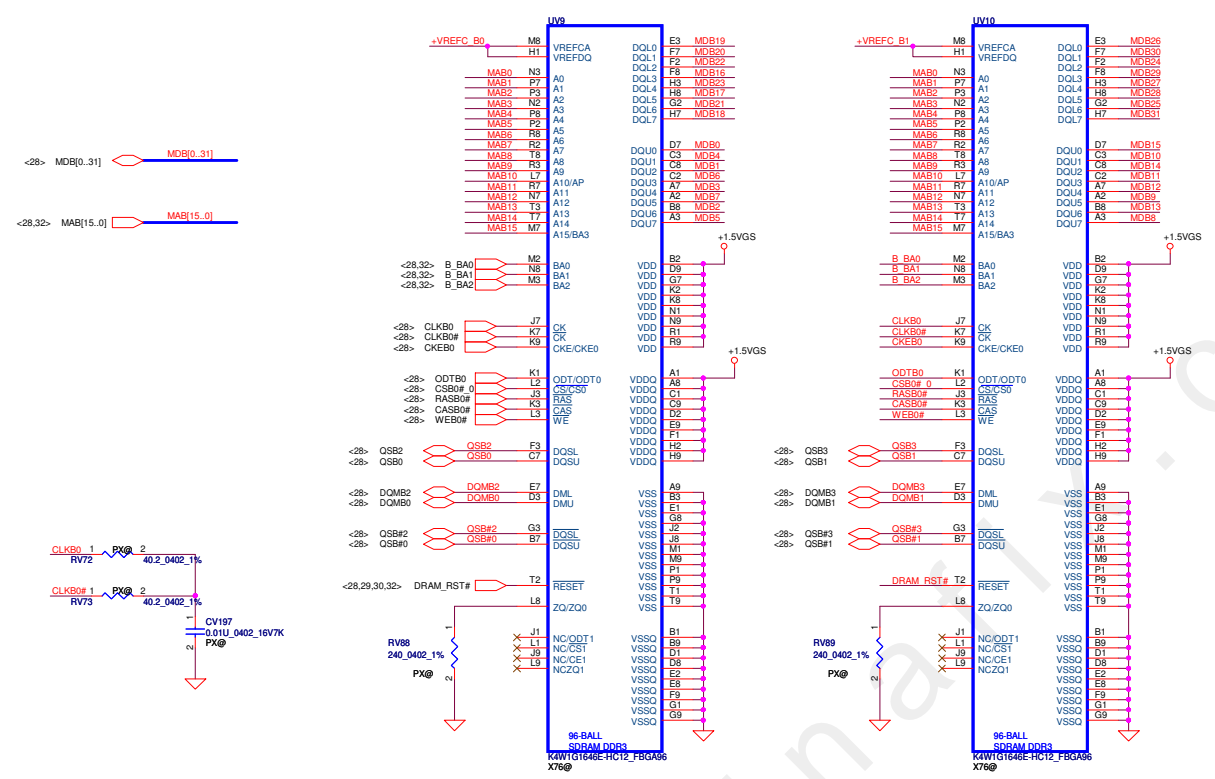
Ball to RV57 < 1"  
 CV100 to RV57 < 200 mil  
 CV100 to RV53 < 1"

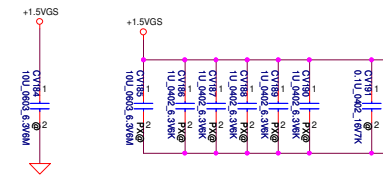
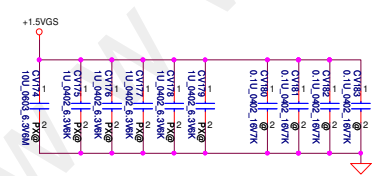
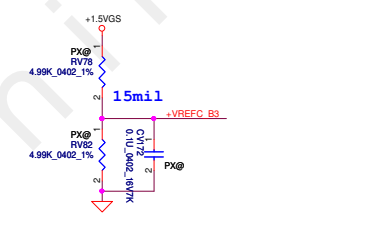
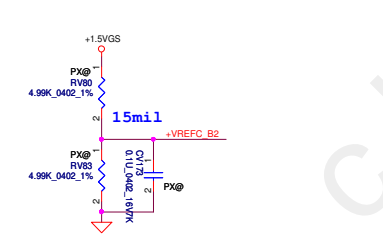
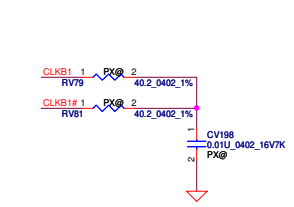
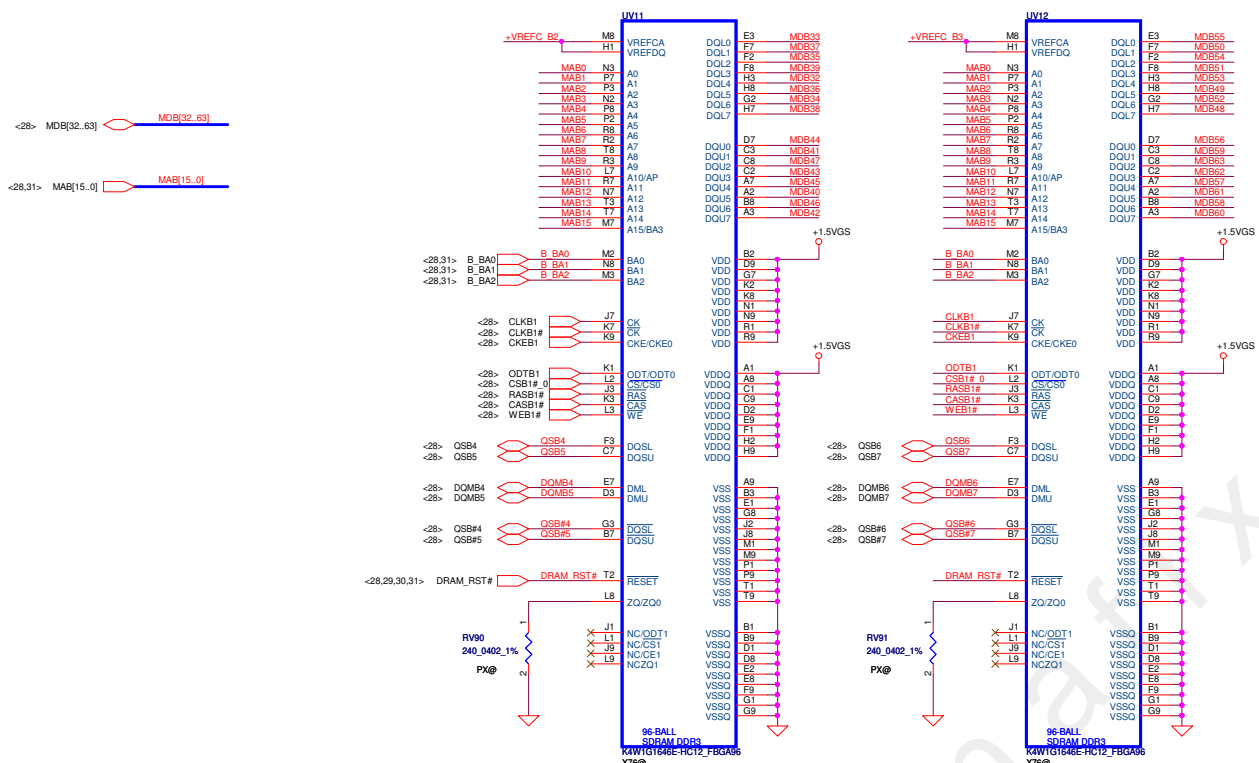


**DRAM\_RST# is a daisy-chain net that connects to all VRAM**  
 This basic topology should be used for DRAM\_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and | Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM Load and board to pass Reset Signal Spec.  
 Place all these components very close to GPU (Within 25mm) and keep all component close to each other (within 5mm) except Rsr2



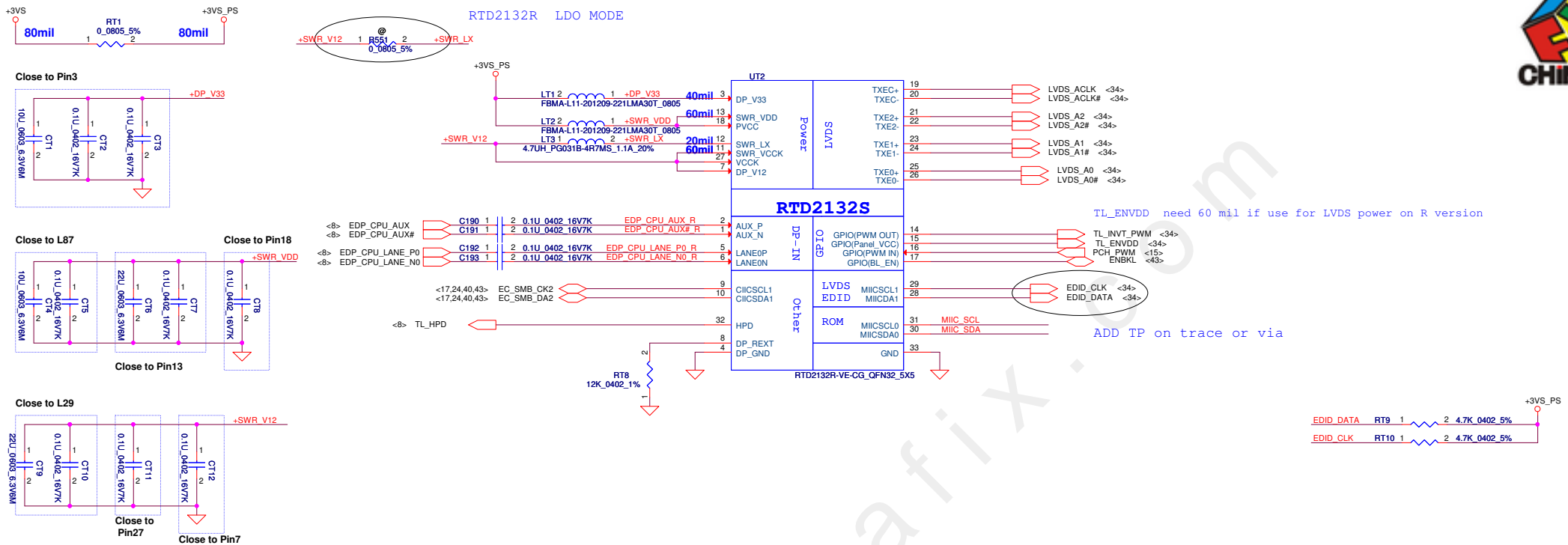






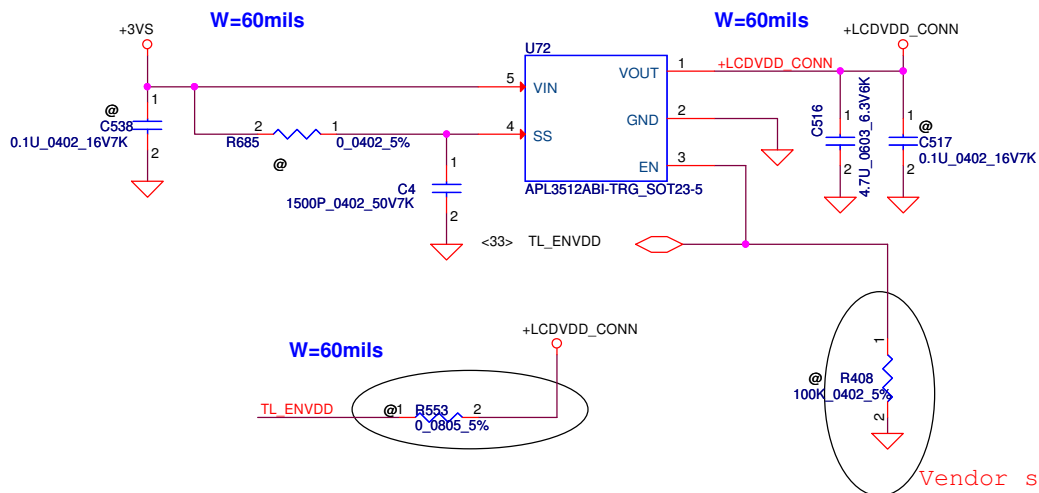
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Size	C	Document Number	QIY2 LA6884P	Rev
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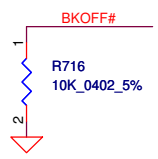


	MIIC_SDA	0	1
MIIC_SCL		X	EC CODE
		1	Internal ROM
			EEPROM

# LCD POWER CIRCUIT

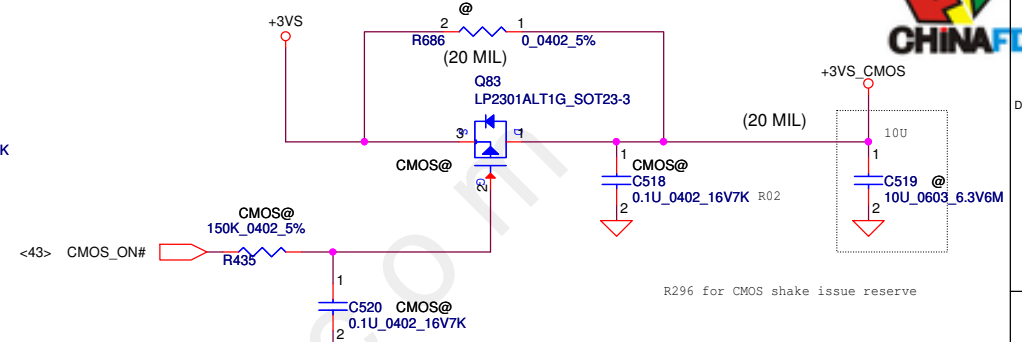


RTD2132R Internal load switch for +LCD\_VCC



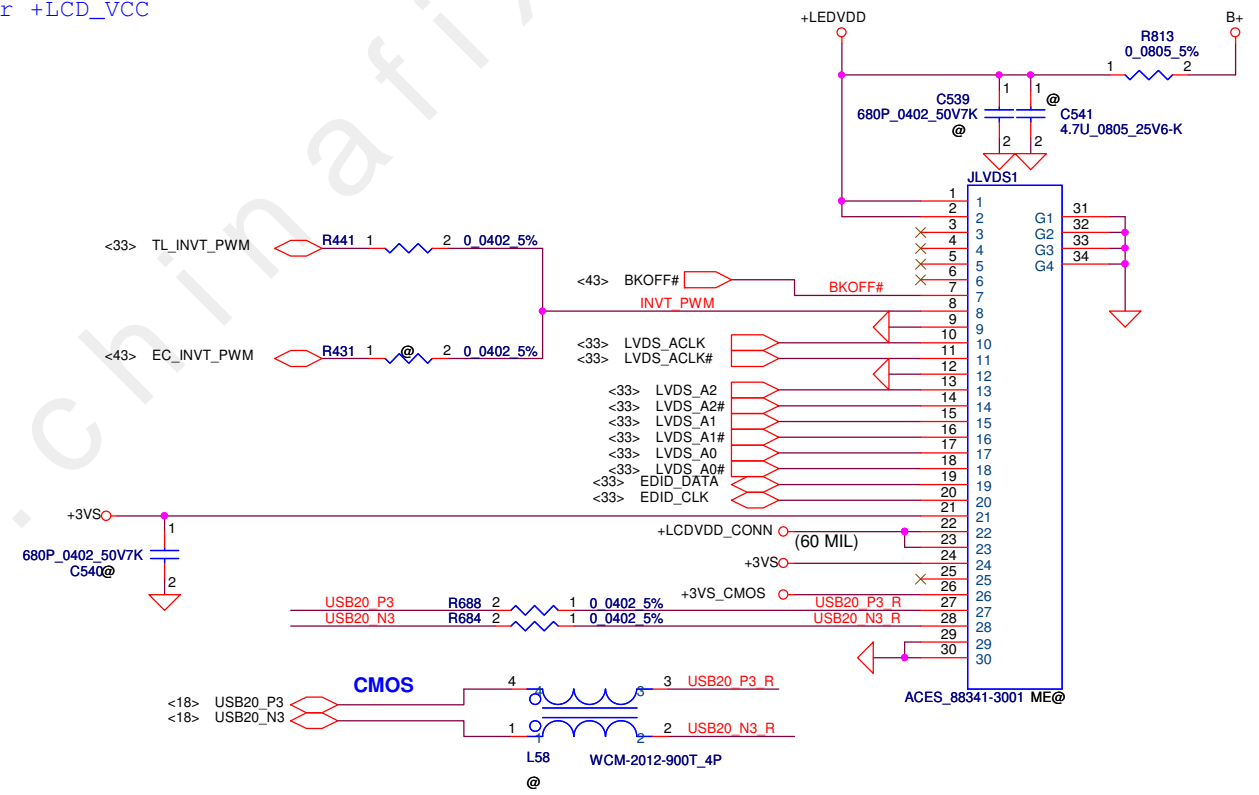
Vendor suggest reserve

# CMOS Camera



R296 for CMOS shake issue reserve

# VGA LCD/PANEL BD. Conn.

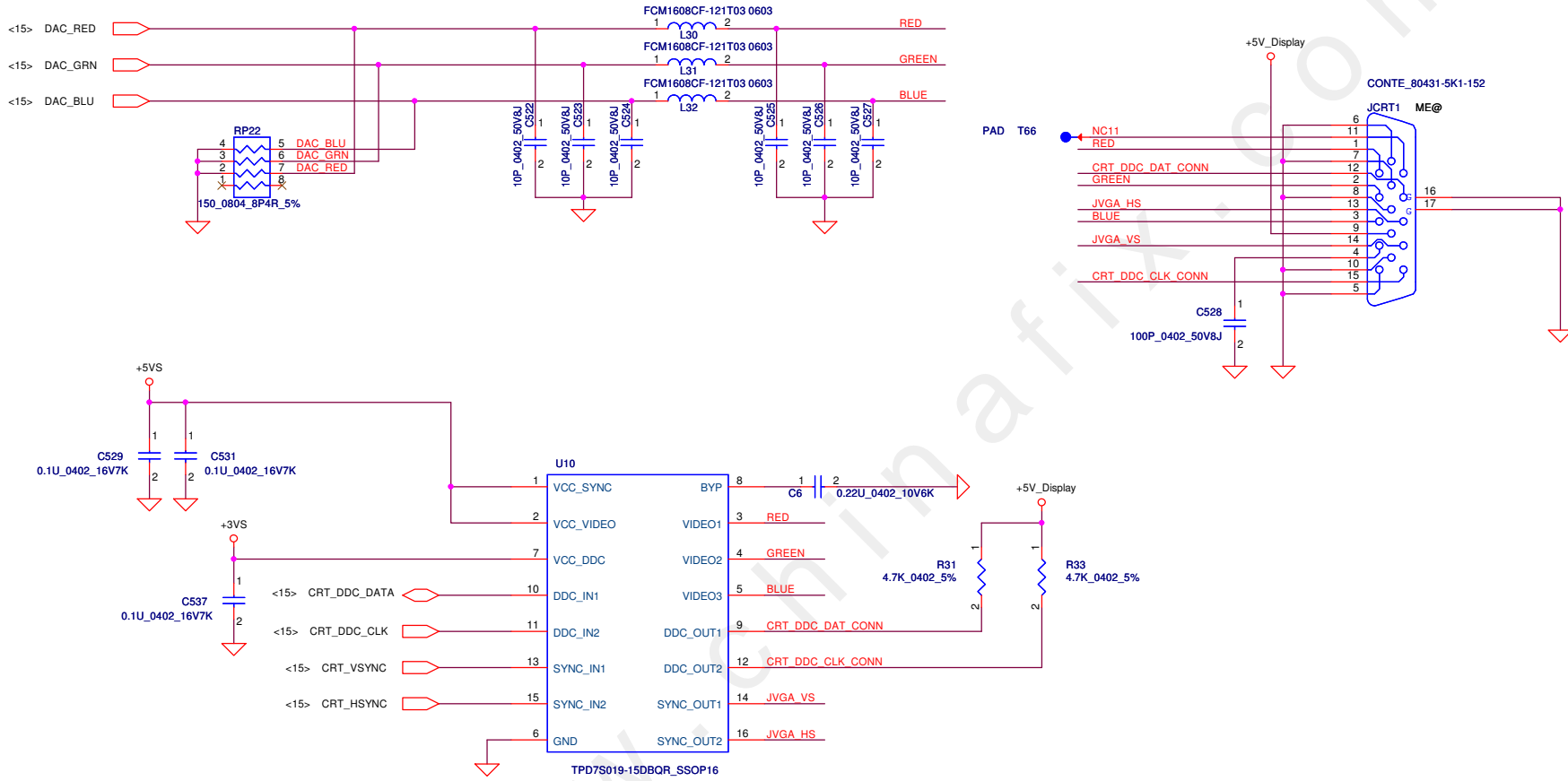


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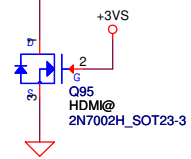
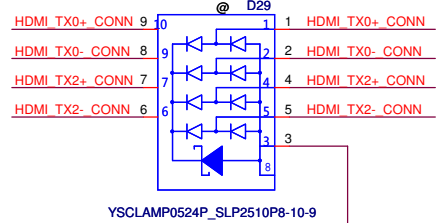
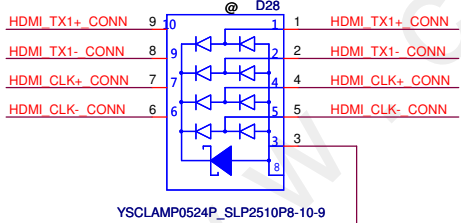
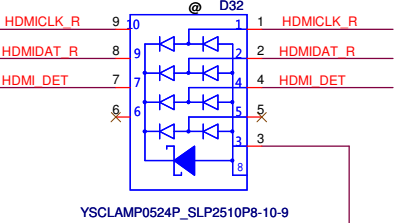
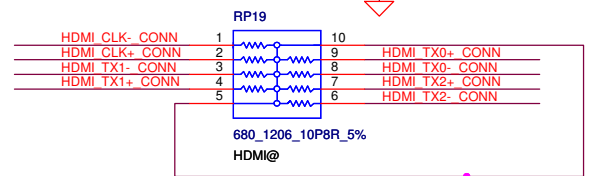
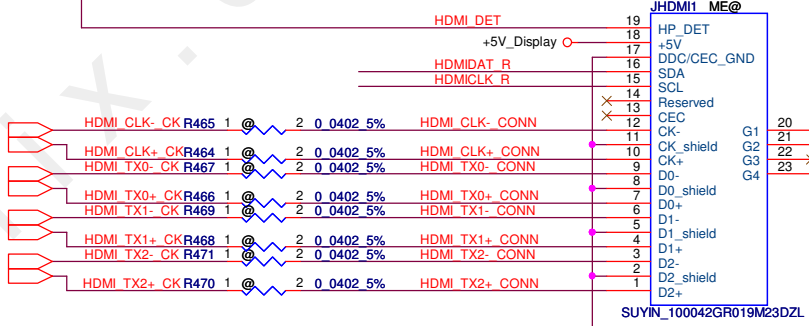
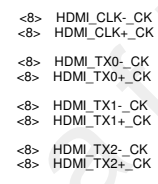
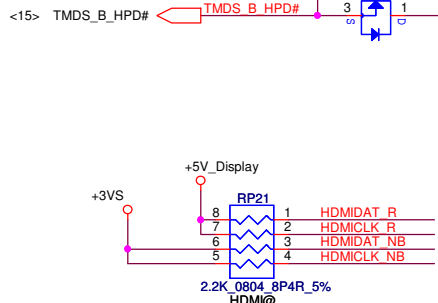
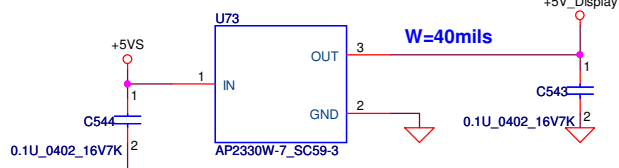
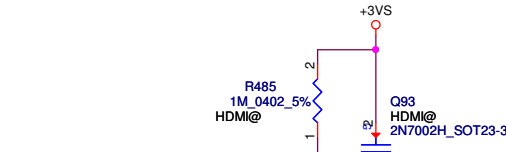
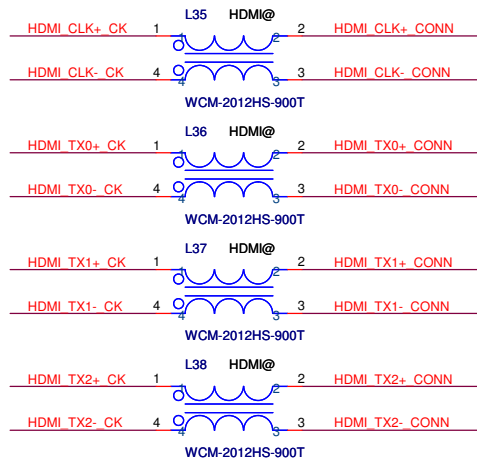
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Size		<b>LVDS/CAMERA</b>	
Document Number	Date		Rev
<b>LA-9641P</b>	Thursday, October 11, 2012	Sheet	2.0
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		60	



# CRT Connector

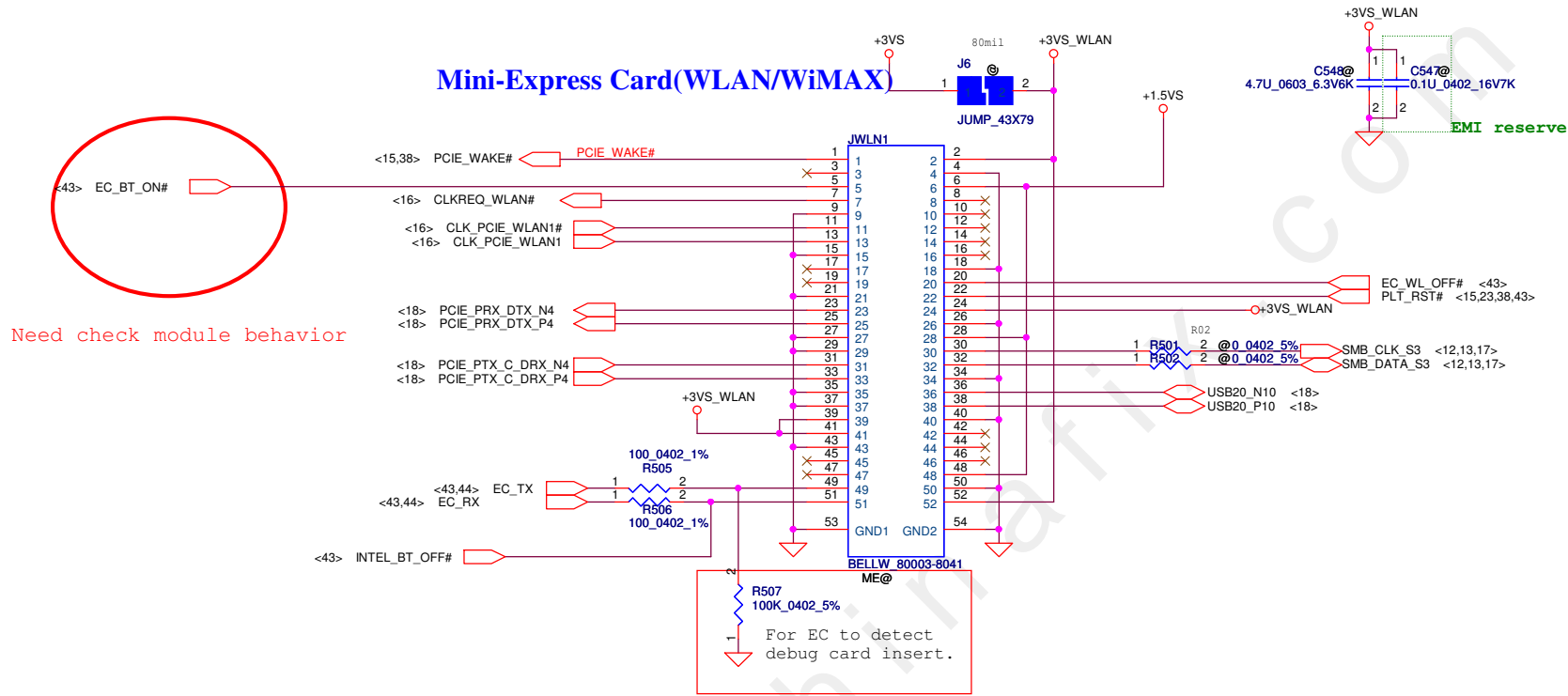


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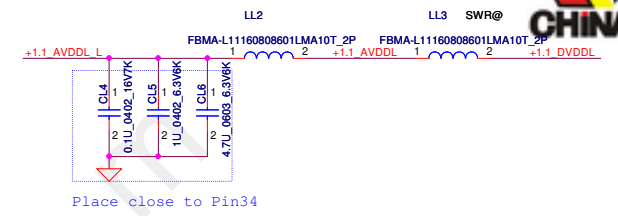
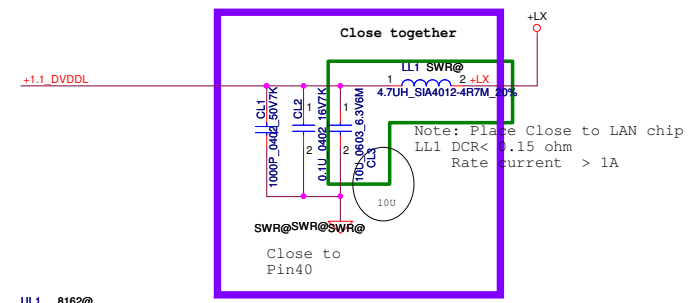
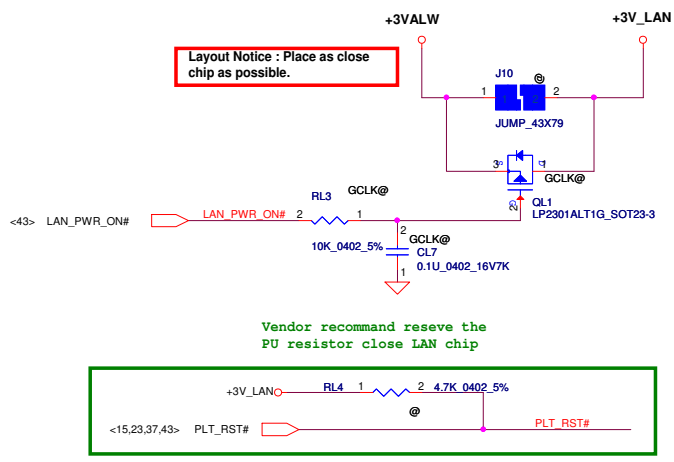


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				Document Number	LA-9641P
Date: Thursday, October 11, 2012				Sheet	36 of 60

# Mini-Express Card for WLAN/WiMAX(Half)

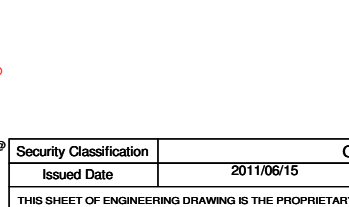
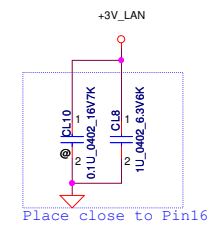
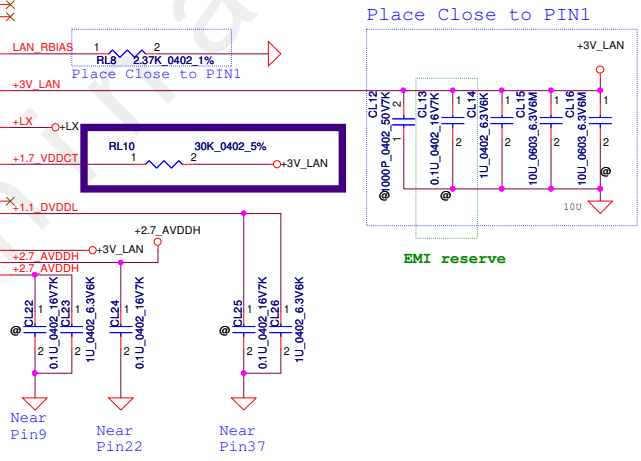
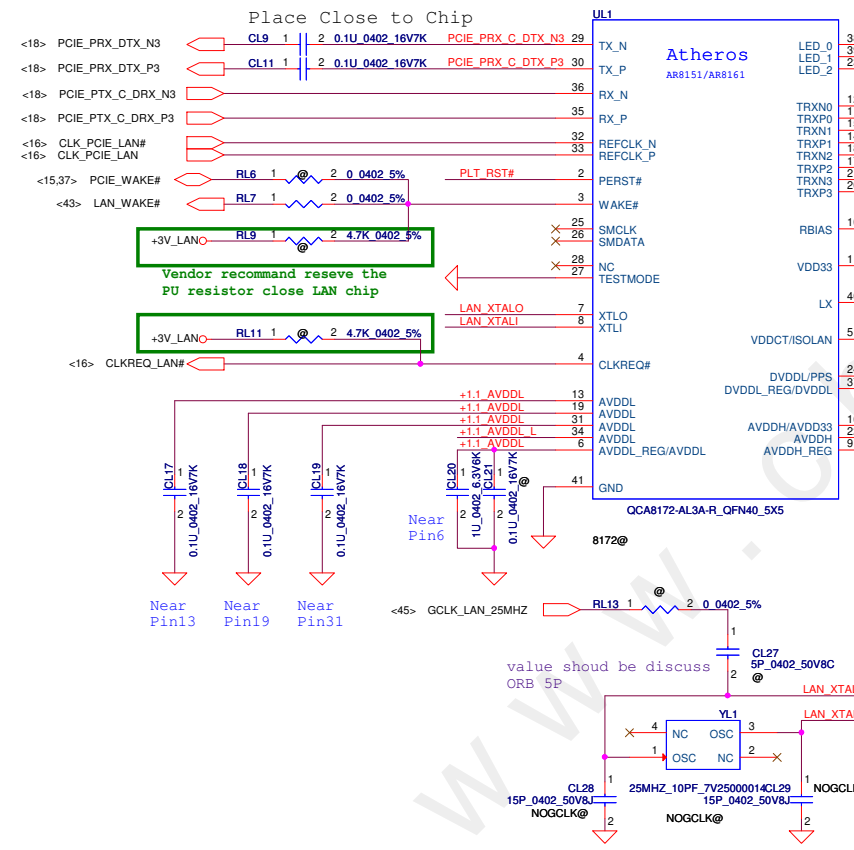


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UL1 8162@  
AR8162-AL3A-R

SA000065400 S IC QCA8172-AL3A-R QFN 40P E-LAN CTRL  
SA000052J10 S IC AR8162-AL3A-R QFN 40P E-LAN CTRL

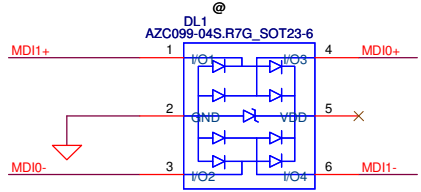


Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	LAN-AR8162/8172	
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				LA-7982P	1.0
Date:	Thursday, October 11, 2012	Sheet	38	of 60	

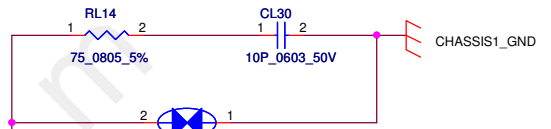
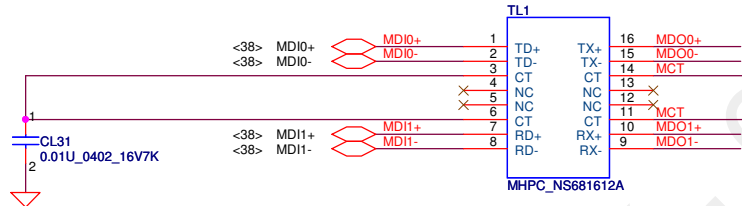


DL1  
 1'S PN:SC300001G00  
 2'S PN:SC300002E00

Place Close to TL1



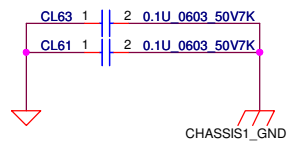
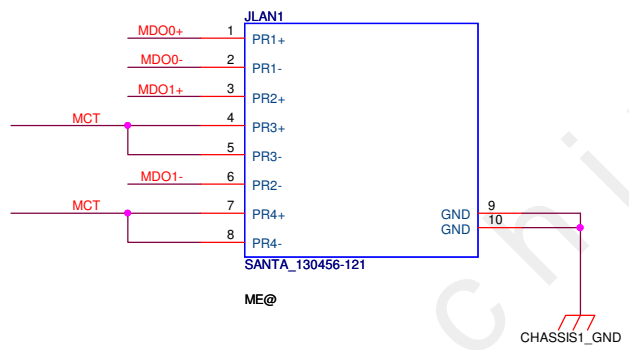
Reserve gas tube for EMI go rural solution



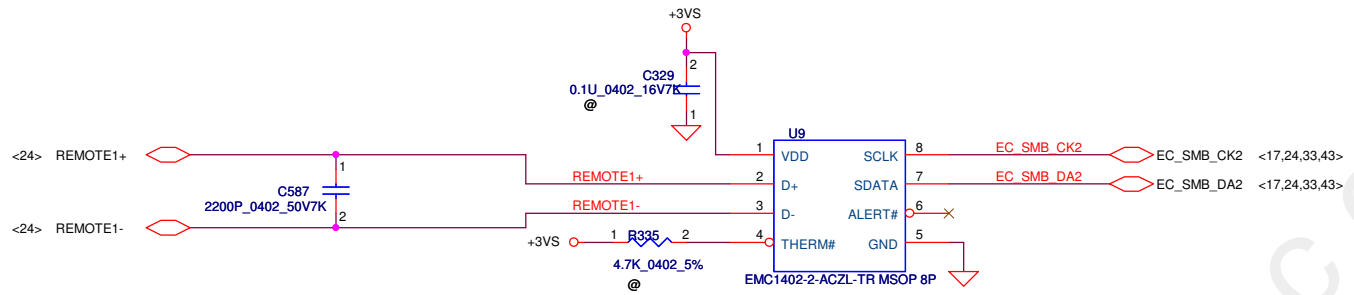
Place Close to TL1

DLL1  
 BS4200N-C-LV\_SMB-F2  
 GAS@

Need check Symbol



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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title LAN_Transformer	
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				Document Number LA-7982P	Date Thursday, October 11, 2012

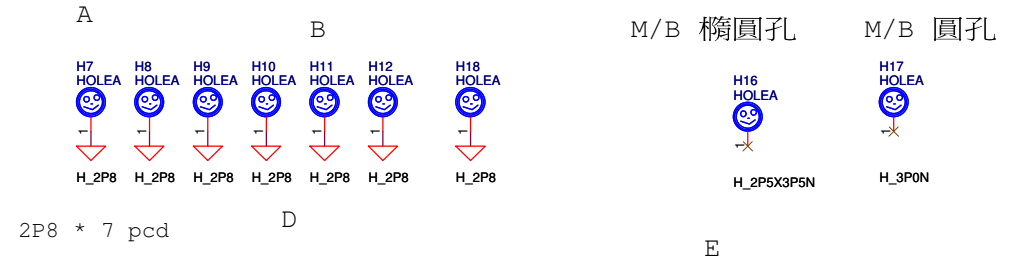
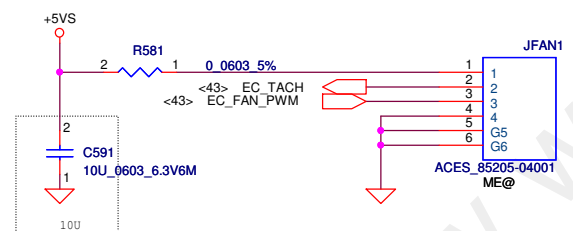


EMC1412-A (SA00003YA00)  
Address 1111\_100xb  
S IC EMC1412-A-ACZL-TR MSOP 8P SENSOR

REMOTE1, 2+/-:  
Trace width/space: 10/10 mil  
Trace length: <8"



**FAN1 Conn**

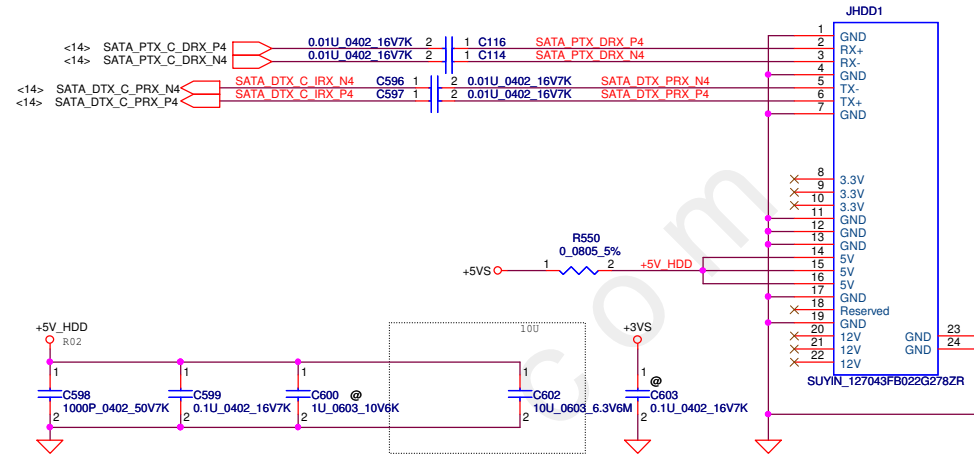


Security Classification	Compal Secret Data			<b>Compal Electronics, Ltd.</b>	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	<b>Fintek-Thermal IC/FAN/screw</b>
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				Date: Thursday, October 11, 2012	Sheet

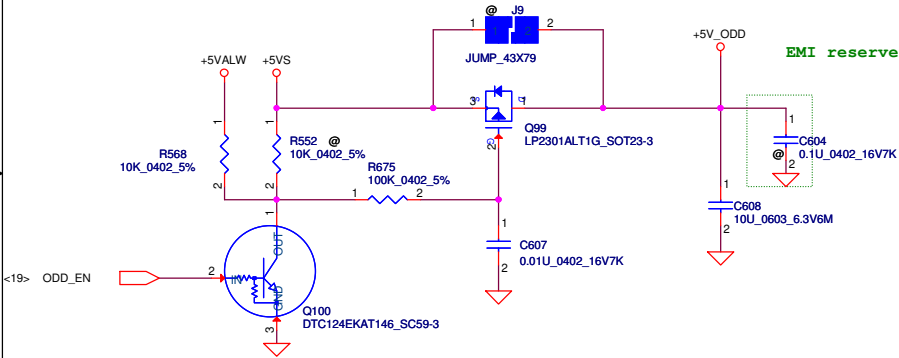




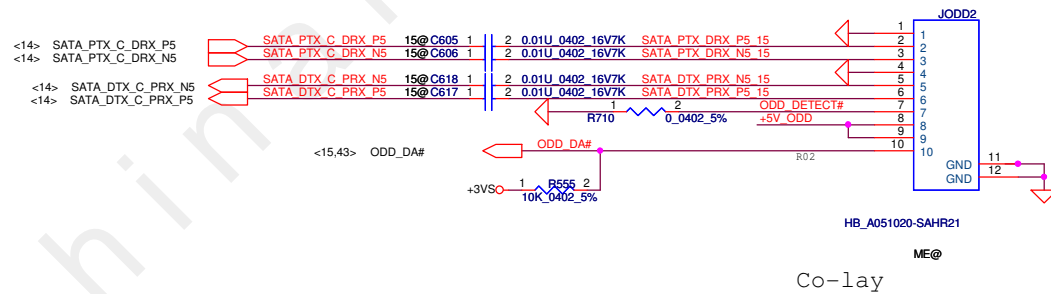
### SATA HDD Conn.



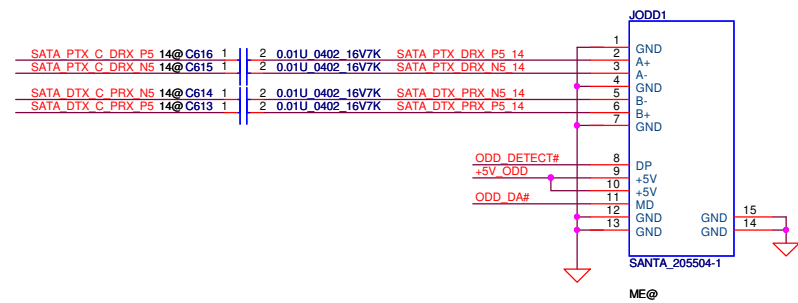
### ODD Power Control



### FOR 15" SATA ODD FFC Conn.

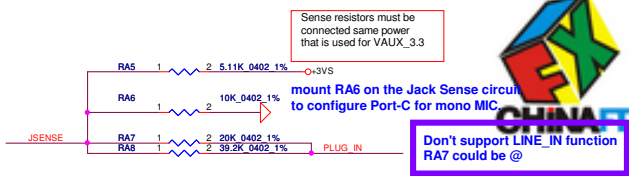


### FOR 14" SATA ODD Conn.

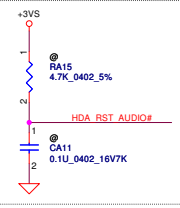


Security Classification	Compal Secret Data			Title	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	HDD/ODD/BT Connector	
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				Document Number	LA-9641P
				Date:	Thursday, October 11, 2012
				Sheet	41 of 60

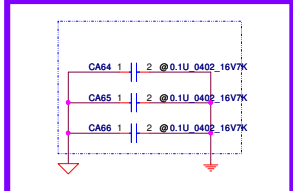
**CX20751**  
**High Definition Audio Codec SoC**  
**With Integrated Class-D Stereo**  
**Amplifier.**  
**An integrated 5 V to 3.3 V Low-dropout**  
**voltage regulator (LDO).**  
**An integrated 3.3 V to 1.8V Low-dropout**  
**voltage regulator (LDO).**



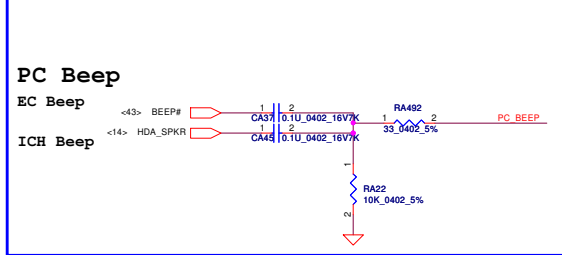
For EMI  
 Near Audio Chip



using wide copper bridge  
 under codec (100 mils or more)



follow vendor suggest  
 & reserver default design

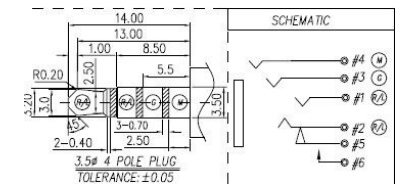


CA3 vendor suggest  
 change to 2.2U

AVDD\_3.3 pins output of  
 internal LDO, NOT connect  
 to external supply.

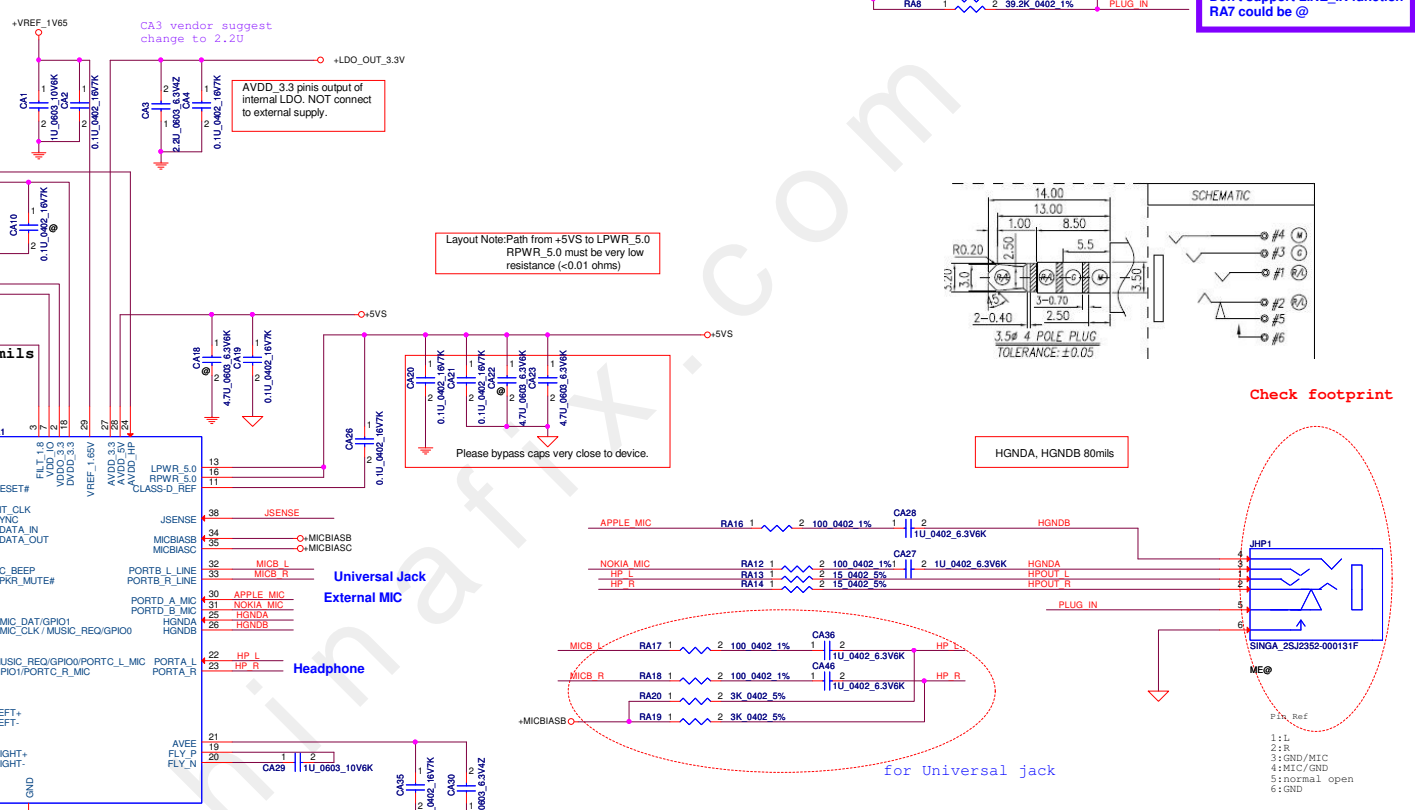
Layout Note: Path from +5VS to LPWR\_5.0  
 RPWR\_5.0 must be very low  
 resistance (<0.01 ohms)

Please bypass caps very close to device.

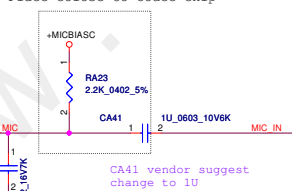


Check footprint

HGND, HGND 80mils



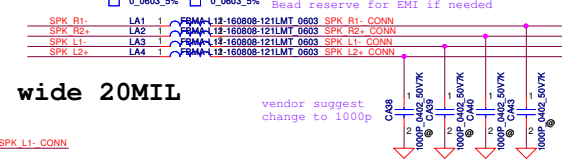
Place colose to Codec chip



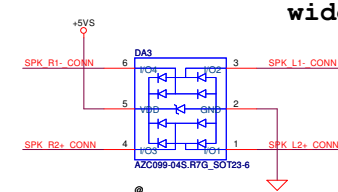
CA41 vendor suggest  
 change to 1U

CA30 vendor suggest  
 change to 2.2U

LA1-LA4 vendor suggest mount 0 ohm first-  
 Bead reserve for EMI if needed



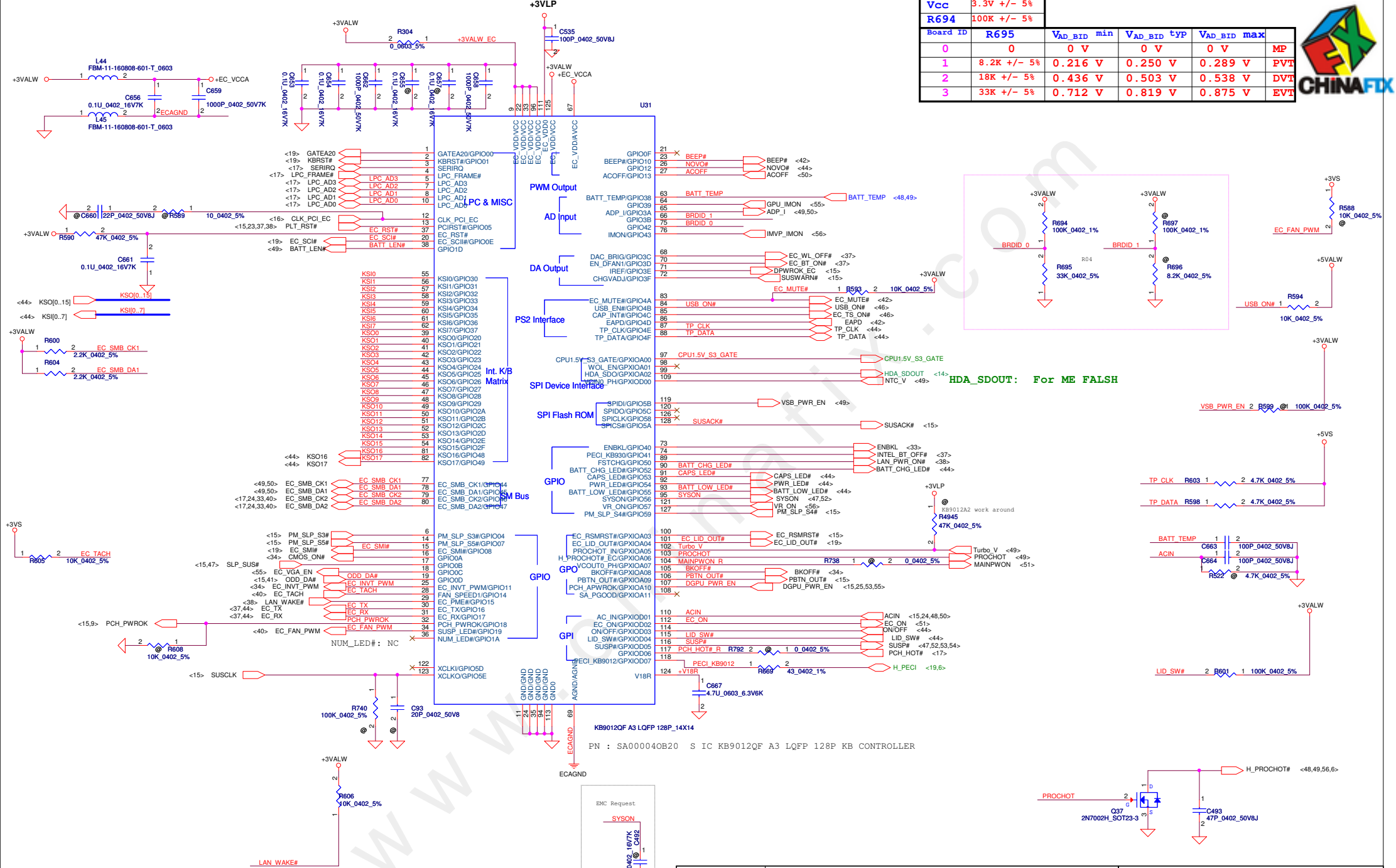
vendor suggest  
 change to 1000p



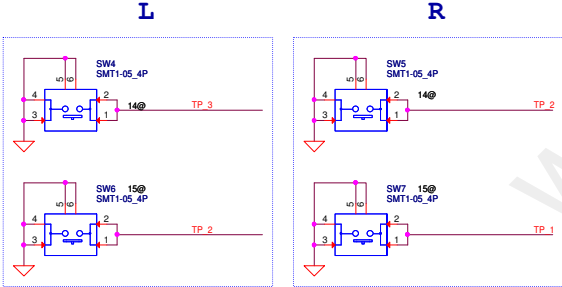
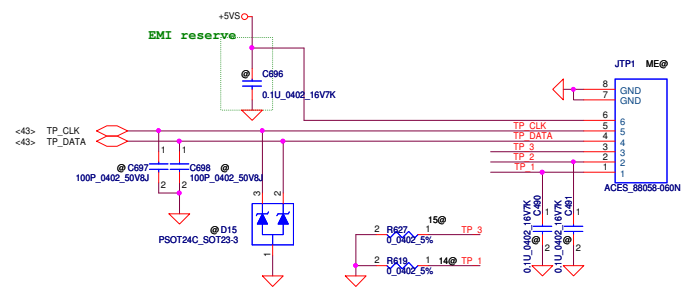
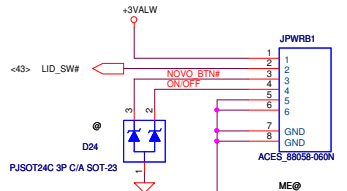
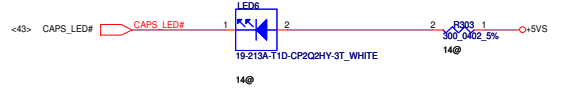
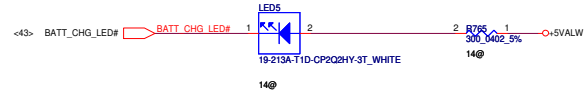
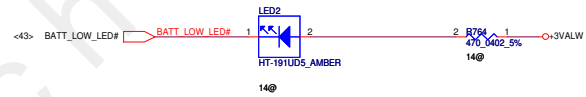
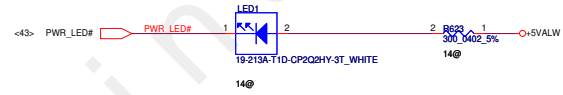
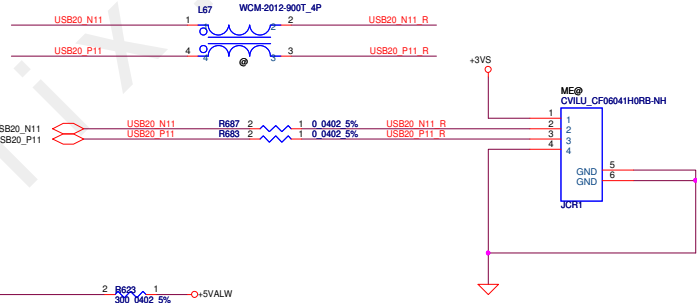
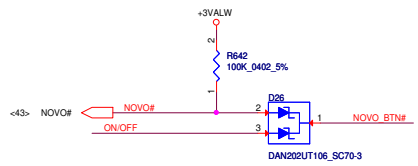
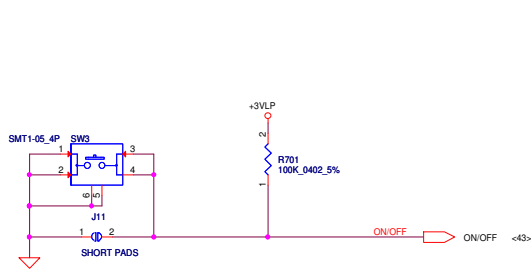
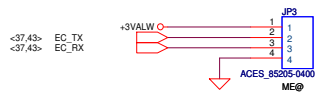
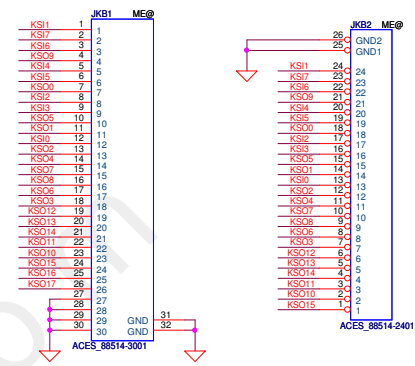
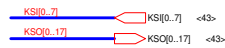
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	CX20751 Codec
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Size	Document Number	Rev	1.0		
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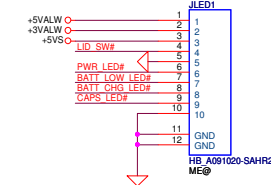
Vcc	3.3V +/- 5%				
R694	100K +/- 5%				
Board ID	R695	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max	MP
0	0	0 V	0 V	0 V	PVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	DVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	DVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	EVT



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Size	Document Number	Rev	Date	
Custom	LA-9641P	2.0	Thursday, October 11, 2012   Sheet 43 of 60	



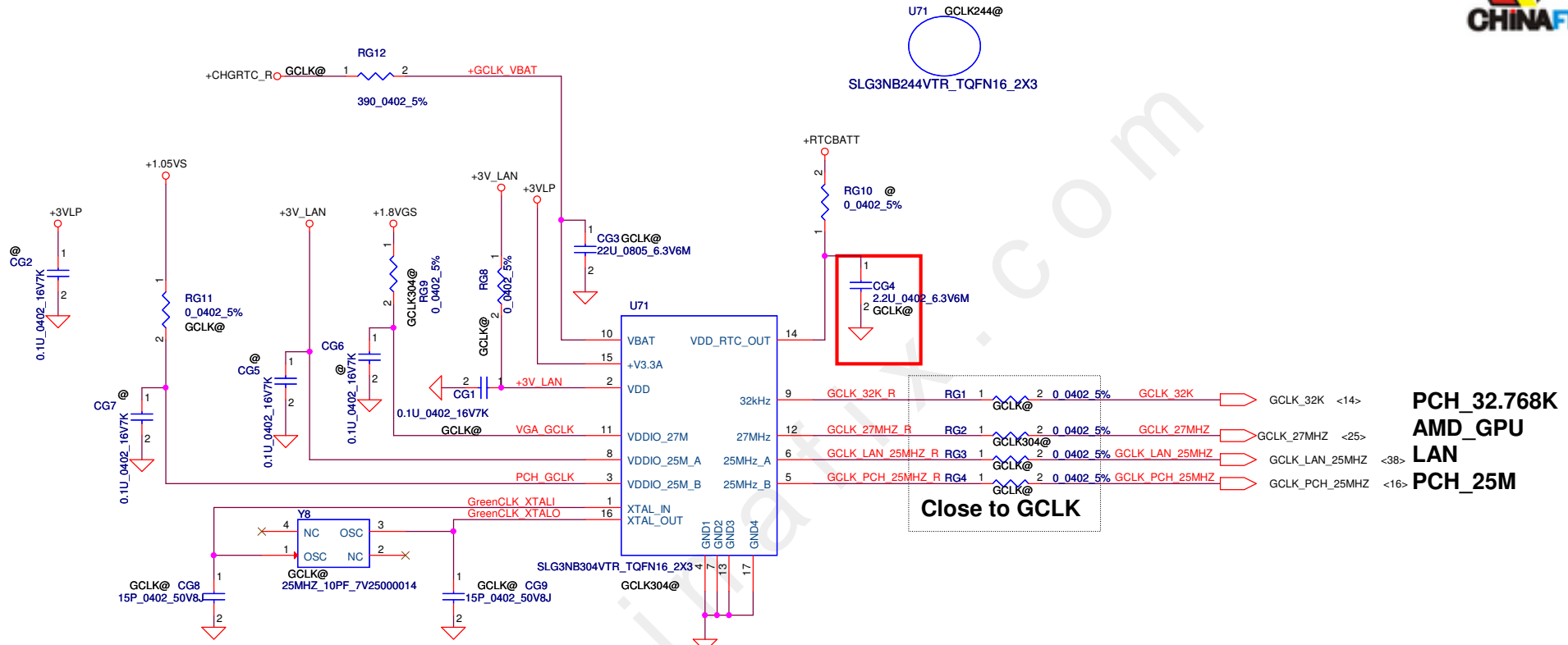
15"	14"
1 VCC	1 VCC
2 CLK	2 CLK
3 DAT	3 DAT
4 GND	4 L
5 L	5 R
6 R	6 GND



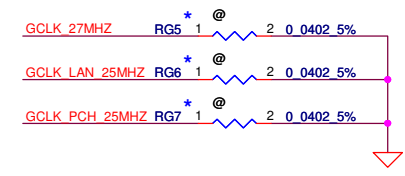
# Green Clock



Every power trace need:  
W=20mils

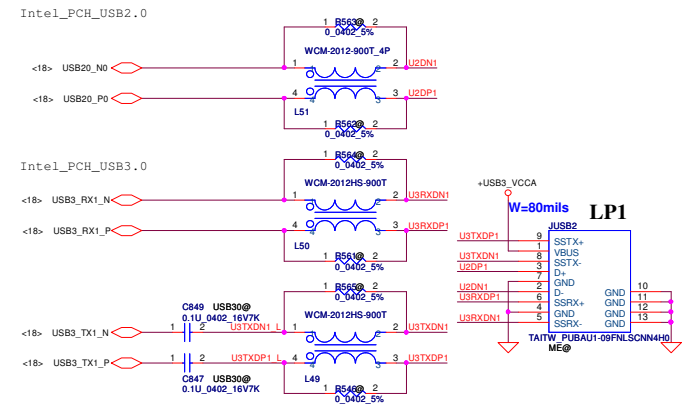
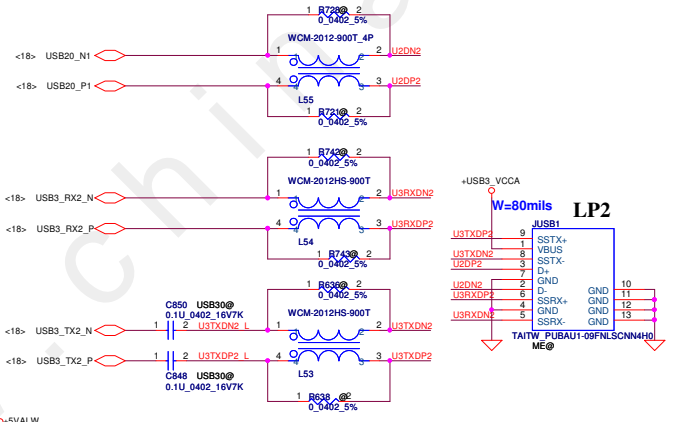
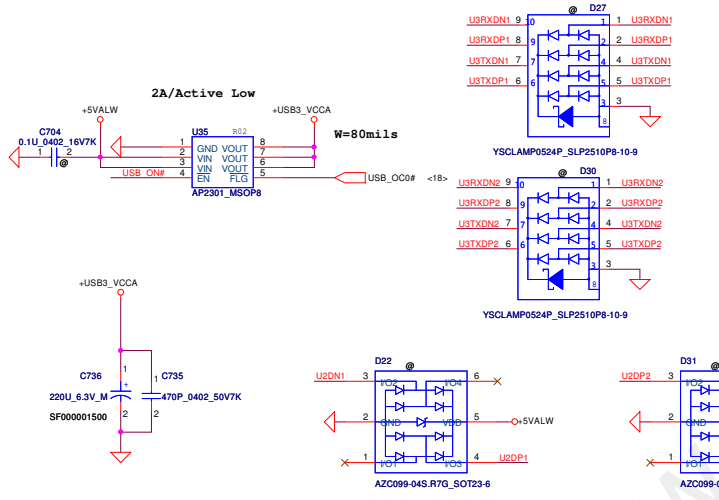
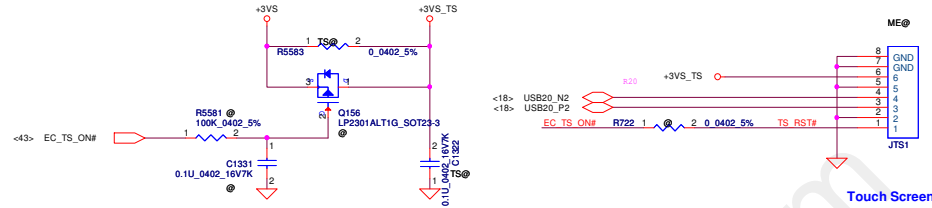
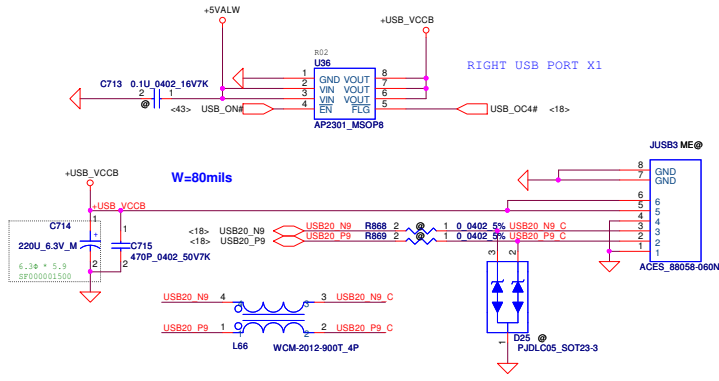


Reserved for Swing Level adjustment  
(Close GCLK side)



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				Document Number
Date:			Thursday, October 11, 2012	Sheet
			45	of 60

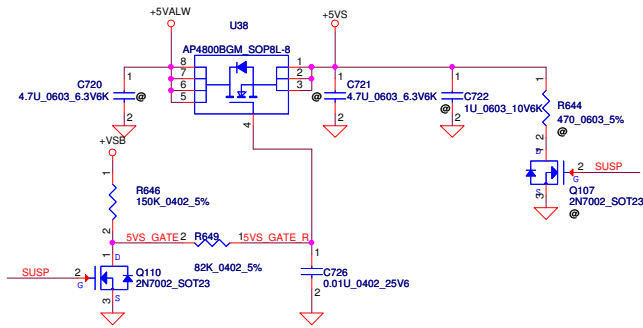
Right Ext.USB Conn.



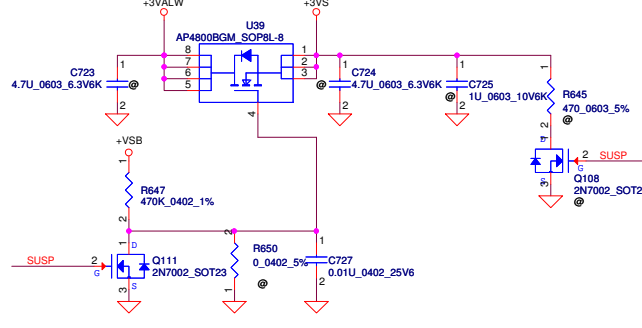
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title
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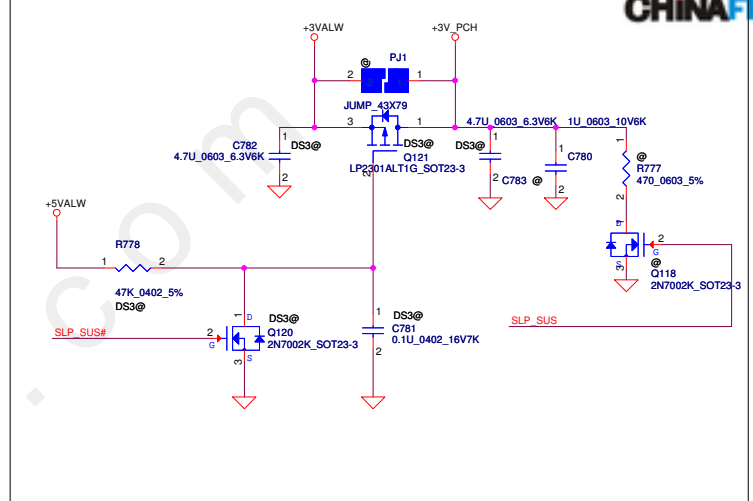
**+5VALW TO +5VS**



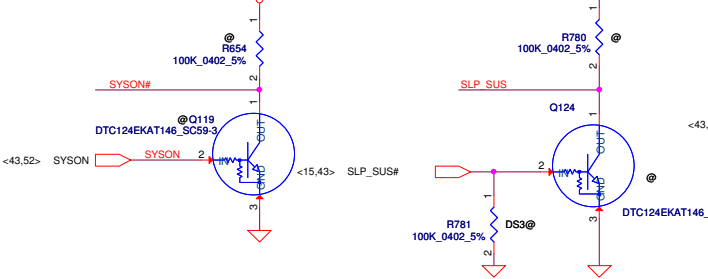
**+3VALW TO +3VS**



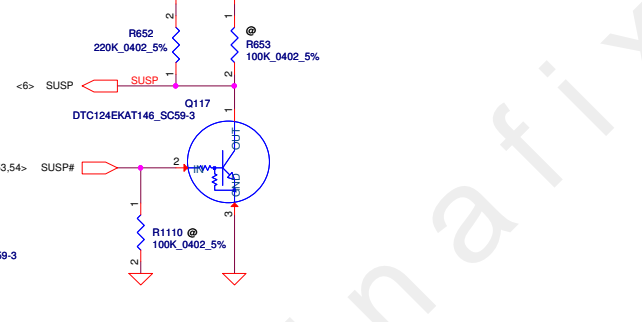
**+3VALW TO +3VALW(PCH AUX Power)**



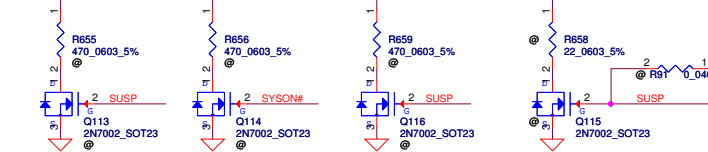
**+5VALW**



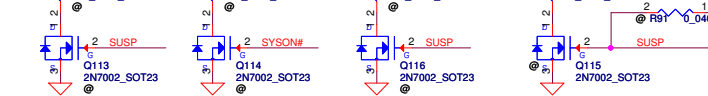
**+RTCVC**



**+1.5VS**



**+1.35V**



**+1.05VS**

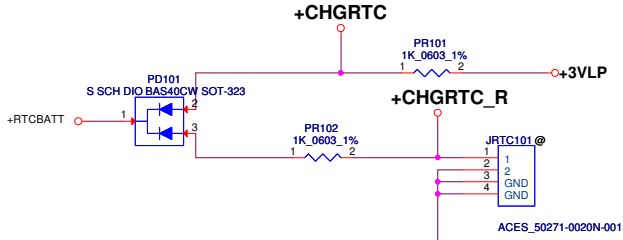
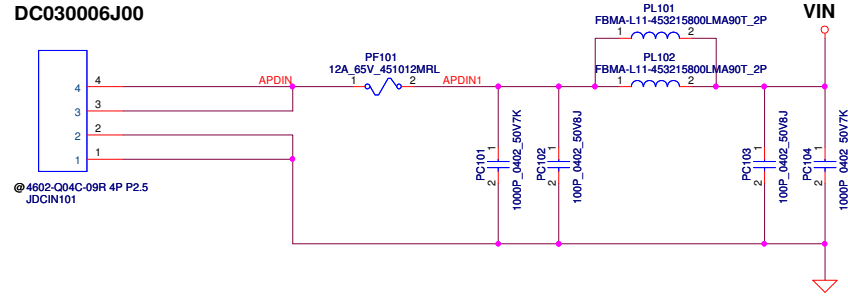


**+0.675VS**

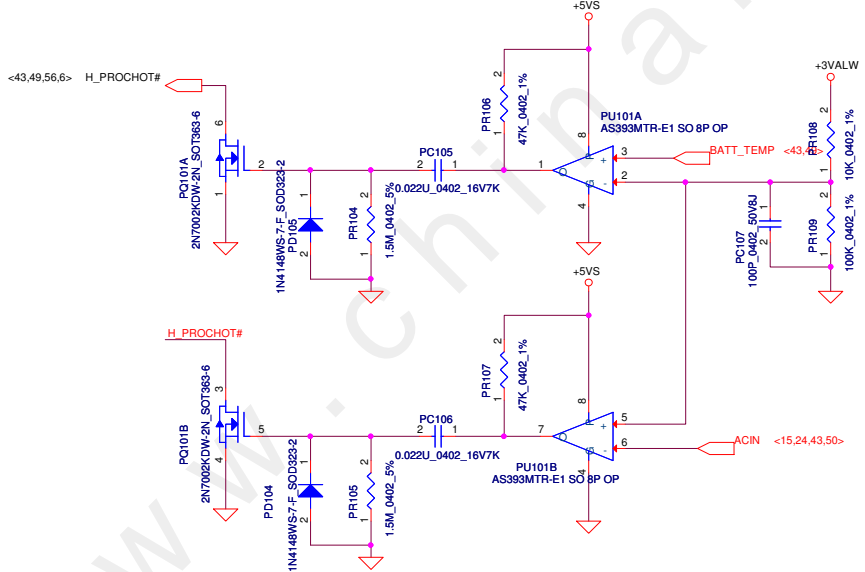


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Issued Date	2011/06/15	Deciphered Date	2012/07/11	Title	
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Size	Document Number	LA-9641P		Rev	2.0
Date:	Thursday, October 11, 2012	Sheet	47	of	60

DC030006J00

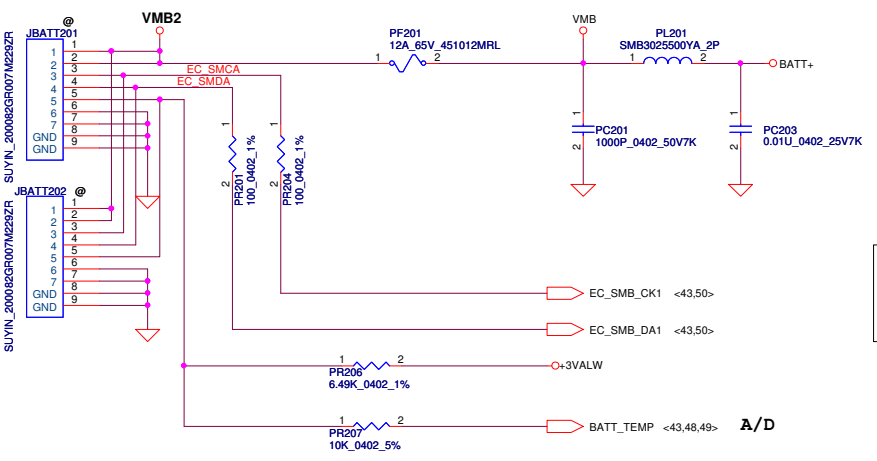


RTC Battery



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				Document Number	Rev
				Gx00	0.1
				Date: Thursday, October 11, 2012	Sheet 48 of 59

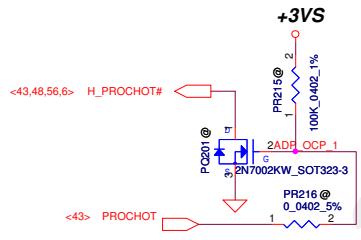




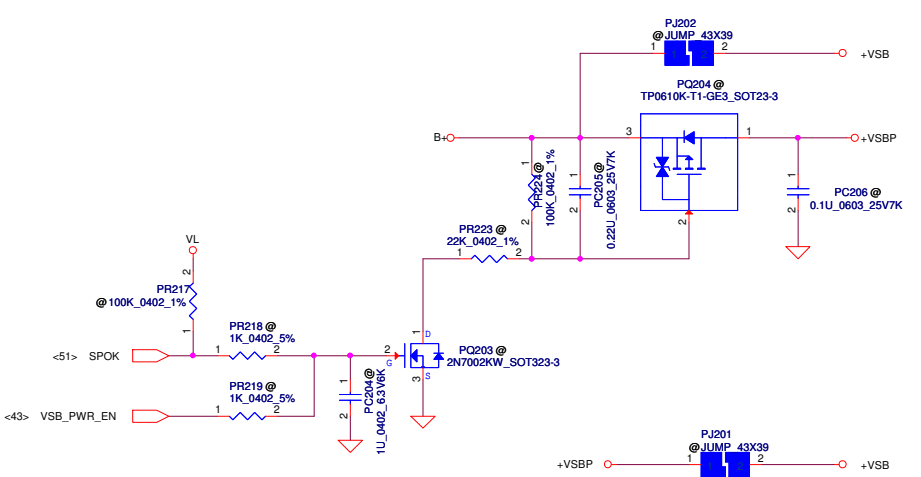
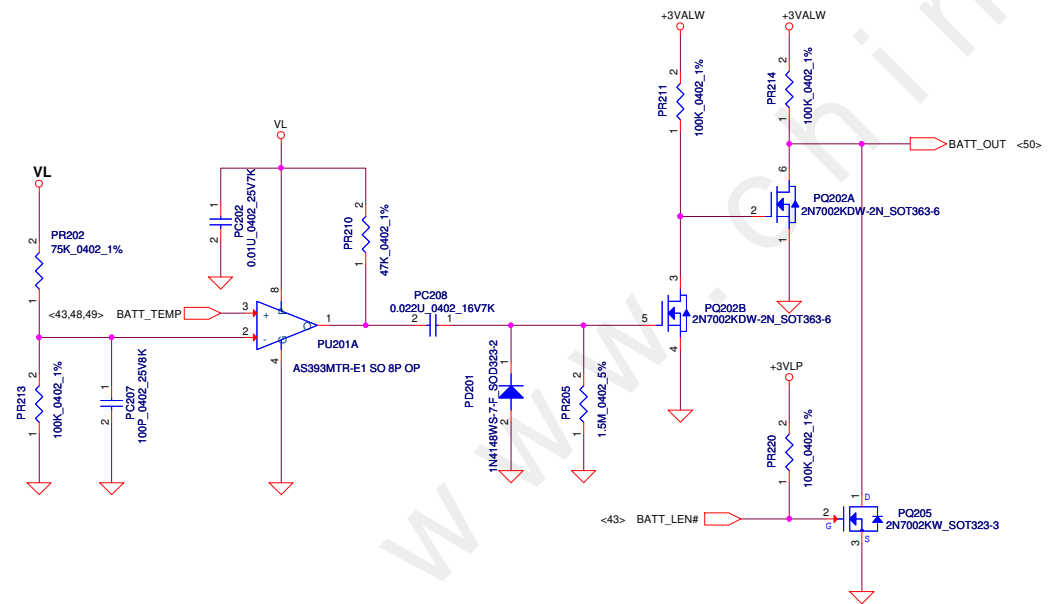
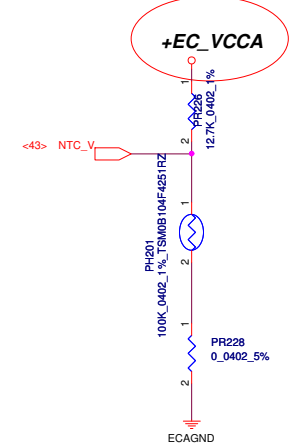
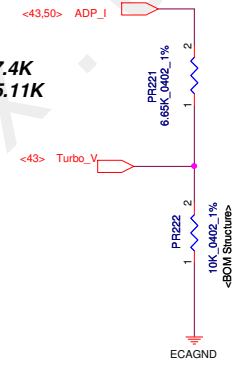
**PH201 under CPU bottom side :**  
**CPU thermal protection at 93 +-3 degree C**  
**Recovery at 56 +-3 degree C**

**90W(DIS) : 6.65K 100W active 90W recovery**  
**65W(UMA) : 1.65K 70W active 65W recovery**

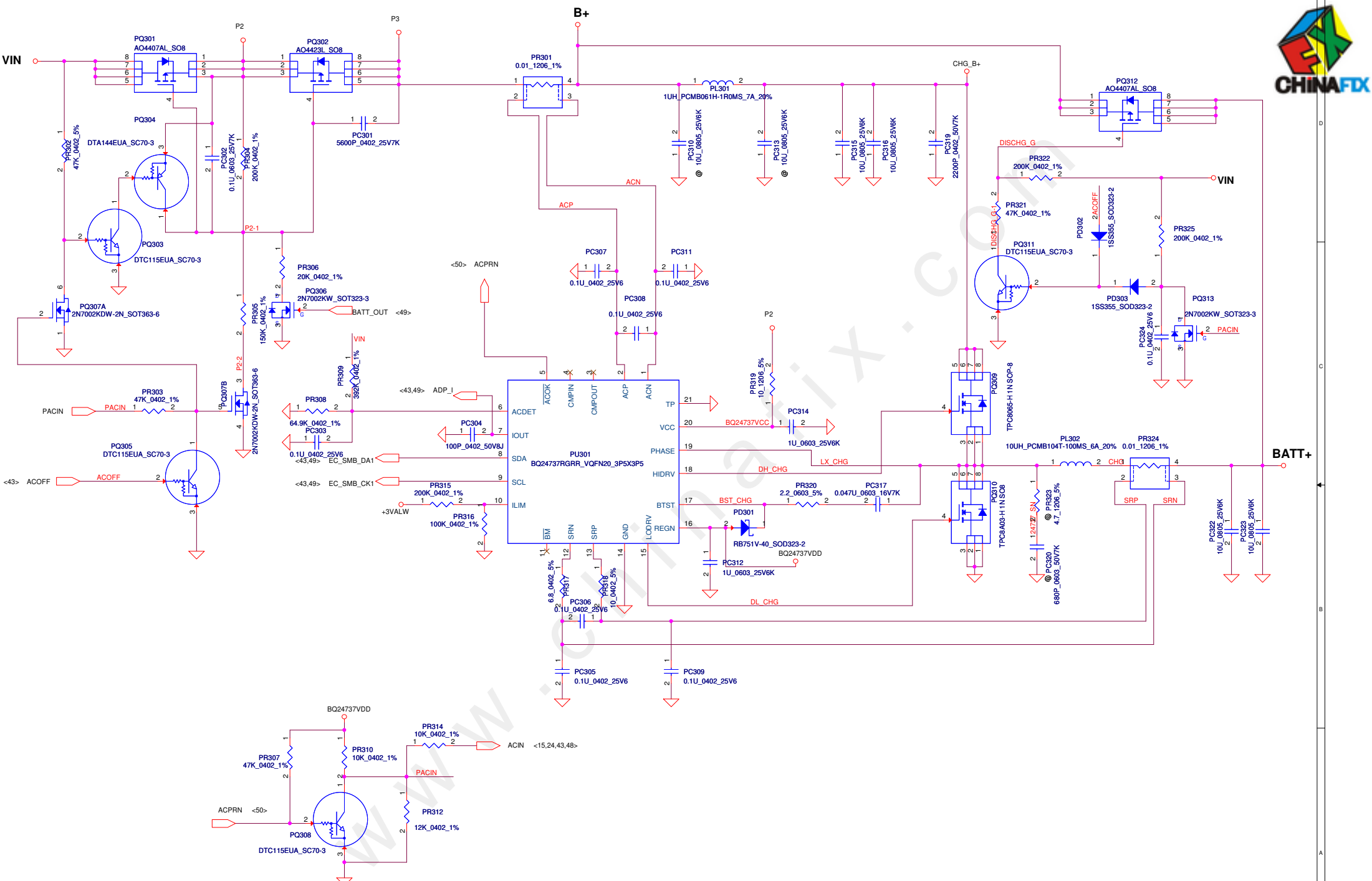
20120314  
 Change to +EC\_VCCA from +3VLP



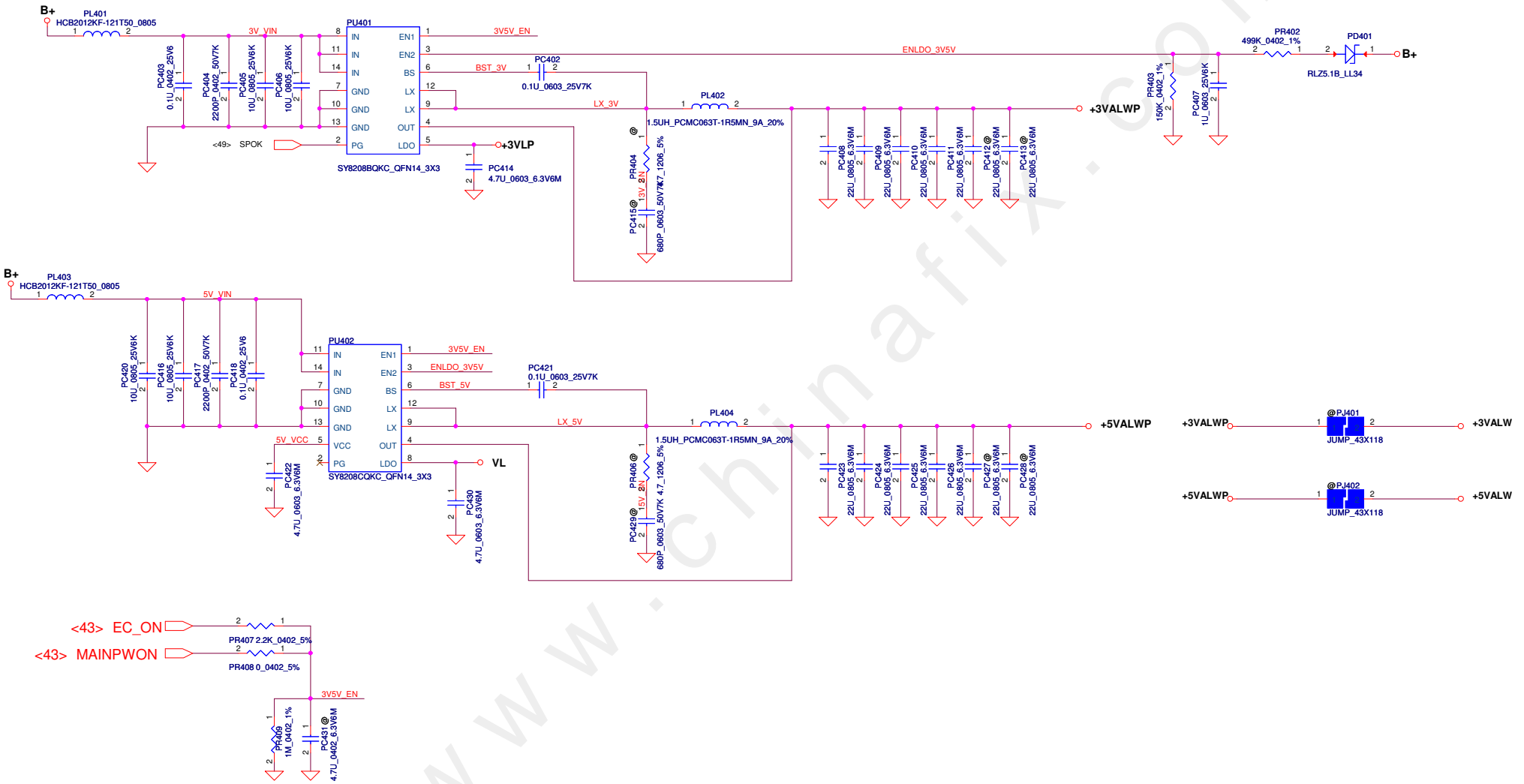
**90W(DIS) : 27.4K**  
**65W(UMA) : 5.11K**



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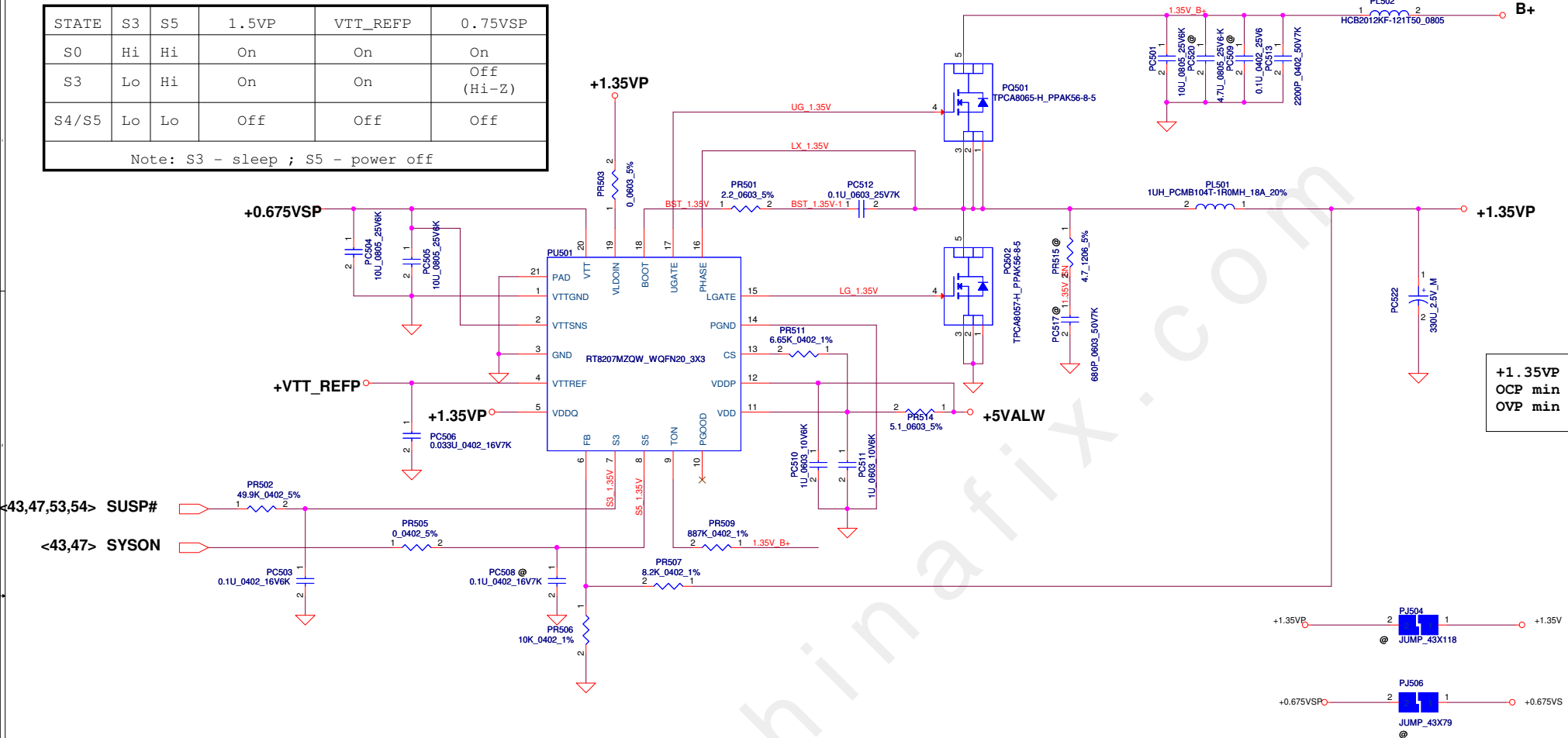
**Compal Electronics, Inc.**  
**PWR- 3VALWP/5VALWP**

Rev  
0.1

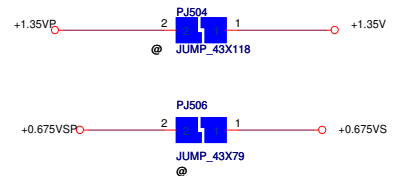


STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

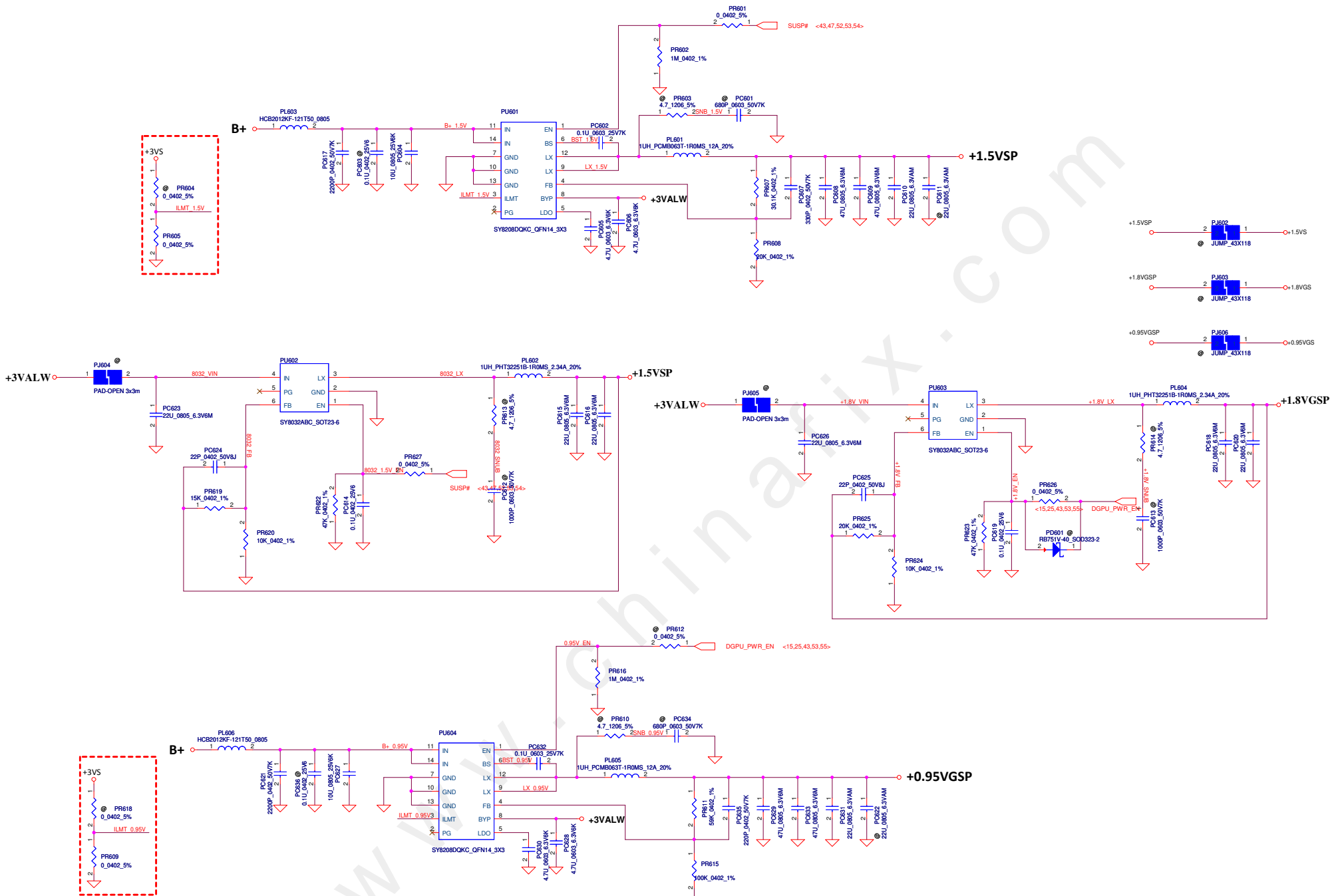
Note: S3 - sleep ; S5 - power off



+1.35VP  
 OCP min 20A  
 OVP min 1.485V

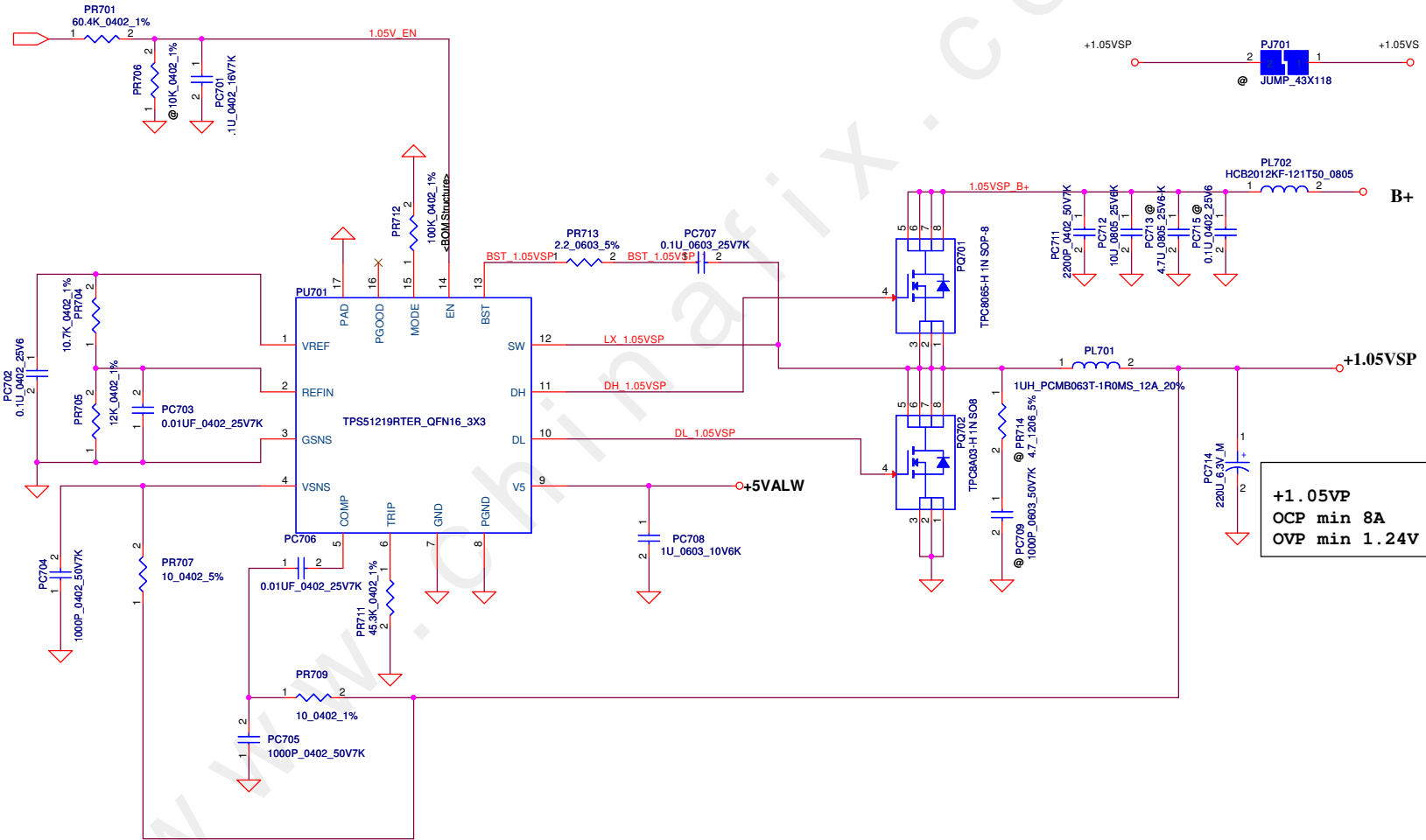


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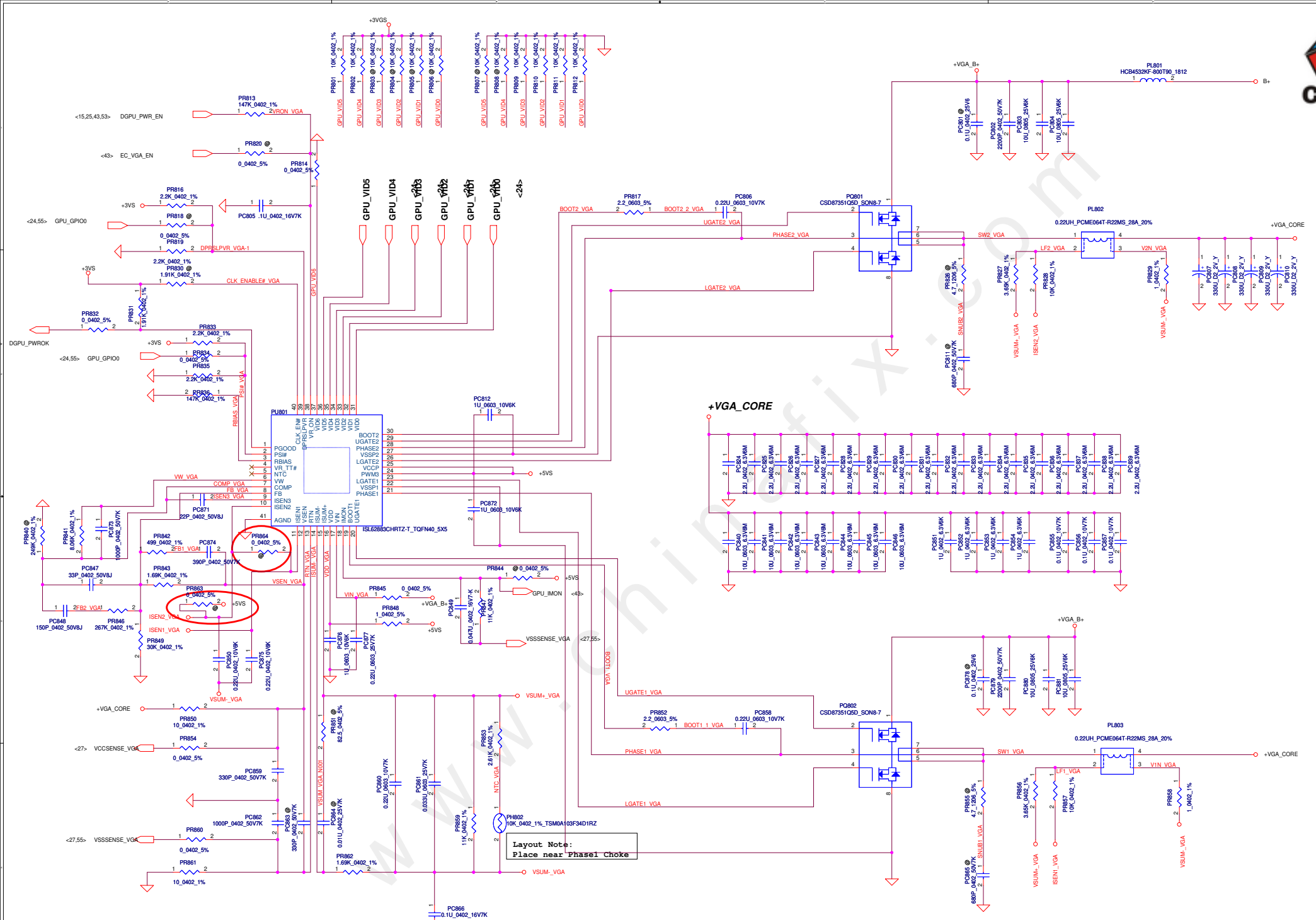


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<43,47,52,53> SUSP#

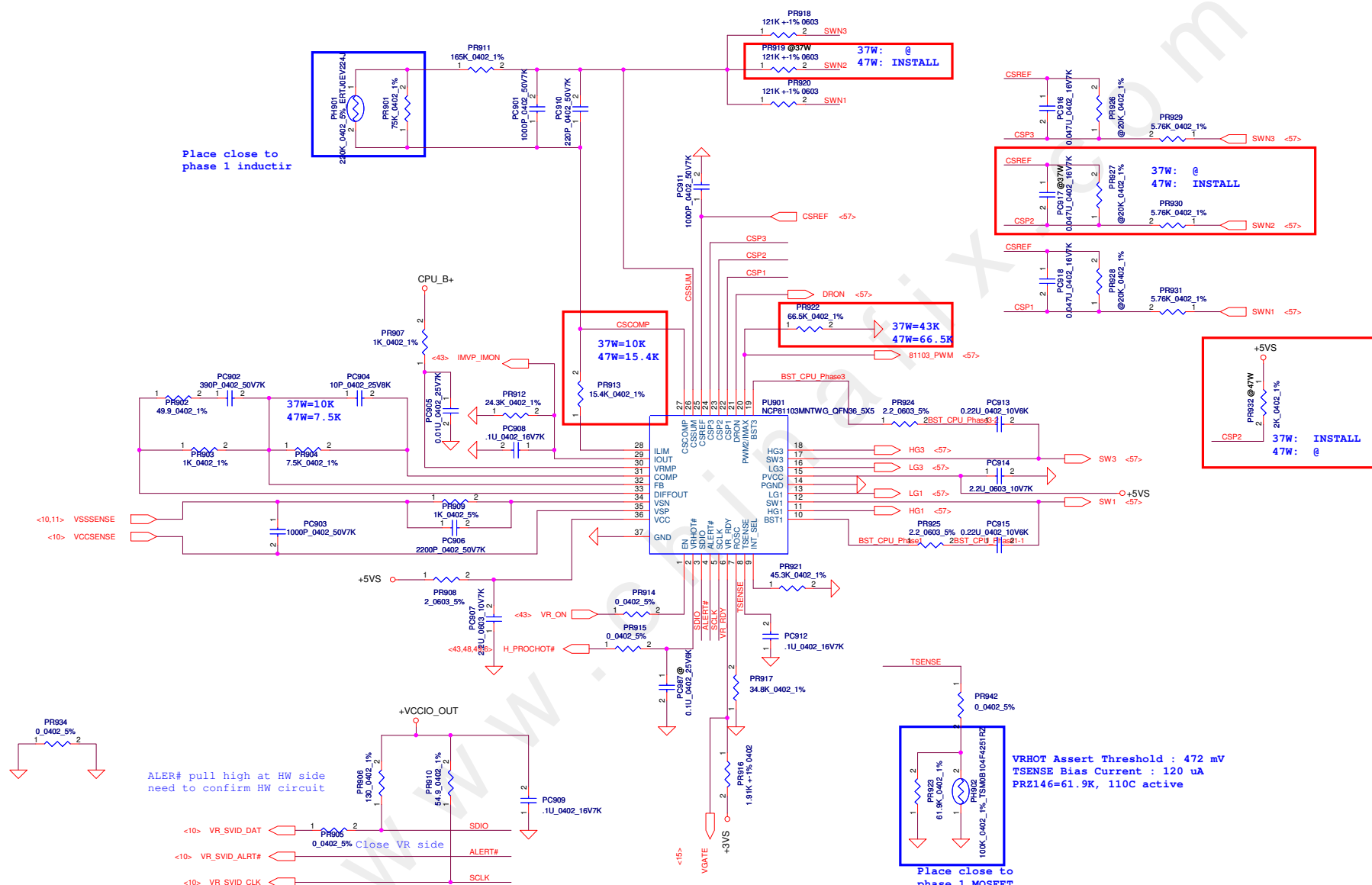


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Layout Note:  
Place near Phase1 Choke

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				VGA_COREP	
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Place close to phase 1 inductor

ALER# pull high at HW side need to confirm HW circuit

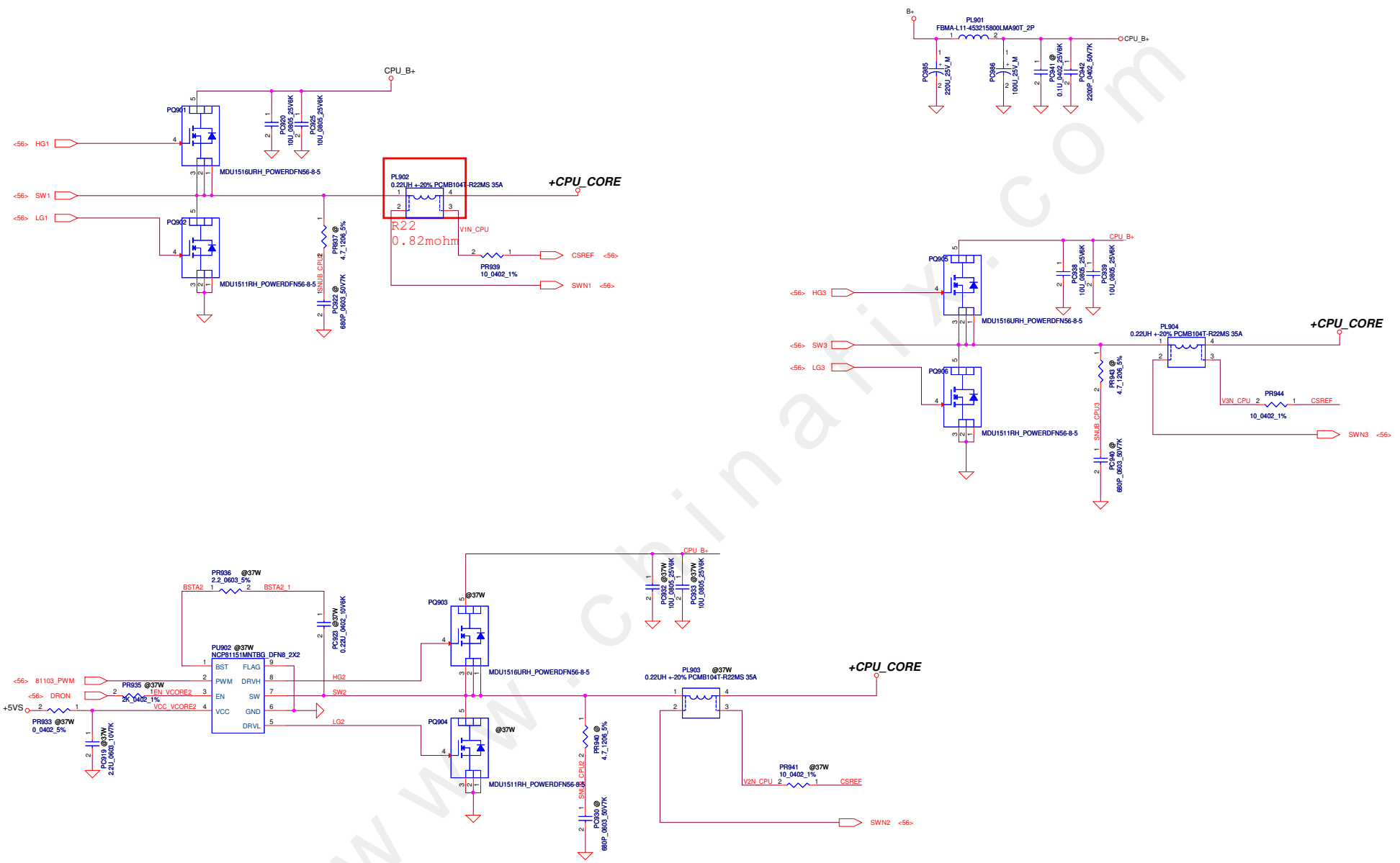
Close VR side

Place close to phase 1 MOSFET

VRHOT Assert Threshold : 472 mV  
TSENSE Bias Current : 120 uA  
PRZ146=61.9K, 110C active

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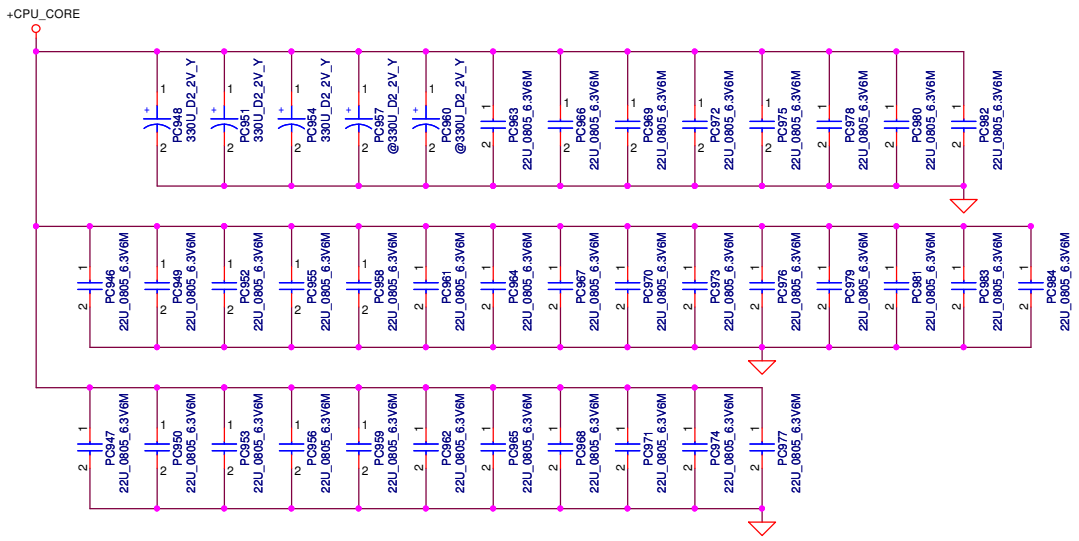




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**+CPU\_CORE** 3 X 330u/9m (47W) 2X330u/9m (37W)  
 34 X 22u/0805 34 X 22u/0805



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Version change list (P.I.R. List)



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