

LCFC Confidential

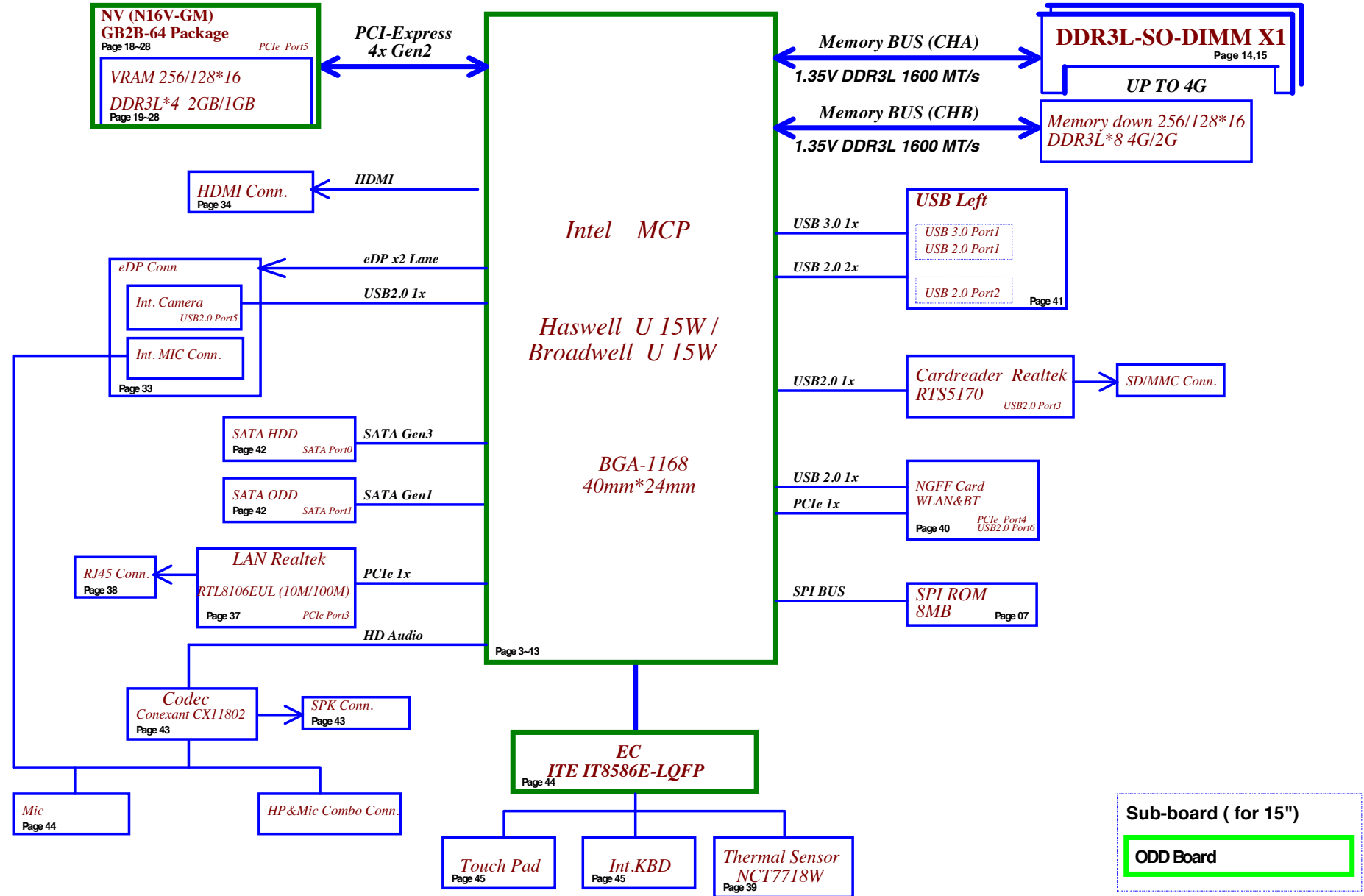
CG510 M/B Schematics Document

Intel Broadwell U-Processor with DDRIIL + NV920

2015-05-09

REV: 0.2

Security Classification	LC Future Center Secret Data			Title		
Issued Date	2015/02/27	Deciphered Date	2013/08/05	Cover Page		
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Sub-board (for 15")
ODD Board

Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane	B+	+3VALW +5VALW	+3VALW_PCH	+1.35V	+5VS
					+3VS
State	S0	O	O	O	+1.5VS
					+1.35VS
S3	O	O	O	O	+1.05VS
					+0.675VS
S3 Battery only	O	O	O	O	CPU_CORE
					+VGA_CORE
S5 S4/AC Only	O	O	O	X	+3VGS
					+1.8VGS
S5 S4 Battery only	O	X	X	X	+1.35VGS
					+0.95VGS
S5 S4 AC & Battery don't exist	X	X	X	X	

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0 XHCI		USB 3.0 XHCI	
0	USB Port (Right Side)		
1	USB Port1 (Left Side)	1	USB Port1 (Left Side)
2	USB Port2 (Left Side)	2	
3	Cardreader	3	
4	TOUCH PANEL	4	
5	Camera		
6	NGFF(WLAN)		
7			

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
UMA@	UMA SKU part
PX@	Discrete GPU SKU part
100M@	100M LAN Part
GIGA@	GIGA LAN Part
JET@	For AMD Jet GPU part
TOPAZ@	For AMD Topaz GPU part
RANKA@	For VRAM RankA part
RANKB@	For VRAM RankB part
ME@	ME part(connector, hole)
TS@	For support touch panel sku part
AOAC@	AOAC support part
H2@	Hynix 128Mx16 VRAM part
H4@	Hynix 256Mx16 VRAM part
M2@	Micron 128Mx16 VRAM part
M4@	Micron 256Mx16 VRAM part
S2@	Samsung 128Mx16 VRAM part
S4@	Samsung 256Mx16 VRAM part
H2GX4@	Hynix 128Mx16 VRAM x4pcs sku
M2GX4@	Micron 128Mx16 VRAM x4pcs sku
S2GX4@	Samsung 128Mx16 VRAM x4pcs sku
H4GX4@	Hynix 256Mx16 VRAM x4pcs sku
M4GX4@	Micron 256Mx16 VRAM x4pcs sku
S4GX4@	Samsung 256Mx16 VRAM x4pcs sku
H2GX8@	Hynix 128Mx16 VRAM x8pcs sku
M2GX8@	Micron 128Mx16 VRAM x8pcs sku
S2GX8@	Samsung 128Mx16 VRAM x8pcs sku
H4GX8@	Hynix 256Mx16 VRAM x8pcs sku
M4GX8@	Micron 256Mx16 VRAM x8pcs sku
S4GX8@	Samsung 256Mx16 VRAM x8pcs sku
CD@	Cost down part
BCD@	Cost down part for BDW project
SINGLE@	Single Rank VRAM sku
DUAL@	Dual Rank VRAM sku

PCIE PORT LIST

Port	Device
1	
2	
3	LAN
4	WLAN
5	Discrete GPU
6	

SMBUS Control Table

	SOURCE	VGA	BATT	IT8586E	SODIMM	WLAN WIMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1	IT8586E			V						
EC_SMB_DA1	+3VALW	X	V	+3VALW	X	X	X	X	X	V
EC_SMB_CK2	IT8586E			V						
EC_SMB_DA2	+3VS	+3VGS	X	+3VS	X	X	+3VS	+3VALW_PCH	X	X
PCH_SMB_CLK	PCH									
PCH_SMB_DATA	+3VALW_PCH	X	X	X	+3VS	+3VS	X	+3VALW_PCH	X	X

EC SM Bus1 address

Device	Address
Smart Battery	0X16
Charger	0001 0010 b

EC SM Bus2 address

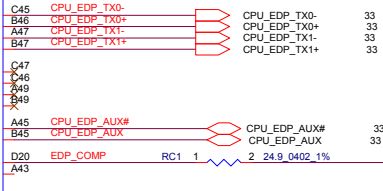
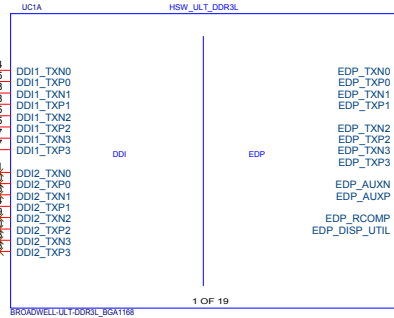
Device	Address
Thermal Sensor NCT7718W	1001_100xb
VGA	0x41(default)
PCH	need to update

PCH SM Bus address

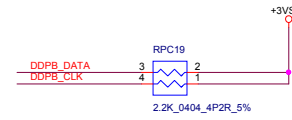
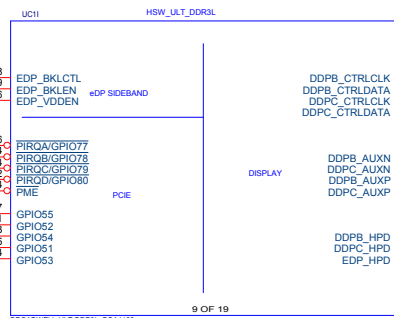
Device	Address
DDR DIMMA	1010 000Xb
DDR DIMMB	1010 010Xb
Wlan	Rsvd

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HDMI D2
HDMI D1
HDMI D0
HDMI CLK

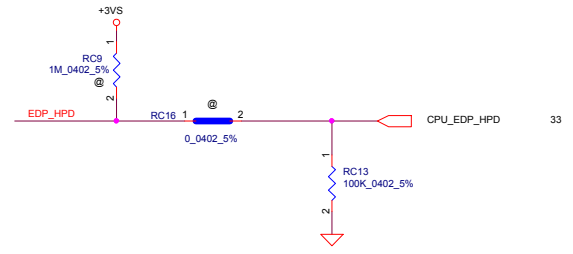
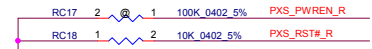
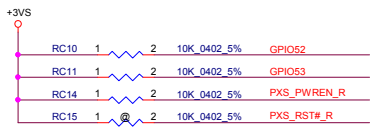
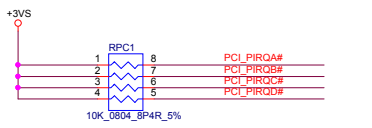
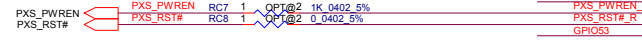


+VCCIOA_OUT & EDP_COMP :
Trace Width: 20mil
Space: 25mil
Max length: 100mil

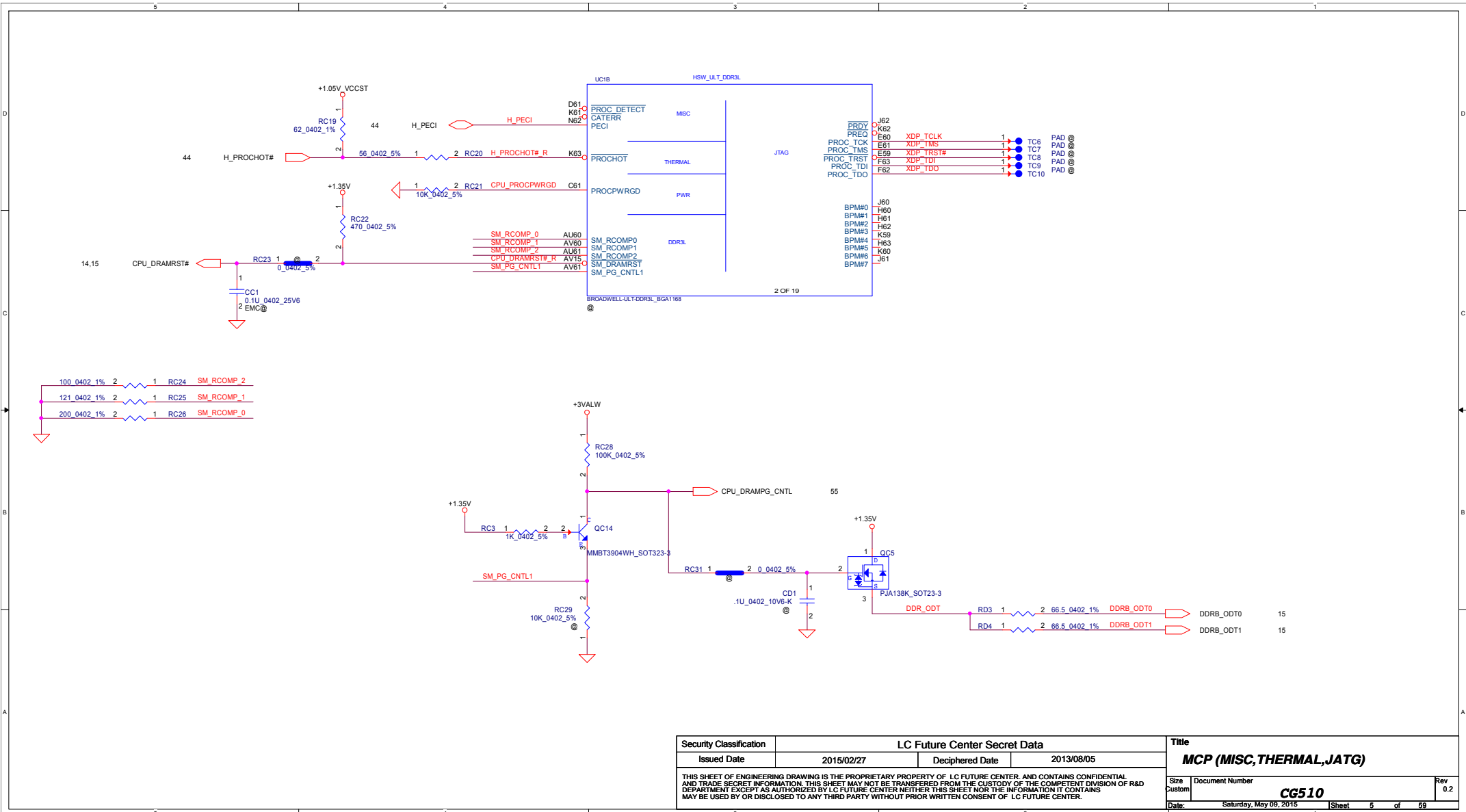


DDPx_CTRLCLK
The signal has a weak internal pull-down.
* H Port is detected.
L Port is not detected.

21.58
19

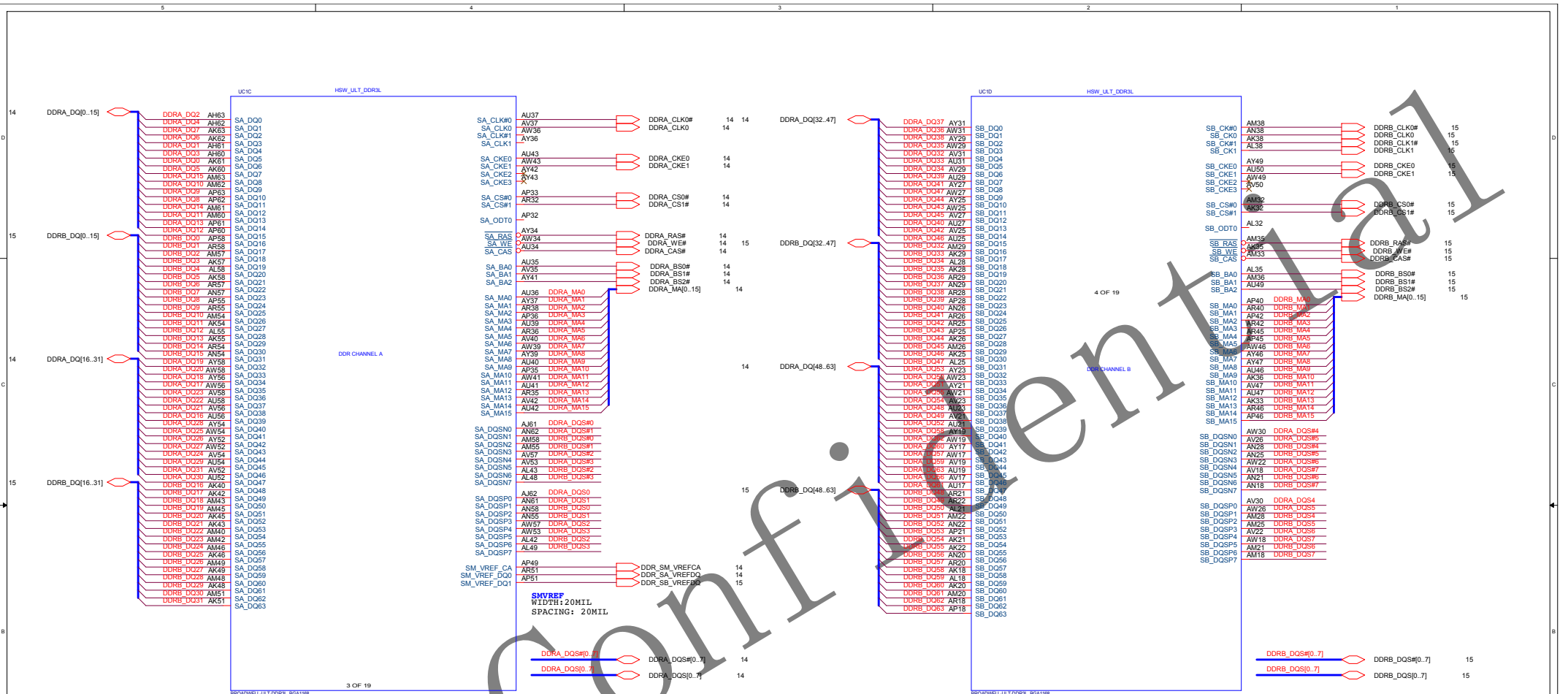


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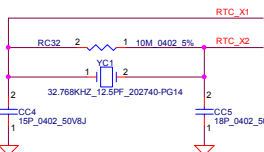


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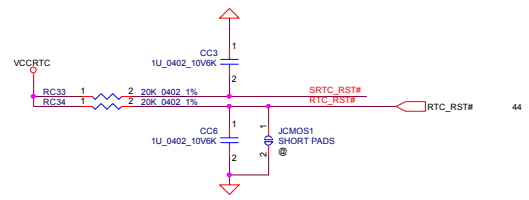
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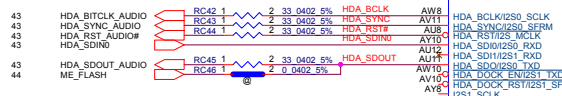
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CRYSTAL
 1. Space 15MIL
 2. No trace under crystal
 3. Place on opposite side of MCP for temp influence



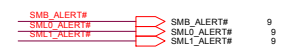
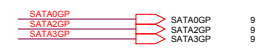
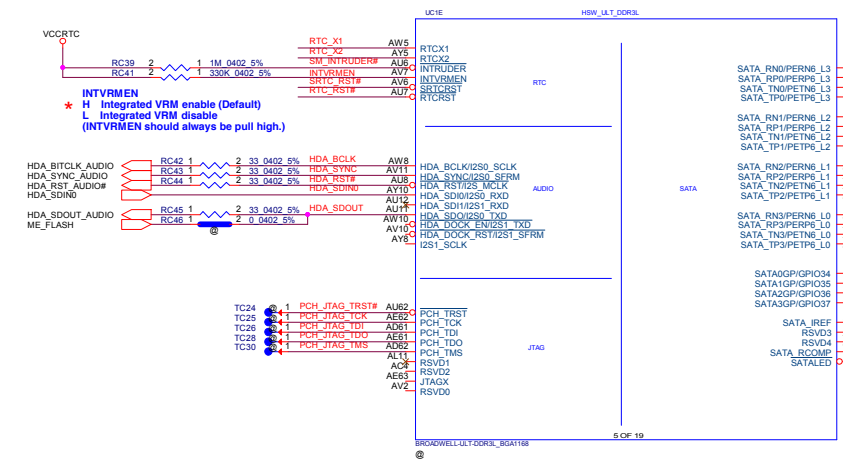
INTVRMEN
 * H Integrated VRM enable (Default)
 L Integrated VRM disable
 (INTVRMEN should always be pull high.)



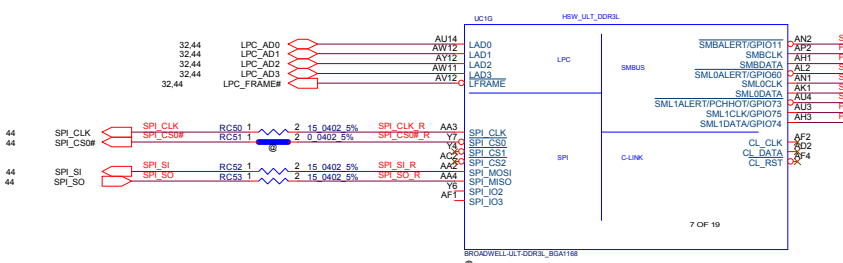
HDA_SDO This signal has a weak internal pull-down.
 * 0 = Enable security measures defined in the Flash Descriptor.
 1 = Disable Flash Descriptor Security(override). This strap should only be asserted high during external pull-up in manufacturing/debug environments ONLY.



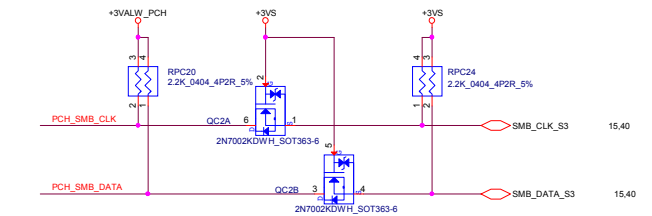
For EMI



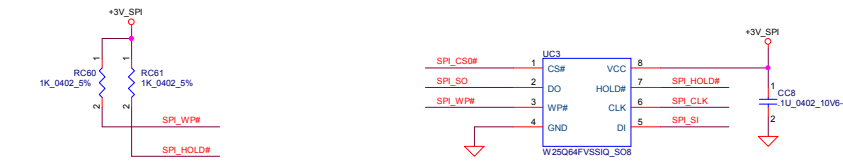
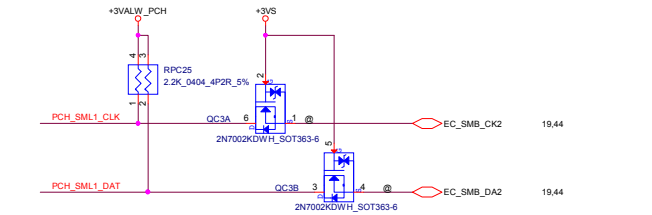
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 Width: 12-15mil
 Space: 12mil
 Length: 500mil



DIMM1, DIMM2, NGFF

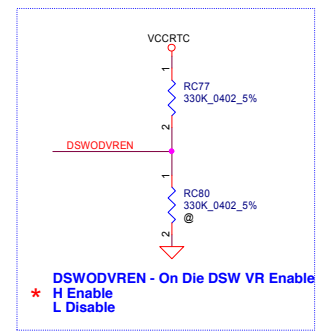
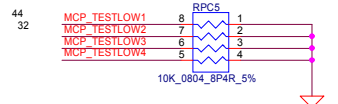
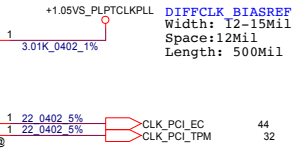
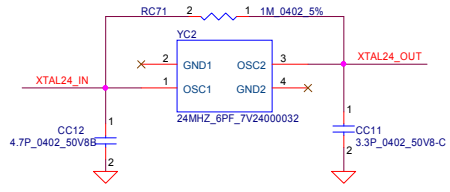
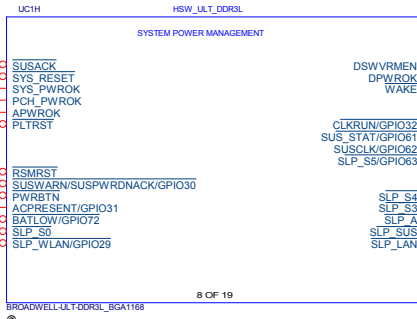
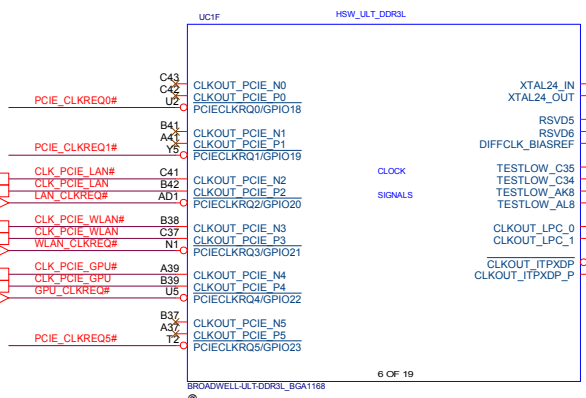
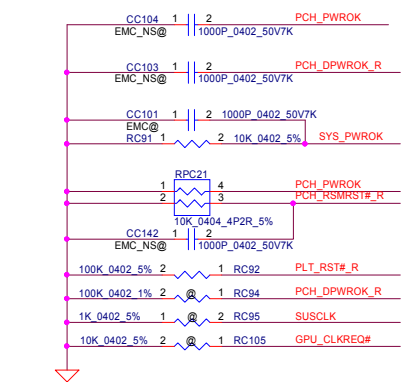
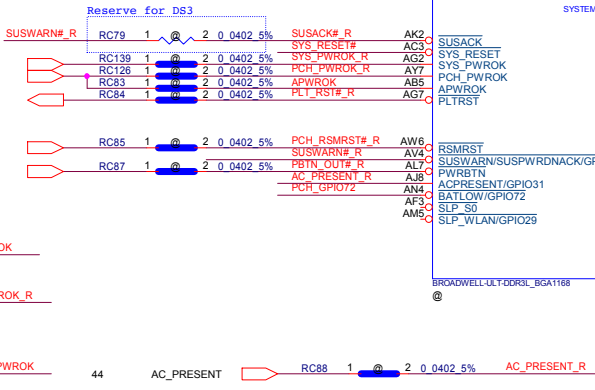
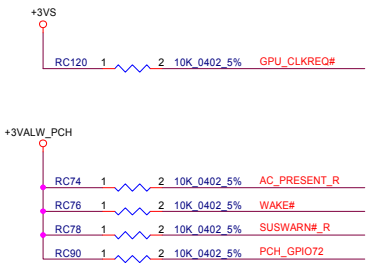
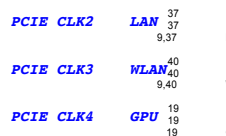
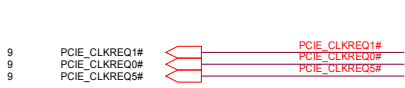


GPU, EC, Thermal Sensor



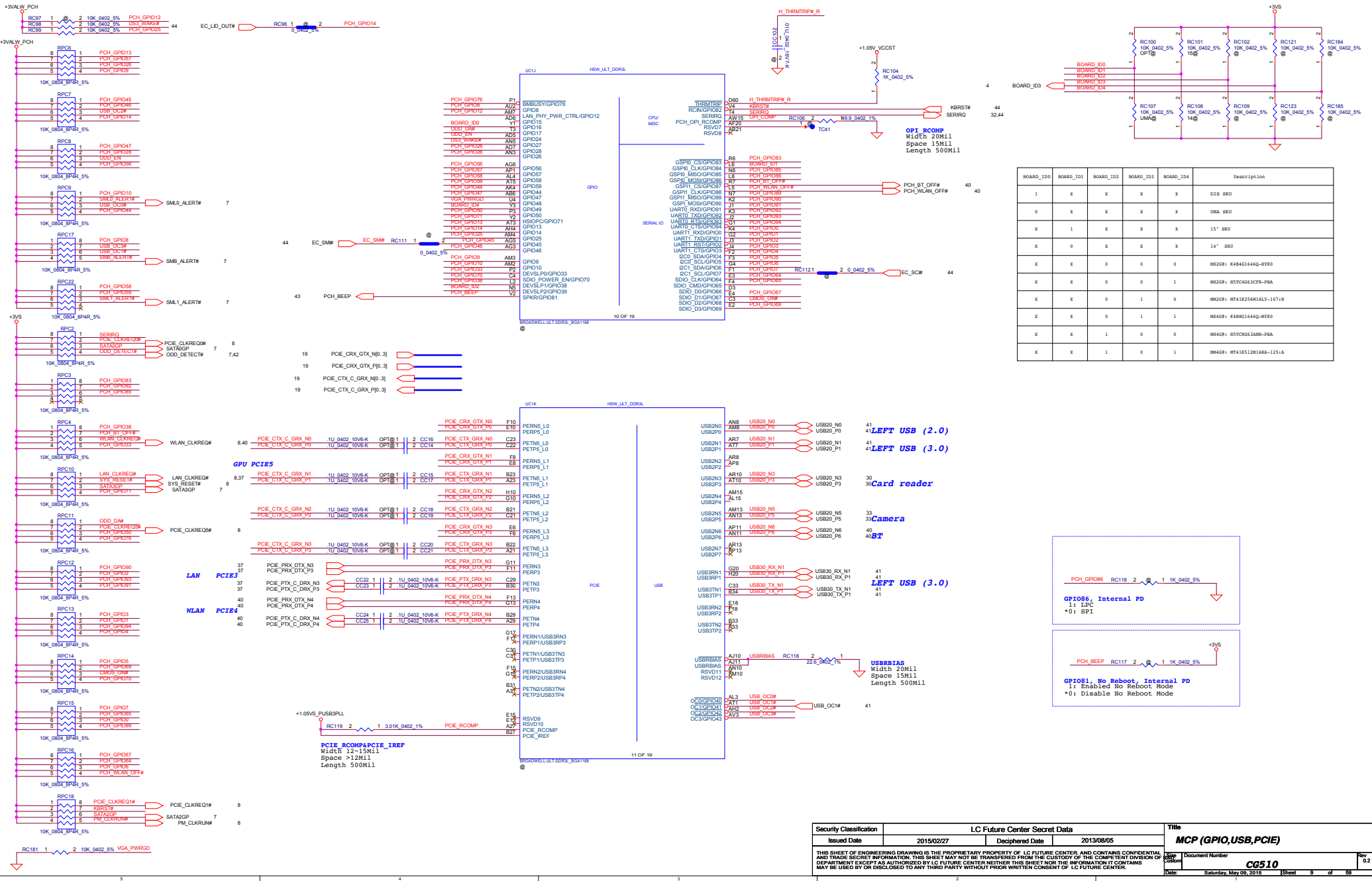
+3V SPI
 1. If support DS3, connect to +3VS and don't support EC mirror code;
 * 2. If don't support DS3, connect to +3VALW_PCH and support EC mirror code.

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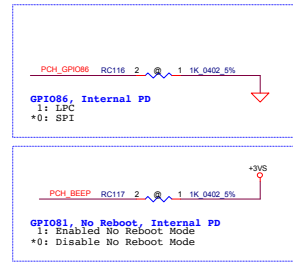


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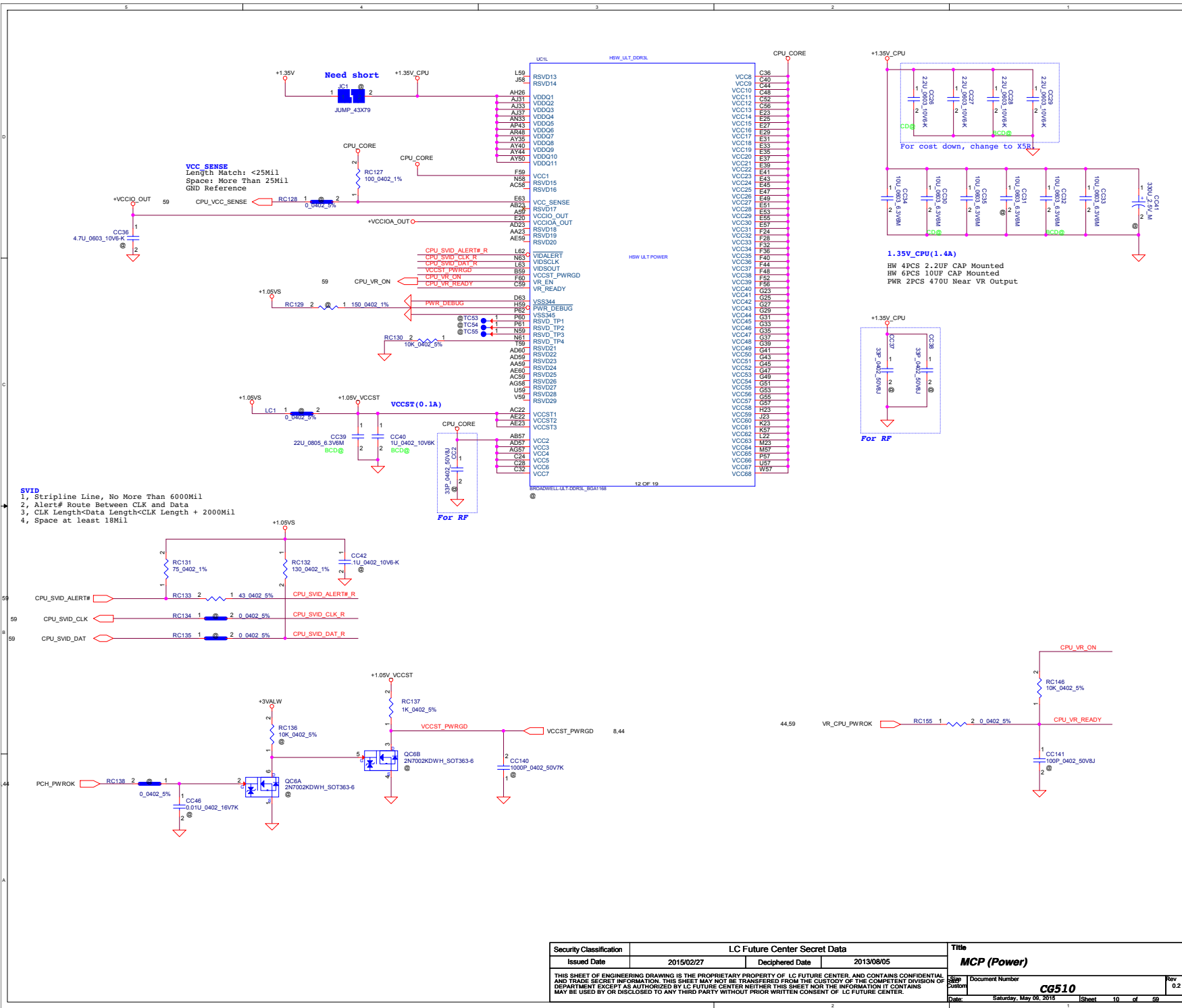
Title		MCP (Clock, PM)	
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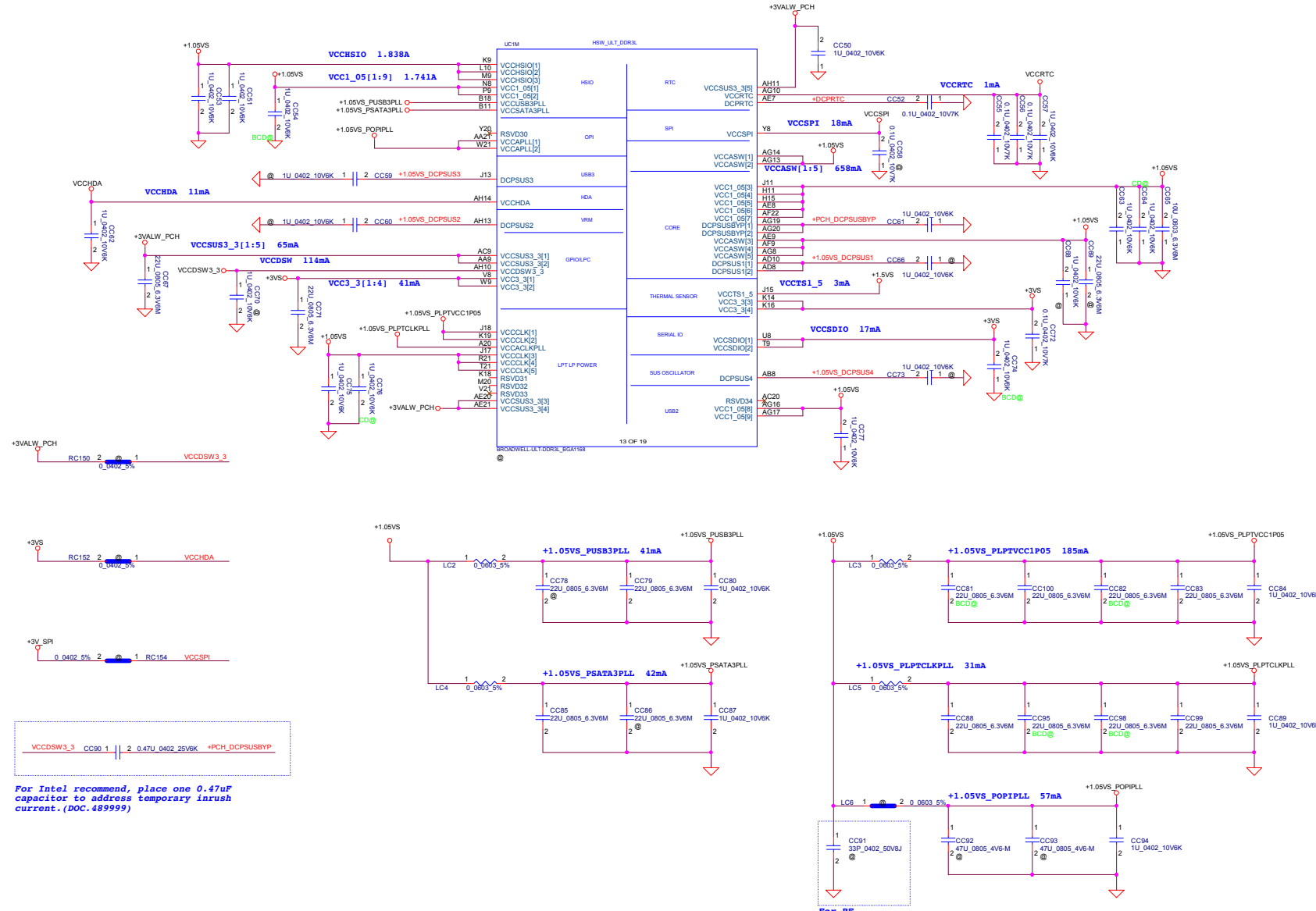
BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	BOARD_ID4	Description
1	X	X	X	X	D18 SKU
0	X	X	X	X	UNA SKU
X	1	X	X	X	15" SKU
X	0	X	X	X	14" SKU
X	X	0	0	0	H820P: K48G16440-8YX0
X	X	0	0	1	H820P: H57C6463CF9-P9A
X	X	0	1	0	H820P: H741K256N16L1-107H
X	X	0	1	1	H820P: K48G16440-8YX0
X	X	1	0	0	H840P: H57C6463JAN9-P9A
X	X	1	0	1	H840P: H741K512N168A-1251A



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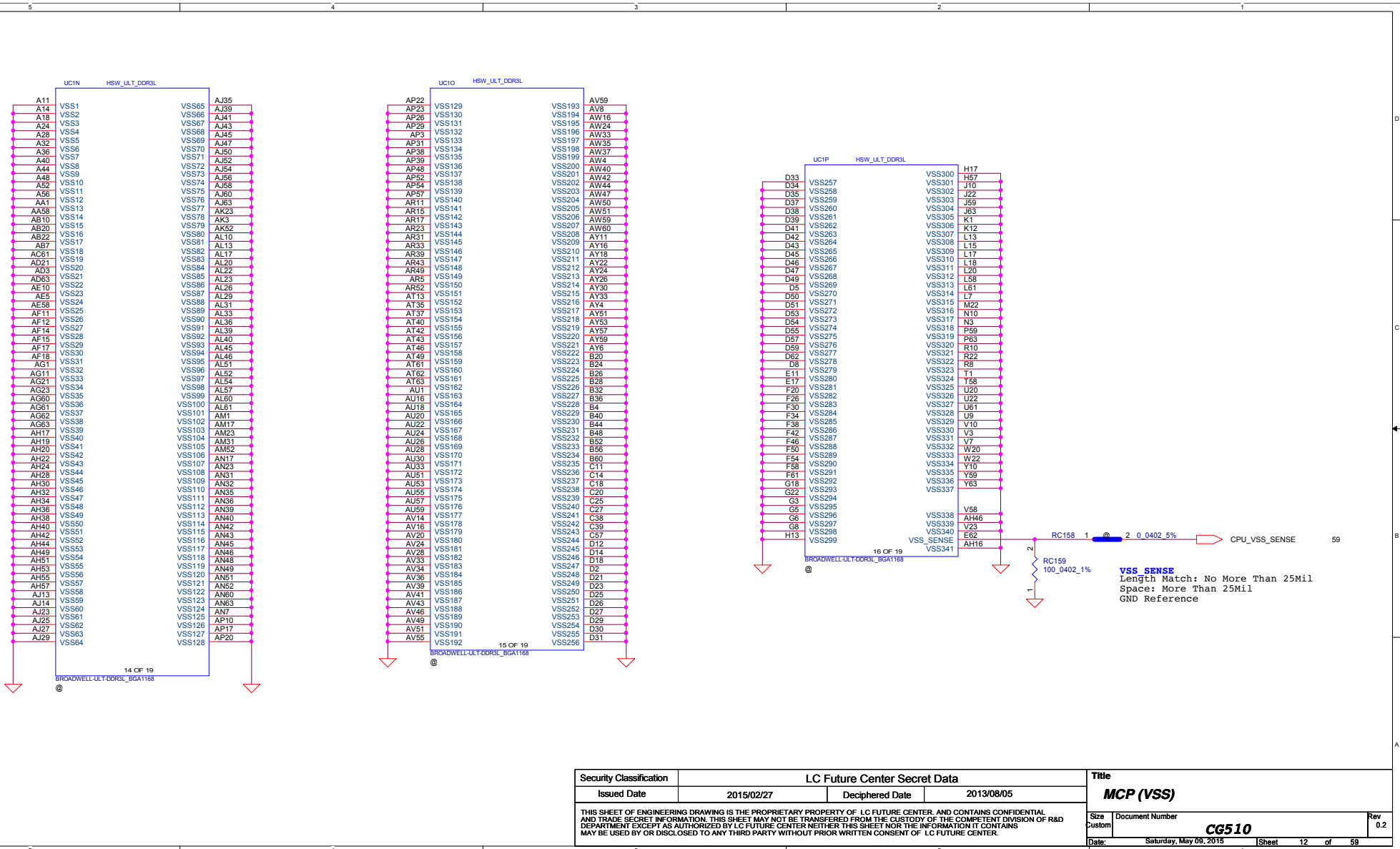


VCCDSW3_3 CC90 1 2 0.47U 0402 25V6K +PCH_DCPUSBYYP

For Intel recommend, place one 0.47uF capacitor to address temporary inrush current. (DOC. 489999)

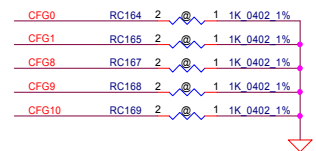
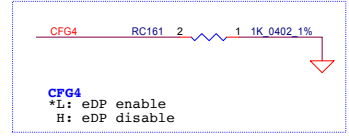
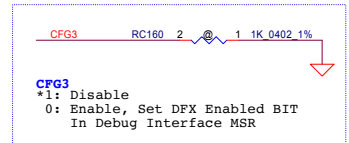
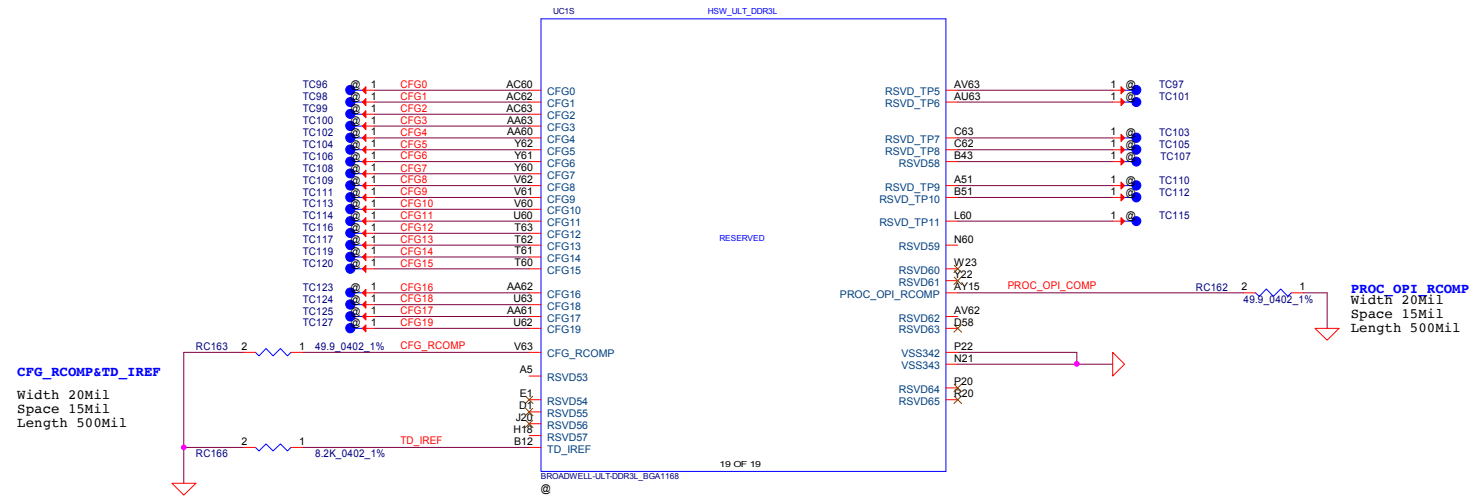
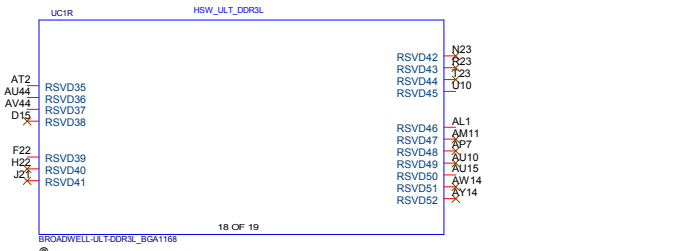
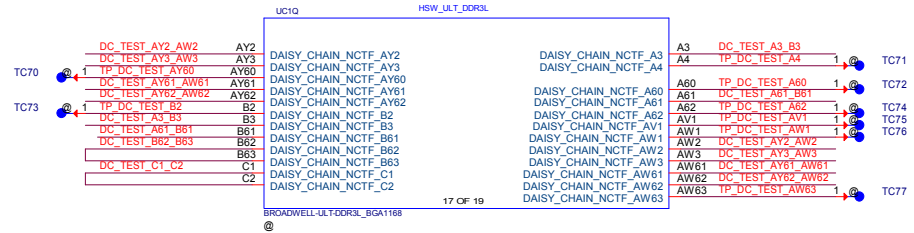
For RF

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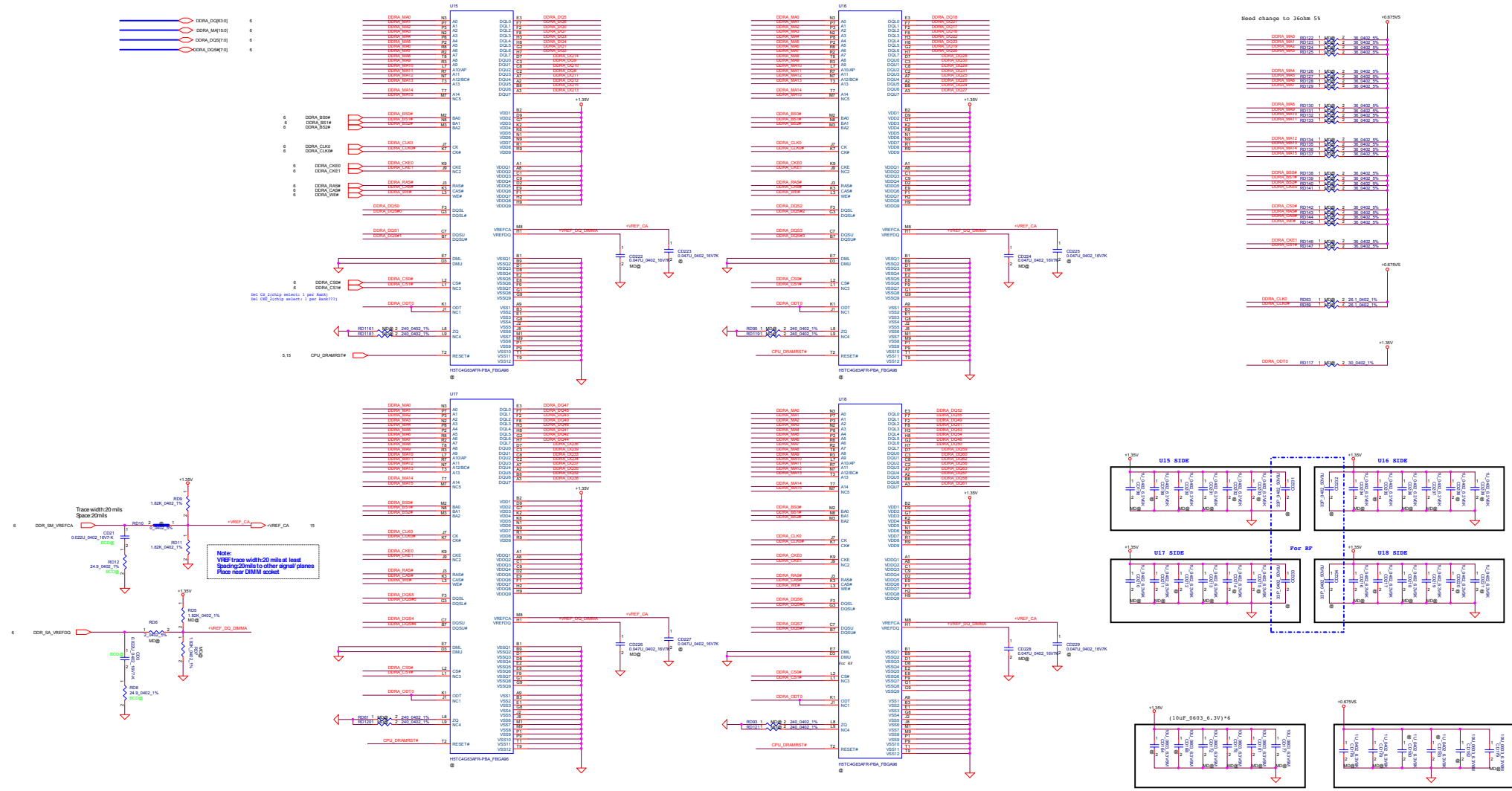
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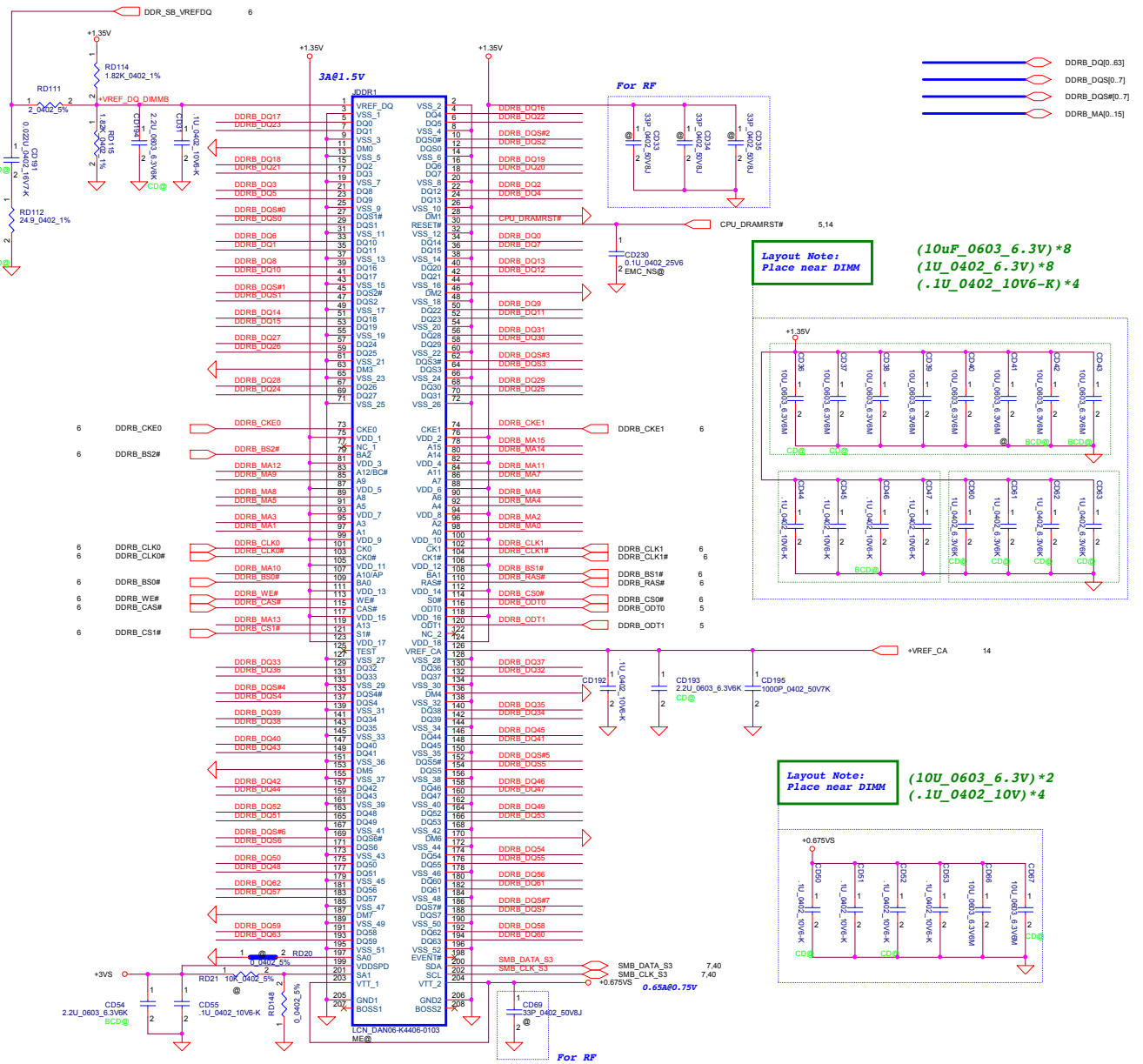
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Signal voltage level = 0.675 V
 PLACE TWO 4.7K RESISTORS CLOSE TO
 DENSE OR DIRM_VREF_CA + DIRM_VREF_DO
 Decoupling caps are needed; One 0.1uF placed close to VREF pins



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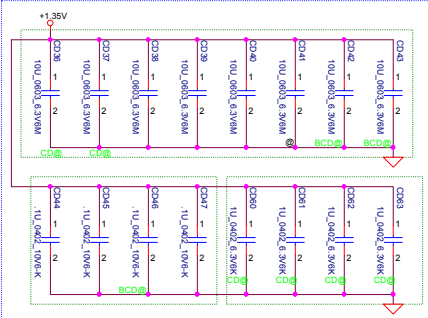
DDR3 SO-DIMM B



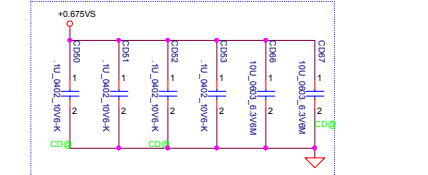
Swap Table

Pin Number	Pin Name	Net Name
5	DQ0	DDR3_DQ17
7	DQ1	DDR3_DQ23
15	DQ2	DDR3_DQ18
17	DQ3	DDR3_DQ24
4	DQ4	DDR3_DQ16
6	DQ5	DDR3_DQ22
16	DQ6	DDR3_DQ19
18	DQ7	DDR3_DQ25
10	DQS#0	DDR3_DQS#2
12	DQS0	DDR3_DQS2
21	DQ8	DDR3_DQ3
23	DQ9	DDR3_DQ5
33	DQ10	DDR3_DQ6
35	DQ11	DDR3_DQ1
22	DQ12	DDR3_DQ2
24	DQ13	DDR3_DQ4
34	DQ14	DDR3_DQ0
36	DQ15	DDR3_DQ7
27	DQS#1	DDR3_DQS#0
29	DQS1	DDR3_DQS0
39	DQ16	DDR3_DQ8
41	DQ17	DDR3_DQ10
51	DQ18	DDR3_DQ14
53	DQ19	DDR3_DQ15
40	DQ20	DDR3_DQ13
42	DQ21	DDR3_DQ12
50	DQ22	DDR3_DQ9
52	DQ23	DDR3_DQ11
45	DQS#2	DDR3_DQS#1
47	DQS2	DDR3_DQS1
57	DQ24	DDR3_DQ27
59	DQ25	DDR3_DQ26
67	DQ26	DDR3_DQ28
69	DQ27	DDR3_DQ24
56	DQ28	DDR3_DQ31
58	DQ29	DDR3_DQ30
68	DQ30	DDR3_DQ29
70	DQ31	DDR3_DQ31
62	DQS#3	DDR3_DQS#3
64	DQS3	DDR3_DQS3
129	DQ32	DDR3_DQ33
131	DQ33	DDR3_DQ36
141	DQ34	DDR3_DQ39
143	DQ35	DDR3_DQ38
130	DQ36	DDR3_DQ37
132	DQ37	DDR3_DQ32
140	DQ38	DDR3_DQ35
142	DQ39	DDR3_DQ34
135	DQS#4	DDR3_DQS#4
137	DQS4	DDR3_DQS4
147	DQ40	DDR3_DQ40
149	DQ41	DDR3_DQ43
157	DQ42	DDR3_DQ42
159	DQ43	DDR3_DQ44
146	DQ44	DDR3_DQ45
148	DQ45	DDR3_DQ41
158	DQ46	DDR3_DQ46
160	DQ47	DDR3_DQ47
152	DQS#5	DDR3_DQS#5
154	DQS5	DDR3_DQS5
163	DQ48	DDR3_DQ52
165	DQ49	DDR3_DQ51
175	DQ50	DDR3_DQ50
177	DQ51	DDR3_DQ48
164	DQ52	DDR3_DQ49
166	DQ53	DDR3_DQ53
174	DQ54	DDR3_DQ54
176	DQ55	DDR3_DQ55
169	DQS#6	DDR3_DQS#6
171	DQS6	DDR3_DQS6
181	DQ56	DDR3_DQ62
183	DQ57	DDR3_DQ57
191	DQ58	DDR3_DQ59
193	DQ59	DDR3_DQ62
190	DQ60	DDR3_DQ56
182	DQ61	DDR3_DQ61
192	DQ62	DDR3_DQ58
194	DQ63	DDR3_DQ60
186	DQS#7	DDR3_DQS#7
188	DQS7	DDR3_DQS7

Layout Note: Place near DIMM
 $(10\mu F_{0603_6.3V}) * 8$
 $(1U_{0402_6.3V}) * 8$
 $(.1U_{0402_10V6-K}) * 4$



Layout Note: Place near DIMM
 $(10U_{0603_6.3V}) * 2$
 $(.1U_{0402_10V}) * 4$



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B				B
A				A

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N15x GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	I/O	-	System side PCIe reset Monitor
GPIO9	I/O	N/A	2.2K Pull-up
GPIO10	OUT	N/A	
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16		N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT		GPU PCIe self-reset control
OVERT	OUT		Active Low Thermal Catastrophic Over Temperature

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

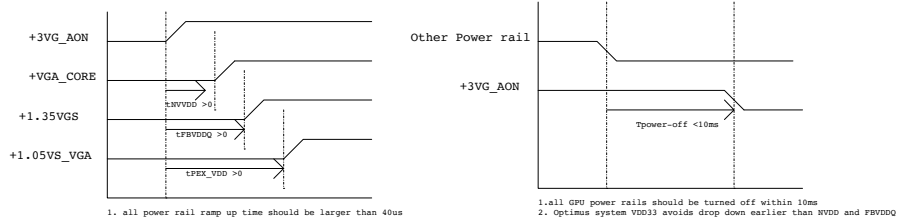
Products	GPU	Mem	NVCLK	NVVDD			FBVDD		FBVDD0		PCI Express		I/O and PLLVDD		Other		
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	
N14X 128bit IGB DDR3	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

N15x Multi-level Straps

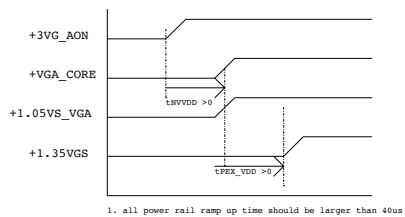
Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

N15V-GM Power Sequence



N15S-GT Power Sequence



N15x Binary Straps

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

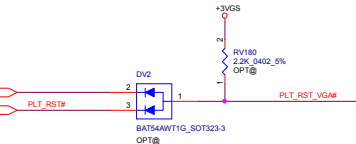
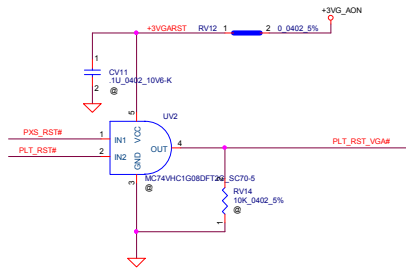
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- 9 PCIe_CRX_GTX_N0..3
- 9 PCIe_CRX_GTX_P0..3
- 9 PCIe_CRX_C_GRX_N0..3
- 9 PCIe_CRX_C_GRX_P0..3

- 7.44 EC_SMB_CK2 RV7 10R7K 2 0.0402 5% VGA_SMB_CK2
- 7.44 EC_SMB_DA2 RV9 10R7K 2 0.0402 5% VGA_SMB_DA2

PU AT EC SIDE, +3VS AND 4.7K

- | | | | | | | | | | |
|-----------------|------|-------|---|----|--------|------|-------------------|------|-----------|
| PCIe_CRX_GTX_P0 | CV10 | OPT@1 | 2 | 1U | 0.0402 | 10%K | PCIe_CRX_C_GTX_P0 | ACD9 | PEX_TX0 |
| PCIe_CRX_GTX_N0 | CV13 | OPT@1 | 2 | 1U | 0.0402 | 10%K | PCIe_CRX_C_GTX_N0 | ABG0 | PEX_TX0_N |
| PCIe_CRX_GTX_P1 | CV8 | OPT@1 | 2 | 1U | 0.0402 | 10%K | PCIe_CRX_C_GTX_P1 | AD10 | PEX_TX1 |
| PCIe_CRX_GTX_N1 | CV9 | OPT@1 | 2 | 1U | 0.0402 | 10%K | PCIe_CRX_C_GTX_N1 | AD11 | PEX_TX1_N |
| PCIe_CRX_GTX_P2 | CV6 | OPT@1 | 2 | 1U | 0.0402 | 10%K | PCIe_CRX_C_GTX_P2 | AD14 | PEX_TX2 |
| PCIe_CRX_GTX_N2 | CV7 | OPT@1 | 2 | 1U | 0.0402 | 10%K | PCIe_CRX_C_GTX_N2 | AD17 | PEX_TX2_N |
| PCIe_CRX_GTX_P3 | CV4 | OPT@1 | 2 | 1U | 0.0402 | 10%K | PCIe_CRX_C_GTX_P3 | AD18 | PEX_TX3 |
| PCIe_CRX_GTX_N3 | CV5 | OPT@1 | 2 | 1U | 0.0402 | 10%K | PCIe_CRX_C_GTX_N3 | AD19 | PEX_TX3_N |



Differential signal

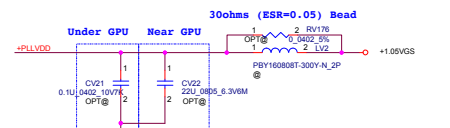
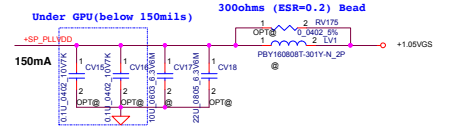
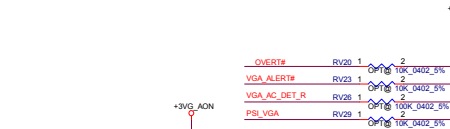
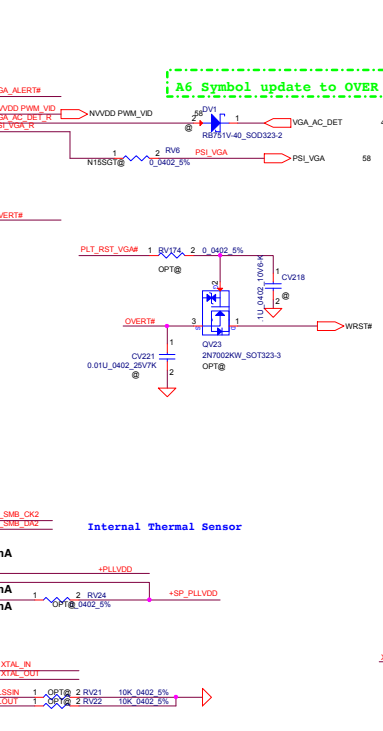
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|-------------|------|--------------|
| CLK_POE_GPU | AE3 | PEX_REFCLK |
| CLK_POE_GPU | AE5 | PEX_REFCLK_N |
| CLK_POE_GPU | ACD8 | PEX_CLKREQ_N |
| PEX_TX0_OUT | AF22 | PEX_TX0_OUT |
| PEX_TX0_OUT | AC29 | PEX_TX0_OUT |
| PLT_RSTVGA# | AC7 | PEX_RST_N |
| PLT_RSTVGA# | AF25 | PEX_TERMPP |

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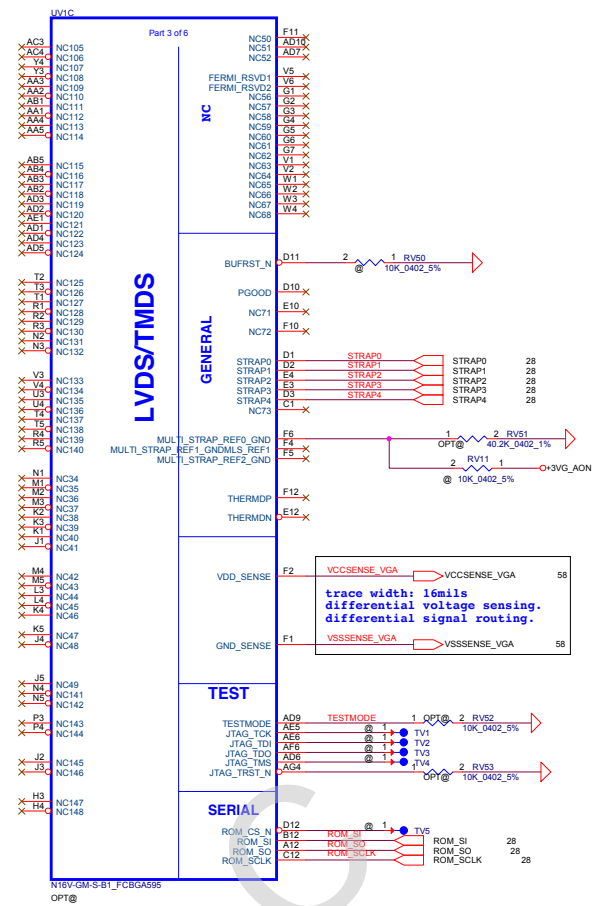
GPU_CLKREQ#

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|-------------------|-------|-----------|
| PCIe_CRX_C_GRX_P0 | AG8 | PEX_RX0 |
| PCIe_CRX_C_GRX_N0 | AG7 | PEX_RX0_N |
| PCIe_CRX_C_GRX_P1 | AE7 | PEX_RX1 |
| PCIe_CRX_C_GRX_N1 | AE6 | PEX_RX1_N |
| PCIe_CRX_C_GRX_P2 | AF9 | PEX_RX2 |
| PCIe_CRX_C_GRX_N2 | AF8 | PEX_RX2_N |
| PCIe_CRX_C_GRX_P3 | AG10 | PEX_RX3 |
| PCIe_CRX_C_GRX_N3 | AG9 | PEX_RX3_N |
| NC81 | NC81 | NC81 |
| NC82 | NC82 | NC82 |
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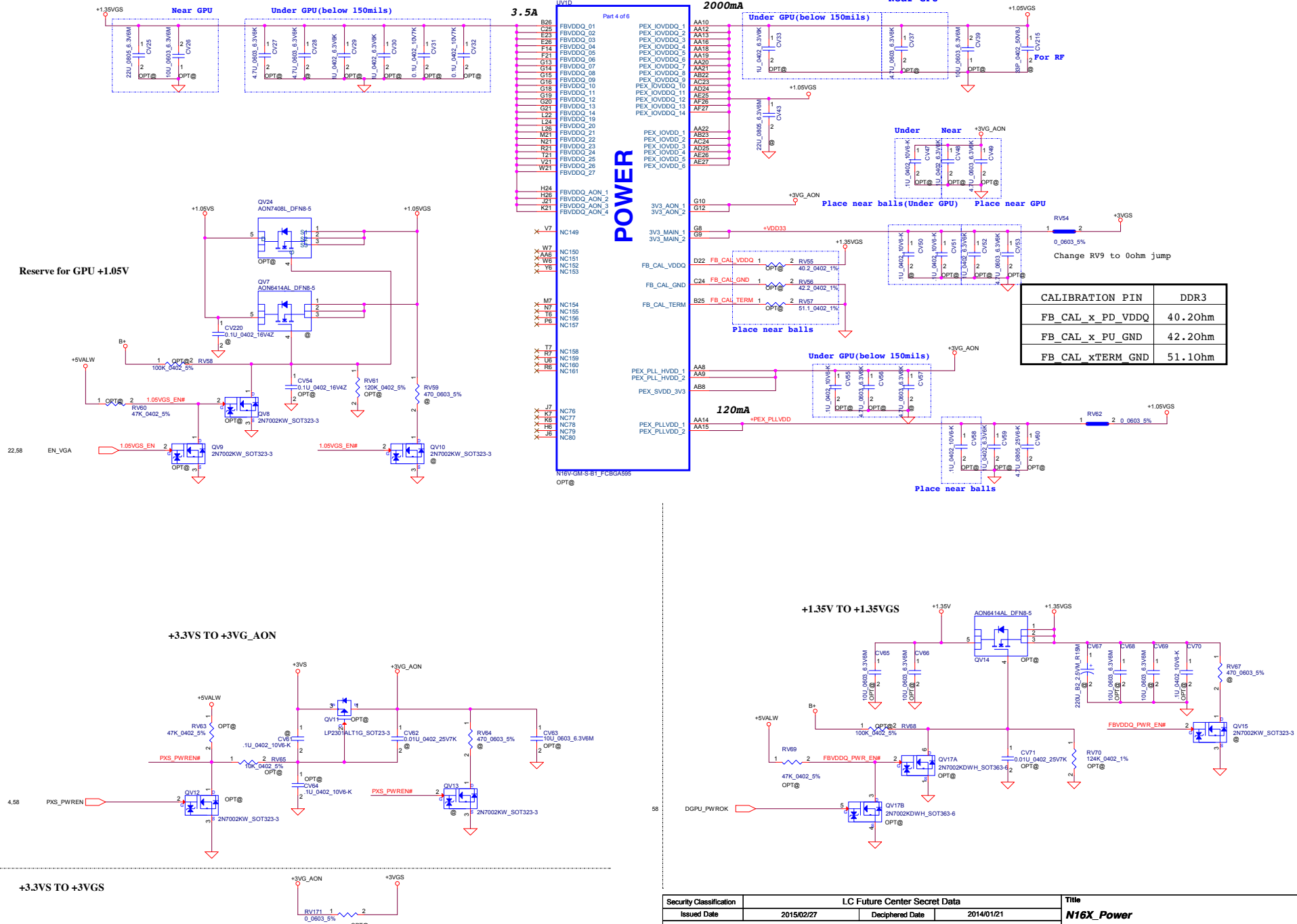
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|-------|-------|--------------|
| GPIO | C6 | GPIO0 |
| GPIO | B2 | GPIO1 |
| GPIO | C7 | GPIO2 |
| GPIO | CF | GPIO3 |
| GPIO | AD | GPIO4 |
| GPIO | AE | GPIO5 |
| GPIO | BE | GPIO6 |
| GPIO | BF | GPIO7 |
| GPIO | CF | GPIO8 |
| GPIO | CF | GPIO9 |
| GPIO | CF | GPIO10 |
| GPIO | D7 | GPIO11 |
| GPIO | B1 | GPIO12 |
| GPIO | B1 | GPIO13 |
| GPIO | D5 | GPIO14 |
| GPIO | D4 | GPIO15 |
| GPIO | DC | GPIO16 |
| GPIO | DD | GPIO17 |
| GPIO | DE | GPIO18 |
| GPIO | DF | GPIO19 |
| GPIO | CH | GPIO20 |
| GPIO | CH | GPIO21 |
| OVERT | A8 | OVERT# |
| OVERT | AB8 | OVERT# |
| OVERT | AE3 | OVERT# |
| OVERT | AE4 | OVERT# |
| OVERT | W5 | OVERT# |
| OVERT | NC102 | OVERT# |
| OVERT | NC103 | OVERT# |
| OVERT | NC104 | OVERT# |
| I2C | B7 | I2CA_SCL |
| I2C | AD | I2CA_SDA |
| I2C | CB | I2CB_SCL |
| I2C | CB | I2CB_SDA |
| I2C | AB | I2CC_SCL |
| I2C | AB | I2CC_SDA |
| I2C | D9 | I2CS_SCL |
| I2C | D8 | I2CS_SDA |
| CLK | L8 | CORE_PLLVDD |
| CLK | M6 | SP_PLLVDD |
| CLK | N8 | VID_PLLVDD |
| CLK | C11 | XTAL_IN |
| CLK | B10 | XTAL_OUT |
| CLK | A10 | XTAL_SSIN |
| CLK | C10 | XTAL_OUTBUFF |



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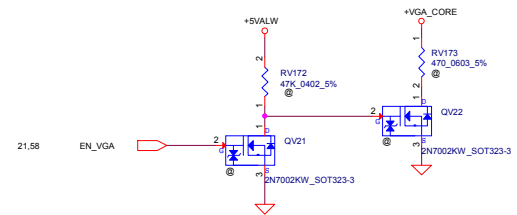
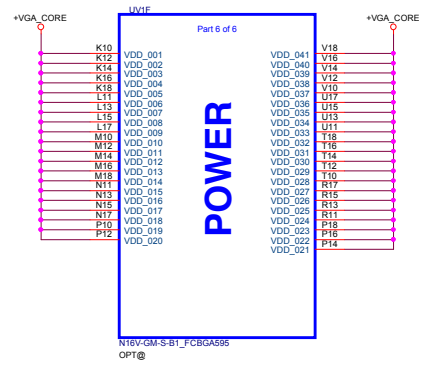
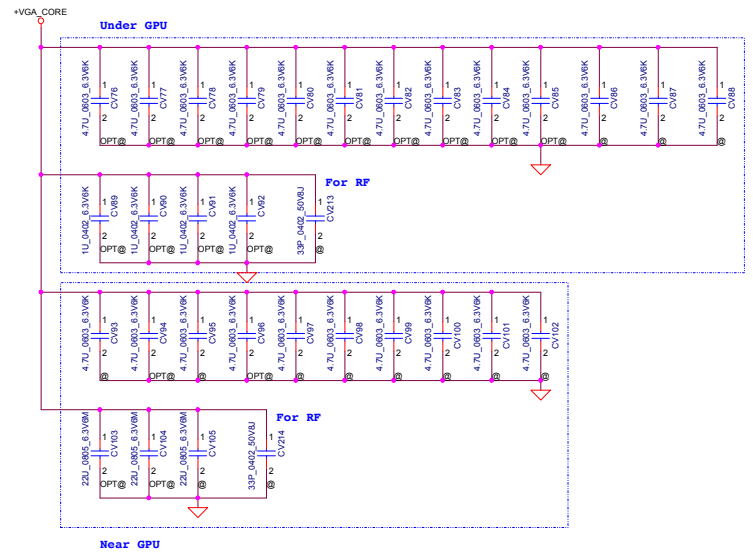
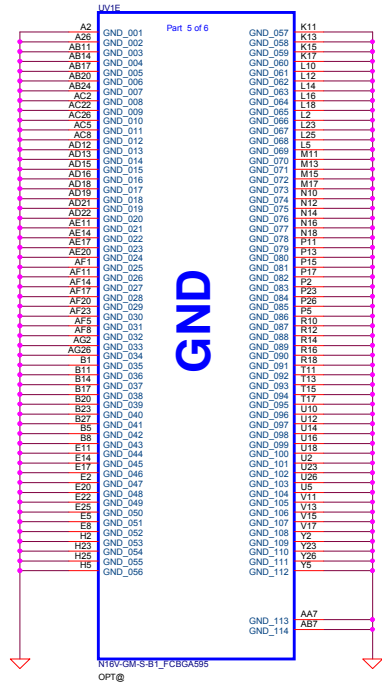


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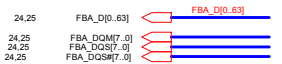


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Title		CG510
N16X_Power		
Sheet	Document Number	Rev
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Date	Saturday, May 08, 2015	13Sheet 21 of 60

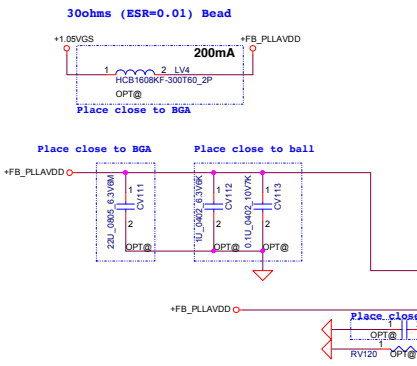
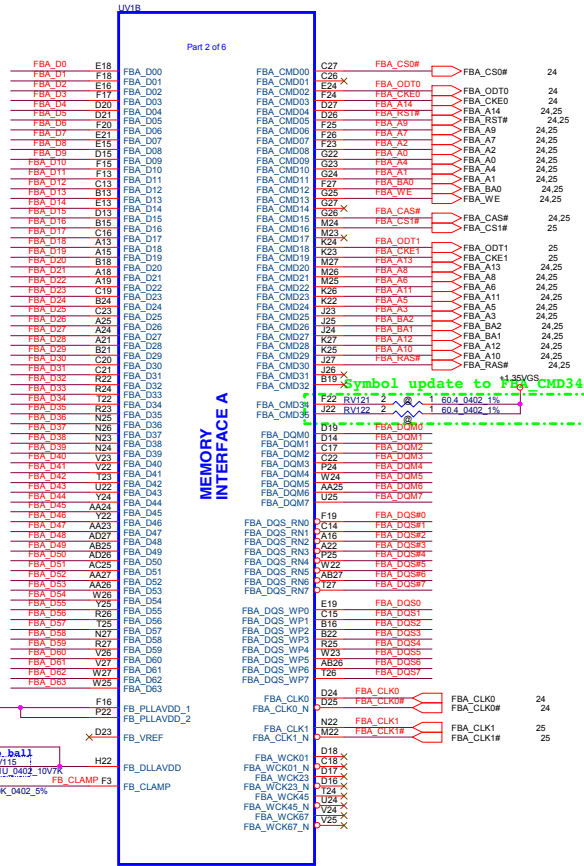


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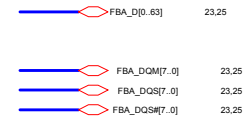
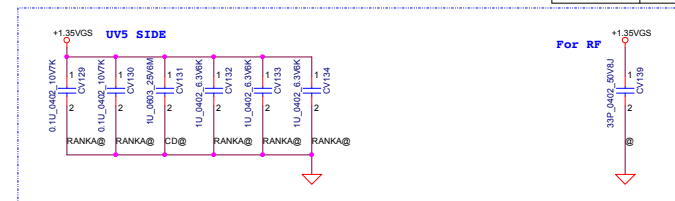
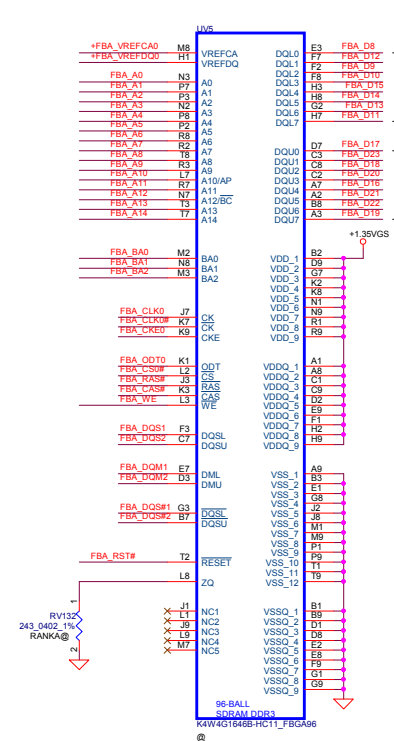
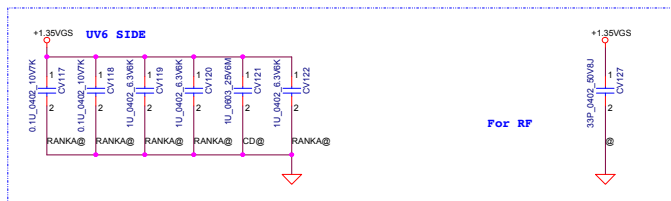
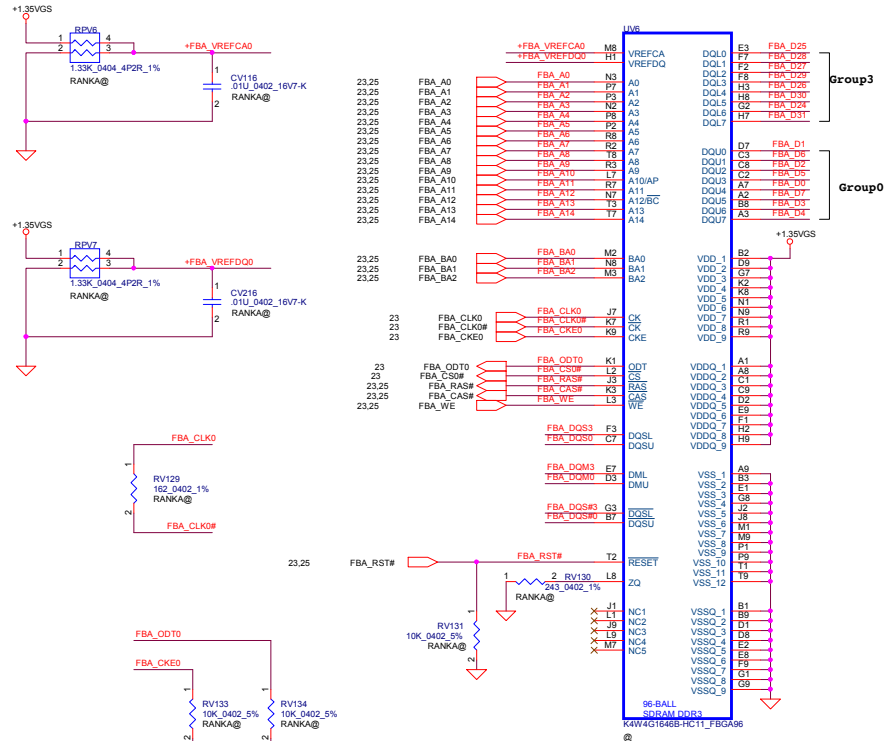
CMD mapping mod Mode D

Address	Rank0	
	0..31	32..63
Fbx_CMD0	CS0#	
Fbx_CMD1		
Fbx_CMD2	ODT0	
Fbx_CMD3	CKE0	
Fbx_CMD4	A14	A14
Fbx_CMD5	RST	RST
Fbx_CMD6	A9	A9
Fbx_CMD7	A7	A7
Fbx_CMD8	A2	A2
Fbx_CMD9	A0	A0
Fbx_CMD10	A4	A4
Fbx_CMD11	A1	A1
Fbx_CMD12	BA0	BA0
Fbx_CMD13	WE	WE
Fbx_CMD14	A15	A15
Fbx_CMD15	CAS#	CAS#
Fbx_CMD16		CS1#
Fbx_CMD17		
Fbx_CMD18		ODT1
Fbx_CMD19		CKE1
Fbx_CMD20	A13	A13
Fbx_CMD21	A8	A8
Fbx_CMD22	A6	A6
Fbx_CMD23	A11	A11
Fbx_CMD24	A5	A5
Fbx_CMD25	A3	A3
Fbx_CMD26	BA2	BA2
Fbx_CMD27	BA1	BA1
Fbx_CMD28	A12	A12
Fbx_CMD29	A10	A10
Fbx_CMD30	RAS#	RAS#
Fbx_CMD31		
Fbx_CMD32		
Fbx_CMD33		
Fbx_CMD34	DBG0	
Fbx_CMD35	DBG1	



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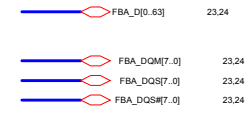
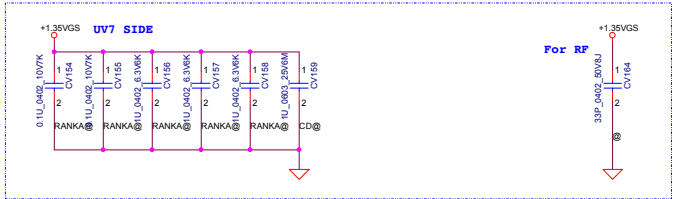
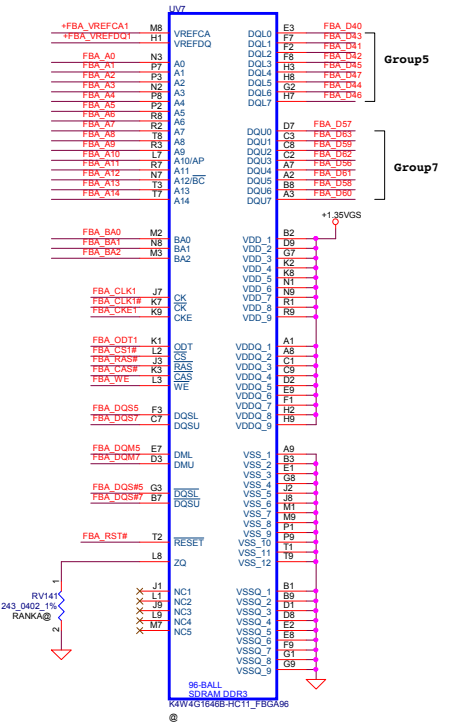
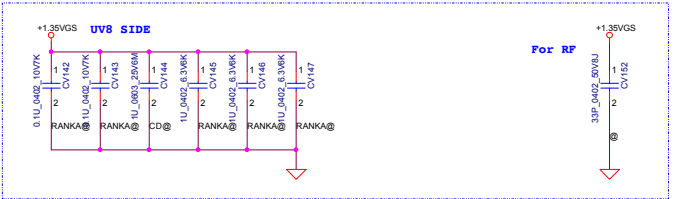
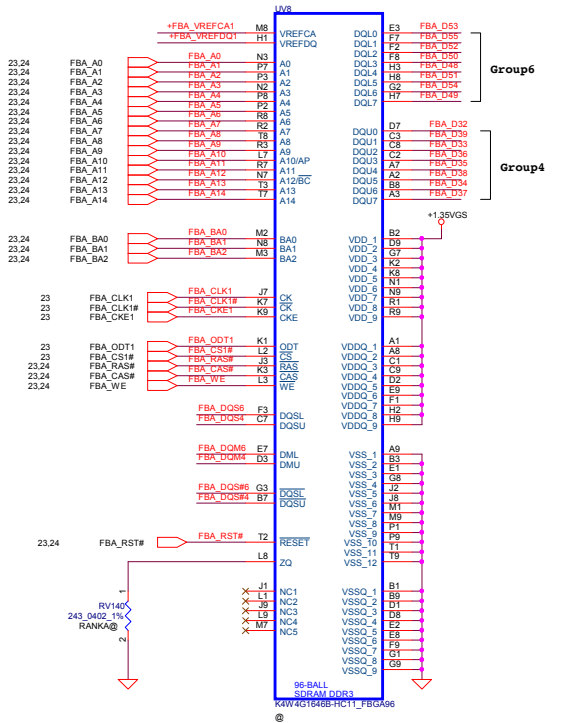
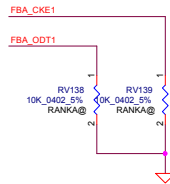
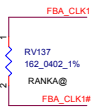
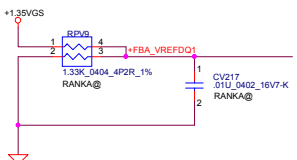
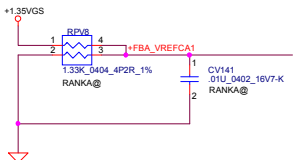
at least 16 mils width(optimal)
20 mils spacing to other signals /planes



CMD mapping mod Mode D

Address	Rank0	
	0..31	32..63
FBX_CMD0	CS0#	
FBX_CMD1		
FBX_CMD2	ODT0	
FBX_CMD3	CKE0	
FBX_CMD4	A14	A14
FBX_CMD5	RST	RST
FBX_CMD6	A9	A9
FBX_CMD7	A7	A7
FBX_CMD8	A2	A2
FBX_CMD9	A0	A0
FBX_CMD10	A4	A4
FBX_CMD11	A1	A1
FBX_CMD12	BA0	BA0
FBX_CMD13	WE	WE
FBX_CMD14	A15	A15
FBX_CMD15	CAS#	CAS#
FBX_CMD16	CS1#	
FBX_CMD17		
FBX_CMD18	ODT1	
FBX_CMD19	CKE1	
FBX_CMD20	A13	A13
FBX_CMD21	A8	A8
FBX_CMD22	A6	A6
FBX_CMD23	A11	A11
FBX_CMD24	A5	A5
FBX_CMD25	A3	A3
FBX_CMD26	BA2	BA2
FBX_CMD27	BA1	BA1
FBX_CMD28	A12	A12
FBX_CMD29	A10	A10
FBX_CMD30	RAS#	RAS#
FBX_CMD31		
FBX_CMD32		
FBX_CMD33		
FBX_CMD34	DBG0	
FBX_CMD35	DBG1	

at least 16 mils width(optimal)
20 mils spacing to other signals/planes



CMD mapping mod Mode D

Address	Rank0	
FBx_CMD0	0..31	32..63
FBx_CMD1	CS0#	
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FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE	WE
FBx_CMD14	A15	A15#
FBx_CMD15	CAS#	CAS#
FBx_CMD16	CS1#	
FBx_CMD17		
FBx_CMD18	ODT1	
FBx_CMD19	CKE1	
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#
FBx_CMD31		
FBx_CMD32		
FBx_CMD33		
FBx_CMD34	DBG0	
FBx_CMD35	DBG1	

6 4 3 2 1

D

D

C

C

B

B

A

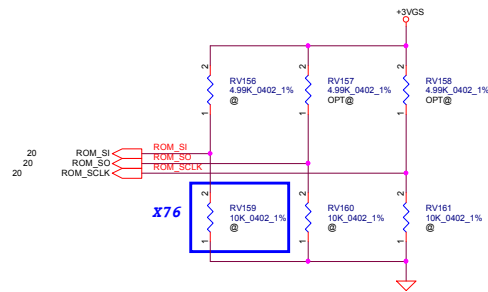
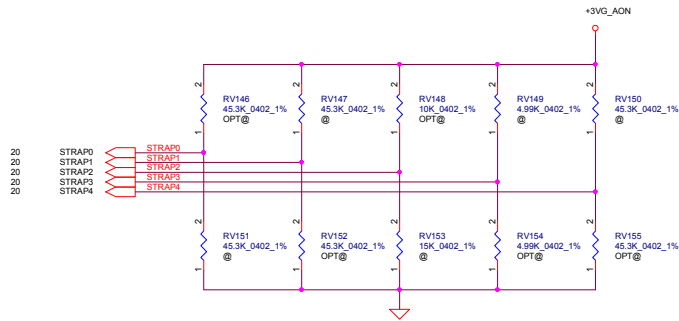
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Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50kOhm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
SD0344916J		
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
SD0344928J		
30.1K	1101	0101
SD0344928J		
34.8K	1110	0110
45.3K	1111	0111
SD03445328J		

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

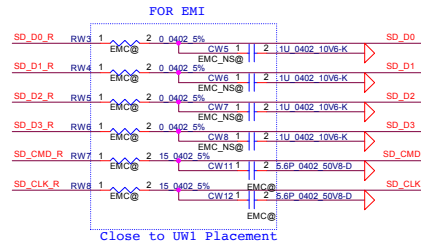
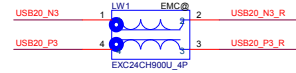
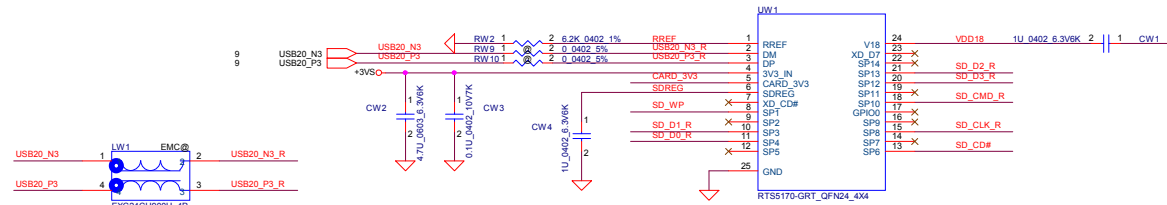
X76

GPU	FB Memory (DDR3L)	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4		
N16V-GM	H5TC4G63AFR-11C	0xE	PU 4.99K	PU 4.99K	PU 45.3K	PD 45.3K	PU 10K	PD 4.99K	PD 45.3K		
	Hynix 900MHz	256M x 16								PU 34.8K	
	Micron 900MHz	M741J256M16HA-093G:E								0xD	PU 30.1K
	H5TC2G63FFR-11C	0xB									
	Hynix 900MHz	128M x 16								0xB	PU 20K
	Micron 900MHz	M741J128M16JT-093G								0x8	PU 4.99K
	Samsung 900MHz	K4W2G1646Q-BC1A								0x7	
		128M x 16								0x7	PD 45.3K

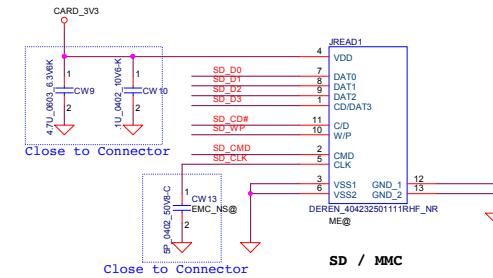
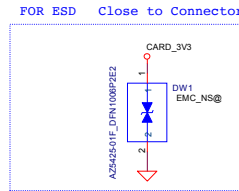
VRAM	I76	VRAM P/N
Samsung	X7606012101	SA000055H40
Micron	X7606012001	SA00005M120
Hynix	X7606012002	SA00005VS00

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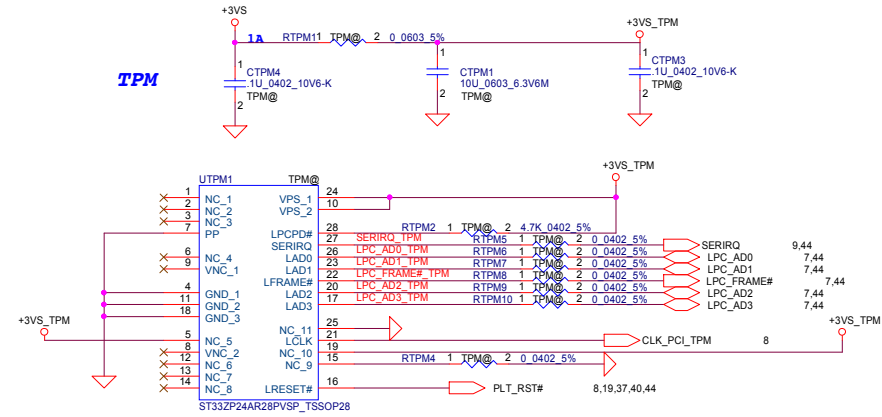


CW11,CW12 need to change 5.6pf CAP as EMC request



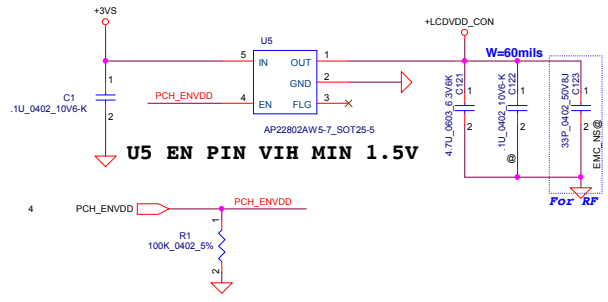
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Date: Saturday, May 09, 2015			Rev 0.2

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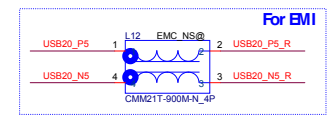
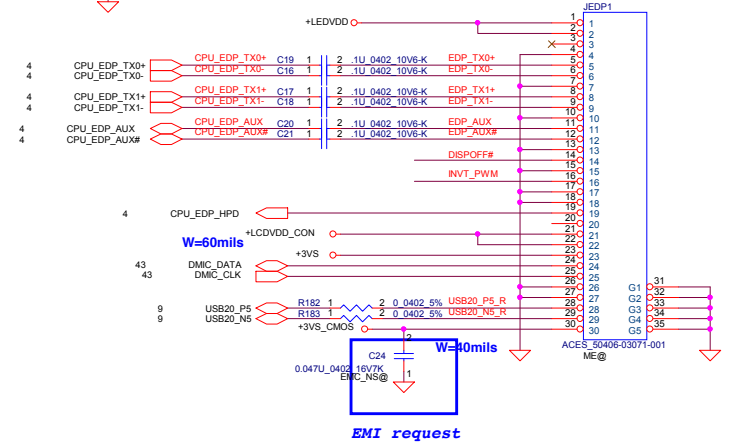
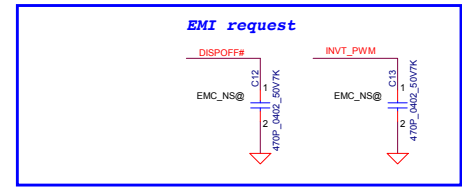
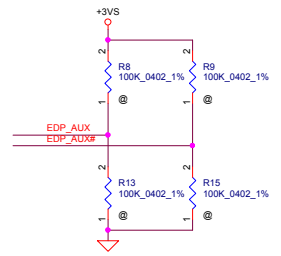
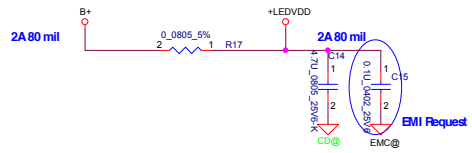
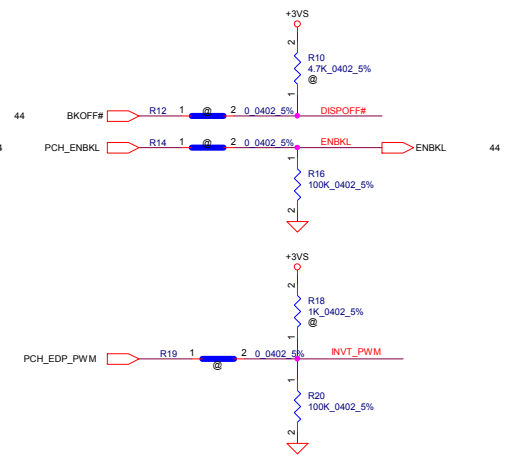
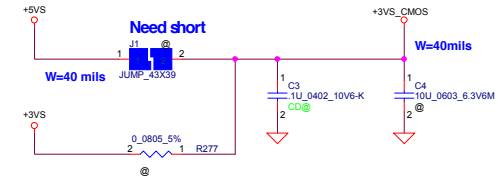


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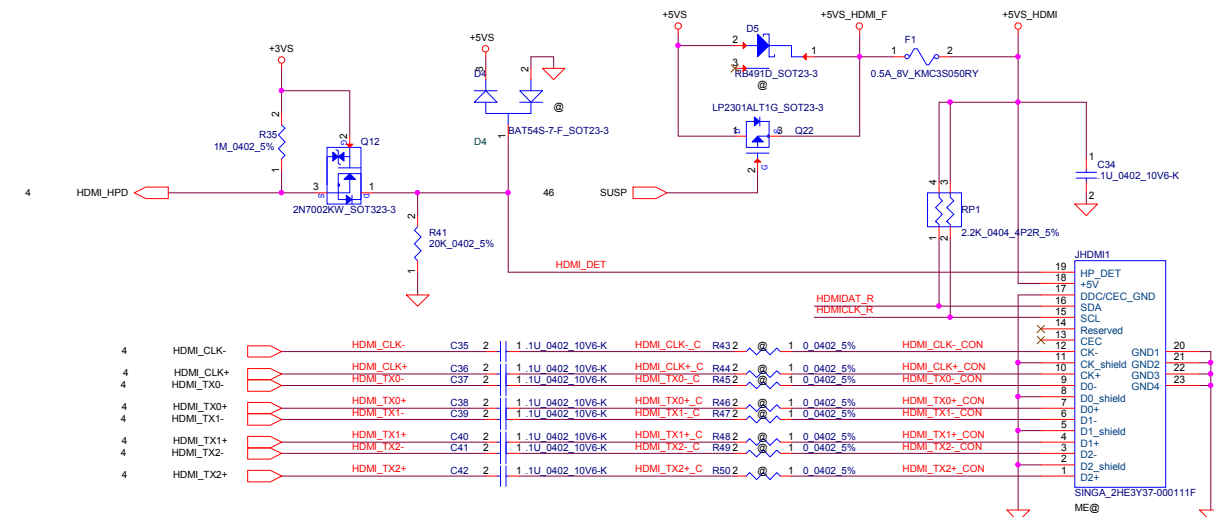
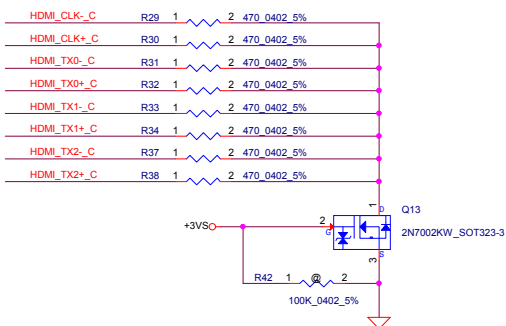
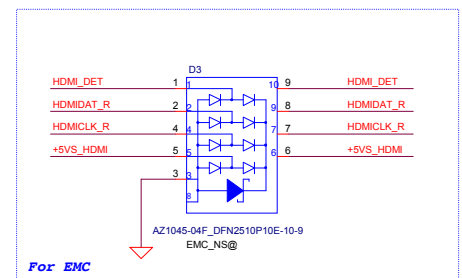
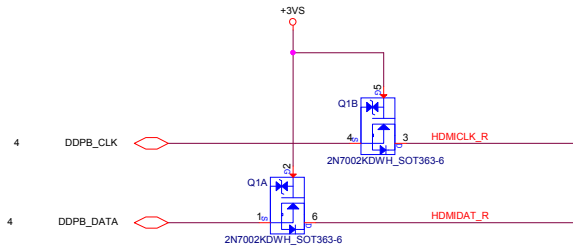
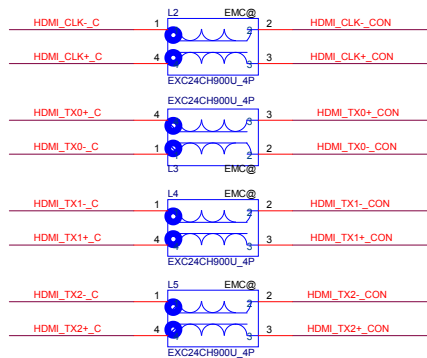
LCD POWER CIRCUIT



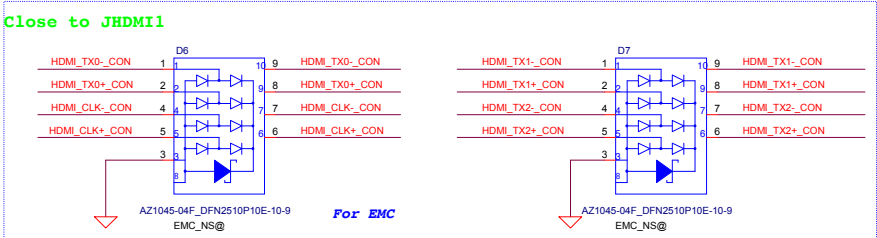
CMOS Camera



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Issued Date	2015/02/27	Deciphered Date	2013/08/05
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Date			Monday, May 11, 2015
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4	HDMI_CLK-	HDMI_CLK-	C35	2	1.1U_0402_10V6-K	HDMI_CLK-_C	R43	2	@	1	0.0402_5%	HDMI_CLK-_CON
4	HDMI_CLK+	HDMI_CLK+	C38	2	1.1U_0402_10V6-K	HDMI_CLK+_C	R44	2	@	1	0.0402_5%	HDMI_CLK+_CON
4	HDMI_TX0-	HDMI_TX0-	C37	2	1.1U_0402_10V6-K	HDMI_TX0-_C	R45	2	@	1	0.0402_5%	HDMI_TX0-_CON
4	HDMI_TX0+	HDMI_TX0+	C38	2	1.1U_0402_10V6-K	HDMI_TX0+_C	R46	2	@	1	0.0402_5%	HDMI_TX0+_CON
4	HDMI_TX1-	HDMI_TX1-	C39	2	1.1U_0402_10V6-K	HDMI_TX1-_C	R47	2	@	1	0.0402_5%	HDMI_TX1-_CON
4	HDMI_TX1+	HDMI_TX1+	C40	2	1.1U_0402_10V6-K	HDMI_TX1+_C	R48	2	@	1	0.0402_5%	HDMI_TX1+_CON
4	HDMI_TX2-	HDMI_TX2-	C41	2	1.1U_0402_10V6-K	HDMI_TX2-_C	R49	2	@	1	0.0402_5%	HDMI_TX2-_CON
4	HDMI_TX2+	HDMI_TX2+	C42	2	1.1U_0402_10V6-K	HDMI_TX2+_C	R50	2	@	1	0.0402_5%	HDMI_TX2+_CON



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Issued Date	2015/02/27	Deciphered Date	2013/08/05	Blank	
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				Rev 0.2	Sheet 35 of 59

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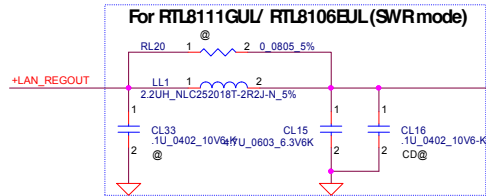
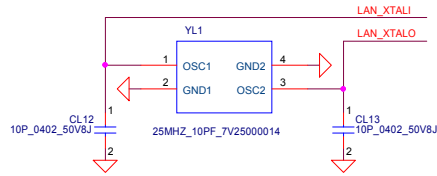
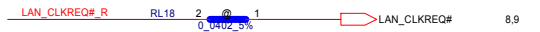
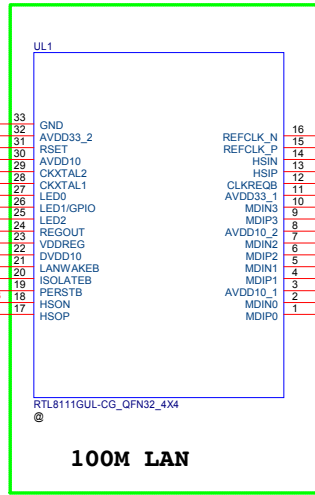
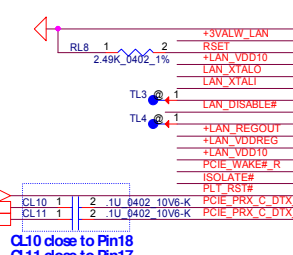
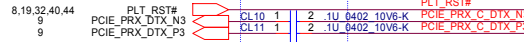
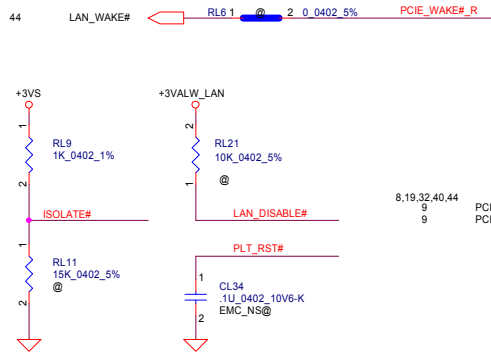
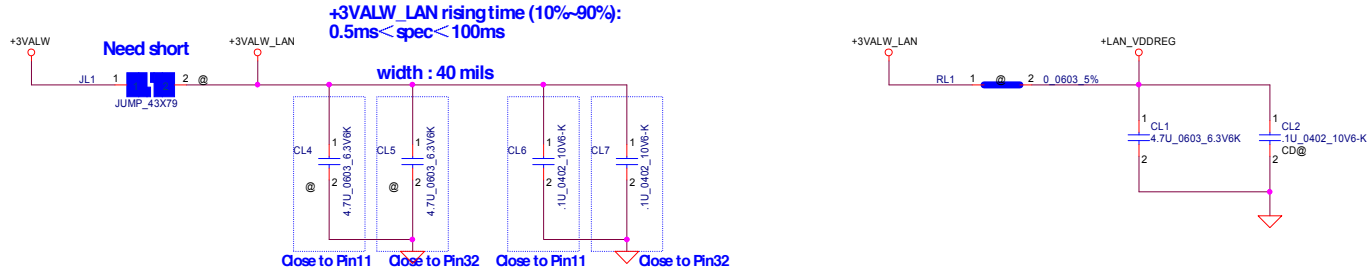
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Issued Date	2015/02/27	Deciphered Date	2013/08/05	Blank	
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				Custom	CG510
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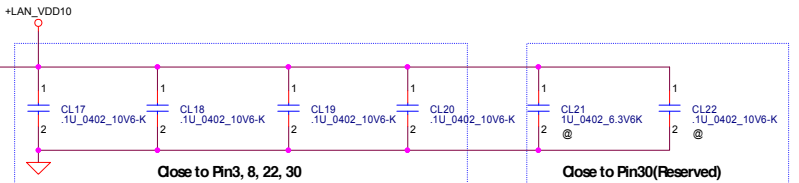
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+3VALW TO +3VALW_LAN

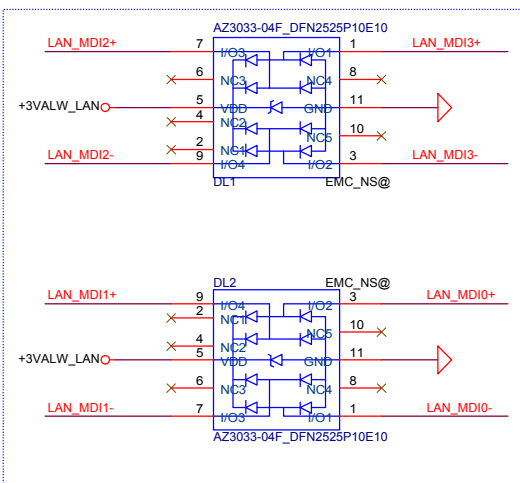


Layout Note: LL1 must be within 200mil to Pin24.
CL15, CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

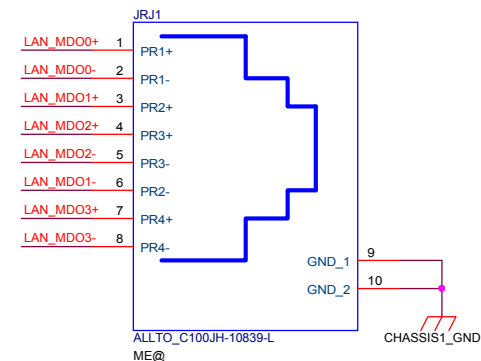
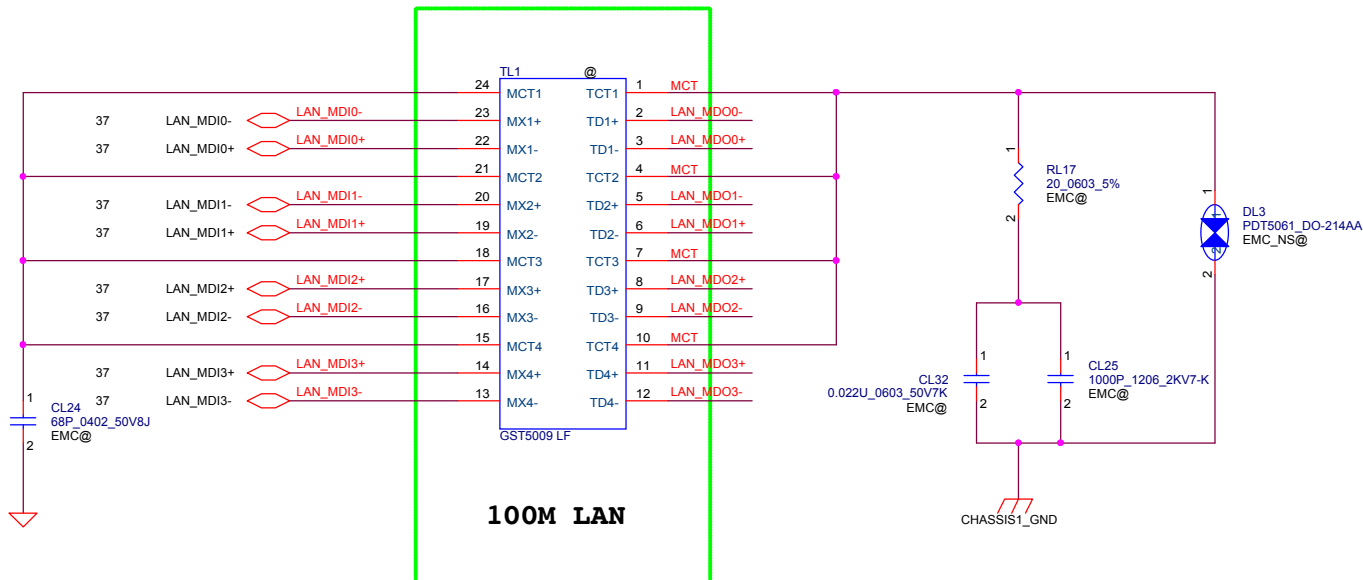
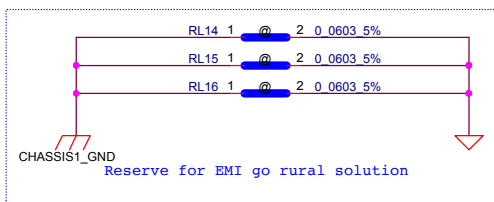


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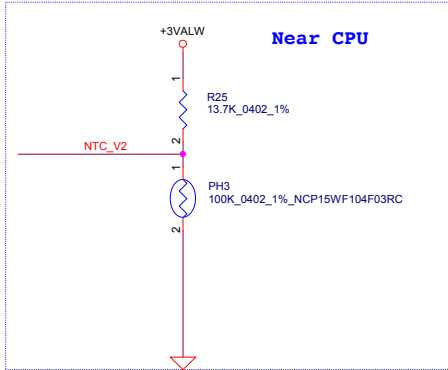
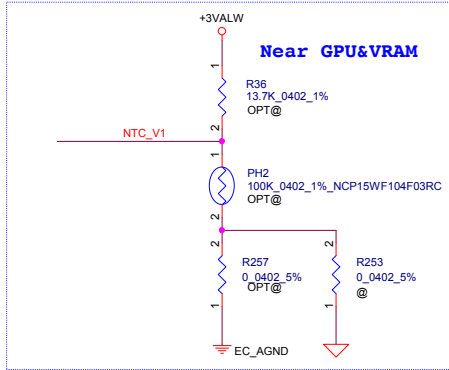
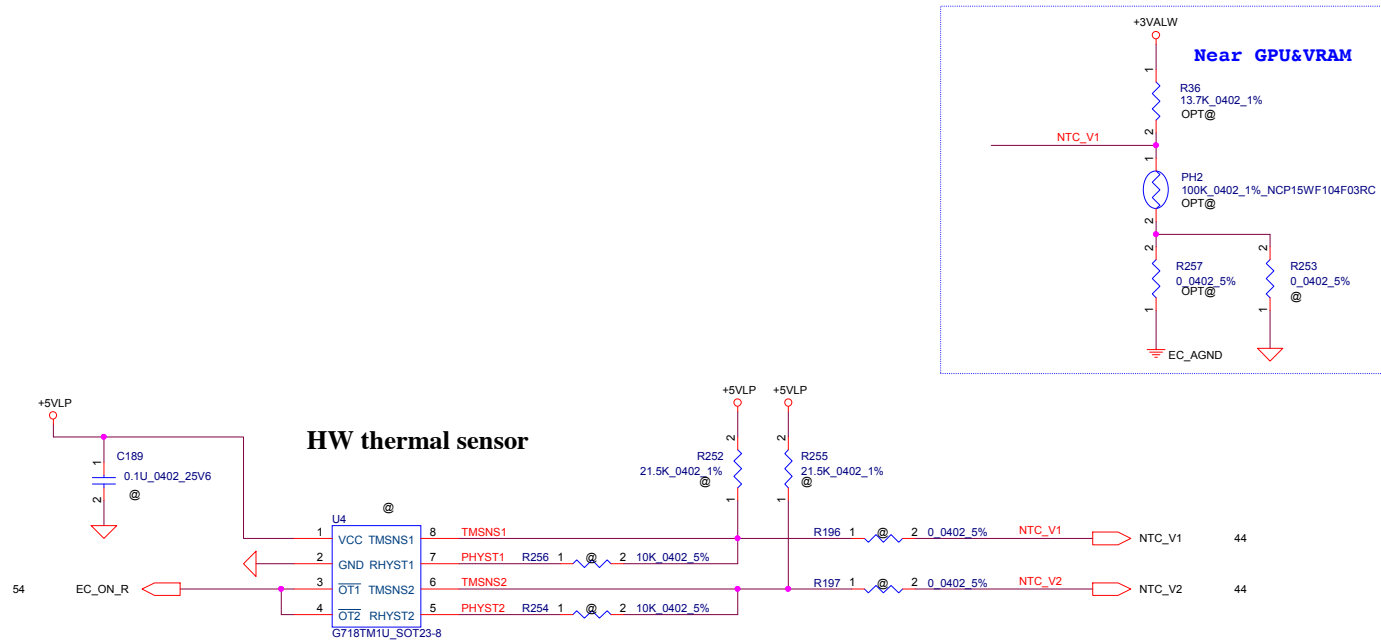
DL1/DL2
1'S PN:SC30003M00



Place Close to TL1



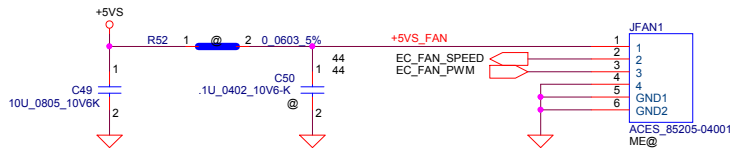
Security Classification	LC Future Center Secret Data		Title
Issued Date	2015/02/27	Deciphered Date	2013/08/05
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for layout optimized, change the EC_AGND to GND

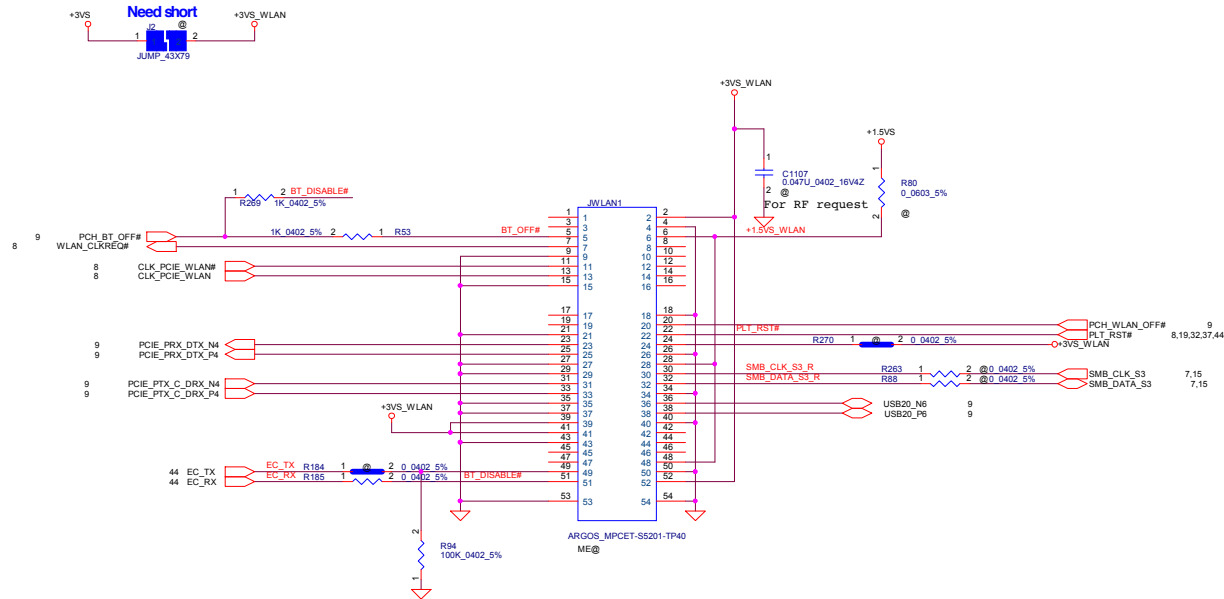
over temperature threshold:
 $RSET=3*RTMH$
 $92+/-30C$
Hysteresis temperature threshold.
 $RHYST=(RSET*RTML)/(3*RTML-RSET)$
 $56+/-30C$

FAN Conn



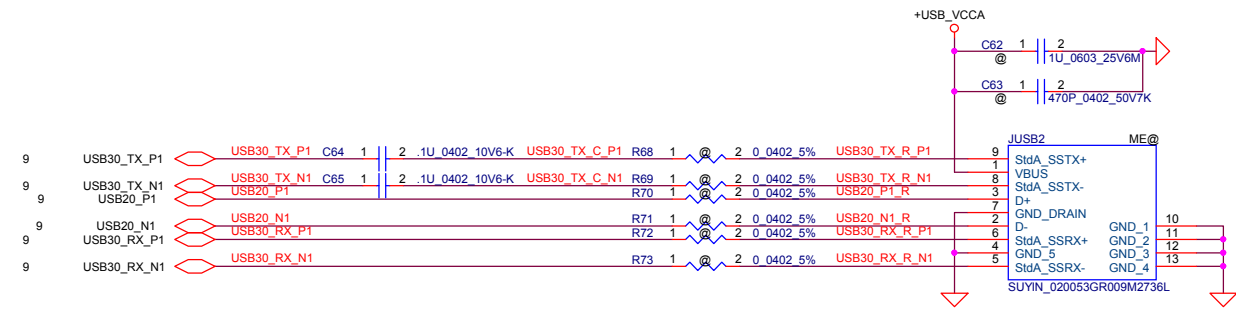
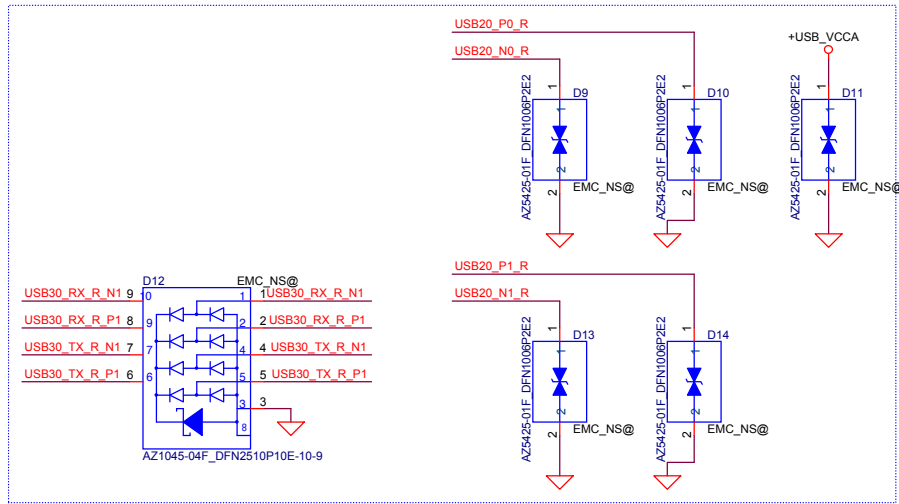
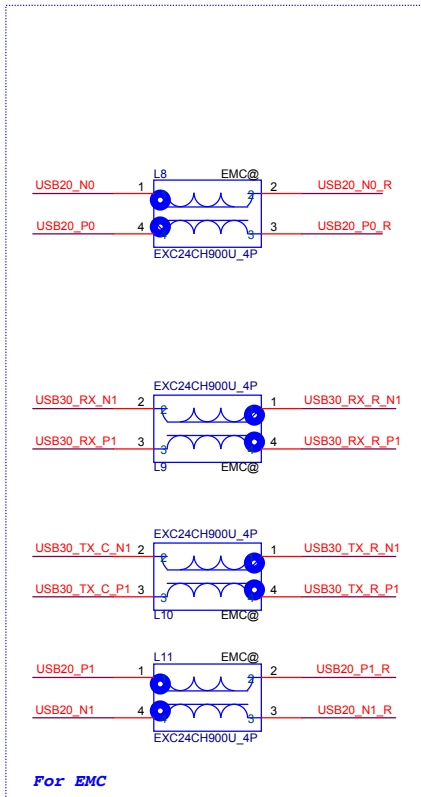
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Issued Date	2015/02/27	Deciphered Date	2013/08/05
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Mini-Express Card(WLAN/WiMAX)



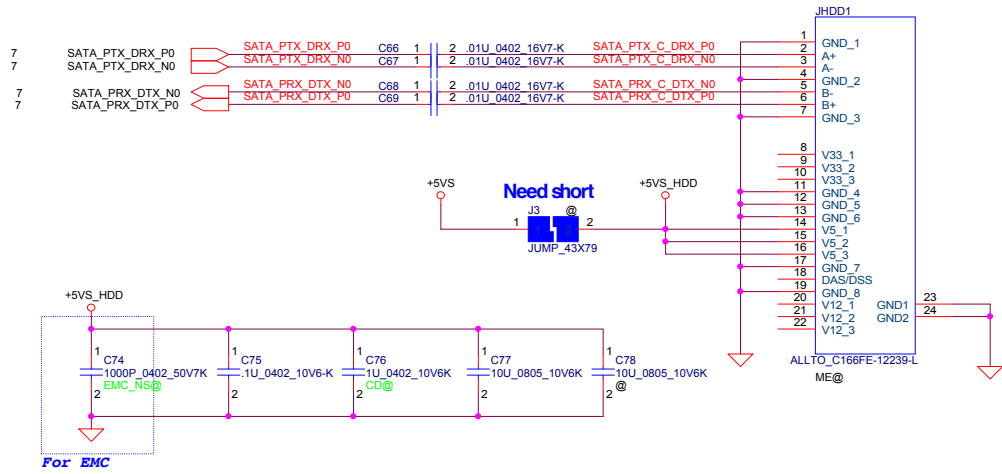
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/02/27	Deciphered Date	2013/08/05	PCIe WLAN	
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LEFT SIDE USB PORT X2

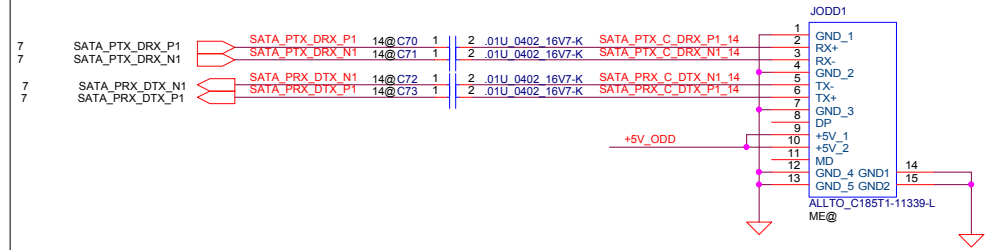


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Issued Date	2015/02/27	Deciphered Date	2013/08/05	USB2.0/USB3.0 PORT (LEFT)	
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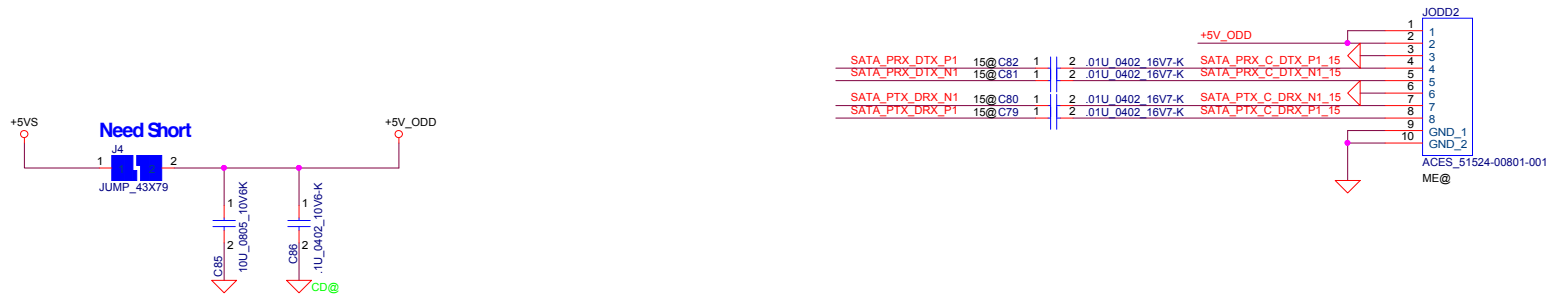
SATA HDD Conn.



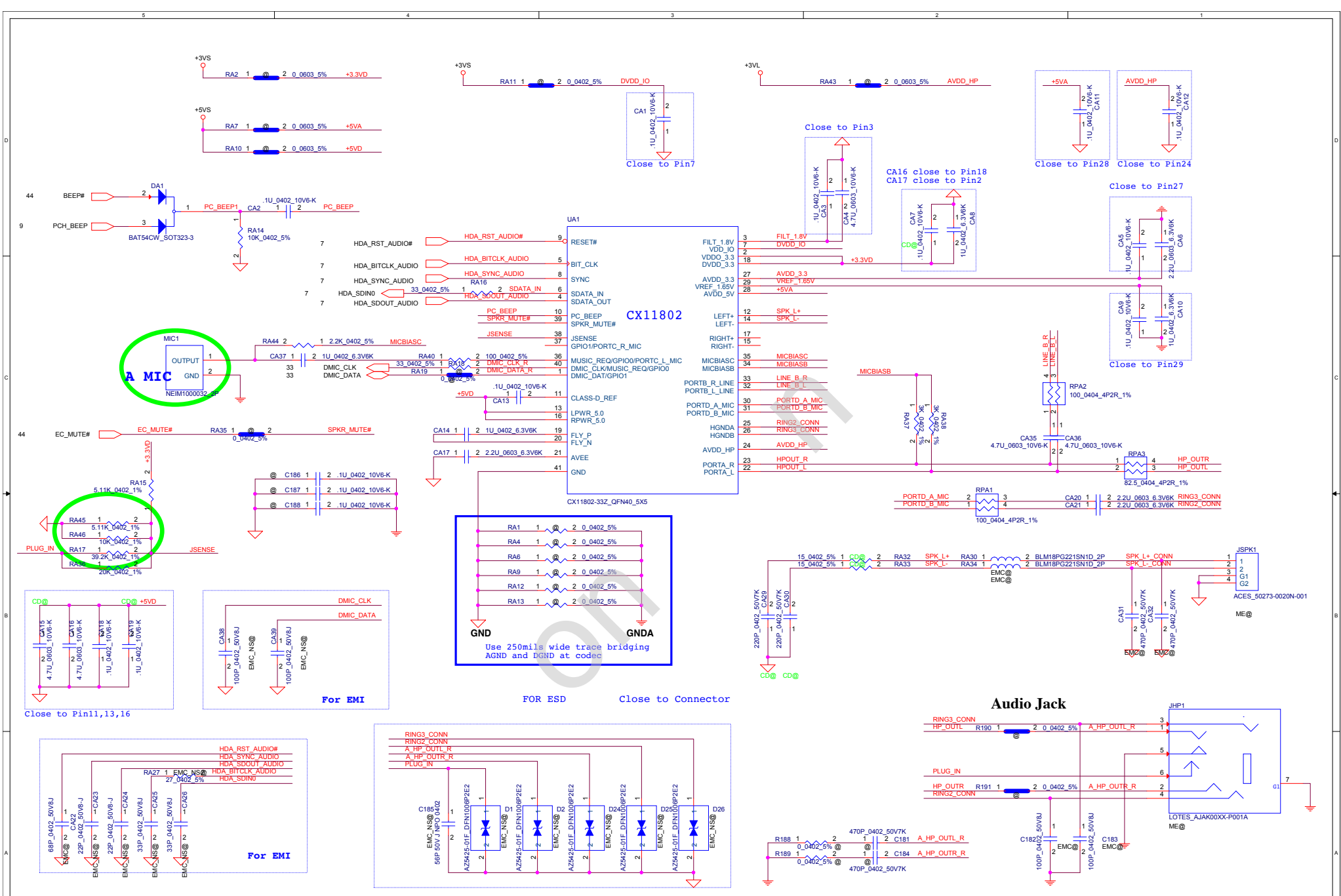
FOR 14" SATA ODD Conn.



FOR 15" SATA ODD FFC Conn

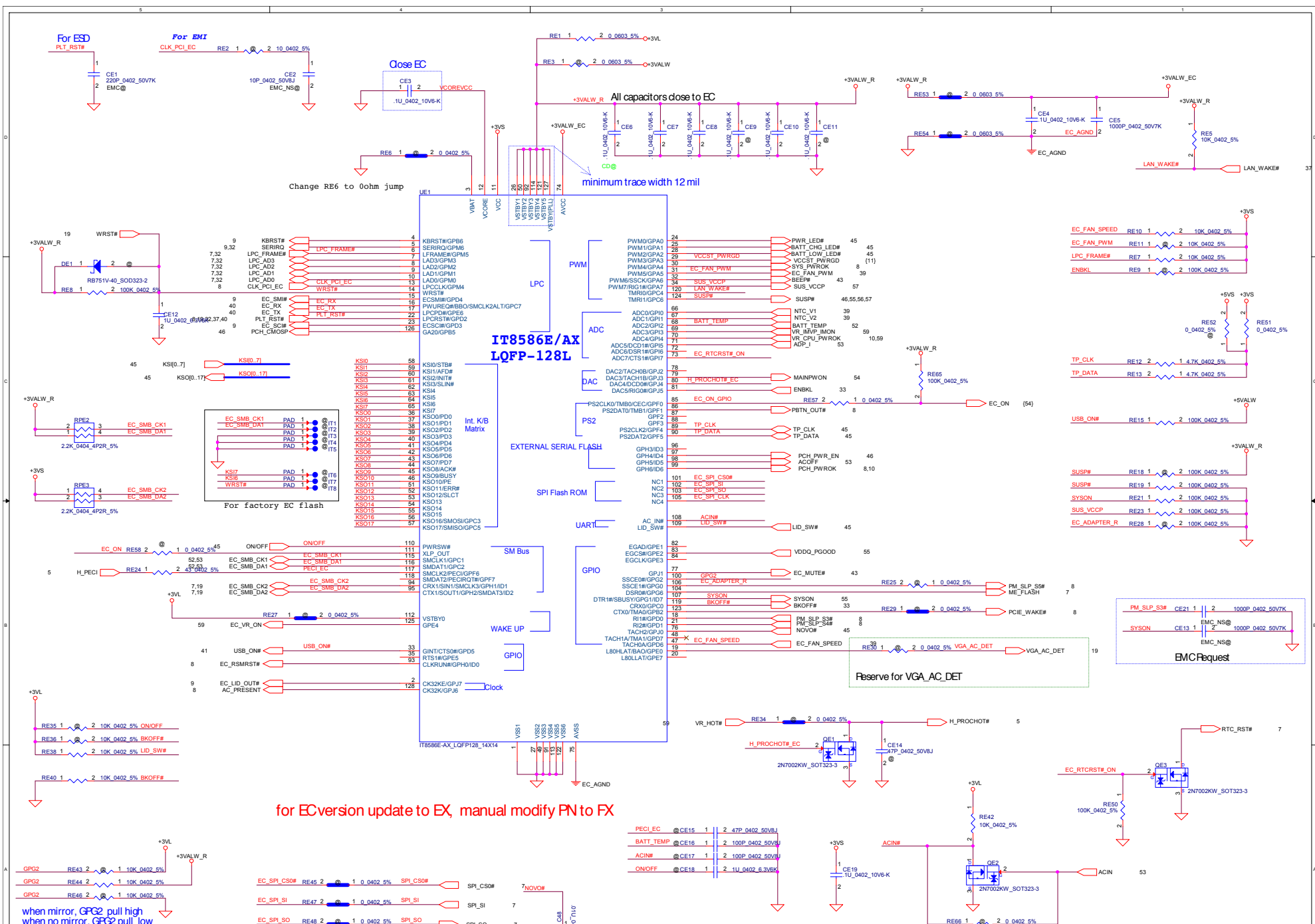


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Codec_CX11802		Document Number	CG510
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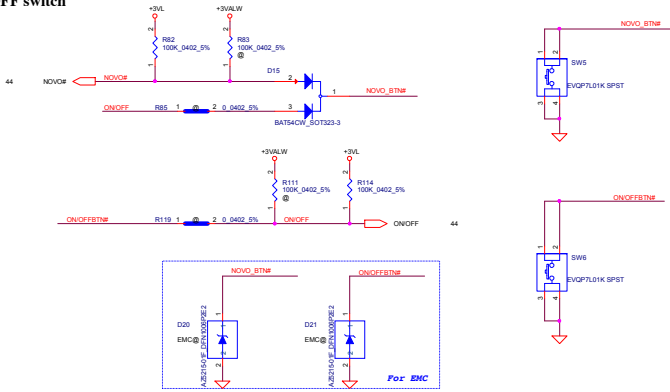
for ECversion update to EX, manual modify PN to FX

PECL_EC	@CE15	1	2	47P_0402_50VJ
BATT_TEMP	@CE16	1	2	100P_0402_50VJ
ACIN#	@CE17	1	2	100P_0402_50VJ
ONOFF	@CE18	1	2	1U_0402_439K

when mirror, GPG2 pull high
when no mirror, GPG2 pull low

Security Classification				LC Future Center Secret Data		Title	
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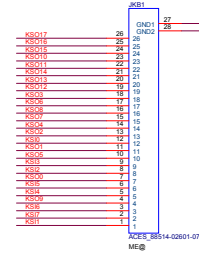
ON/OFF switch



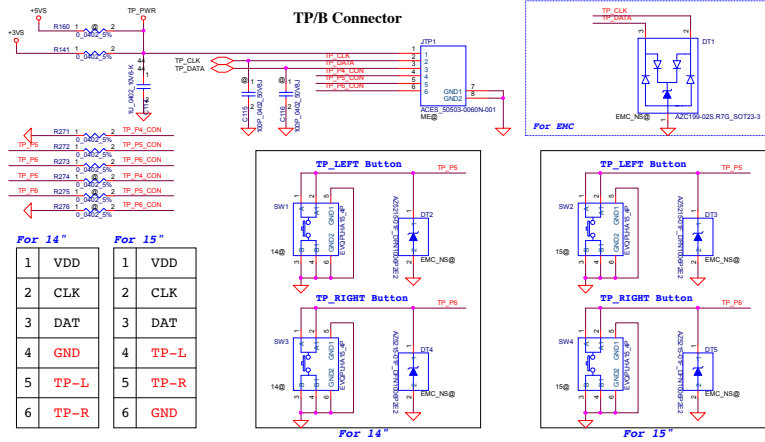
K/B Connector



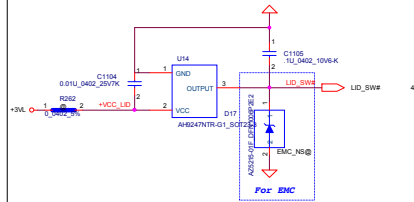
15"



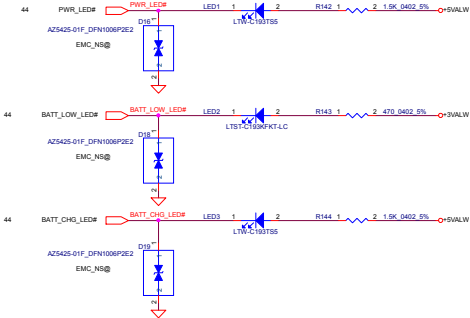
TP/B Connector



Hall Sensor



LED



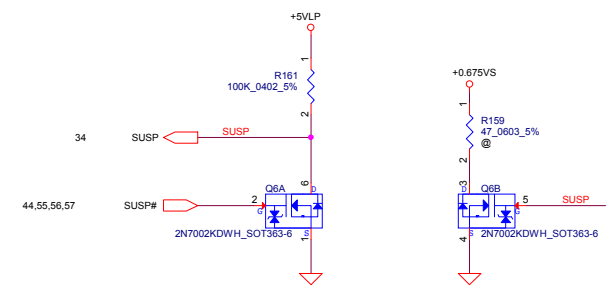
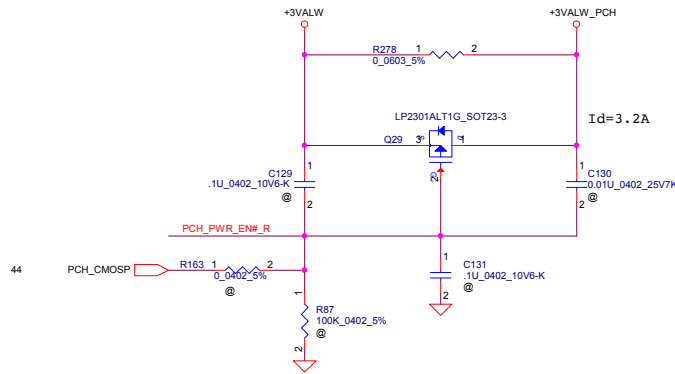
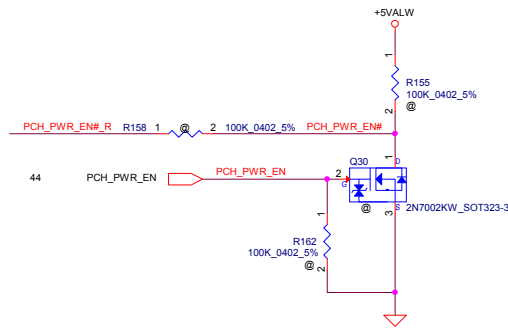
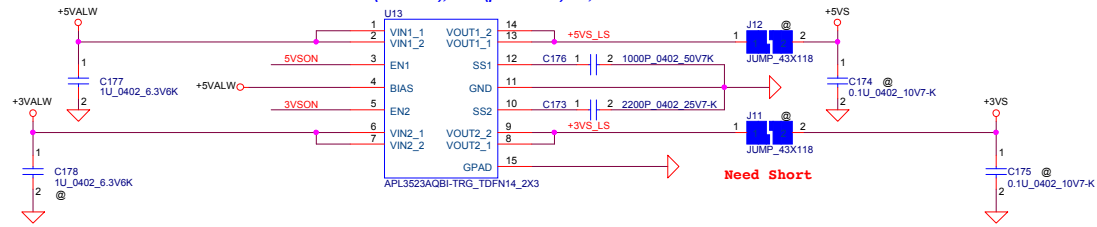
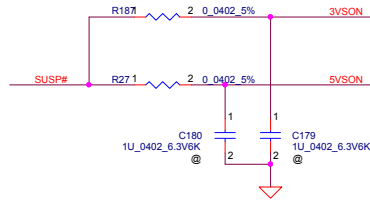
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/02/27	Deciphered Date	2013/06/05	KBD/PWR/LED/TP Conn.	
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Load Switch
+5VALW To +5VS
+3VALW To +3VS

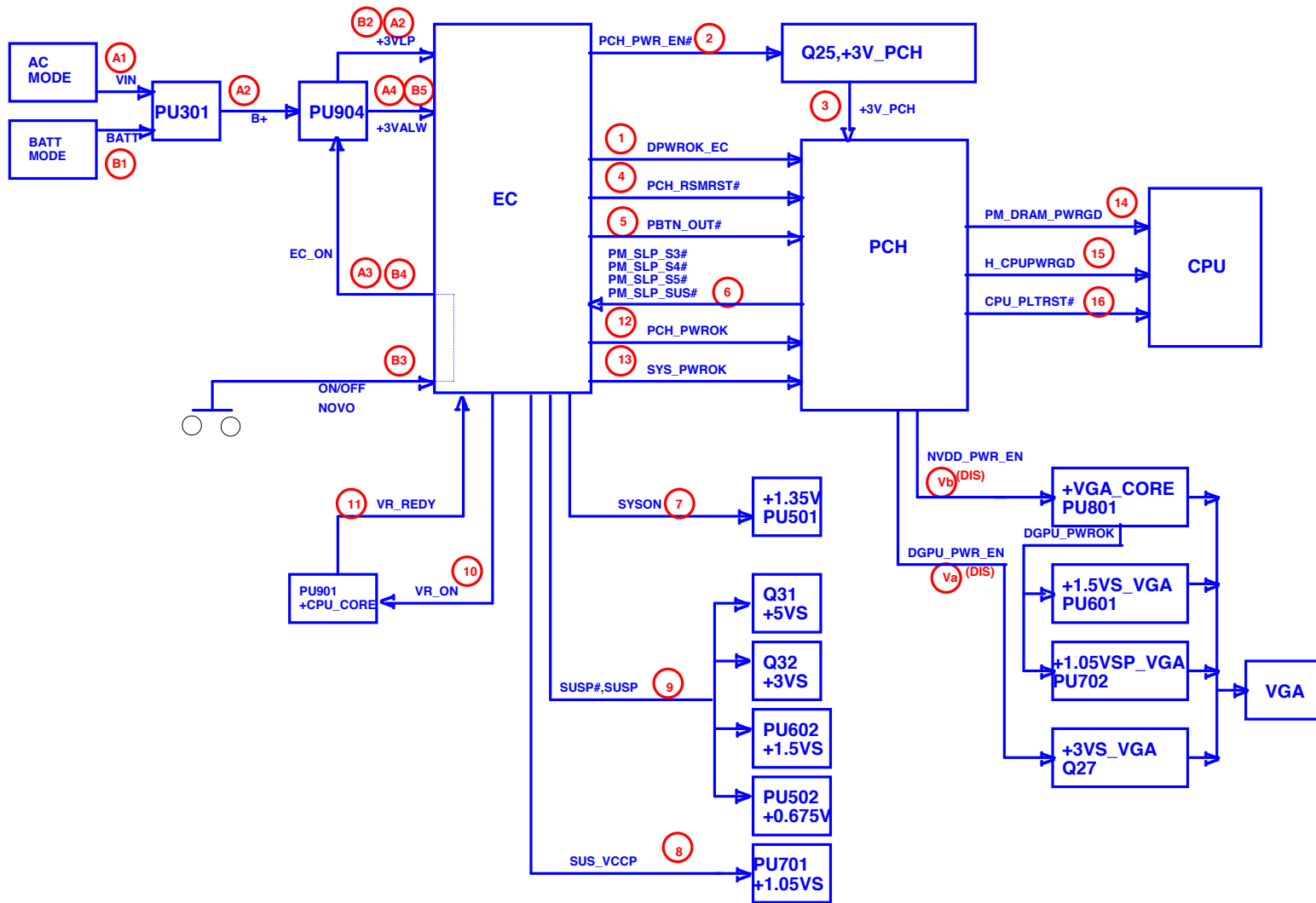
+3VS C173 --> 2.74ms
+5VS C176 --> 2.03ms

VIN 5V and 3.3V (VBias=5V), I_{MAX}(per channel)=6A, R_{DS}=16mohm

Need Short



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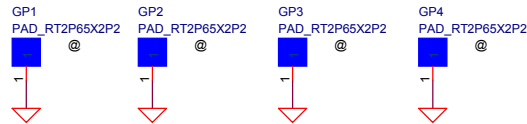
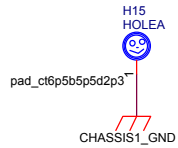
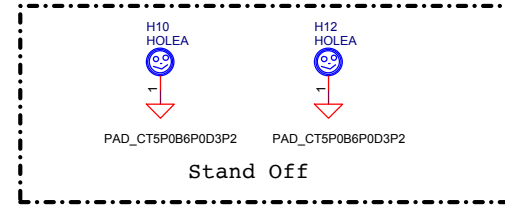
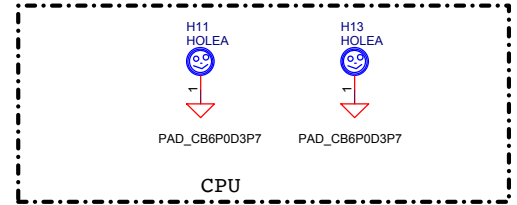
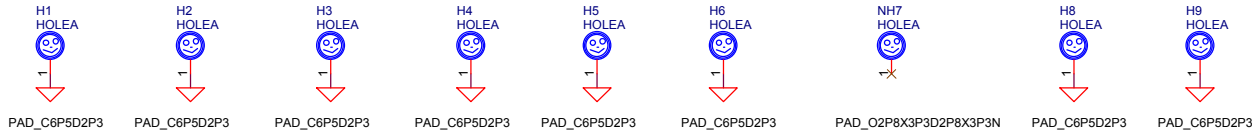
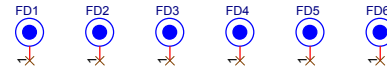
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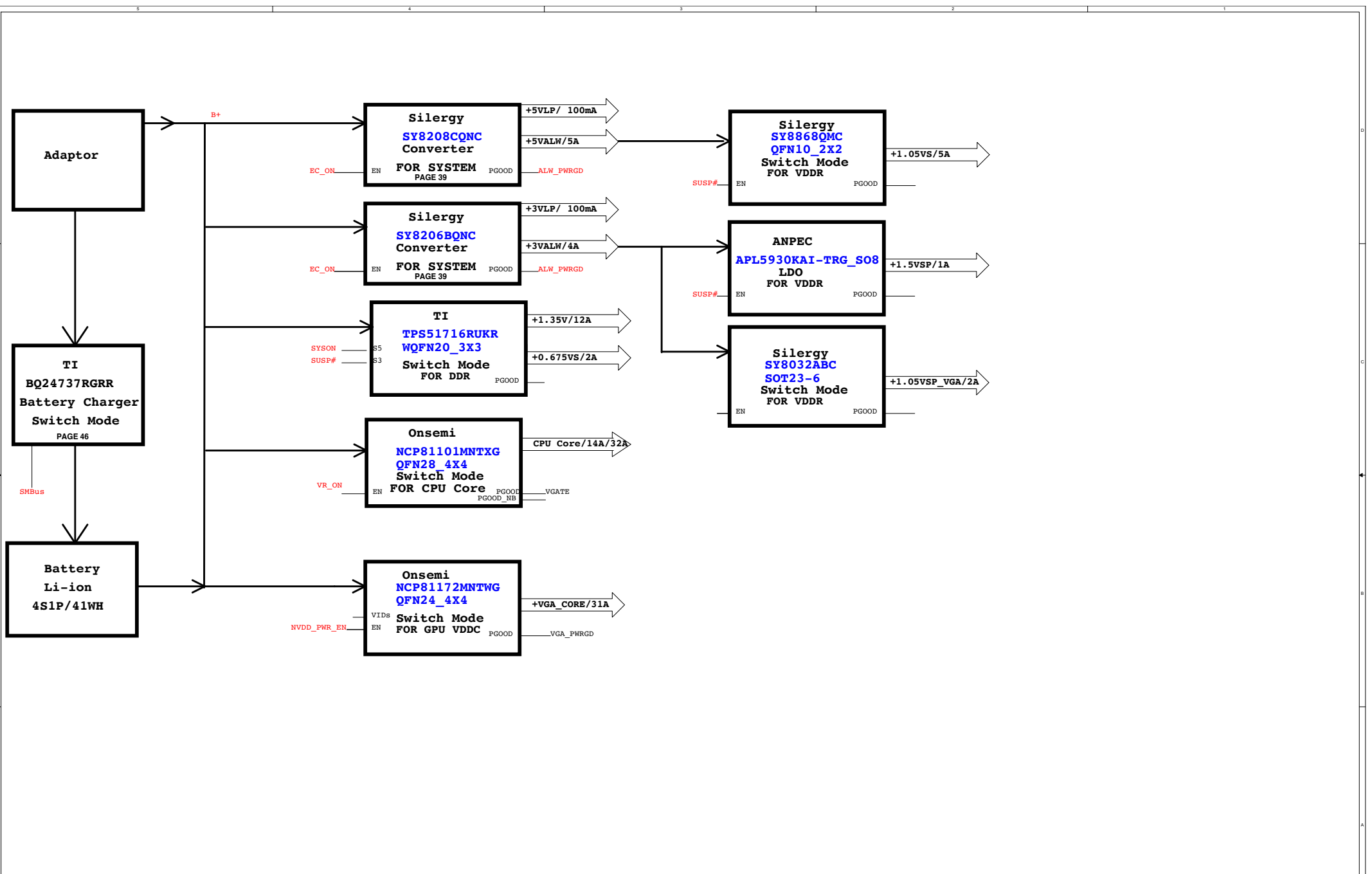
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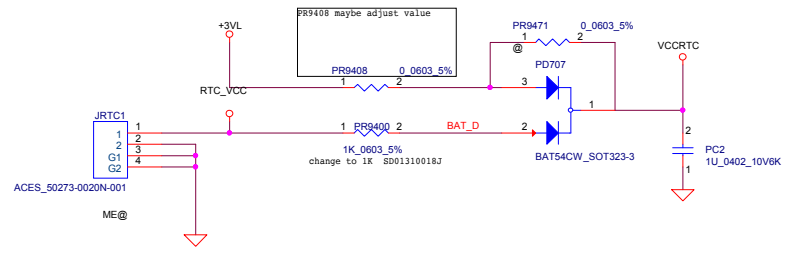
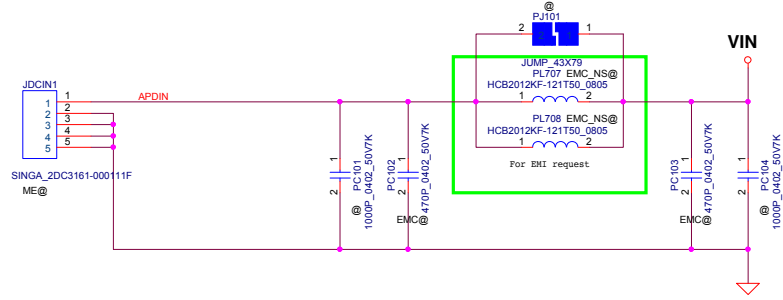
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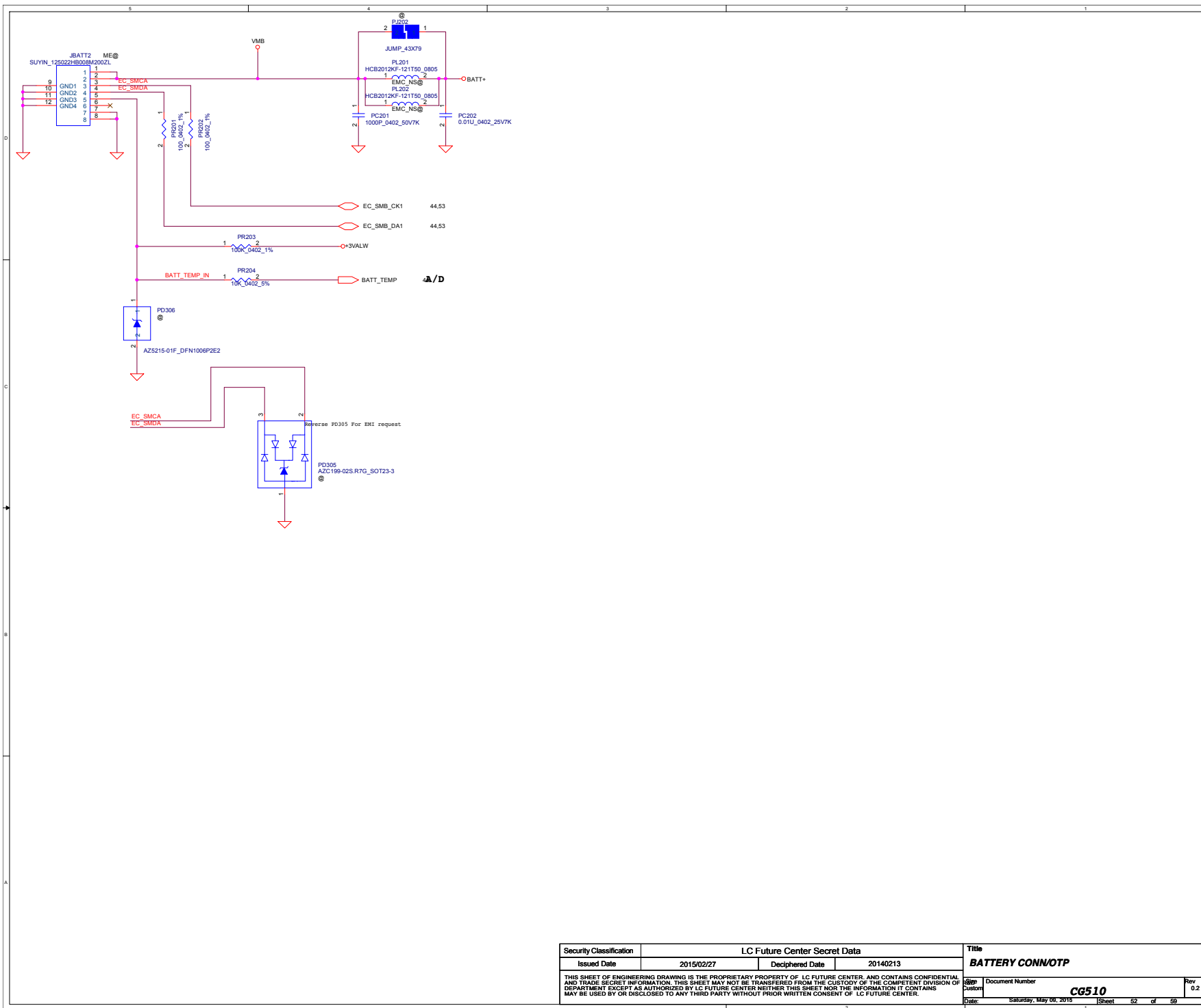
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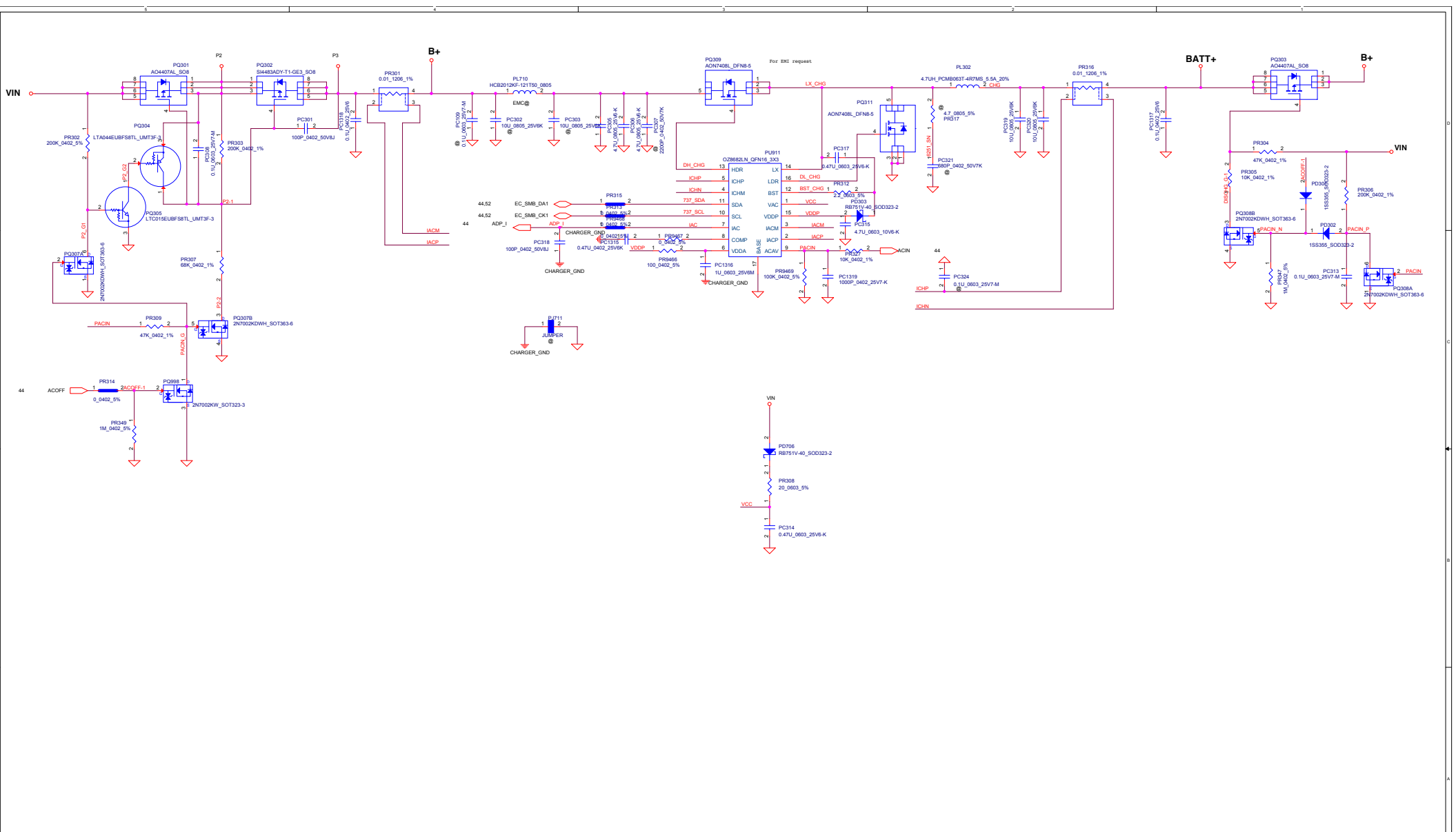
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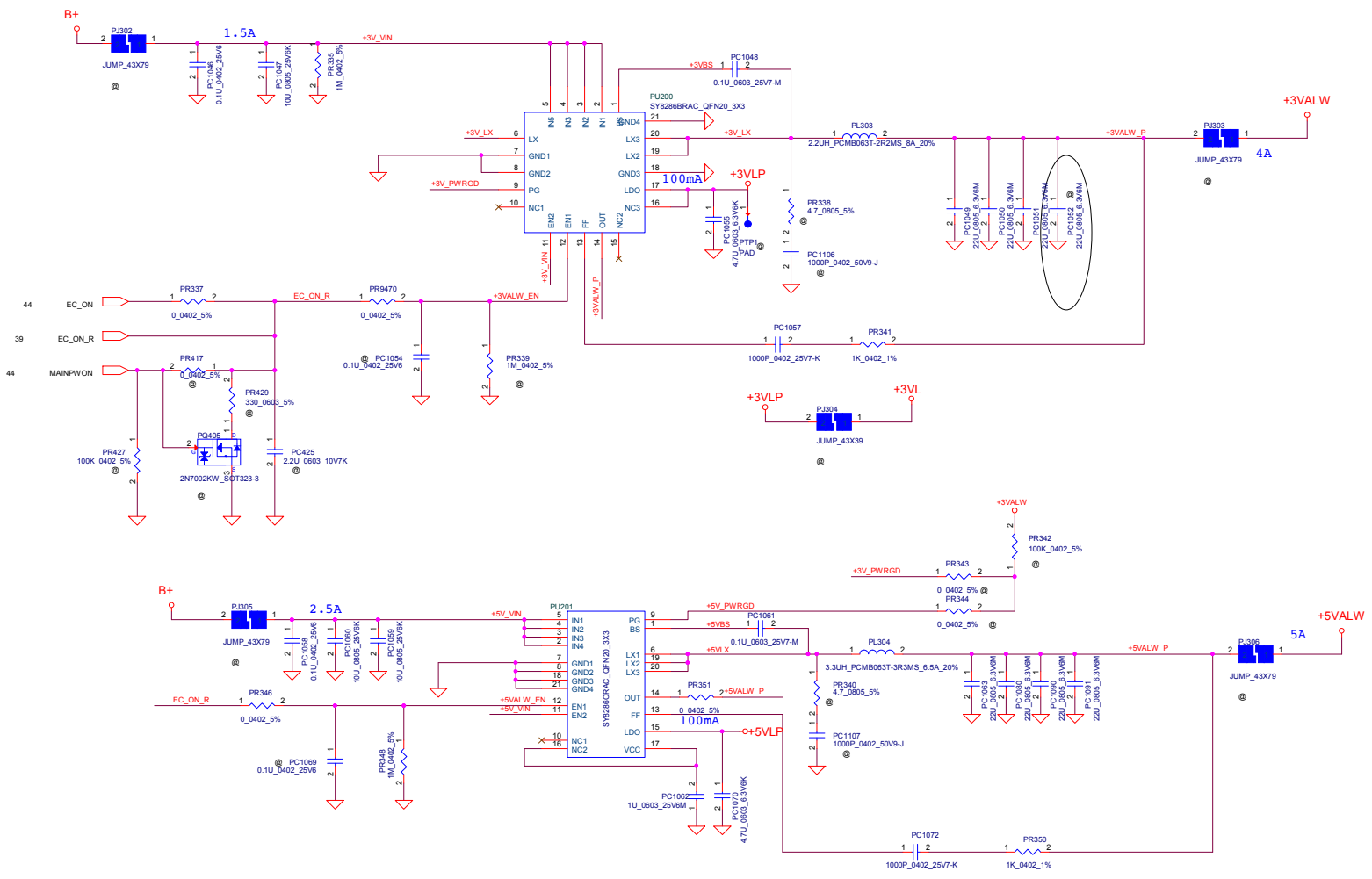
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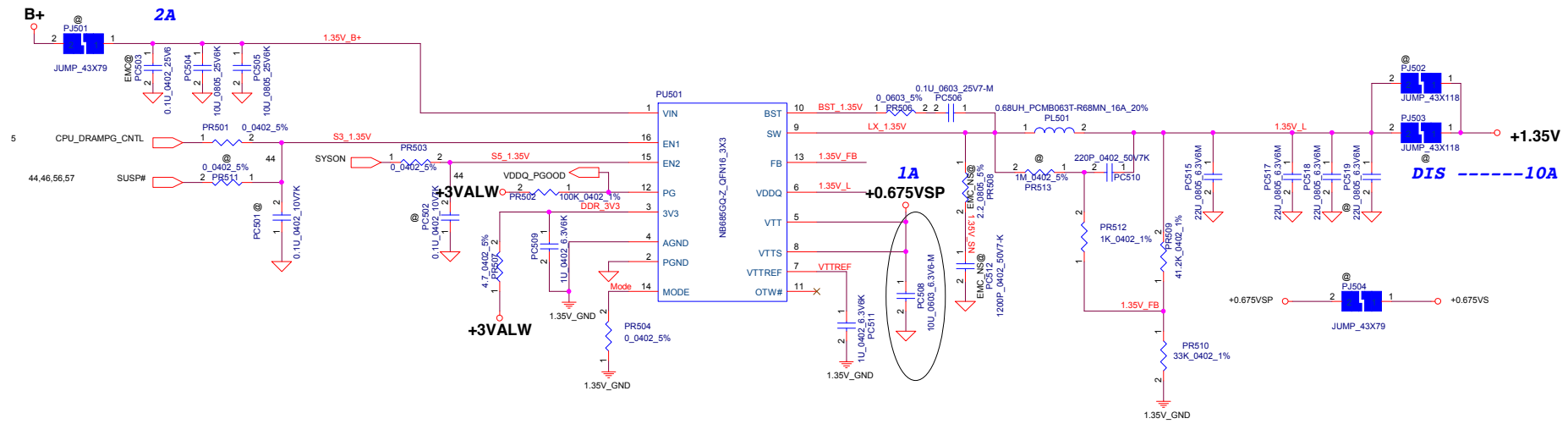
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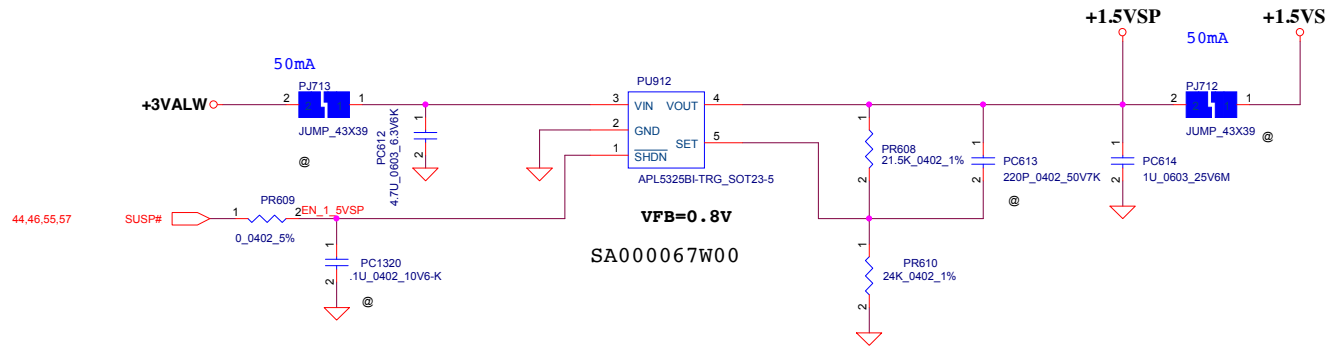
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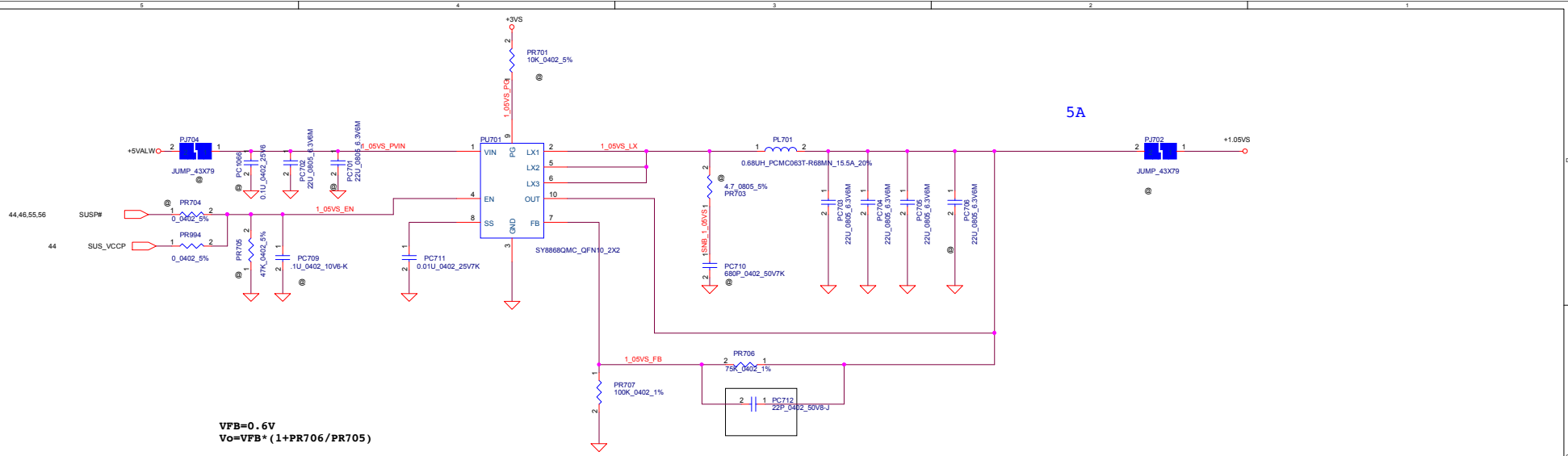
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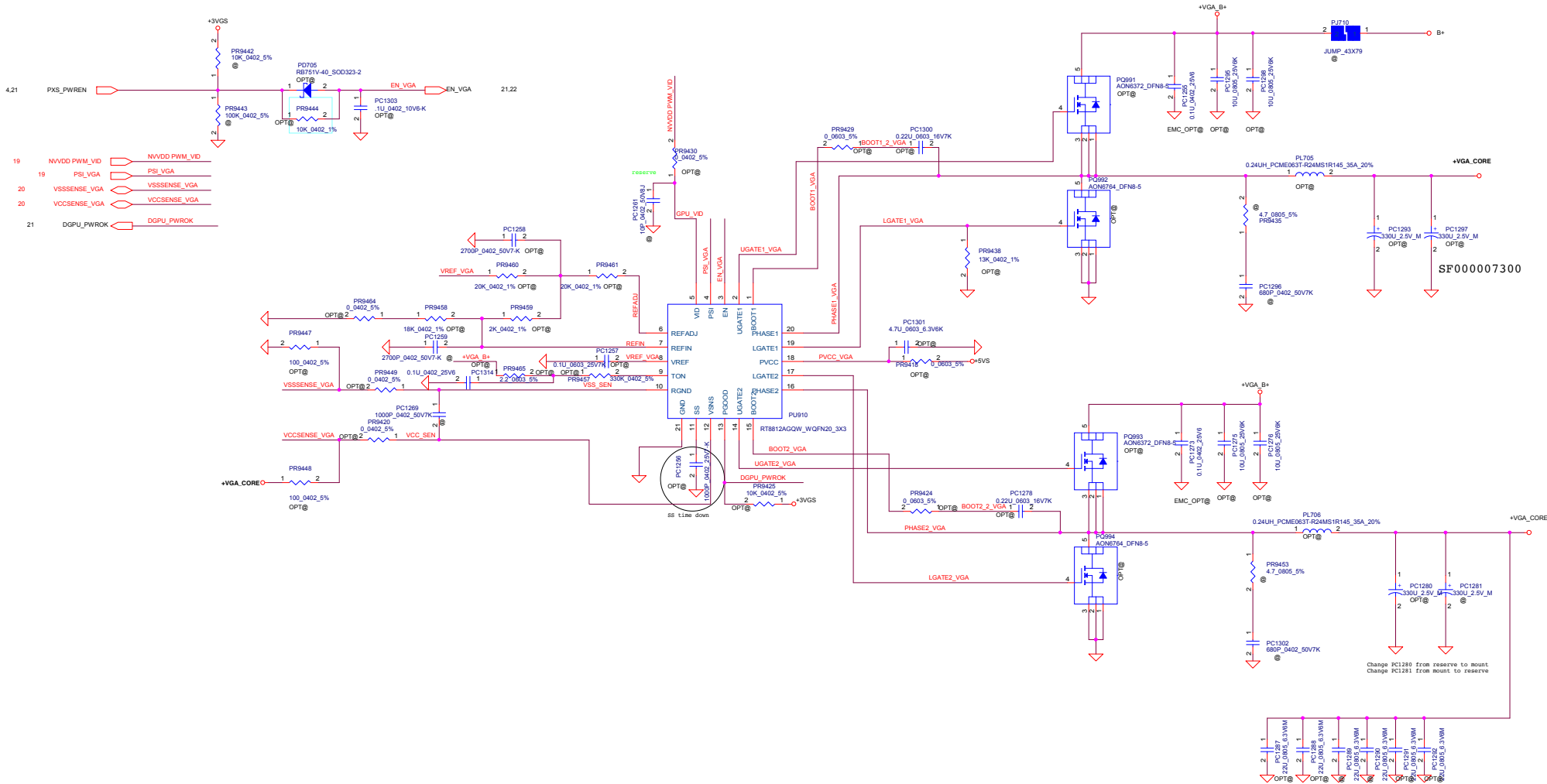
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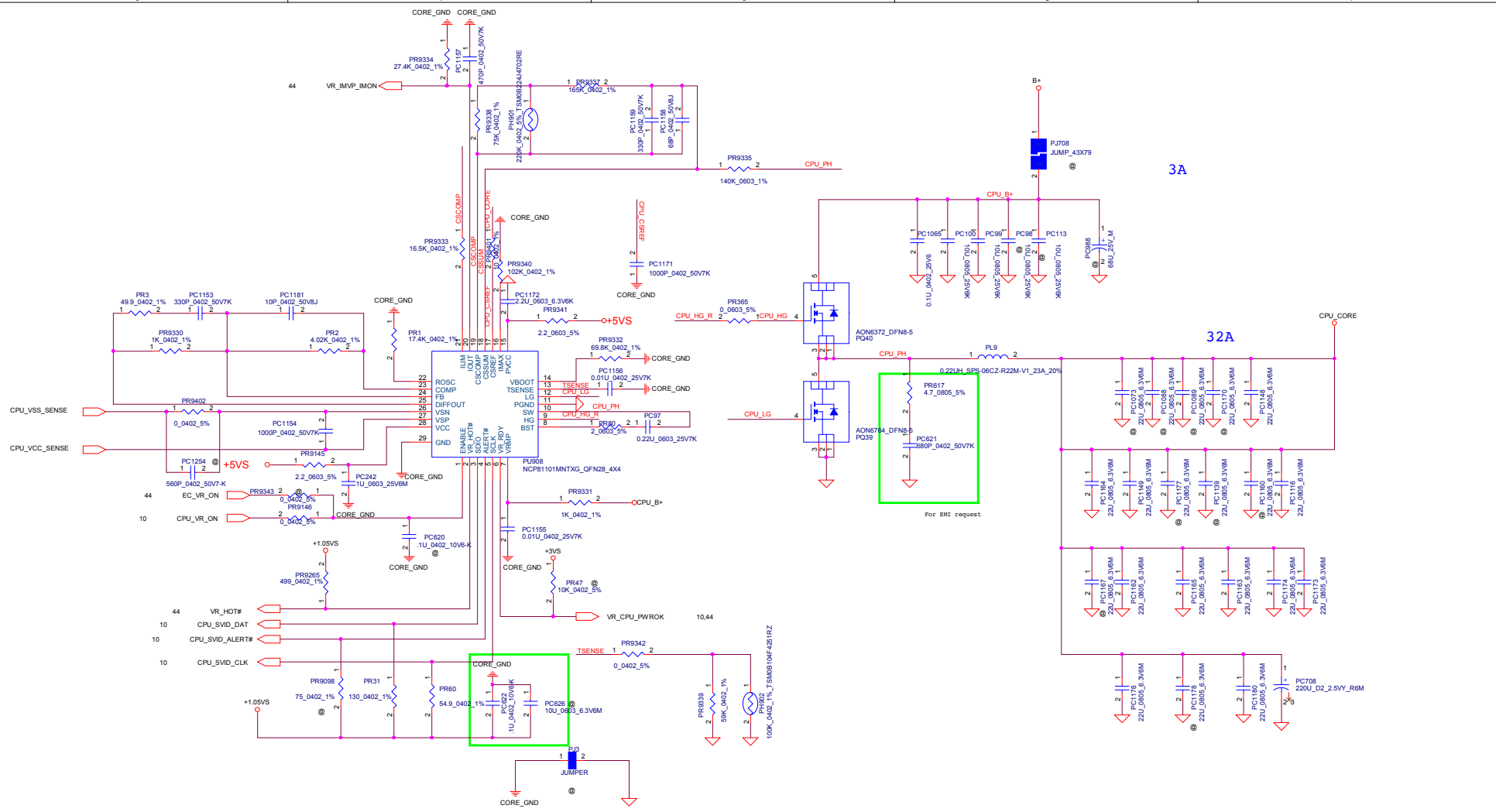
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