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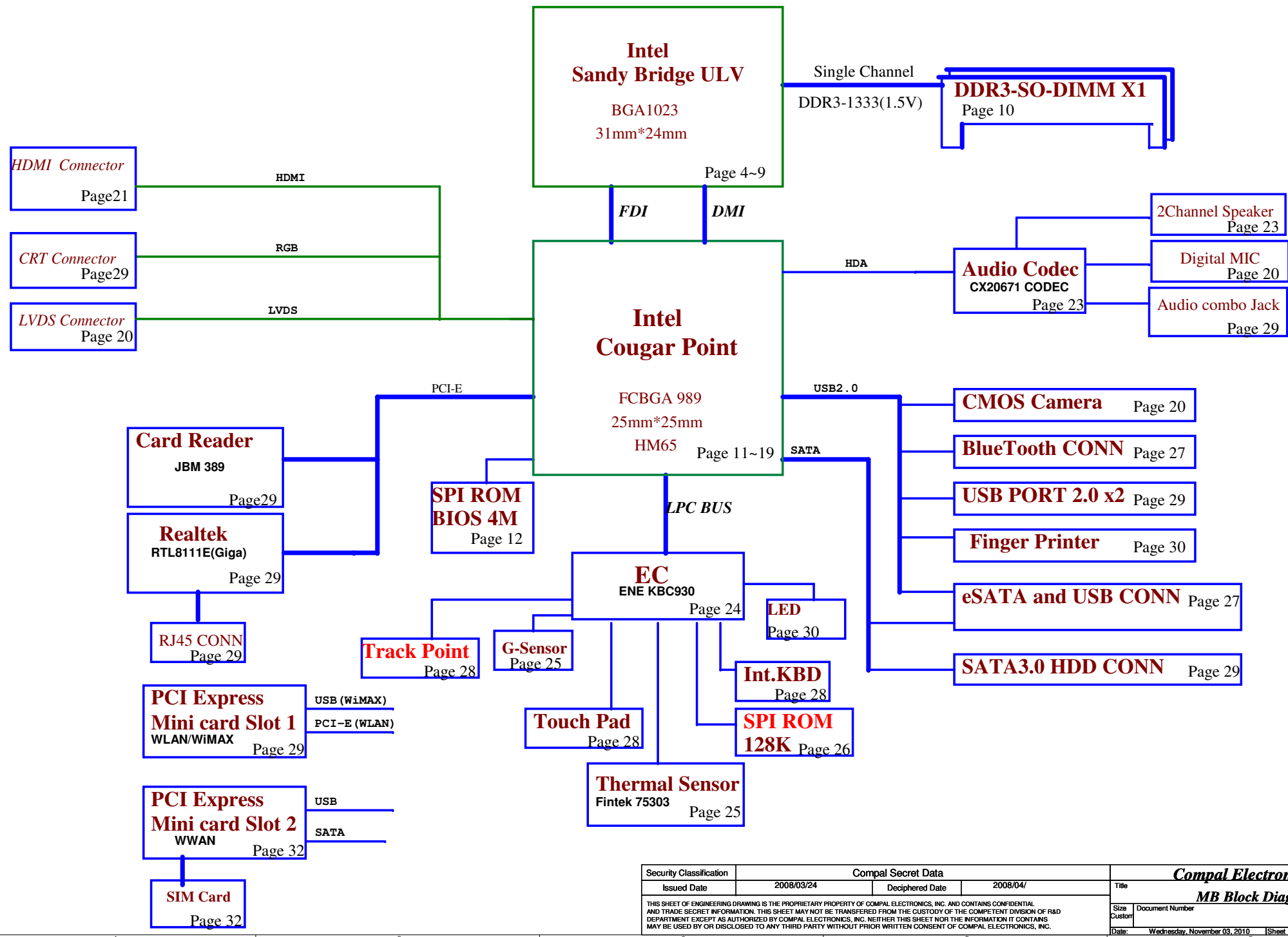
LA7041- Edge Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH

2010-10-05

REV: 0.2

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2009/08/01	Deciphered Date	2010/08/01	Title Cover Page		
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				Date:	Wednesday, November 03, 2010	Sheet 1 of 40



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Size	Custom	Document Number	Rev	0.2	
Date: Wednesday, November 03, 2010				Sheet 2 of 40	

Voltage Rails

power plane	+B	+5VALW	+1.5V	+5VS
				+3VS
State		+3VALW		+1.8VS
				+1.5VS
				+1.05VS
				+VGF_X_CORE
				+CPU_CORE
				+0.75VS
				+1.5VS_DISVGA
				+1.0VS
				+NVVDD
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS
Full ON	HIGH	HIGH	HIGH	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	
3	
4	
5	
6	
7	

USB Port Table

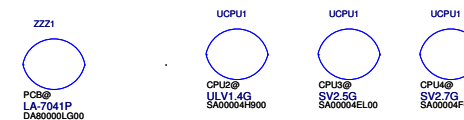
USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB_COMBO
		1	USB_PORT
		2	NO USE
	UHCI1	3	NO USE
		4	WWAN
		5	CAMERA
EHCI2	UHCI3	6	HM65 not support
		7	HM65 not support
		8	WLAN
	UHCI4	9	USB_CHARGER
		10	NO USE
		11	NO USE
UHCI6	12	FINGER-PRINTER	
	13	BLUETOOTH	

BTO Option Table

BTO Item	BOM Structure
3G	
Unpop	e

BOM Structure Table

Structure	Function
CPU1@	CPU type
CPU2@	CPU type
CPU3@	CPU type
CPU4@	CPU type
3G@	3G Sim card
PCB@	M/B
SV@	SV CAP
ULV@	ULV CAP



EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

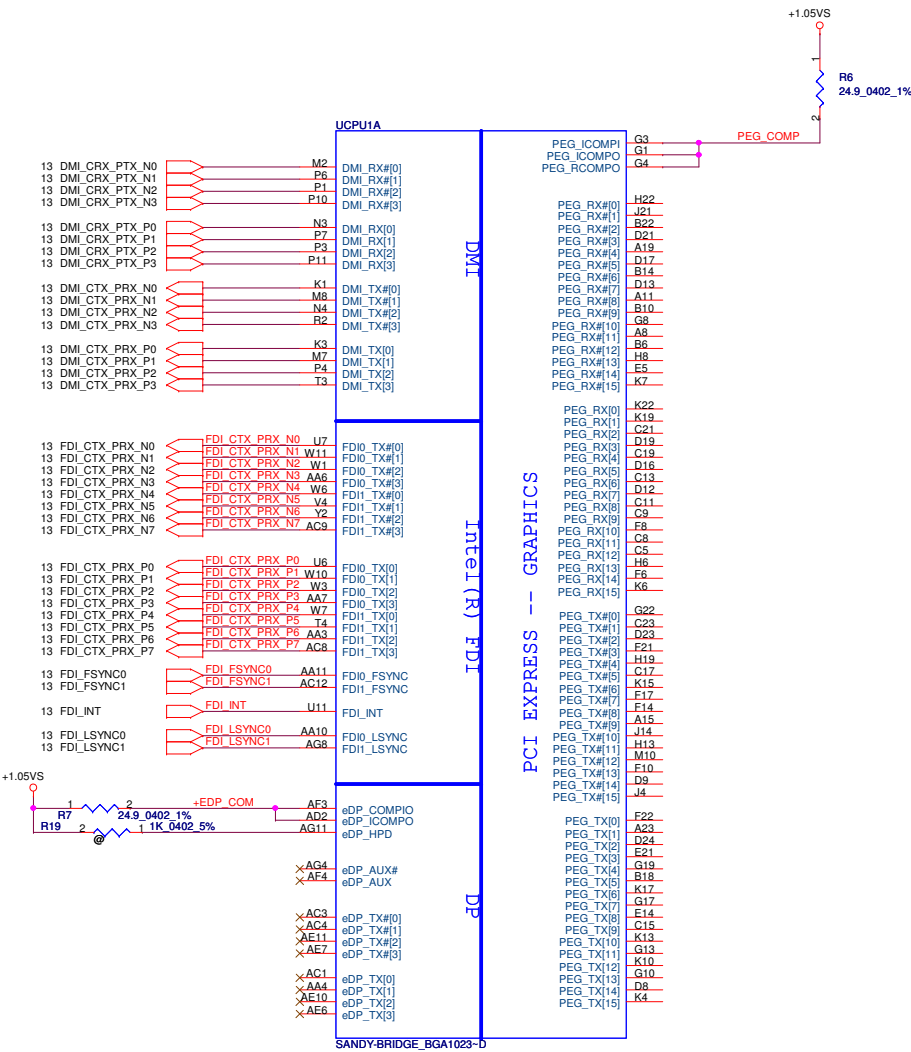
Device	Address
PCH	1001 0110 b
Thermal sensor	1001 1110 b
G sensor	0111 0010 b

nomsata@

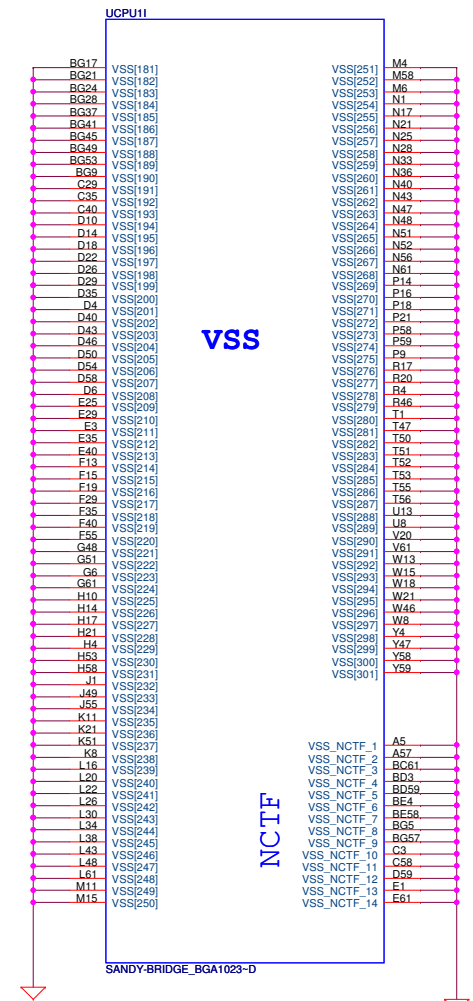
PCH SM Bus address

Device	Address
DDR DIMM0	1010 0000b
DDR DIMM2	1010 0100b
EEPROM(U32)	1010 100xb

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Size	Document Number	Rev	Date	
	<Doc>	0.2	Wednesday, November 03, 2010 Sheet 3 of 40	

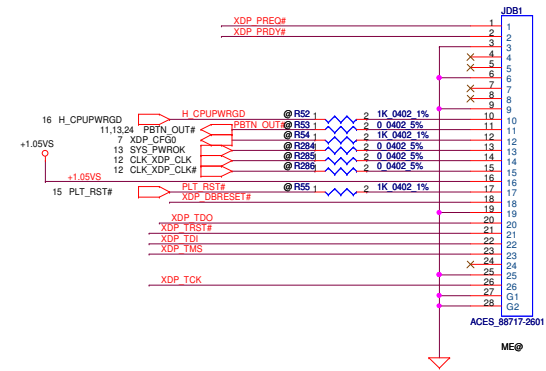
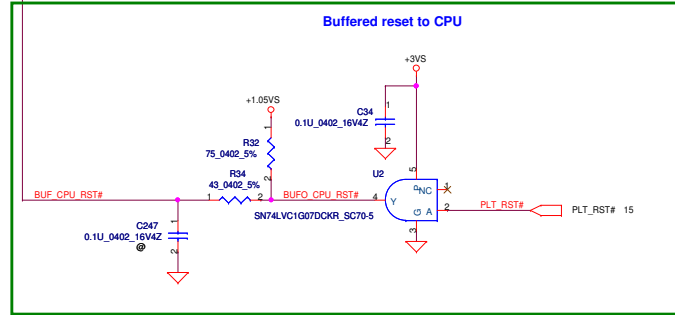
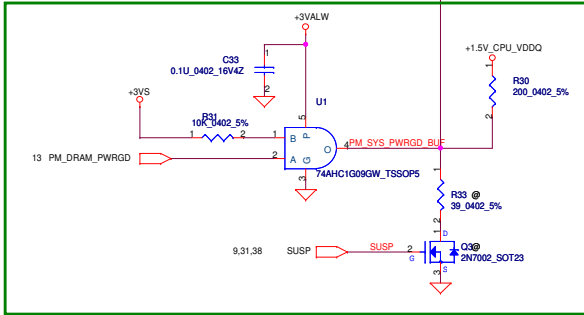
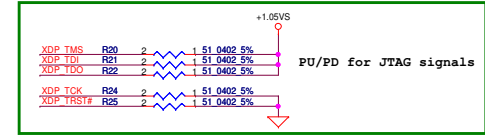
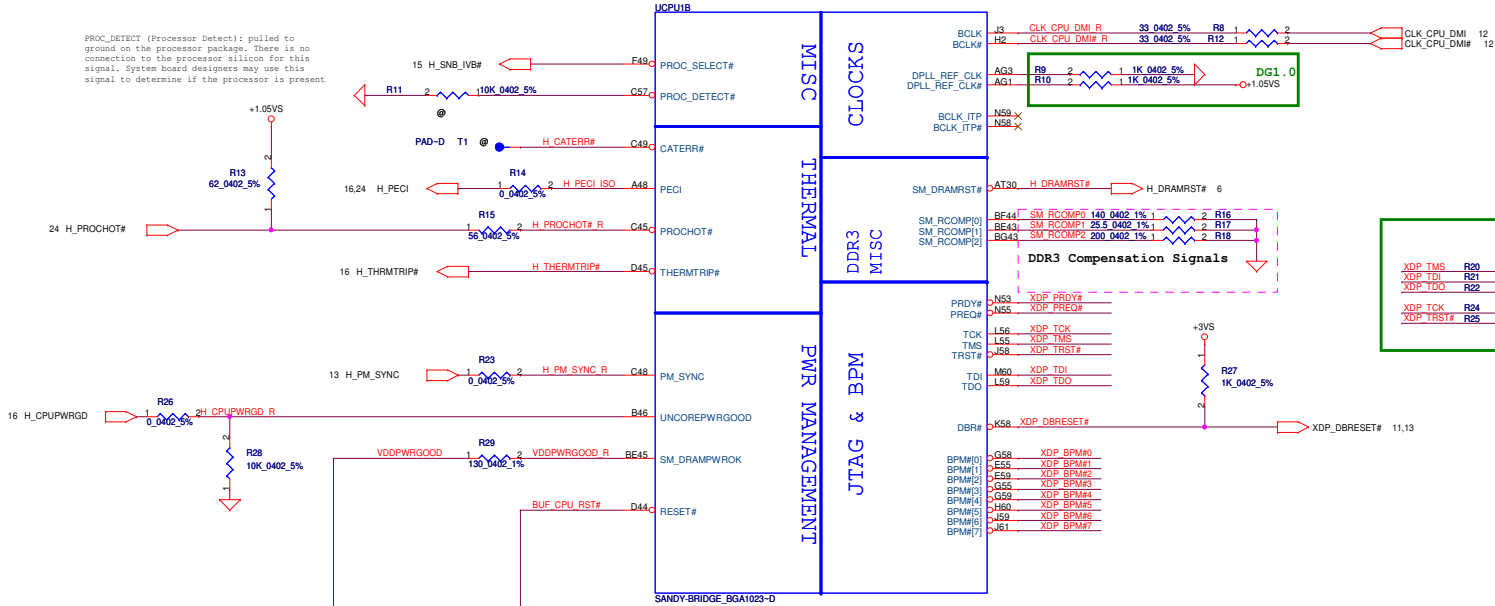


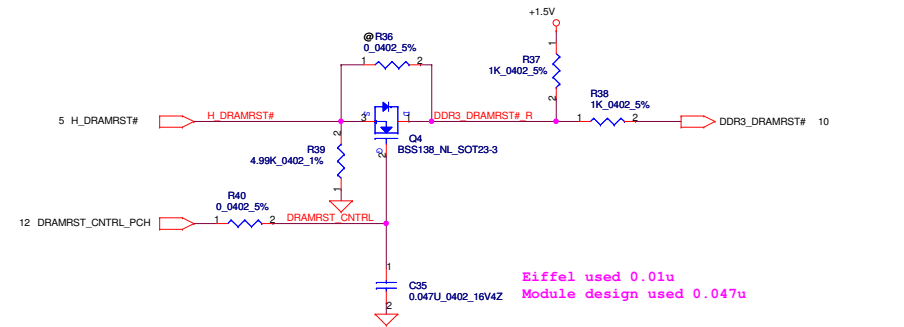
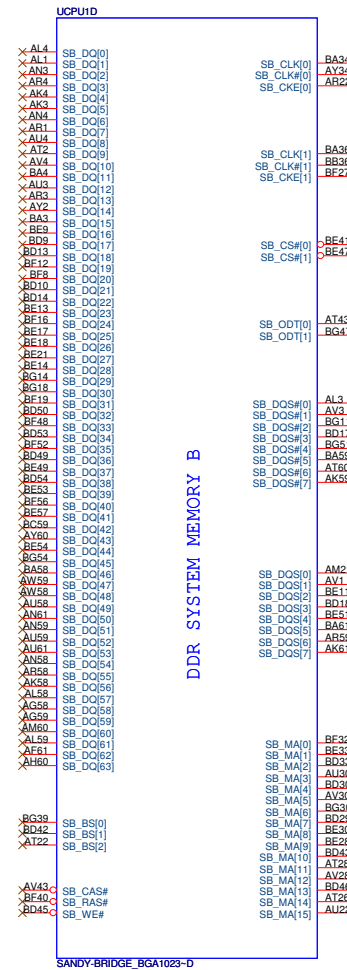
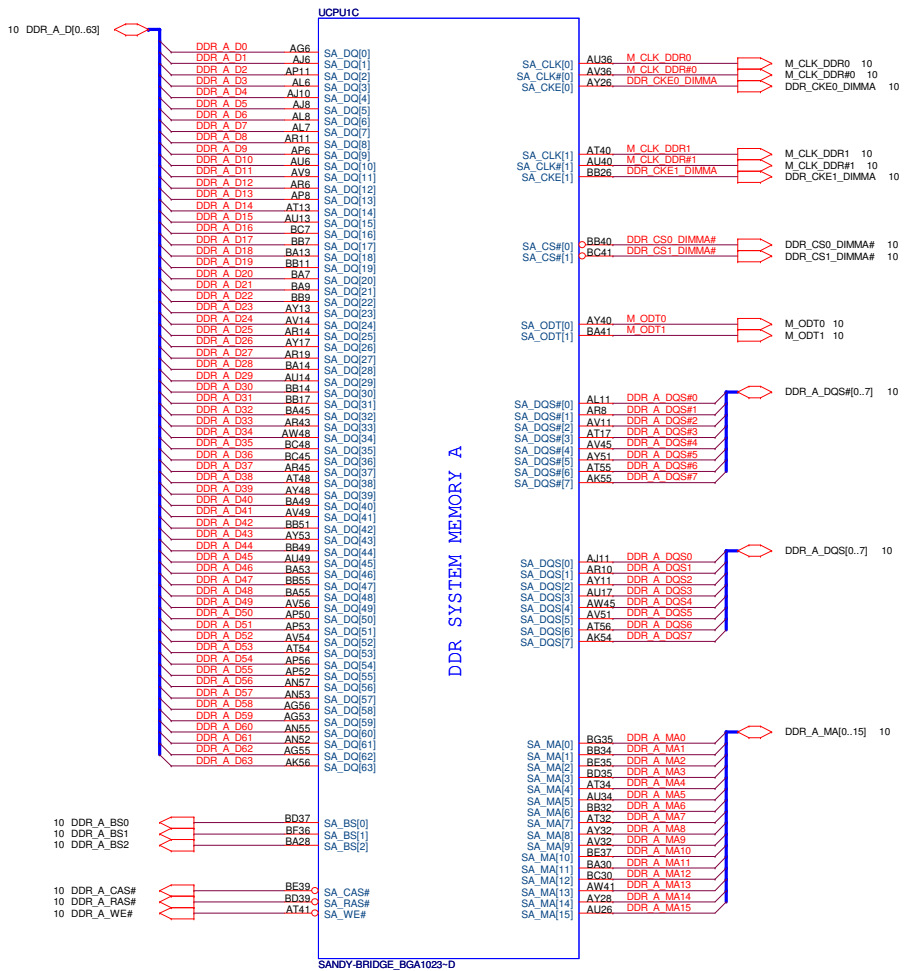
PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



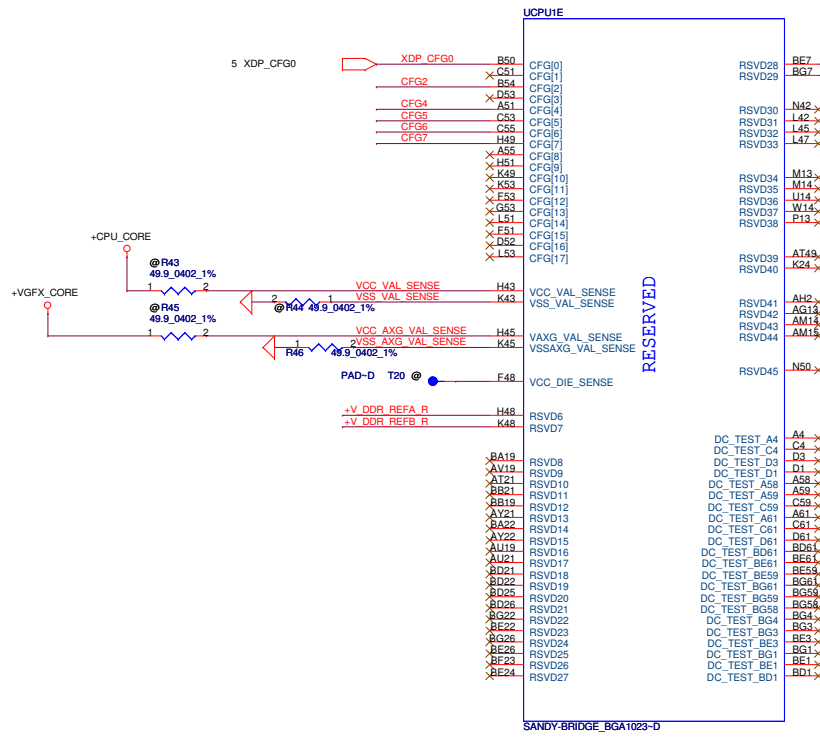
Security Classification		Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2010/07/06	Deciphered Date	2011/07/06	PROCESSOR(I/6) DMI,FDI,PEG			
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Date:	Wednesday, November 03, 2010	Sheet	4 of 40				

PROC_DETECT (Processor Detect): pulled to ground on the processor package. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present

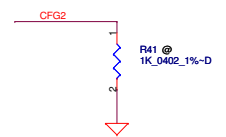




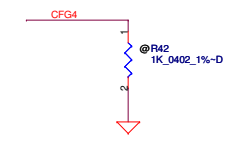
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LA-7041P			Rev	0.2
Date: Wednesday, November 03, 2010				Sheet 6 of 40



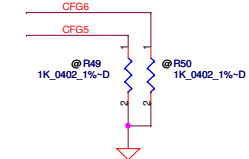
CFG Straps for Processor



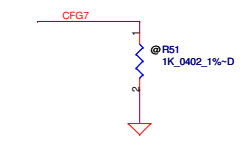
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	*1: (Default) Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed



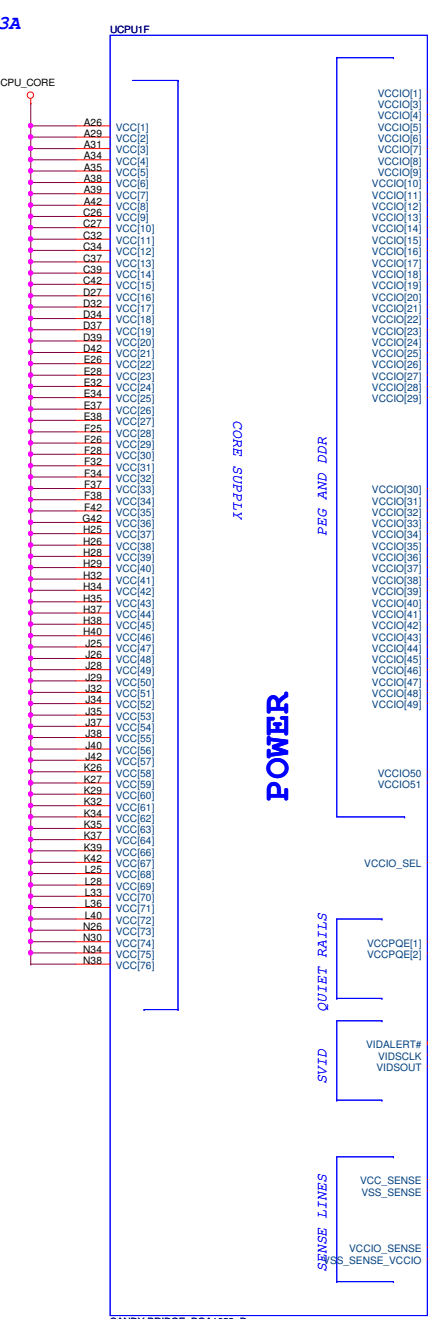
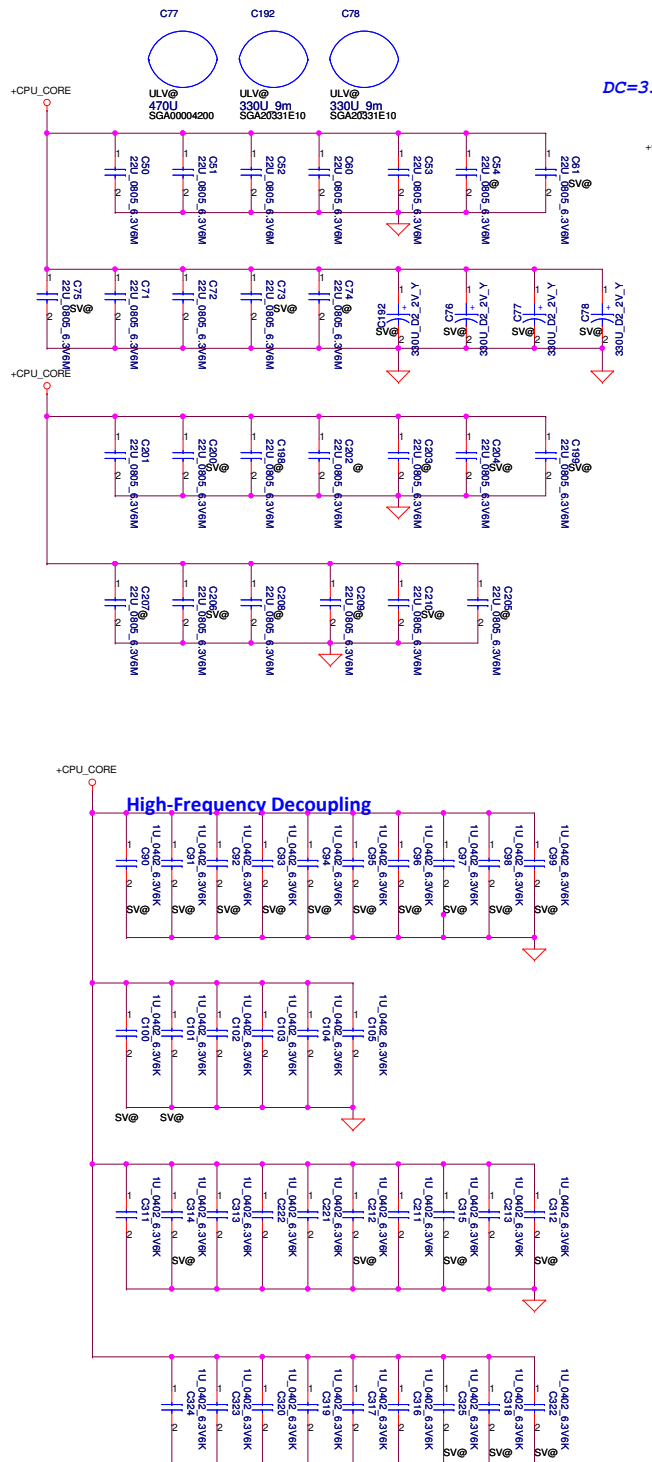
Display Port Presence Strap	
CFG4	*1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



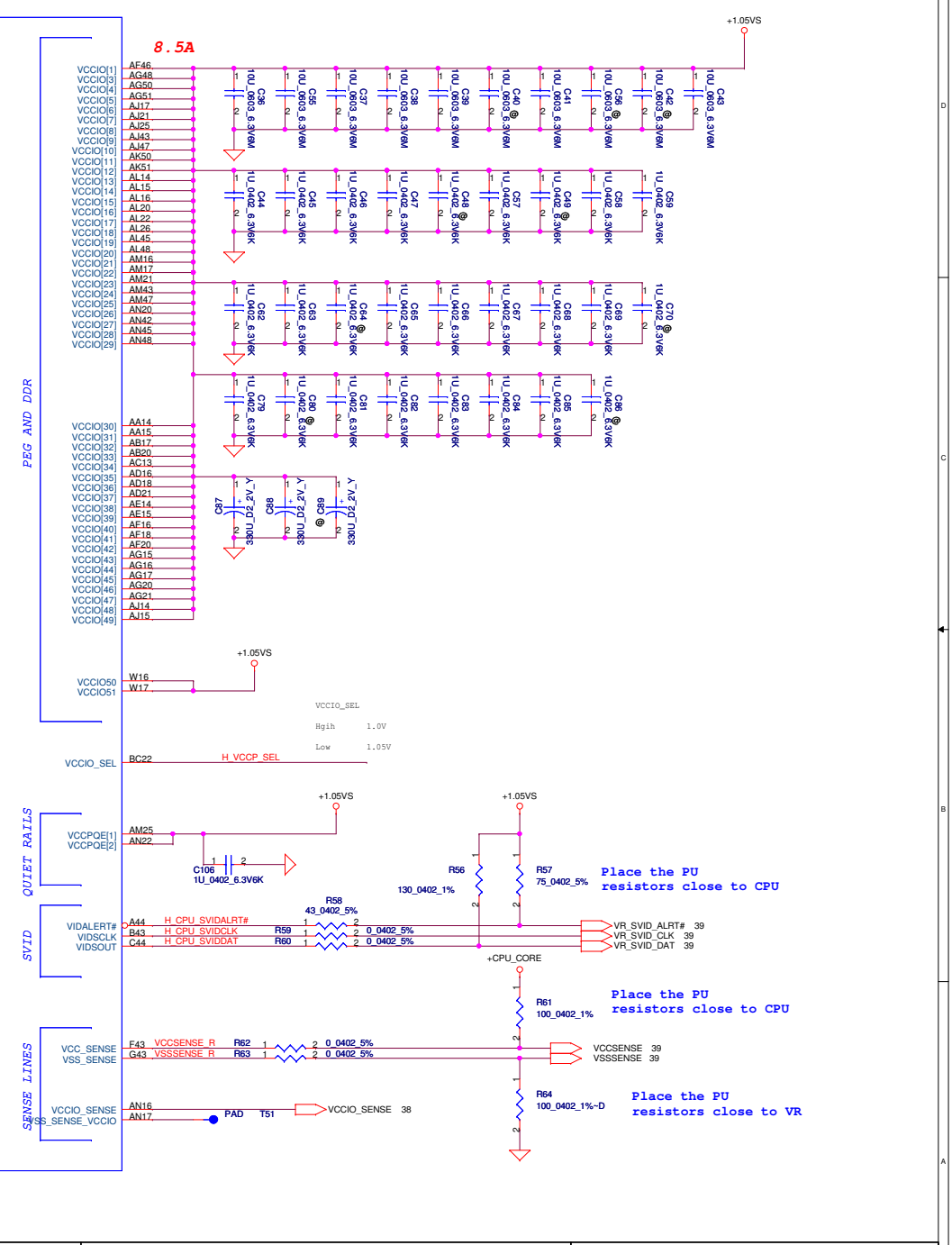
PCIe Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



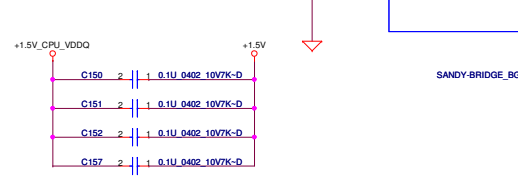
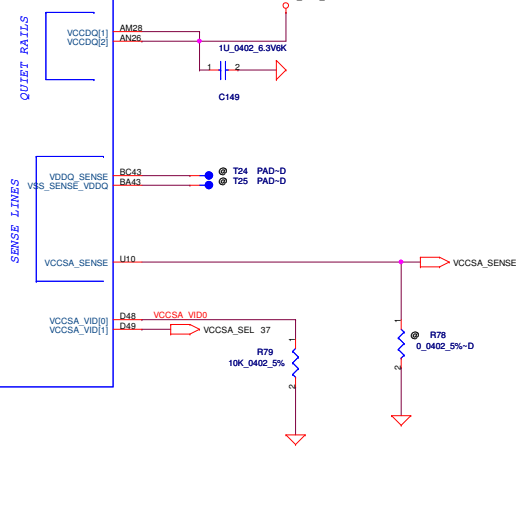
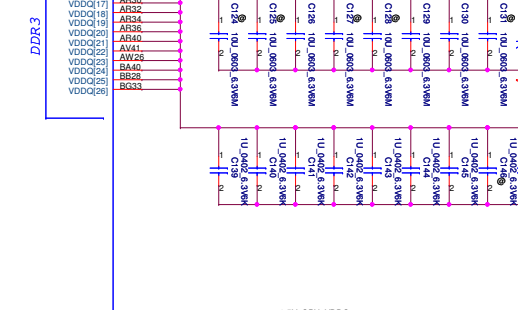
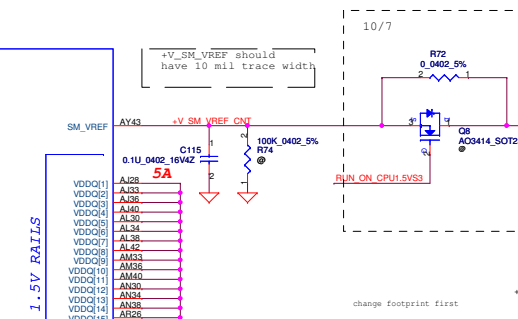
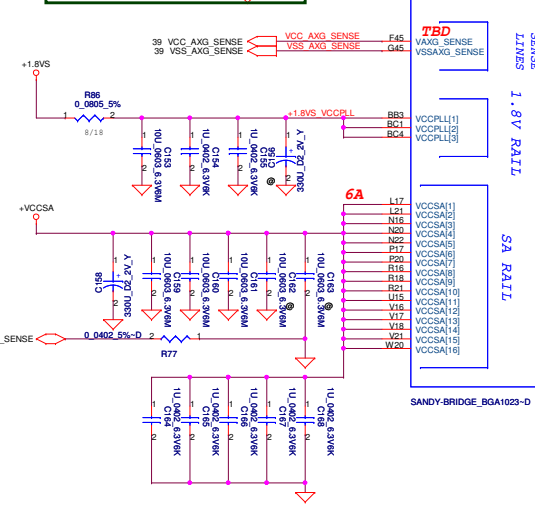
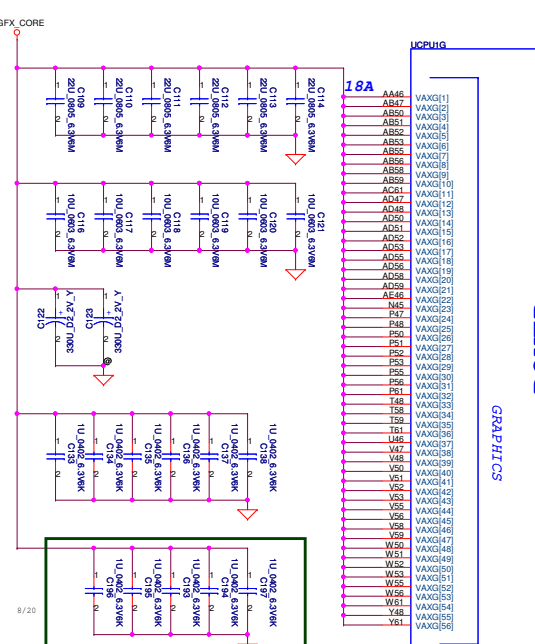
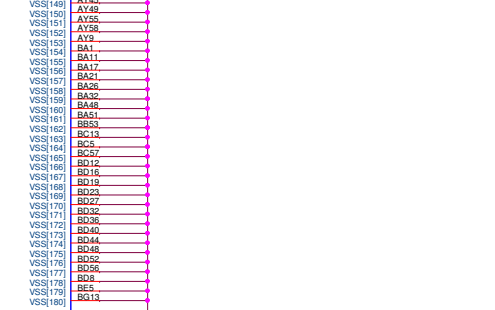
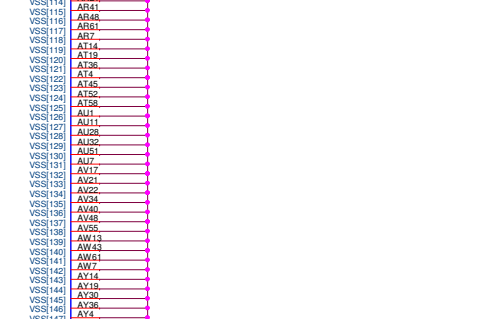
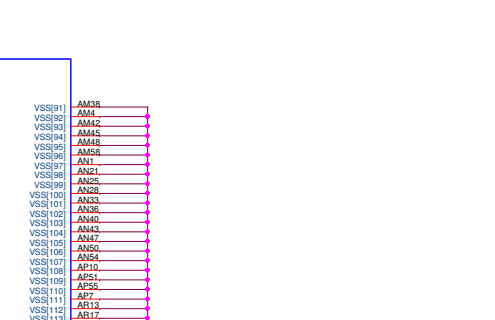
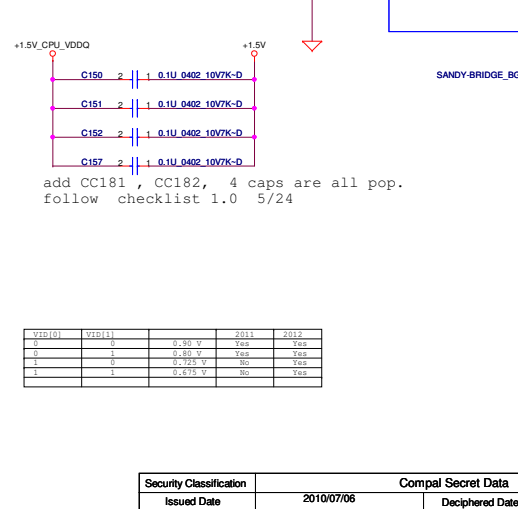
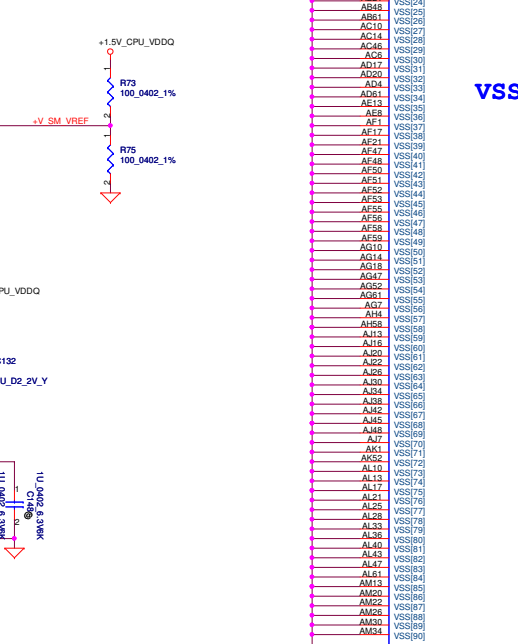
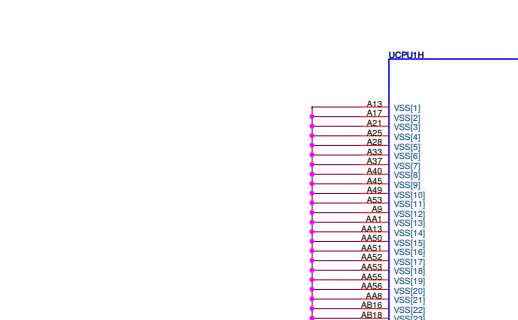
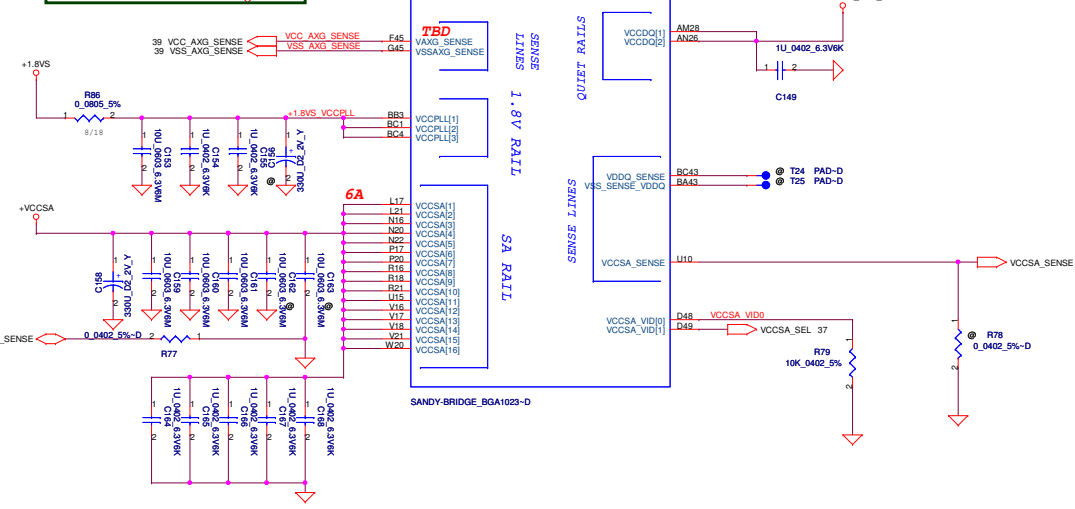
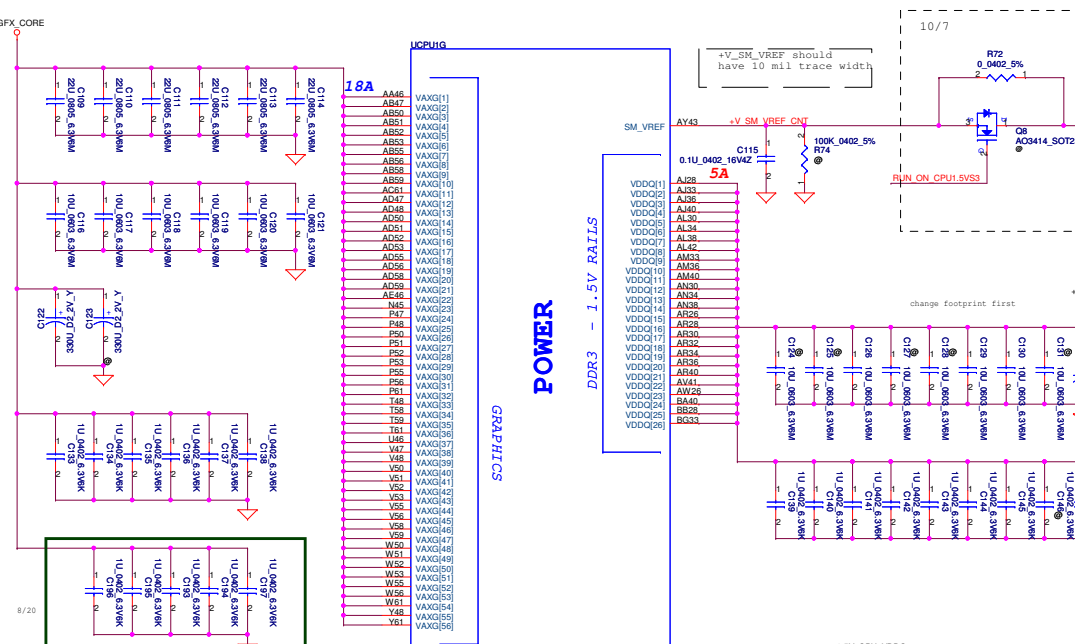
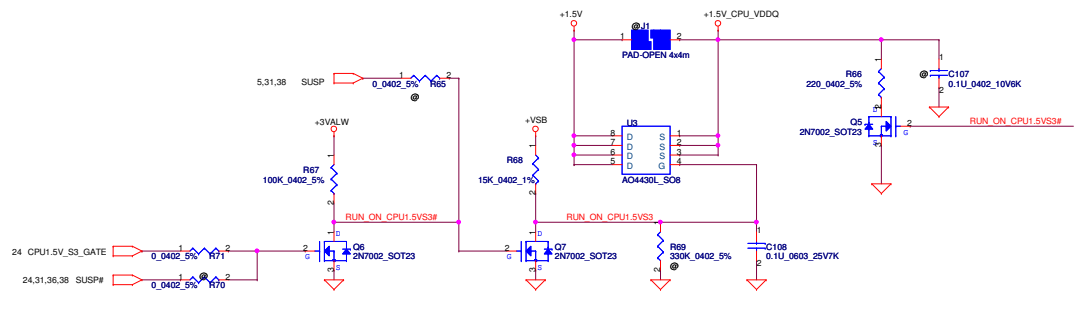
PEG DEFER TRAINING	
CFG7	*1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



POWER

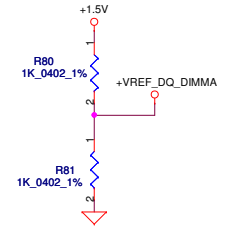
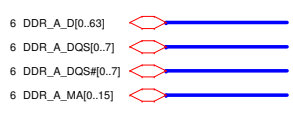
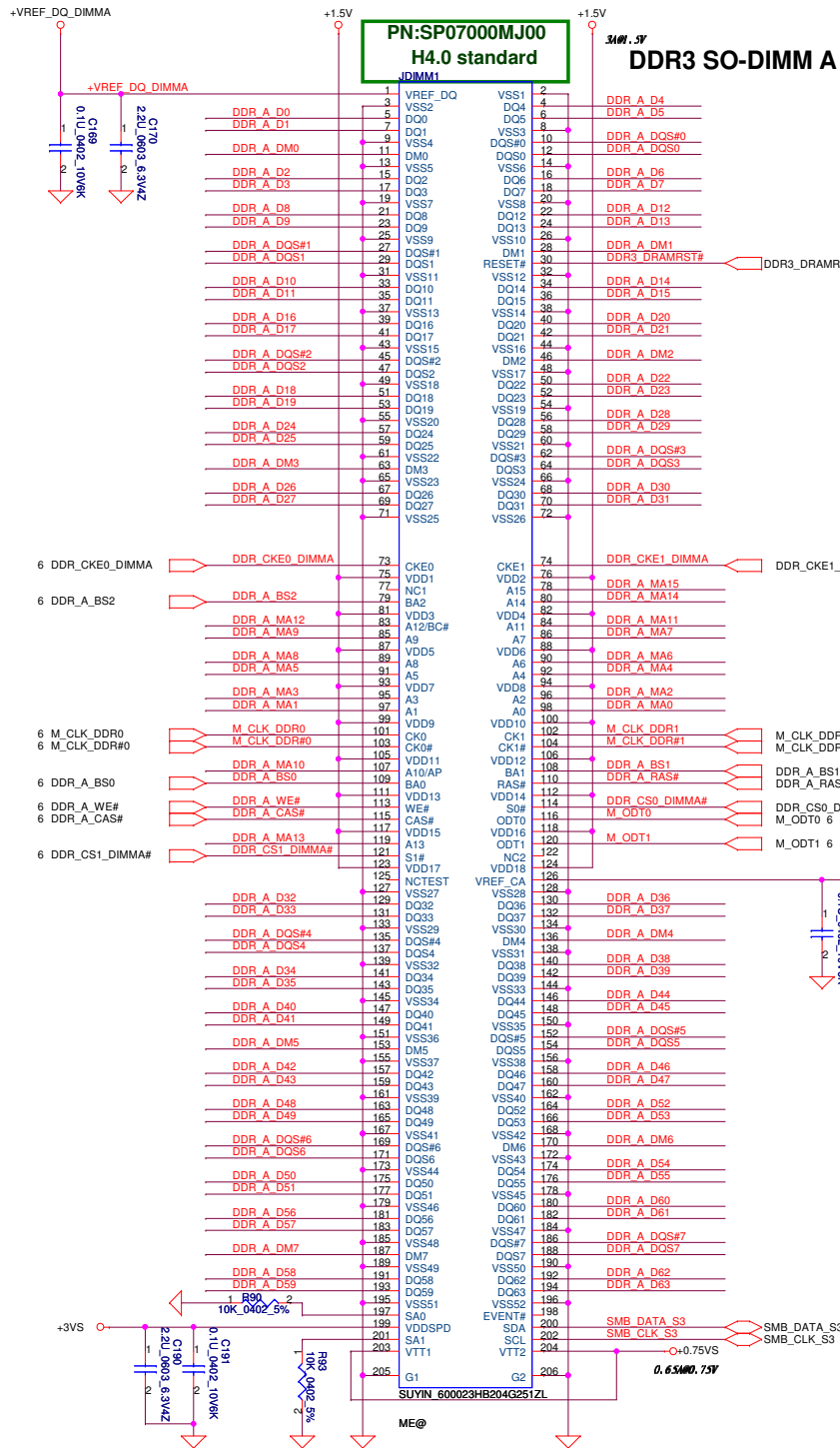


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				Document Number LA-7041P
				Rev 0.2
				Date: Wednesday, November 03, 2010 Sheet 8 of 40

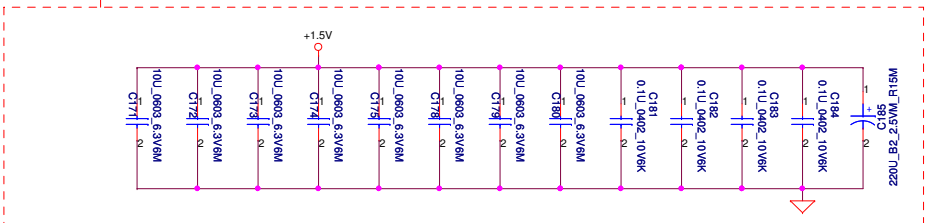


add CC181, CC182, 4 caps are all pop.
follow checklist 1.0 5/24

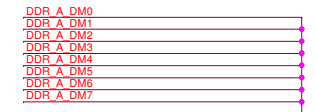
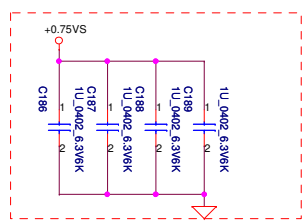
VDDIO	VSS[11]	0.90 V	2011	2012
0	1	0.80 V	Yes	Yes
1	0	0.725 V	No	Yes
1	1	0.675 V	No	Yes



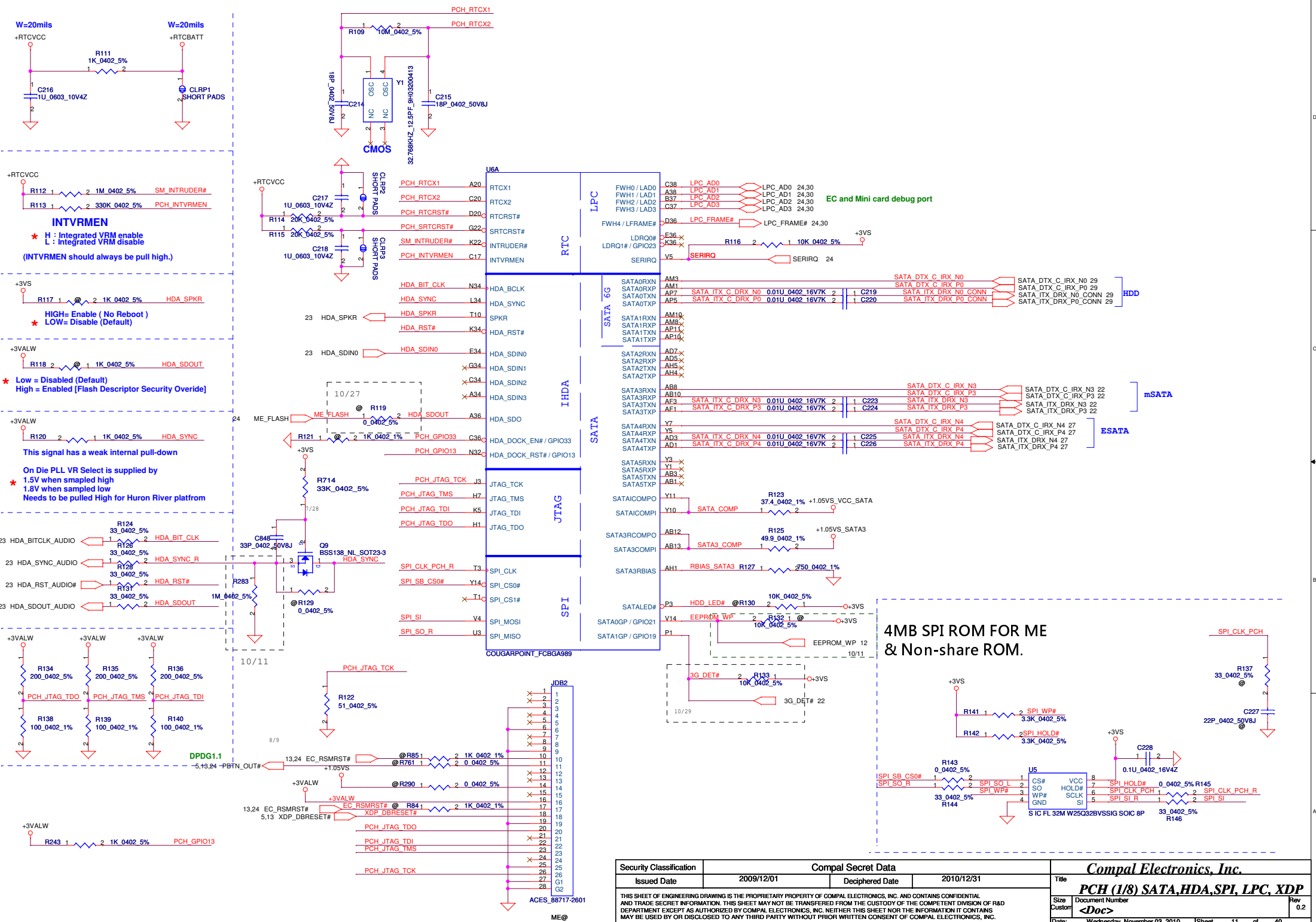
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Place near DIMM



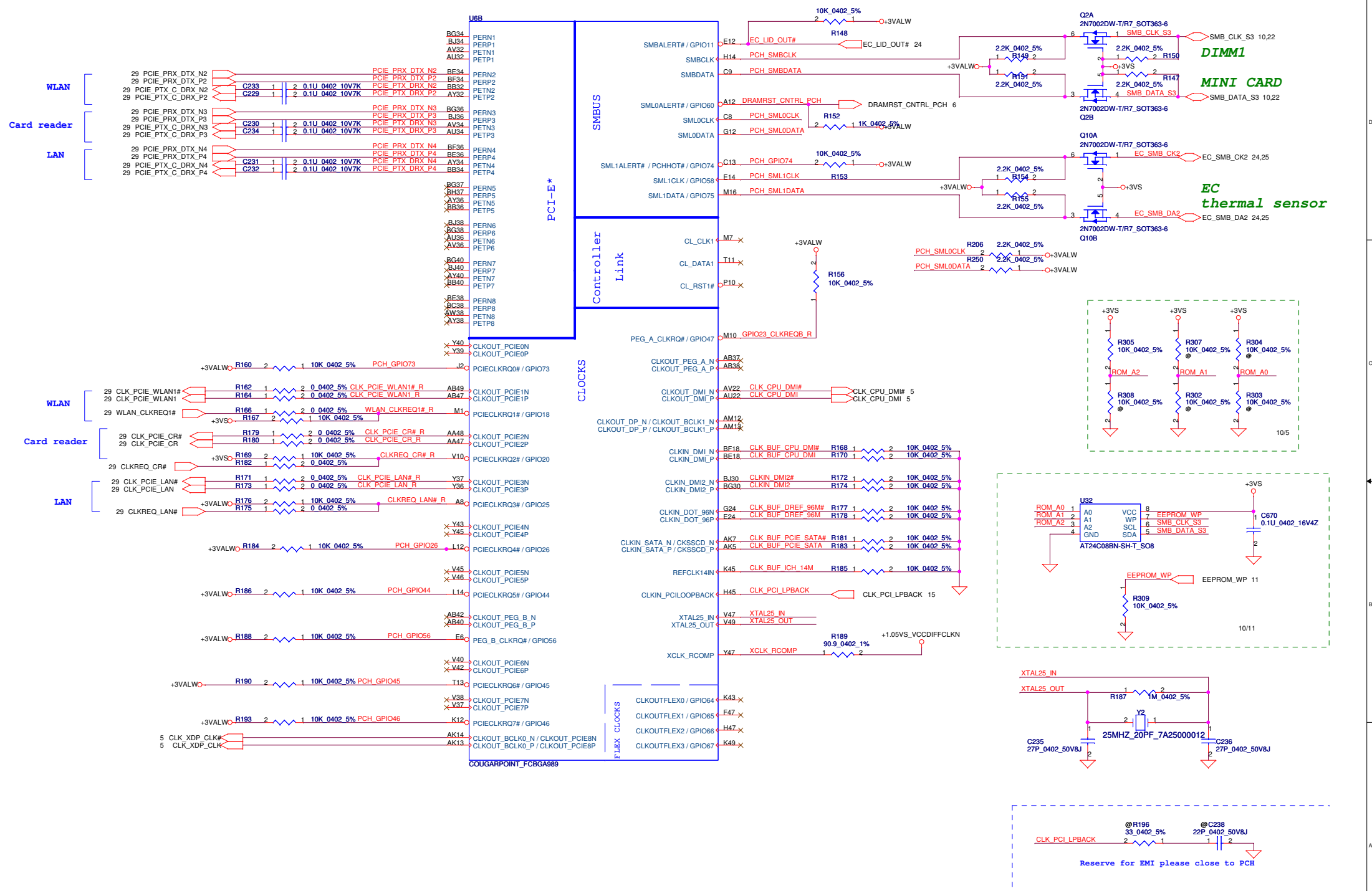
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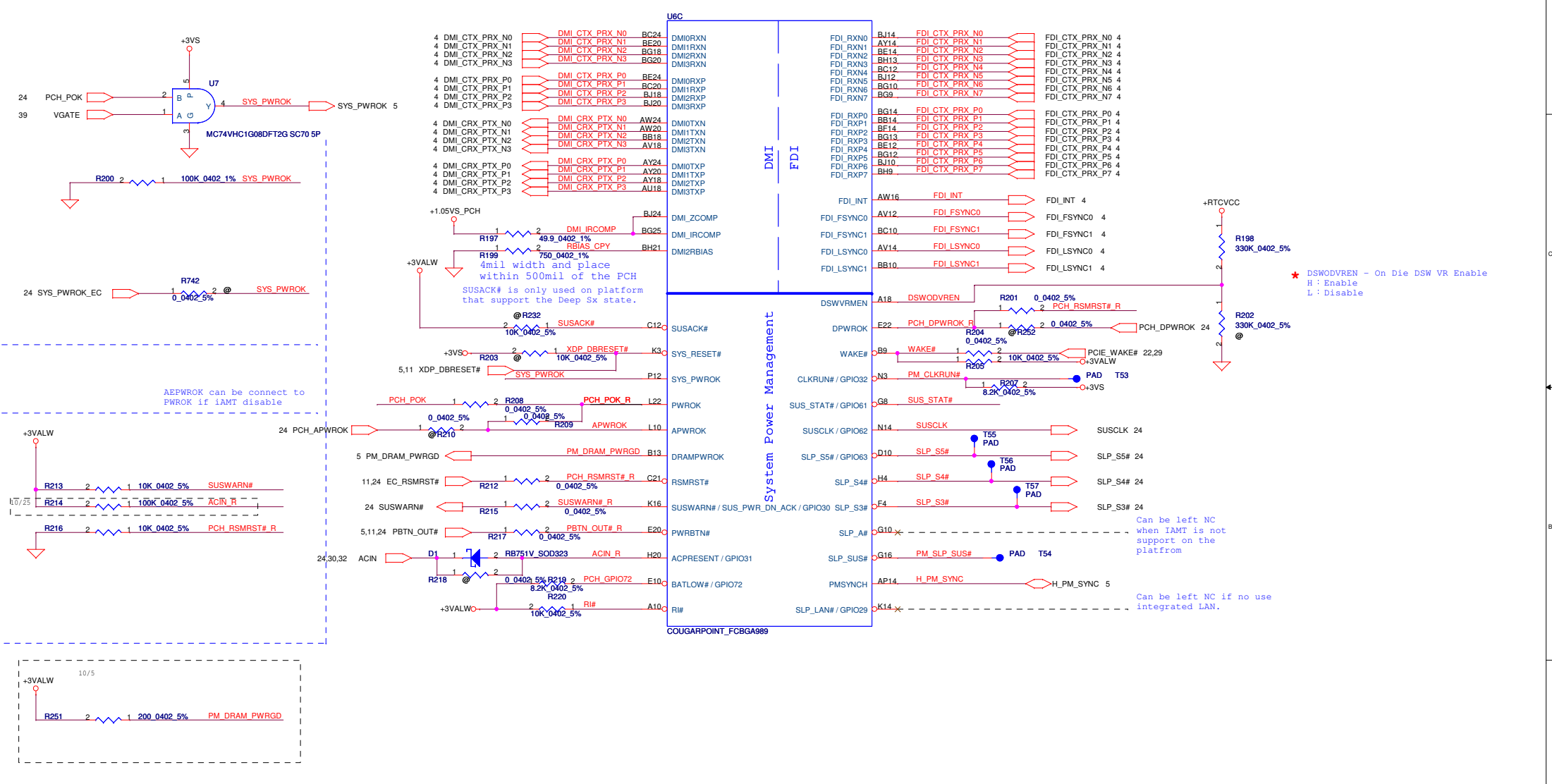
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Customer	Document Number	<Doc>		0.2	
Date:	Wednesday, November 03, 2010	Sheet	10	of 40	



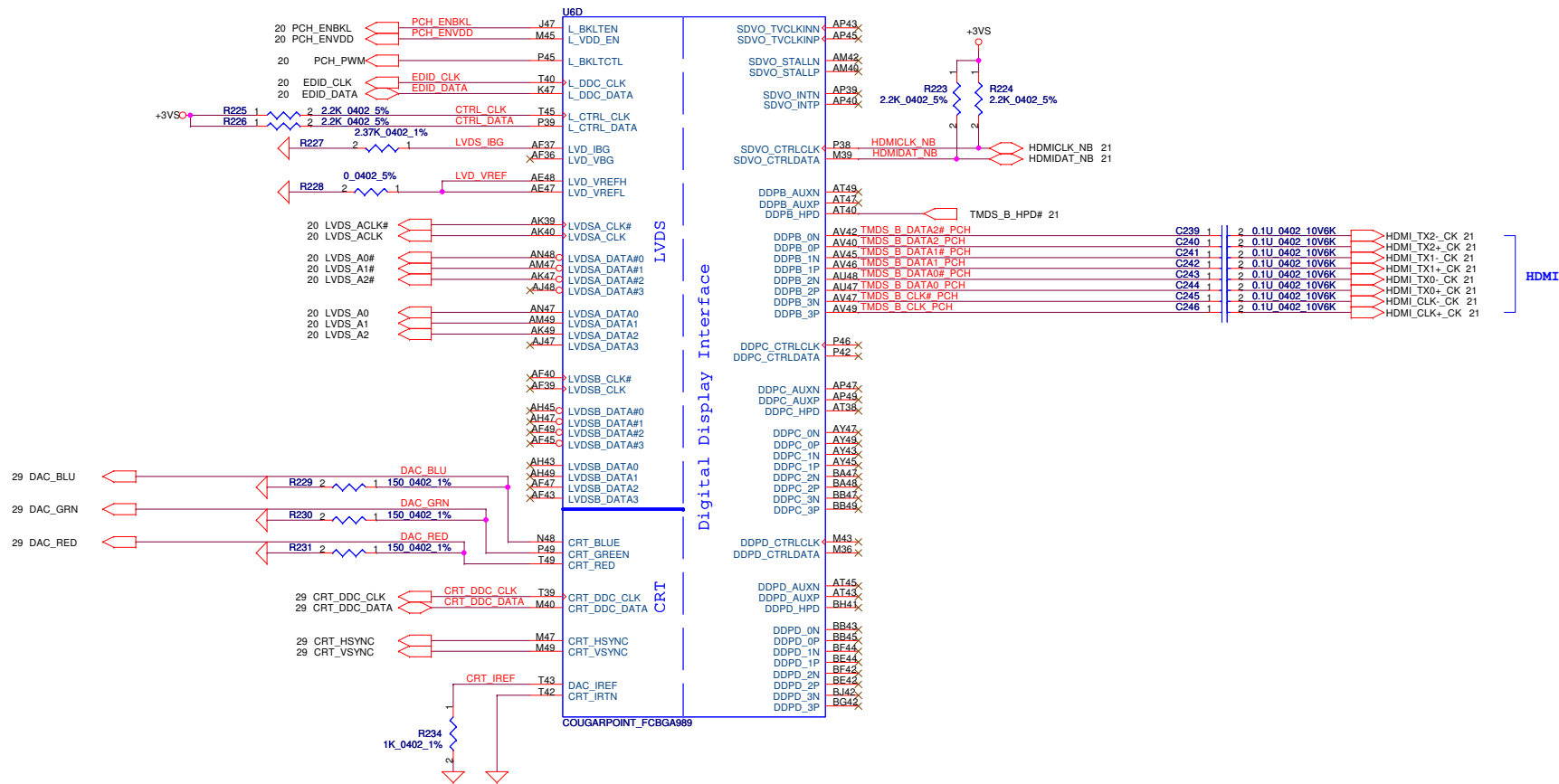
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Size	Document Number			Rev	
Customer	<Doc>			0.2	
Date:	Wednesday, November 03, 2010	Sheet	11	of 40	



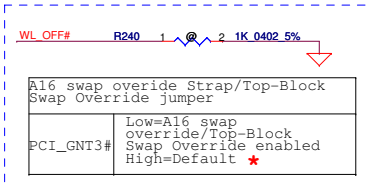
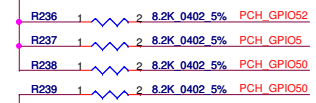
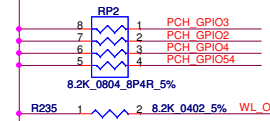
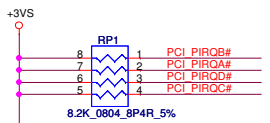
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Issued Date	2009/12/01	Deciphered Date	2010/12/31	Compal Electronics, Inc. PCH (2/8) PCIE, SMBUS, CLK	
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Size	Document Number	Rev		Date	
Custom	<Doc>	0.2		Wednesday, November 03, 2010	
Sheet		12		of 40	



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Size	Document Number	Date		Sheet	Rev
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				of	40



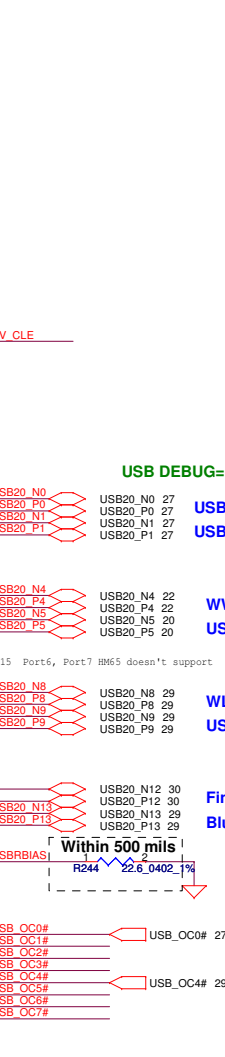
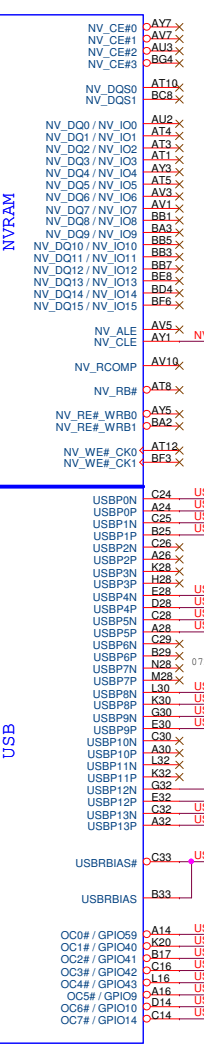
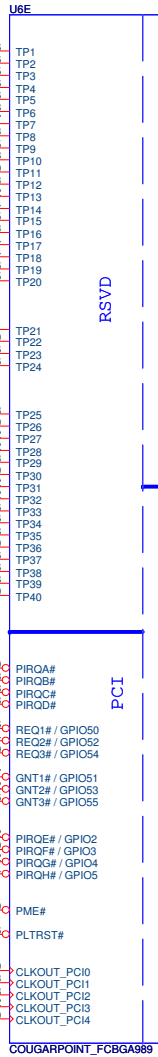
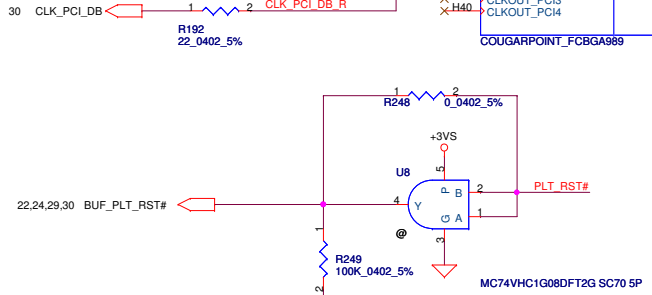
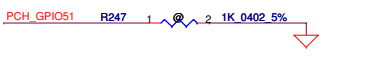
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Date:	Wednesday, November 03, 2010	Sheet	14	of	40



A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low=A16 swap override/Top-Block Swap Override enabled High=Default *

GPIO53=This Signal has a weak internal pull-up.
NOTE: The internal pull-up is disabled after PLTRST# deasserts.

Boot BIOS Strap bit1 BBS1		
GPIO51 Bit11	GPIO19 Bit10	Boot BIOS Destination
0	1	Reserved
1	0	Reserved
1	1	* SPI (Default)
0	0	LPC



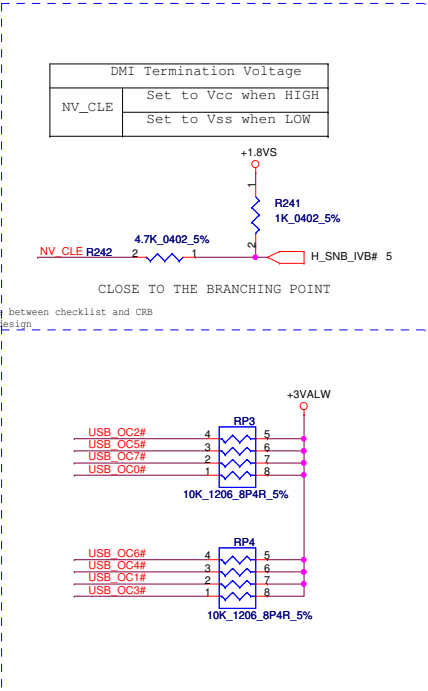
USB DEBUG=PORT1 AND PORT9

USB (COMBO) USB

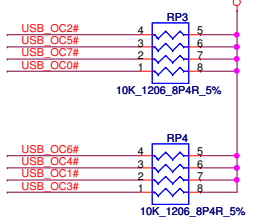
WWAN USB Camera

WLAN USB charger

Finger Printer Bluetooth



It's difference between checklist and CRB Here is CRB's design



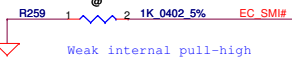
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Size			Rev	
Date: Wednesday, November 03, 2010			15 of 40	

Compal Electronics, Inc.	
PCH (5/9) PCI, USB	
<Doc>	
Rev 0.2	

6/24 Change to @ follow module design and double check on module design meeting

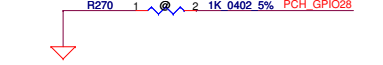
ICC_EN#
Integrated Clock Chip Enable

H ; Disable
L ; Enable



GPIO28
On-Die PLL Voltage Regulator

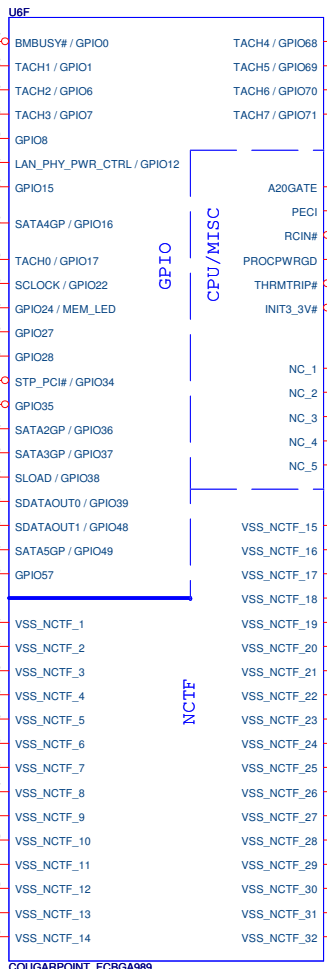
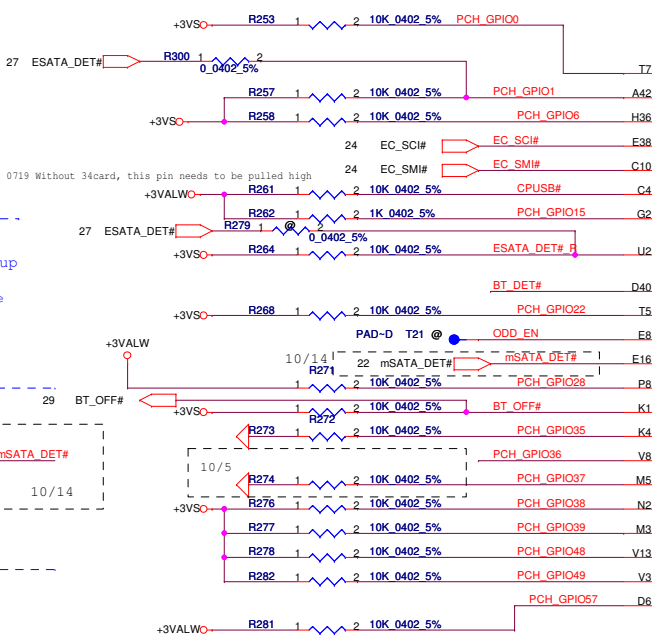
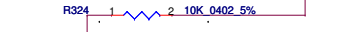
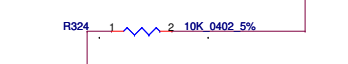
This signal has a weak internal pull up
H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable



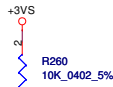
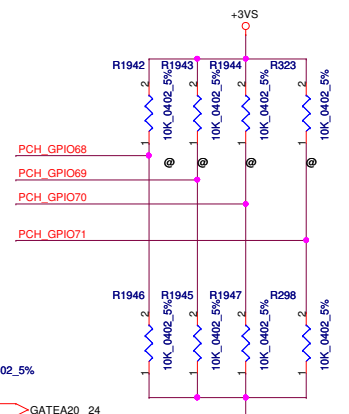
mSATA_DET#



PCH_GPIO36



COUGARPOINT_FCBGA989

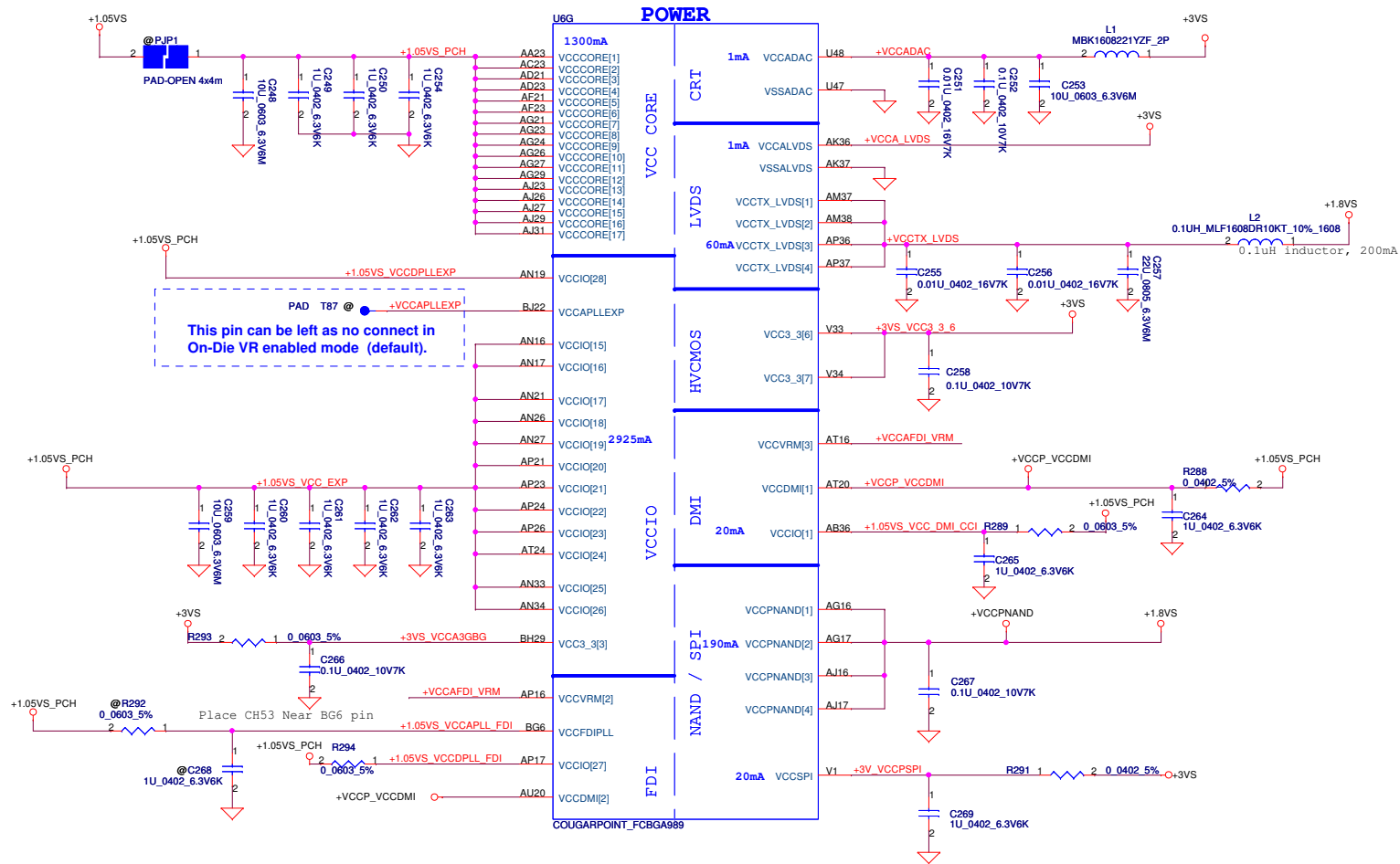


INIT3_3V
This signal has weak internal PU, can't pull low

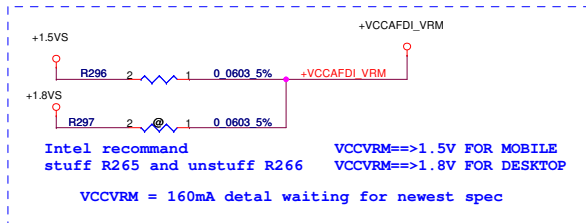
Intel schematic review recommend.

PCH_GPIO69	PCH_GPIO70	PCH_GPIO71	Function
0	0	0	UMA

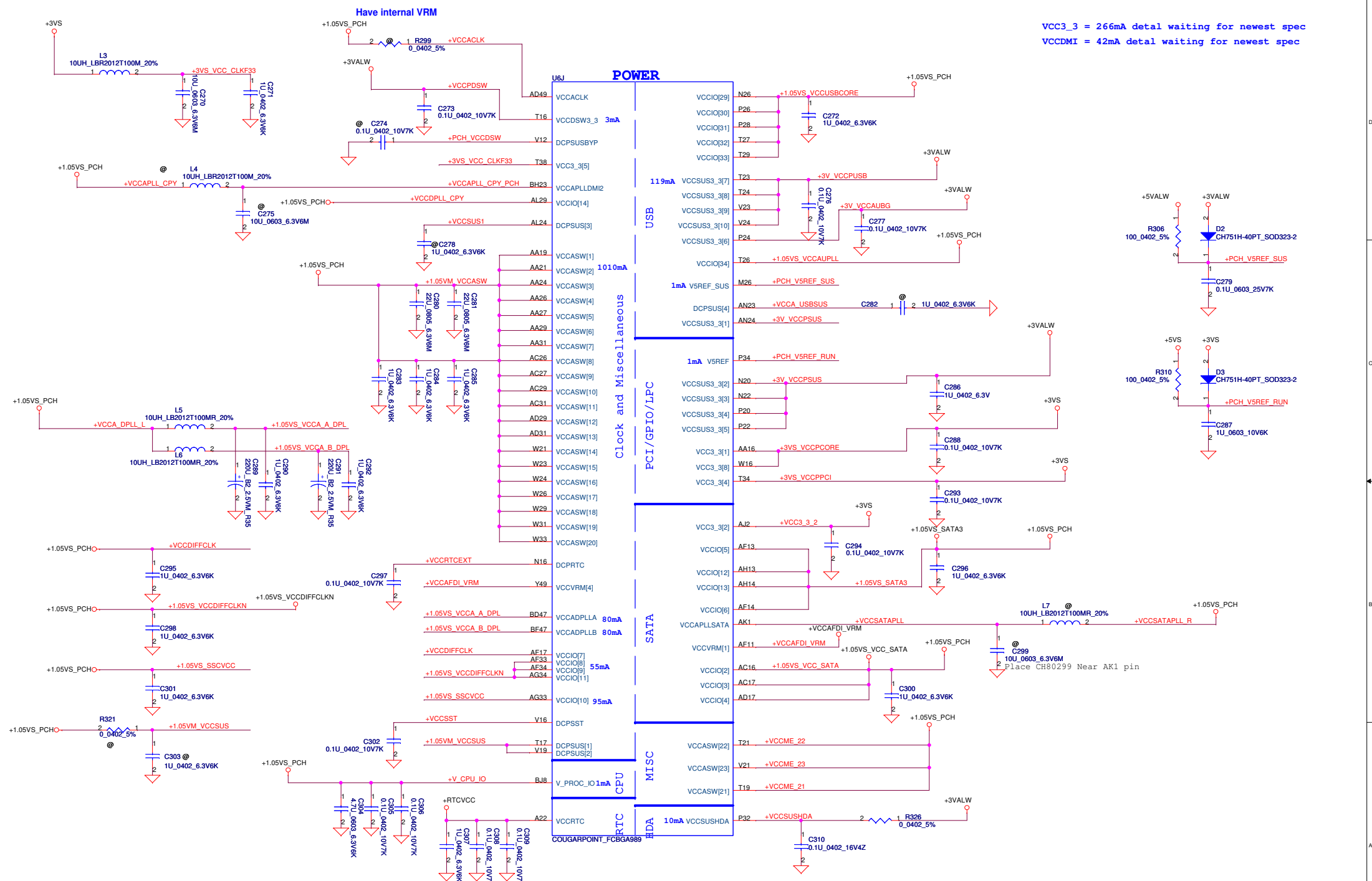
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				Sheet	16 of 40
				Rev	0.2



This pin can be left as no connect in On-Die VR enabled mode (default).

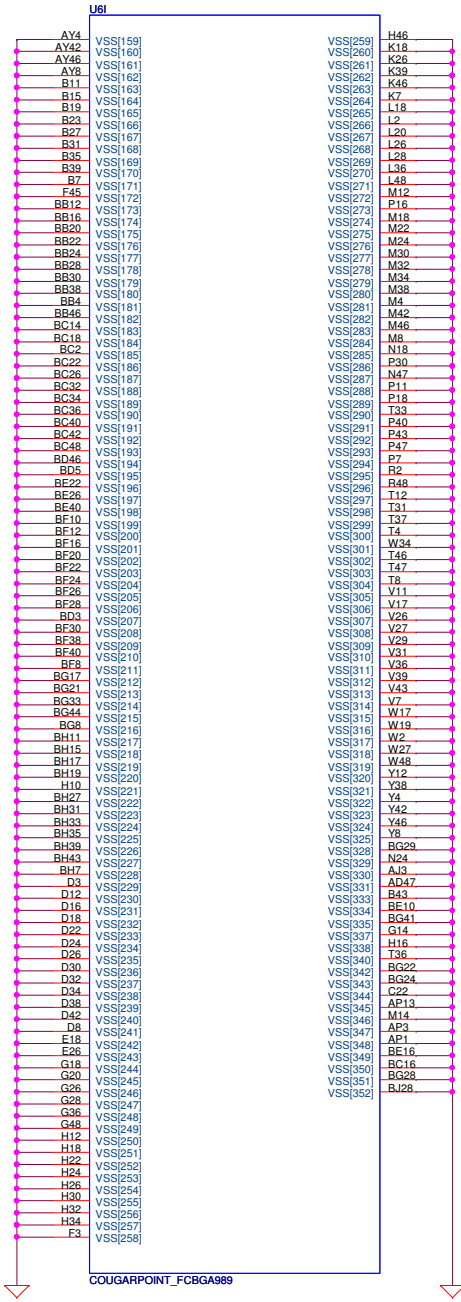
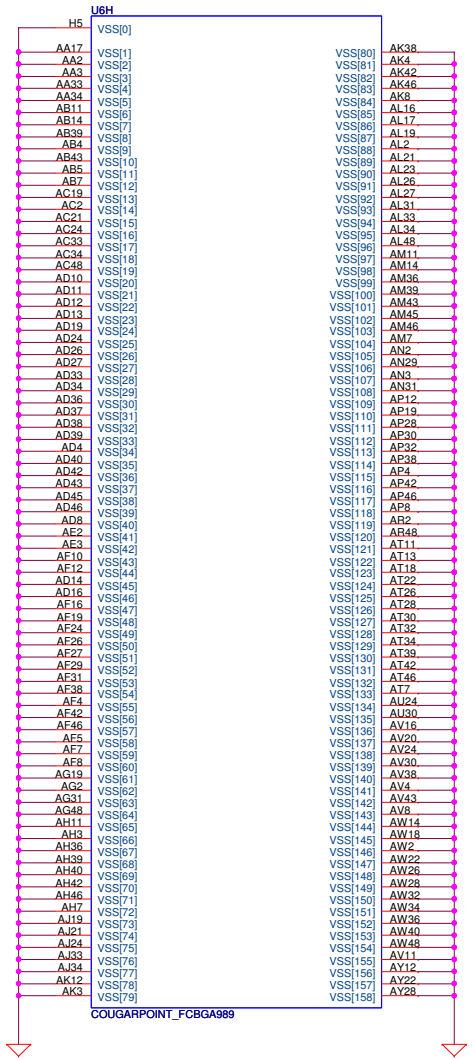


PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06



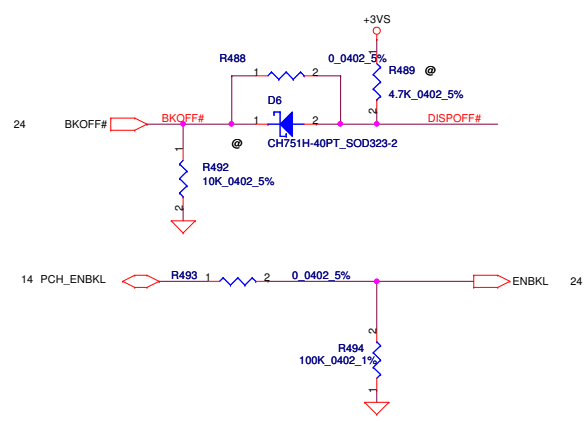
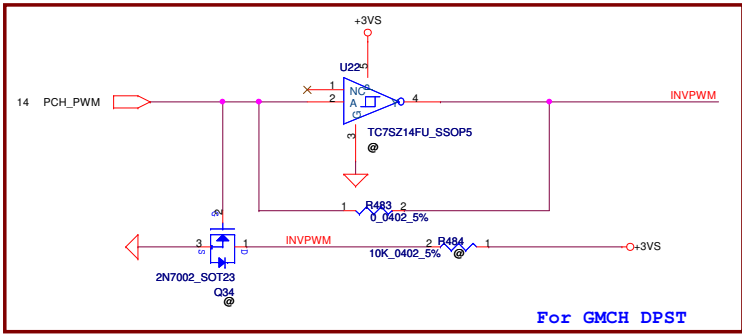
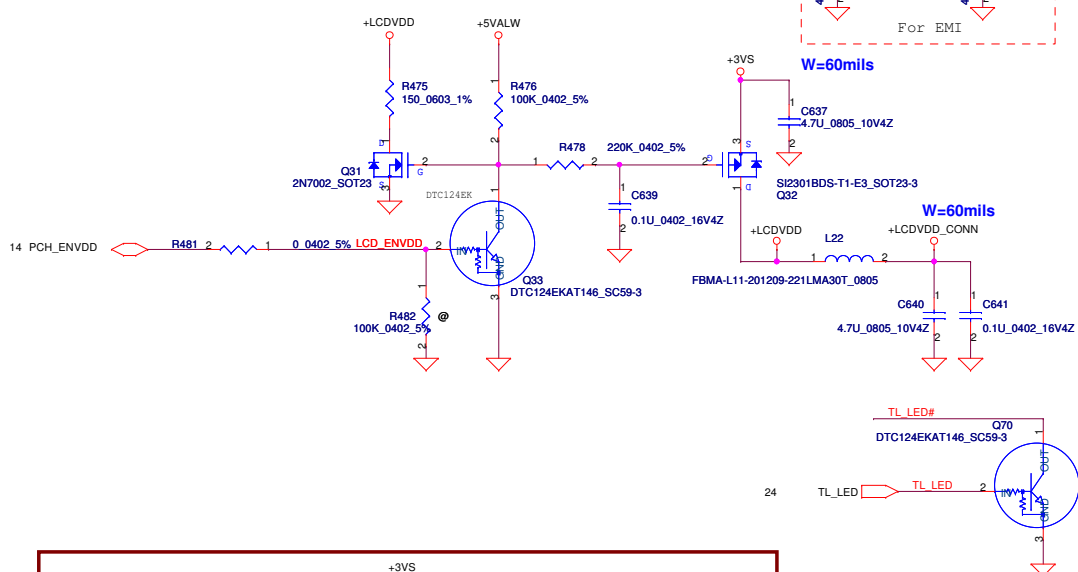
VCC3_3 = 266mA detal waiting for newest spec
 VCCDMI = 42mA detal waiting for newest spec

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Date:	Wednesday, November 03, 2010	Sheet	18	of	40
Rev	0.2				

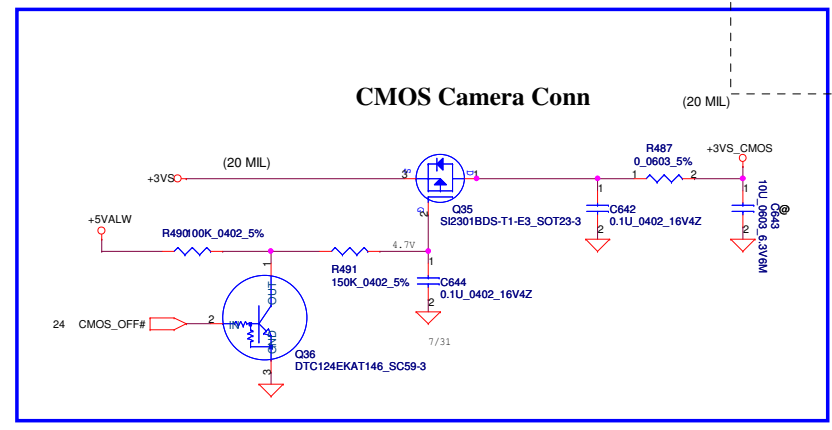
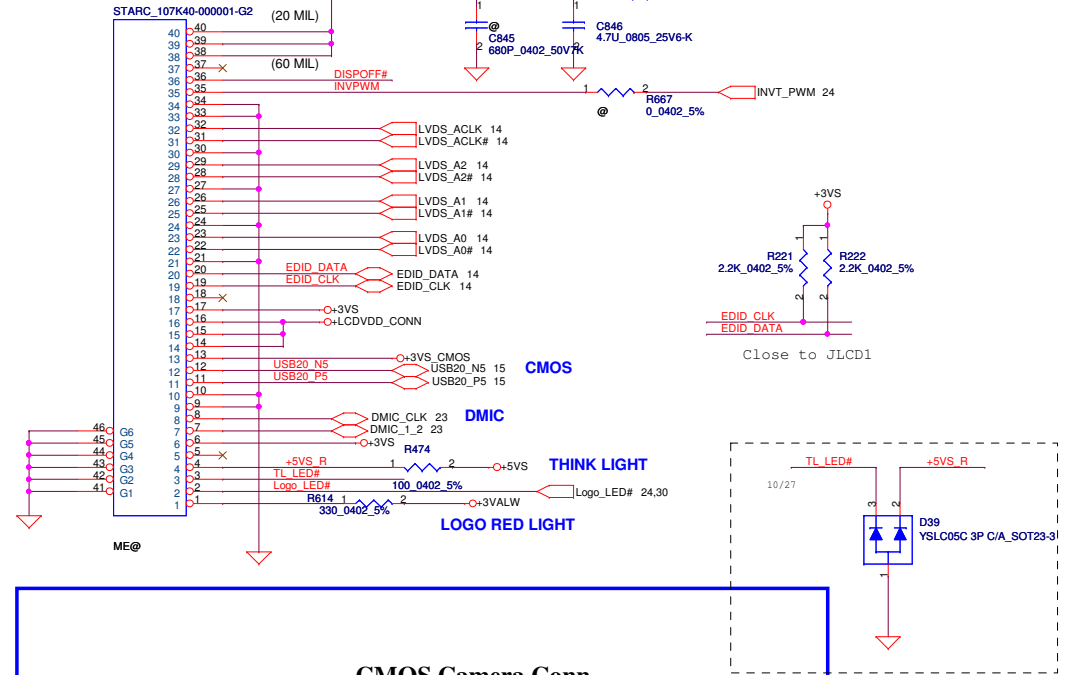


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Date:	Wednesday, November 03, 2010			Sheet	19 of 40

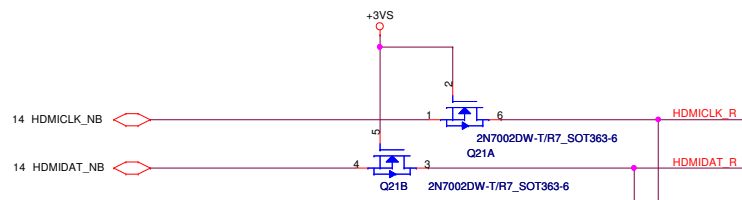
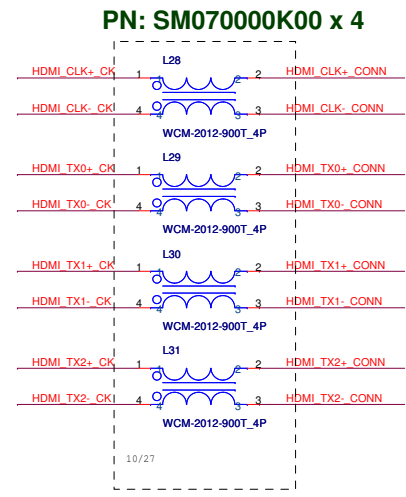
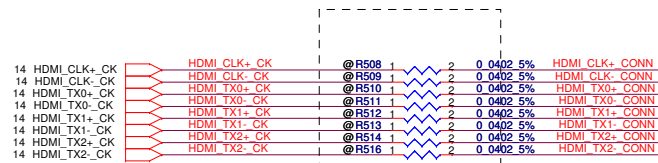
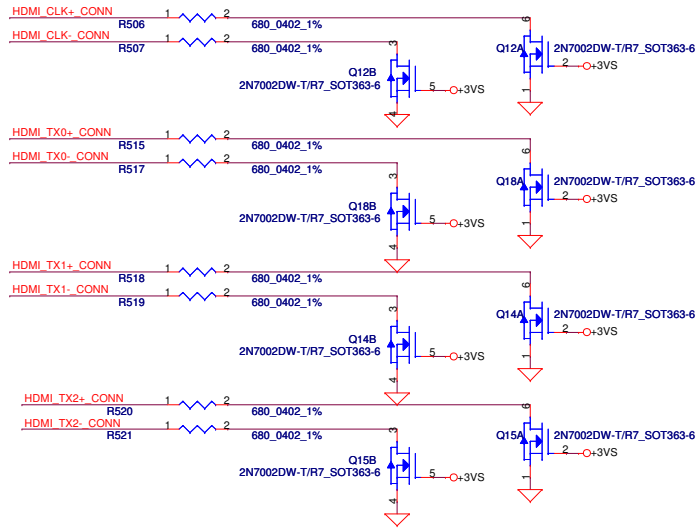
LCD POWER CIRCUIT



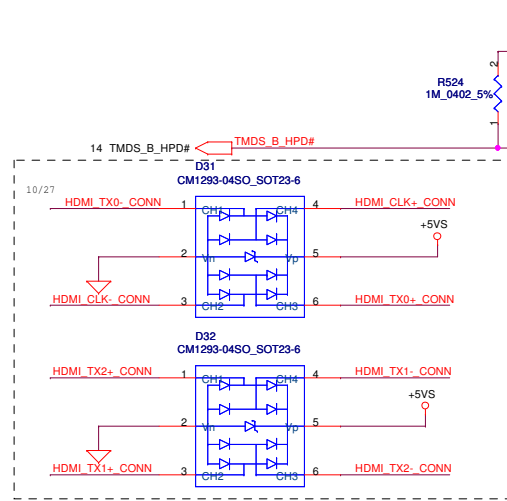
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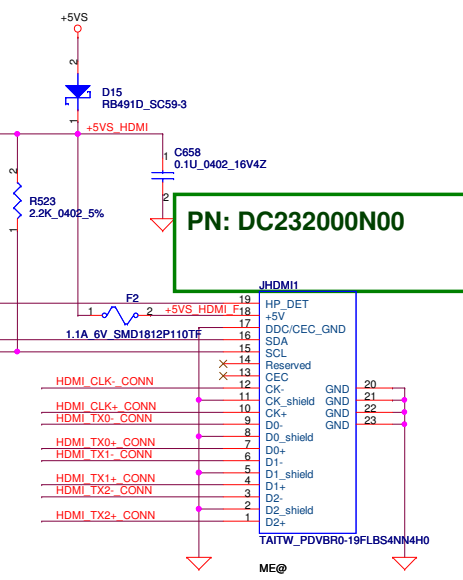
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Date:	Wednesday, November 03, 2010	Sheet	20	of 40	



PN: SCA0000U10



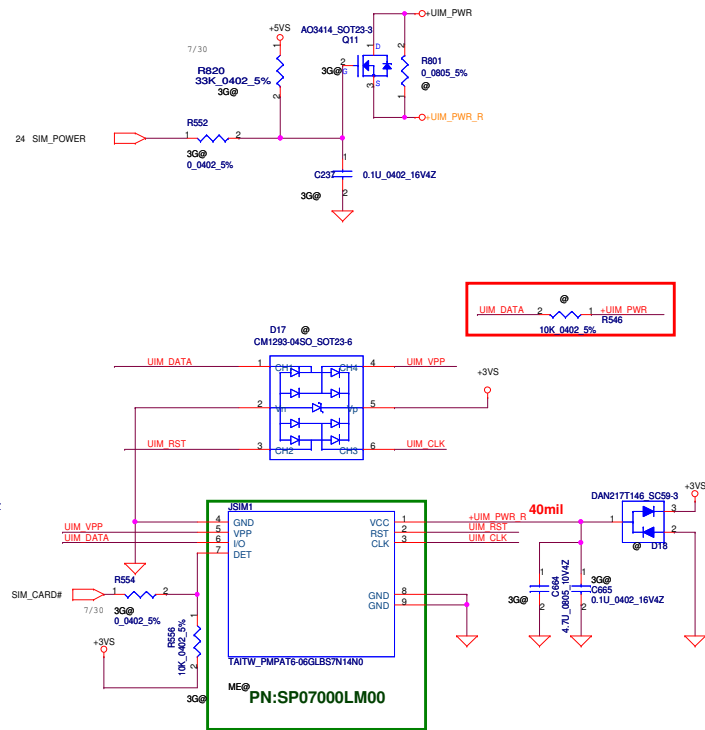
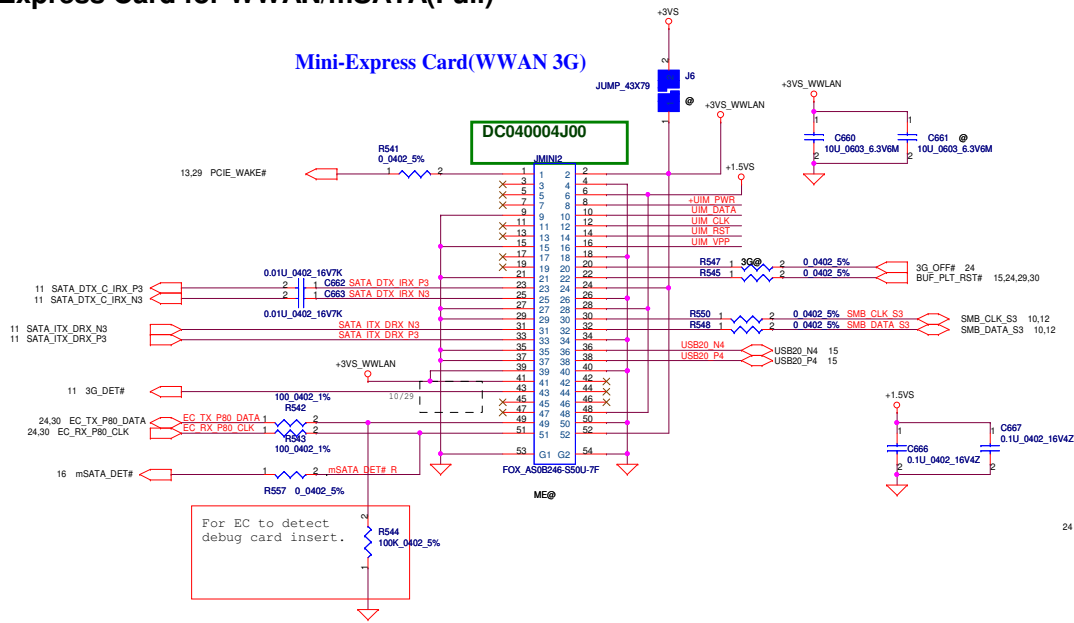
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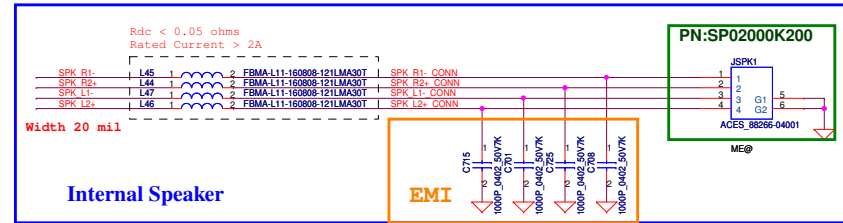
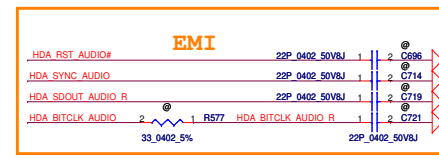
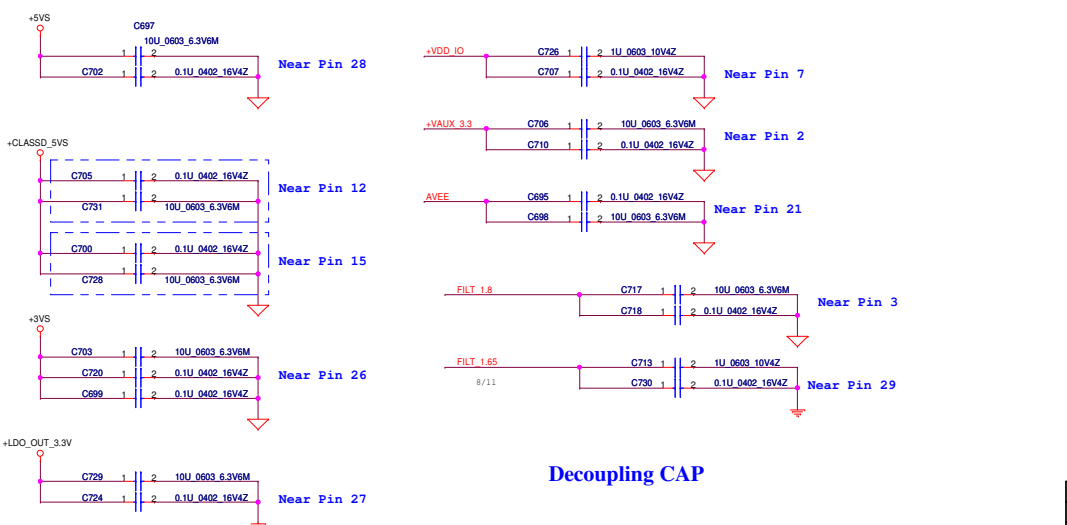
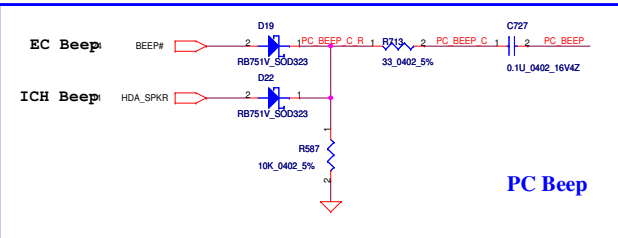
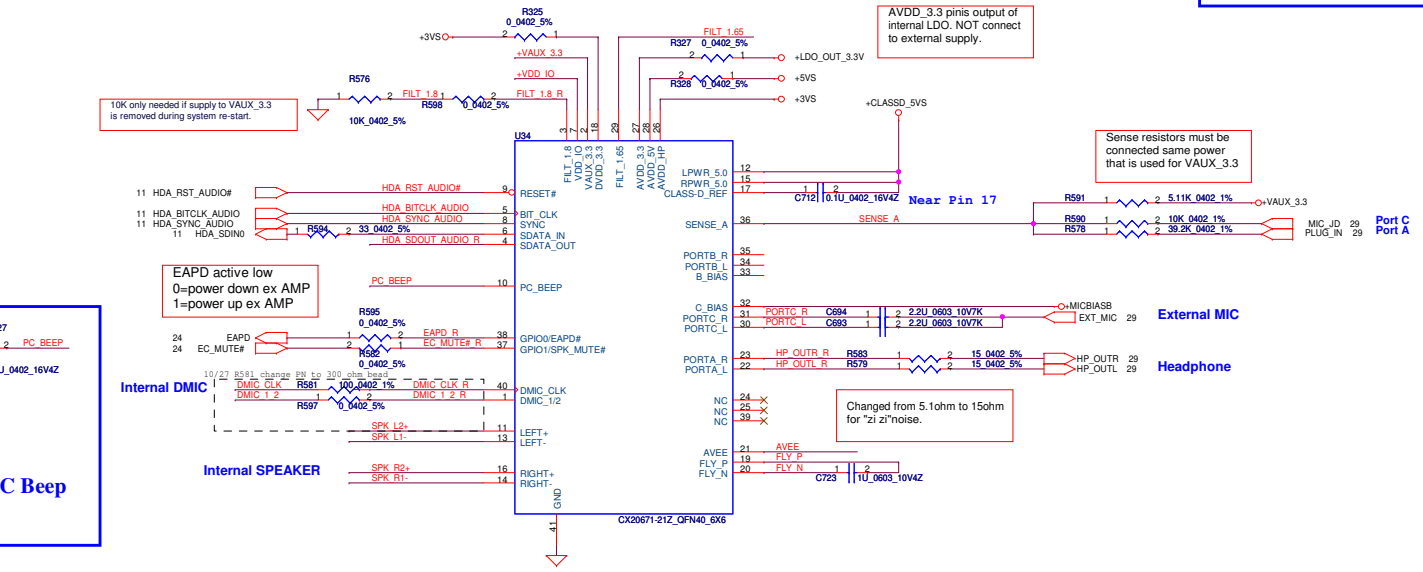
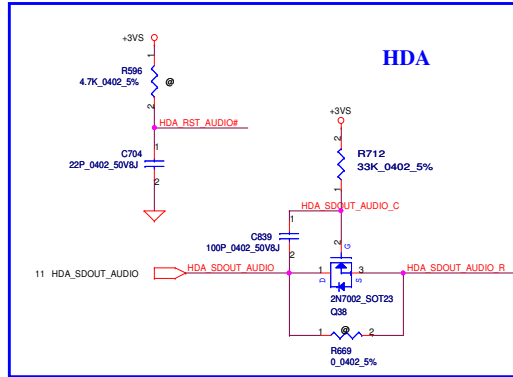
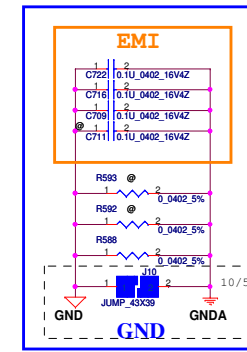
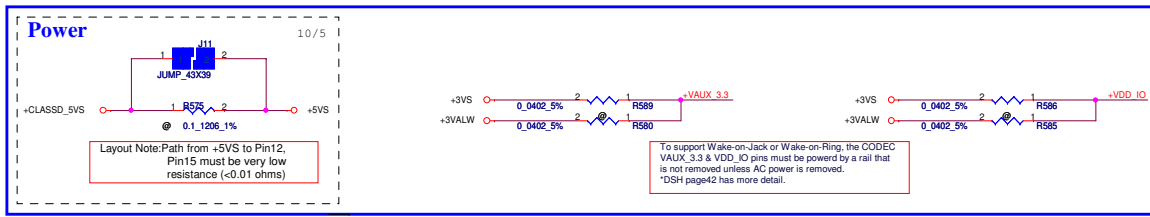
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				Sheet 21	of 40

Mini-Express Card for WWAN/mSATA(Full)

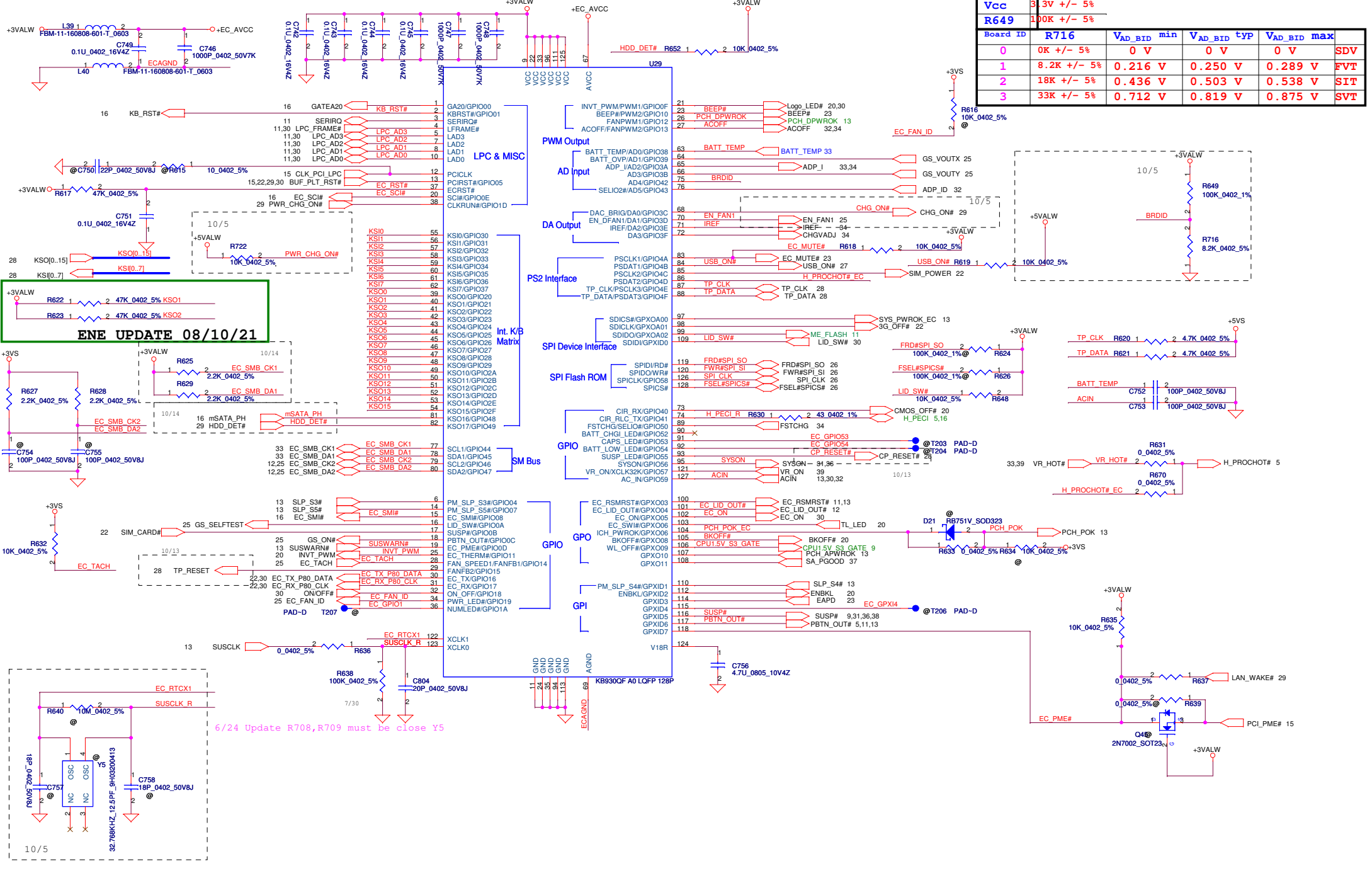
Mini-Express Card(WWAN 3G)



CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).



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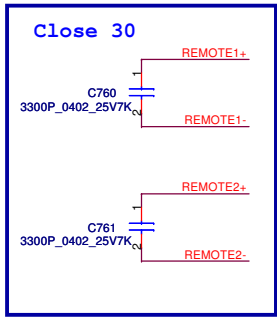


Board ID	R716	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	SDV
0	0K +/- 5%	0 V	0 V	0 V	SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	FVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	SIT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	SVT

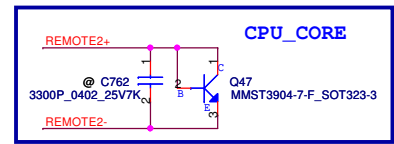
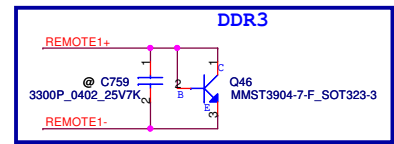
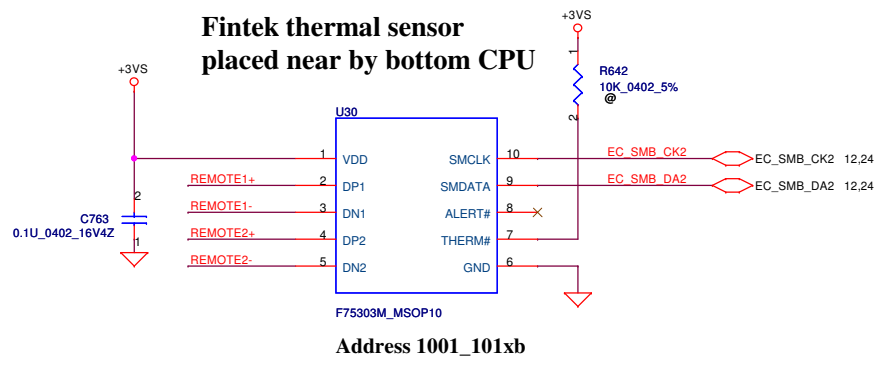
ENE UPDATE 08/10/21

6/24 Update R708, R709 must be close Y5

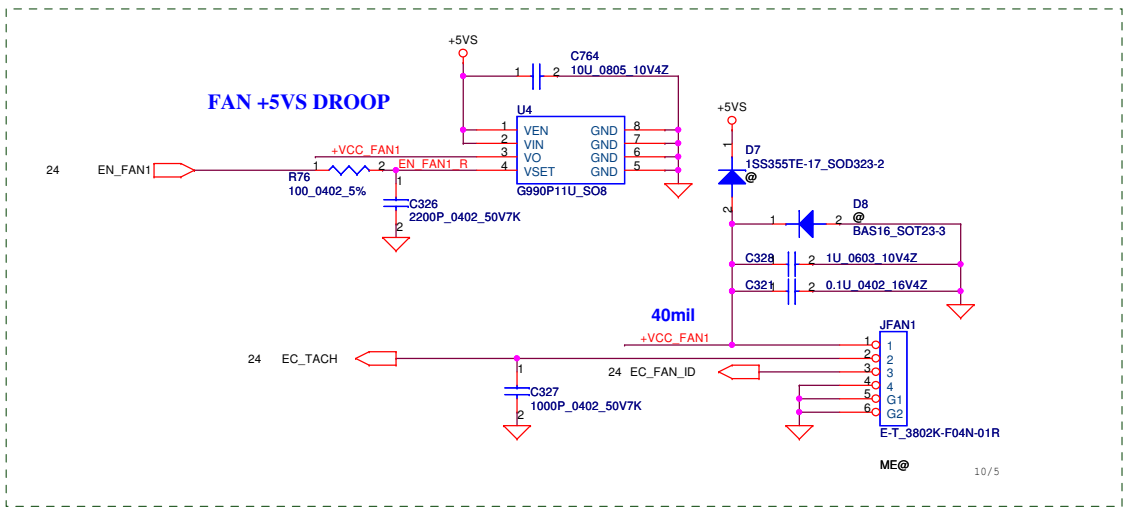
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				Date:	Wednesday, November 03, 2010
				Sheet	24 of 40



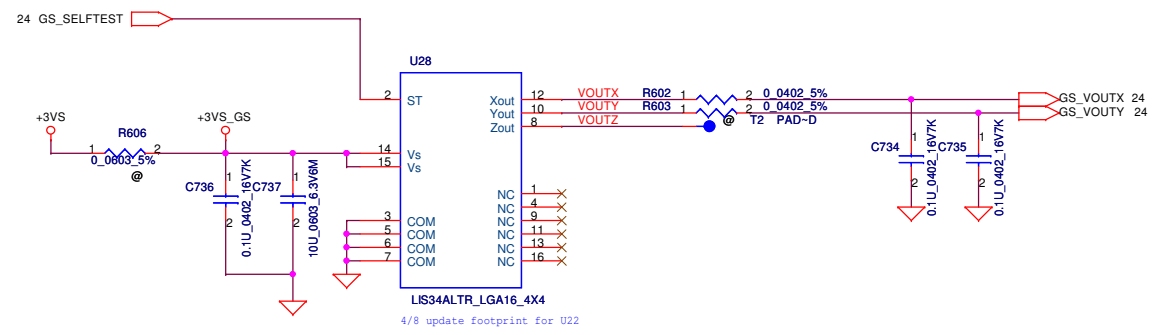
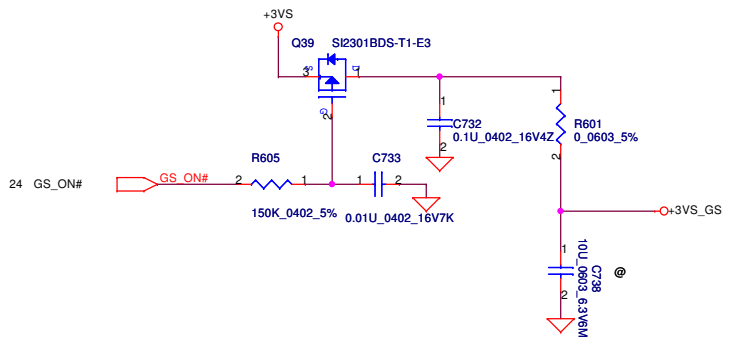
Fintek thermal sensor placed near by bottom CPU



REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

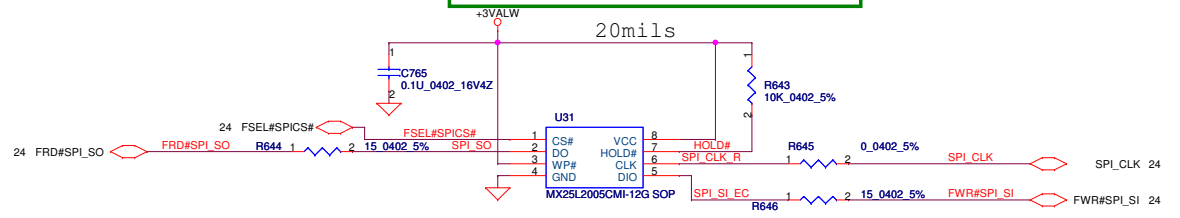


APS G-Sensor

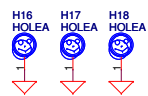


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Size Custom	Document Number	<Doc>		Rev 0.2
Date: Wednesday, November 03, 2010	Sheet 25	of 40		

**FOR EC 128KB SPI ROM
(150mil PACKAGE)
PN:SA00002C100**

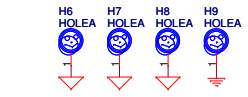


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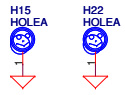
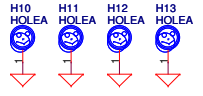


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H_2P3

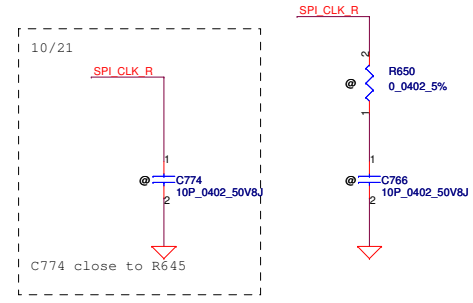


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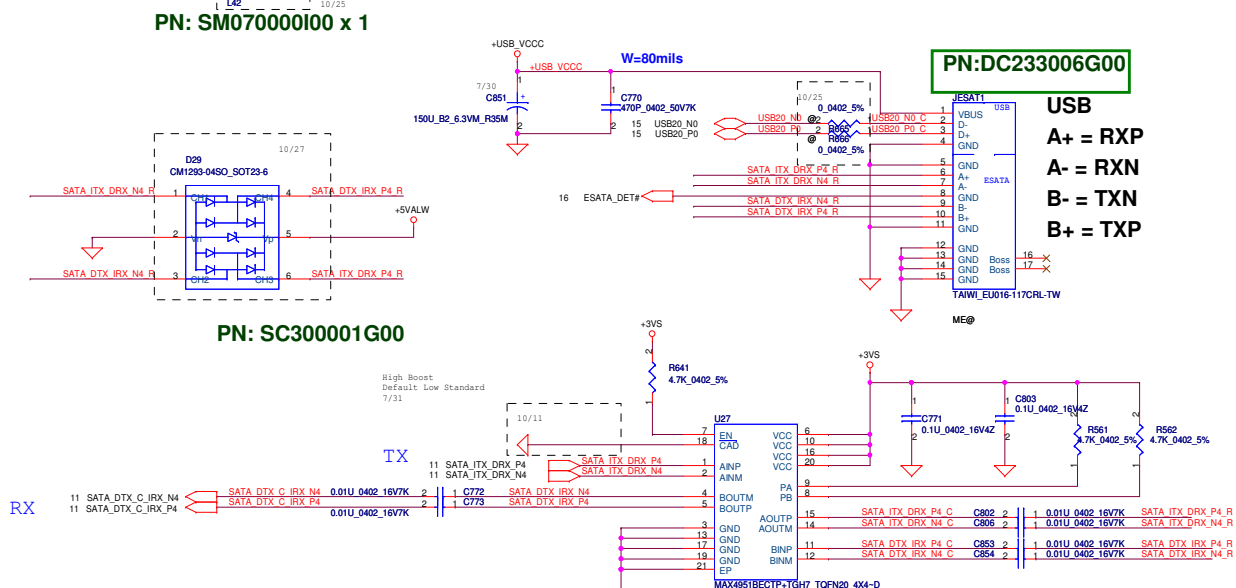
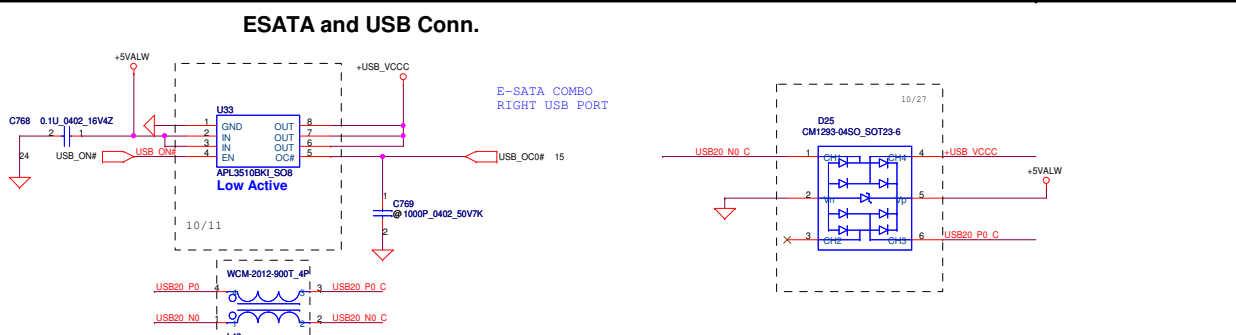
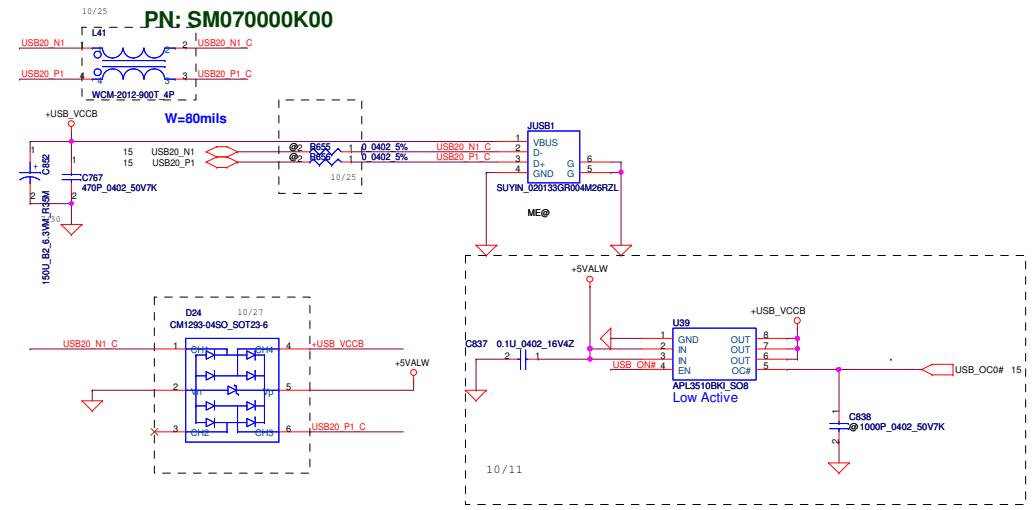


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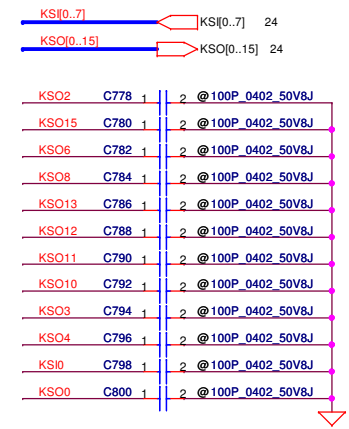


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				LA-5751P	0.2
Date: Wednesday, November 03, 2010				Sheet	26 of 40



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Date:	Wednesday, November 03, 2010	Sheet	27	of 40

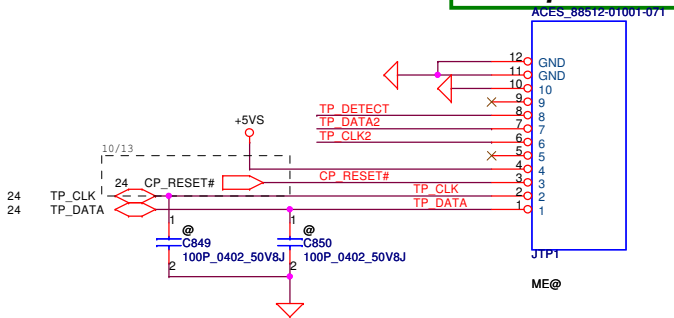
INT_KBD Conn.



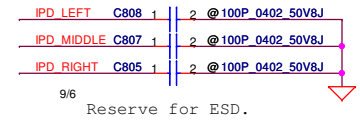
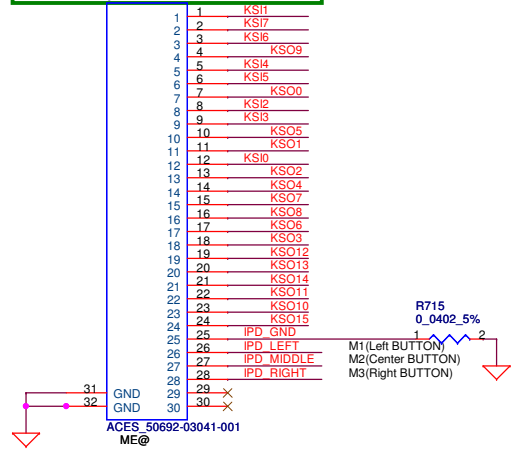
CONN PIN define need double check

PN:SP011007284(R)

Click pad 10PIN

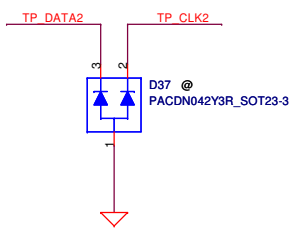
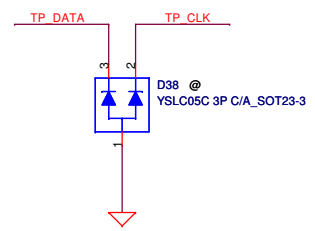
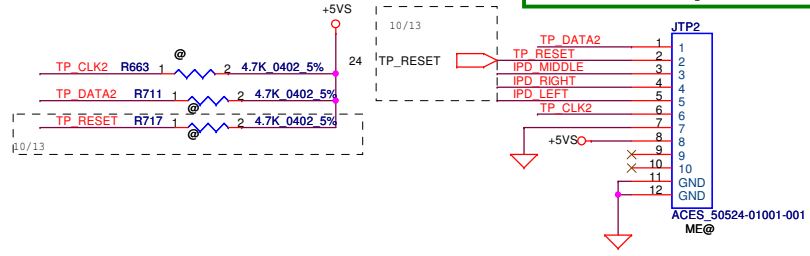


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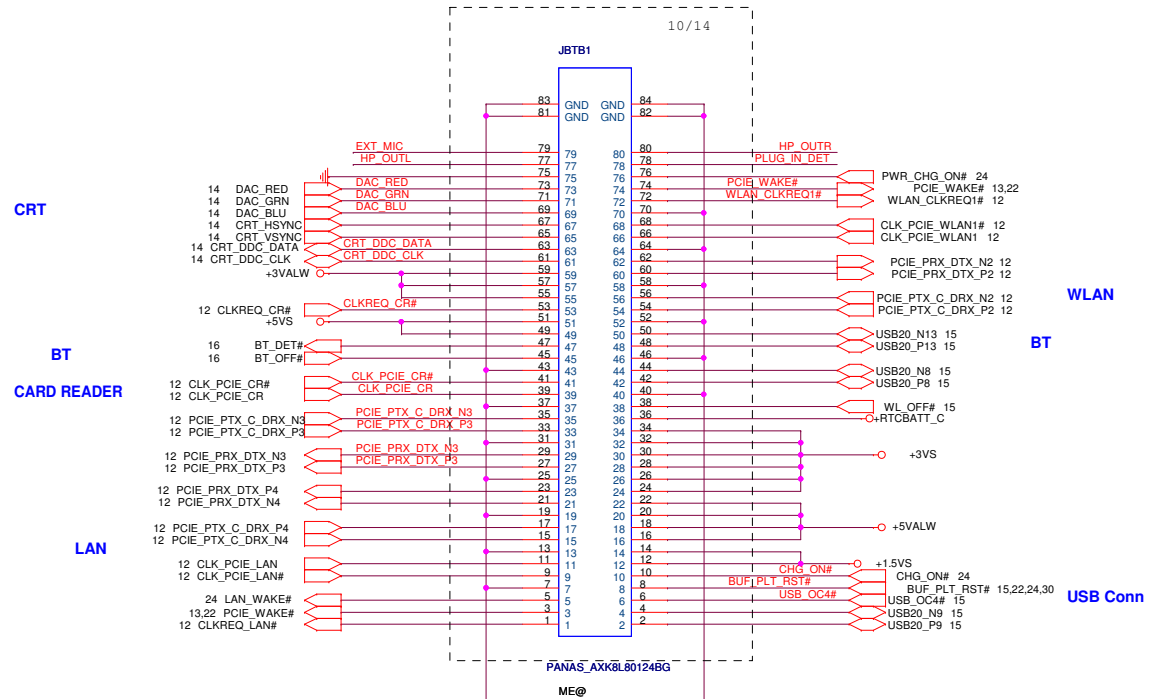
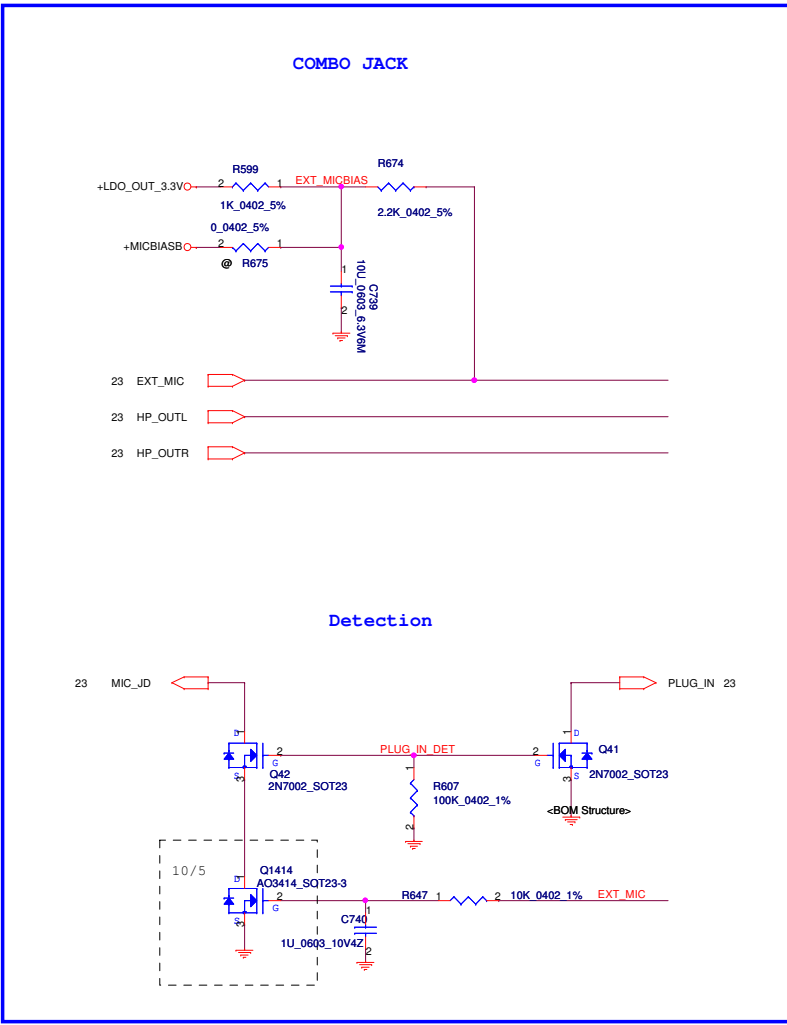
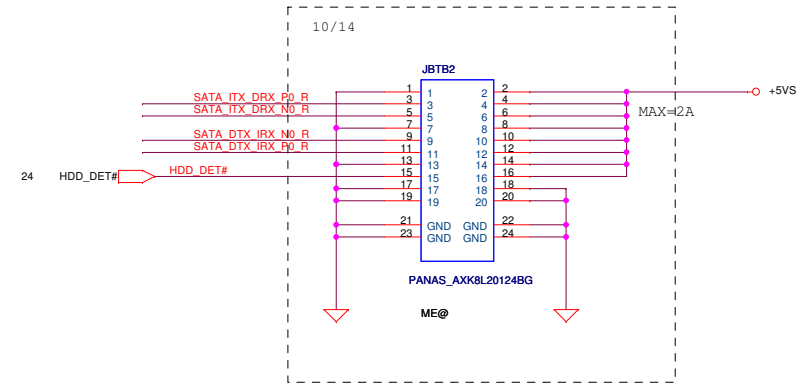
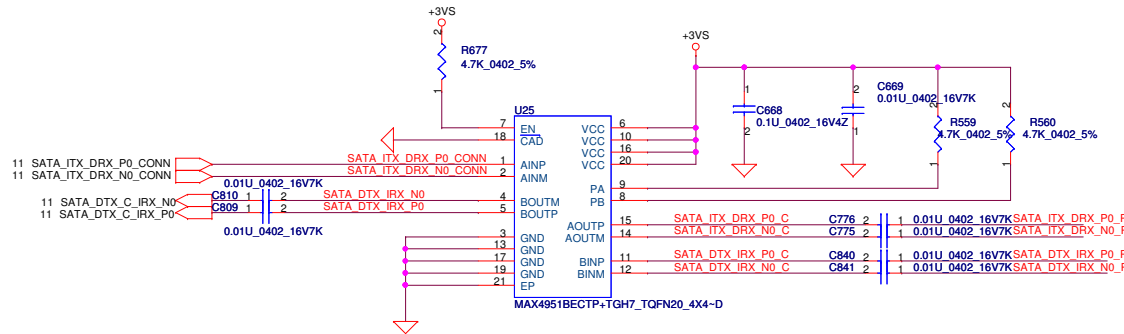
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Track point

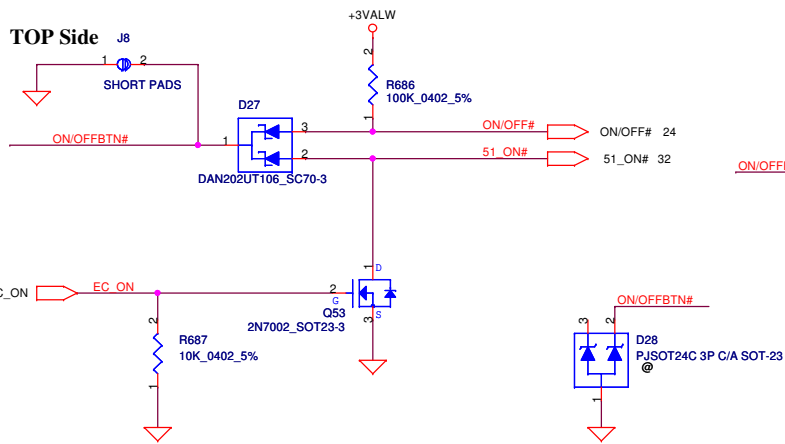


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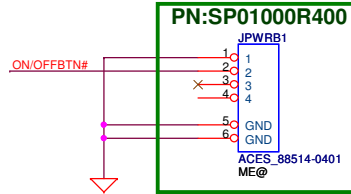
Compal Electronics, Inc.		
KB /TP		
Size Custom	Document Number LA-7041P	Rev 0.2
Date:	Wednesday, November 03, 2010	Sheet 28 of 40



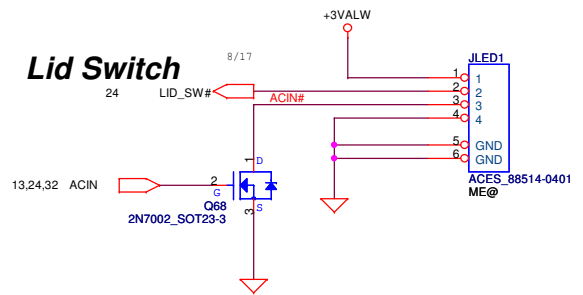
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			Compal Electronics, Inc. HDD/I/O BTB Connector	
Size	Document Number	Rev		
Custom		0.2		
Date:	Wednesday, November 03, 2010	Sheet	29	of 40



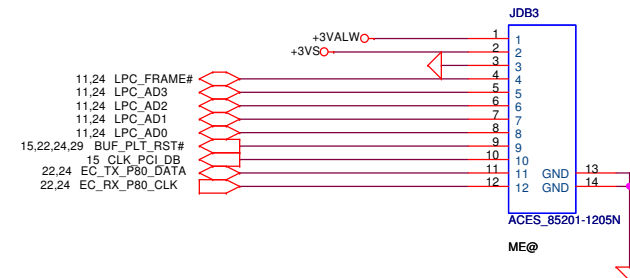
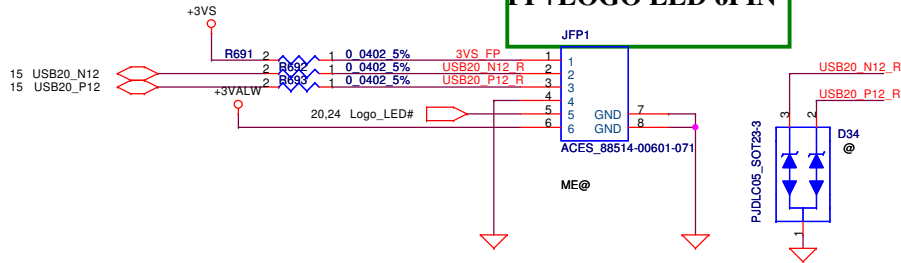
Power Bottom Board Conn. 4pin



*EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00*

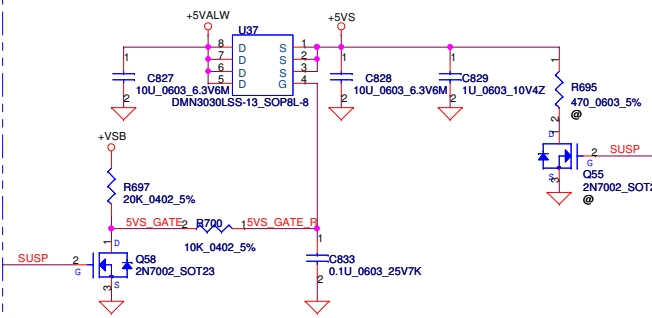


**PN: SP010014M00
FP+LOGO LED 6PIN**

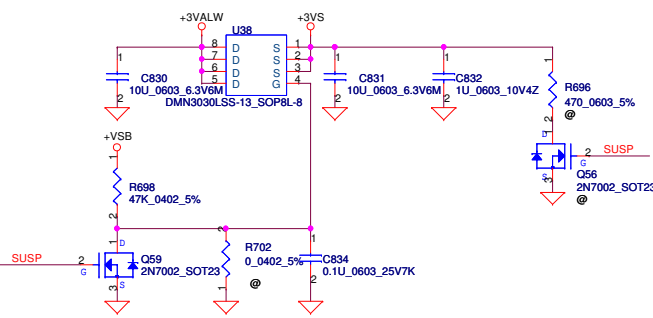


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Date: Wednesday, November 03, 2010	Sheet 30	of 40		

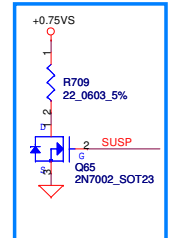
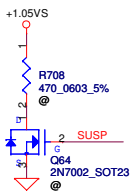
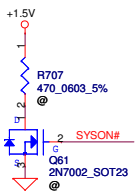
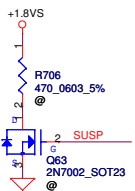
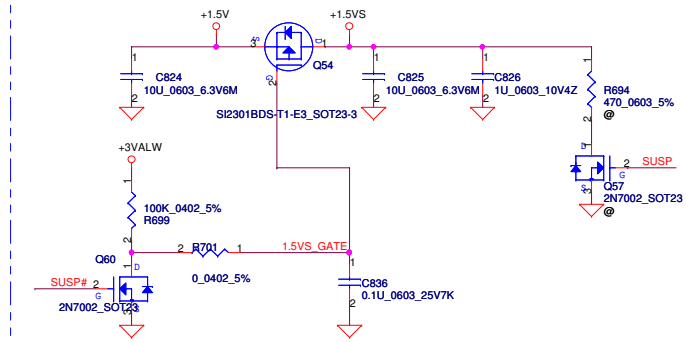
+5VALW TO +5VS



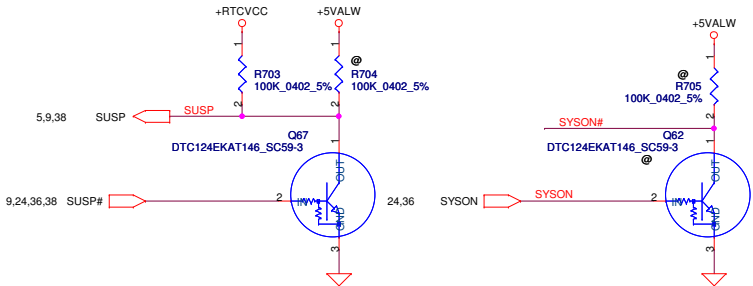
+3VALW TO +3VS



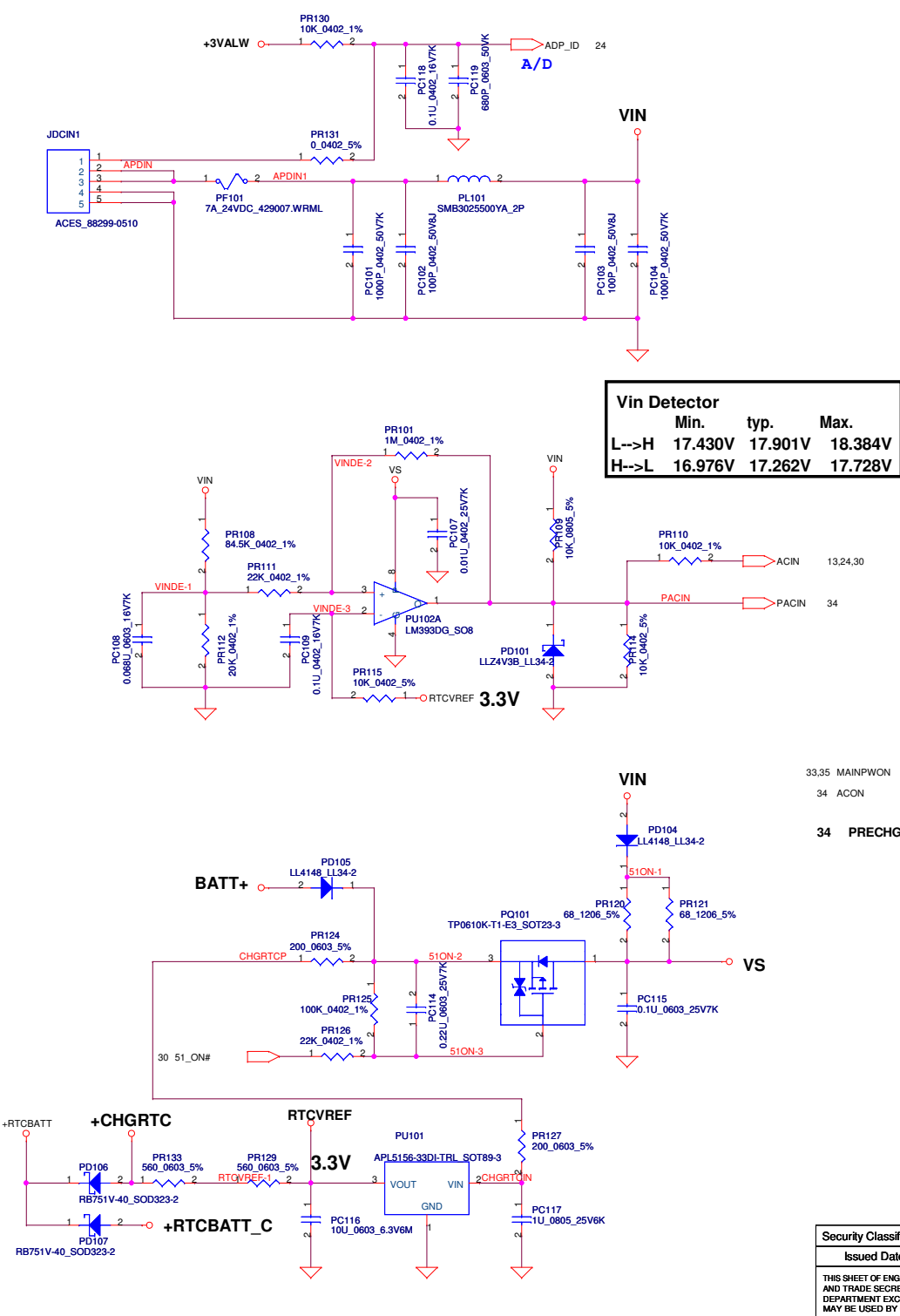
+1.5V to +1.5VS



For Intel S3 Power Reduction.



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				Size	Document Number
Date: Wednesday, November 03, 2010				Sheet	31 of 40

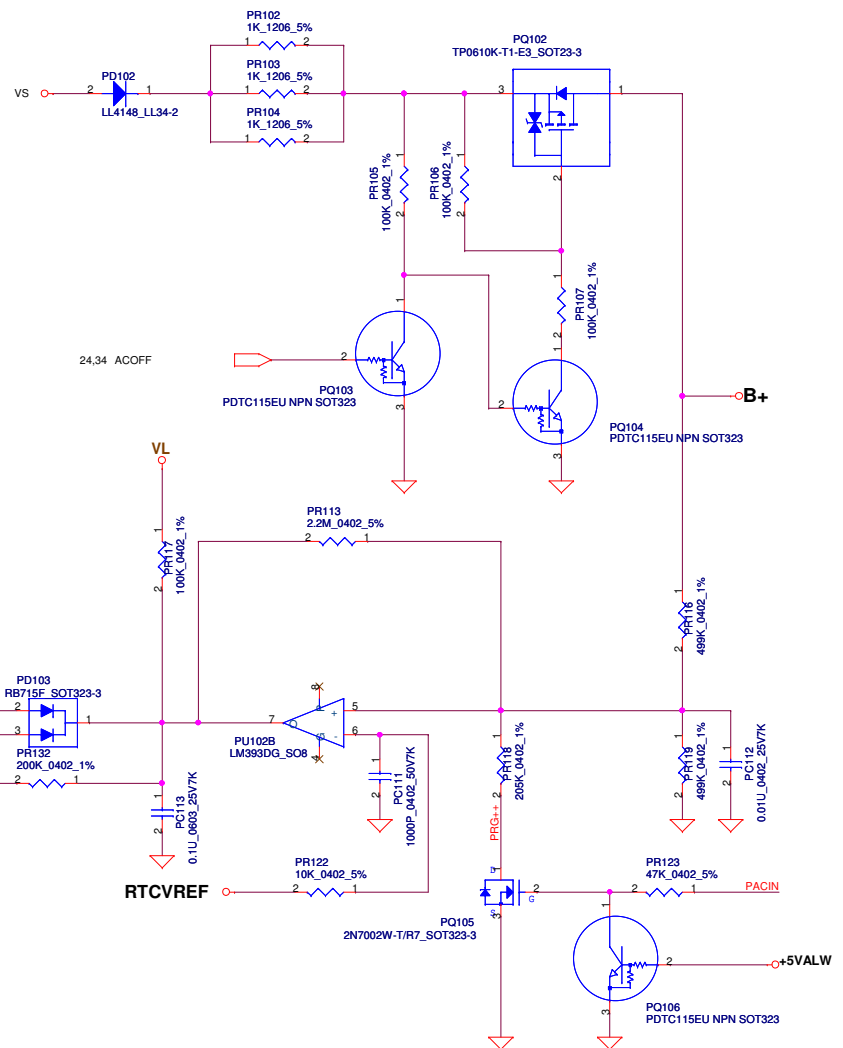


ACIN Precharge detector

	Min.	typ.	Max.
L->H	14.991V	15.381V	15.782V
H->L	13.860V	14.247V	14.621V

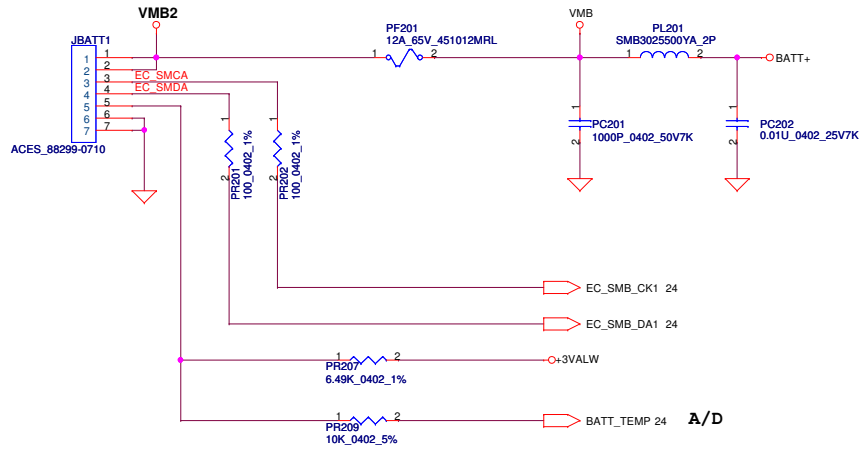
BATT ONLY Precharge detector

	Min.	typ.	Max.
L->H	7.196V	7.349V	7.505V
H->L	6.138V	6.214V	6.056V

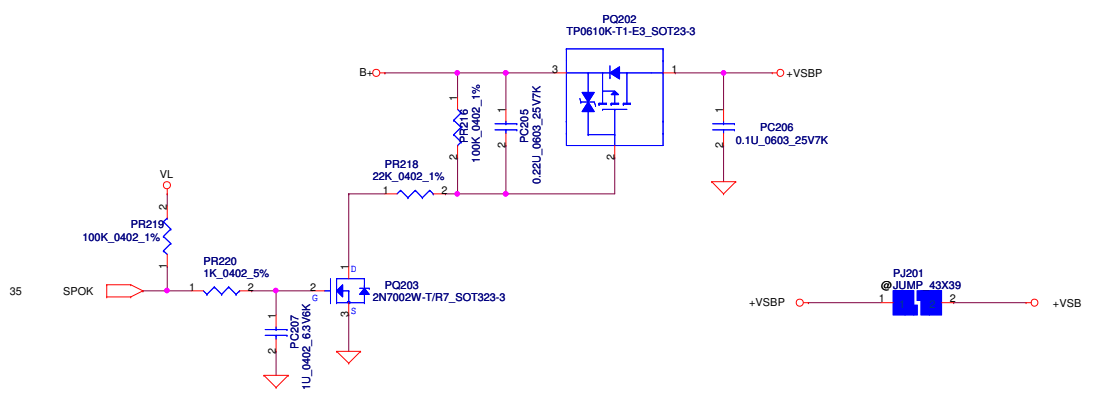
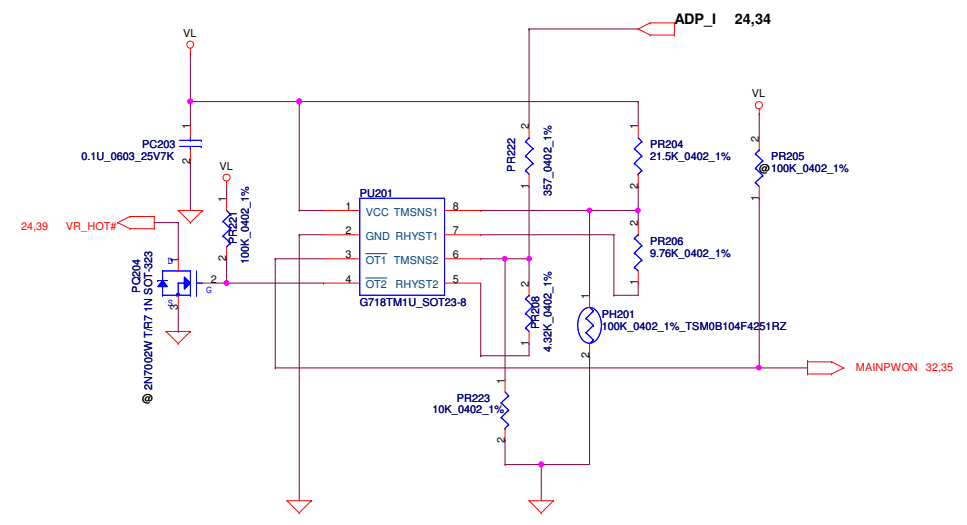


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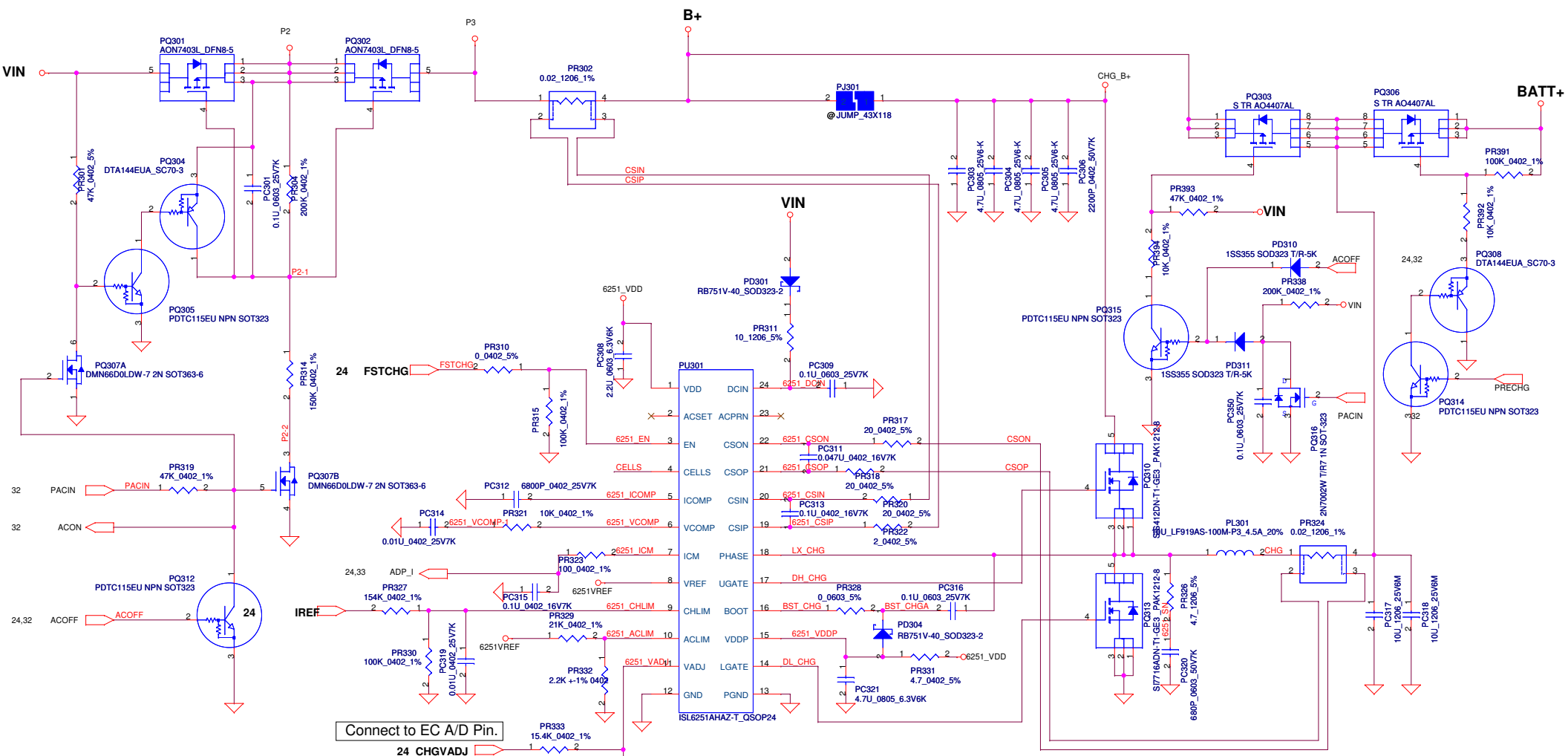
Compal Electronics, Inc.		
Title PWR DCIN / Vin Detector /Pre-charge		
Size Custom	Document Number	Rev 0.1
Date:	Wednesday, November 03, 2010	Sheet 32 of 40



PH201 under CPU botten side :
 CPU thermal protection at 92 degree C
 Recovery at 56 degree C



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Size	Custom	Document Number	Rev	Date: Wednesday, November 03, 2010 Sheet 33 of 40	
			0.1		



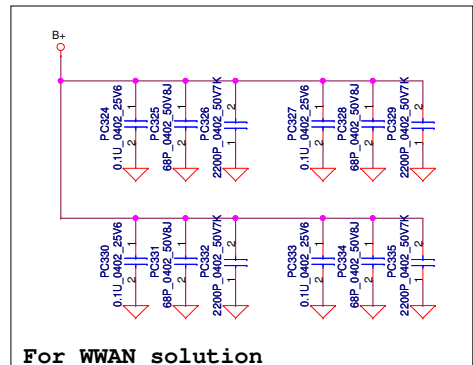
Connect to EC A/D Pin.
24 CHGVADJ

$CHGVADJ = (V_{cell} - 4) / 0.10627$	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

UMA CP mode
 $V_{aLim} = 2.39 * (2.2K / (2.2K + 21K)) = 0.2513V$
 $I_{nput} = (1 / 0.015) * ((0.05 * V_{aLim}) / (2.39 + 0.05))$
 where $V_{aLim} = 0.2513V$, $I_{nput} = 2.7629A$

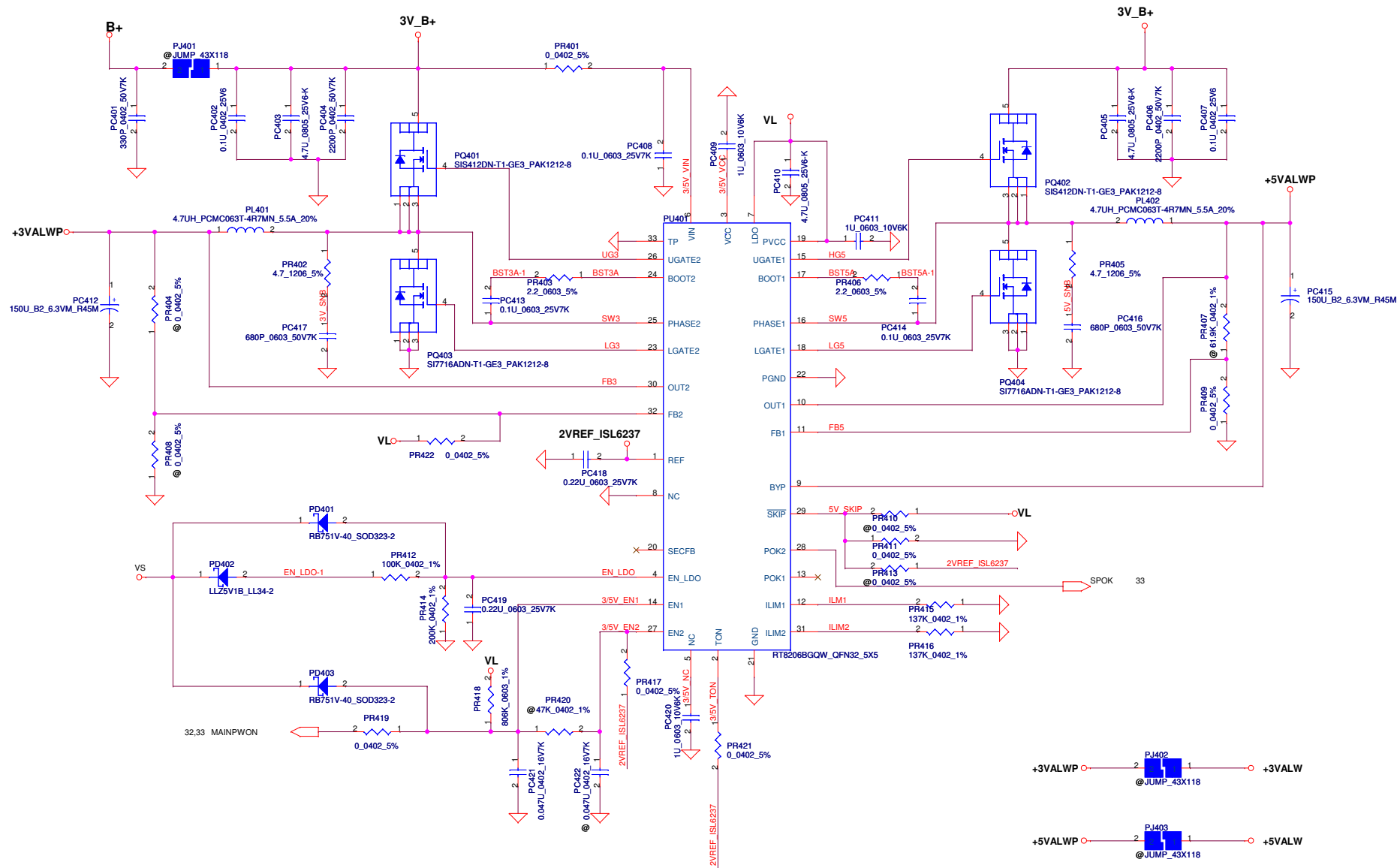
CC=0.25A-3A
 IREF=1.016*Icharge
 IREF=0.254V-3.048V
 VCHLIM need over 95mV

3cell : GND
 4cell : VDD

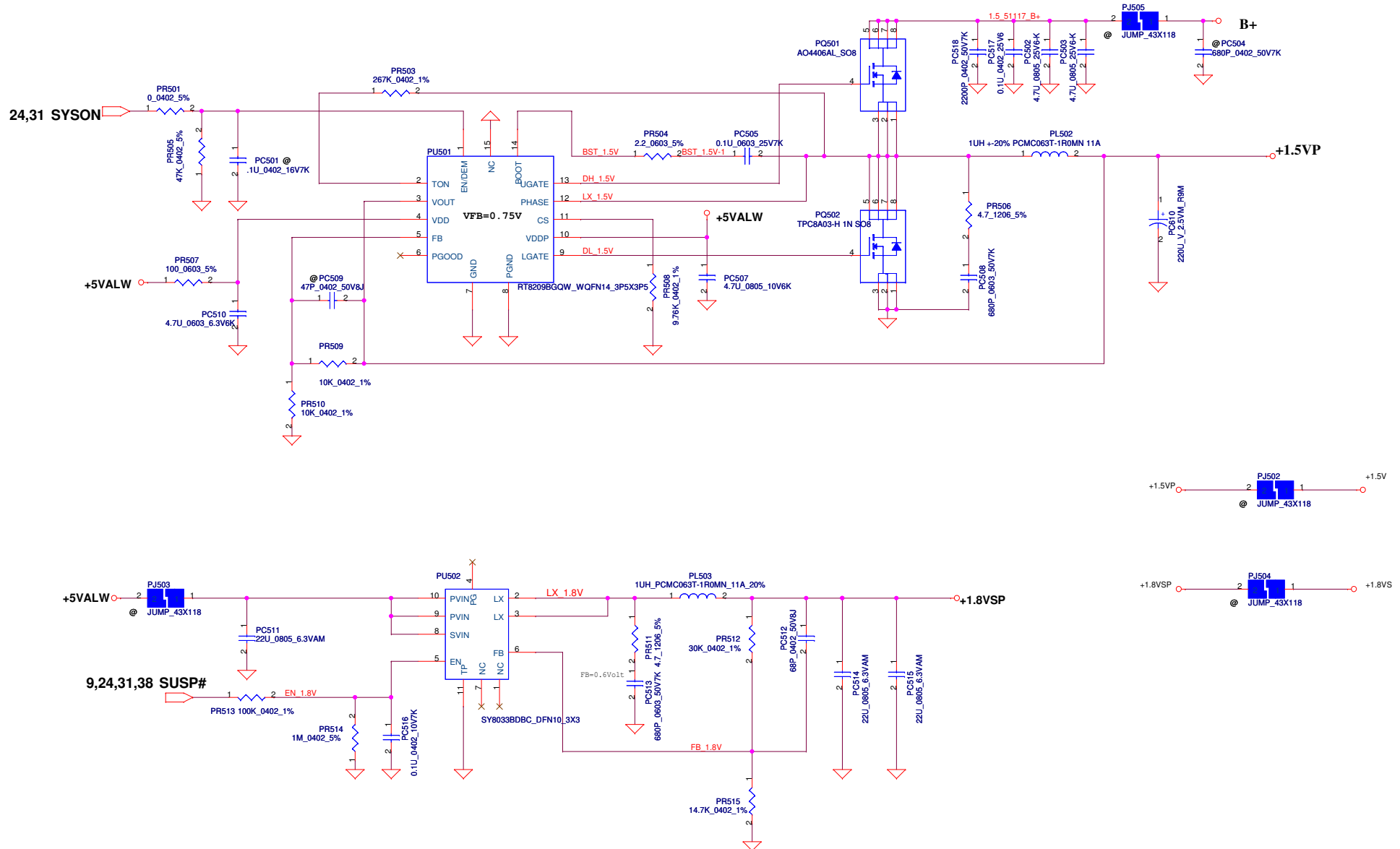


For WWAN solution

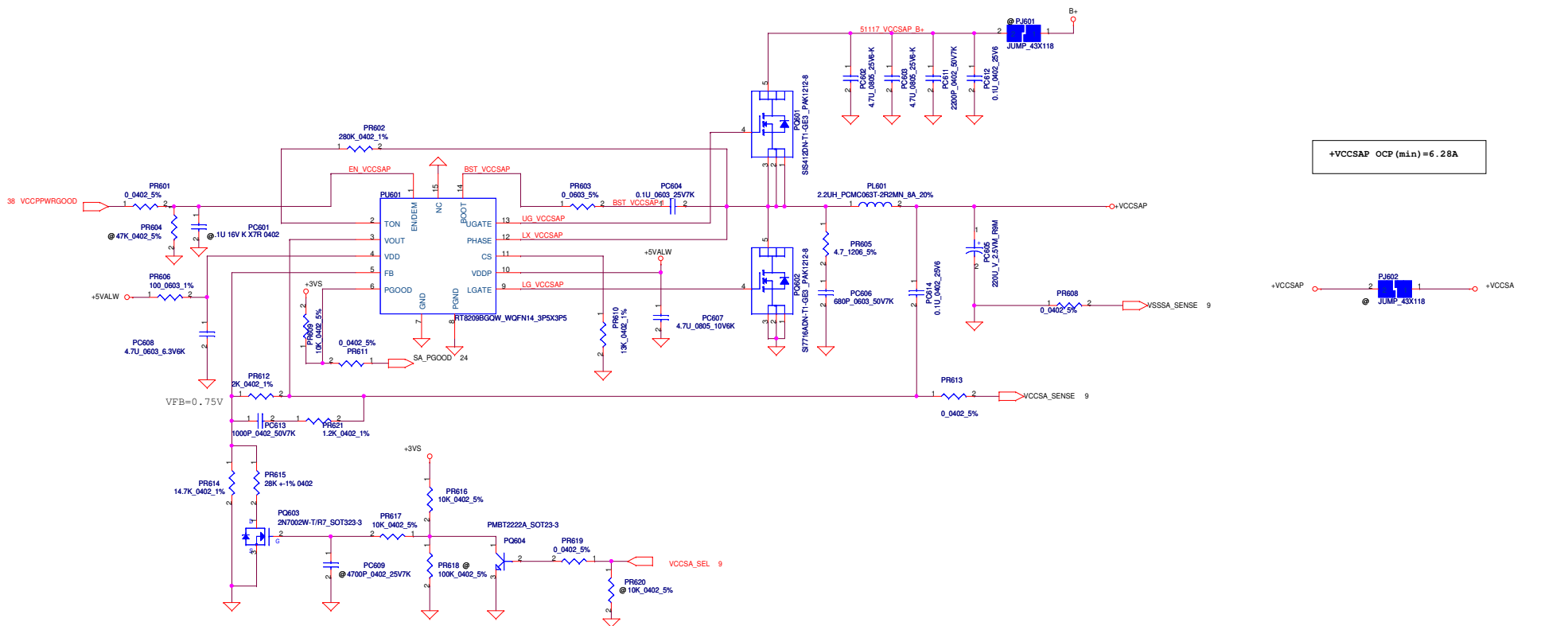
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Size	Document Number	Date: Wednesday, November 03, 2010		Sheet	34 of 40
					Rev
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				Date:	Wednesday, November 03, 2010 Sheet 35 of 40

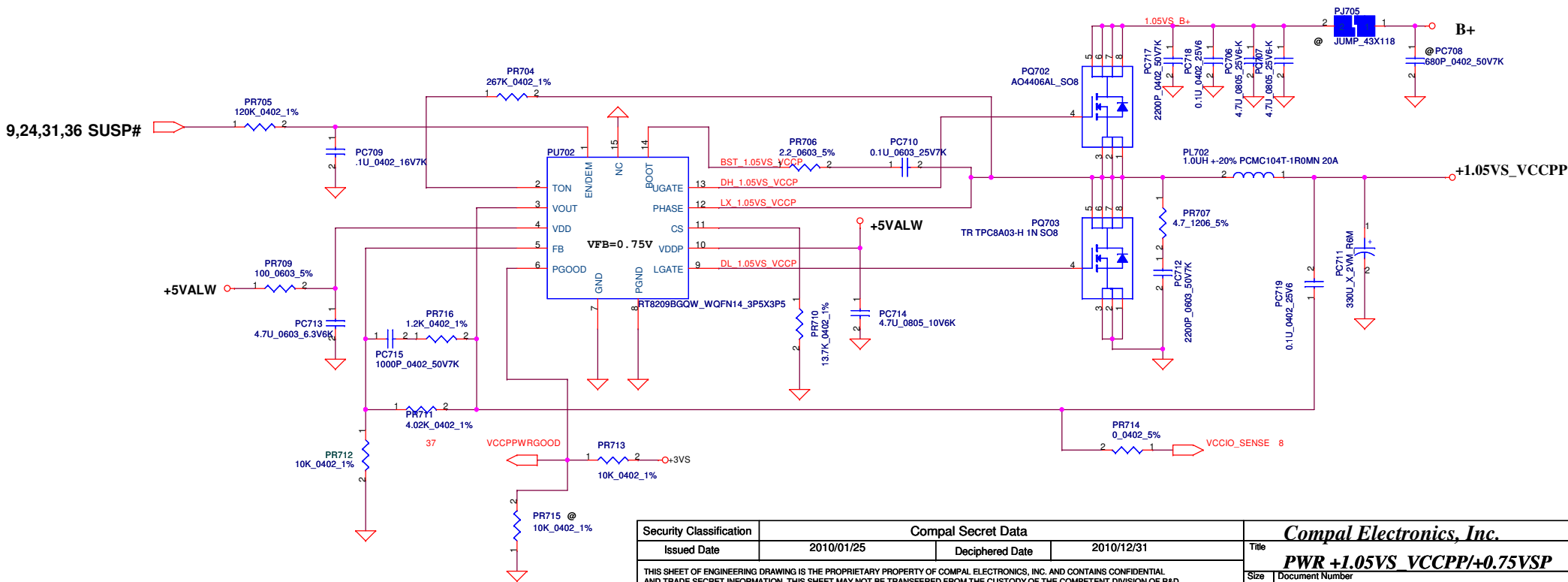
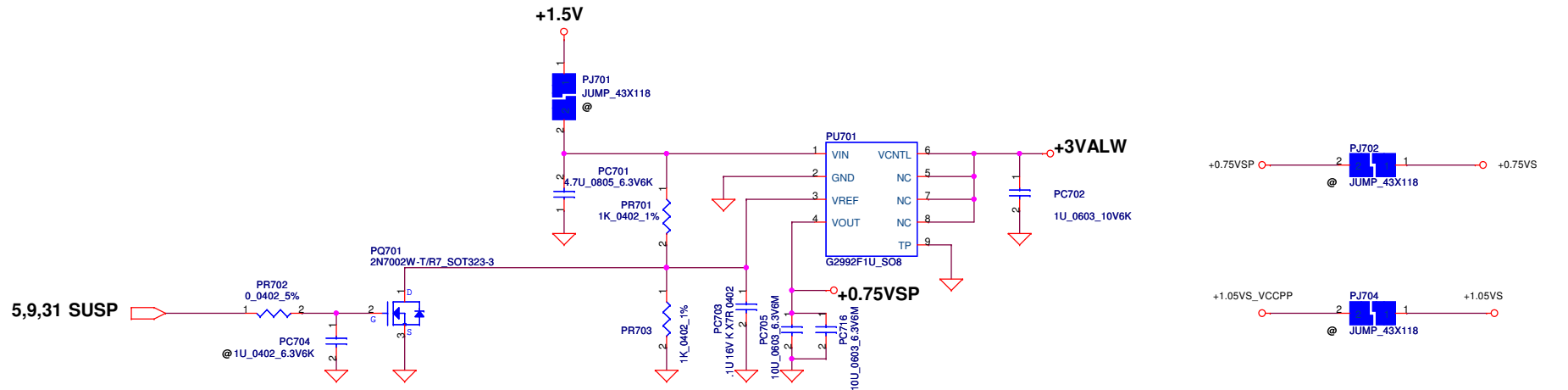


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Date:	Wednesday, November 03, 2010	Sheet	36	of	40



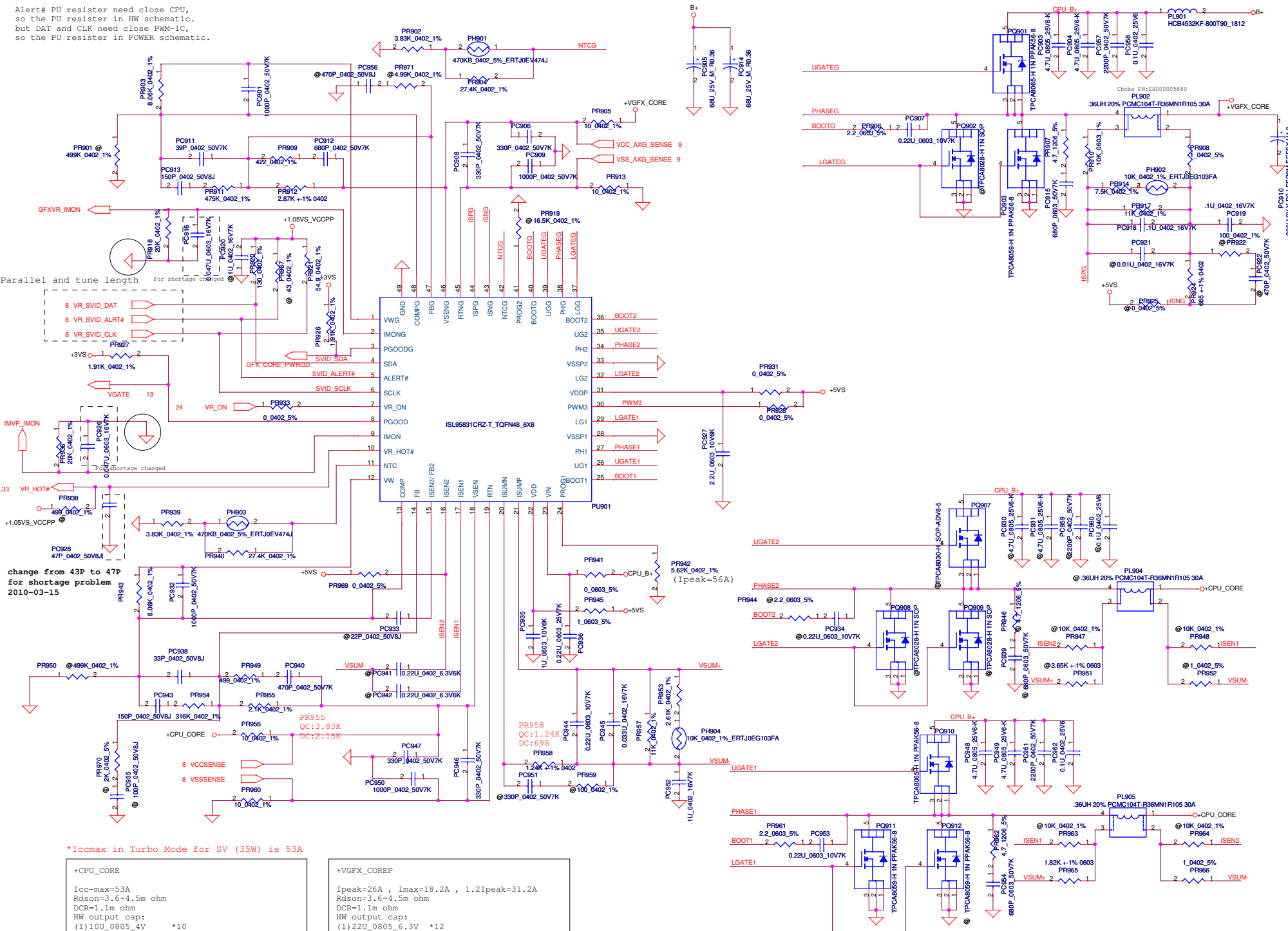
VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012	Required
0	0	0.9 V	Yes	Yes
0	1	0.85 V	Yes	Yes
1	1	0.75V	No	Yes
1	1	0.65V	No	Yes

Note: Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL due to the VID[0] is don't care for this setting.)



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Size	Custom	Document Number		Rev	0.1
Date:	Wednesday, November 03, 2010	Sheet	38	of	40

Alert# PU resistor need close CPU,
so the PU resistor in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resistor in POWER schematic.



*Iccmax in Turbo Mode for SV (35W) is 53A

+CPU_CORE	
Icc-max=53A	
Rdson=3.6~4.5m ohm	
DCR=1.1m ohm	
HW output cap:	
(1) 10U_0805_4V *10	
(2) 22U_0805_6.3V *15	
(3) 470U_D2_2V *4 (ESR=4.5m ohm)	

*OCP setting value=71.5A

+VGFX_COREP	
Ipeak=26A, Imax=18.2A, 1.2Ipeak=31.2A	
Rdson=3.6~4.5m ohm	
DCR=1.1m ohm	
HW output cap:	
(1) 22U_0805_6.3V *12	
(2) 470U_D2_2V *2 (ESR=4.5m ohm)	

*OCP setting value=37A

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Compal Electronics, Inc.	
PWR +CPU_CORE/+VGFX_CORE	
Size	Document Number
Custom	
Date:	Wednesday, November 03, 2010
Sheet	39 of 40
Rev	0.1

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
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17					

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				Sheet	40 of 40
				Rev	0.1