

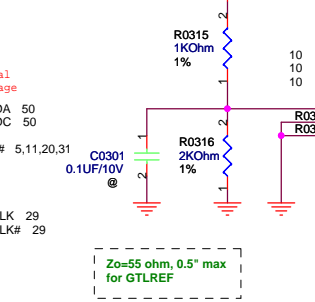
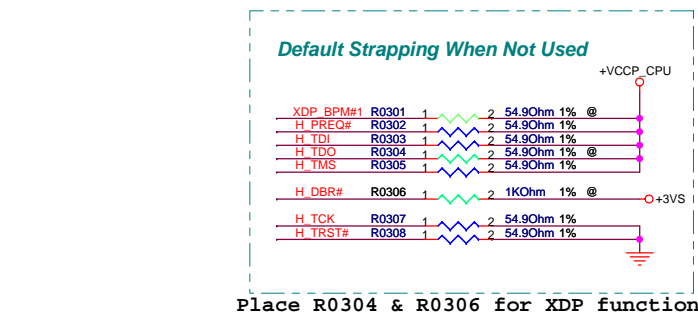
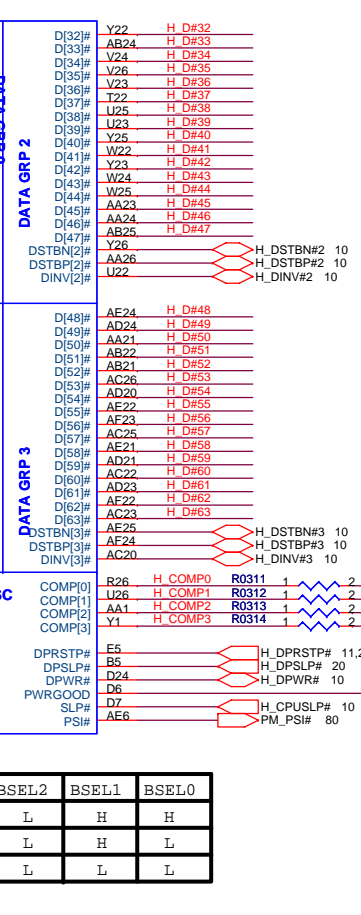
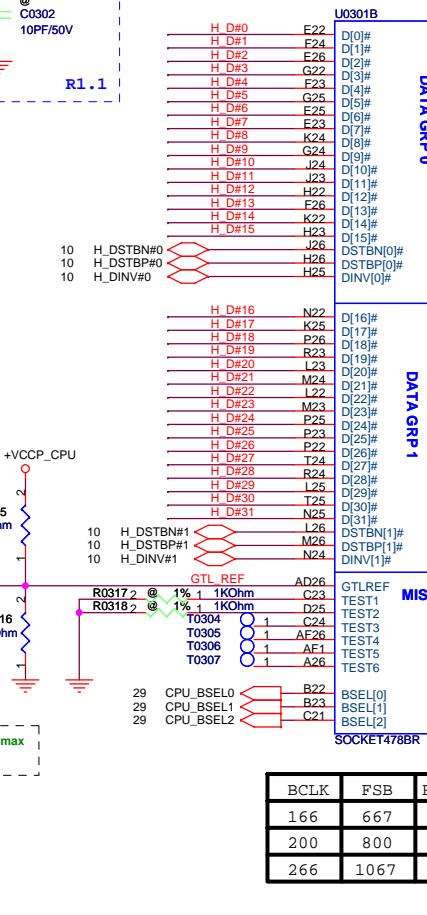
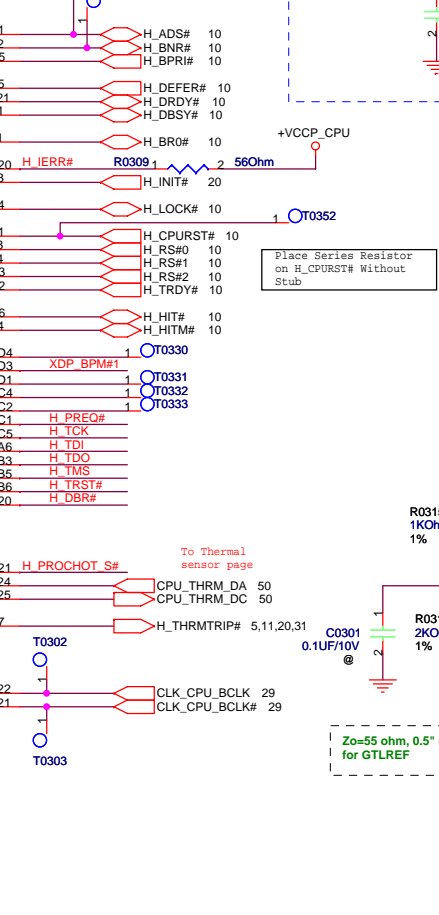
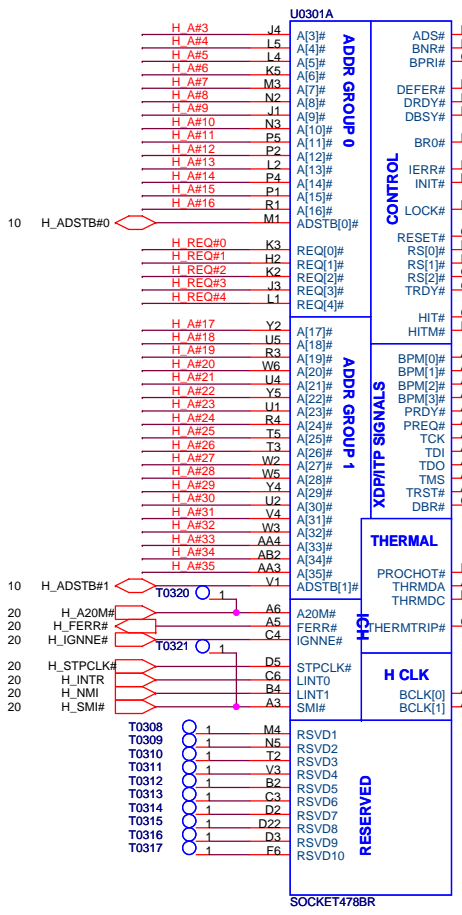
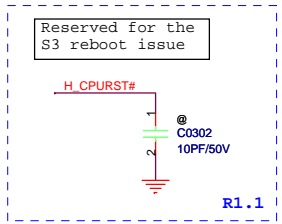
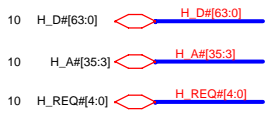
Rocky30 Schematic Index

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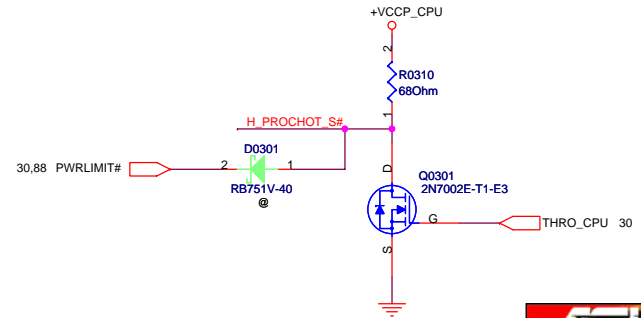
ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	GPI	PM_SYNC#	+3VS
GPIO 01	GPI	-	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#	+3VS
GPIO 06	GPI	-	+3VS
GPIO 07	GPI	-	+3VS
GPIO 08	GPI	EXT_SMI#	+3VSUS
GPIO 09	Native	UWB_ON	+3VSUS
GPIO 10	GPI	-	+3VSUS
GPIO 11	Native	EXT_SCI#	+3VSUS
GPIO 12	GPO	-	+3VSUS
GPIO 13	GPI	CB_SD#	+3VSUS
GPIO 14	GPI	RTLAN_DSM#	+3VSUS
GPIO 15	Native	-	+3VSUS
GPIO 16	Native	PM DPRSLPVR	+3VS
GPIO 17	GPI	WLAN_LED	+3VS
GPIO 18	GPO	-	+3VS
GPIO 19	GPI	-	+3VS
GPIO 20	GPO	-	+3VS
GPIO 21	GPI	-	+3VS
GPIO 22	GPI	BT_DET#	+3VS
GPIO 23	Native	-	+3VS
GPIO 24	GPO	WLAN_ON	+3VSUS
GPIO 25	Native	-	+3VSUS
GPIO 26	Native	-	+3VSUS
GPIO 27	GPO	BT_ON	+3VSUS
GPIO 28	GPO	-	+3VSUS
GPIO 29	Native	USB_OC5#	+3VSUS
GPIO 30	Native	USB_OC6#	+3VSUS
GPIO 31	Native	USB_OC7#	+3VSUS
GPIO 32	GPO	-	+3VS
GPIO 33	GPO	-	+3VS
GPIO 34	GPO	-	+3VS
GPIO 35	GPO	CLK_SATA_REQ#	+3VS
GPIO 36	GPI	GPIO36	+3VS
GPIO 37	GPI	PCB_ID0	+3VS
GPIO 38	GPI	PCB_ID1	+3VS
GPIO 39	GPI	PCB_ID2	+3VS
GPIO 40	Native	USB_OC1#	+3VSUS
GPIO 41	Native	USB_OC2#	+3VSUS
GPIO 42	Native	USB_OC3#	+3VSUS
GPIO 43	Native	USB_OC4#	+3VSUS
GPIO 44	Native	USB_OC8#	N/A
GPIO 45	Native	USB_OC9#	N/A
GPIO 46	Native	USB_OC10#	N/A
GPIO 47	Native	USB_OC11#	N/A
GPIO 48	GPI	-	+3VS
GPIO 49	GPO	HDCP_EEPROM_PROTECT#	+3VS
GPIO 50	Native	PCI_REQ#1	+3VS
GPIO 51	Native	-	+3VS
GPIO 52	Native	PCI_REQ#2	+3VS
GPIO 53	Native	-	+3VS
GPIO 54	Native	PCI_REQ#3	+3VS
GPIO 55	Native	-	+3VS
GPIO 56	GPI	-	+3VSUS
GPIO 57	GPI	-	+3VSUS
GPIO 58	GPI	-	+3VSUS
GPIO 59	Native	USB_OC0#	+3VSUS
GPIO 60	Native	RTLAN_DSM_EN	+3VSUS

EC GPIO	Use As	Signal Name	Power
GPA0	GPO	PWR_LED#	
GPA1	GPO	CHG_LED#	
GPA2	GPO	BATSEL_3S#	
GPA3	-	NOVO_CARE_LED#	
GPA4	GPO	LCD_BL_PWM	
GPA5	GPO	FAN_PWM	
GPA6	GPO	-	
GPA7	GPO	-	
GPB0	GPO	CHG_EN#	
GPB1	GPO	PRECHG	
GPB2	GPI	-	
GPB3	ALT	SMB0_CLK	
GPB4	ALT	SMB0_DAT	
GPB5	OD	A20GATE	
GPB6	OD	RCIN#	
GPB7	GPO	PM_RSMRST#	
GPC0	GPI	-	
GPC1	ALT	SMB1_CLK	
GPC2	ALT	SMB1_DAT	
GPC3	GPO	PM_PWRBTN#	
GPC4	ALT	AC_IN_OC#	
GPC5	GPO	OP_SD#	
GPC6	ALT	BAT1_IN_OC#	
GPC7	GPO	RFON_SW#	
GPD0	GPI	PWRLIMIT#	
GPD1	ALT	PM_SUSC#	
GPD2	ALT	BUF_PLT_RST#	
GPD3	OD	EXT_SCI#	
GPD4	OD	EXT_SMI#	
GPD5	GPO	LCD_BACKOFF#	
GPD6	ALT	FAN0_TACH	
GPD7	GPI	-	
GPE0	GPO	VSUS_ON	
GPE1	GPO	SUSC_EC#	
GPE2	GPO	SUSB_EC#	
GPE3	GPO	CPU_VRON	
GPE4	ALT	PWR_SW#	
GPE5	ALT	-	
GPE6	GPI	LID_SW#	
GPE7	GPO	MEDIA_KEY#	
GPF0	GPI	-	
GPF1	GPI	NOVO_CARE#	
GPF2	ALT	TP1_CLK	
GPF3	ALT	TP1_DAT	
GPF4	ALT	TP_CLK	
GPF5	ALT	TP_DAT	
GPF6	GPO	THRO_CPU	
GPF7	GPO	SUSPEND_LED#	
GPG0	GPI	PM_THERM#_EC	
GPG1	ALT	PM_SUSB#	
GPG2	GPO	BAT1_CNT2#	
-	-	-	
-	-	-	

EC GPIO	Use As	Signal Name	Power
-	-	-	
GPG6	GPO	-	
-	-	-	
GPH0	OD	PM_CLKRUN#	
GPH1	ALT	3G_ON#	
GPH2	ALT	LOGO_LED#	
GPH3	GPO	BAT_LEARN	
GPH4	GPO	-	
GPH5	GPO	NUM_LED#	
GPH6	GPO	CAP_LED#	
-	-	-	
GPIO	GPI	NV_OVERT#	
GPI1	GPI	SUS_PWRGD	
GPI2	GPI	ALL_SYSTEM_PWRGD	
GPI3	GPI	VRM_PWRGD	
GPI4	GPI	XOUT	
GPI5	GPI	YOUT	
GPI6	GPI	-	
GPI7	GPI	-	
GPJ0	GPO	EC_CLK_EN	
GPJ1	GPO	PM_PWROK	
GPJ2	GPI	-	
GPJ3	-	-	
GPJ4	GPO	BL_DA	
GPJ5	GPO	-	
GPK0	GPI	-	
GPK1	GPI	-	
GPK2	GPI	-	
GPK3	GPI	-	
GPK4	GPI	-	
GPK5	GPI	-	
GPL0	GPI	APS_PWR_CNT#	
GPL1	GPI	APS_ST#	
GPL2	GPO	USB_PWR_EN#	
GPL3	GPO	-	
GPL4	GPO	-	
GPL5	GPO	AC_ID	
GPL6	GPO	AC_65W	
GPL7	GPO	CHG_LOW_LED#	
GPK6	GPO	-	
GPK7	GPI	-	
-	-	-	
-	-	-	

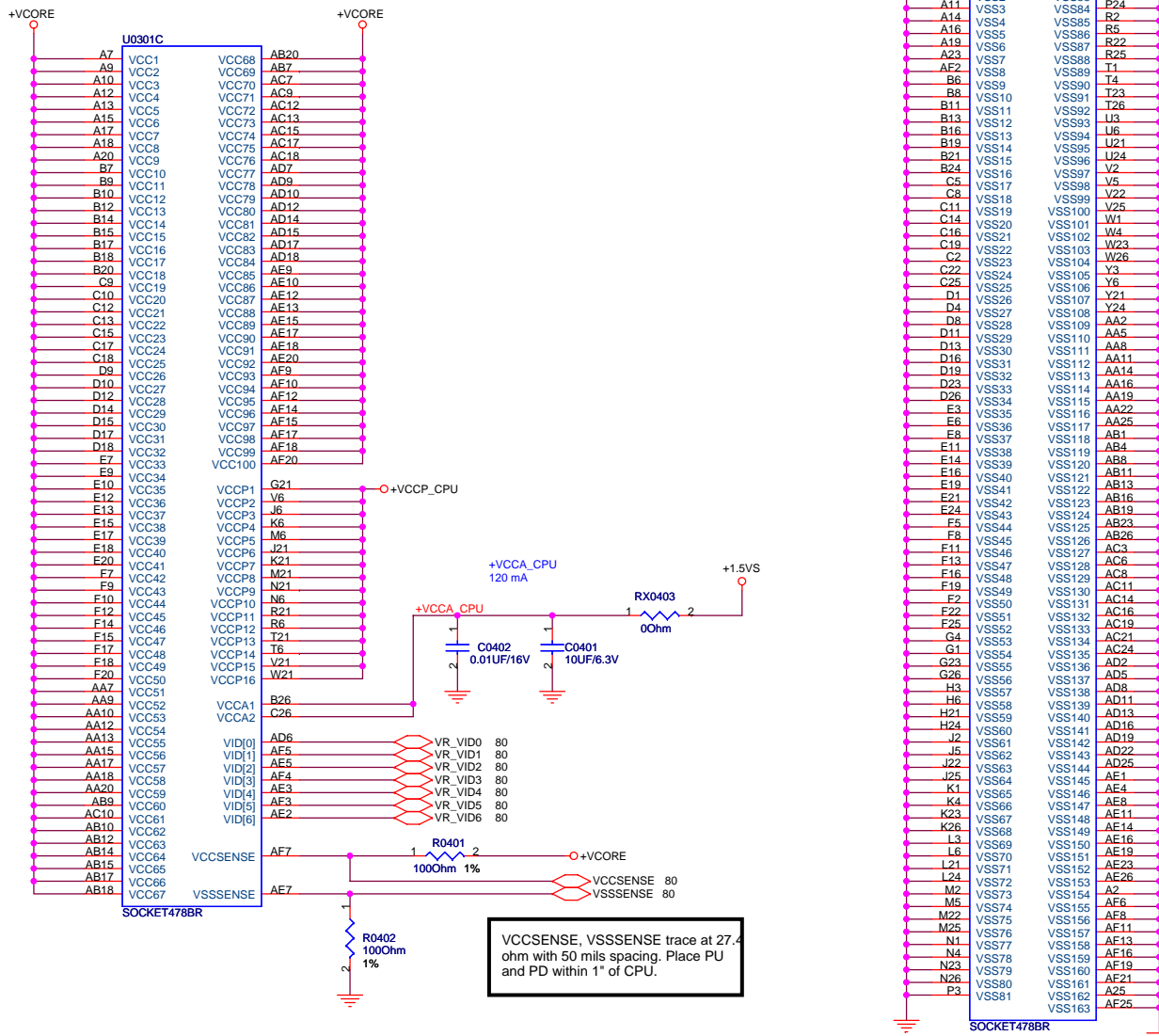


BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1067	L	L	L

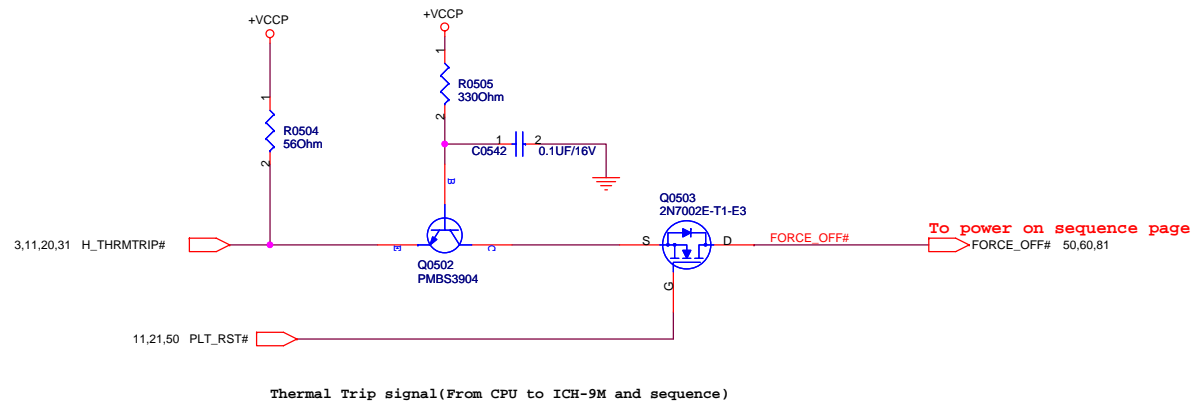
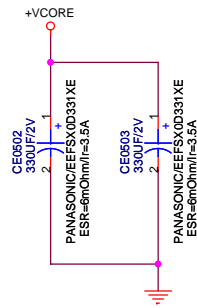
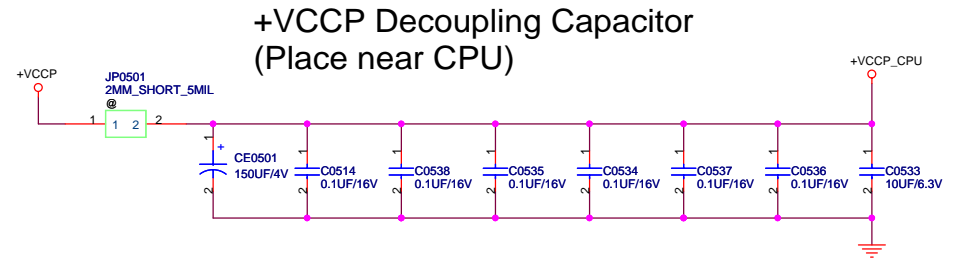
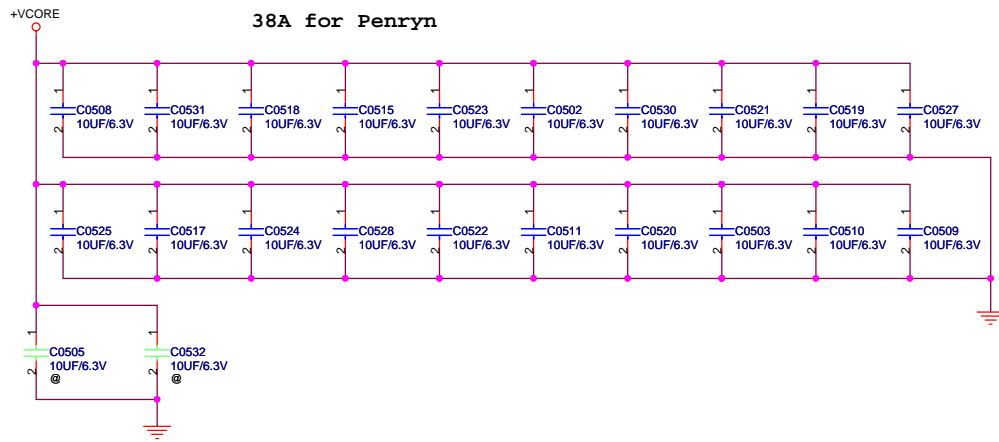


Comp0,2 connect with Zo=27.4 ohm, make trace length shorter than 0.5".
 Comp 1,3 connect with Zo=55 ohm, make trace length shorter than 0.5".

Place Series Resistor on H_PWRGD Without Stub



VCCSENSE, VSSSENSE trace at 27.4 ohm with 50 mils spacing. Place PU and PD within 1" of CPU.



5

4

3

2

1

D

D

C

C

B

B

A

A



Title :

Engineer: *Peter Lo*

Size	Project Name	Rev
A	Rocky30	1.2

Date: **Friday, March 14, 2008** Sheet **6** of **94**

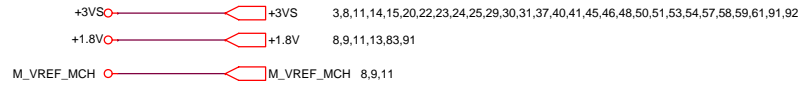
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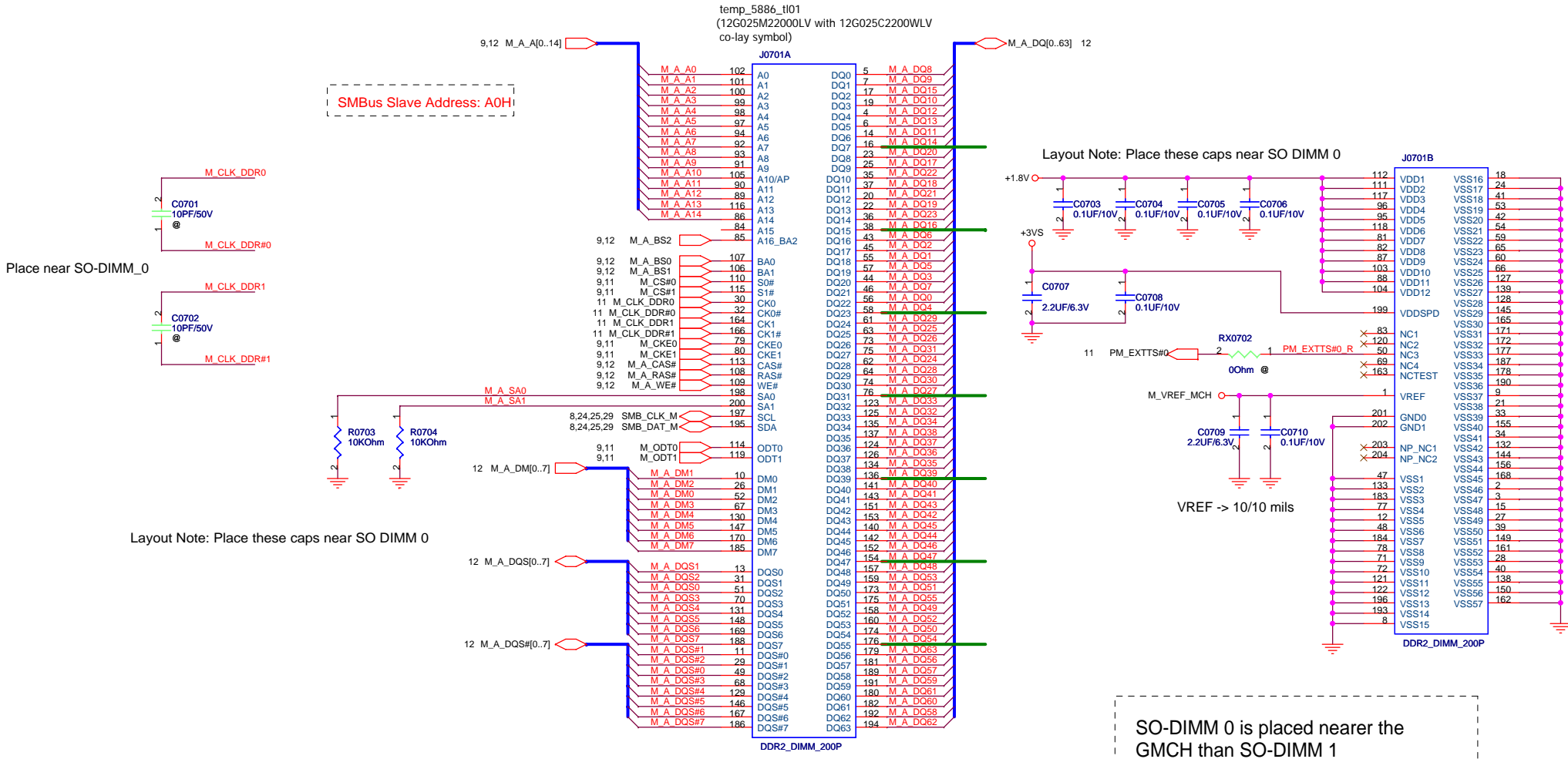
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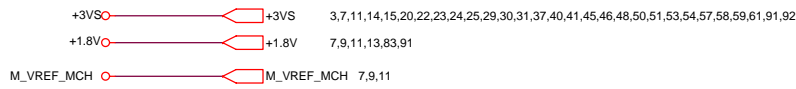
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1



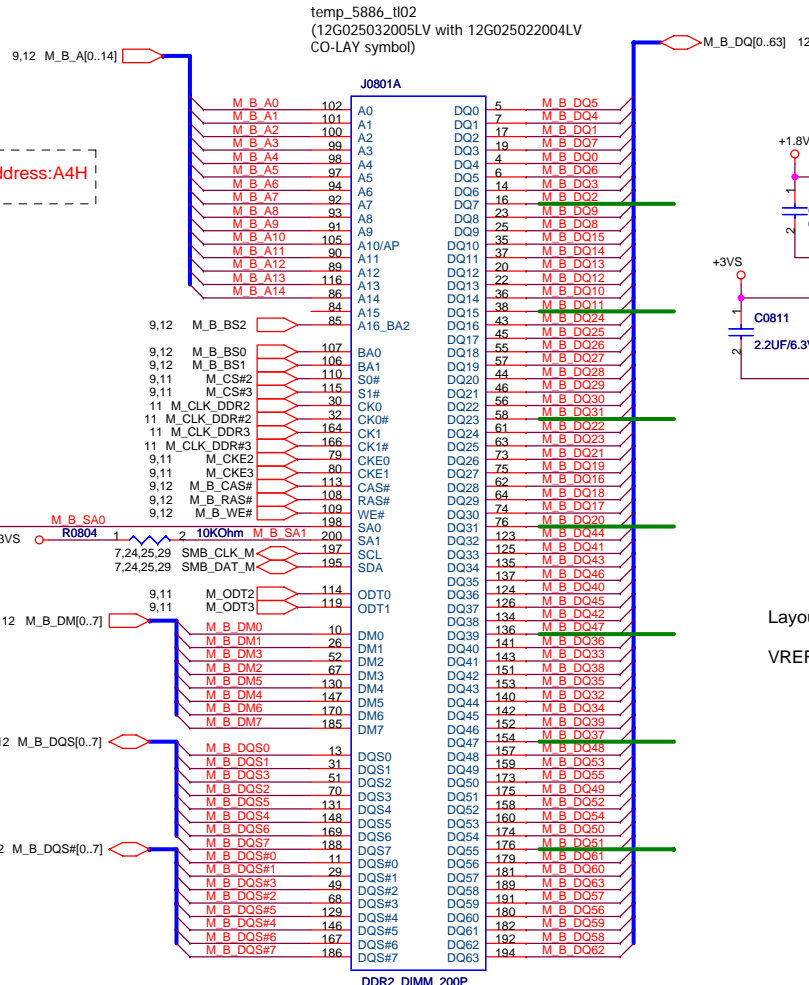
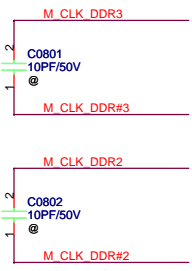
SMBus Slave Address:A0H



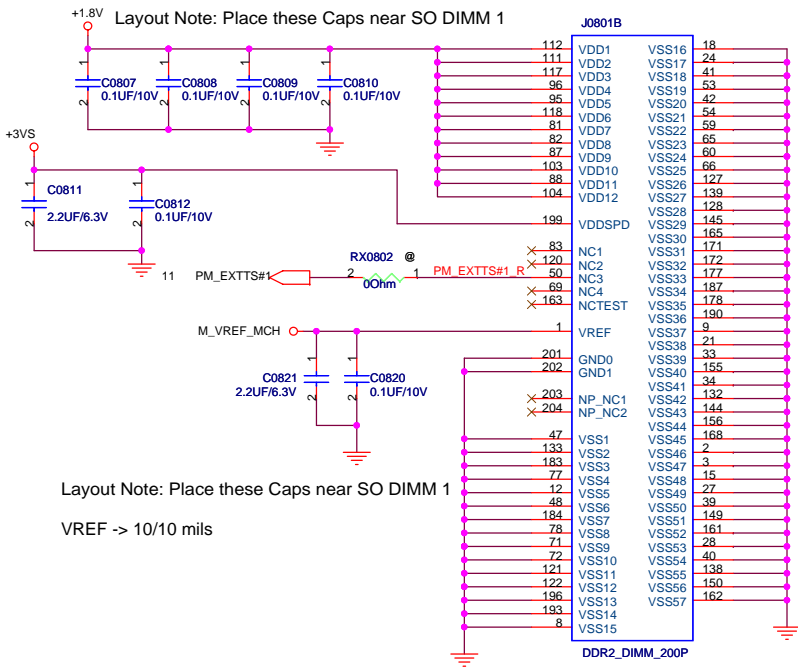


SMBus Slave Address:A4H

Place near SO-DIMM_1



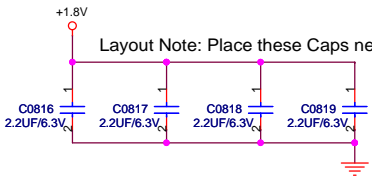
Layout Note: Place these Caps near SO DIMM 1

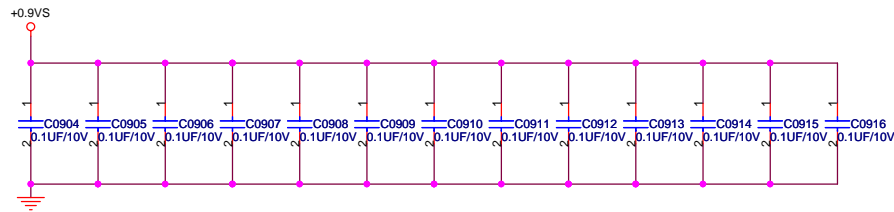
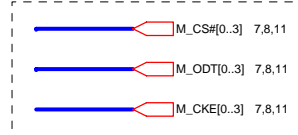
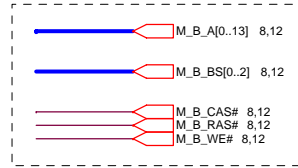
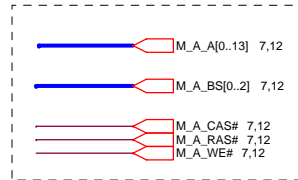
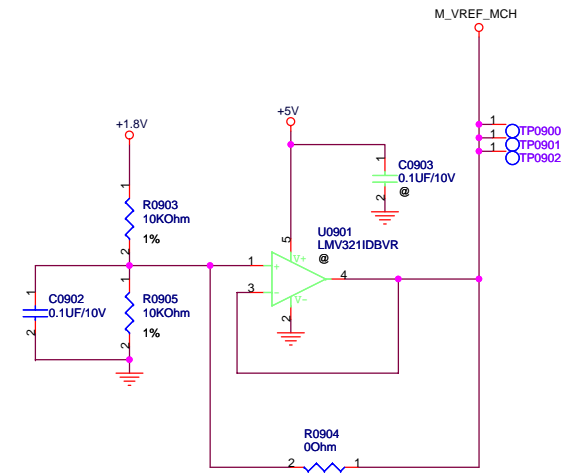
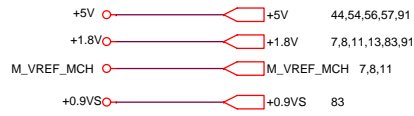


Layout Note: Place these Caps near SO DIMM 1

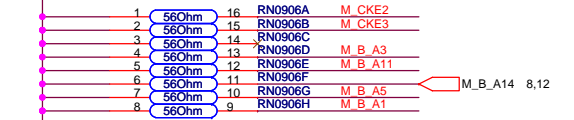
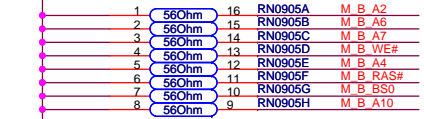
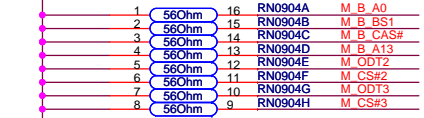
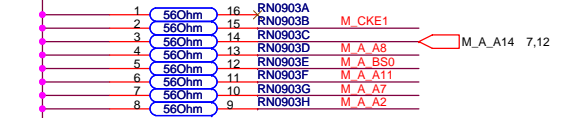
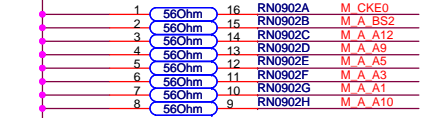
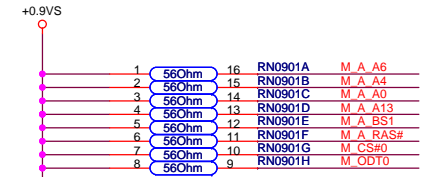
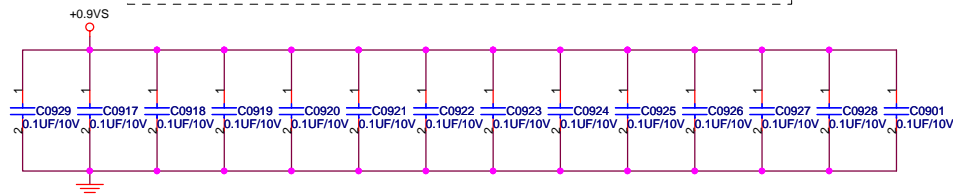
VREF -> 10/10 mils

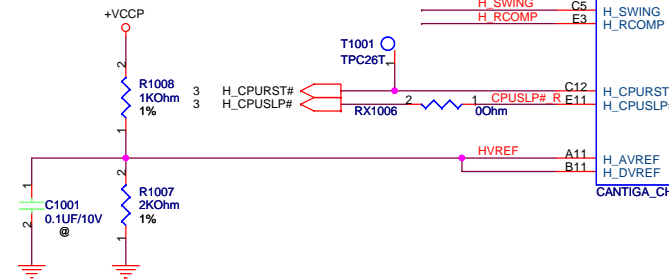
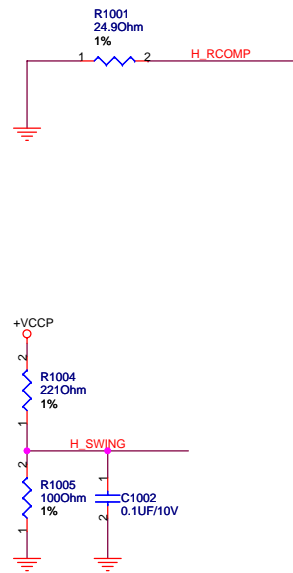
Layout Note: Place these Caps near the SO-DIMM_1





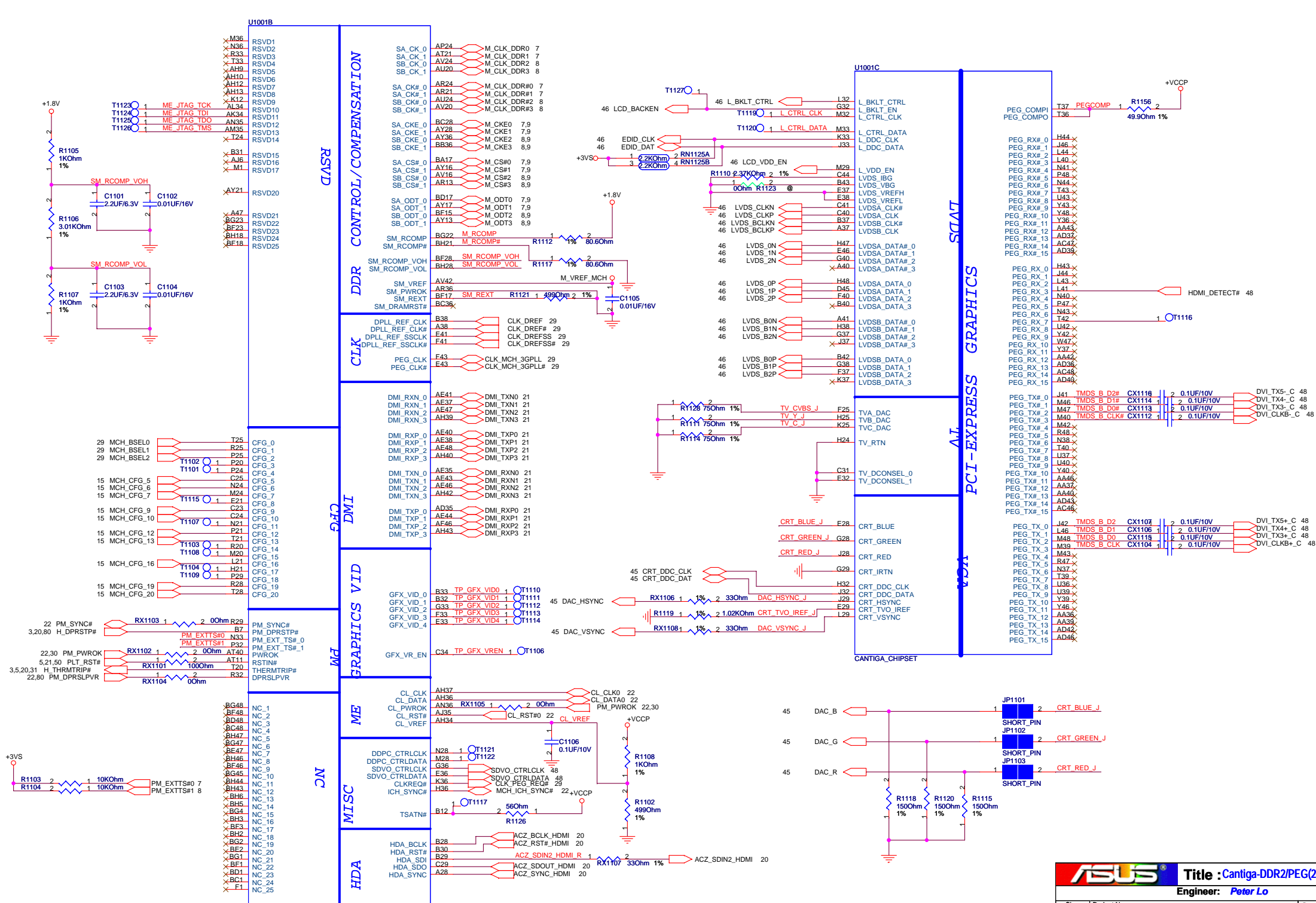
Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS





CAP 0.1u within 100 mils from GMCH

U1001A		HOST	
H_D#0	F2	H_D#_0	H_D#_0
H_D#1	G8	H_D#_1	H_D#_1
H_D#2	F8	H_D#_2	H_D#_2
H_D#3	E6	H_D#_3	H_D#_3
H_D#4	G2	H_D#_4	H_D#_4
H_D#5	H6	H_D#_5	H_D#_5
H_D#6	H2	H_D#_6	H_D#_6
H_D#7	F6	H_D#_7	H_D#_7
H_D#8	D4	H_D#_8	H_D#_8
H_D#9	H4	H_D#_9	H_D#_9
H_D#10	M3	H_D#_10	H_D#_10
H_D#11	M11	H_D#_11	H_D#_11
H_D#12	J1	H_D#_12	H_D#_12
H_D#13	J2	H_D#_13	H_D#_13
H_D#14	N12	H_D#_14	H_D#_14
H_D#15	J6	H_D#_15	H_D#_15
H_D#16	L2	H_D#_16	H_D#_16
H_D#17	R2	H_D#_17	H_D#_17
H_D#18	N9	H_D#_18	H_D#_18
H_D#19	L6	H_D#_19	H_D#_19
H_D#20	M5	H_D#_20	H_D#_20
H_D#21	L3	H_D#_21	H_D#_21
H_D#22	N2	H_D#_22	H_D#_22
H_D#23	R1	H_D#_23	H_D#_23
H_D#24	N5	H_D#_24	H_D#_24
H_D#25	N6	H_D#_25	H_D#_25
H_D#26	P13	H_D#_26	H_D#_26
H_D#27	N8	H_D#_27	H_D#_27
H_D#28	L7	H_D#_28	H_D#_28
H_D#29	N10	H_D#_29	H_D#_29
H_D#30	M3	H_D#_30	H_D#_30
H_D#31	Y3	H_D#_31	H_D#_31
H_D#32	AD14	H_D#_32	H_D#_32
H_D#33	Y6	H_D#_33	H_D#_33
H_D#34	Y10	H_D#_34	H_D#_34
H_D#35	Y12	H_D#_35	H_D#_35
H_D#36	Y14	H_D#_36	H_D#_36
H_D#37	Y7	H_D#_37	H_D#_37
H_D#38	W2	H_D#_38	H_D#_38
H_D#39	AA8	H_D#_39	H_D#_39
H_D#40	Y9	H_D#_40	H_D#_40
H_D#41	AA13	H_D#_41	H_D#_41
H_D#42	AA9	H_D#_42	H_D#_42
H_D#43	AA11	H_D#_43	H_D#_43
H_D#44	AD10	H_D#_44	H_D#_44
H_D#45	AD13	H_D#_45	H_D#_45
H_D#46	AE12	H_D#_46	H_D#_46
H_D#47	AE9	H_D#_47	H_D#_47
H_D#48	AA2	H_D#_48	H_D#_48
H_D#49	AD8	H_D#_49	H_D#_49
H_D#50	AA3	H_D#_50	H_D#_50
H_D#51	AD3	H_D#_51	H_D#_51
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H_D#56	AE3	H_D#_56	H_D#_56
H_D#57	AC3	H_D#_57	H_D#_57
H_D#58	AE11	H_D#_58	H_D#_58
H_D#59	AE8	H_D#_59	H_D#_59
H_D#60	AG2	H_D#_60	H_D#_60
H_D#61	AD6	H_D#_61	H_D#_61
H_D#62		H_D#_62	H_D#_62
H_D#63		H_D#_63	H_D#_63
H_SWING C5		H_SWING	H_SWING
H_RCOMP E3		H_RCOMP	H_RCOMP
H_CPURST#		H_CPURST#	H_CPURST#
H_CPUSLP#		H_CPUSLP#	H_CPUSLP#
HVREF A11		HVREF	HVREF
H_AVREF B11		H_AVREF	H_AVREF
H_DVREF		H_DVREF	H_DVREF
CANTIGA_CHIPSET		CANTIGA_CHIPSET	CANTIGA_CHIPSET
A14 H_A#3		A14	H_A#3
C15 H_A#4		C15	H_A#4
E16 H_A#5		E16	H_A#5
H13 H_A#6		H13	H_A#6
C18 H_A#7		C18	H_A#7
M16 H_A#8		M16	H_A#8
H_A#_8		H_A#_8	H_A#_8
H_A#_9		H_A#_9	H_A#_9
J13 H_A#9		J13	H_A#9
P16 H_A#10		P16	H_A#10
H_A#_10		H_A#_10	H_A#_10
R16 H_A#11		R16	H_A#11
H_A#_11		H_A#_11	H_A#_11
N17 H_A#12		N17	H_A#12
H_A#_12		H_A#_12	H_A#_12
M13 H_A#13		M13	H_A#13
H_A#_13		H_A#_13	H_A#_13
E17 H_A#14		E17	H_A#14
H_A#_14		H_A#_14	H_A#_14
P17 H_A#15		P17	H_A#15
H_A#_15		H_A#_15	H_A#_15
E17 H_A#16		E17	H_A#16
H_A#_16		H_A#_16	H_A#_16
G20 H_A#17		G20	H_A#17
H_A#_17		H_A#_17	H_A#_17
B19 H_A#18		B19	H_A#18
H_A#_18		H_A#_18	H_A#_18
E20 H_A#19		E20	H_A#19
H_A#_19		H_A#_19	H_A#_19
H16 H_A#21		H16	H_A#21
H_A#_21		H_A#_21	H_A#_21
J20 H_A#22		J20	H_A#22
H_A#_22		H_A#_22	H_A#_22
L17 H_A#23		L17	H_A#23
H_A#_23		H_A#_23	H_A#_23
A17 H_A#24		A17	H_A#24
H_A#_24		H_A#_24	H_A#_24
B17 H_A#25		B17	H_A#25
H_A#_25		H_A#_25	H_A#_25
L16 H_A#26		L16	H_A#26
H_A#_26		H_A#_26	H_A#_26
C21 H_A#27		C21	H_A#27
H_A#_27		H_A#_27	H_A#_27
H17 H_A#28		H17	H_A#28
H_A#_28		H_A#_28	H_A#_28
H20 H_A#29		H20	H_A#29
H_A#_29		H_A#_29	H_A#_29
H_A#_30		H_A#_30	H_A#_30
B18 H_A#30		B18	H_A#30
H_A#_31		H_A#_31	H_A#_31
K17 H_A#31		K17	H_A#31
H_A#_32		H_A#_32	H_A#_32
B20 H_A#32		B20	H_A#32
H_A#_33		H_A#_33	H_A#_33
F21 H_A#33		F21	H_A#33
H_A#_34		H_A#_34	H_A#_34
K21 H_A#34		K21	H_A#34
H_A#_35		H_A#_35	H_A#_35
L20 H_A#35		L20	H_A#35
H_ADS#		H_ADS#	H_ADS#
H_ADSTB#_0		H_ADSTB#_0	H_ADSTB#_0
G17		G17	H_ADSTB#_1
H_ADSTB#_1		H_ADSTB#_1	H_ADSTB#_1
A9		A9	H_BNR#
H_BNR#		H_BNR#	H_BNR#
E11		E11	H_BPR#
H_BPR#		H_BPR#	H_BPR#
H_BRO#		H_BRO#	H_BRO#
G12		G12	H_BRO#
H_BRO#		H_BRO#	H_DEFER#
E9		E9	H_DEFER#
H_DEFER#		H_DEFER#	H_DBSY#
B10		B10	H_DBSY#
H_DBSY#		H_DBSY#	HPLL_CLK
AH7		AH7	CLK_MCH_BCLK
HPLL_CLK		HPLL_CLK	CLK_MCH_BCLK#
AH6		AH6	CLK_MCH_BCLK#
HPLL_CLK#		HPLL_CLK#	H_DPWR#
J11		J11	H_DPWR#
H_DPWR#		H_DPWR#	H_DRDY#
H_DRDY#		H_DRDY#	H_DRDY#
E9		E9	H_DRDY#
H_DRDY#		H_DRDY#	H_HIT#
H_HIT#		H_HIT#	H_HIT#
H_HIT#		H_HIT#	H_HIT#
E12		E12	H_HIT#
H_HIT#		H_HIT#	H_LOCK#
H_LOCK#		H_LOCK#	H_LOCK#
H11		H11	H_LOCK#
H_LOCK#		H_LOCK#	H_TRDY#
C9		C9	H_TRDY#
H_TRDY#		H_TRDY#	H_TRDY#
H_DINV#_0		J8	H_DINV#_0
H_DINV#_1		L3	H_DINV#_1
H_DINV#_2		Y13	H_DINV#_2
H_DINV#_3		Y1	H_DINV#_3
H_DINV#_3		Y1	H_DINV#_3
H_DSTBN#_0		L10	H_DSTBN#_0
H_DSTBN#_1		M7	H_DSTBN#_1
H_DSTBN#_2		AA5	H_DSTBN#_2
H_DSTBN#_3		AE6	H_DSTBN#_3
H_DSTBN#_3		AE6	H_DSTBN#_3
H_DSTBP#_0		L9	H_DSTBP#_0
H_DSTBP#_1		M8	H_DSTBP#_1
H_DSTBP#_2		AA6	H_DSTBP#_2
H_DSTBP#_3		AE5	H_DSTBP#_3
H_DSTBP#_3		AE5	H_DSTBP#_3
H_REQ#_0		B15	H_REQ#_0
H_REQ#_1		K13	H_REQ#_1
H_REQ#_2		E13	H_REQ#_2
H_REQ#_3		B13	H_REQ#_3
H_REQ#_4		B14	H_REQ#_4
H_REQ#_4		B14	H_REQ#_4
H_RS#_0		B6	H_RS#_0
H_RS#_1		E12	H_RS#_1
H_RS#_2		C8	H_RS#_2
H_RS#_2		C8	H_RS#_2



7 M_A_DQ[0:63]

- M_A_DQ0 AJ38
- M_A_DQ1 AJ41
- M_A_DQ2 AN38
- M_A_DQ3 AM38
- M_A_DQ4 AJ36
- M_A_DQ5 AJ40
- M_A_DQ6 AM44
- M_A_DQ7 AM42
- M_A_DQ8 AN43
- M_A_DQ9 AN44
- M_A_DQ10 AU40
- M_A_DQ11 AT38
- M_A_DQ12 AN41
- M_A_DQ13 AN39
- M_A_DQ14 AU44
- M_A_DQ15 AU42
- M_A_DQ16 AV39
- M_A_DQ17 AY44
- M_A_DQ18 BA40
- M_A_DQ19 BD43
- M_A_DQ20 AV41
- M_A_DQ21 AY43
- M_A_DQ22 BA41
- M_A_DQ23 BC40
- M_A_DQ24 AY37
- M_A_DQ25 BD38
- M_A_DQ26 AV37
- M_A_DQ27 AT36
- M_A_DQ28 AY38
- M_A_DQ29 BB38
- M_A_DQ30 AV36
- M_A_DQ31 AW36
- M_A_DQ32 BD13
- M_A_DQ33 AU11
- M_A_DQ34 BC11
- M_A_DQ35 BA12
- M_A_DQ36 AU13
- M_A_DQ37 AV13
- M_A_DQ38 BD12
- M_A_DQ39 BC12
- M_A_DQ40 BB9
- M_A_DQ41 BA9
- M_A_DQ42 AU10
- M_A_DQ43 AV9
- M_A_DQ44 BA11
- M_A_DQ45 BD9
- M_A_DQ46 AY8
- M_A_DQ47 BA6
- M_A_DQ48 AV5
- M_A_DQ49 AV7
- M_A_DQ50 AT9
- M_A_DQ51 AN8
- M_A_DQ52 AU5
- M_A_DQ53 AU6
- M_A_DQ54 AT5
- M_A_DQ55 AN10
- M_A_DQ56 AM11
- M_A_DQ57 AM5
- M_A_DQ58 AJ9
- M_A_DQ59 AJ8
- M_A_DQ60 AN12
- M_A_DQ61 AM13
- M_A_DQ62 AJ11
- M_A_DQ63 AJ12

U1001D

- SA_DQ_0
- SA_DQ_1
- SA_DQ_2
- SA_DQ_3
- SA_DQ_4
- SA_DQ_5
- SA_DQ_6
- SA_DQ_7
- SA_DQ_8
- SA_DQ_9
- SA_DQ_10
- SA_DQ_11
- SA_DM_0
- SA_DM_1
- SA_DM_2
- SA_DM_3
- SA_DM_4
- SA_DM_5
- SA_DM_6
- SA_DM_7
- SA_DQS_0
- SA_DQS_1
- SA_DQS_2
- SA_DQS_3
- SA_DQS_4
- SA_DQS_5
- SA_DQS_6
- SA_DQS_7
- SA_MA_0
- SA_MA_1
- SA_MA_2
- SA_MA_3
- SA_MA_4
- SA_MA_5
- SA_MA_6
- SA_MA_7
- SA_MA_8
- SA_MA_9
- SA_MA_10
- SA_MA_11
- SA_MA_12
- SA_MA_13
- SA_MA_14

DDR SYSTEM MEMORY A

- SA_BS_0
- SA_BS_1
- SA_BS_2
- SA_RAS#
- SA_CAS#
- SA_WE#
- AM37 M_A_DM0
- AT41 M_A_DM1
- AY41 M_A_DM2
- AU39 M_A_DM3
- BB12 M_A_DM4
- AY6 M_A_DM5
- AT7 M_A_DM6
- AJ5 M_A_DM7
- AJ44 M_A_DQS0
- AT44 M_A_DQS1
- BA43 M_A_DQS2
- BC37 M_A_DQS3
- AW12 M_A_DQS4
- BC8 M_A_DQS5
- AU8 M_A_DQS6
- AM7 M_A_DQS7
- AJ43 M_A_DQS#0
- AT43 M_A_DQS#1
- BA44 M_A_DQS#2
- BD37 M_A_DQS#3
- AY12 M_A_DQS#4
- BD8 M_A_DQS#5
- AU9 M_A_DQS#6
- AM8 M_A_DQS#7
- BA21 M_A_A0
- BC24 M_A_A1
- BG24 M_A_A2
- BH24 M_A_A3
- BC25 M_A_A4
- BA24 M_A_A5
- BD24 M_A_A6
- BG27 M_A_A7
- BE25 M_A_A8
- AW24 M_A_A9
- BC21 M_A_A10
- BG26 M_A_A11
- BH26 M_A_A12
- BH17 M_A_A13
- AY25 M_A_A14

8 M_B_DQ[0:63]

- M_B_DQ0 AK47
- M_B_DQ1 AH46
- M_B_DQ2 AP47
- M_B_DQ3 AP48
- M_B_DQ4 AJ46
- M_B_DQ5 AJ48
- M_B_DQ6 AM48
- M_B_DQ7 AP48
- M_B_DQ8 AU47
- M_B_DQ9 AU46
- M_B_DQ10 BA48
- M_B_DQ11 AY48
- M_B_DQ12 AT47
- M_B_DQ13 AR47
- M_B_DQ14 BA47
- M_B_DQ15 BC47
- M_B_DQ16 BC46
- M_B_DQ17 BC44
- M_B_DQ18 RG43
- M_B_DQ19 BF43
- M_B_DQ20 BE45
- M_B_DQ21 BC41
- M_B_DQ22 BE40
- M_B_DQ23 BF41
- M_B_DQ24 BG38
- M_B_DQ25 BF38
- M_B_DQ26 BH35
- M_B_DQ27 BG35
- M_B_DQ28 BH40
- M_B_DQ29 BG39
- M_B_DQ30 BG34
- M_B_DQ31 BH34
- M_B_DQ32 BH34
- M_B_DQ33 BG12
- M_B_DQ34 BH11
- M_B_DQ35 BG8
- M_B_DQ36 BH12
- M_B_DQ37 BF11
- M_B_DQ38 BF8
- M_B_DQ39 BG7
- M_B_DQ40 BC6
- M_B_DQ41 BC6
- M_B_DQ42 AY3
- M_B_DQ43 AY1
- M_B_DQ44 BF6
- M_B_DQ45 BF5
- M_B_DQ46 BA1
- M_B_DQ47 BD3
- M_B_DQ48 AV2
- M_B_DQ49 AU3
- M_B_DQ50 AN2
- M_B_DQ51 AN2
- M_B_DQ52 AY2
- M_B_DQ53 AV1
- M_B_DQ54 AP3
- M_B_DQ55 AR1
- M_B_DQ56 AL1
- M_B_DQ57 AL2
- M_B_DQ58 AJ1
- M_B_DQ59 AH1
- M_B_DQ60 AH2
- M_B_DQ61 AM3
- M_B_DQ62 AH3
- M_B_DQ63 AJ3

U1001E

- SB_DQ_0
- SB_DQ_1
- SB_DQ_2
- SB_DQ_3
- SB_DQ_4
- SB_DQ_5
- SB_DQ_6
- SB_DQ_7
- SB_DQ_8
- SB_DQ_9
- SB_DQ_10
- SB_DQ_11
- SB_DM_0
- SB_DM_1
- SB_DM_2
- SB_DM_3
- SB_DM_4
- SB_DM_5
- SB_DM_6
- SB_DM_7
- SB_DQS_0
- SB_DQS_1
- SB_DQS_2
- SB_DQS_3
- SB_DQS_4
- SB_DQS_5
- SB_DQS_6
- SB_DQS_7
- SB_DQS#_0
- SB_DQS#_1
- SB_DQS#_2
- SB_DQS#_3
- SB_DQS#_4
- SB_DQS#_5
- SB_DQS#_6
- SB_DQS#_7
- SB_MA_0
- SB_MA_1
- SB_MA_2
- SB_MA_3
- SB_MA_4
- SB_MA_5
- SB_MA_6
- SB_MA_7
- SB_MA_8
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- SB_MA_10
- SB_MA_11
- SB_MA_12
- SB_MA_13
- SB_MA_14

DDR SYSTEM MEMORY B

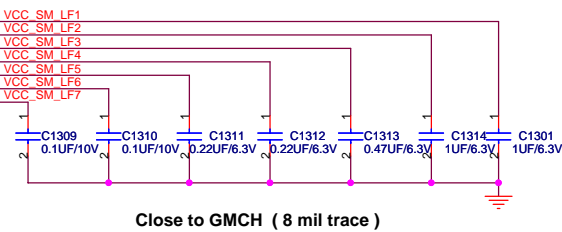
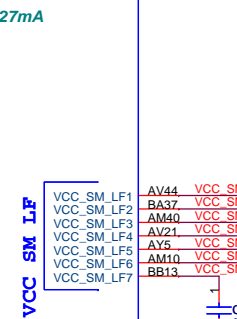
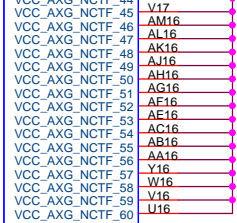
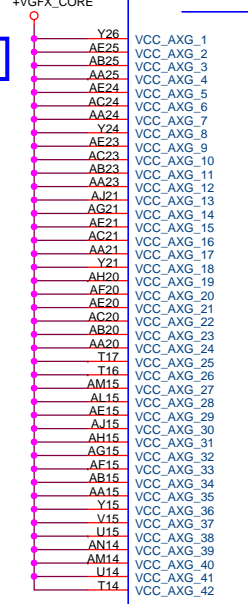
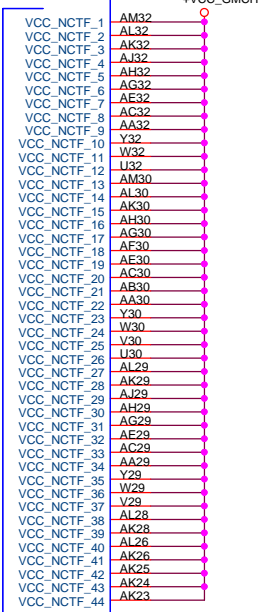
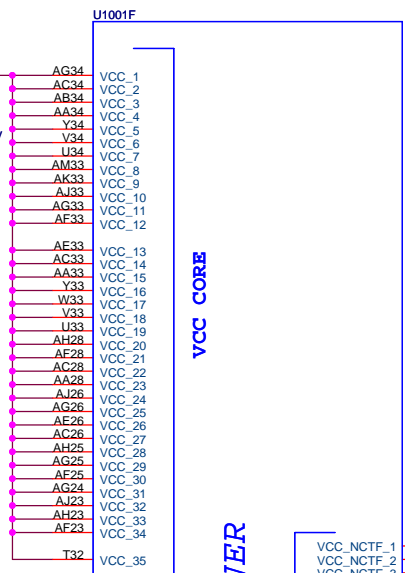
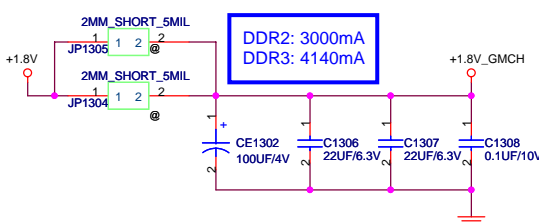
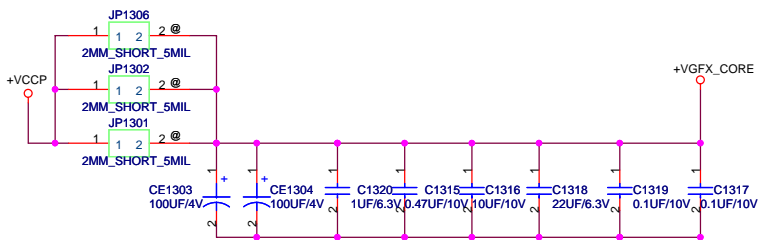
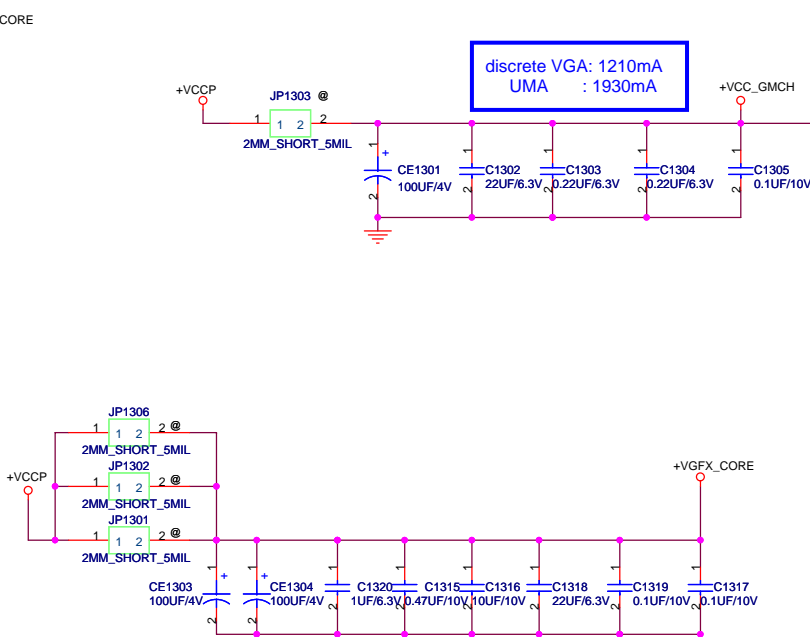
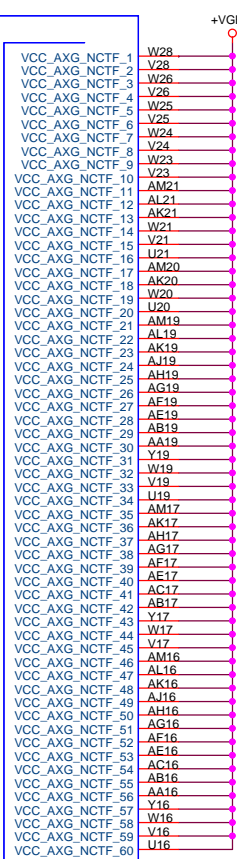
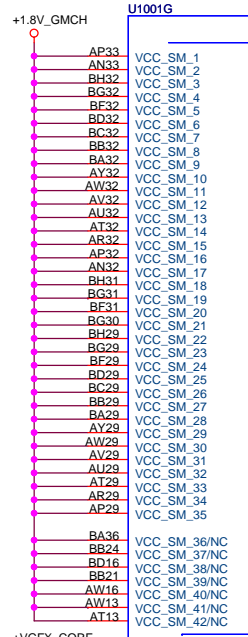
- SB_BS_0
- SB_BS_1
- SB_BS_2
- SB_RAS#
- SB_CAS#
- SB_WE#
- AM47 M_B_DM0
- AY47 M_B_DM1
- BD40 M_B_DM2
- BF35 M_B_DM3
- BG11 M_B_DM4
- BA3 M_B_DM5
- AP1 M_B_DM6
- AK2 M_B_DM7
- AL47 M_B_DQS0
- AV48 M_B_DQS1
- BG41 M_B_DQS2
- BG37 M_B_DQS3
- BH9 M_B_DQS4
- BB2 M_B_DQS5
- AU1 M_B_DQS6
- AN6 M_B_DQS7
- AL46 M_B_DQS#0
- AV47 M_B_DQS#1
- BH41 M_B_DQS#2
- BH37 M_B_DQS#3
- BG9 M_B_DQS#4
- BC2 M_B_DQS#5
- AT2 M_B_DQS#6
- AN5 M_B_DQS#7
- AV17 M_B_A0
- BA25 M_B_A1
- BC25 M_B_A2
- AU25 M_B_A3
- AW25 M_B_A4
- BB28 M_B_A5
- AU28 M_B_A6
- AW28 M_B_A7
- AT33 M_B_A8
- BD33 M_B_A9
- BB16 M_B_A10
- AW33 M_B_A11
- AY33 M_B_A12
- BH15 M_B_A13
- AU33 M_B_A14

CANTIGA_CHIPSET

CANTIGA_CHIPSET

ASUS Title : Cantiga-DDR2 (3)
 Engineer: Peter Lo

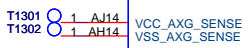
Size	Project Name	Rev
Custom	Rocky30	1.2
Date: Tuesday, April 01, 2008	Sheet 12 of 94	

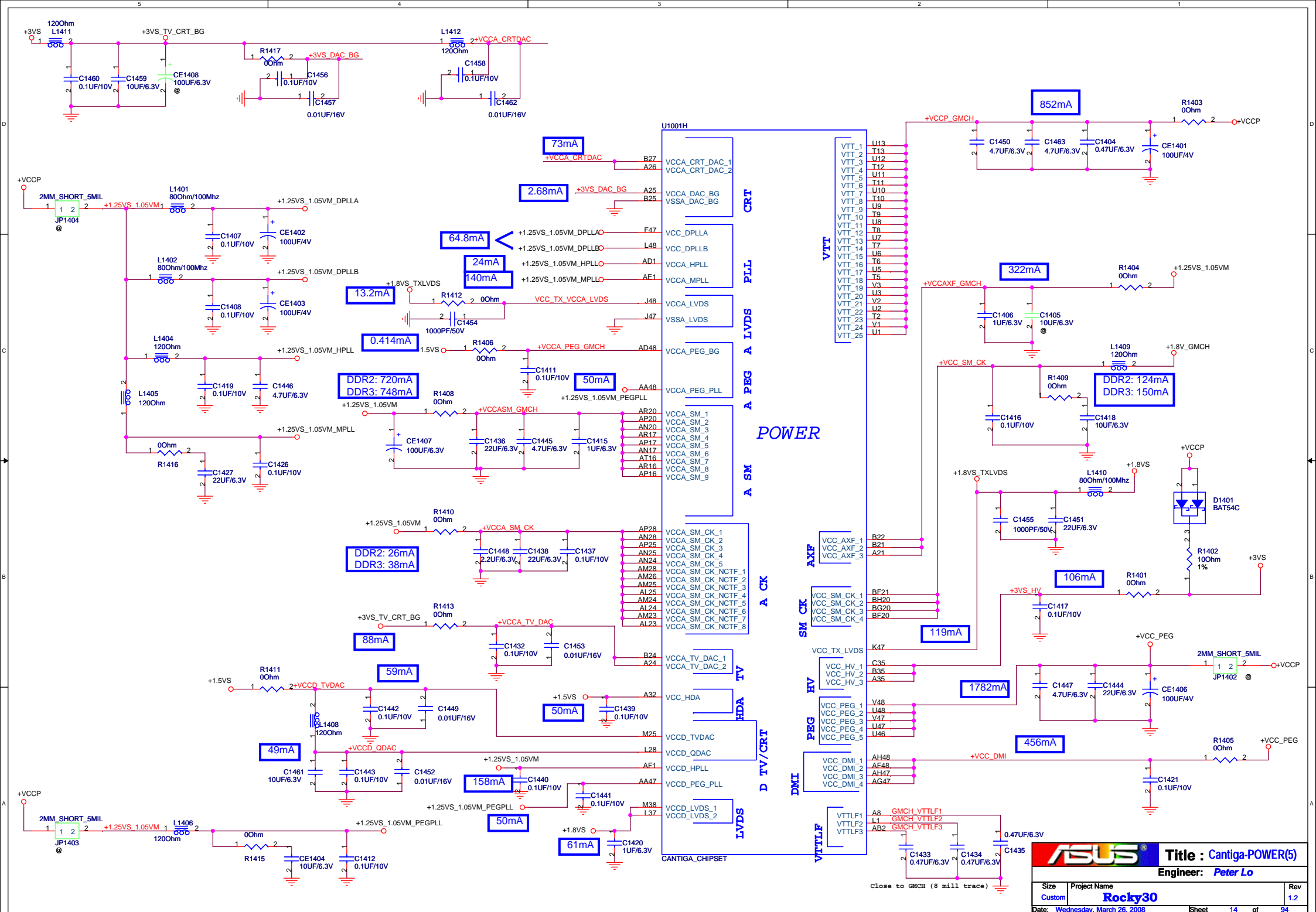


6326mA

Max: 6327mA

Route VCC_AGX_SENSE and VSS_AGX_SENSE differentially.



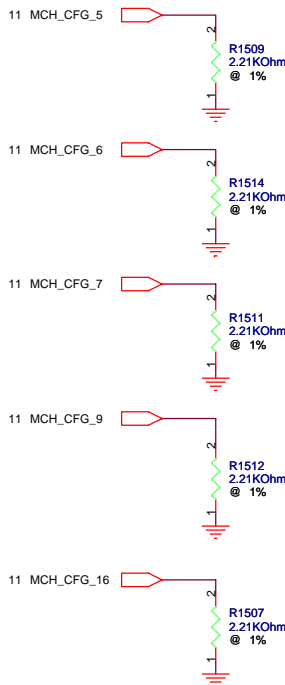
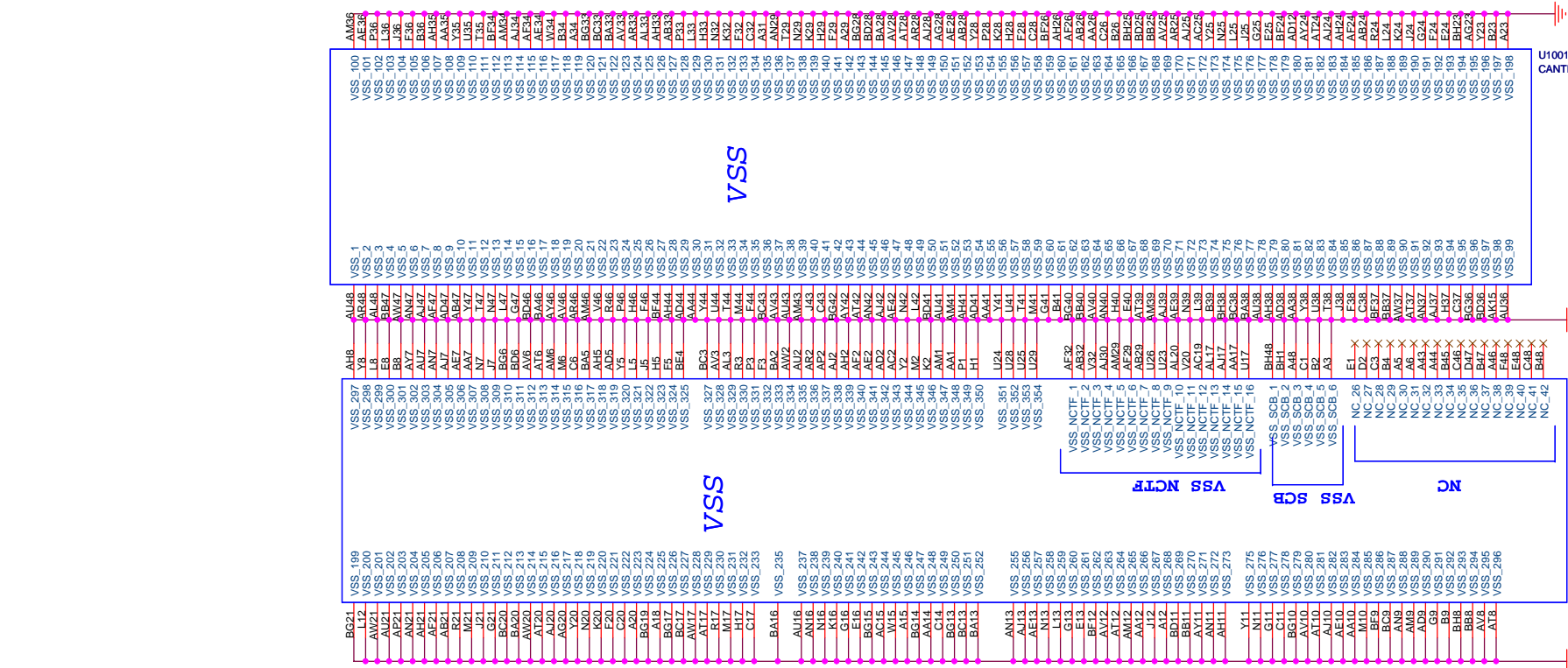


- U1001H**
- VCCA_CRT_DAC_1
 - VCCA_CRT_DAC_2
 - VCCA_DAC_BG
 - VSSA_DAC_BG
 - VCC_DPLLA
 - VCC_DPLLB
 - VCCA_HPLL
 - VCCA_MPLL
 - VCCA_LVDS
 - VSSA_LVDS
 - VCCA_PEG_BG
 - VCCA_PEG_PLL
 - VCCA_SM_1
 - VCCA_SM_2
 - VCCA_SM_3
 - VCCA_SM_4
 - VCCA_SM_5
 - VCCA_SM_6
 - VCCA_SM_7
 - VCCA_SM_8
 - VCCA_SM_9
 - VCCA_SM_CK_1
 - VCCA_SM_CK_2
 - VCCA_SM_CK_3
 - VCCA_SM_CK_4
 - VCCA_SM_CK_5
 - VCCA_SM_CK_NCTF_1
 - VCCA_SM_CK_NCTF_2
 - VCCA_SM_CK_NCTF_3
 - VCCA_SM_CK_NCTF_4
 - VCCA_SM_CK_NCTF_5
 - VCCA_SM_CK_NCTF_6
 - VCCA_SM_CK_NCTF_7
 - VCCA_SM_CK_NCTF_8
 - VCCA_TV_DAC_1
 - VCCA_TV_DAC_2
 - VCC_HDA
 - VCCD_TV_DAC
 - VCCD_QDAC
 - VCCD_HPPLL
 - VCCD_HPLL
 - VCCD_PEG_PLL
 - VCCD_LVDS_1
 - VCCD_LVDS_2

POWER

ASUS Title : Cantiga-POWER(5)
 Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.2
Date: Wednesday, March 26, 2008	Sheet 14 of 94	



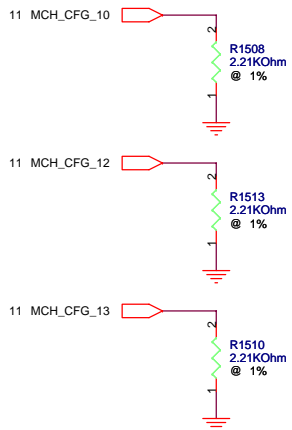
CFG5 : DMI STRAP
HIGH = DMI X 4 (Default)
LOW = DMI X 2

CFG6 : Integrated TPM Host Interface
HIGH = iTPM disable (Default)
LOW = iTPM enable

CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite
HIGH = With confidentiality (Default)
LOW = Without confidentiality

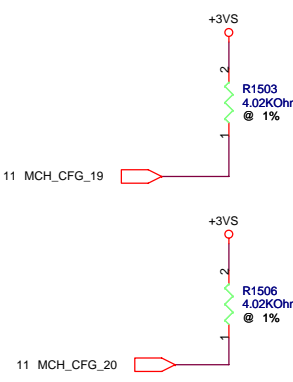
CFG9 : PCIE GRAPHIC LANE
LOW = Reverse Lanes
HIGH = Normal Operation (Default)

CFG16 : FSB Dynamic ODT
HIGH = Enable (Default)
LOW = Disable



CFG10 : PCIe Loopback
HIGH = Disable (Default)
LOW = Enable

CFG [13:12] : XOR/ALL-Z
00 = Reserved
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation (Default)



CFG19 : DMI Lane Reversal
LOW = NORMAL (default)
HIGH = Reverse Lanes

CFG20 : SDVO/PCIE CONCURRENT MODE
LOW = ONLY SDVO or PCIE is Operational (Default)
HIGH = SDVO and PCIE are operating simultaneously via the PEG port

5

4

3

2

1

D

D

C

C

B

B

A

A

		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size	Project Name	Rev	
B	Rocky30	1.2	
Date: <i>Friday, March 14, 2008</i>		Sheet	16 of 94

5

4

3

2

1

5

4

3

2

1

D

D

C


C

B

B

A

A

		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size	Project Name	Rev	
B	Rocky30	1.2	
Date: <i>Friday, March 14, 2008</i>		Sheet	17 of 94

5

4

3

2

1

5

4

3

2

1

D

D

C


C

B

B

A

A

		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size	Project Name	Rev	
B	Rocky30	1.2	
Date: <i>Friday, March 14, 2008</i>		Sheet	18 of 94

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		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size	Project Name		Rev
B	Rocky30		1.2
Date: <i>Friday, March 14, 2008</i>		Sheet	19 of 94

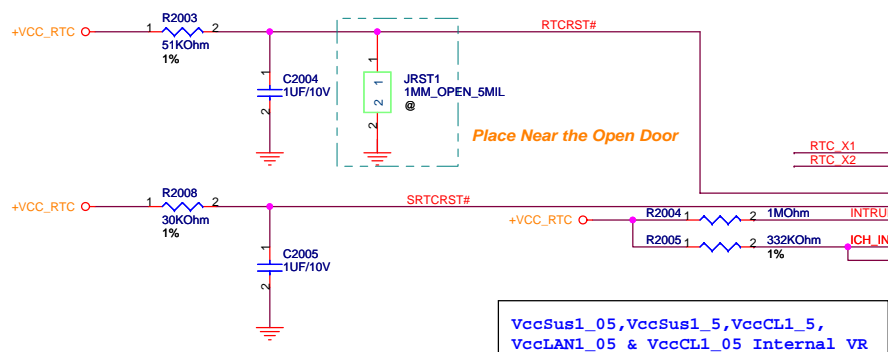
5

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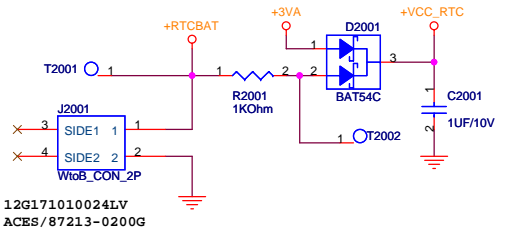
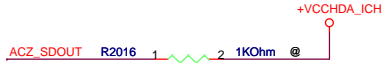
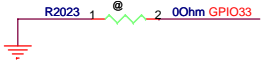
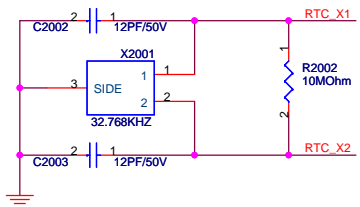
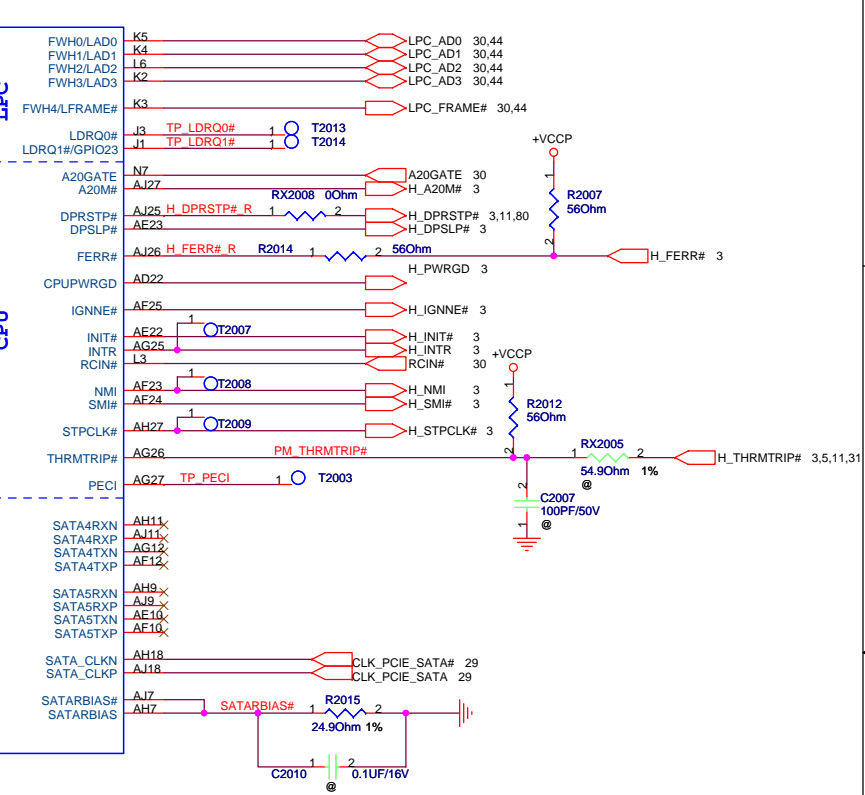
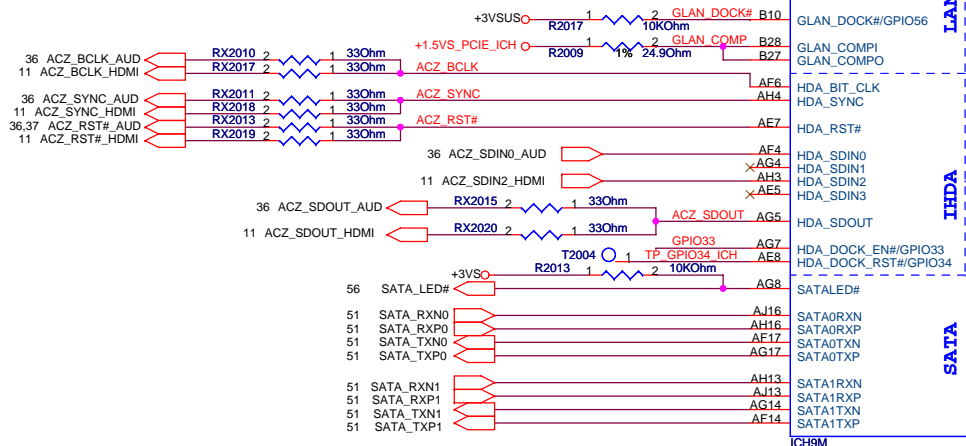
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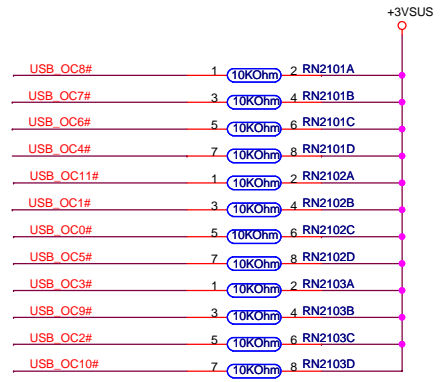
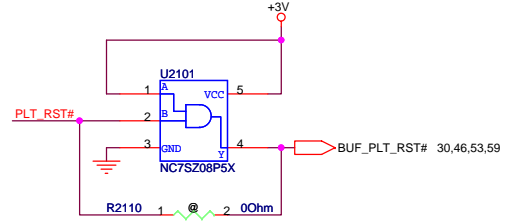
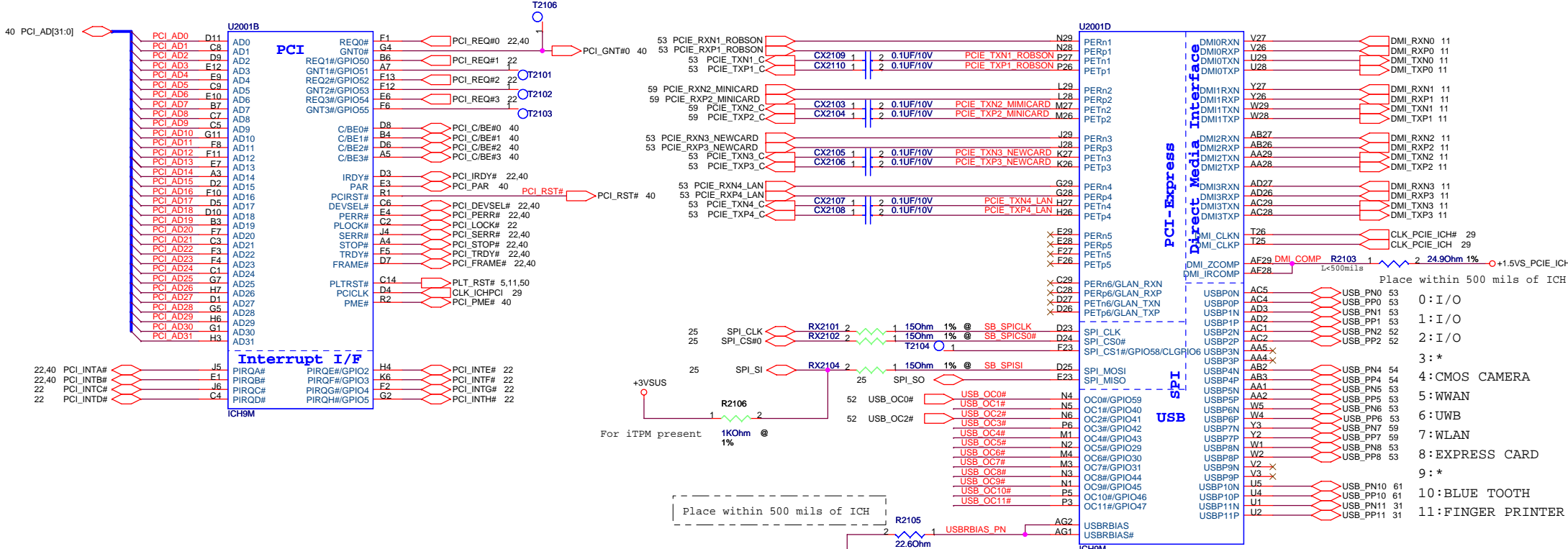
VccSus1_05, VccSus1_5, VccCL1_5,
VccLAN1_05 & VccCL1_05 Internal VR
High = Enable (Default)
Low = Disable



[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap
00 = Reserved
01 = Enter XOR Chain
10 = Normal Operation (Default)
11 = Set PCIe Port Config Bit 1

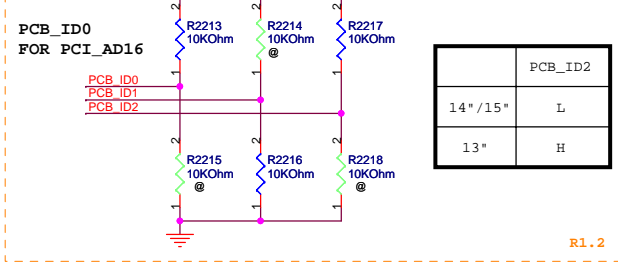
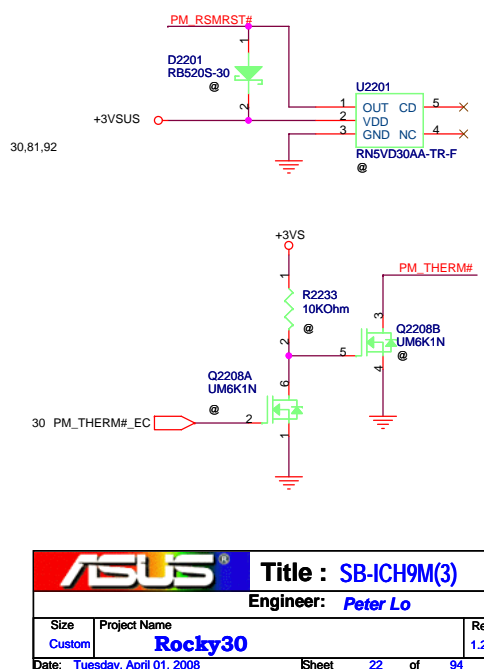
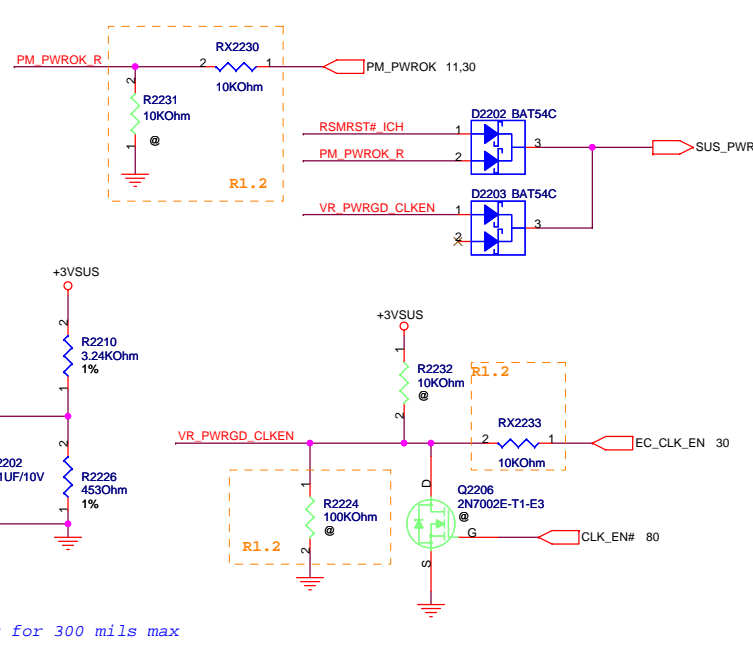
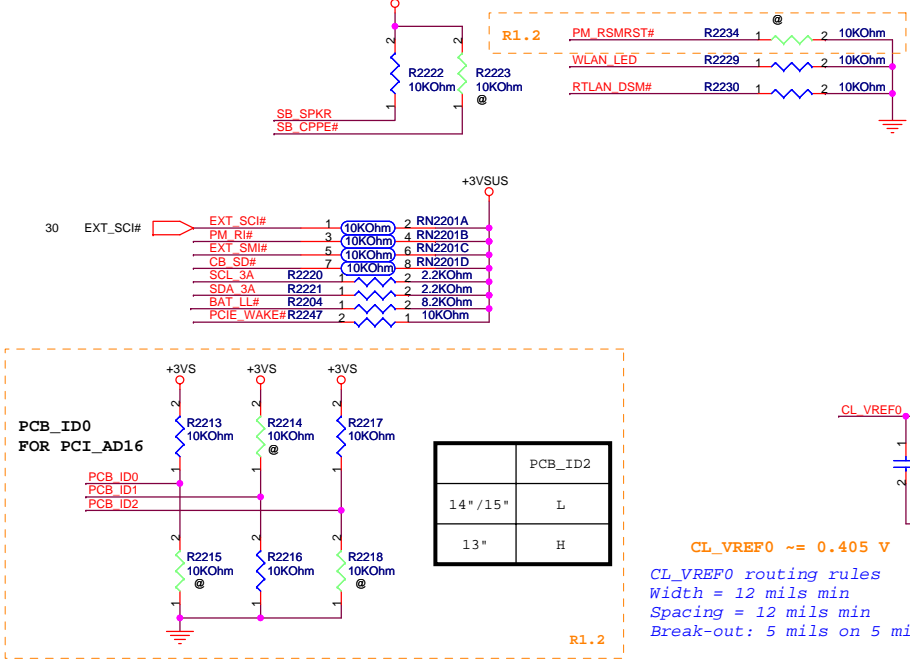
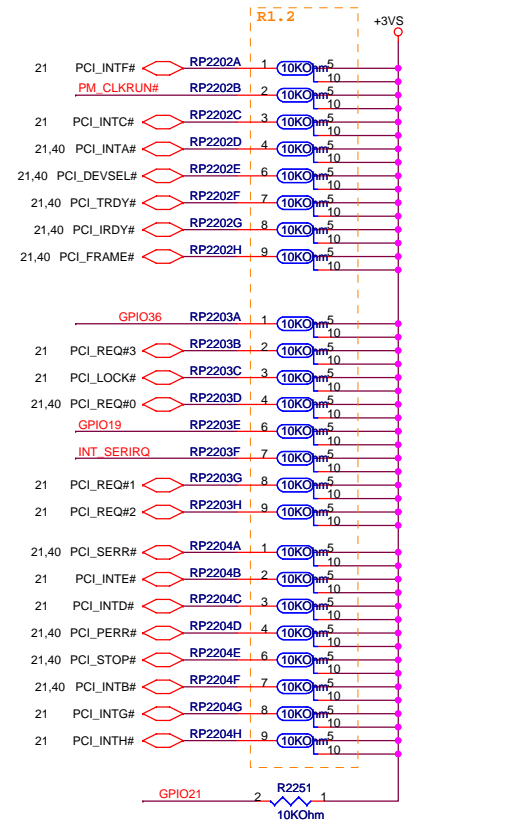
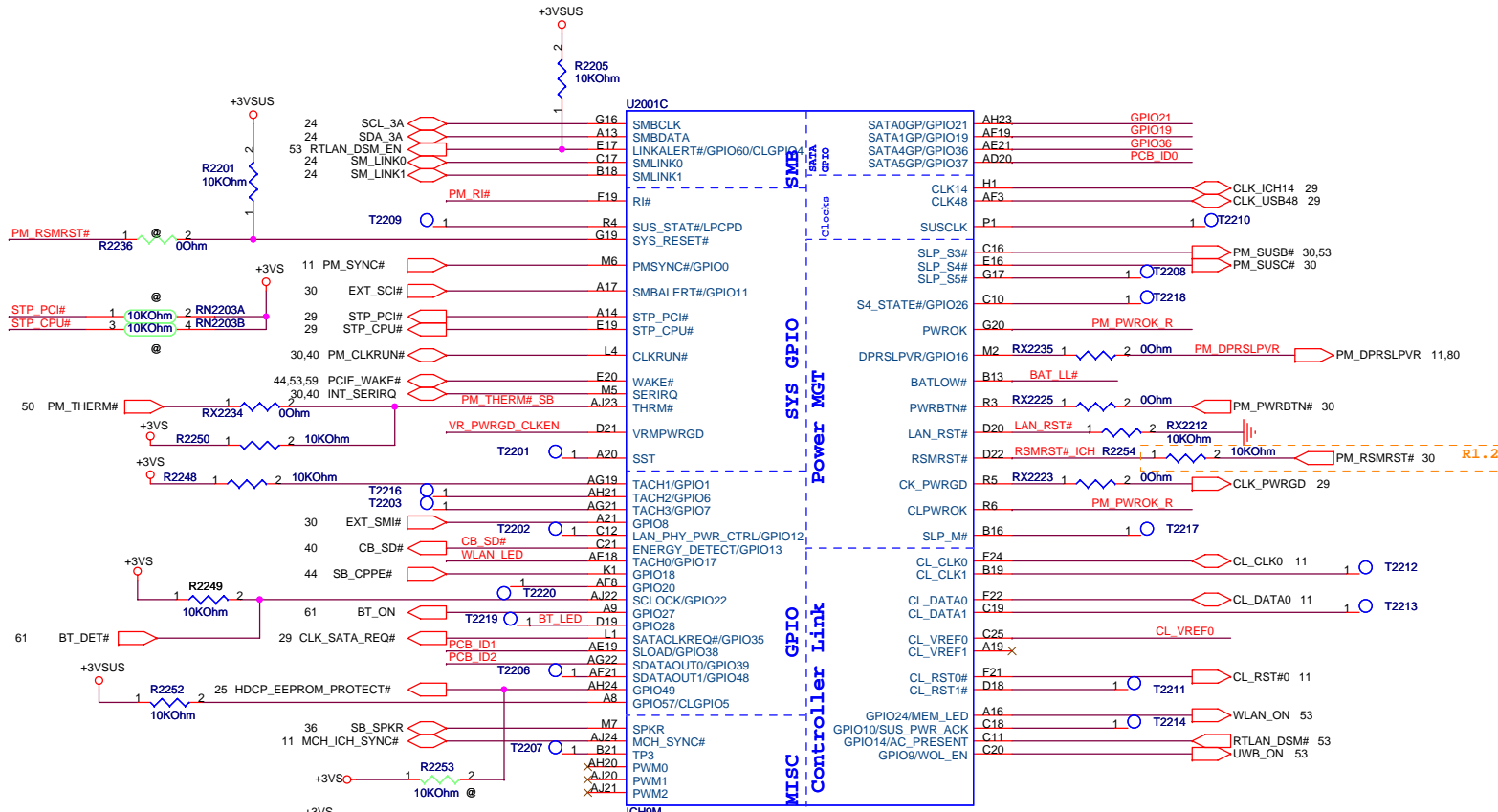
12G171010024LV
ACBS/87213-0200G

ASUS		Title : SB-ICH9M(1)	
		Engineer: Peter Lo	
Size	Project Name	Rev	
Custom	Rocky30	1.2	
Date: Tuesday, April 01, 2008		Sheet	20 of 94



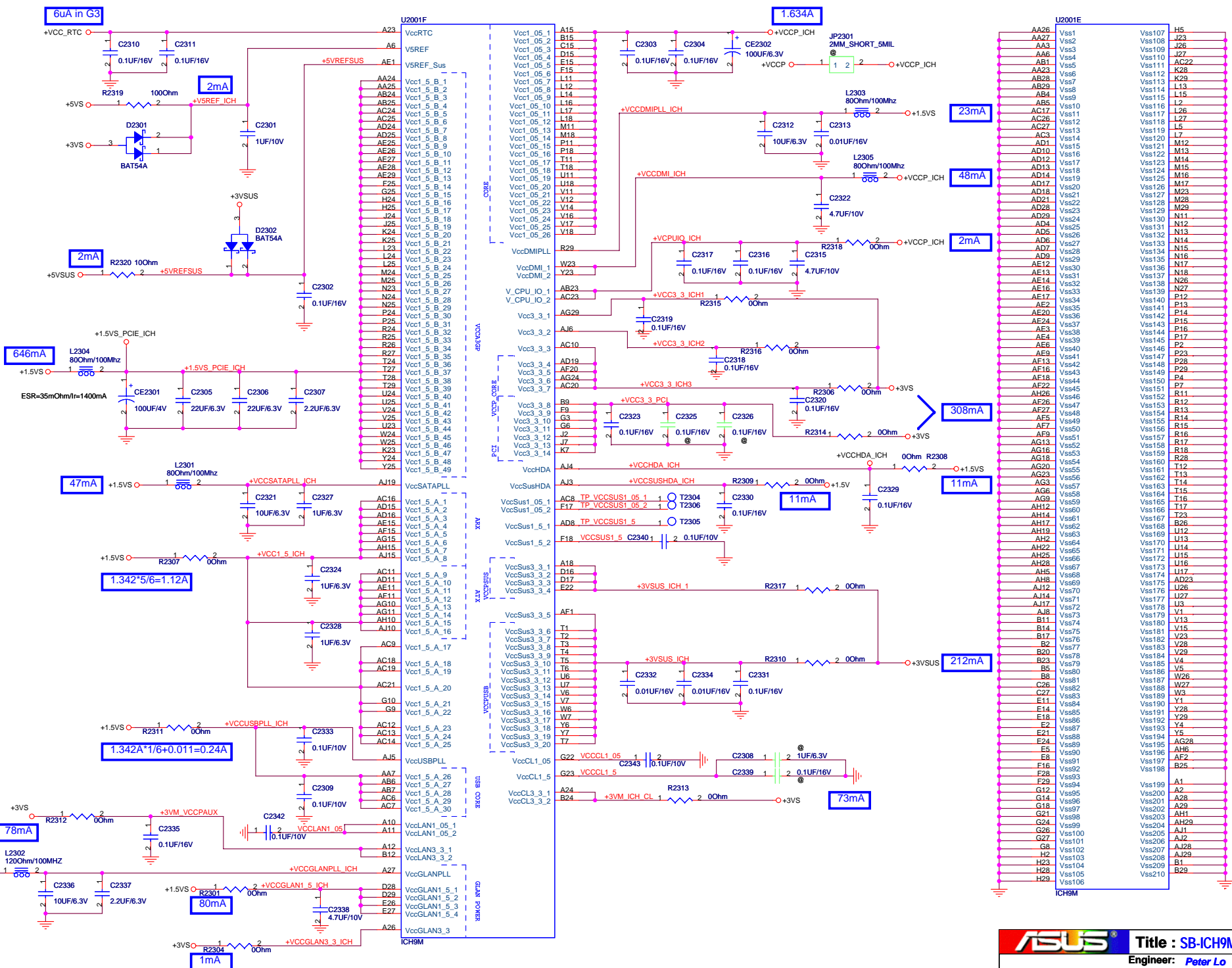
ICH9M Boot BIOS select

IPC	GNT#0	CS#1	(default)
PCI	1	0	
SPI	0	1	



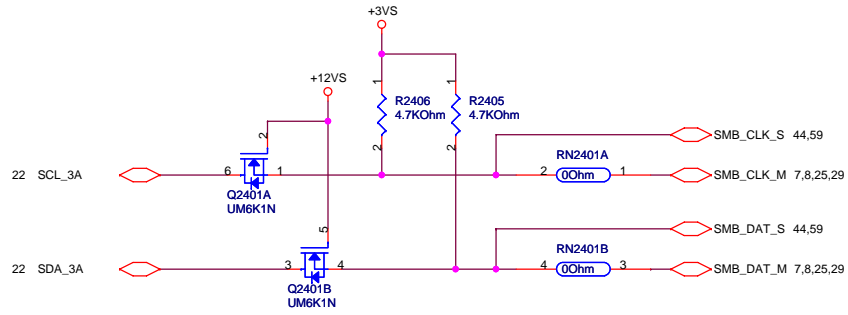
PCB_ID1	PCB_ID2
14" / 15"	L
13"	H

CL_VREF0 ~ 0.405 V
 CL_VREF0 routing rules
 Width = 12 mils min
 Spacing = 12 mils min
 Break-out: 5 mils on 5 mils for 300 mils max



ICH9-M

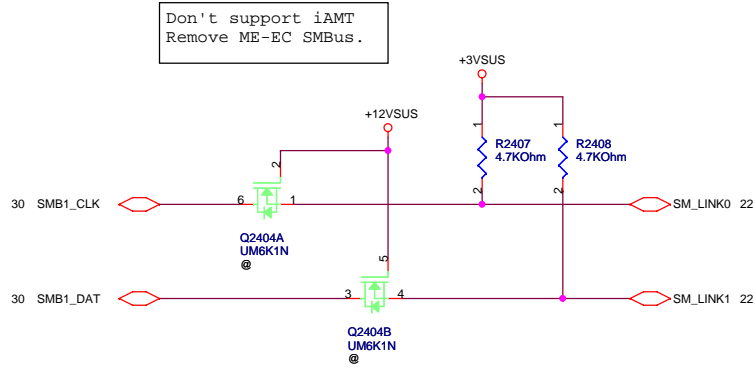
ICH9M



NEWCARD, WLAN
 CLOCK GEN
 SO-DIMM0 , SO-DIMM1
 NEWCARD, WLAN
 CLOCK GEN
 SO-DIMM0 , SO-DIMM1

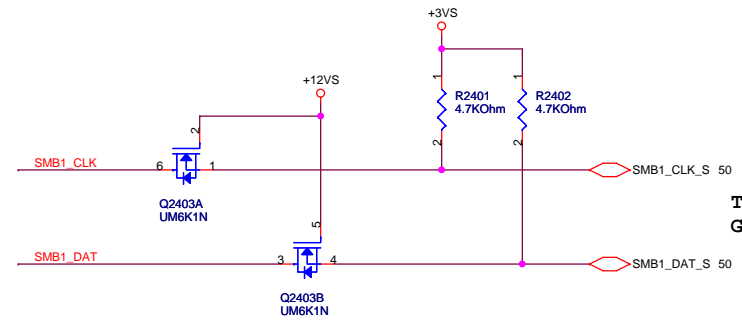
EC

EC

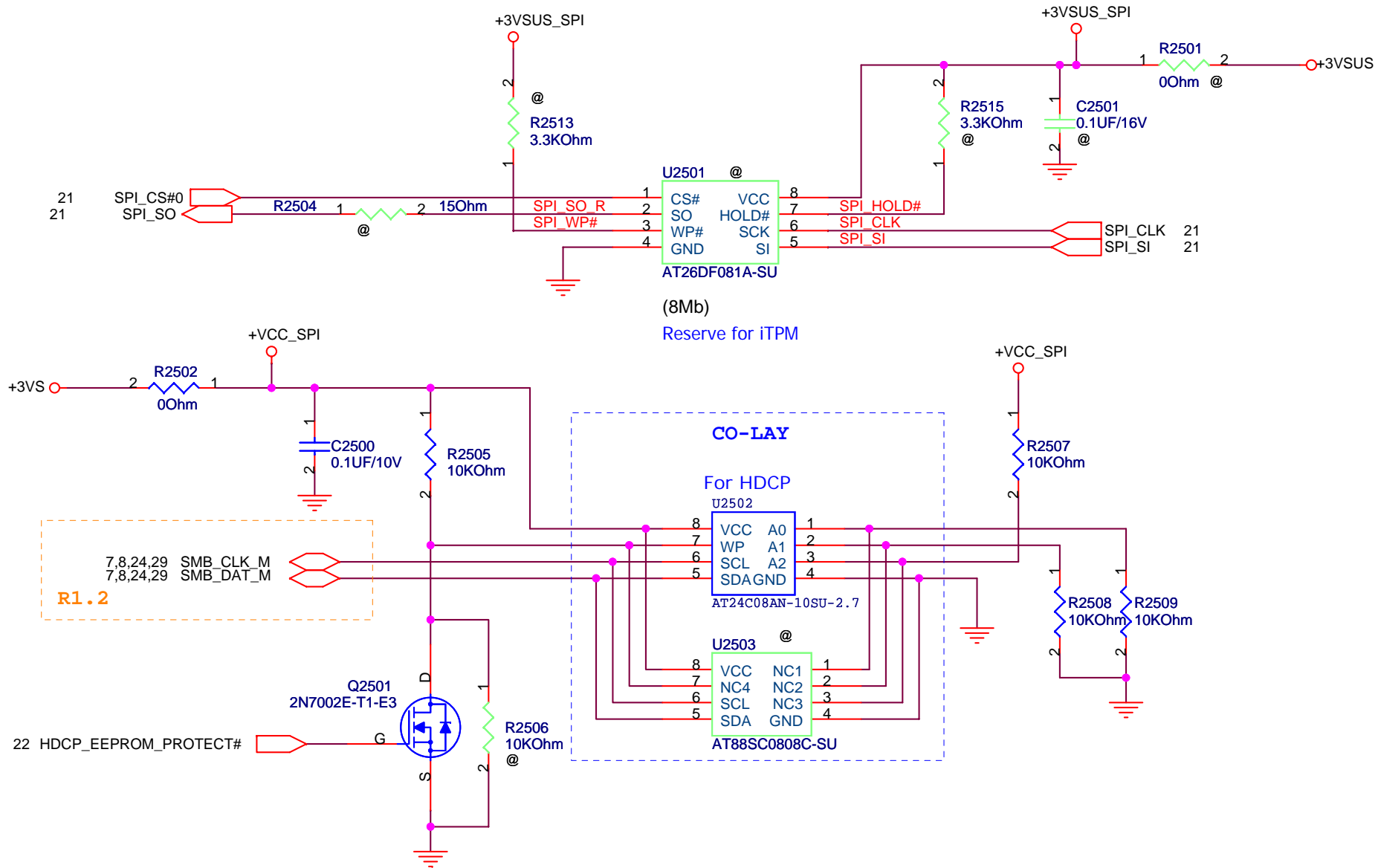


SB

EC




THERMAL IC
 G781, G781-1



U2502-AT24C08A :
 Stuff : R2506 ; U2502 ; R2507 ; R2508 ; R2509
 Nostuff : R2505

U2503-AT88SC0808C :
 Stuff : U2503
 Nostuff : R2505 ; R2506 ; R2507 ; R2508 ; R2509

		Title : SPI ROM	
		Engineer: Peter Lo	
Size Custom	Project Name Rocky30		Rev 1.2
Date: Tuesday, April 01, 2008		Sheet 25 of 94	

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Title :

Engineer: *Peter Lo*

Size	Project Name	Rev
A	Rocky30	1.2

Date: **Friday, March 14, 2008** Sheet **26** of **94**

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		Title :
		Engineer: <i>Peter Lo</i>
Size	Project Name	Rev
A	Rocky30	1.2
Date: <i>Friday, March 14, 2008</i>		Sheet <i>27</i> of <i>94</i>

5

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Title :

Engineer: *Peter Lo*

Size	Project Name	Rev
A	Rocky30	1.2

Date: **Friday, March 14, 2008** Sheet **28** of **94**

5

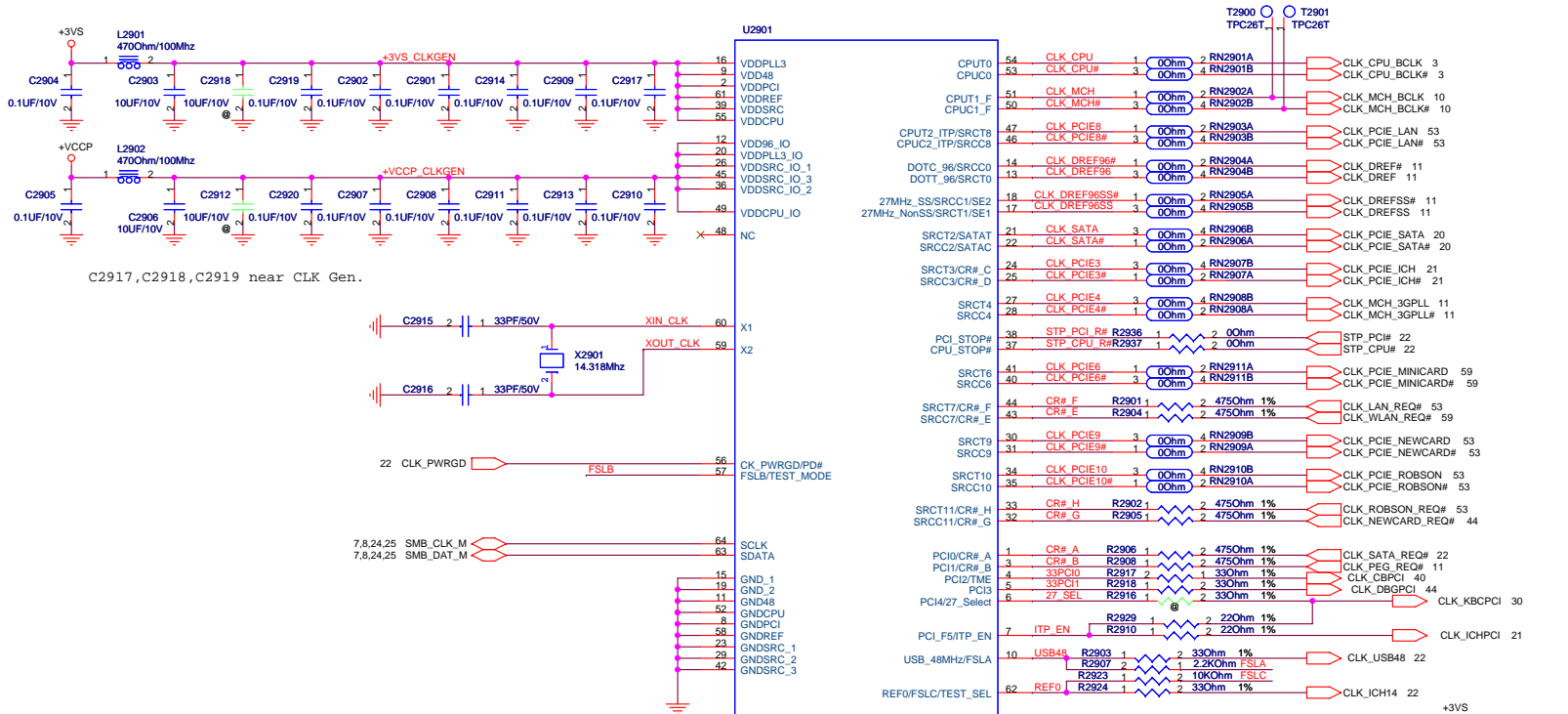
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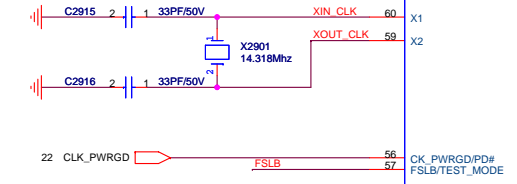
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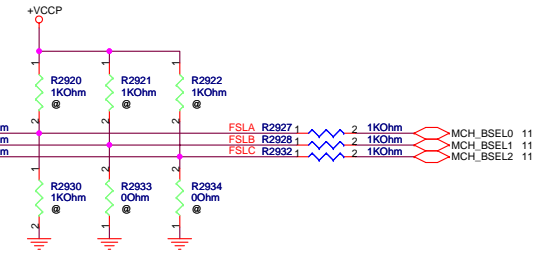
+VCCP ○ +VCCP 5,10,11,13,14,20,23,80,82
 +3VS ○ +3VS 3,7,8,11,14,15,20,22,23,24,25,30,31,37,40,41,45,46,48,50,51,53,54,57,58,59,61,91,92



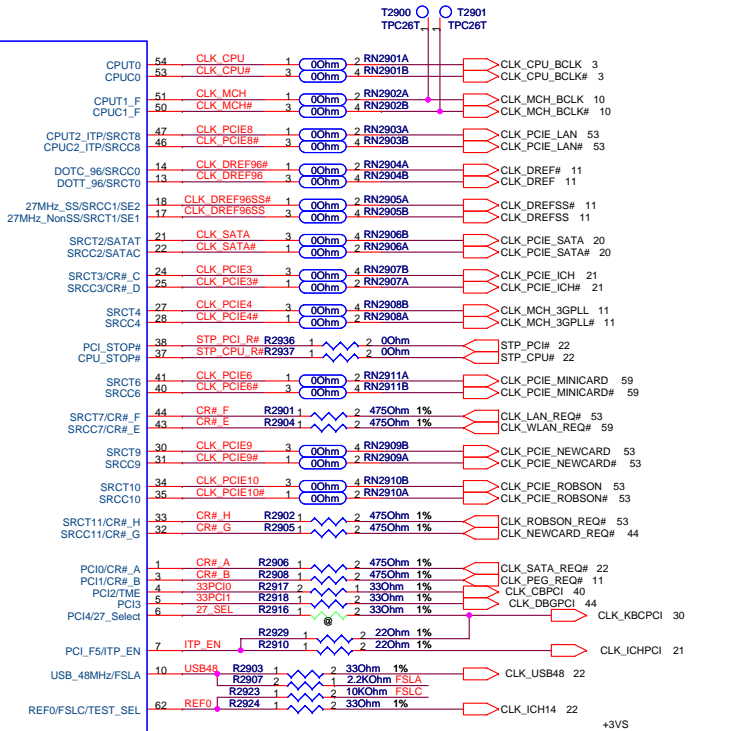
C2917, C2918, C2919 near CLK Gen.



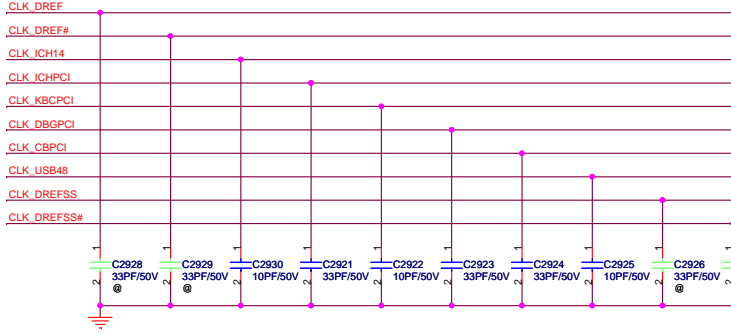
7,8,24,25 SMB_CLK_M
 7,8,24,25 SMB_DAT_M



BCLK	FSB	FSLC	FSLB	FSLA
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0



C2921, C2922, C2923, C2924, C2925, C2926, C2927, C2928, C2929, C2930 near CLK Gen.



CR#_A	0 = SRC 0	
	1 = SRC 2	SATA
CR#_B	0 = SRC 1	
	1 = SRC 4	MCH
CR#_C	0 = SRC 0	
	1 = SRC 2	
CR#_D	0 = SRC 1	
	1 = SRC 4	
CR#_E	SRC 6	WLAN
CR#_F	SRC 8	LAN
CR#_G	SRC 9	New Card
CR#_H	SRC 10	Robson

Latched Input Select

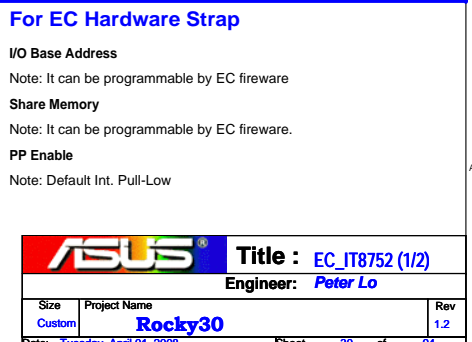
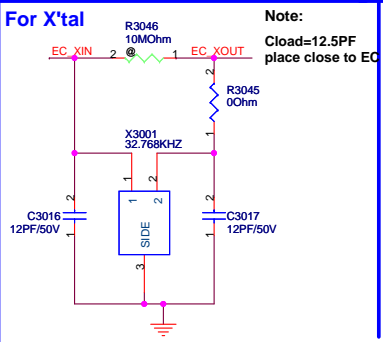
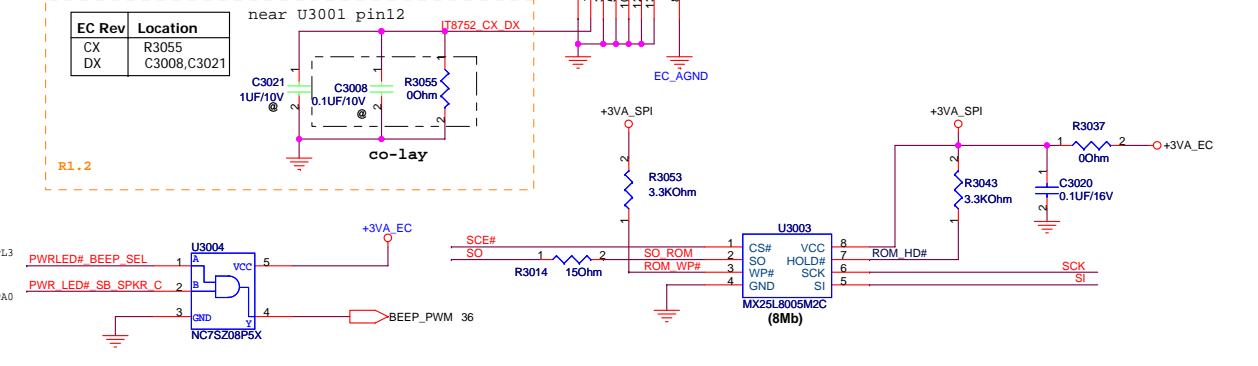
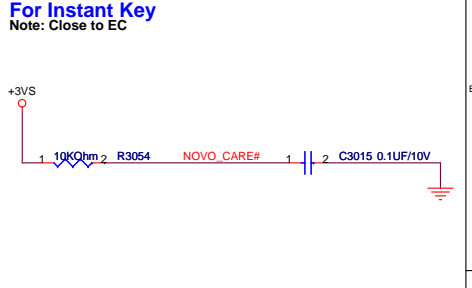
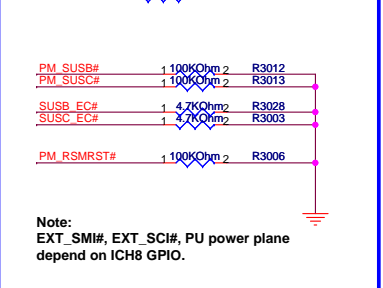
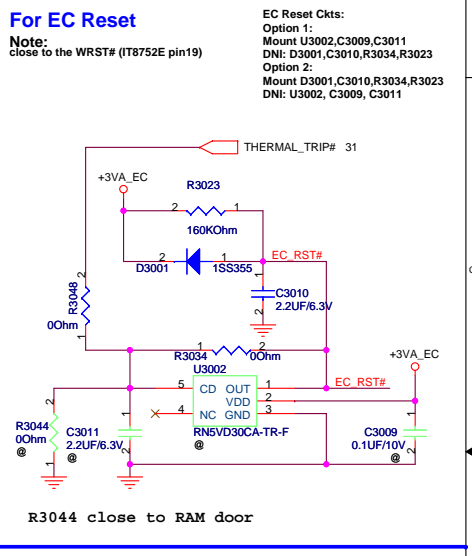
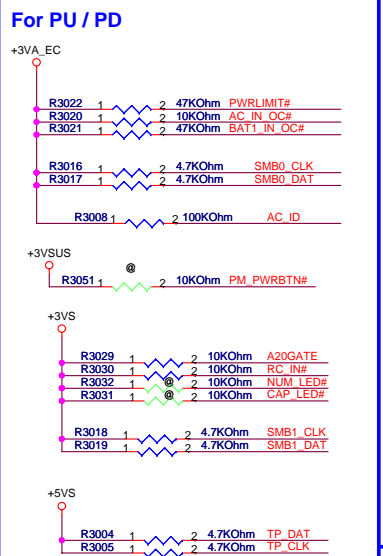
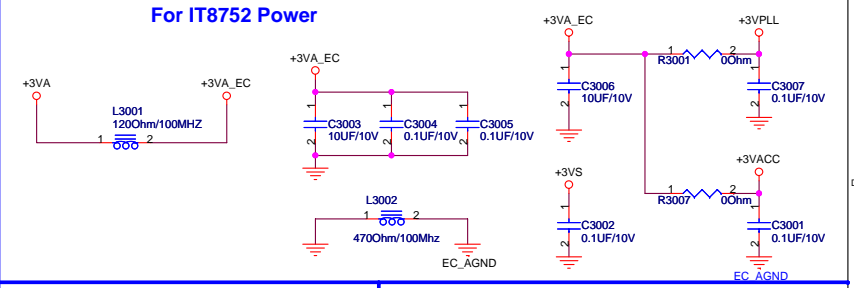
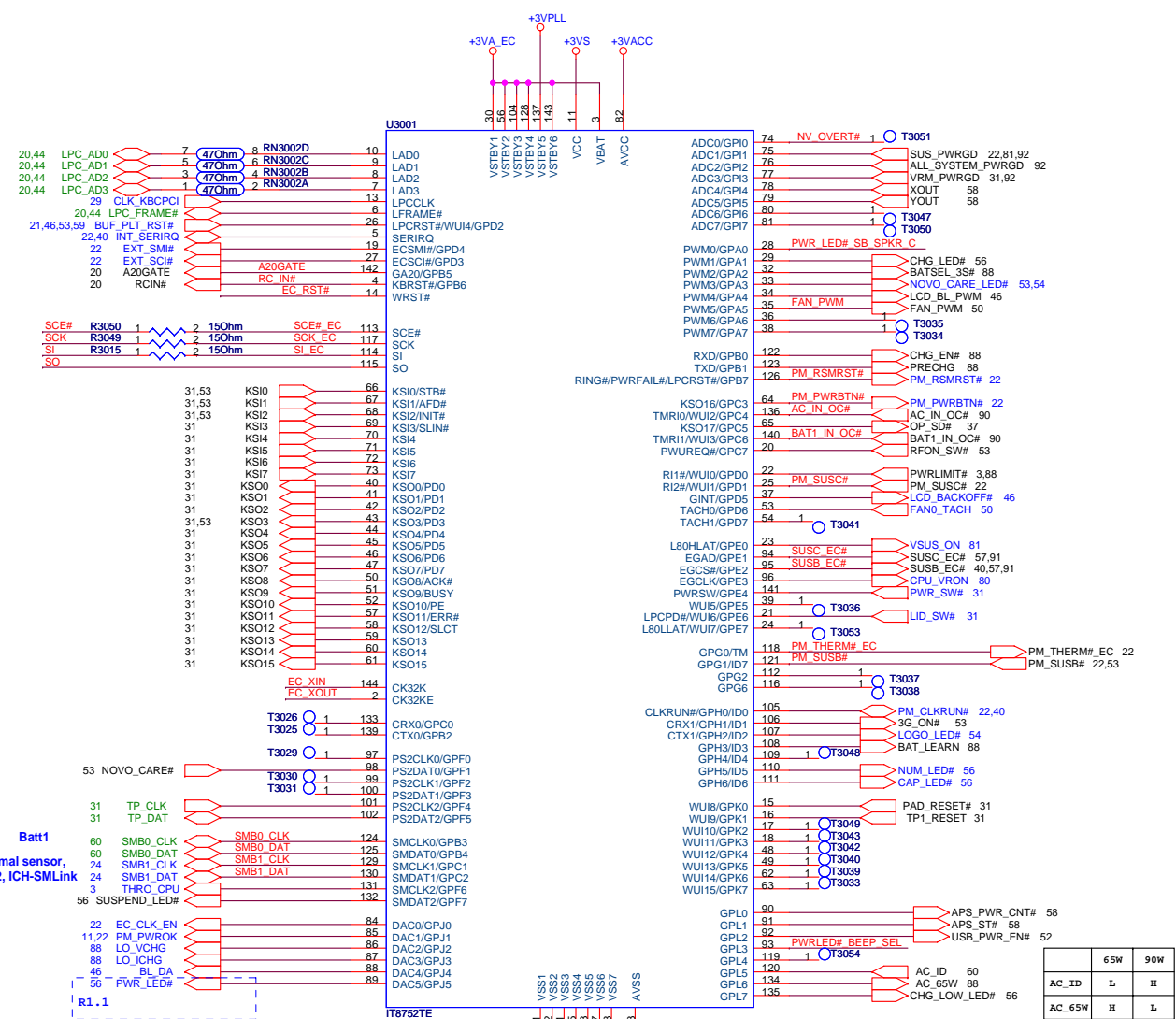
0 = SRC 8 Decide pin
 1 = CPU_ITP_CLK 46, 47



27_Select=0, Decide pin
 pin#13/14=DOT96; 13/14, 17/18
 pin#17/18=LCD_SST;

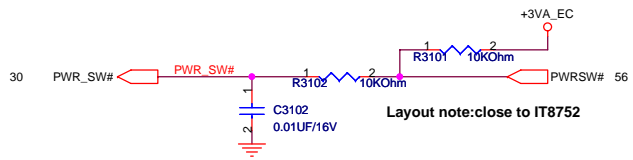
27_Select=1,
 pin#13/14=SRC0;
 pin#17/18=27MHz non-spread SE clock;

For GM/GL, need to PD for 96MHz output.
 For PM, need to PU for 27MHz output.

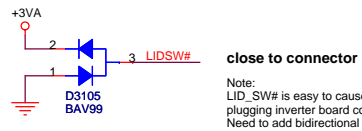
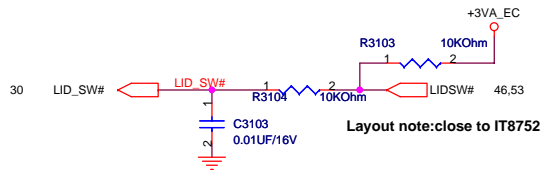


For Switch

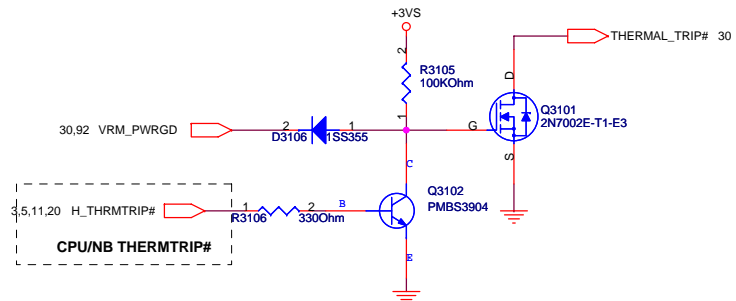
PWR SWITCH



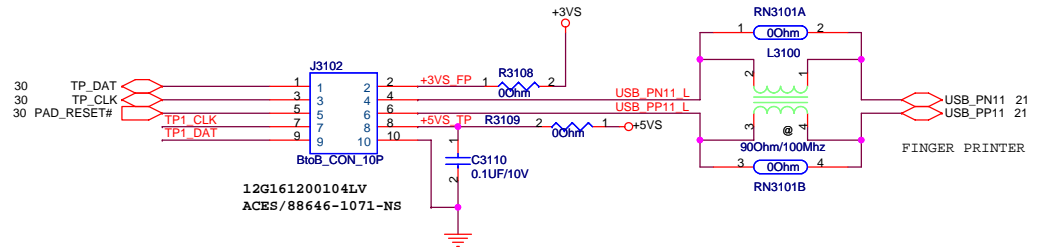
LID SWITCH



For Thermal Control Method

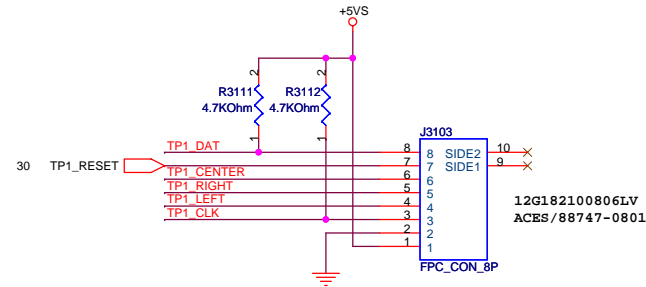


TOUCH PAD CONN

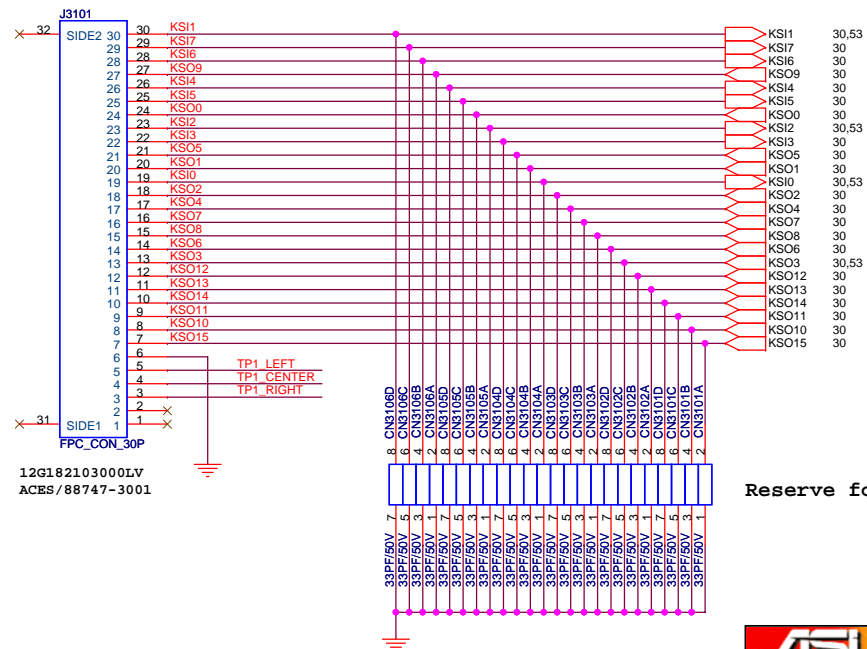


TP : Touch Pad
TP1: Track Point

TRACK POINT CONN



Keyboard Connector



Reserve for WWAN

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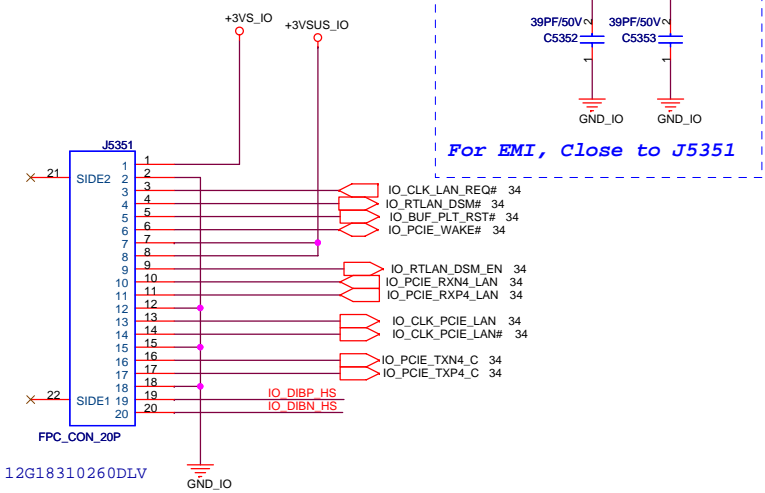


Engineer: *Peter Lo*

Size	Project Name	Rev
Custom	Rocky30	1.2

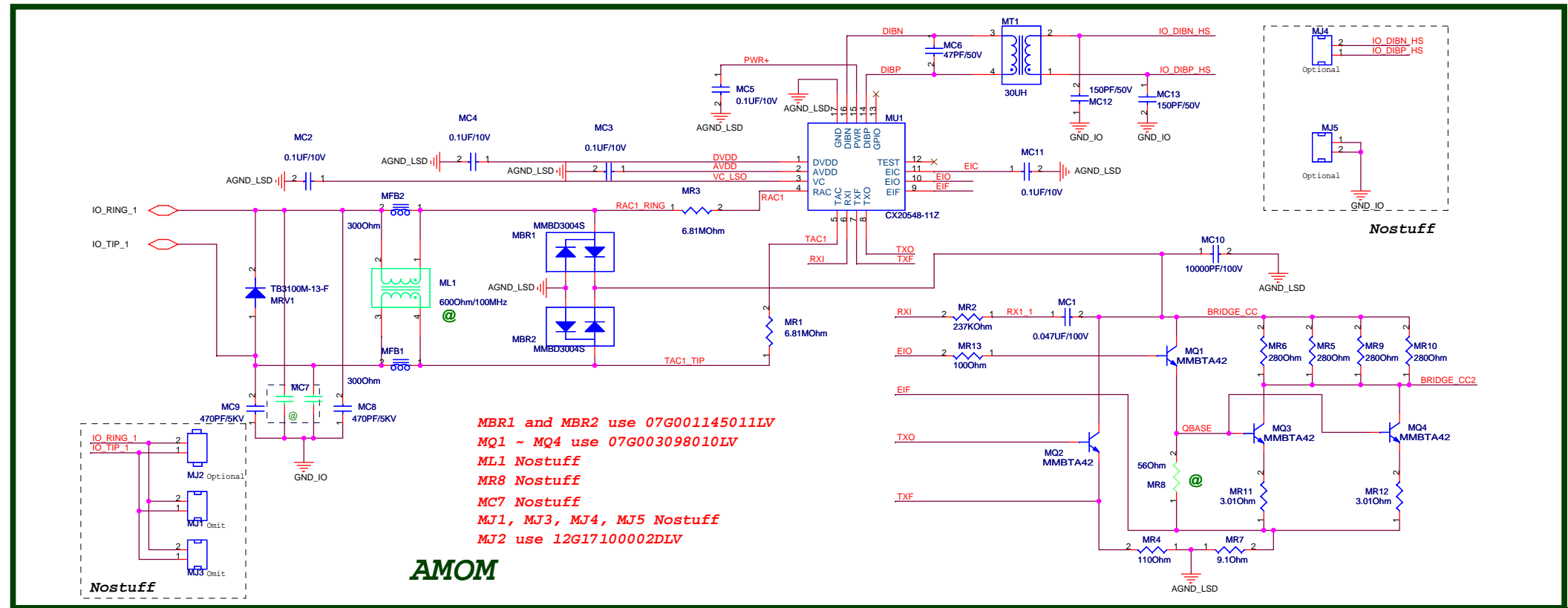
Date: *Friday, March 14, 2008* Sheet 32 of 94

IO BOARD



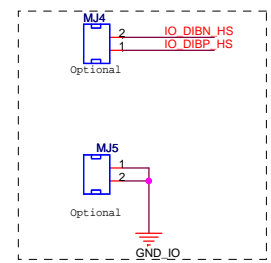
For EMI, Close to J5351

12G18310260DLV
GND_IO



MBR1 and MBR2 use 07G001145011LV
MQ1 ~ MQ4 use 07G003098010LV
ML1 Nostuff
MR8 Nostuff
MC7 Nostuff
MJ1, MJ3, MJ4, MJ5 Nostuff
MJ2 use 12G17100002DLV

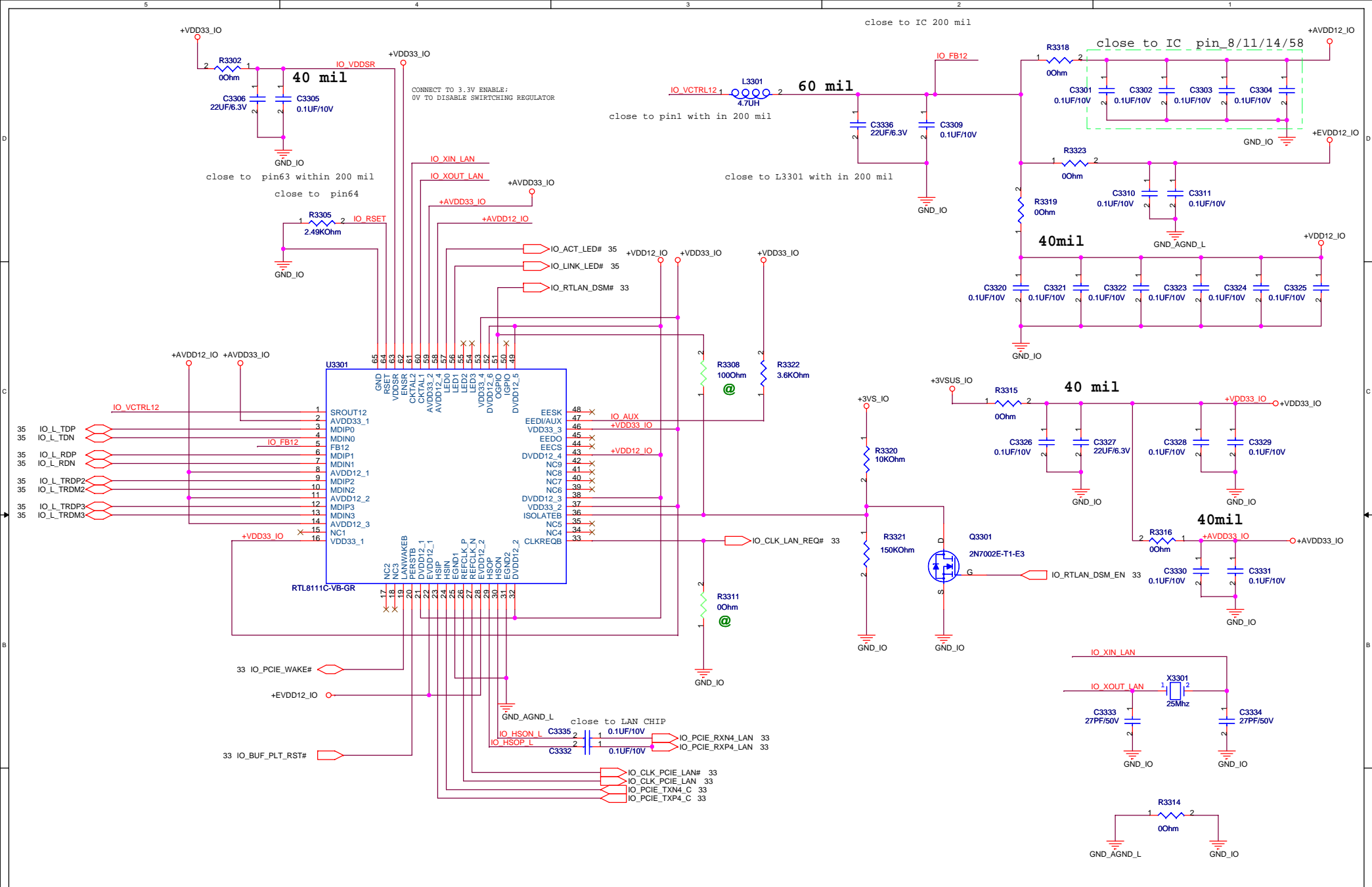
AMOM

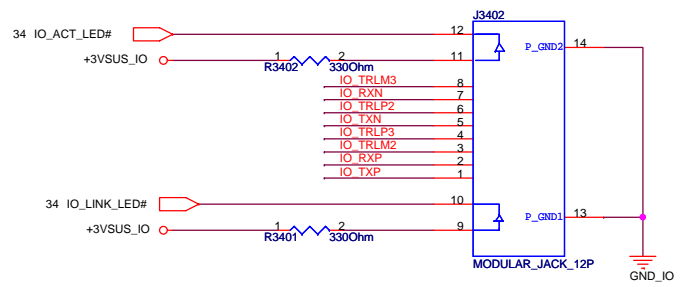
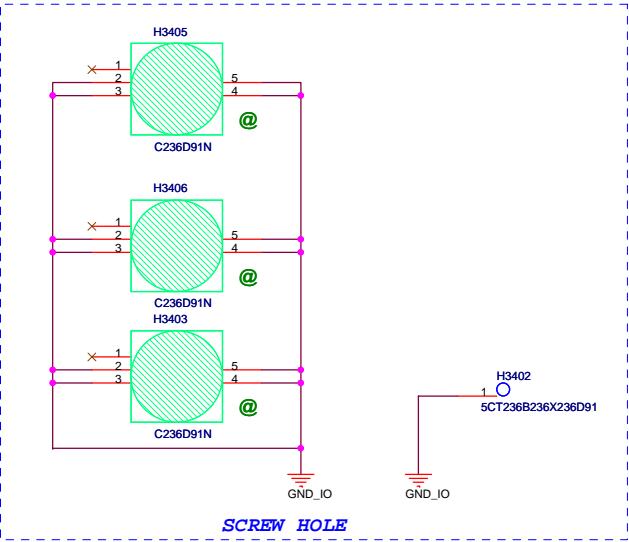
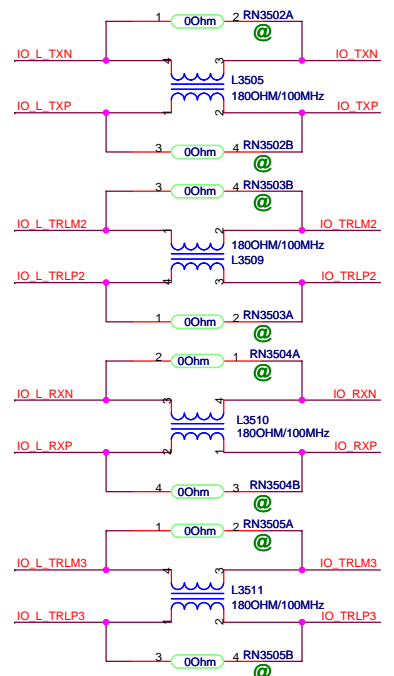
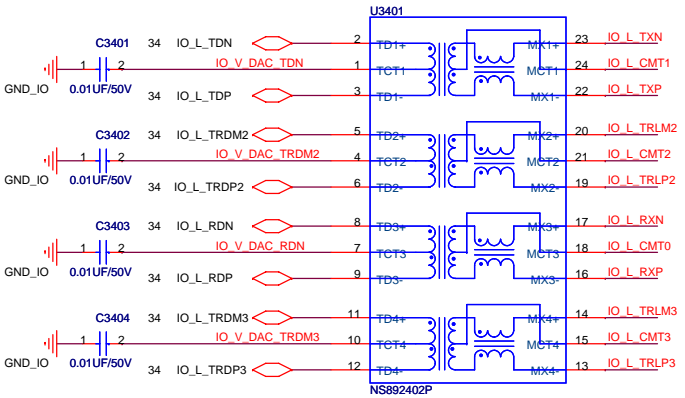
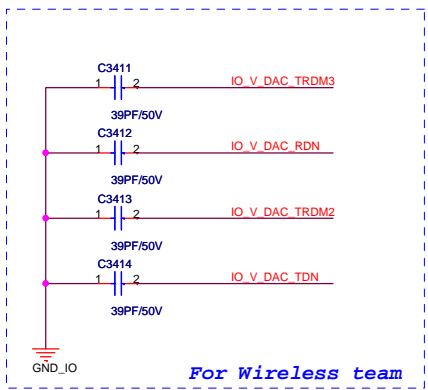


Nostuff

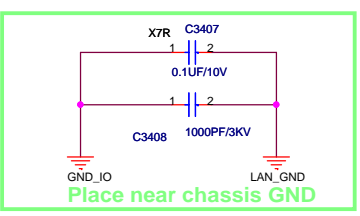
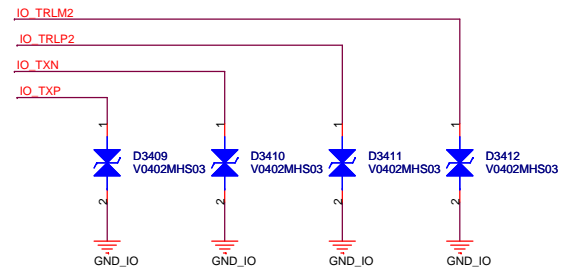
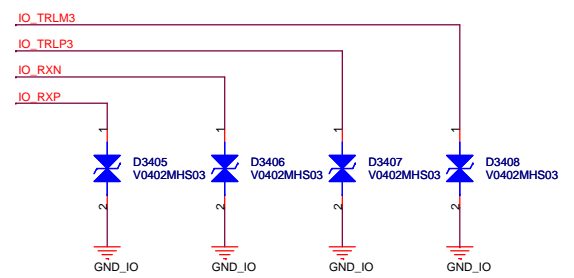
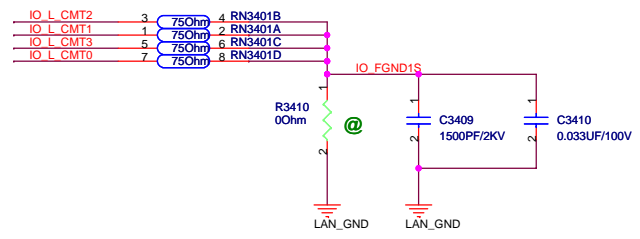
PEGATRON Title : IO BRD CONN&DAA
 Engineer: **Warren**

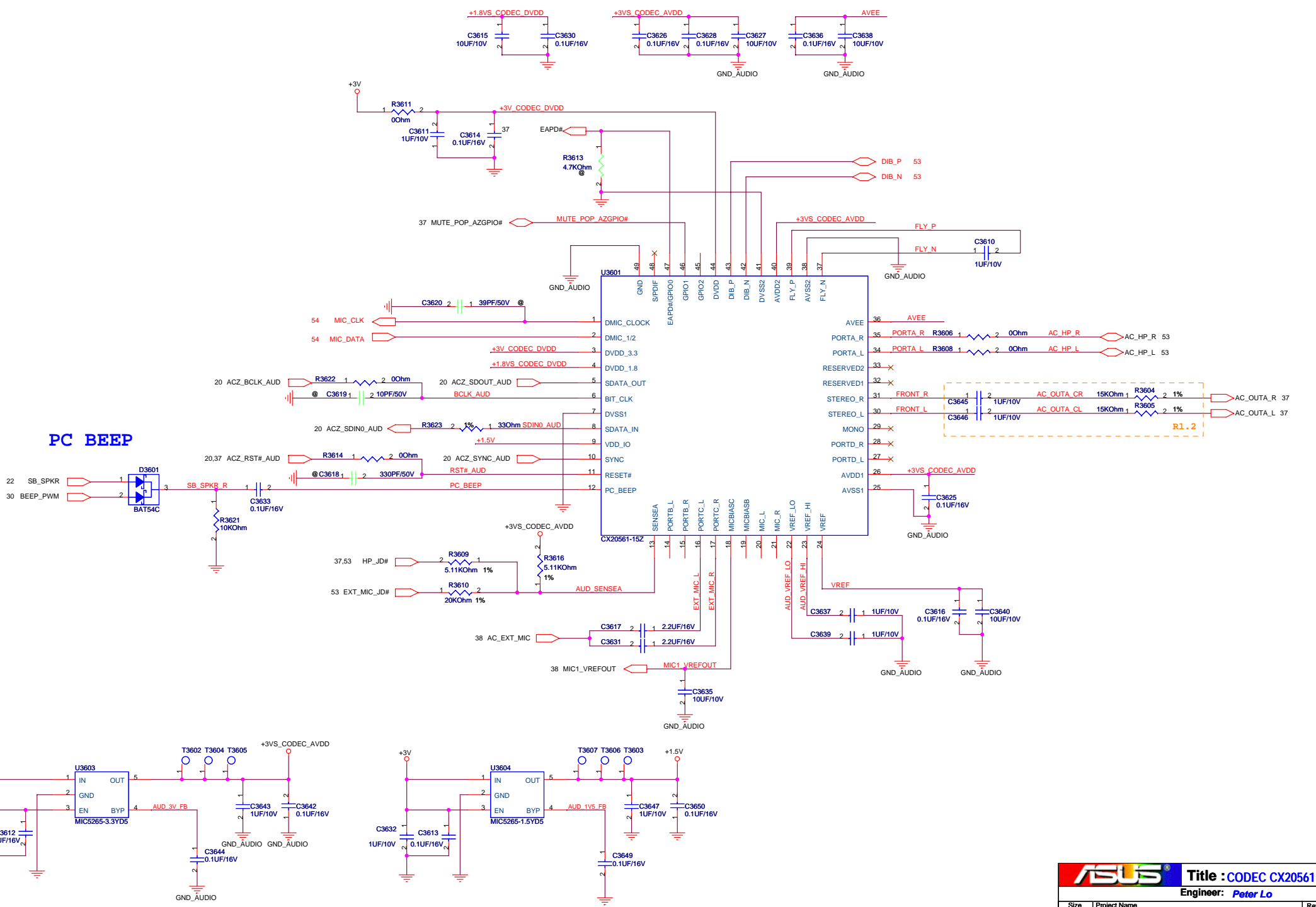
Size	Project Name	Rev
Custom	Rocky 30 IO Board	1.2
Date: Tuesday, April 01, 2008	Sheet 33 of 94	





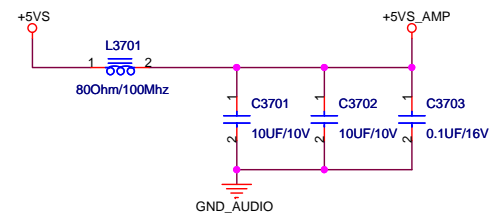
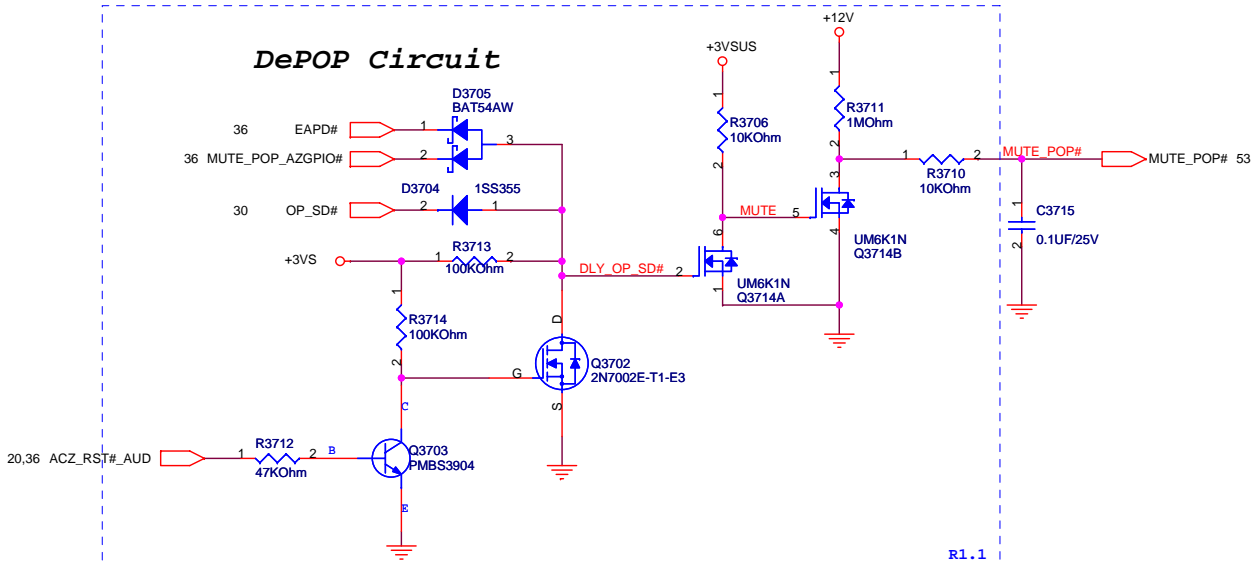
12G148301089LV
ALLTOP/C100Q2-10806-L



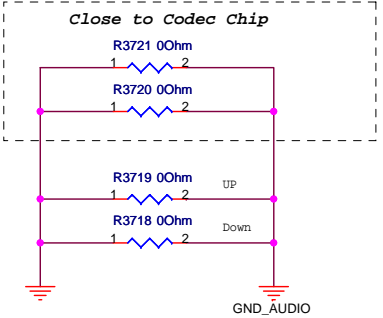


PC BEEP

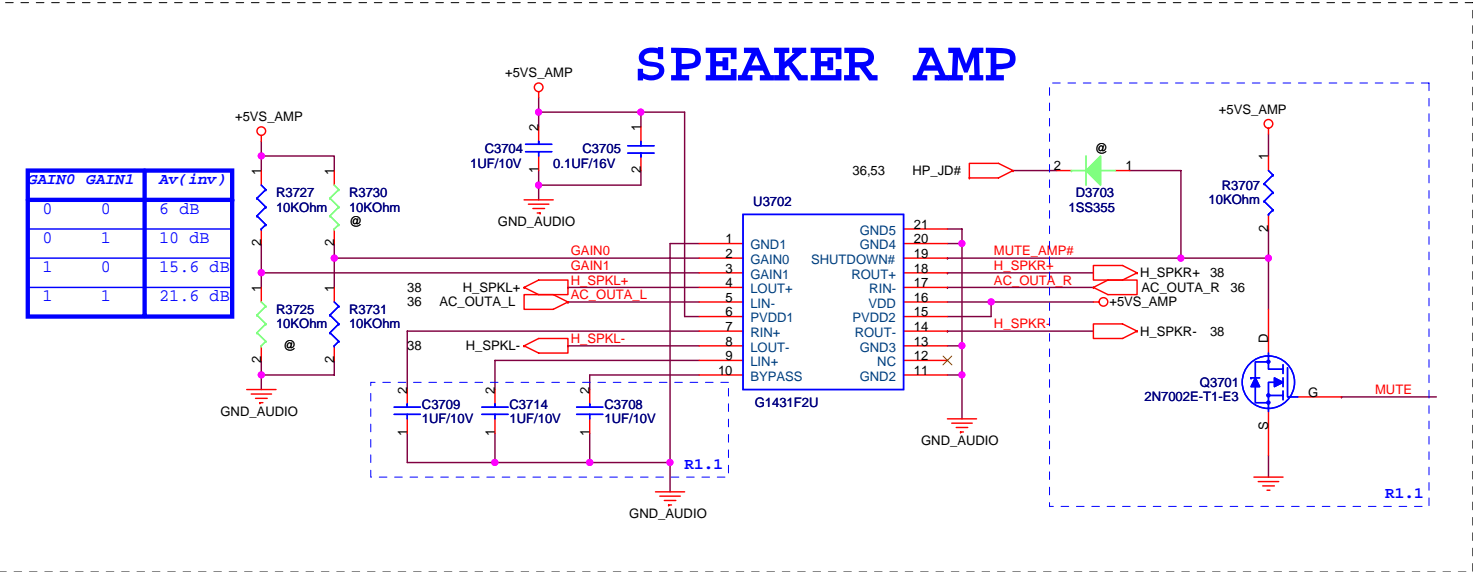
DePOP Circuit



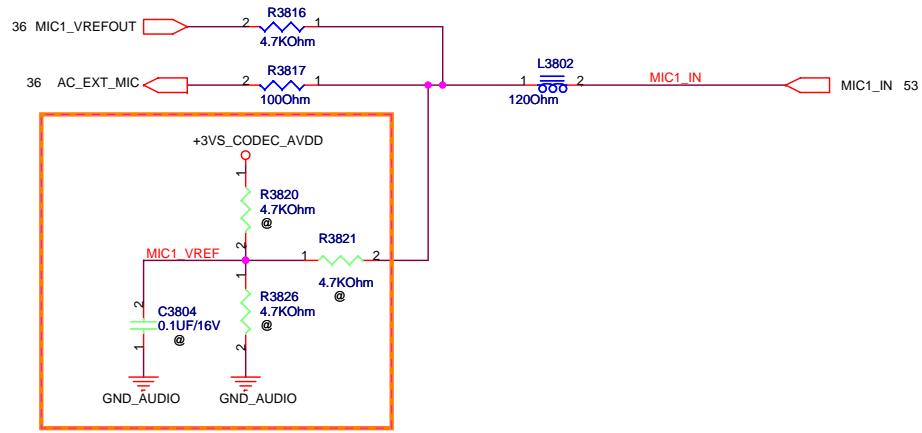
JACK GND



SPEAKER AMP

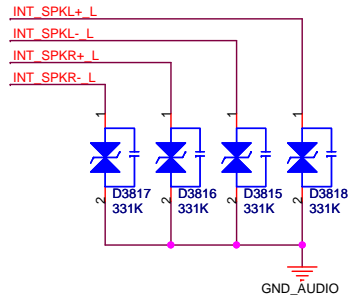
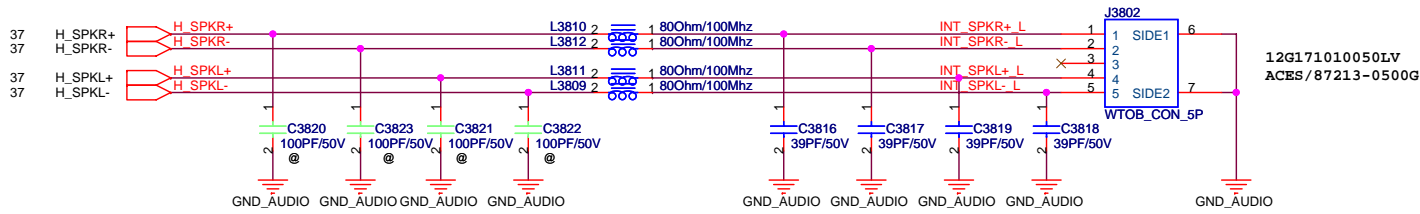


EXT MICROPHONE



Reserved the external MIC bias(T filter).

SPEAKER CONNECTOR



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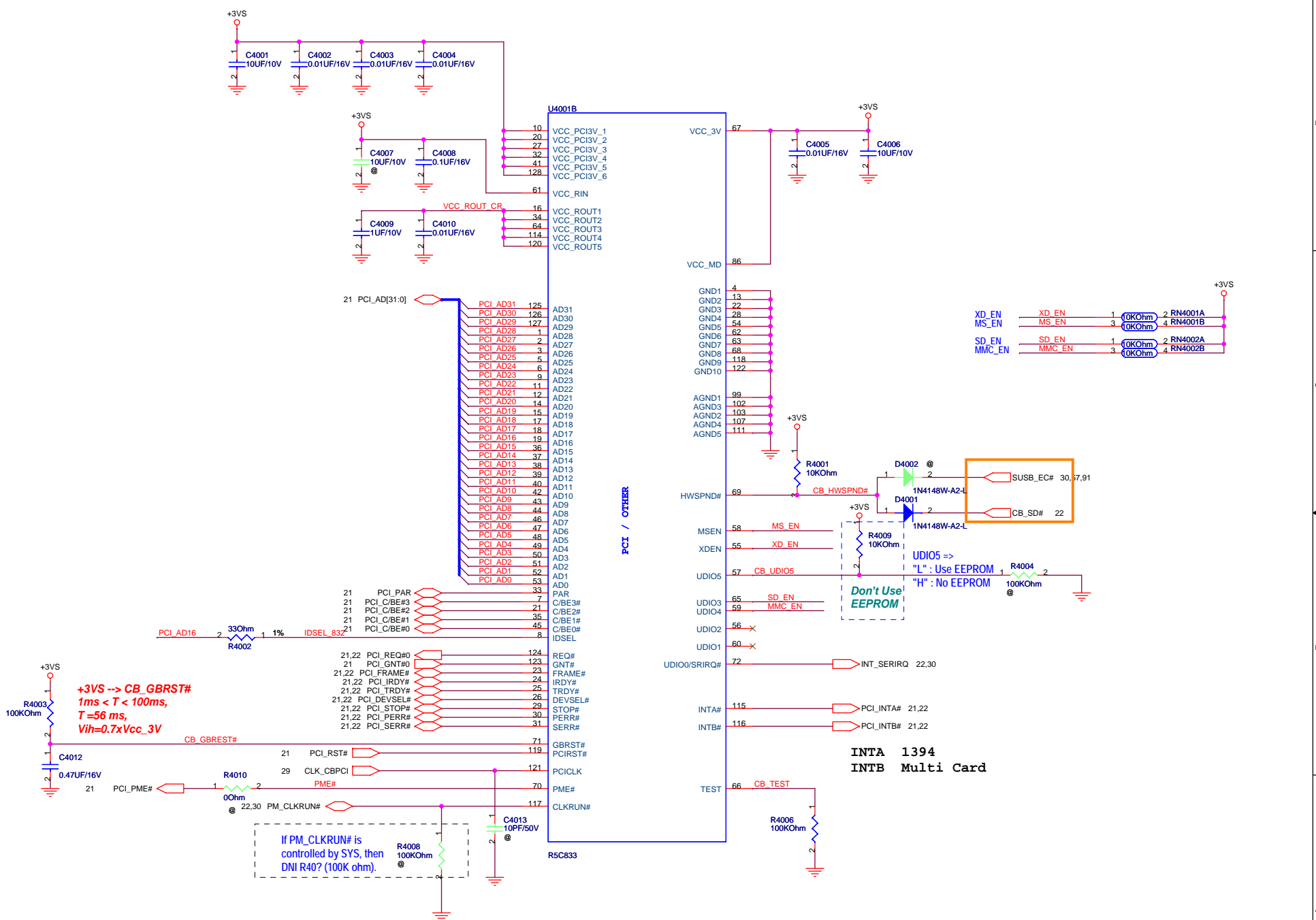
B

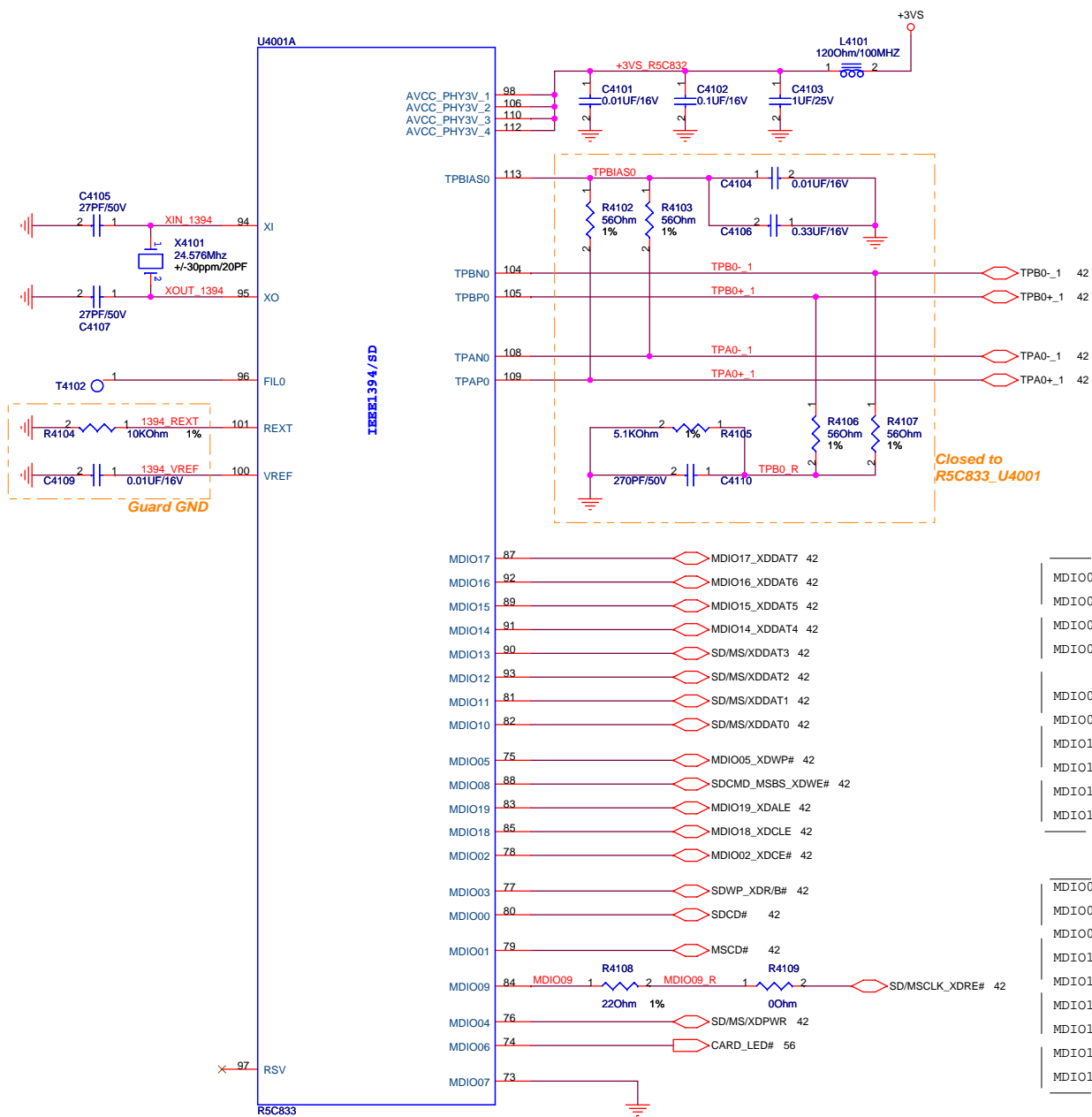
B

A

A

		Title : ***	
Engineer: <i>Peter Lo</i>			
Size Custom	Project Name Rocky30	Rev 1.2	
Date: Friday, March 14, 2008		Sheet 39	of 94





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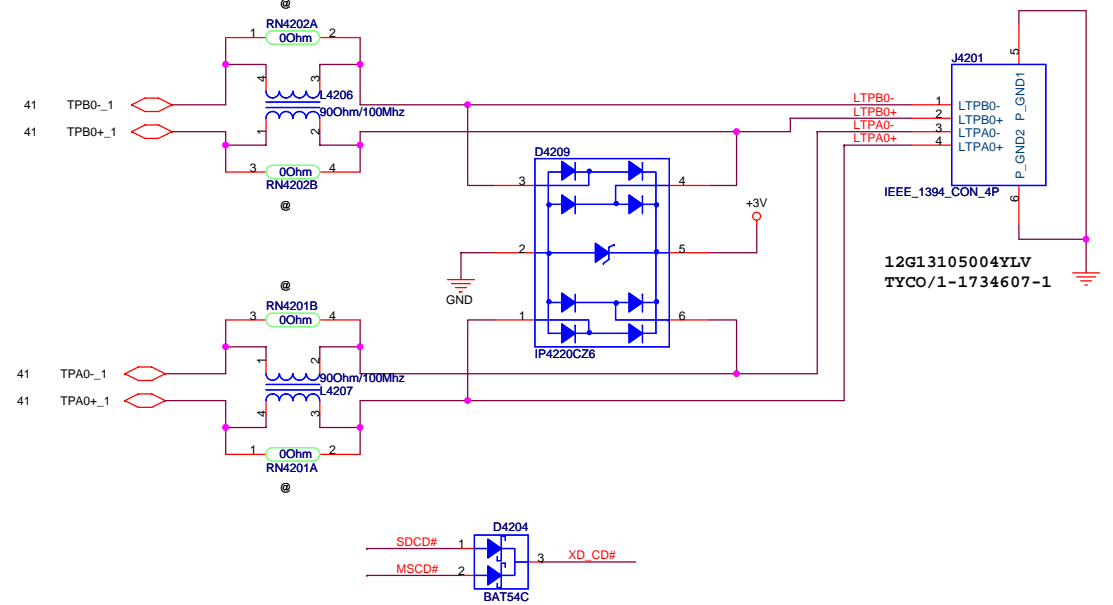
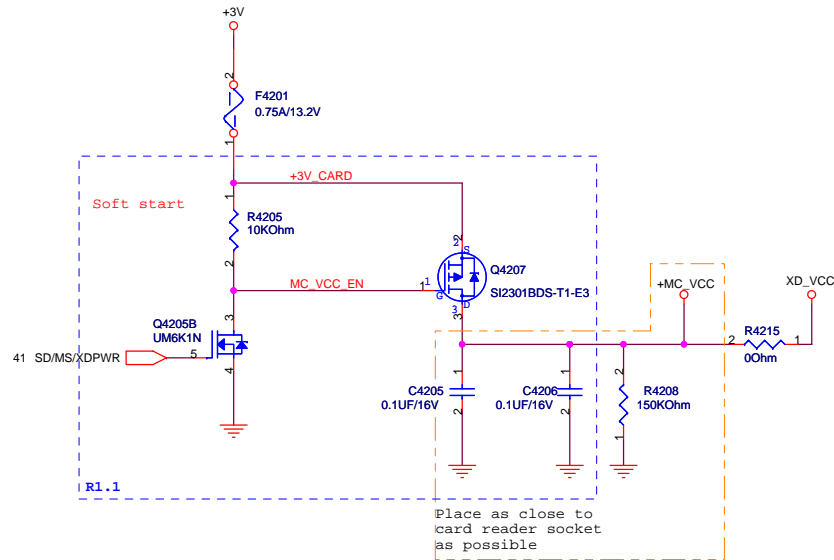
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
           MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

```

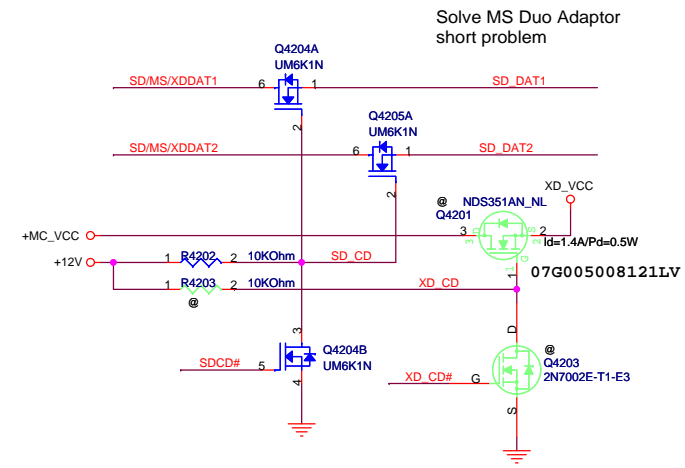
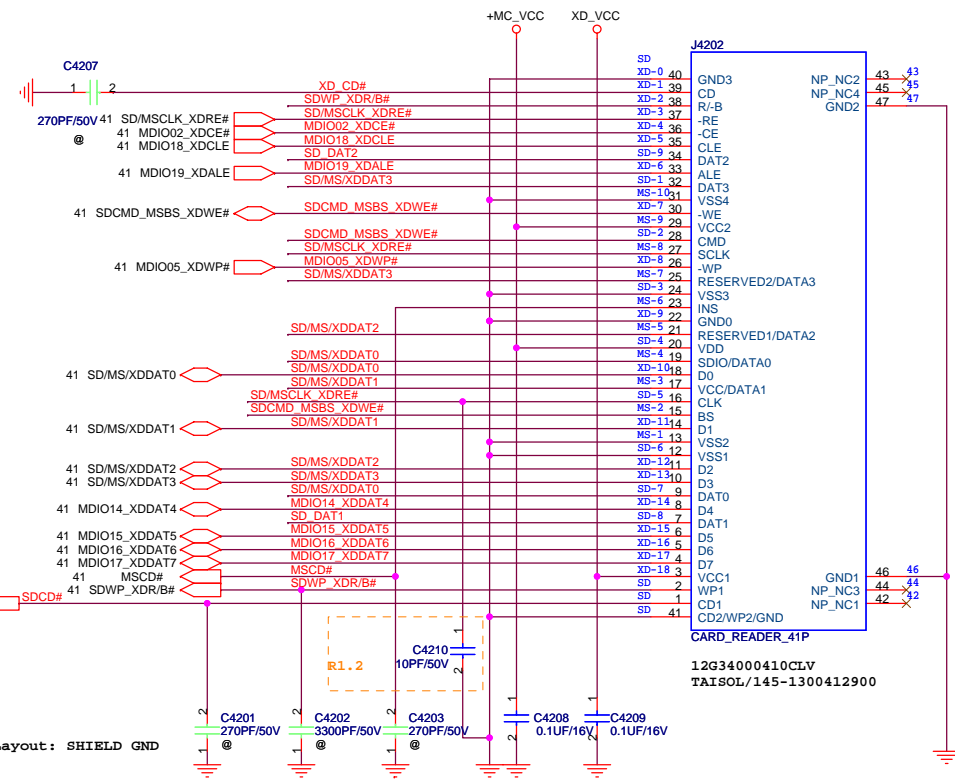
```

MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE

```



12G13105004YLV
TYCO/1-1734607-1



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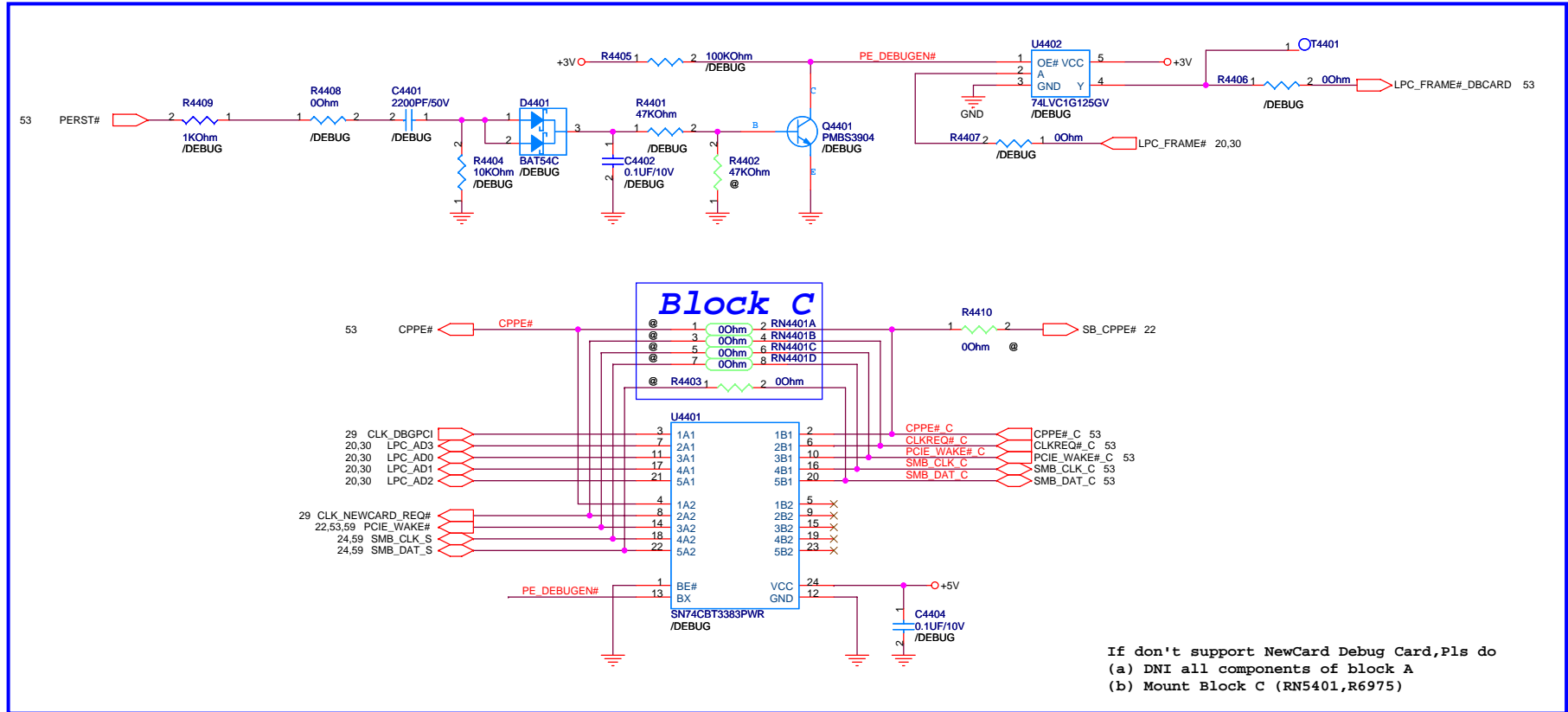


Title : ****

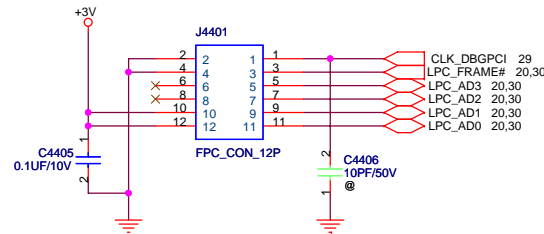
Engineer: *Peter Lo*

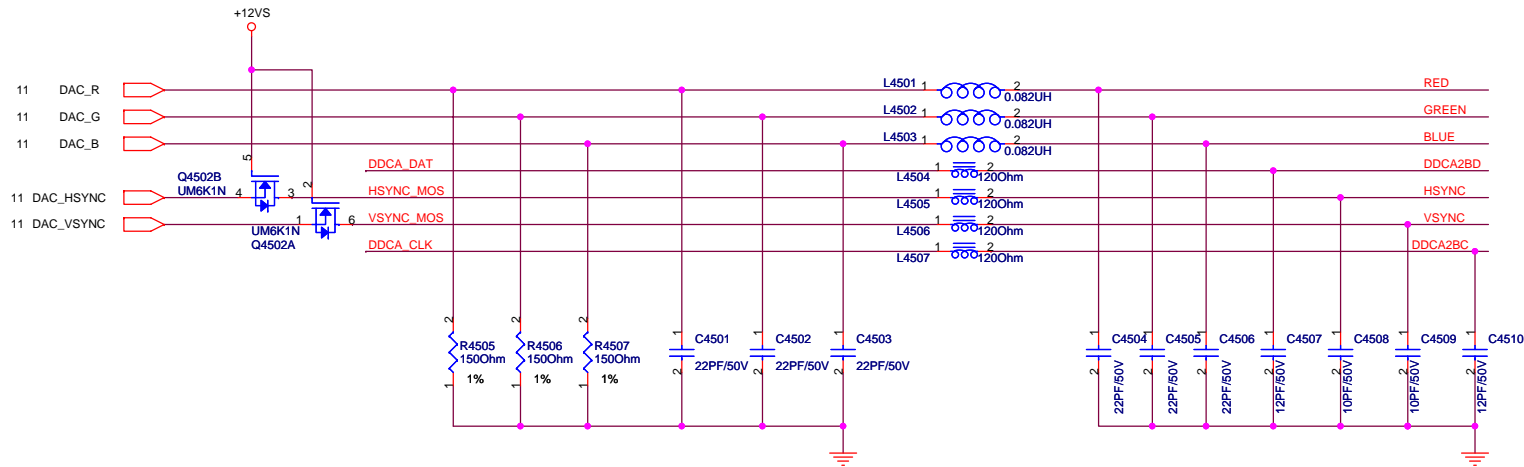
Size	Project Name	Rev
Custom	Rocky30	1.2
Date: Friday, March 14, 2008		Sheet 43 of 94

Block A

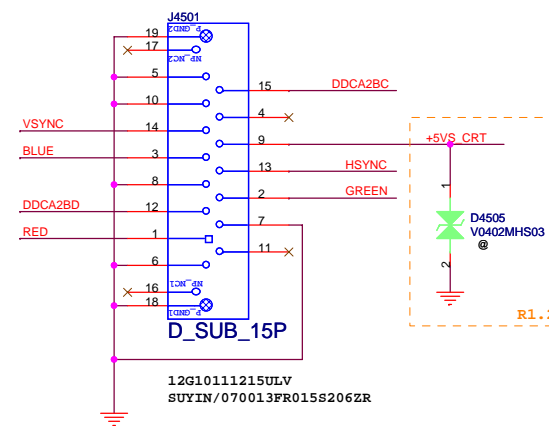
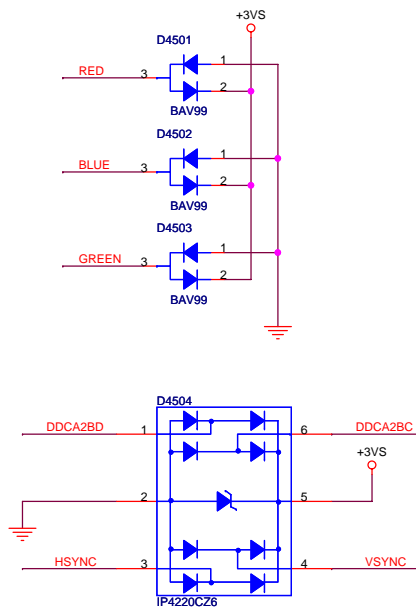
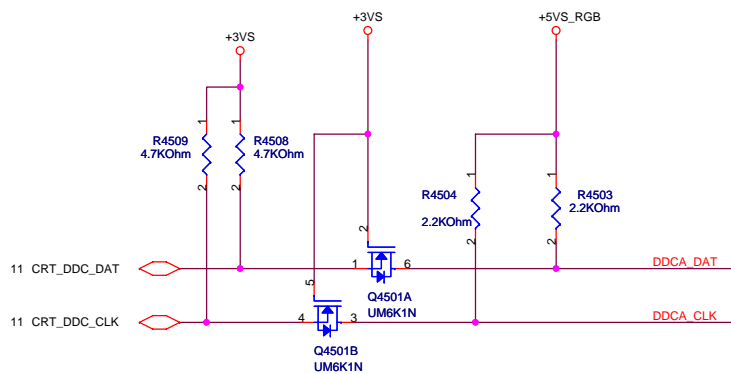


If don't support NewCard Debug Card,Pls do
 (a) DNI all components of block A
 (b) Mount Block C (RN5401,R6975)

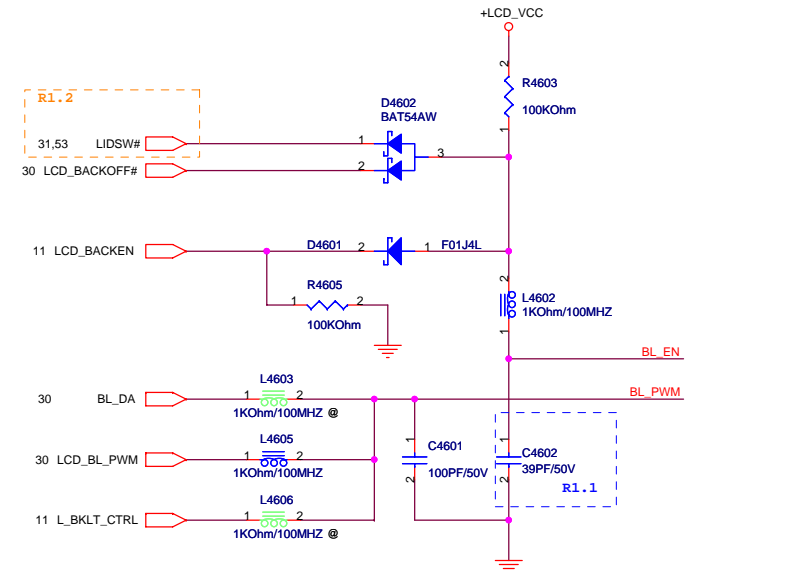
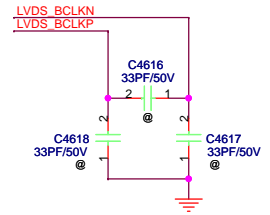
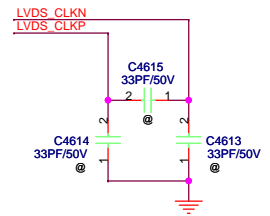
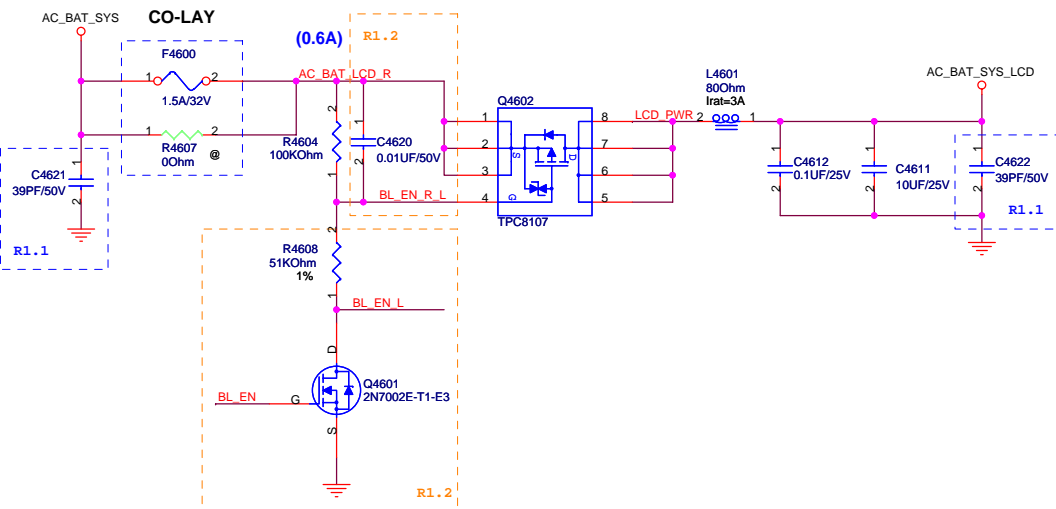
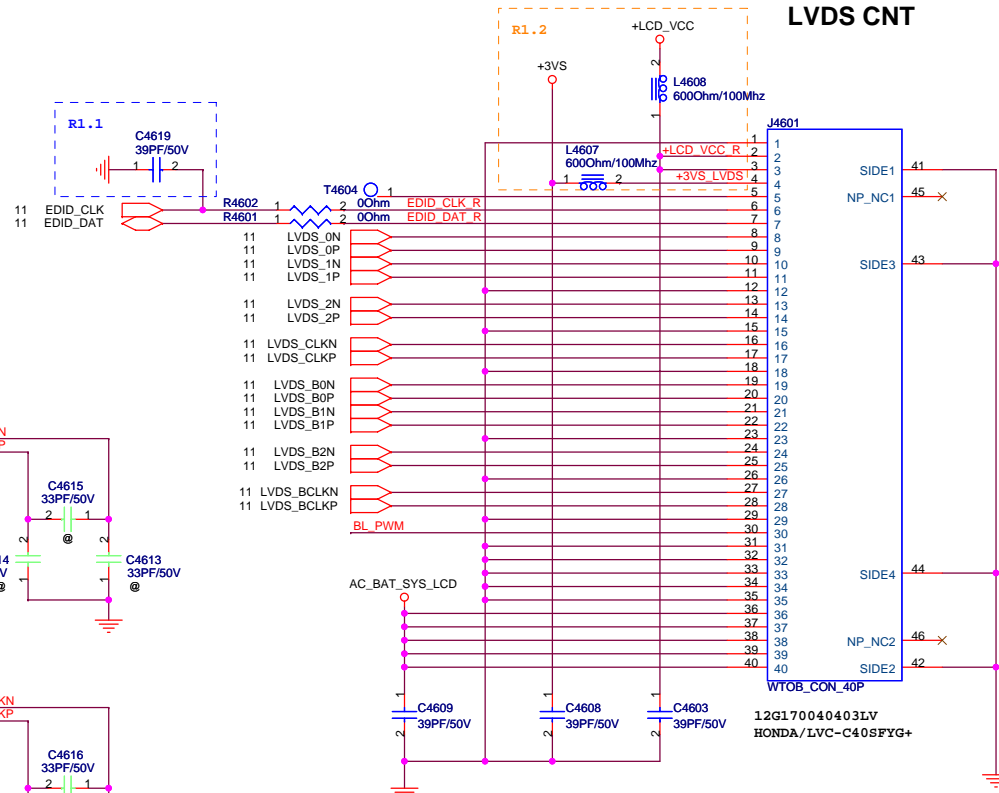




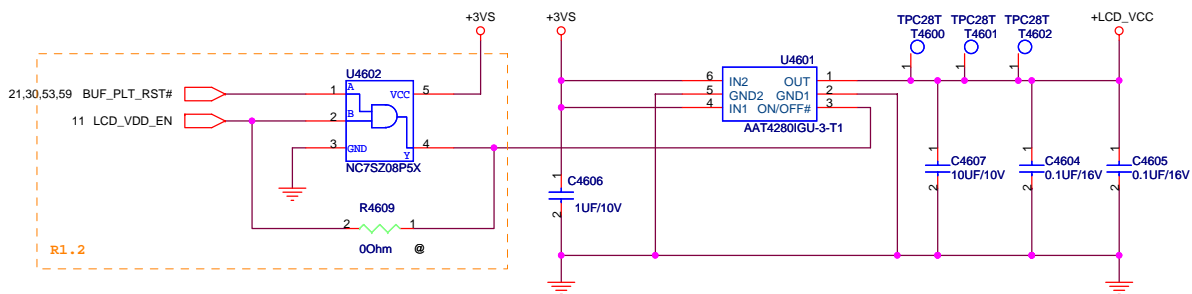
PLACE ESD Diodes near VGA port



LVDS CNT



Power Switch for LCD Power



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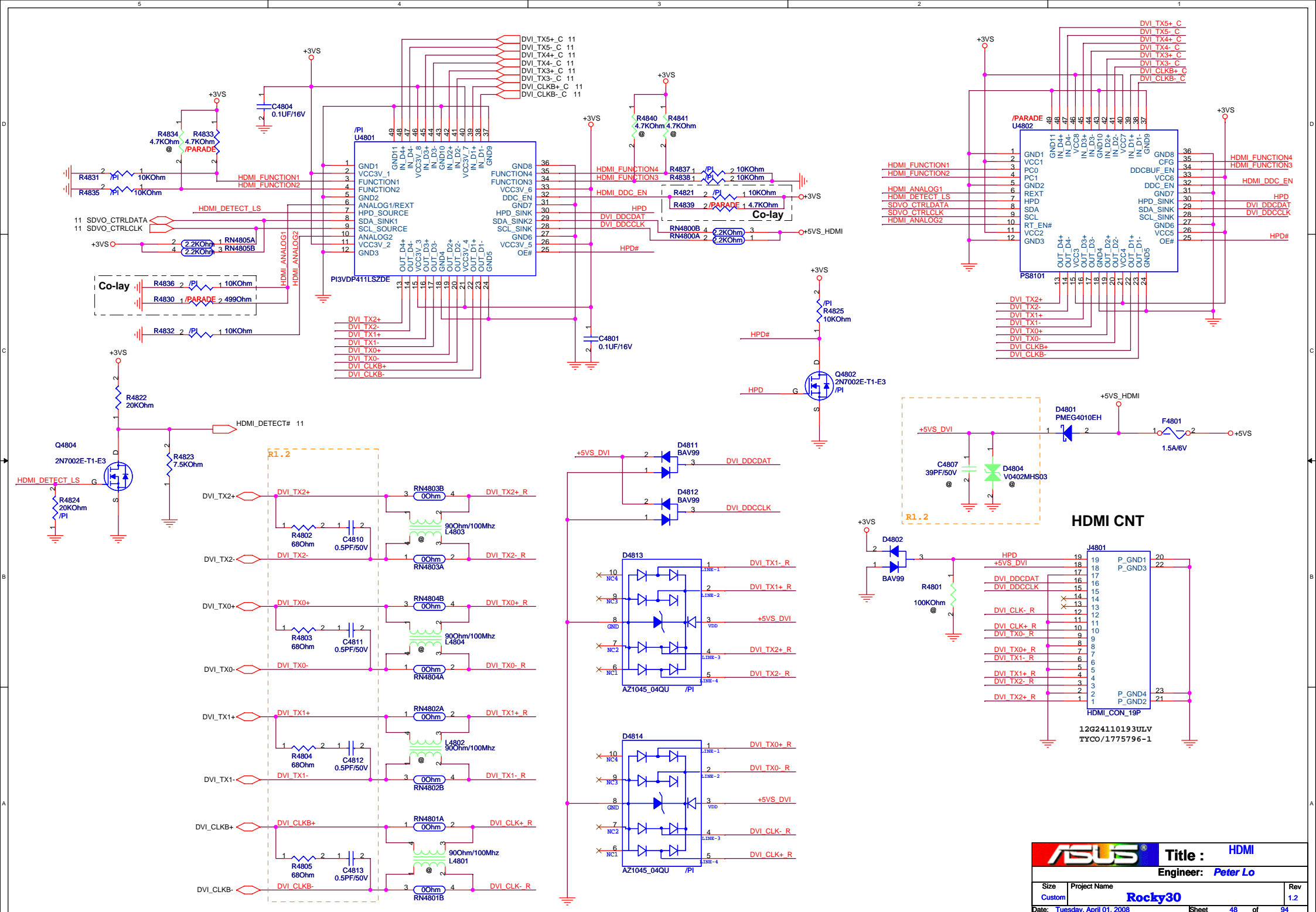
b

b

a

a

		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size	Project Name		Rev
C	Rocky30		1.2
Date: Friday, March 14, 2008		Sheet	47 of 84



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		Title :	
		Engineer: <i>Peter Lo</i>	
Size	Project Name	Rev	
A	Rocky30	1.2	
Date: <i>Friday, March 14, 2008</i>		Sheet	1 of 94

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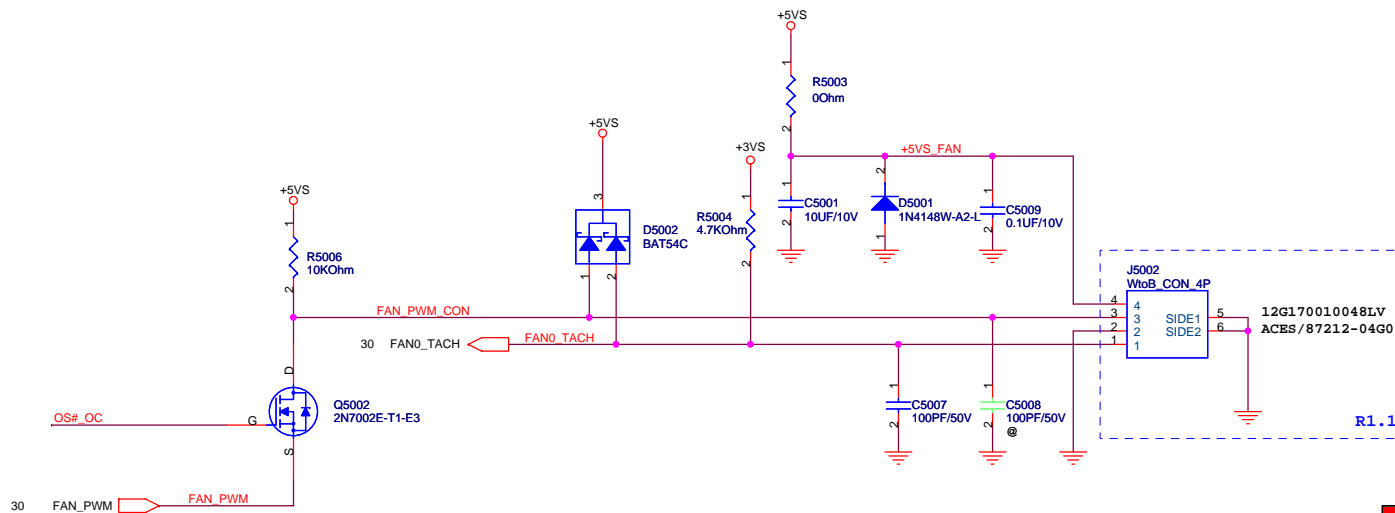
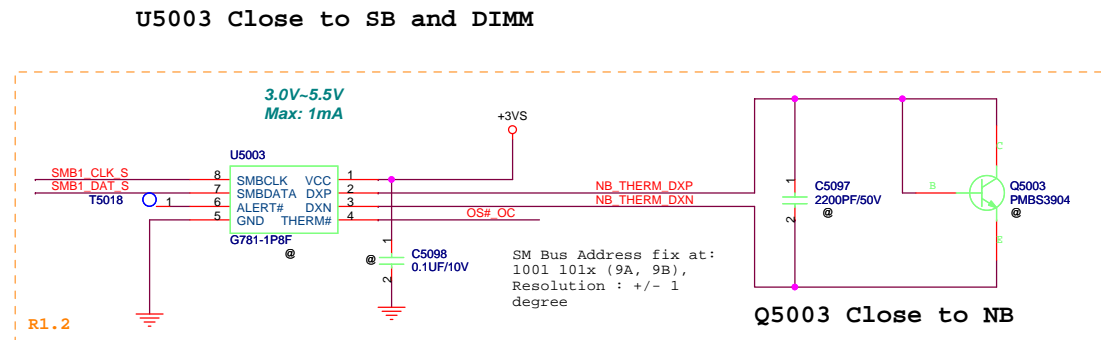
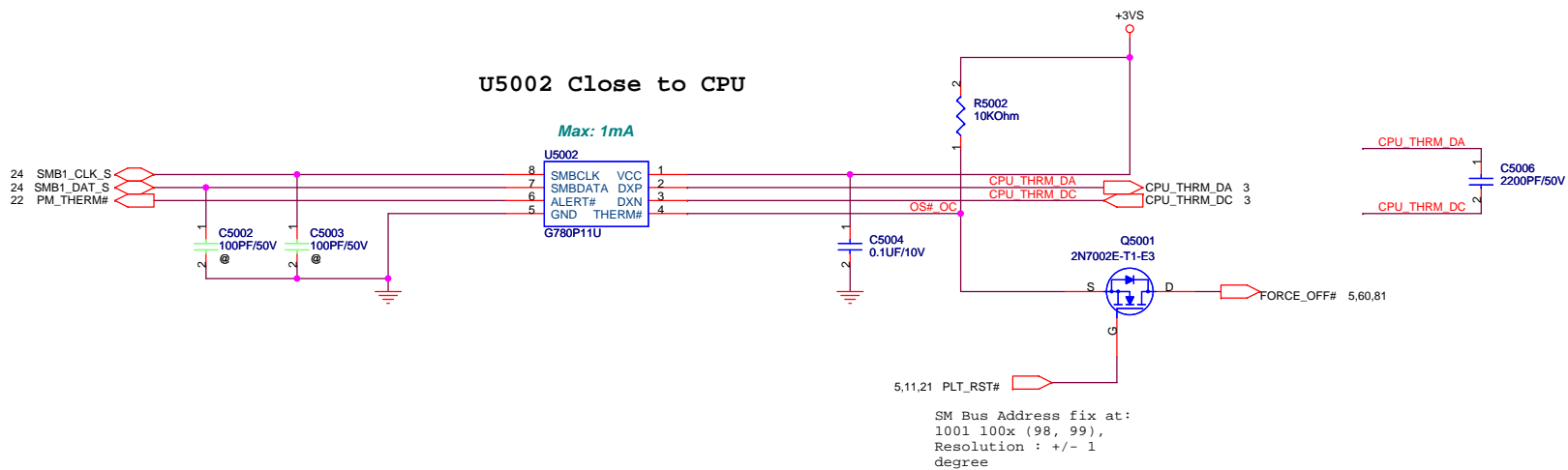
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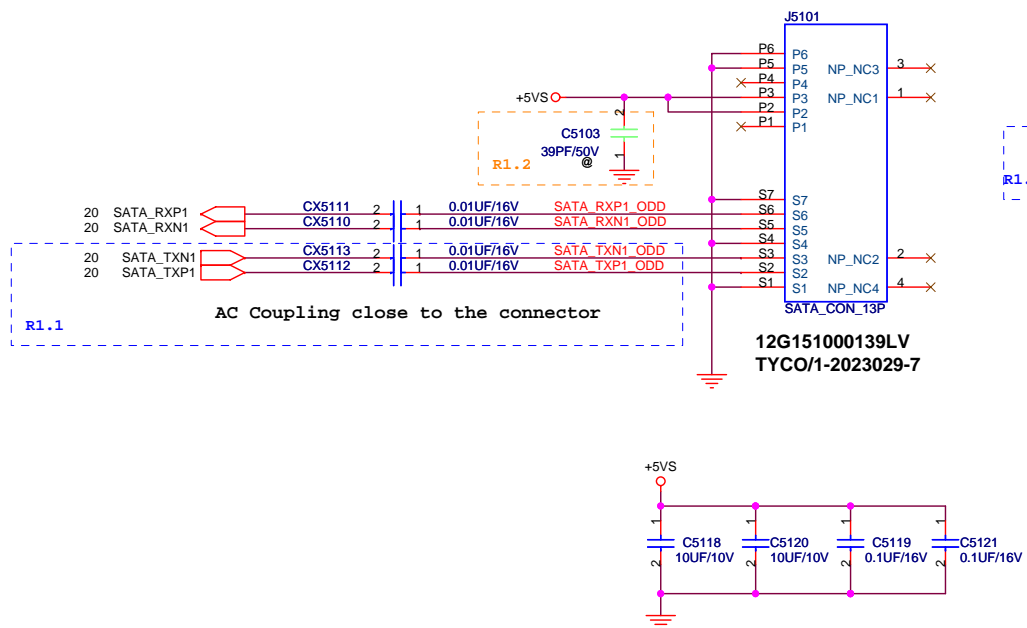
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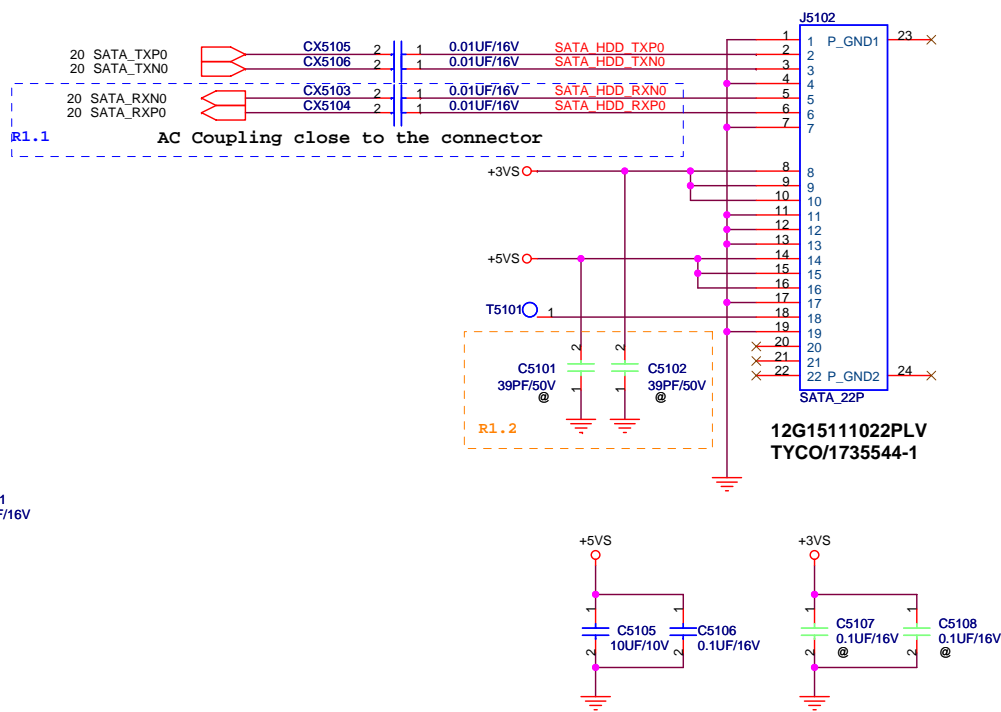
Thermal Sensor



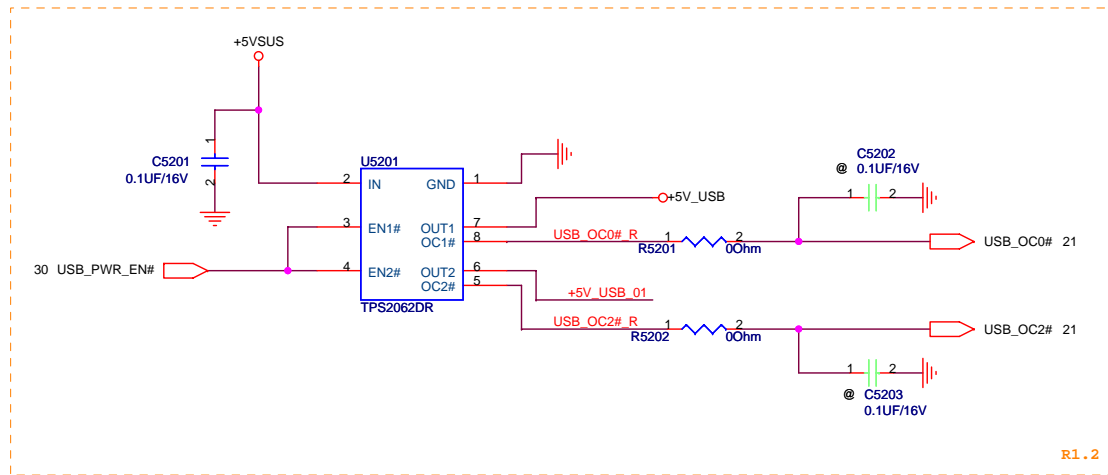
ODD CON



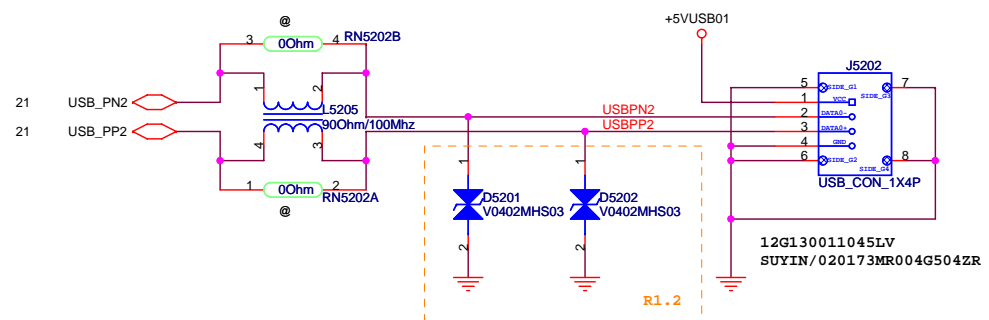
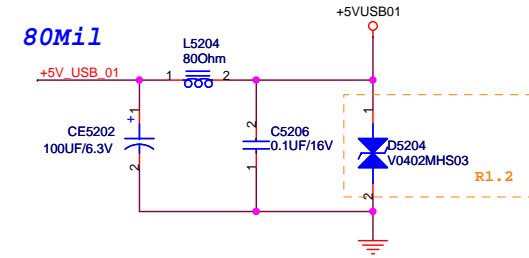
SATA HDD CON



PEGATRON Title Sata HDD & Swap Bay		
Engineer: Peter Lo		
Size B	Project Name Rocky30	Rev 1.2
Date: Tuesday, April 01, 2008 Sheet 51 of 94		

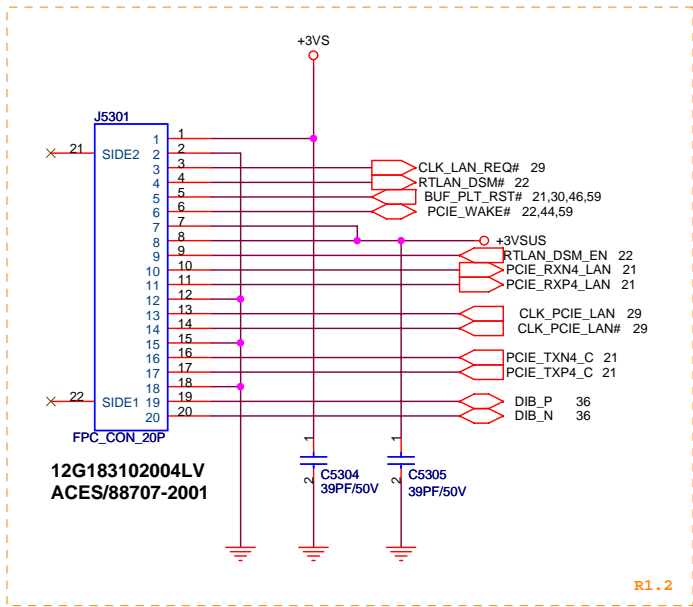


80mi1

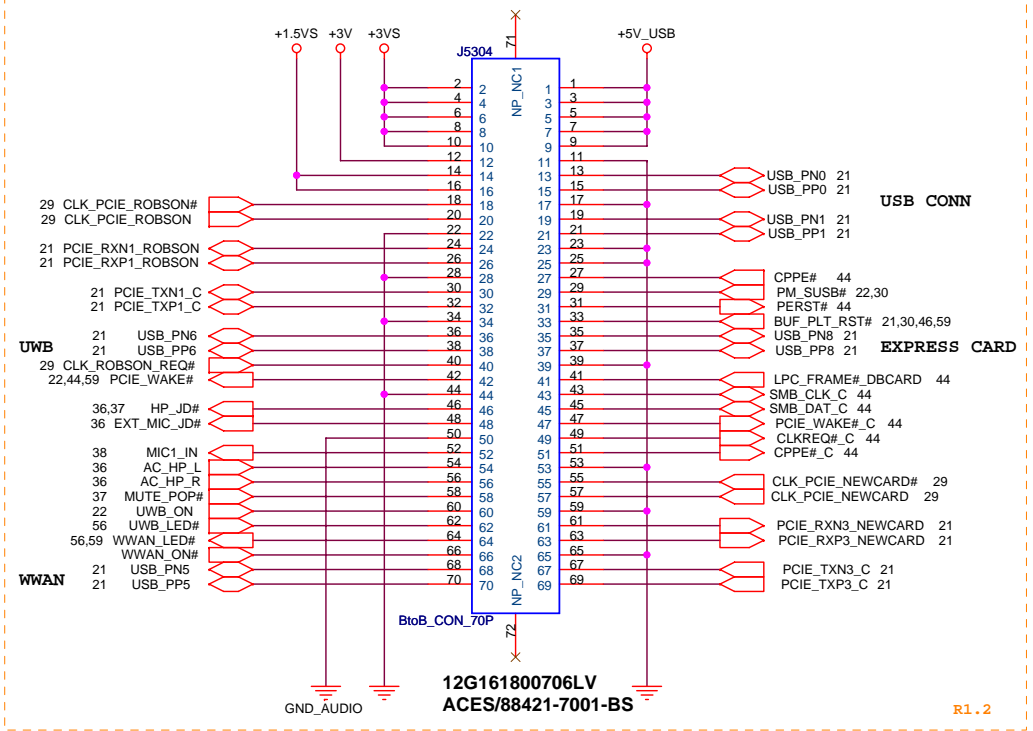


PEGATRON Title : USB CONN		
Engineer: Peter Lo		
Size B	Project Name Rocky30	Rev 1.2
Date: Tuesday, April 01, 2008 Sheet 52 of 94		

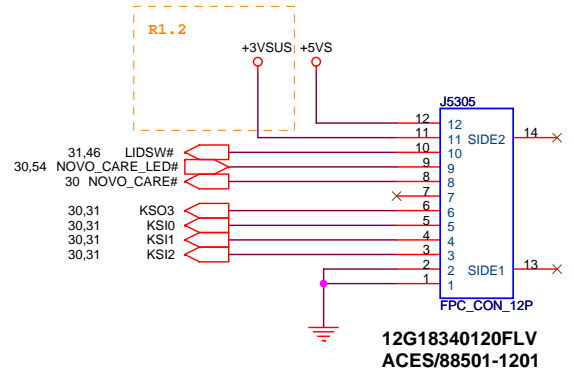
IO BOARD



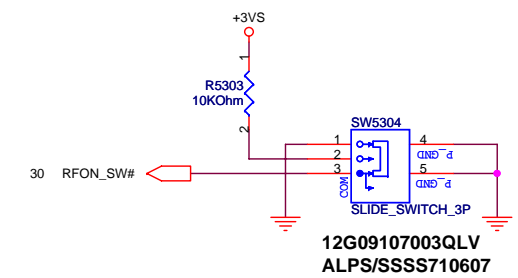
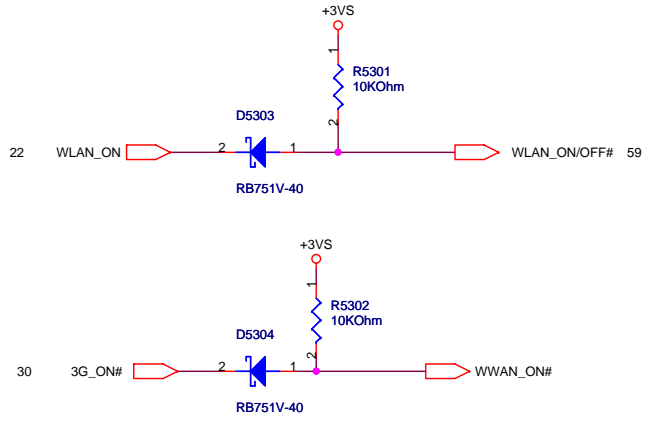
SMALL BOARD



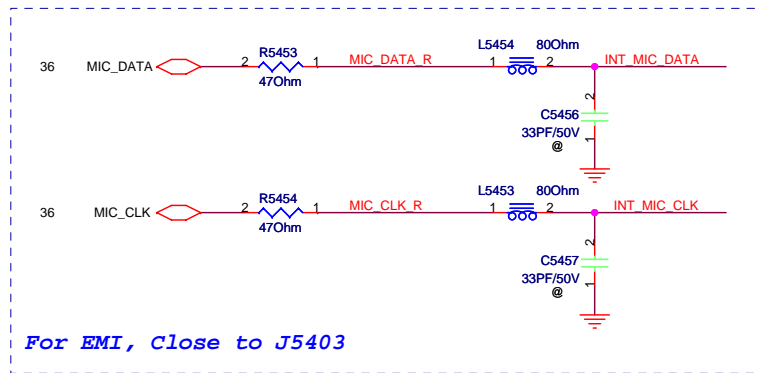
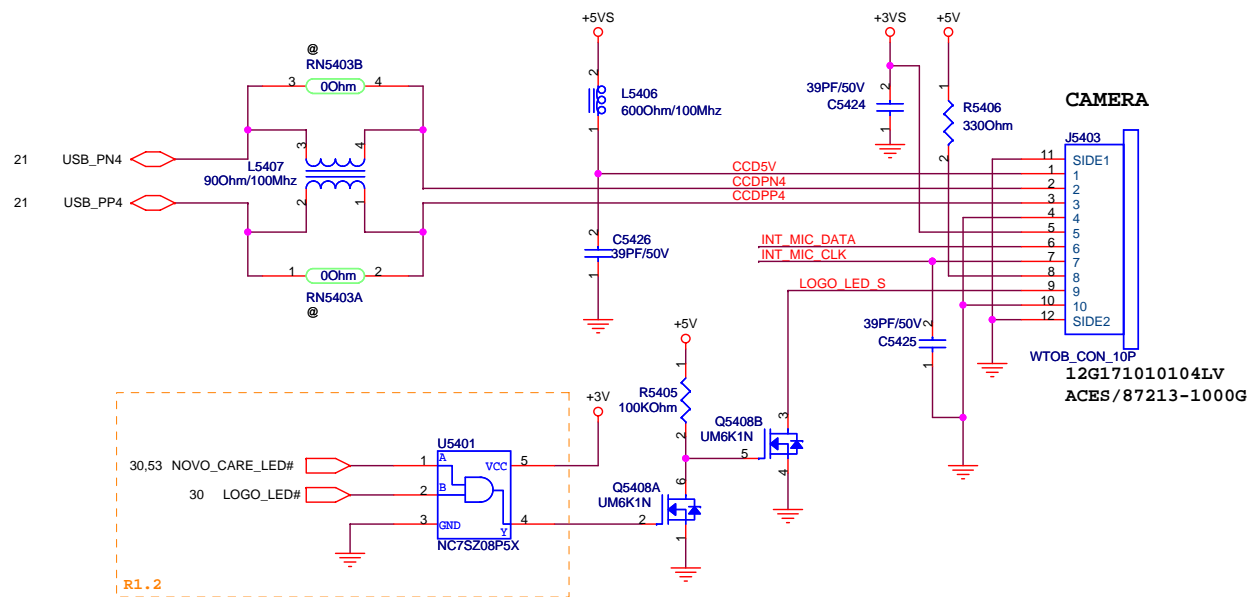
For Media Control Board



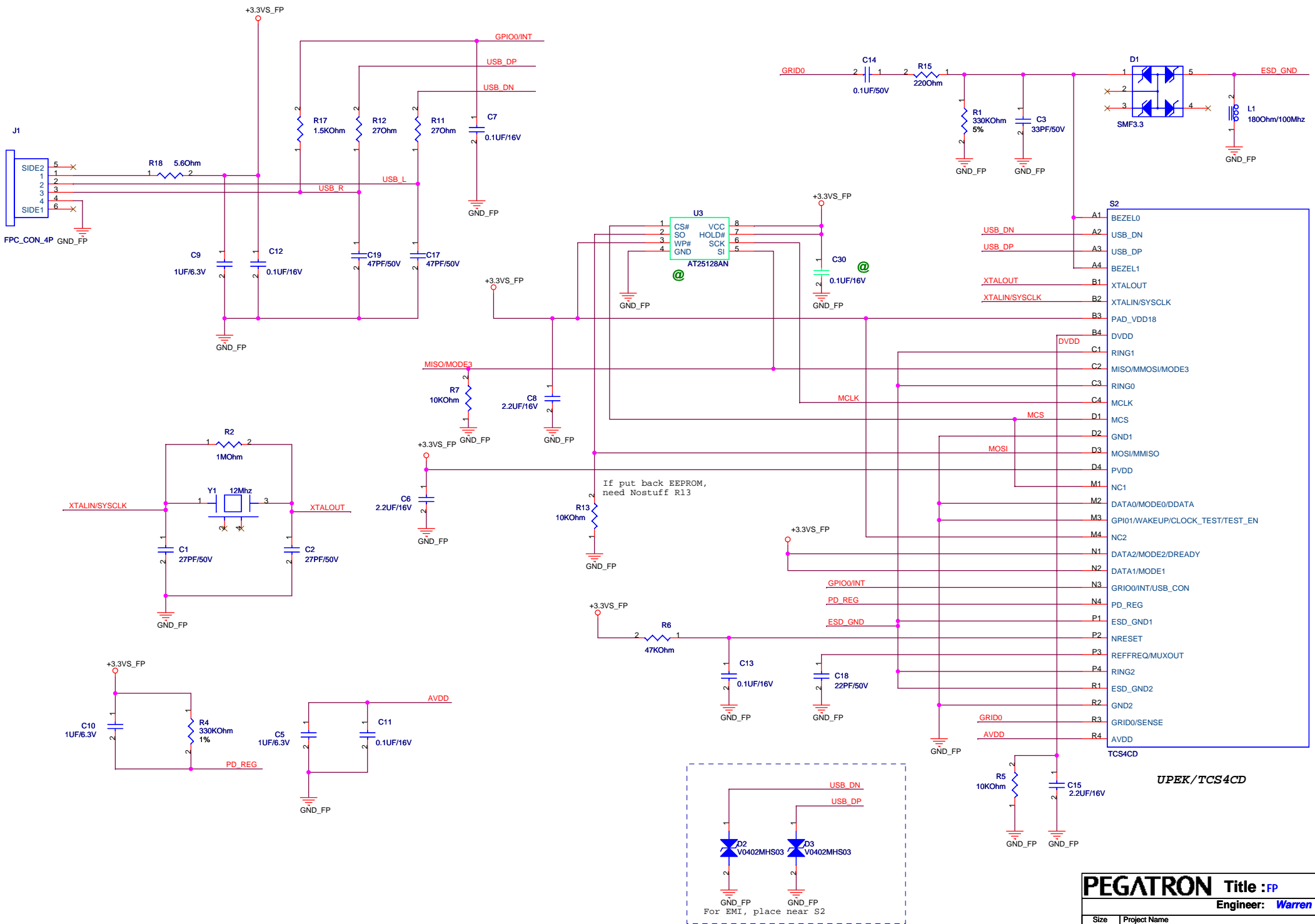
Wireless Switch



PEGATRON Title : IO BOARD		
Engineer: Peter Lo		
Size B	Project Name Rocky30	Rev 1.2
Date: Tuesday, April 01, 2008	Sheet 53 of 94	



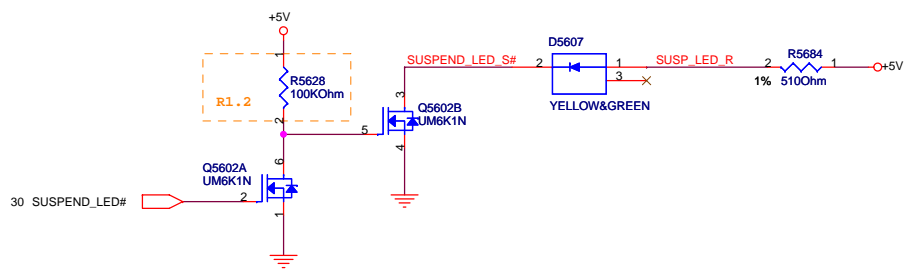
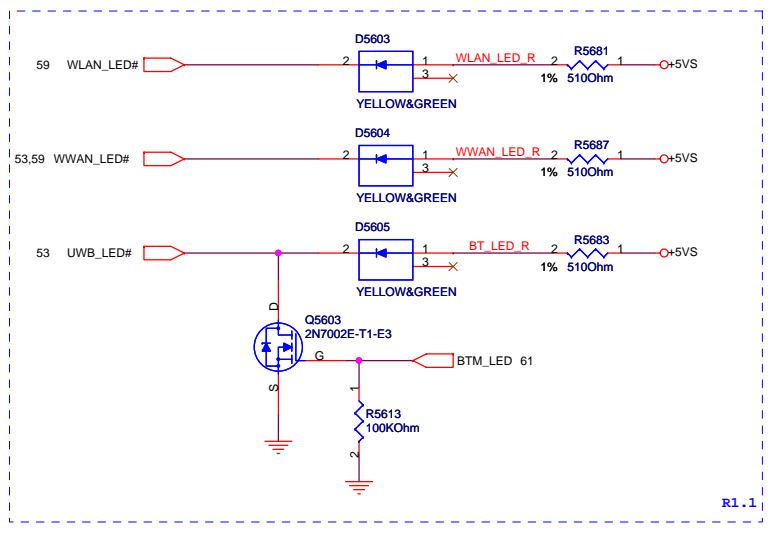
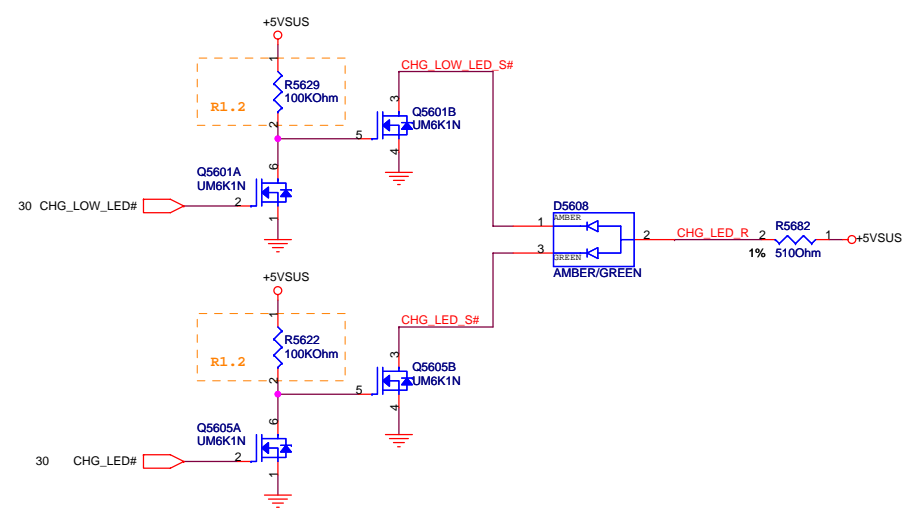
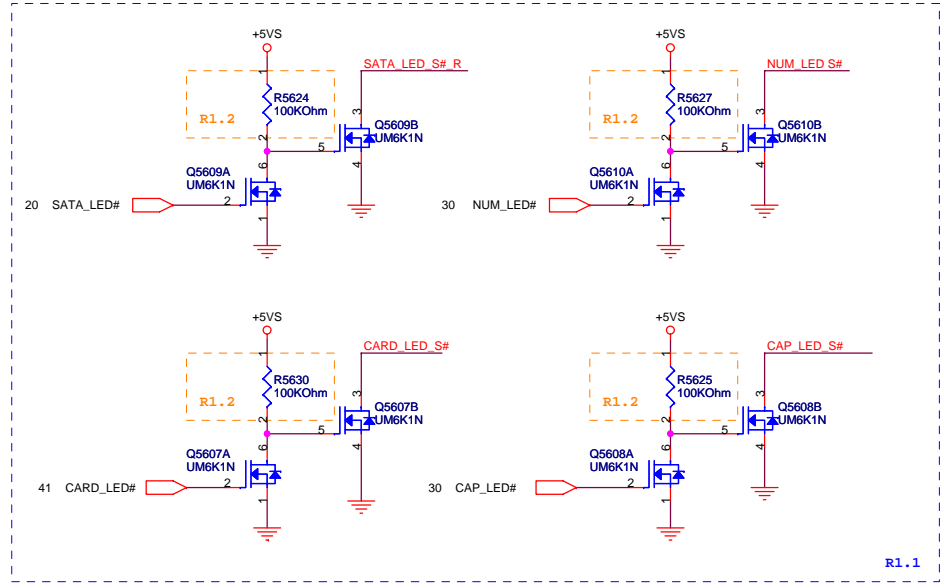
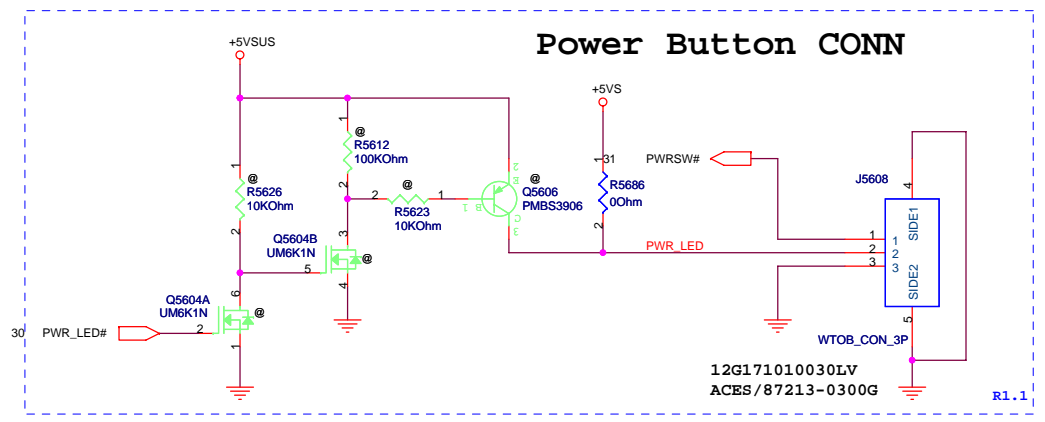
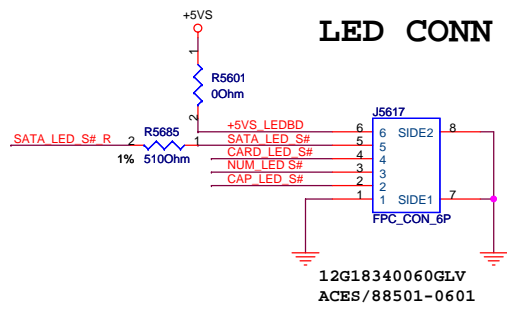
PEGATRON Title : CAMERA		
Engineer: Peter Lo		
Size	Project Name	Rev
B	Rocky30	1.2
Date: Tuesday, April 01, 2008		
Sheet 54 of 94		

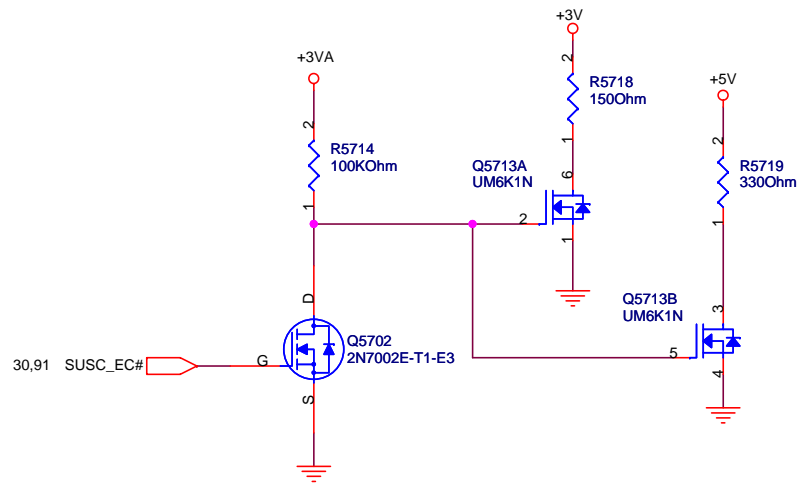
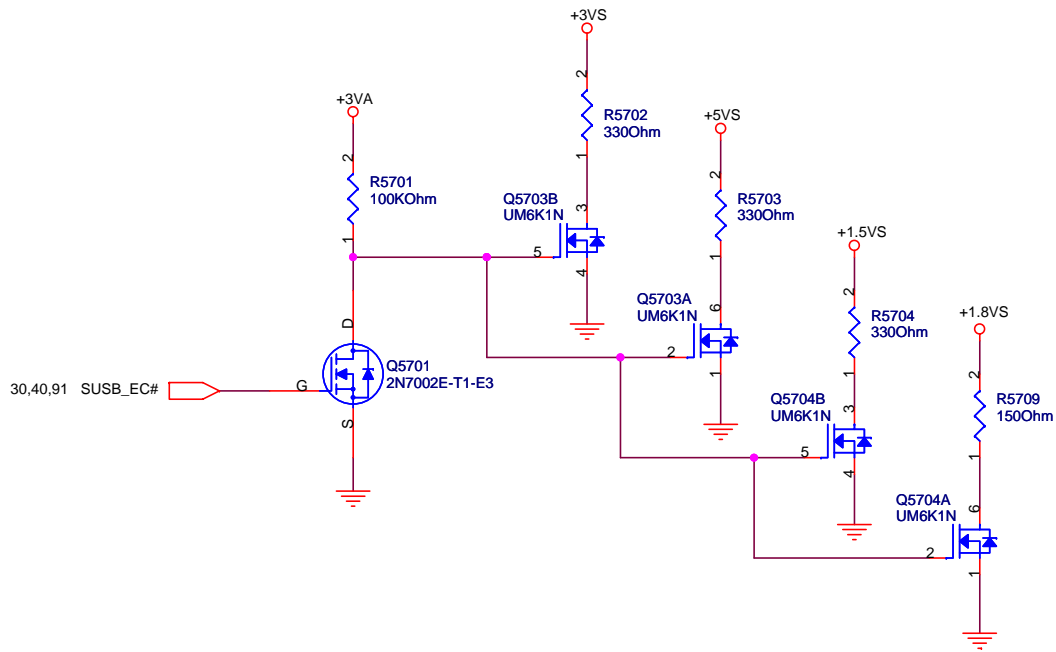


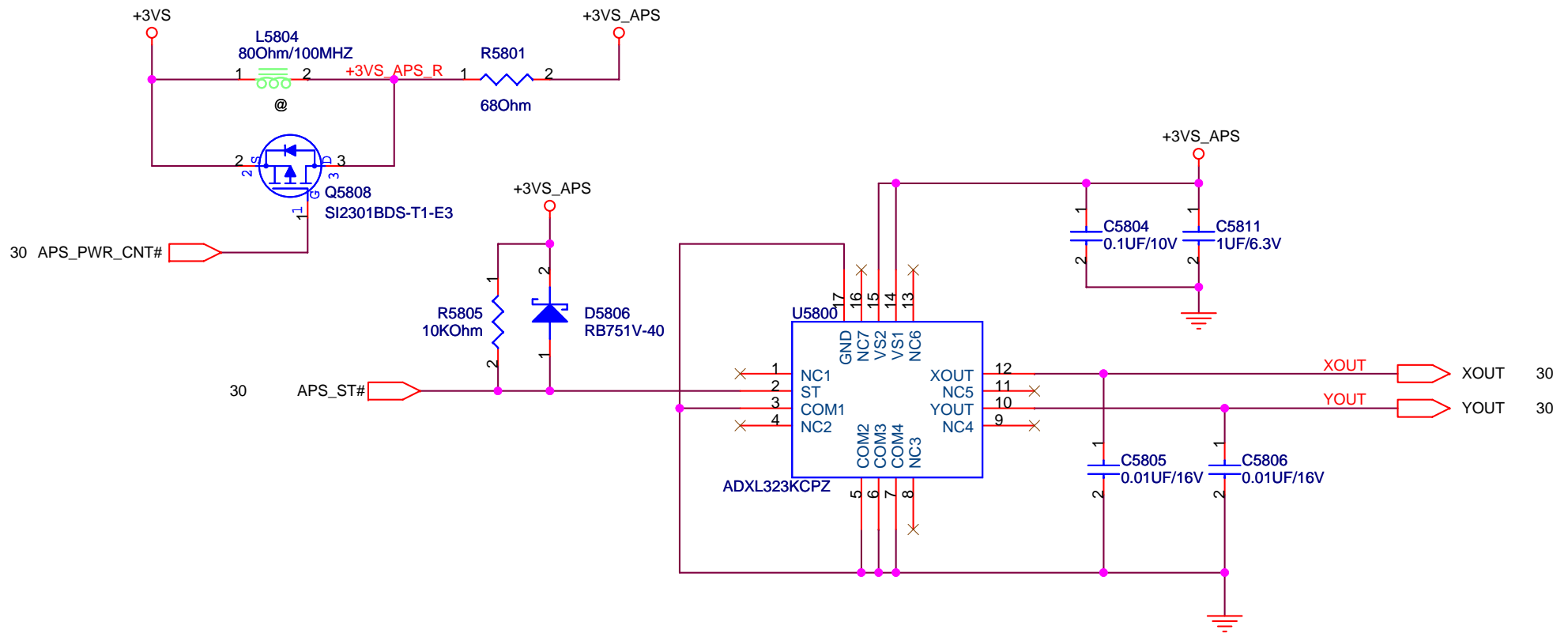
PEGATRON Title : **FP**

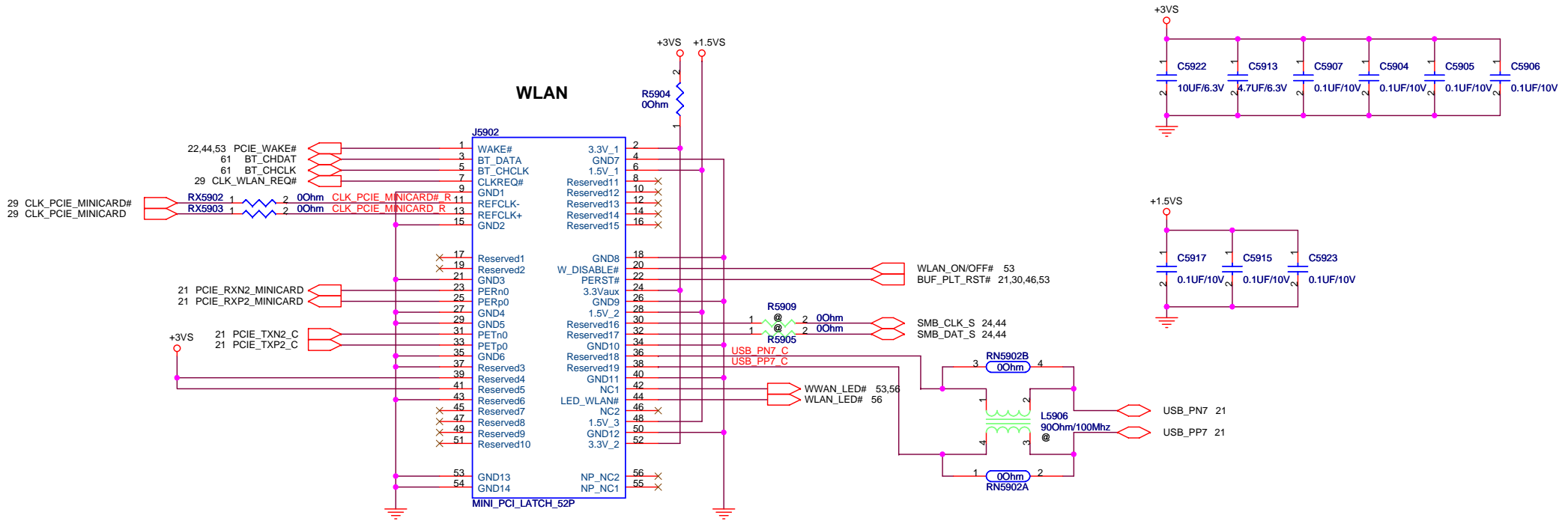
Engineer: **Warren**

Size	Project Name	Rev
Custom	Rocky 40/50	2.1
Date: Thursday, March 20, 2008	Sheet 55 of 94	



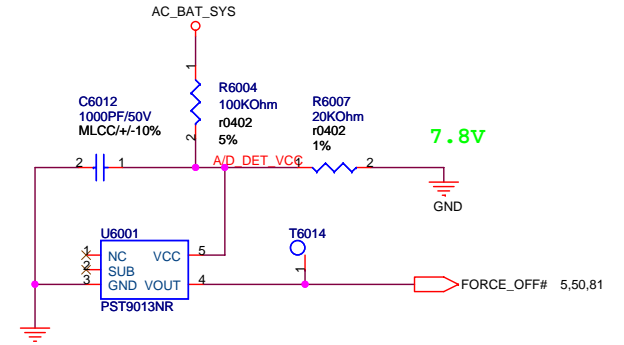
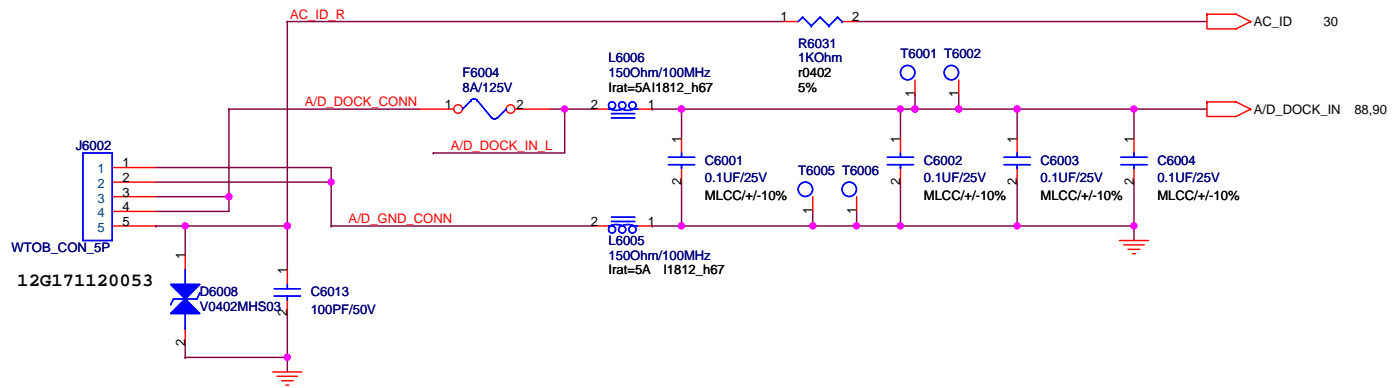






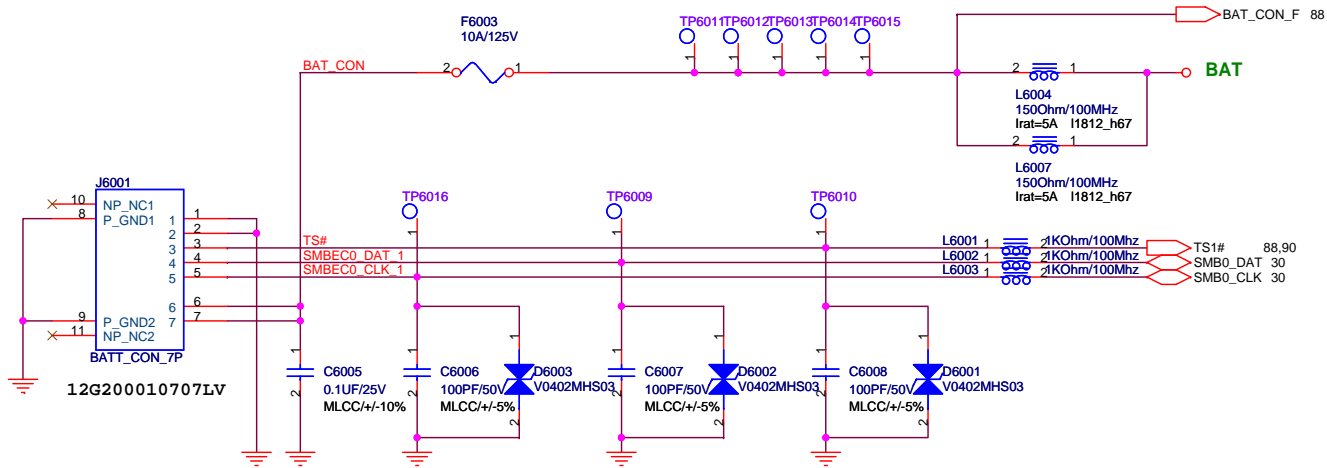
		Title : Mini Card
		Engineer: Peter Lo
Size B	Project Name Rocky30	Rev 1.2
Date: Tuesday, April 01, 2008	Sheet 59	of 94

DC IN CONN

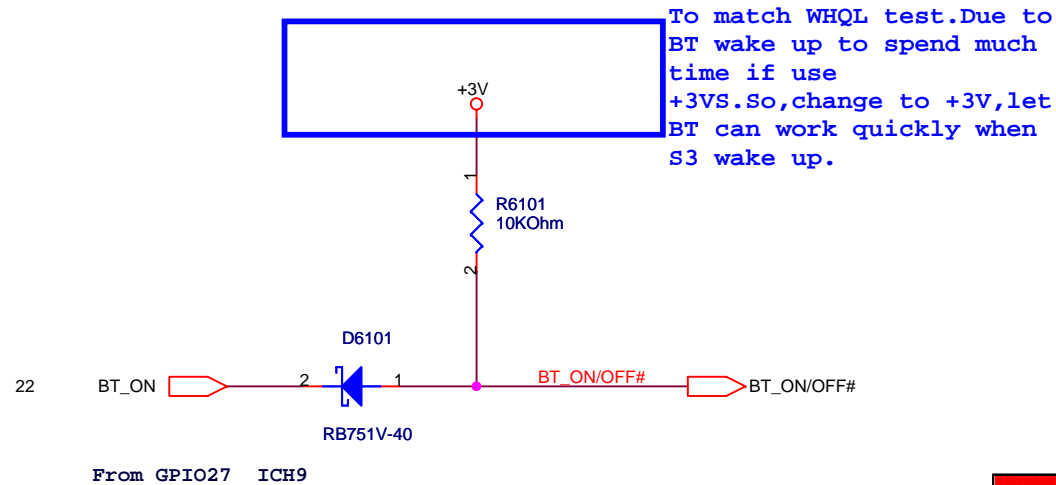
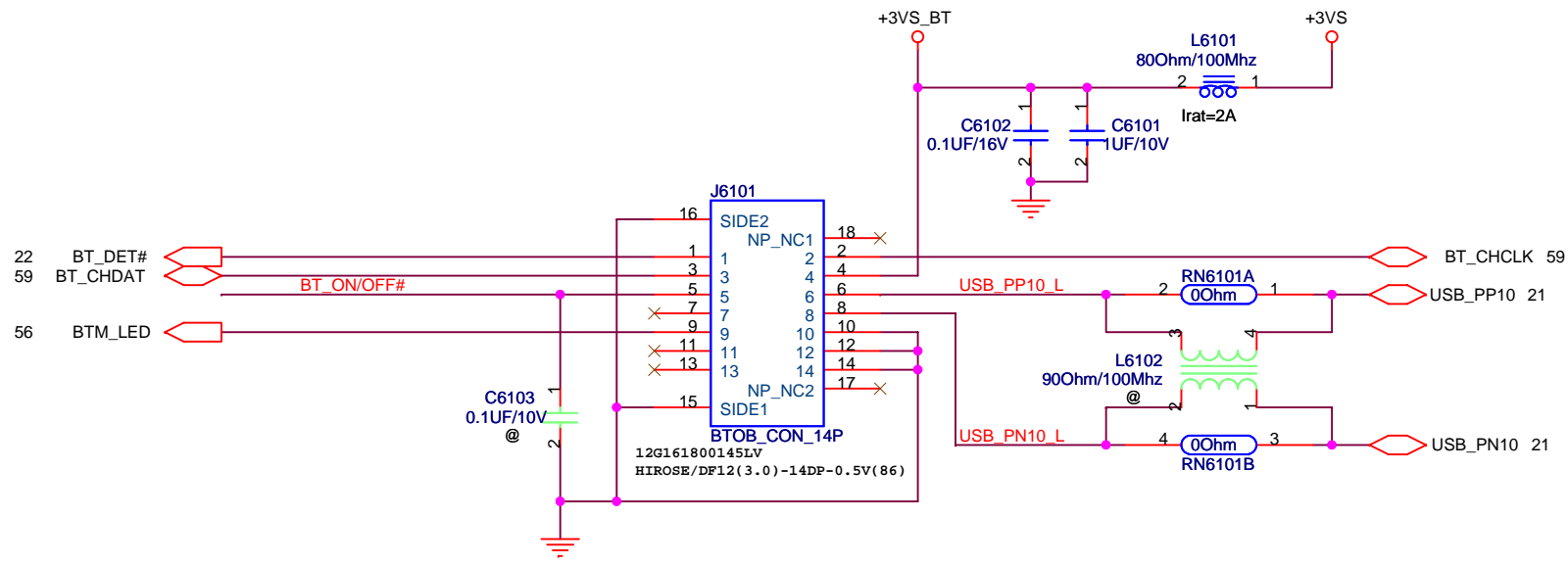


Without Battery & Pull out Adapter

Battery CONN



Blue Tooth



From GPIO27 ICH9

		Title : BlueTooth	
Engineer: <i>Peter Lo</i>			
Size	Project Name		Rev
A4	Rocky30		1.2
Date: Tuesday, April 01, 2008		Sheet	61 of 94

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		Title : ***
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Engineer: *Peter Lo*

Size A4	Project Name Rocky30	Rev 1.2
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		Title : ***	
Engineer: <i>Peter Lo</i>			
Size	Project Name		Rev
A4	Rocky30		1.2
Date: <u>Friday, March 14, 2008</u>		Sheet	63 of 94

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		Title :	
Engineer: <i>Peter Lo</i>			
Size	Project Name	Rev	
A	Rocky30	1.2	
Date: Friday, March 14, 2008		Sheet	64 of 94

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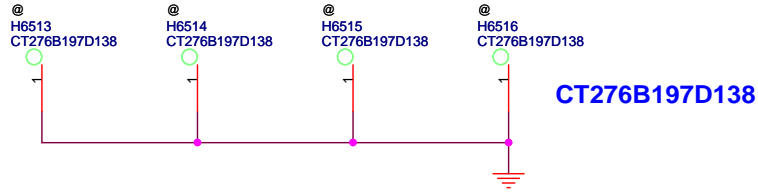
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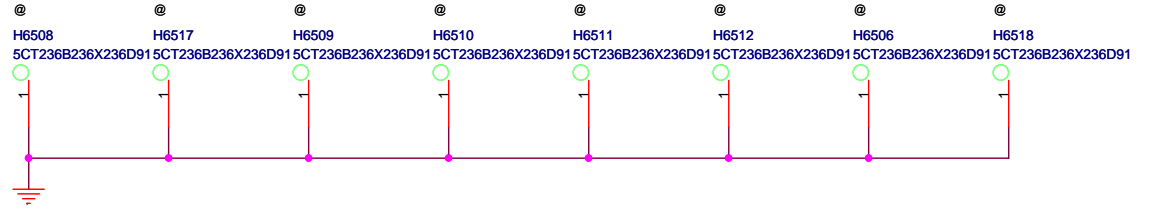
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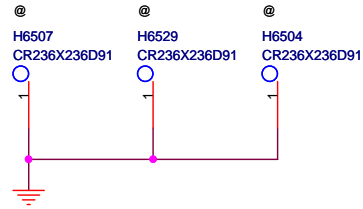
CPU



TOP 5CT236B236X236D91 PTH



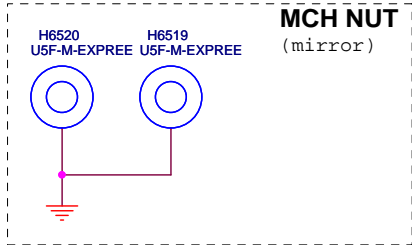
CR236X236D91 PTH



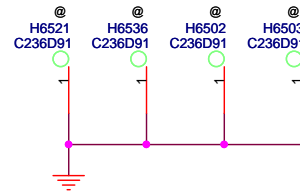
BOT 5CT236B236X236D91 PTH



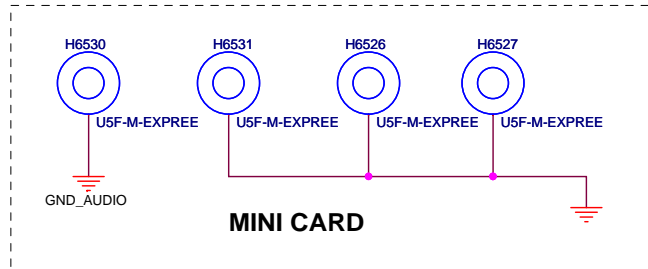
MCH NUT



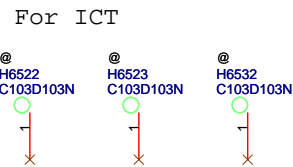
C236D91 PTH



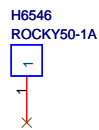
MINI CARD



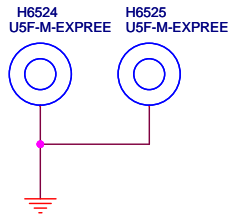
TOOLING HOLE



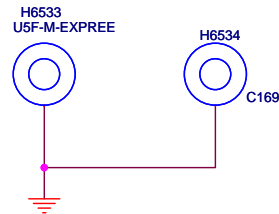
For BT StandOff



For Fan Stand Off
C236B189D150 PTH (mirror)



For KB Stand Off
C236B189D150 PTH



		Title MDC NUT & Hinksink NUT
		Engineer: Peter Lo
Size Custom	Project Name Rocky30	Rev 1.2
Date: Friday, March 28, 2008	Sheet 65	of 94

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		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size	Project Name		Rev
Custom	Rocky30		1.2
Date: Friday, March 14, 2008		Sheet	66 of 94



		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size Custom	Project Name Rocky30	Date: <u>Friday, March 14, 2008</u>	Rev 1.2
		Sheet 67 of 94	

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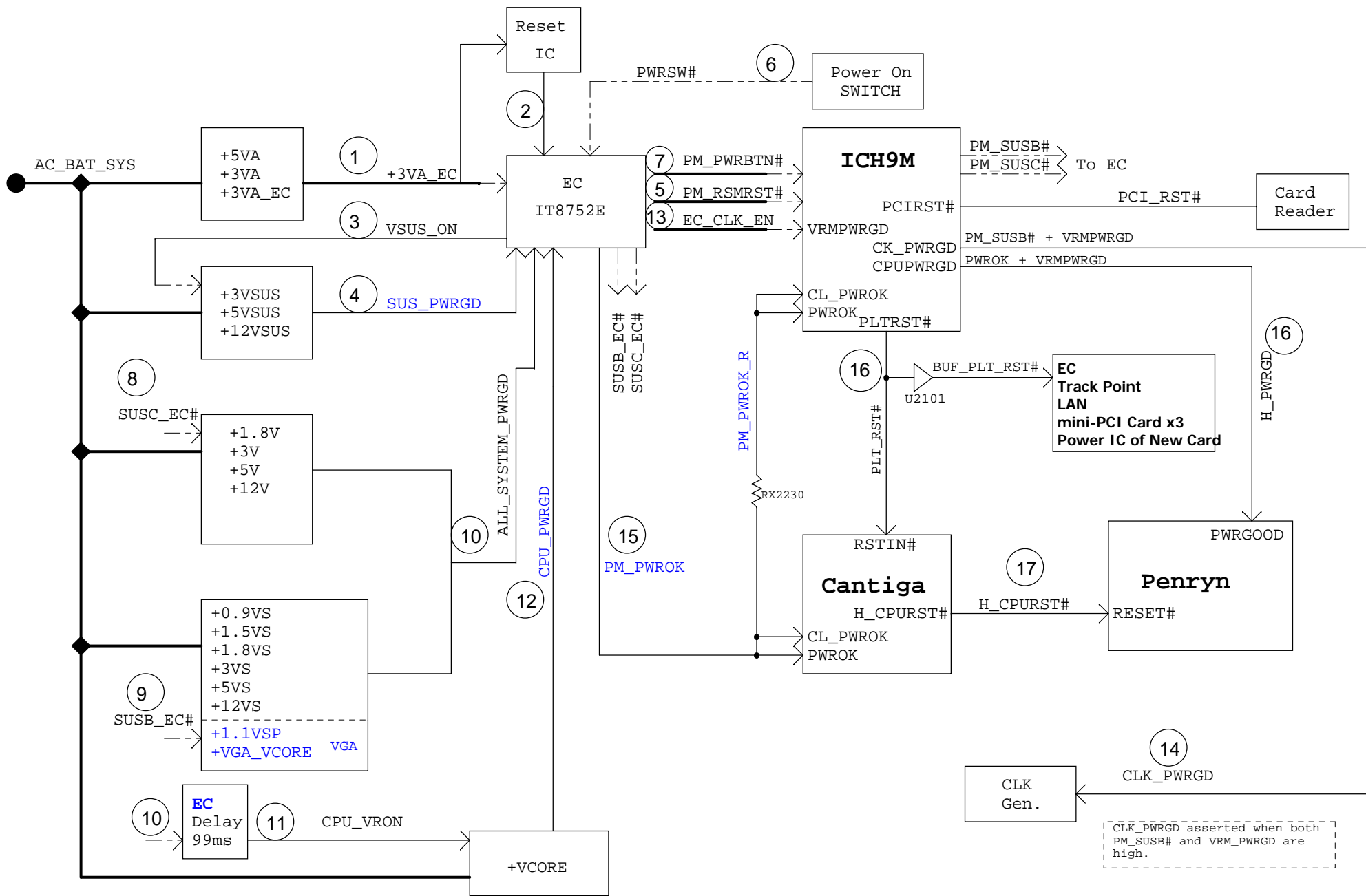
A



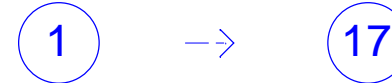
Title : ***

Engineer: *Peter Lo*

Size	Project Name	Rev
Custom	Rocky30	1.2
Date: Friday, March 14, 2008		Sheet 68 of 94



Power On Sequence



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		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size	Project Name		Rev
B	Rocky30		1.2
Date: <i>Friday, March 14, 2008</i>		Sheet	70 of 94

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		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size	Project Name		Rev
B	Rocky30		1.2
Date: <i>Friday, March 14, 2008</i>		Sheet	71 of 94

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		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size	Project Name	Rev	
B	Rocky30	1.2	
Date: <i>Friday, March 14, 2008</i>		Sheet	72 of 94

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		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size	Project Name		Rev
B	Rocky30		1.2
Date: <i>Friday, March 14, 2008</i>		Sheet	73 of 94

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		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size	Project Name		Rev
B	Rocky30		1.2
Date: <i>Friday, March 14, 2008</i>		Sheet	74 of 94

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		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size	Project Name		Rev
B	Rocky30		1.2
Date: <i>Friday, March 14, 2008</i>		Sheet	75 of 94

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		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size	Project Name		Rev
B	Rocky30		1.2
Date: <i>Friday, March 14, 2008</i>		Sheet	76 of 94

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		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size	Project Name	Rev	
B	Rocky30	1.2	
Date: <i>Friday, March 14, 2008</i>		Sheet	77 of 94

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		Title : ***	
		Engineer: <i>Peter Lo</i>	
Size	Project Name		Rev
B	Rocky30		1.2
Date: <i>Friday, March 14, 2008</i>		Sheet	78 of 94

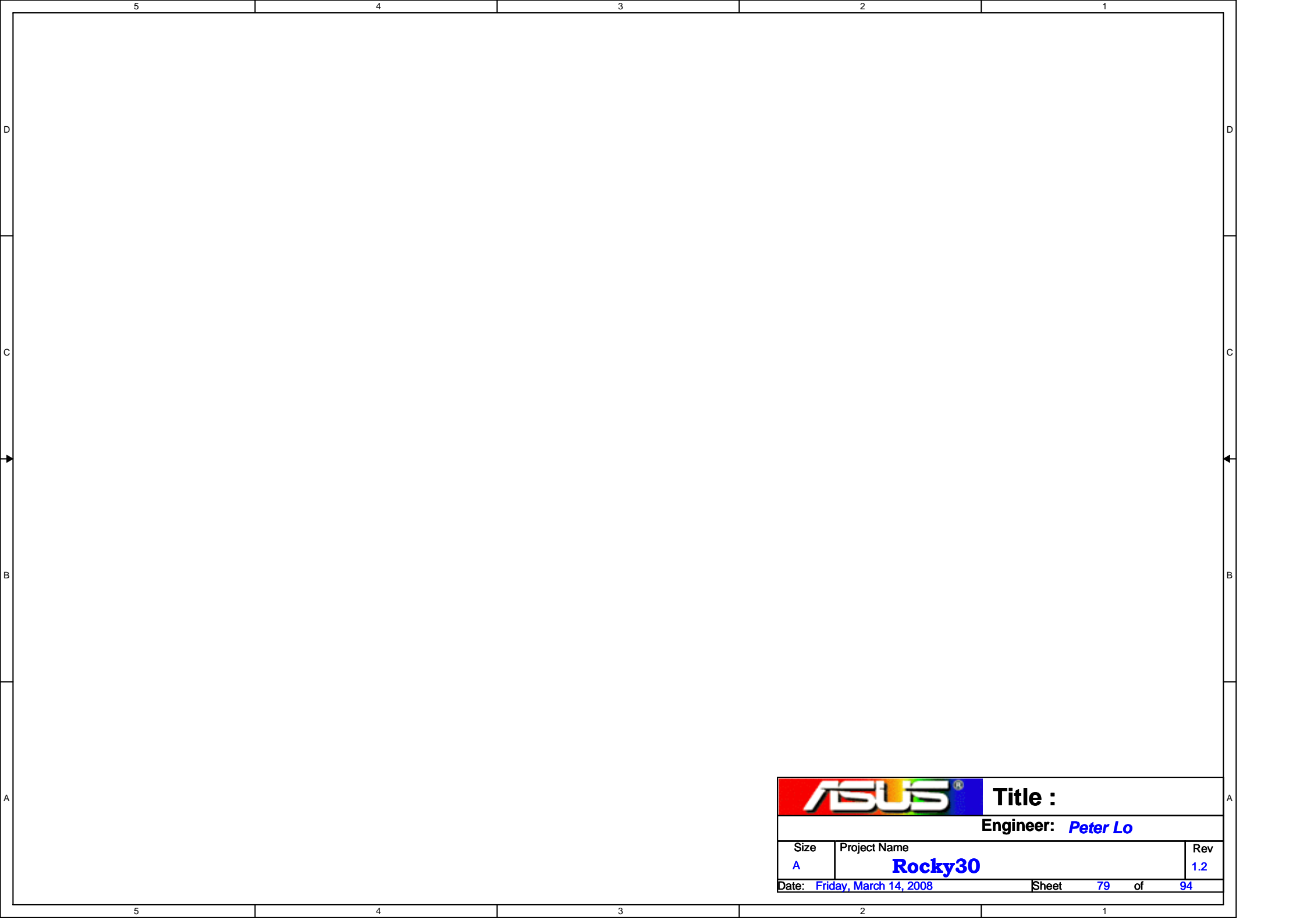
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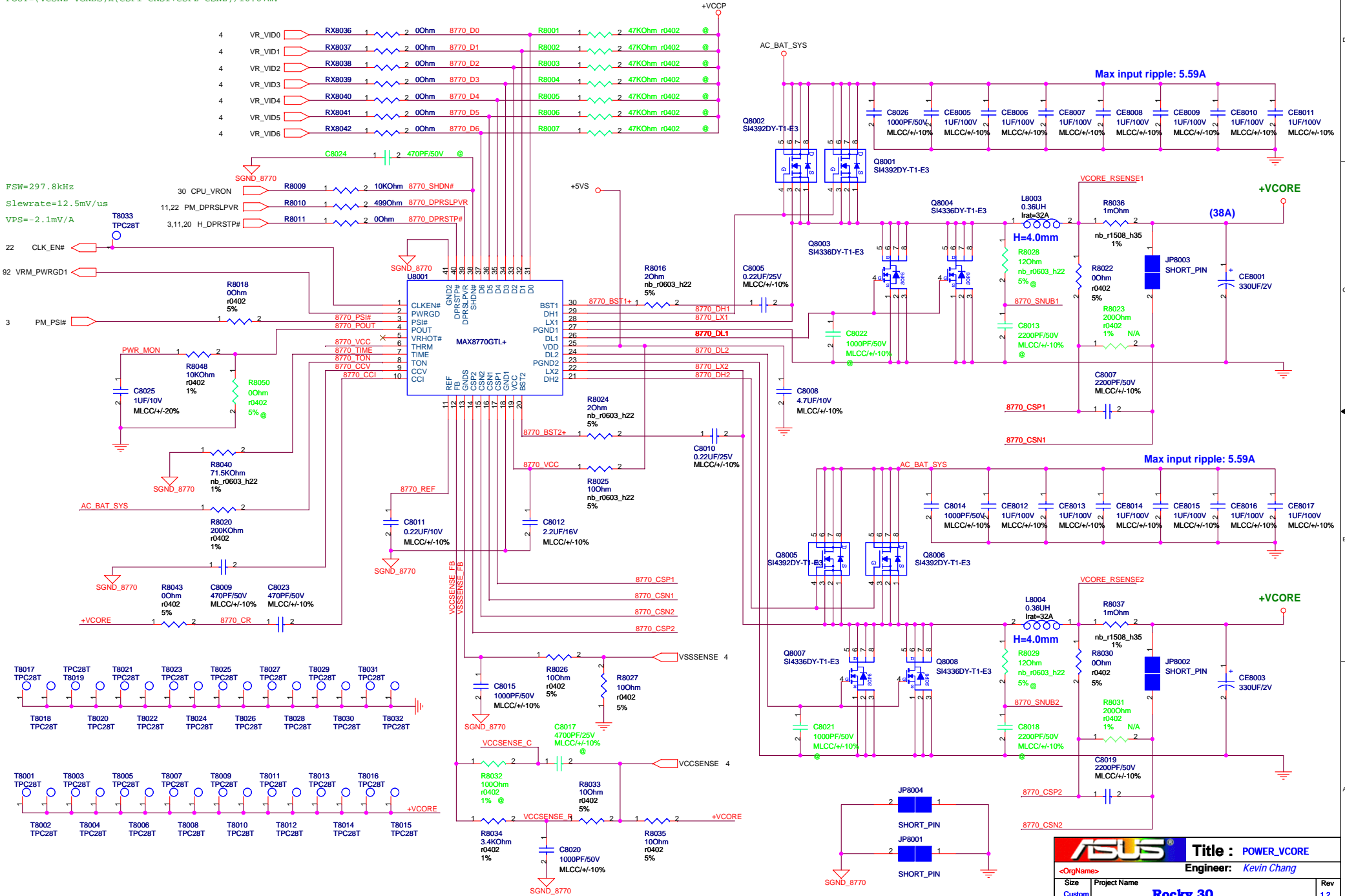
Title :

Engineer: *Peter Lo*

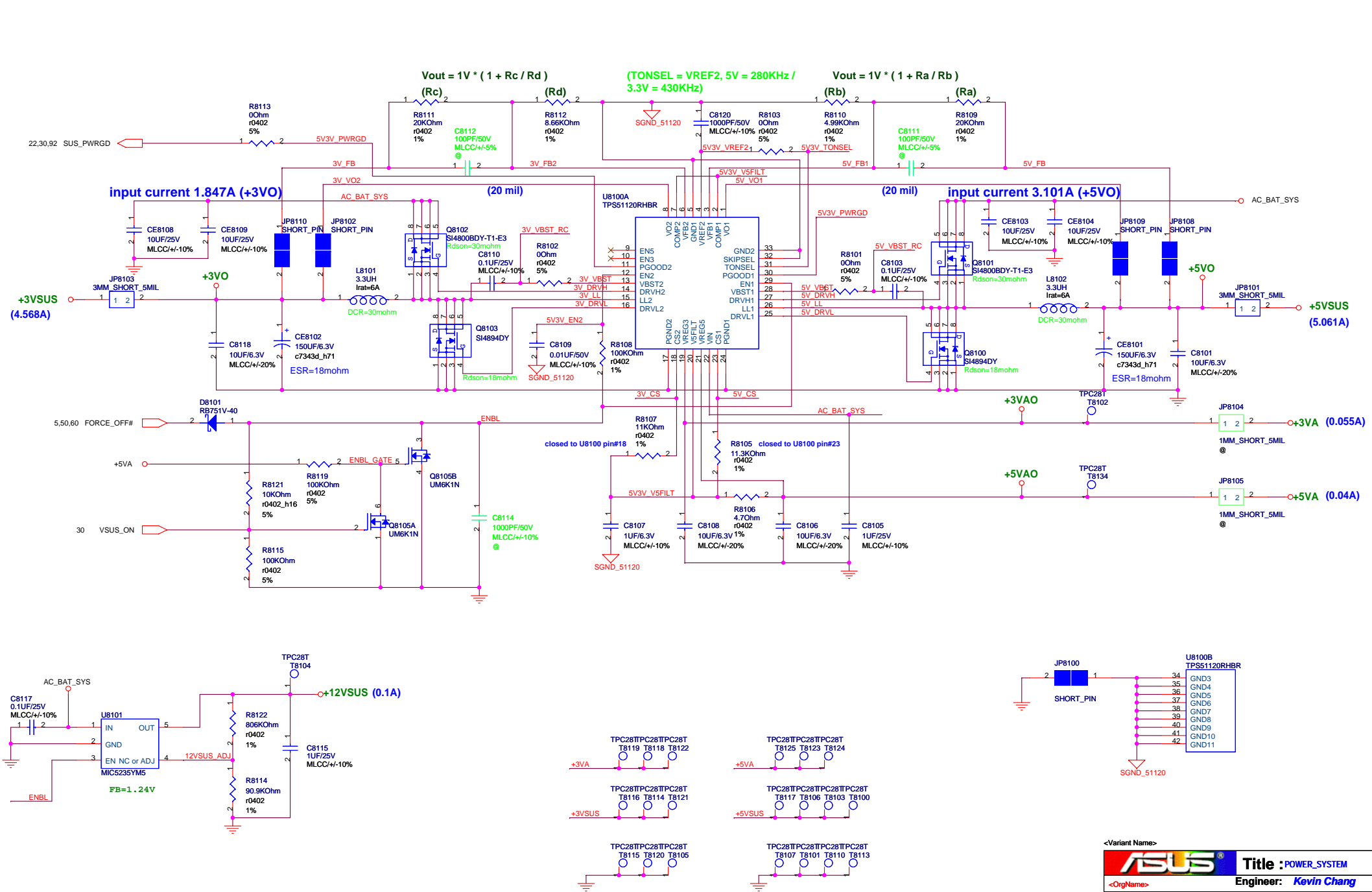
Size	Project Name	Rev
A	Rocky30	1.2
Date: <i>Friday, March 14, 2008</i>		Sheet <i>79</i> of <i>94</i>

IMVP6 CPU VCORE REGULATOR

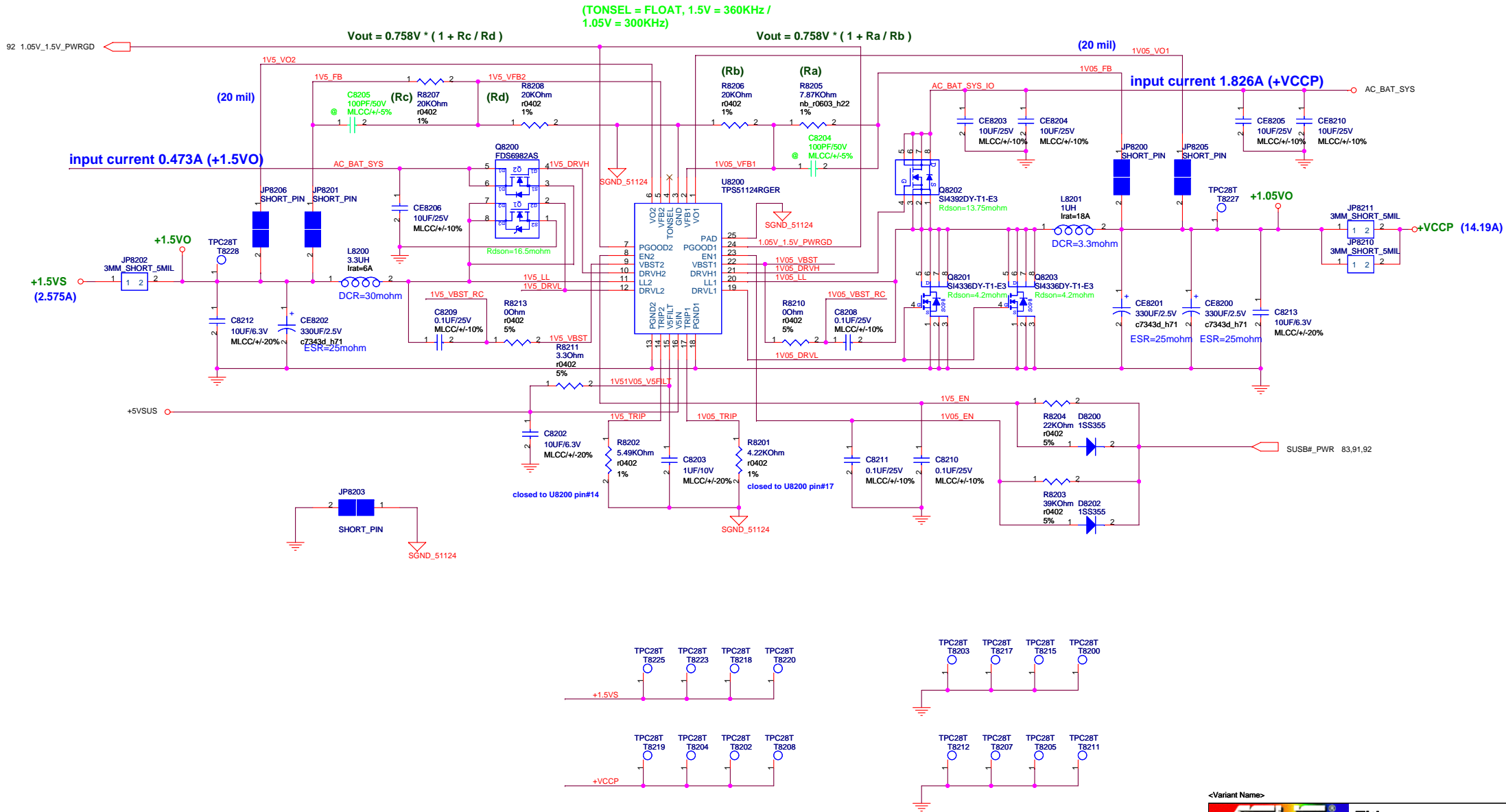
3.3V level logic level: DPRSLPVR, SHDN#
 1.05V level logic: VID, PSI#, DPRSTP#
 $POUT = (VCSN2 - VGND) \times (CSP1 - CNS1 + CSP2 - CNS2) / 16.67mV$



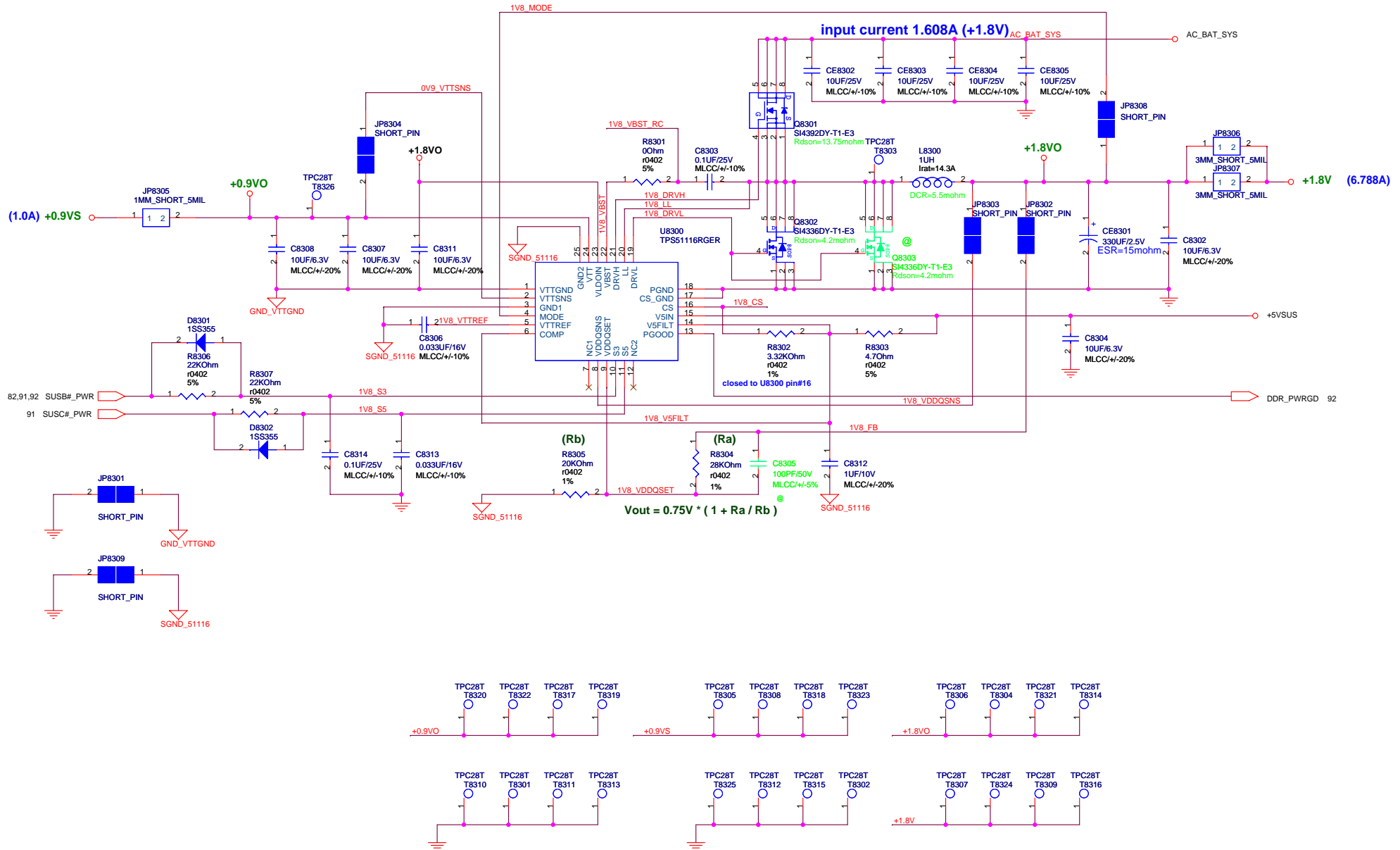
+5V / +3.3V POWER SUPPLY



+1.5VS / +VCCP POWER SUPPLY



+1.8V / +0.9VS POWER SUPPLY



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		Title : PWR_-****
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<OrgName>		Engineer:
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Size	Project Name	Rev
A4	Rocky30	1.2



		Title :	
<OrgName>		Engineer: <i>Kevin Chang</i>	
Size	Project Name		Rev
Custom	Rocky30		1.2
Date: <i>Friday, March 14, 2008</i>		Sheet	85 of 94

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D

C

C

B

B

A

A



Title : PWR_-****

Engineer: *Kevin Chang*

Size	Project Name	Rev
A4	Rocky30	1.2

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		Title : POWER_SHUTDOWN#	
<OrgName>		Engineer:	
Size	Project Name	Rev	
A4	Rocky30	1.2	
Date: Friday, March 14, 2008		Sheet	87 of 94

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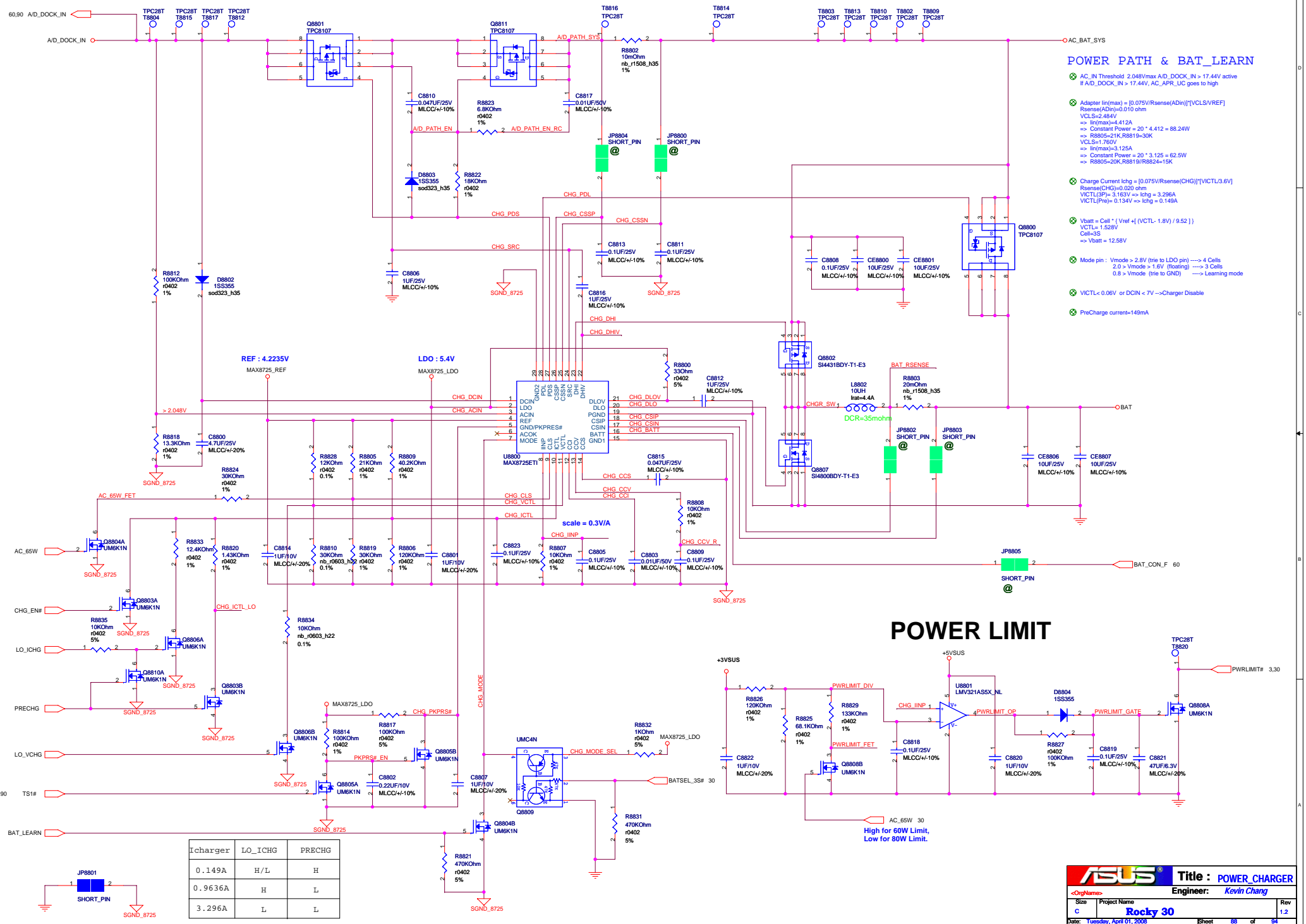
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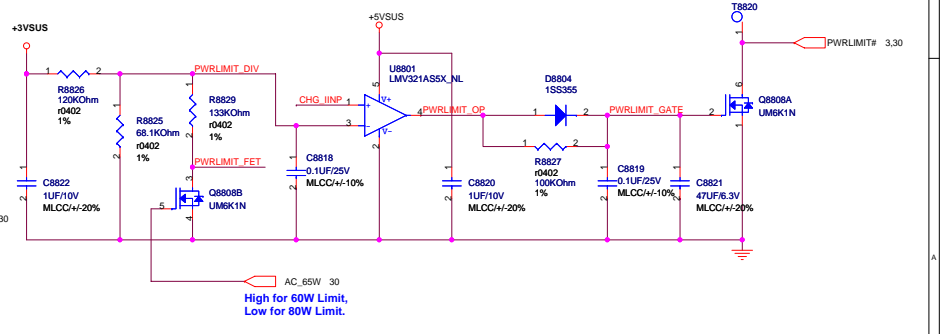
BATTERY CHARGER



POWER PATH & BAT_LEARN

- AC_IN Threshold: 2.048V(max A/D_DOCK_IN > 17.44V active
if A/D_DOCK_IN > 17.44V, AC_APR_UC goes to high
- Adaptor In(max) = $[0.075V / \text{Rsense(ADin)}] \cdot [VCLSV / \text{REF}]$
Rsense(ADin) = 0.010 ohm
VCLSV = 2.454V
=> In(max) = 4.412A
=> Constant Power = $20 \cdot 4.412 = 88.24W$
=> R8805 = 21K, R8819 = 30K
VCLSV = 1.760V
=> In(max) = 3.125A
=> Constant Power = $20 \cdot 3.125 = 62.5W$
=> R8805 = 20K, R8819 / R8824 = 15K
- Charge Current Ichg = $[0.075V / \text{Rsense(CHG)}] \cdot [VICTL / 3.6V]$
Rsense(CHG) = 0.020 ohm
VICTL(OP) = 3.163V => Ichg = 3.296A
VICTL(Pre) = 0.134V => Ichg = 0.149A
- Vbat = Cell * (Vref + (VCTL - 1.8V) / 9.52)
VCTL = 1.528V
Cell = 3S
=> Vbat = 12.58V
- Mode pin : Vmode > 2.8V (tie to LDO pin) -> 4 Cells
2.0 < Vmode < 1.8V (floating) -> 3 Cells
0.8 < Vmode (tie to GND) -> Learning mode
- VICTL < 0.06V or DCIN < 7V -> Charger Disable
- PreCharge current = 149mA

POWER LIMIT



High for 60W Limit,
Low for 80W Limit.

Icharger	LO_ICHG	PRECHG
0.149A	H/L	H
0.9636A	H	L
3.296A	L	L

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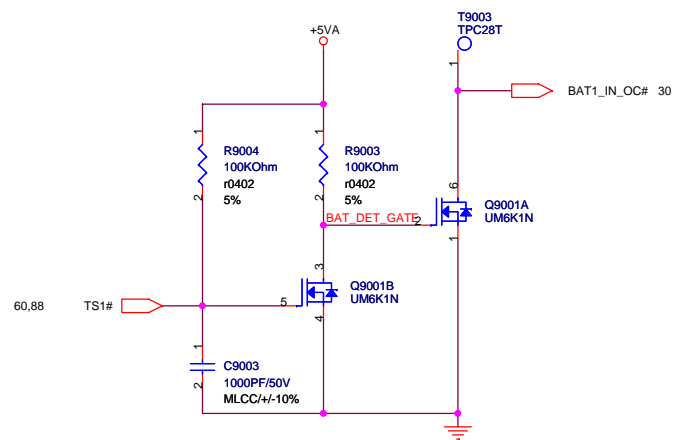
Title : TFT-LCD DRIVE

<OrgName> **Engineer:**

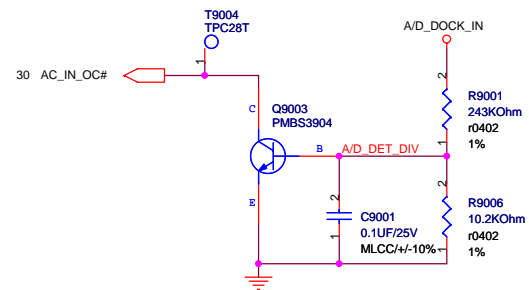
Size	Project Name	Rev
A4	Rocky30	1.2

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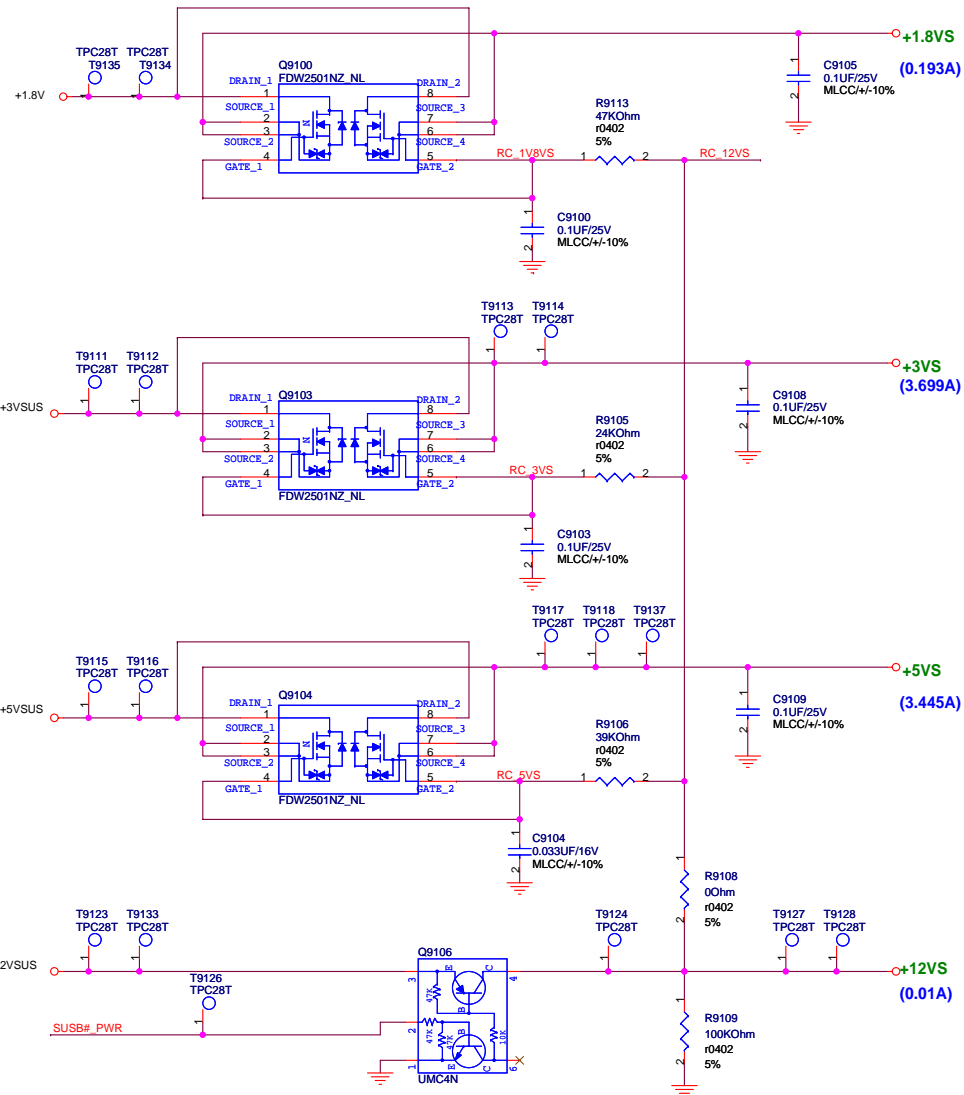
BATTERY IN DETECT



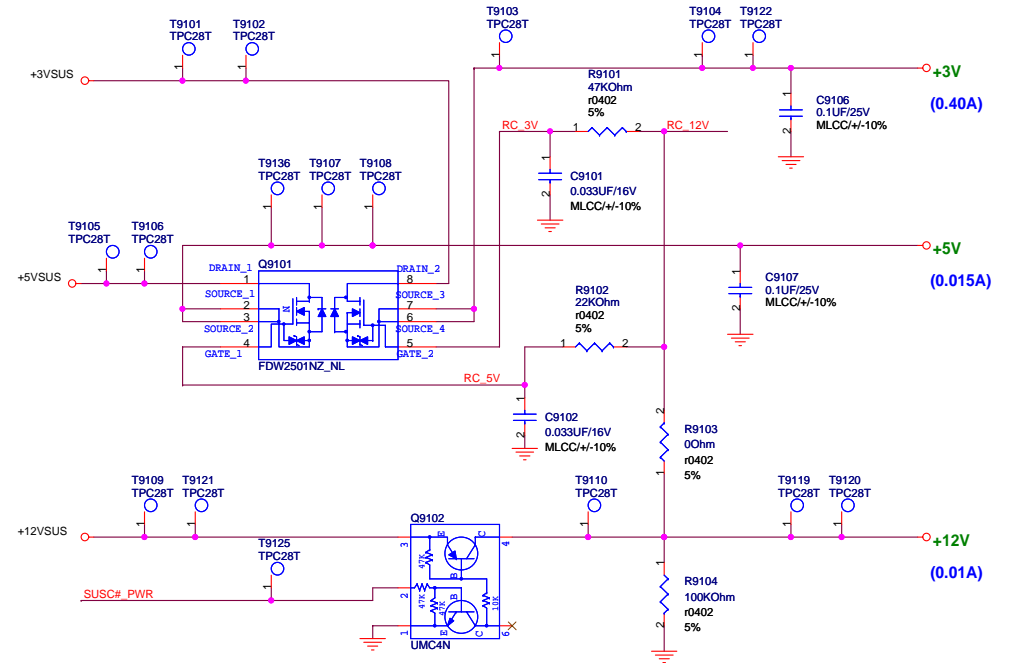
ADAPTER IN DETECT



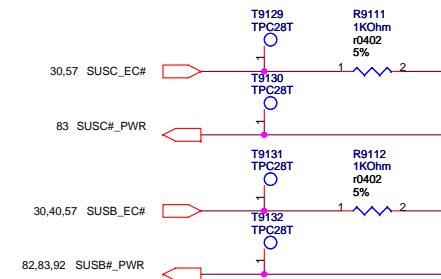
SUSB#_PWR Load SW



SUSC#_PWR Load SW

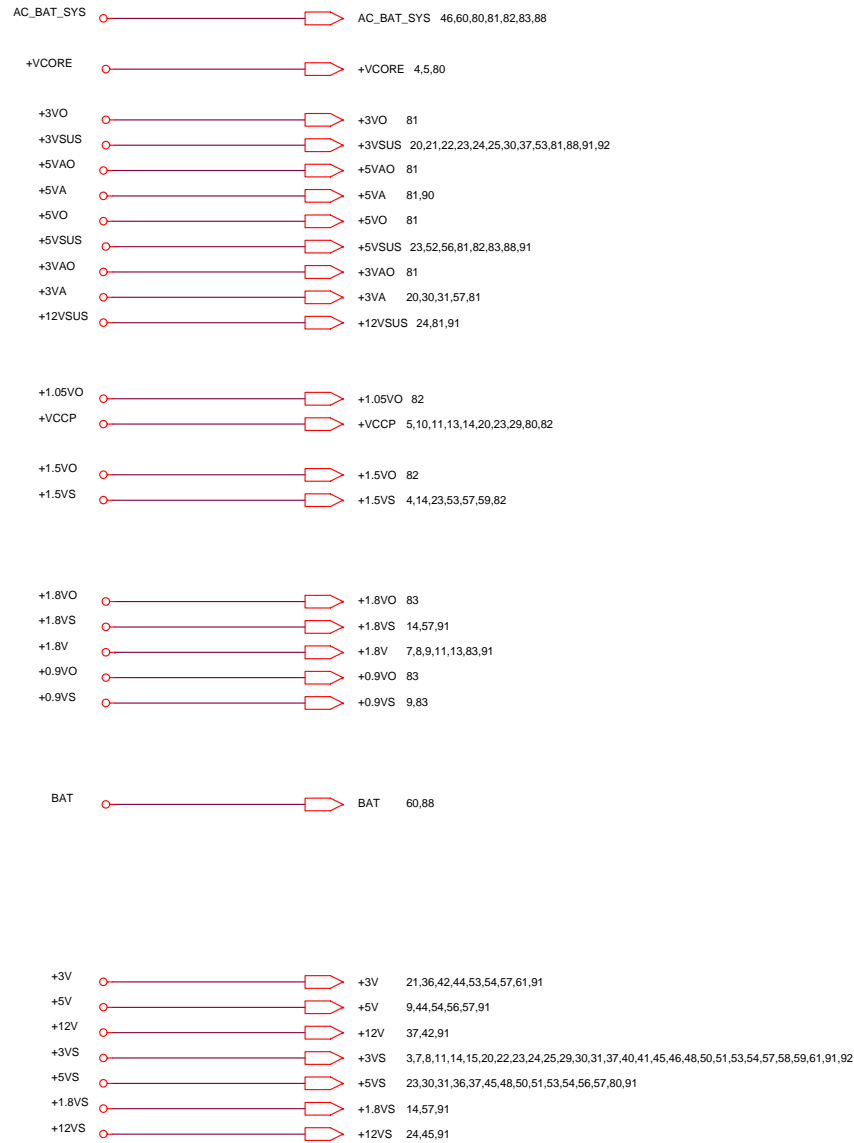


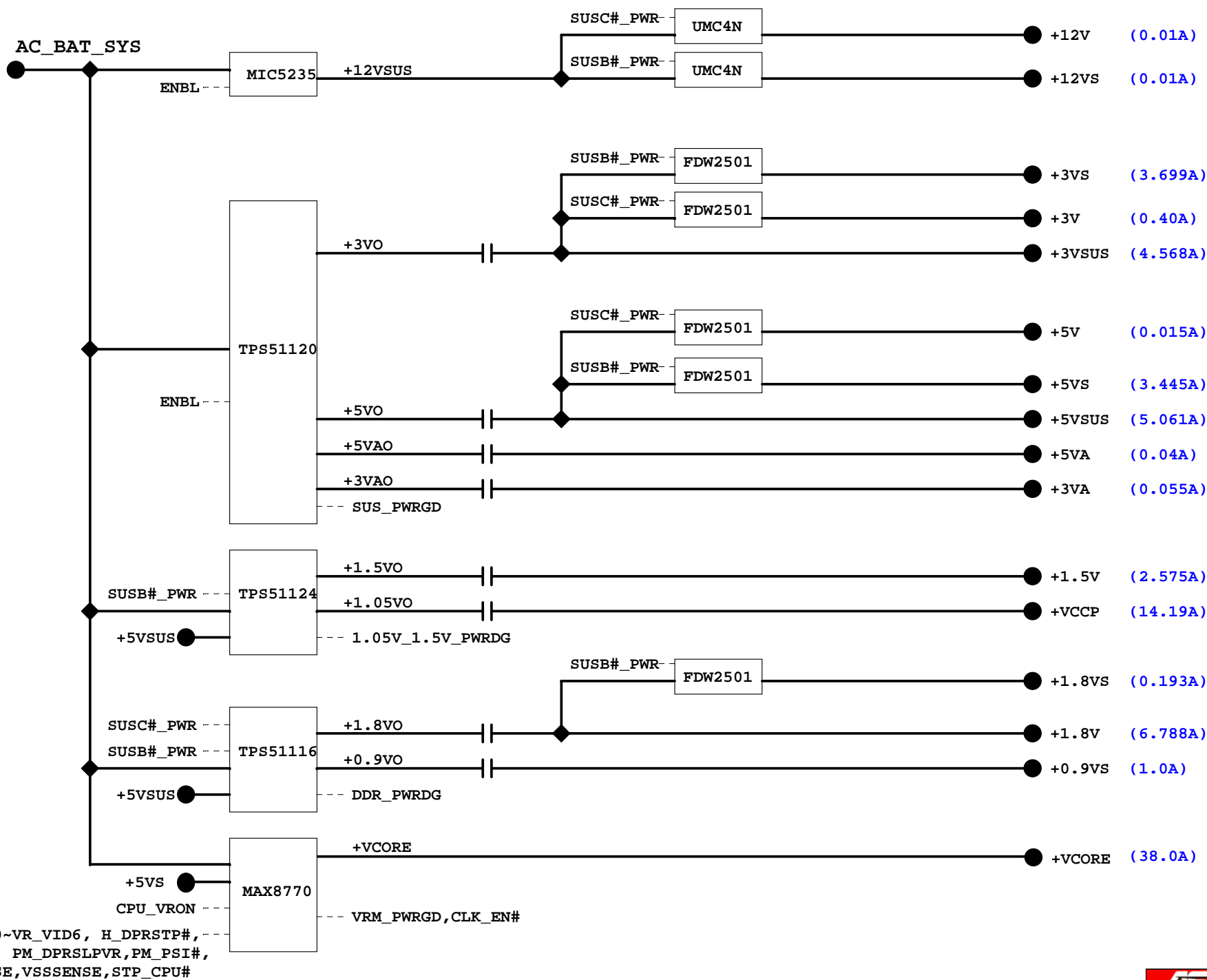
Enable Signal



POWER GOOD DETECTOR







VR_VID0~VR_VID6, H_DPRSTP#,
MCH_OK, PM DPRSLPVR, PM_PSI#,
VCCSENSE, VSSSENSE, STP_CPU#