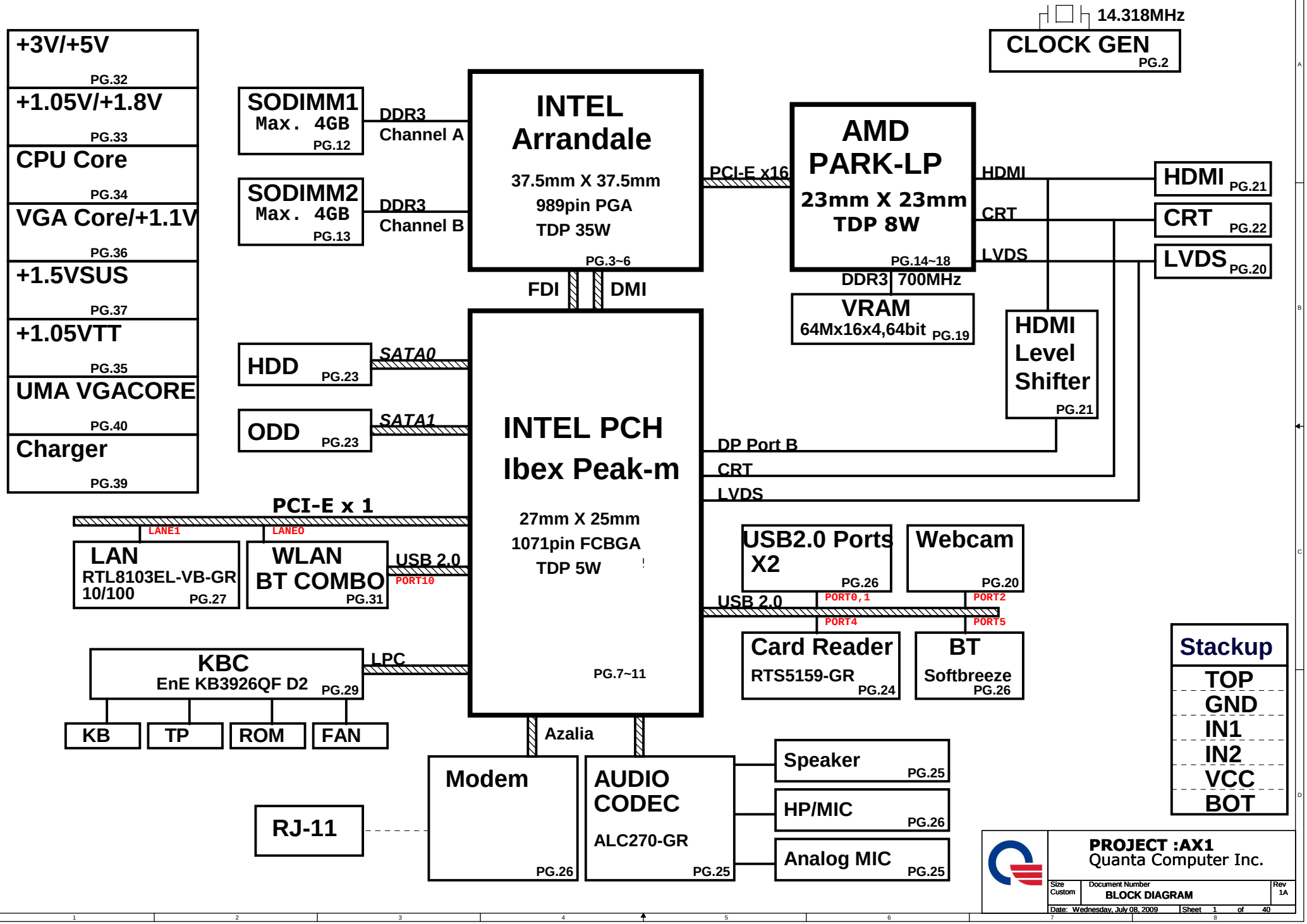
AX1 INTEL UMA/DISCRETE SYSTEM DIAGRAM



PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

Date: Wednesday, July 08, 2009 Sheet 1 of 40

25mA
+1.05V
+VDDIO_CLK
L33
HCB1608KF-181T15_6
C454 0.1U/10V_4
C436 0.1U/10V_4
C423 10U/6.3V_6S
C442 *10U/6.3V_8S
Place each 0.1uF cap close to pin

150mA
+3V
+VDDSE_CLK
L37
HCB1608KF-181T15_6
C469 4.7U/6.3V_6
C465 0.1U/10V_4
C480 0.1U/10V_4
Place each 0.1uF cap close to pin

150mA
+3V
+VDDCORE_CLK
L35
*HCB1608KF-181T15_6
+1.5V
L34
HCB1608KF-181T15_6
C425 4.7U/6.3V_6
C435 0.1U/10V_4
C481 0.1U/10V_4
C437 0.1U/10V_4
Place each 0.1uF cap close to pin

Y1
XTAL_IN
XTAL_OUT
14.318MHZ
C460 33P/50V_4
C455 33P/50V_4

+3V
R298 *10K/F_4
CPU_SEL
R300 10K/F_4

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

U13
9LRS3197
QFN32
+VDDSE_CLK
+VDDCORE_CLK
C482 *0.047U/10V
+VDDIO_CLK
C415 *0.047U/10V
<8,12,13> CGDAT_SMB
<8,12,13> CGCLK_SMB
+3V
<8> CLK_ICH_14M
R279 10K/F_4
R293 33_4
CPU_SEL
C477 *10P/50V_4
Place R8044 within 0.5" of C/G
CK_PWRGD_R
XTAL_OUT
XTAL_IN
VDD_LCD
VDD_REF
VDD_USB
VDD_SRC
VDD_CPU
VDD_CPU_IO
VDD_SRC_IO
SDATA
SCLK
CPU_STOP#
REF_0/CPU_SEL
CK_PWRGD/PD#_3.3
XOUT
XIN
VSS_SATA
VSS_USB
VSS_LCD
CPU-0
CPU-0#
CPU-1
CPU-1#
DOT96T_LPR
DOT96C_LPR
SRC-1
SRC-1#
SATA
SATA#
27MHz_nonSS
27MHz_SS
GND
VSS_REF
VSS_CPU
VSS_SRC
CLK_BUF_BCLK_P
CLK_BUF_BCLK_N
RP24 *4P2R-S-0
CLK_BUF_BCLK_P <8>
CLK_BUF_BCLK_N <8>
CLK_BUF_DREFCLK
CLK_BUF_DREFCLK#
RP27 *4P2R-S-0
CLK_BUF_DREFCLK <8>
CLK_BUF_DREFCLK# <8>
CLK_BUF_PCIE_3GPLL
CLK_BUF_PCIE_3GPLL#
RP25 *4P2R-S-0
CLK_BUF_PCIE_3GPLL <8>
CLK_BUF_PCIE_3GPLL# <8>
CLK_BUF_DREFSSCLK
CLK_BUF_DREFSSCLK#
RP26 *4P2R-S-0
CLK_BUF_DREFSSCLK <8>
CLK_BUF_DREFSSCLK# <8>
CLK_VGA_27M_NOSS
R304 22_4
R494 22_4
0918 SI Modify
CLK_VGA_27M_SS
R303 *33_4
EVGA-XTALI <15>
27M_TCK <15>
CLK_27M_SS <15>
Discrete only

+3V
R282 1K/F_4
CK_PWRGD_R
Q15 2N7002E
R280 100K/F_4
<34> VR_PWRGD_CLKEN#

+1.05V <7,8,9,11,13,33,34,40>
+1.5V <31,38>
+3V <3,7,8,9,10,11,12,13,15,20,21,22,23,24,25,26,27,28,29,30,31,34,38>

EMI request
+3V
C812 .1U/10V_4
C813 .1U/10V_4
C814 .1U/10V_4
C815 .1U/10V_4
+1.05V
C816 .1U/10V_4
C817 .1U/10V_4
C818 .1U/10V_4
C819 .1U/10V_4
C820 .1U/10V_4
C821 .1U/10V_4

CPU
H6 H4 H3 H11
*H-TC248BC197D150P2

GPU
H10 H9
*H-TC248BC197D150P2
H0 H1 H2 H5 H7 H8
*H-c354d118p2
*H-c236d118p2
*H-c276d118p2

H12 H13 H16 H17 H18
*H-c354d118p2
*H-c354d354n
*H-TSBC394D118P2
*H-TSBC276D118P2
*H-O-AX1-1

PAD0 PAD1 PAD2 PAD3 PAD4 PAD5 PAD6 PAD7 PAD8

PROJECT :AX1
Quanta Computer Inc.
Size: Custom
Document Number: Clock Gen(9LRS3197)/HOLES
Rev: 1A
Date: Thursday, November 12, 2009
Sheet 2 of 40

	DIS	UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

03

U16A

DMI

Intel(R) FDI

PCI EXPRESS -- GRAPHICS

2.7GT/s data rate

IC,AUB_CFD_rPGA,R1P0

U16B

MISC

THERMAL

CLOCKS

DDR3 MISC

PWR MANAGEMENT

JTAG & BPM

IC,AUB_CFD_rPGA,R1P0

JTAG MAPPING

for S3 power reduction

SI modify

Discrete Only

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (Check list 1.0).

SI modify

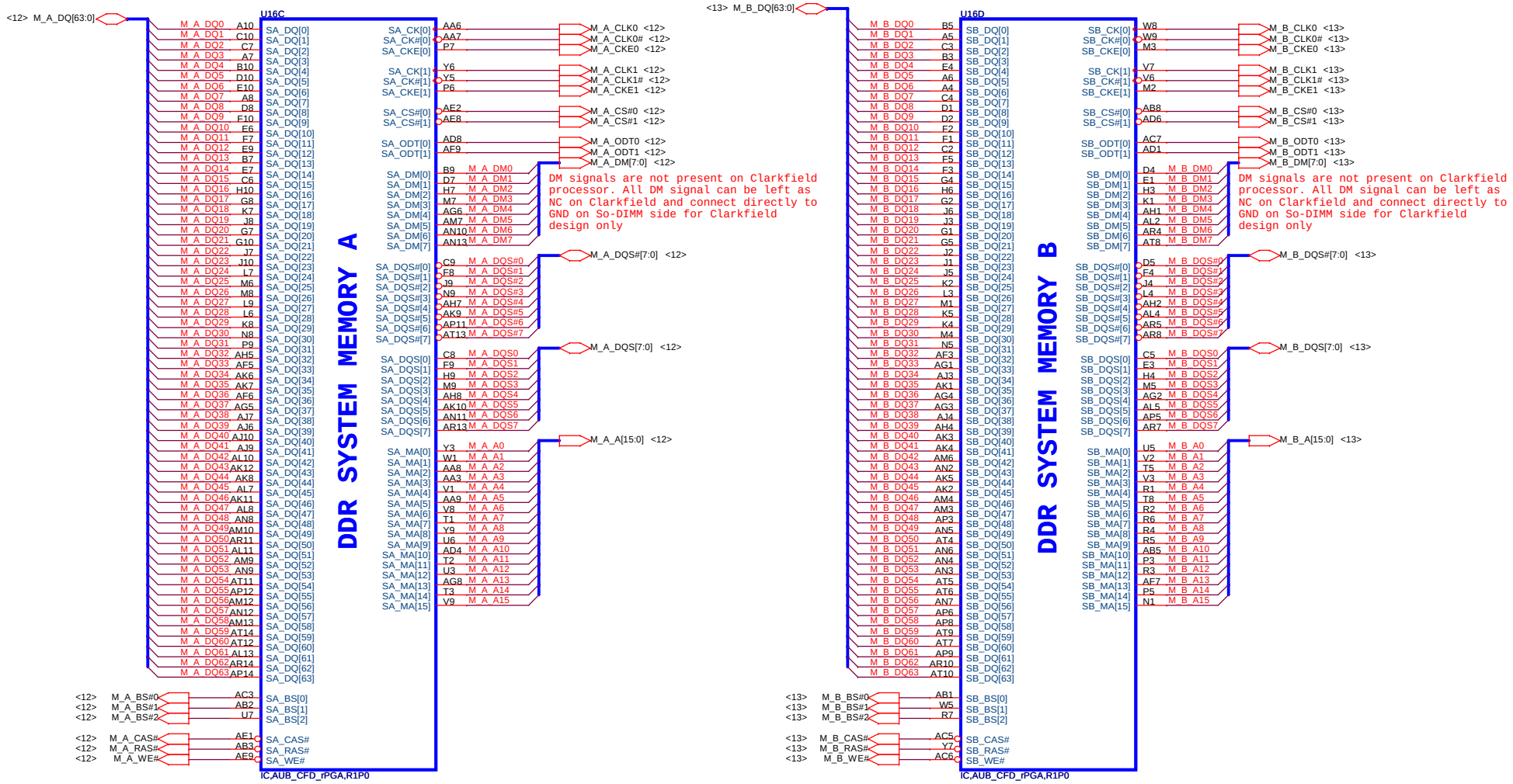
Use a voltage divider with VDDQ (1.5 V) rail ON in S3) and resistor combination of 1.5K ±1% (to VDDQ)/750±1% (to GND) to convert to processor VTT level.

Scan Chain (Default)	STUFF -> Ra, Rc, Re NO STUFF -> Rb, Rd
CPU Only	STUFF -> Ra, Rb NO STUFF -> Rc, Rd, Re
GMCH Only	STUFF -> Rd, Re NO STUFF -> Ra, Rb, Rc

PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 1/4(HOST&PEX)	1A
Date: Monday, November 30, 2009	Sheet 3 of 40	

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 2/4(DDR)	1A

Date: Thursday, November 12, 2009 | Sheet 4 of 40

18A

	DIS	UMA
Rc	NA	4.7K
Rd	NA	0 ohm
Re	NA	0 ohm
Rf	NA	NA

U16F

POWER

CPU CORE SUPPLY

1.1V RAIL POWER

CPU VIDS

SENSE LINES

+VCORE

C147 22U/6.3V_8S
C25 22U/6.3V_8S
C639 22U/6.3V_8S
C538 22U/6.3V_8S
C184 22U/6.3V_8S
C144 22U/6.3V_8S
C148 22U/6.3V_8S
C236 22U/6.3V_8S
C627 22U/6.3V_8S
C170 22U/6.3V_8S
C169 22U/6.3V_8S
C654 22U/6.3V_8S
C631 10U/6.3V_8
C204 10U/6.3V_8
C186 10U/6.3V_8
C537 10U/6.3V_8
C202 10U/6.3V_8
C146 10U/6.3V_8
C30 10U/6.3V_8
C235 10U/6.3V_8
C171 10U/6.3V_8
C238 10U/6.3V_8
C237 10U/6.3V_8
C648 10U/6.3V_8
C145 10U/6.3V_8
C203 10U/6.3V_8
C646 10U/6.3V_8
C234 10U/6.3V_8
C233 0.1U/10V_4
C227 0.1U/10V_4

C154 2 *0.047U/10V
C153 2 *0.047U/10V
C152 2 *0.047U/10V

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

IC,AUB_CFD_rPGA,R1P0

VTT0_1 VTT0_2 VTT0_3 VTT0_4 VTT0_5 VTT0_6 VTT0_7 VTT0_8 VTT0_9 VTT0_10 VTT0_11 VTT0_12 VTT0_13 VTT0_14 VTT0_15 VTT0_16 VTT0_17 VTT0_18 VTT0_19 VTT0_20 VTT0_21 VTT0_22 VTT0_23 VTT0_24 VTT0_25 VTT0_26 VTT0_27 VTT0_28 VTT0_29 VTT0_30 VTT0_31 VTT0_32

AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

+1.05V_VTT

C637 10U/6.3V_8
C625 10U/6.3V_8
C597 10U/6.3V_8
C531 10U/6.3V_8
C47 10U/6.3V_8
C605 10U/6.3V_8
C52 10U/6.3V_8
C645 22U/6.3V_8S
C105 22U/6.3V_8S
C630 22U/6.3V_8S

VTT0_33 VTT0_34 VTT0_35 VTT0_36 VTT0_37 VTT0_38 VTT0_39 VTT0_40 VTT0_41 VTT0_42 VTT0_43 VTT0_44

AE10 AE10 AC10 AB10 Y10 W10 U10 T10 J12 J11 J16 J15

+1.05V_VTT

C102 22U/6.3V_8S
C126 22U/6.3V_8S

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

PSI# AN33 H_PSI# <34>

VID[0] AK35 CPU_VID0 <34>
VID[1] AK33 CPU_VID1 <34>
VID[2] AK34 CPU_VID2 <34>
VID[3] AL35 CPU_VID3 <34>
VID[4] AL33 CPU_VID4 <34>
VID[5] AM33 CPU_VID5 <34>
VID[6] AM35 CPU_VID6 <34>
PROC_DPRSLPVR AM34 DPRSLPVR <34>

VTT_SELECT G15

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

ISENSE AN35 I_MON <34>

VTT_SENSE B15 VTT_SENSE <35>
VSS_SENSE_VTT A15 VSS_SENSE_VTT <35>

R389 100/F_4
R393 100/F_4

VCC_SENSE AJ34 VCCSENSE <34>
VSS_SENSE AJ35 VSSSENSE <34>

UMA only

Please note that +VCC_GFX_CORE
should be 1.05V in Auburndale

+VGACORE_IGPU

C641 *22U/6.3V_8S
C642 *22U/6.3V_8S
C644 *10U/6.3V_8
C643 *10U/6.3V_8

	DIS	UMA
Ra	0 ohm	NA

Ra R383 0_8

U16G

POWER

GRAPHICS

SENSE LINES

GRAPHICS VIDs

DDR3 - 1.5V RAILS

FDI

PEG & DMI

1.1V

1.8V

VAXG1 VAXG2 VAXG3 VAXG4 VAXG5 VAXG6 VAXG7 VAXG8 VAXG9 VAXG10 VAXG11 VAXG12 VAXG13 VAXG14 VAXG15 VAXG16 VAXG17 VAXG18 VAXG19 VAXG20 VAXG21 VAXG22 VAXG23 VAXG24 VAXG25 VAXG26 VAXG27 VAXG28 VAXG29 VAXG30 VAXG31 VAXG32 VAXG33 VAXG34 VAXG35 VAXG36

AT21 AT19 AT18 AT16 AR21 AR19 AR18 AR16 AP21 AP19 AP18 AP16 AN21 AN19 AN18 AN16 AM21 AM19 AM18 AM16 AL21 AL19 AL18 AL16 AK21 AK19 AK18 AK16 AJ21 AJ19 AJ16 AH21 AH19 AH18 AH16

VTT1_45 VTT1_46 VTT1_47 VTT1_48 VTT1_49 VTT1_50 VTT1_51 VTT1_52 VTT1_53 VTT1_54 VTT1_55 VTT1_56 VTT1_57 VTT1_58

J24 J23 H25 K26 J27 J26 J25 H27 G28 G27 G26 F26 E26 E25

+1.05V_VTT

C104 22U/6.3V_8S
C600 22U/6.3V_8S
C539 22U/6.3V_8S
C543 22U/6.3V_8S
C544 22U/6.3V_8S
C103 22U/6.3V_8S

VAXG_SENSE AR22
VSSAXG_SENSE AT22

VCC_AXG_SENSE <40>
VSS_AXG_SENSE <40>

GFX_VID[0] AM22
GFX_VID[1] AP22
GFX_VID[2] AN22
GFX_VID[3] AP23
GFX_VID[4] AM23
GFX_VID[5] AP24
GFX_VID[6] AN24

GFXVR_VID_0 <40>
GFXVR_VID_1 <40>
GFXVR_VID_2 <40>
GFXVR_VID_3 <40>
GFXVR_VID_4 <40>
GFXVR_VID_5 <40>
GFXVR_VID_6 <40>

GFX_VR_EN R426 *4.7K_4
GFX_VR_EN AR25
GFX_DPRSLPVR AT25
GFX_IMON AM24

R427 *0_4
R196 *0_4
R195 *1K/J_4

GFXVR_EN <40>
GFXVR_DPRSLPVR <40>
GFXVR_IMON <40>

2A

VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9 VDDQ10 VDDQ11 VDDQ12 VDDQ13 VDDQ14 VDDQ15 VDDQ16 VDDQ17 VDDQ18

AJ1 AF1 AE7 AE4 AC1 AB7 AB4 Y1 W7 W4 U1 T7 T4 P1 N7 N4 L1 H1

C92 1U/6.3V_4
C121 1U/6.3V_4
C133 1U/6.3V_4
C108 1U/6.3V_4
C82 1U/6.3V_4
C86 22U/6.3V_8S
C77 22U/6.3V_8S
C80 *330U/2V_7343

+1.5VSUS

0.1U/10V_4 C182
0.1U/10V_4 C142
0.1U/10V_4 C261
0.1U/10V_4 C189

+1.5VSUS_L

VTT0_59 VTT0_60 VTT0_61 VTT0_62 VTT0_63 VTT0_64 VTT0_65 VTT0_66 VTT0_67 VTT0_68

P10 N10 L10 K10 J22 J20 J18 H21 H20 H19

C612 10U/6.3V_8
C620 10U/6.3V_8
C599 22U/6.3V_8S
C598 22U/6.3V_8S

+1.05V_VTT

VCCPLL1 VCCPLL2 VCCPLL3

L26 L27 M26

C110 22U/6.3V_8S
C258 4.7U/6.3V_6
C111 2.2U/6.3V_6
C263 1U/6.3V_4
C602 1U/6.3V_4

+1.8V

for S3 power reduction

SI modify

Q9 AON6718L

<38> MAIND

<12,38> MAINON_G

R100 *0/F_2512

Q10 2N7002E

R136 220/F_4

+1.5VSUS

for S3 power reduction

SI modify

+VCORE

C34 C35 C36 C39 C43 C530 C533 C534 C536 C24

*10U/6.3V_8

CPU_VID0 R406 1K/J_4
CPU_VID1 R398 *1K/J_4
CPU_VID2 R405 1K/J_4
CPU_VID3 R397 *1K/J_4
CPU_VID4 R409 1K/J_4
CPU_VID5 R411 *1K/J_4
CPU_VID6 R410 *1K/J_4
DPRSLPVR R412 1K/J_4
H_PSI# R413 *1K/J_4
R415 1K/J_4
R421 1K/J_4
R418 *1K/J_4
R414 *1K/J_4
R416 1K/J_4
R429 1K/J_4
R428 *1K/J_4
R422 *1K/J_4
R419 1K/J_4

+1.05V_VTT

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

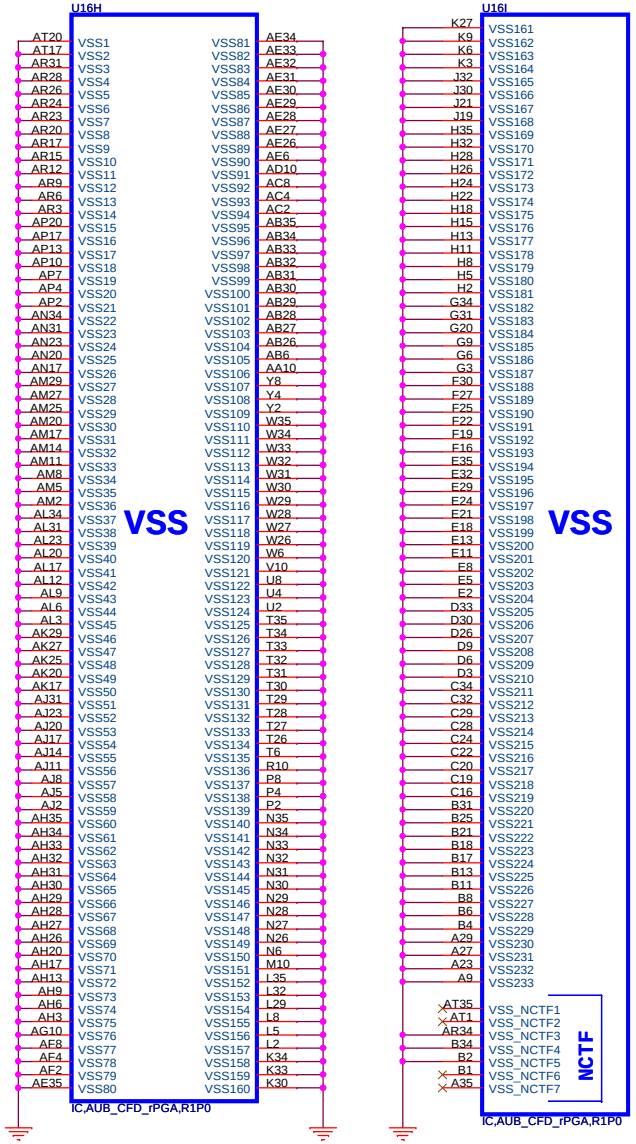
<34> +VCORE
<3,10,11,29,30,34,35,40> +1.05V_VTT
<3,12,13,37,38> +1.5VSUS
<11,33,38> +1.8V

PROJECT :AX1
Quanta Computer Inc.

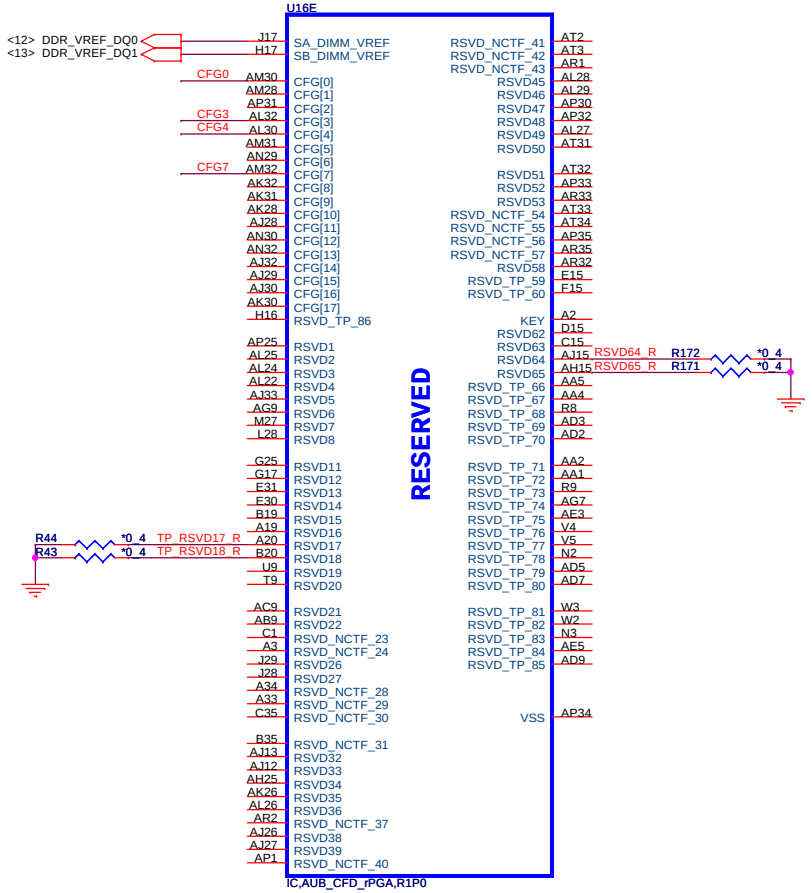
Size	Document Number	Rev
Custom	PROCESSER 3/4(POWER)	1A

Date: Thursday, December 03, 2009 | Sheet 5 of 40

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



CFG[1:0] - PCI_Epress Configuration Select
* 11= 1 x 16 PEG
* 10= 2 x 8 PEG

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

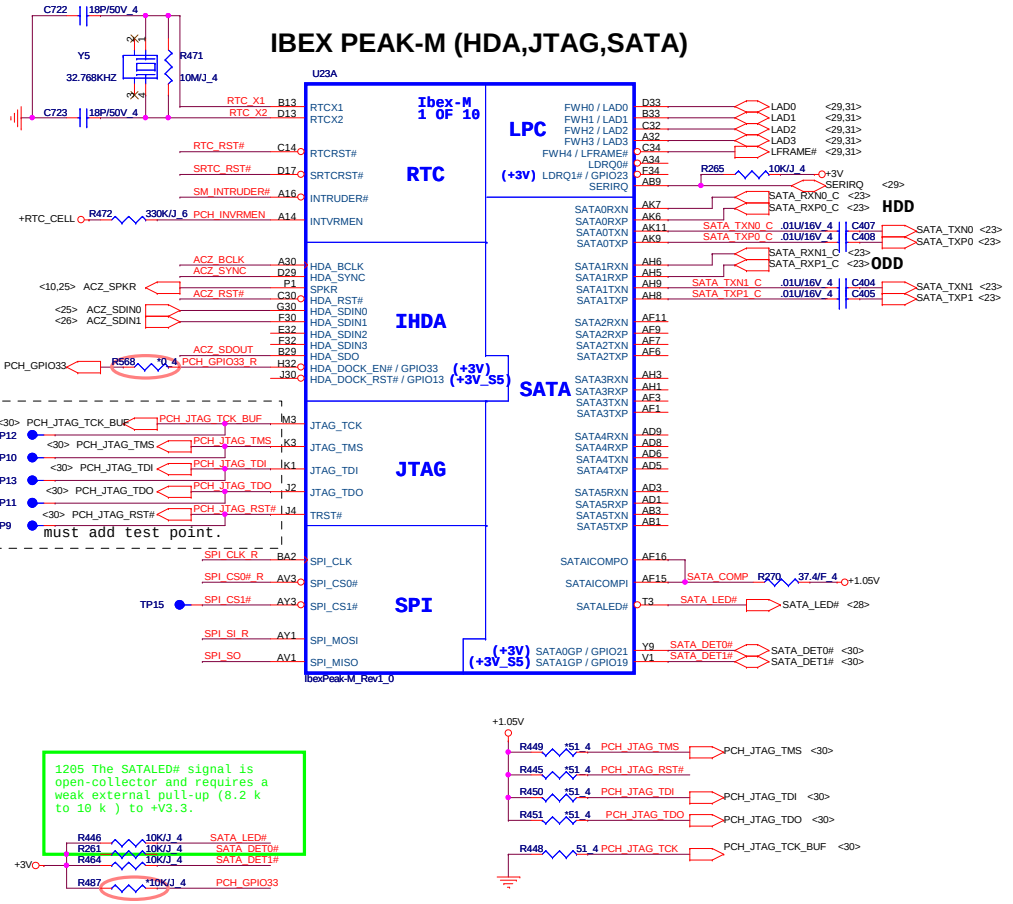
PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 4/4 (GND)	1A

Date: Thursday, November 12, 2009 | Sheet 6 of 40

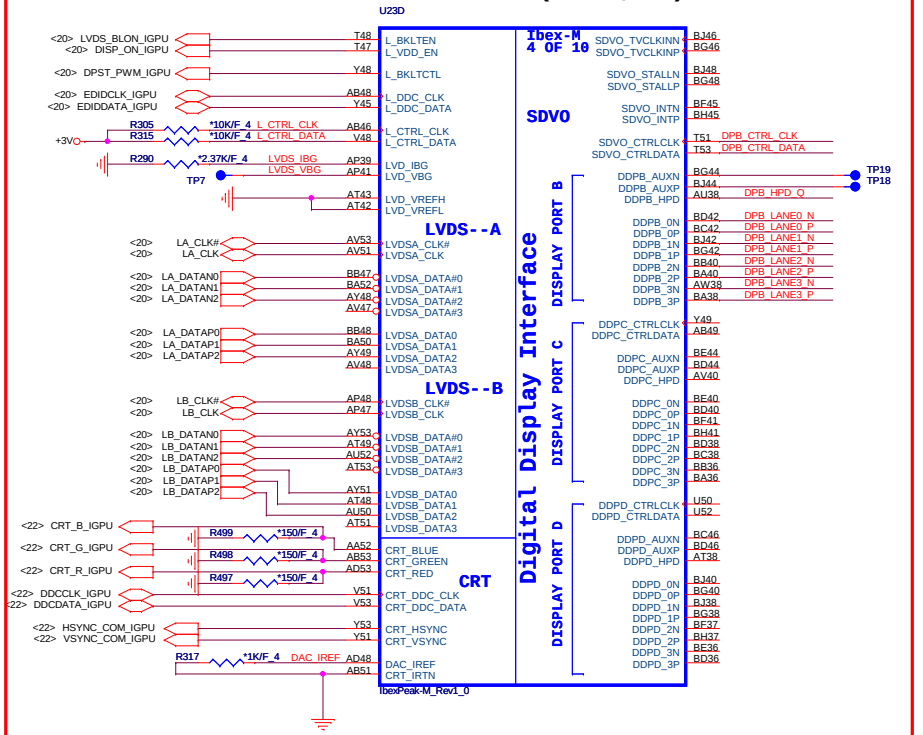
INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

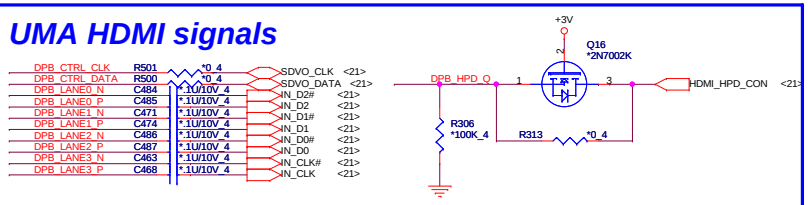


UMA CRT,LVDS&HDMI signals

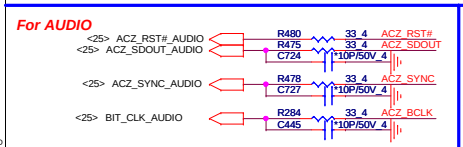
IBEX PEAK-M (LVDS,DDI)



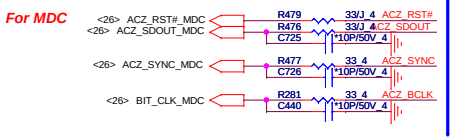
UMA HDMI signals



For AUDIO

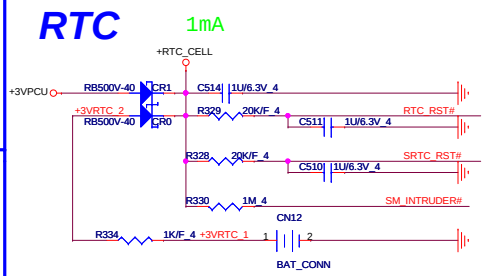


For MDC

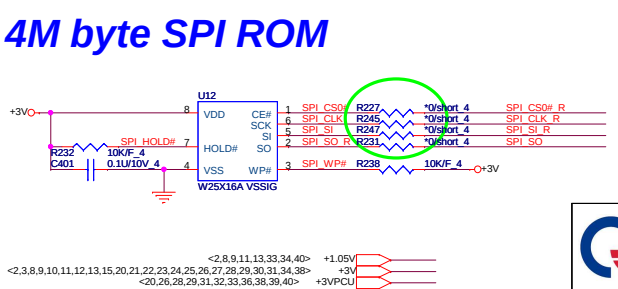


RTC

1mA



4M byte SPI ROM



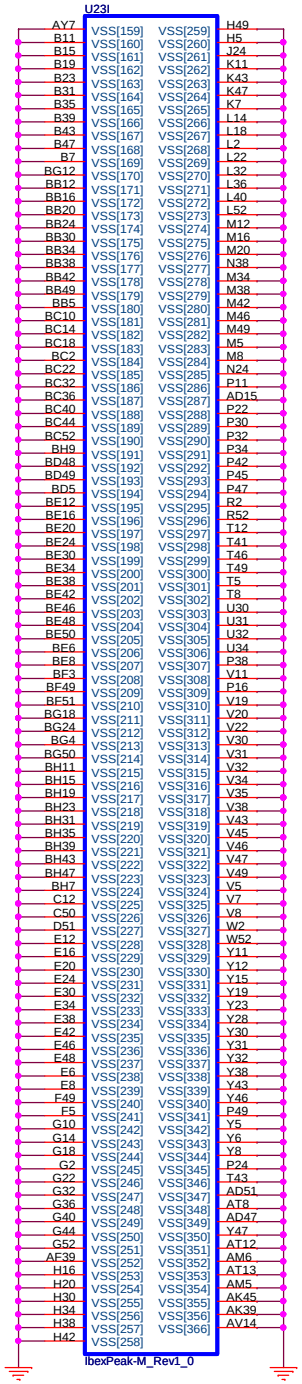
Vendor	PN
Socket	DG008000031
WINBOND	AKE39ZP0N00
MAX	AKE39FP0N00

PROJECT :AX1
Quanta Computer Inc.

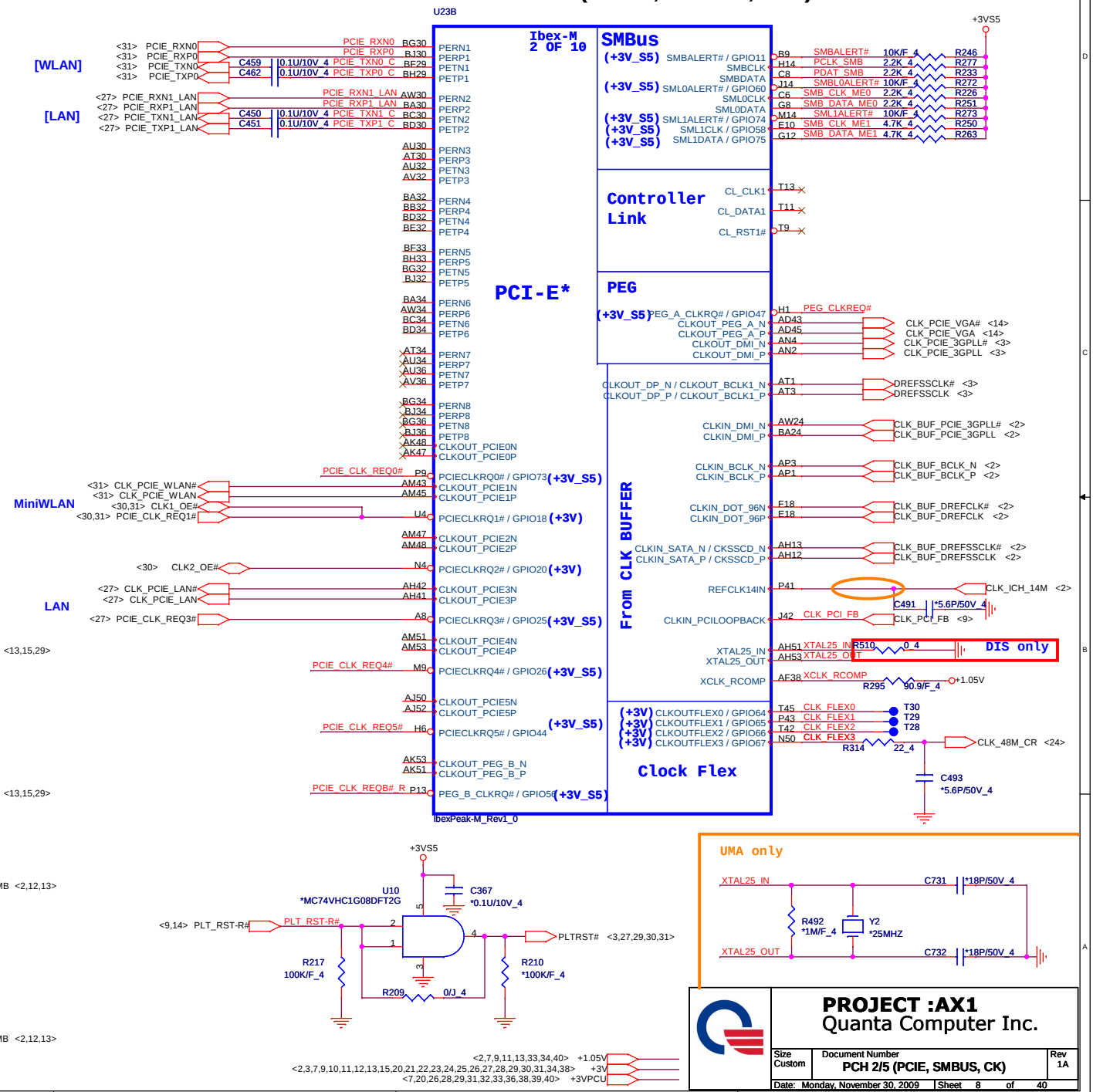
Size	Document Number	Rev
Custom	PCH 1/5 (SATA,HDA,LPC)	1A

Date: Monday, November 30, 2009 | Sheet 7 of 40

IBEX PEAK-M (GND)

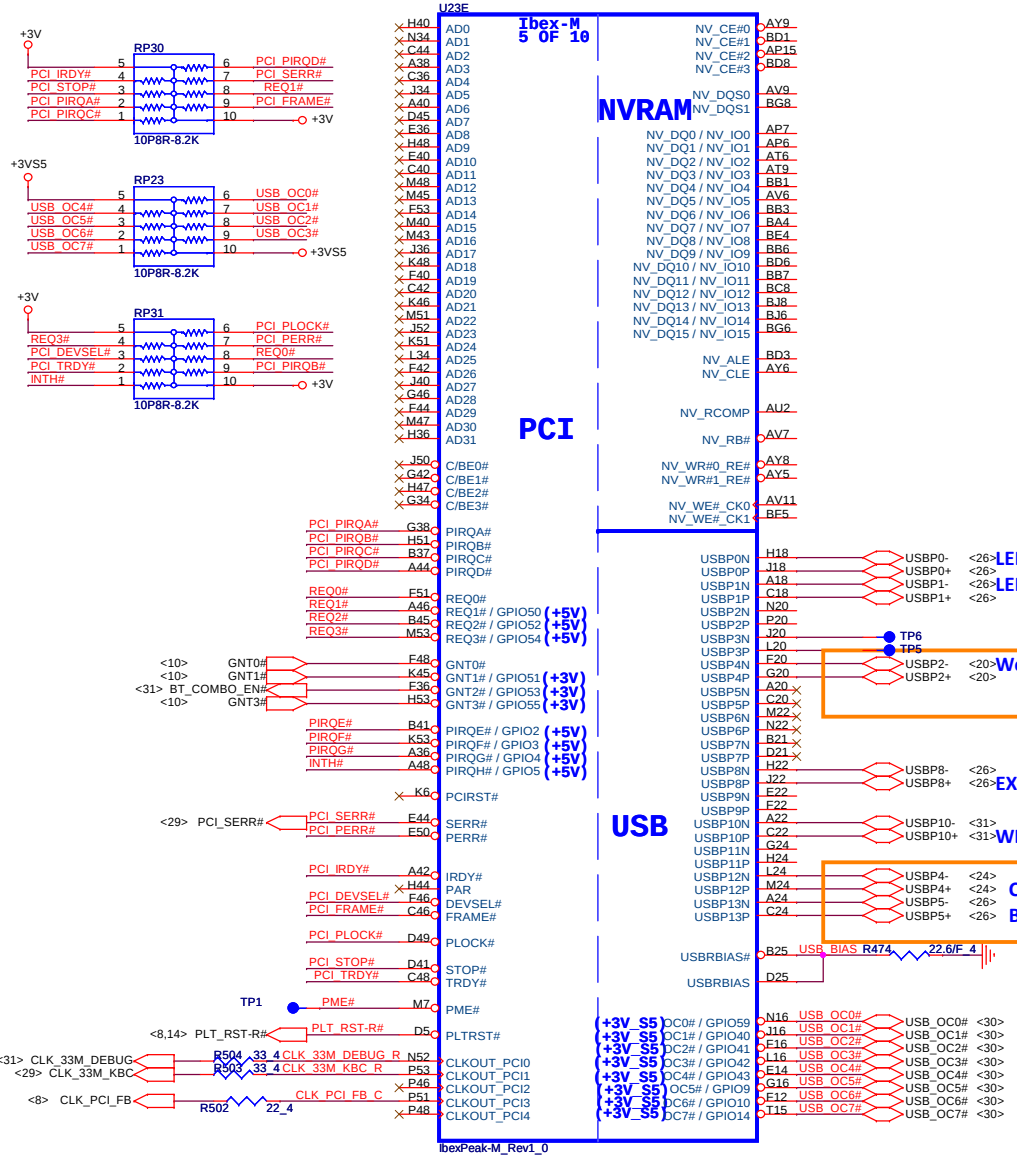


IBEX PEAK-M (PCI-E,SMBUS,CLK)

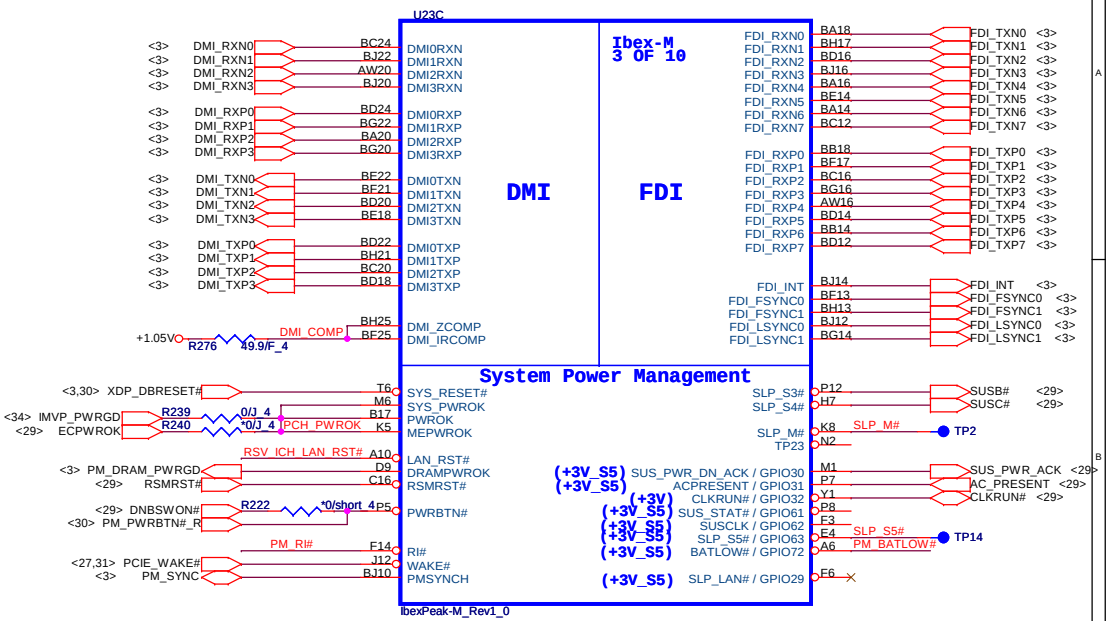


08

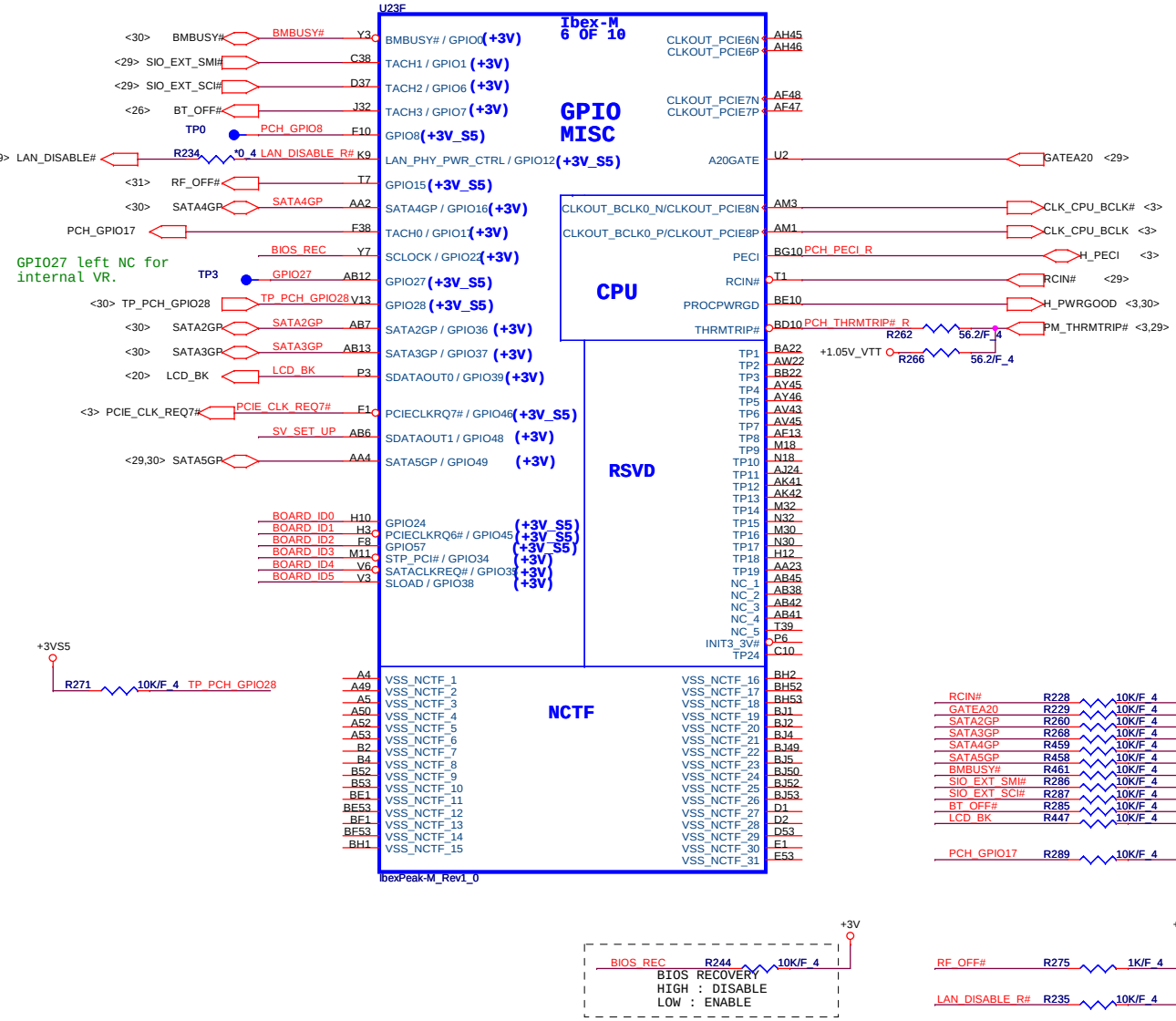
IBEX PEAK-M (PCI,USB,NVRAM)



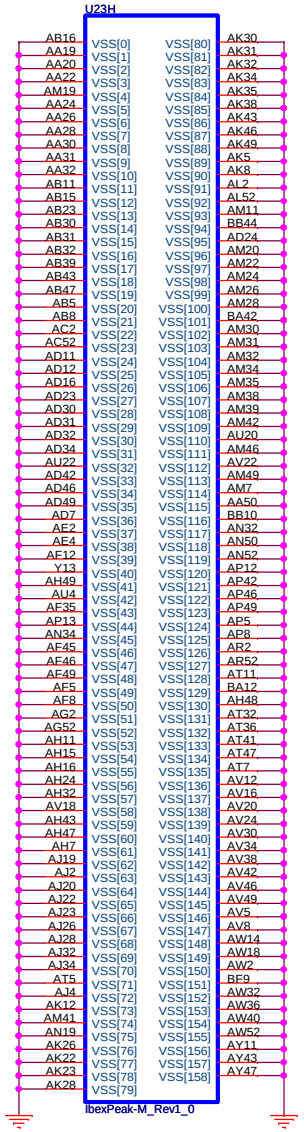
IBEX PEAK-M (DMI,FDI,GPIO)



IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



IBEX PEAK-M (GND)



10

<9> GNT3# R507 *10K_NC

A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

SV_SET_UP R259 10K/F_4 +3V

SV_SET_UP	1-X High = Strong (Default)

<9> GNT0# GNT0# R302 *1K/F_4
<9> GNT1# GNT1# R506 *1K/F_4

Boot BIOS Strap		
PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

No Reboot Strap

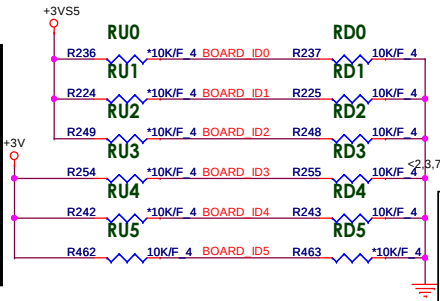
<7,25> ACZ_SPKR *1K/F_4 R466 +3V
<7,29> PCH_GPIO33 R283 *100K/F_4

<3,5,11,29,30,34,35,40> +1.05V_VTT
<5,11,33,38> +1.8V
<2,3,7,8,9,11,12,13,15,20,21,22,23,24,25,26,27,28,29,30,31,34,38> +3V
<3,8,9,11,30,38> +3VS5

BOARD ID SETTING

Board ID5: For idenify UMA and DIS
Board ID4: For idenify FF and DF
Board ID3: Reserve
Board ID2: Reserve
Board ID1: Reserve

Board ID	ID0	ID1	ID2	ID3	ID4	ID5
UMA FF	0	0	0	0	0	0
UMA DF	0	0	0	0	1	0
DIS	0	0	0	0	0	1

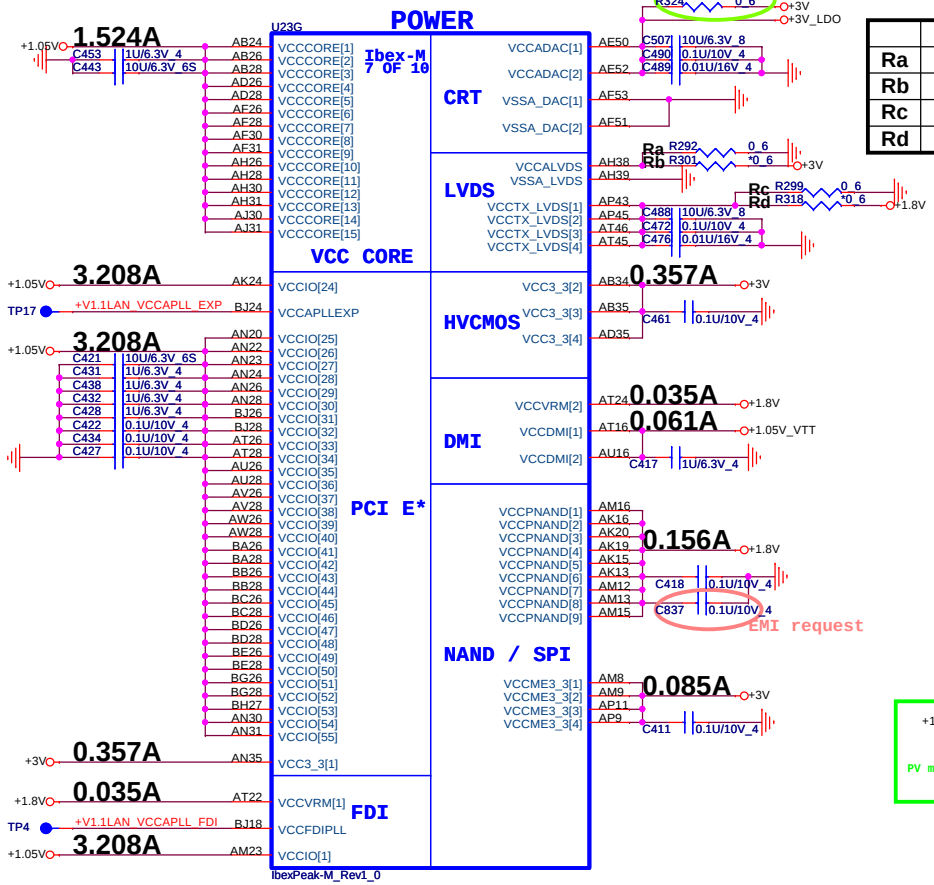


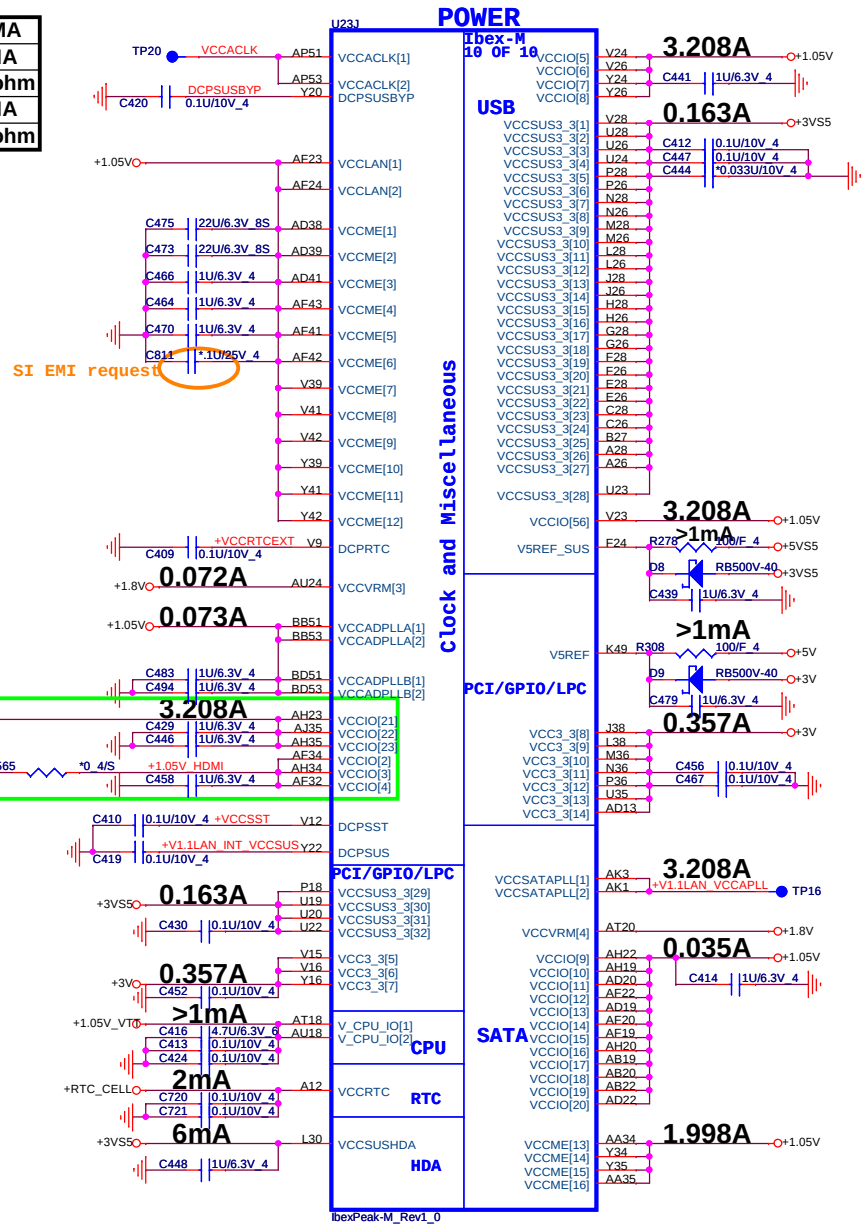
PROJECT :AX1
Quanta Computer Inc.

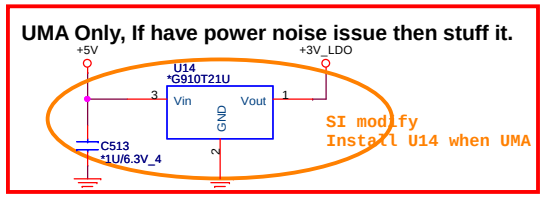
Size	Document Number	Rev
Custom	PCH 4/5 (GPIO & Strap)	1A
Date: Thursday, November 12, 2009	Sheet 10 of 40	

SI modify
Uninstall on UMA
Install on DIS

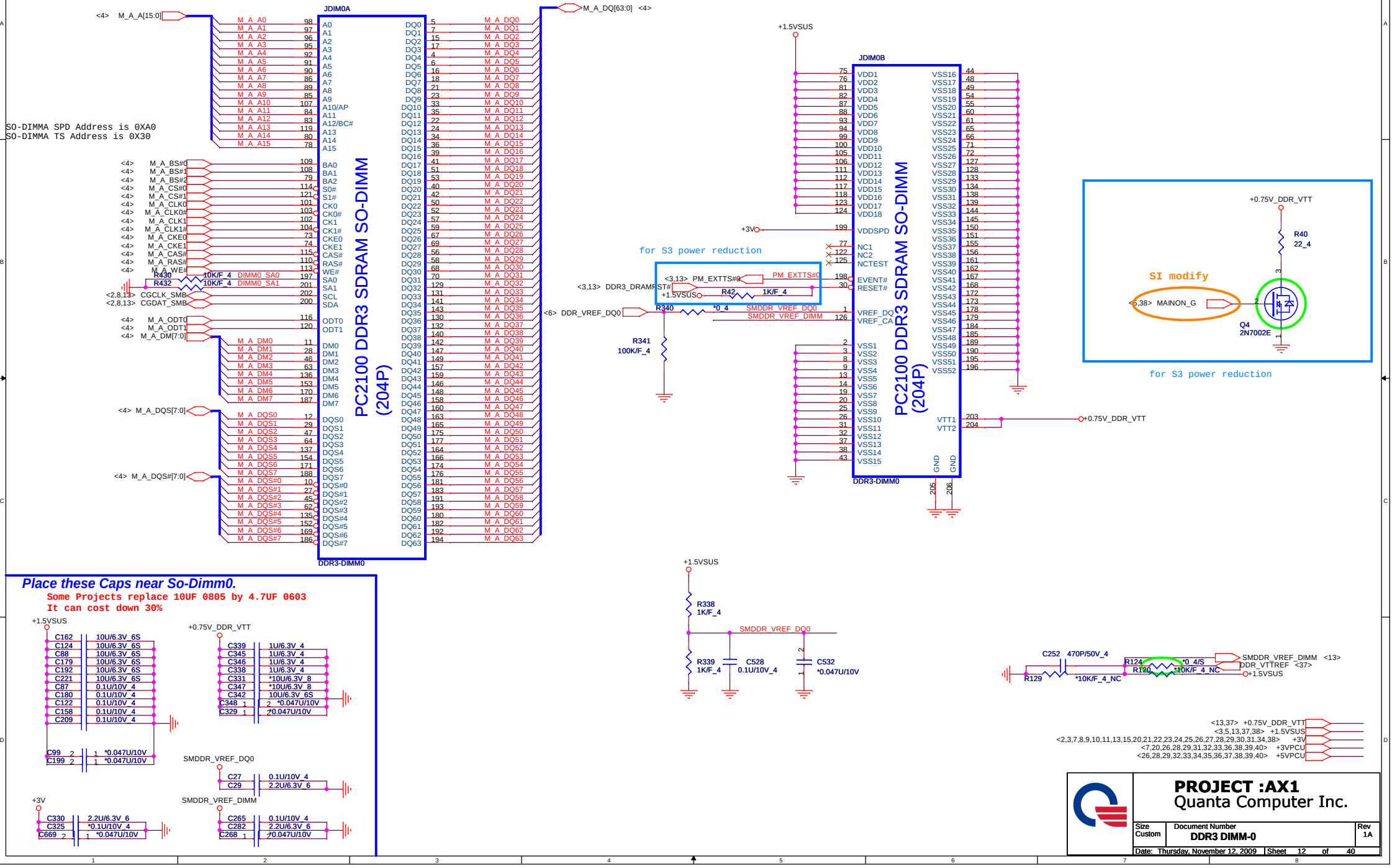
	DIS	UMA
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm

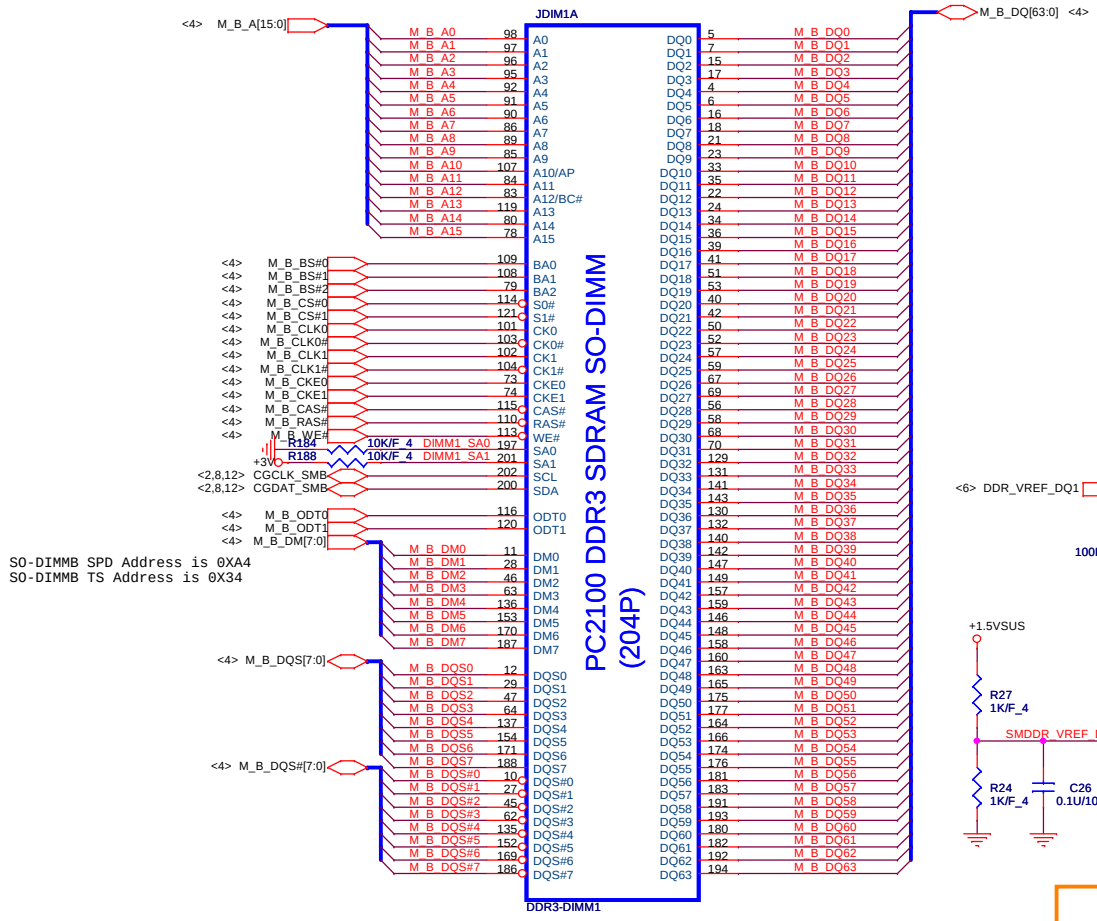


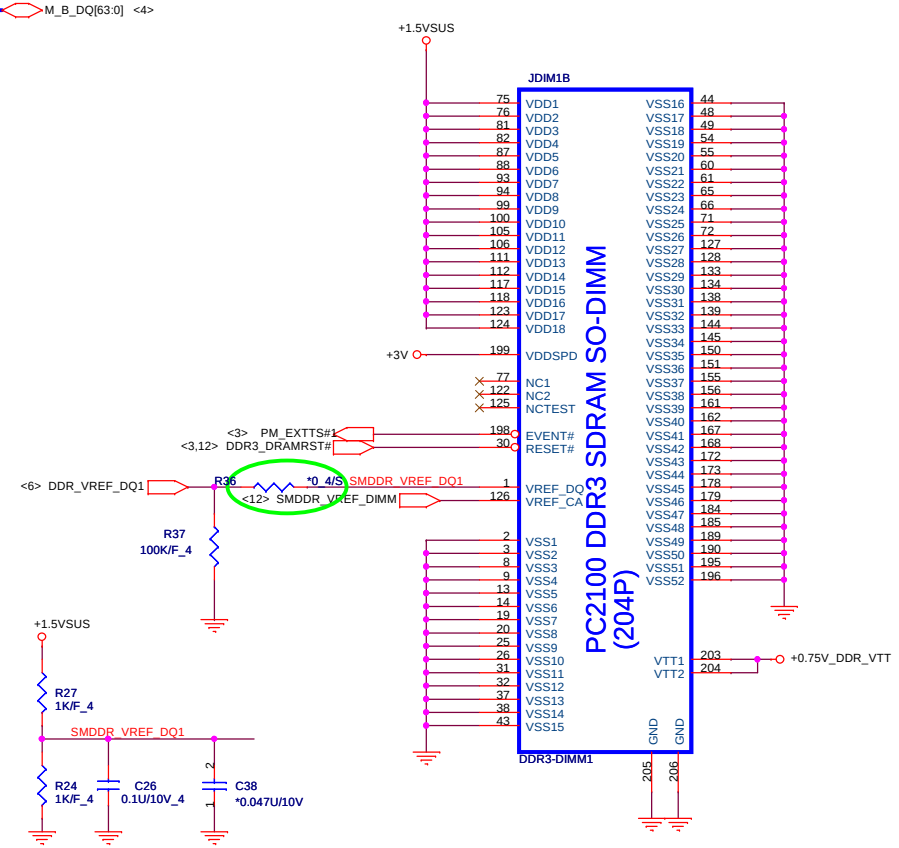


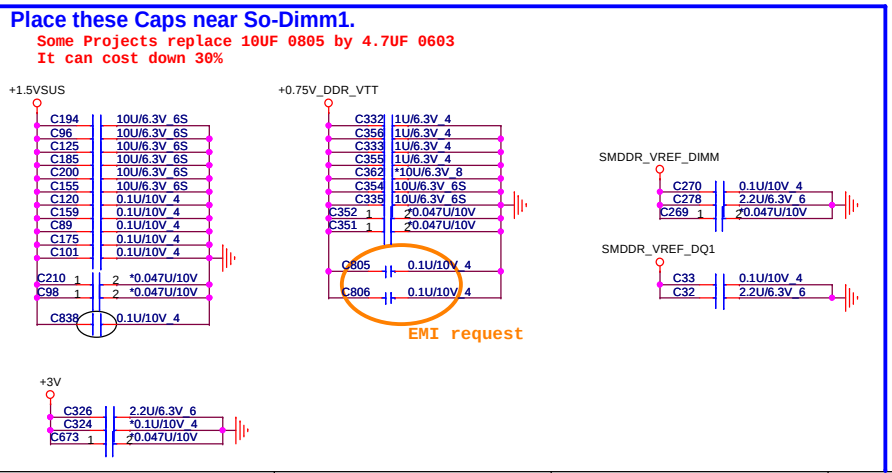


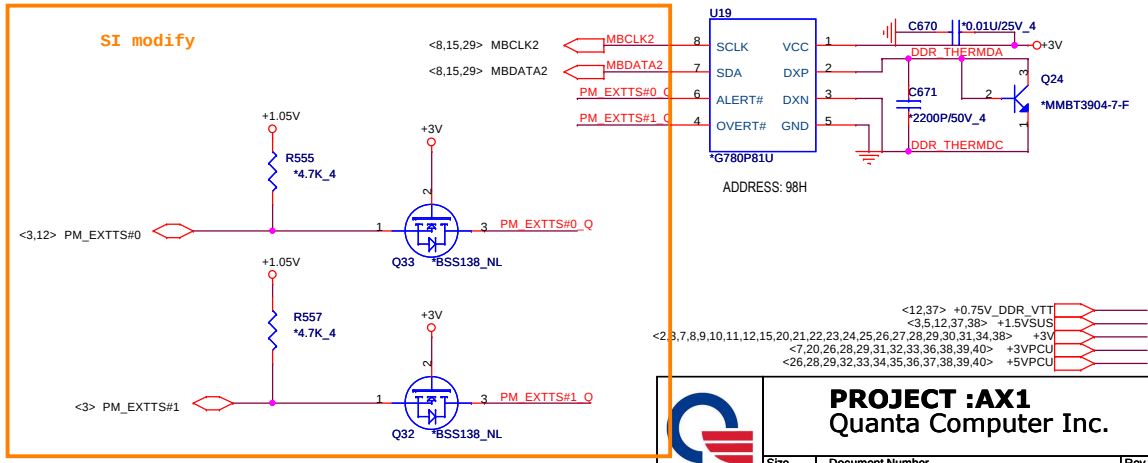
SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30




JDIM1A
PC2100 DDR3 SDRAM SO-DIMM
(204P)
DDR3-DIMM1
M_B_A[15:0]
M_B_DQ[63:0]
M_B_BS#0
M_B_BS#1
M_B_BS#2
M_B_CS#0
M_B_CS#1
M_B_CLK0
M_B_CLK0#
M_B_CLK1
M_B_CLK1#
M_B_CKE0
M_B_CKE1
M_B_CAS#
M_B_RAS#
M_B_WE#
R184 10K/F_4 DIMM1_SA0
R188 10K/F_4 DIMM1_SA1
+3V
CGCLK_SMB
CGDAT_SMB
M_B_ODT0
M_B_ODT1
M_B_DM[7:0]
M_B_DQS[7:0]
M_B_DQS#[7:0]
SO-DIMMB SPD Address is 0XA4
SO-DIMMB TS Address is 0X34


+1.5VSUS
JDIM1B
PC2100 DDR3 SDRAM SO-DIMM
(204P)
DDR3-DIMM1
+3V
PM_EXTTS#1
DDR3_DRAMRST#
DDR_VREF_DQ1
R36 *0_4/S
SMDDR_VREF_DQ1
SMDDR_VREF_DIMM
R37 100K/F_4
R27 1K/F_4
R24 1K/F_4
C26 0.1U/10V_4
C38 *0.047U/10V
+0.75V_DDR_VTT


Place these Caps near So-Dimm1.
Some Projects replace 10UF 0805 by 4.7UF 0603
It can cost down 30%
+1.5VSUS
+0.75V_DDR_VTT
SMDDR_VREF_DIMM
SMDDR_VREF_DQ1
EMI request
+3V


SI modify
MBCLK2
MBDATA2
PM_EXTTS#0_Q
PM_EXTTS#1_Q
U19
*G780P81U
ADDRESS: 98H
C670 *0.01U/25_4
C671 *2200P/50V_4
Q24 *MMBT3904-7-F
DDR_THERMDA
DDR_THERMDC
R555 *4.7K_4
R557 *4.7K_4
Q33 *BSS138_NL
Q32 *BSS138_NL
PM_EXTTS#0
PM_EXTTS#1

POWER
+PCIE_VDDR=1.2V
+VDD_MEM1.8V=1.8V
+VGA_CORE=0.9~1.2V

2.5GT/s bit rate

U17A

PCI EXPRESS INTERFACE

<3> PEG_TX15	PEG_TX15	AF30	PCIE_RX0P	PCIE_TX0P	AH30	C_PEG_RXP15 C123	0.1U/10V_4
<3> PEG_TX#15	PEG_TX#15	AE31	PCIE_RX0N	PCIE_TX0N	AG31	C_PEG_RXN15 C136	0.1U/10V_4
<3> PEG_TX14	PEG_TX14	AE29	PCIE_RX1P	PCIE_TX1P	AG29	C_PEG_RXP14 C151	0.1U/10V_4
<3> PEG_TX#14	PEG_TX#14	AD28	PCIE_RX1N	PCIE_TX1N	AF28	C_PEG_RXN14 C160	0.1U/10V_4
<3> PEG_TX13	PEG_TX13	AD30	PCIE_RX2P	PCIE_TX2P	AF27	C_PEG_RXP13 C139	0.1U/10V_4
<3> PEG_TX#13	PEG_TX#13	AC31	PCIE_RX2N	PCIE_TX2N	AF26	C_PEG_RXN13 C149	0.1U/10V_4
<3> PEG_TX12	PEG_TX12	AC29	PCIE_RX3P	PCIE_TX3P	AD27	C_PEG_RXP12 C163	0.1U/10V_4
<3> PEG_TX#12	PEG_TX#12	AB28	PCIE_RX3N	PCIE_TX3N	AD26	C_PEG_RXN12 C166	0.1U/10V_4
<3> PEG_TX11	PEG_TX11	AB30	PCIE_RX4P	PCIE_TX4P	AC25	C_PEG_RXP11 C168	0.1U/10V_4
<3> PEG_TX#11	PEG_TX#11	AA31	PCIE_RX4N	PCIE_TX4N	AC24	C_PEG_RXN11 C174	0.1U/10V_4
<3> PEG_TX10	PEG_TX10	AA29	PCIE_RX5P	PCIE_TX5P	Y23	C_PEG_RXP10 C190	0.1U/10V_4
<3> PEG_TX#10	PEG_TX#10	Y28	PCIE_RX5N	PCIE_TX5N	Y24	C_PEG_RXN10 C183	0.1U/10V_4
<3> PEG_TX9	PEG_TX9	Y30	PCIE_RX6P	PCIE_TX6P	AB27	C_PEG_RXP9 C181	0.1U/10V_4
<3> PEG_TX#9	PEG_TX#9	W31	PCIE_RX6N	PCIE_TX6N	AB26	C_PEG_RXN9 C176	0.1U/10V_4
<3> PEG_TX8	PEG_TX8	W29	PCIE_RX7P	PCIE_TX7P	W27	C_PEG_RXP8 C205	0.1U/10V_4
<3> PEG_TX#8	PEG_TX#8	V28	PCIE_RX7N	PCIE_TX7N	W26	C_PEG_RXN8 C193	0.1U/10V_4
<3> PEG_TX7	PEG_TX7	V30	PCIE_RX8P	PCIE_TX8P	V25	C_PEG_RXP7 C208	0.1U/10V_4
<3> PEG_TX#7	PEG_TX#7	U31	PCIE_RX8N	PCIE_TX8N	V24	C_PEG_RXN7 C214	0.1U/10V_4
<3> PEG_TX6	PEG_TX6	U29	PCIE_RX9P	PCIE_TX9P	V27	C_PEG_RXP6 C228	0.1U/10V_4
<3> PEG_TX#6	PEG_TX#6	T28	PCIE_RX9N	PCIE_TX9N	U26	C_PEG_RXN6 C218	0.1U/10V_4
<3> PEG_TX5	PEG_TX5	T30	PCIE_RX10P	PCIE_TX10P	U25	C_PEG_RXP5 C229	0.1U/10V_4
<3> PEG_TX#5	PEG_TX#5	R31	PCIE_RX10N	PCIE_TX10N	U24	C_PEG_RXN5 C241	0.1U/10V_4
<3> PEG_TX4	PEG_TX4	R29	PCIE_RX11P	PCIE_TX11P	T25	C_PEG_RXP4 C243	0.1U/10V_4
<3> PEG_TX#4	PEG_TX#4	P28	PCIE_RX11N	PCIE_TX11N	T27	C_PEG_RXN4 C250	0.1U/10V_4
<3> PEG_TX3	PEG_TX3	P30	PCIE_RX12P	PCIE_TX12P	R26	C_PEG_RXP3 C262	0.1U/10V_4
<3> PEG_TX#3	PEG_TX#3	N31	PCIE_RX12N	PCIE_TX12N	R24	C_PEG_RXN3 C253	0.1U/10V_4
<3> PEG_TX2	PEG_TX2	N29	PCIE_RX13P	PCIE_TX13P	P27	C_PEG_RXP2 C266	0.1U/10V_4
<3> PEG_TX#2	PEG_TX#2	M28	PCIE_RX13N	PCIE_TX13N	P26	C_PEG_RXN2 C279	0.1U/10V_4
<3> PEG_TX1	PEG_TX1	M30	PCIE_RX14P	PCIE_TX14P	P24	C_PEG_RXP1 C283	0.1U/10V_4
<3> PEG_TX#1	PEG_TX#1	L31	PCIE_RX14N	PCIE_TX14N	P23	C_PEG_RXN1 C286	0.1U/10V_4
<3> PEG_TX0	PEG_TX0	L29	PCIE_RX15P	PCIE_TX15P	M27	C_PEG_RXP0 C295	0.1U/10V_4
<3> PEG_TX#0	PEG_TX#0	K30	PCIE_RX15N	PCIE_TX15N	N26	C_PEG_RXN0 C289	0.1U/10V_4

PEG_RX15 <3>	PEG_RX#15 <3>
PEG_RX14 <3>	PEG_RX#14 <3>
PEG_RX13 <3>	PEG_RX#13 <3>
PEG_RX12 <3>	PEG_RX#12 <3>
PEG_RX11 <3>	PEG_RX#11 <3>
PEG_RX10 <3>	PEG_RX#10 <3>
PEG_RX9 <3>	PEG_RX#9 <3>
PEG_RX8 <3>	PEG_RX#8 <3>
PEG_RX7 <3>	PEG_RX#7 <3>
PEG_RX6 <3>	PEG_RX#6 <3>
PEG_RX5 <3>	PEG_RX#5 <3>
PEG_RX4 <3>	PEG_RX#4 <3>
PEG_RX3 <3>	PEG_RX#3 <3>
PEG_RX2 <3>	PEG_RX#2 <3>
PEG_RX1 <3>	PEG_RX#1 <3>
PEG_RX0 <3>	PEG_RX#0 <3>

CLOCK

<8> CLK_PCIE_VGA	AK30	PCIE_REFCLKP	
<8> CLK_PCIE_VGA#	AK32	PCIE_REFCLKN	

M93-S3--NC
PARK-S3--install
10K/F_4 R149 N10 NC_PWRGOOD

<8,9> PLT_RST-R# AL27 PERSTB

CALIBRATION

PCIE_CALRP Y22 M72_PCIE_CALRP R83 1.27K/F_4
PCIE_CALRN AA22 M72_PCIE_CALRN R82 2K/F_4 +1.1V_VGA

PARK

100MHz (+/-300ppm) input frequency,
0-0.7V single-ended swing

U17G

DP E/F POWER

+1.8V_DPE_VDD18	AG15 AG16	DPE_VDD18#1 DPE_VDD18#2
+1.1V_DPE_VDD10	AG20 AG21	DPE_VDD10#1 DPE_VDD10#2
	AG14 AH14 AM14 AM16 AM18	DPE_VSSR#1 DPE_VSSR#2 DPE_VSSR#3 DPE_VSSR#4 DPE_VSSR#5
+1.8V_DPE_VDD18	AF16 AG17	DPF_VDD18#1 DPF_VDD18#2
+1.1V_DPE_VDD10	AF22 AG22	DPF_VDD10#1 DPF_VDD10#2
	AF23 AG23 AM20 AM22 AM24	DPF_VSSR#1 DPF_VSSR#2 DPF_VSSR#3 DPF_VSSR#4 DPF_VSSR#5
R110 150/F_4 DPEF_CALR	AF17	DPEF_CALR
+1.8V_DPE_PVDD	AG18 AF19	DPE_PVDD DPE_PVSS
+1.8V_DPF_PVDD R108 *0_4/S	AG19 AF20	NC_DPF_PVDD NC_DPF_PVSS

M93-S3--NC
PARK-S3--install

DP A/B POWER

AE11 AF11	+1.8V_DPA_VDD18	NC_DPA_VDD18#1 NC_DPA_VDD18#2
AF6 AF7	+1.1V_DPB_VDD10	DPA_VDD10#1 DPA_VDD10#2
AE1 AE3 AG1 AG6 AH5		DPA_VSSR#1 DPA_VSSR#2 DPA_VSSR#3 DPA_VSSR#4 DPA_VSSR#5
AE13 AF13	+1.8V_DPA_VDD18	NC_DPB_VDD18#1 NC_DPB_VDD18#2
AF8 AF9	+1.1V_DPB_VDD10	DPB_VDD10#1 DPB_VDD10#2
AF10 AG9 AH8 AM6 AM8		DPB_VSSR#1 DPB_VSSR#2 DPB_VSSR#3 DPB_VSSR#4 DPB_VSSR#5
AE10 DPAB_CALR R88 150/F_4		DPAB_CALR
AG8 AG7	+1.8V_DPA_PVDD	DPA_PVDD DPA_PVSS
AG10 AG11	+1.8V_DPA_PVDD	DPB_PVDD DPB_PVSS

DP PLL POWER

PARK

BLM18PG181SN1D(180,1.5A)_6
L46 +1.1V_DPB_VDD10 +1.1V_VGA 1.1V(S100,D200mA)
C632 0.1U/10V_4 C634 10U/6.3V_6S C633 1U/10V_4

(Park-S3:110mA@1.0V)
(M9X-S2/S3:200mA@1.1V)

+1.1V_DPE_VDD10 +1.1V_DPE_VDD10 L20 +1.1V_VGA
C137 0.1U/10V_4 C127 1U/10V_4 C107 10U/6.3V_6S
BLM18PG181SN1D(180,1.5A)_6

1.8V -(300mA)
+1.8V_DPE_VDD18 L21 +1.8V_VGA
C140 0.1U/10V_4 C128 1U/10V_4 C135 10U/6.3V_6S
BLM18PG181SN1D(180,1.5A)_6

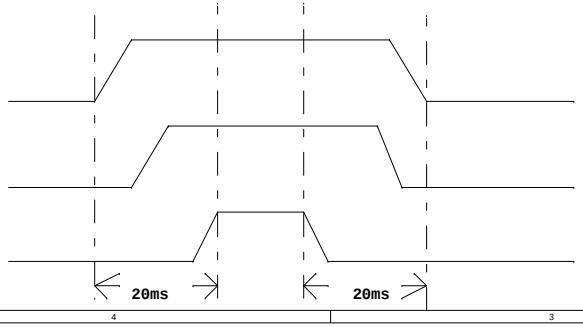
+1.8V_DPF_PVDD +1.8V_DPF_PVDD L43 1.8V(20mA) +1.8V_VGA
C606 0.1U/10V_4 C608 1U/10V_4 C596 10U/6.3V_6S
BLM18PG181SN1D(180,1.5A)_6
Reserve for PARK

Reserve for PARK
+1.8V_DPA_VDD18 +1.8V_DPA_VDD18 L18 1.8V(130mA) +1.8V_VGA
C100 0.1U/10V_4 C119 1U/10V_4 C97 10U/6.3V_6S
BLM18PG181SN1D(180,1.5A)_6

+1.8V_DPA_PVDD +1.8V_DPA_PVDD L47 1.8V(20mA) +1.8V_VGA
C629 0.1U/10V_4 C628 1U/10V_4 C626 10U/6.3V_6S
BLM18PG181SN1D(180,1.5A)_6

+1.8V_DPE_PVDD +1.8V_DPE_PVDD L16 1.8V(20mA) +1.8V_VGA
C85 0.1U/10V_4 C83 1U/10V_4 C79 10U/6.3V_6S
BLM18PG181SN1D(180,1.5A)_6

VGA Core	BPP
VGA Core	VDDC
+1.8V	PCIE_VDDR
+1.8V	PCIE_PVDD
+1.8V	VDDR1
+3V_VGA	VDDR3



PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	M93_PCIE_Interface	1A

Date: Thursday, November 12, 2009 Sheet 14 of 40

MEM_ID[3:0]	Vendor	Type	Vendor P/N
0000	Samsung (E die)	64*16-800MHZ	K4W1G1646E-HC12
0001	Hynix	64*16 -800MHZ	H5TQ1G63BFR-12C

	PWRCNTL1	PWRCNTL0	V-CORE
L	0	0	0.9V
M	0	1	0.95V
H	1	0	1.05V
TBD	1	1	NA

U17B

M93-S3/M92-S2

Memory ID

DVO

DPA

DPB

DPC

I2C

GENERAL PURPOSE I/O

DAC1

DAC2

M92-S2/M93-S3

PLL/CLOCK

DDC/AUX

THERMAL

PARK

Reserve for PARK

For M93-S3: Use 150 Ohms Pull Down
For M92-S2: Use 0R to VDDR4
For Park-S3: NC

GPIO22(ROMCS#)
PD without external VBIOS ROM

0916: AMD modify

Need check again

1.8V(120mADPLL_PVDD)

1.1V(300mA DPLL_VDDC)

1.8V(20mA TSVDD)

For Int Clk 27Mhz

CL=20PF

Thermal Sensor

I2C ADDRESS: 9AH

PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	M93_MAIN	1A

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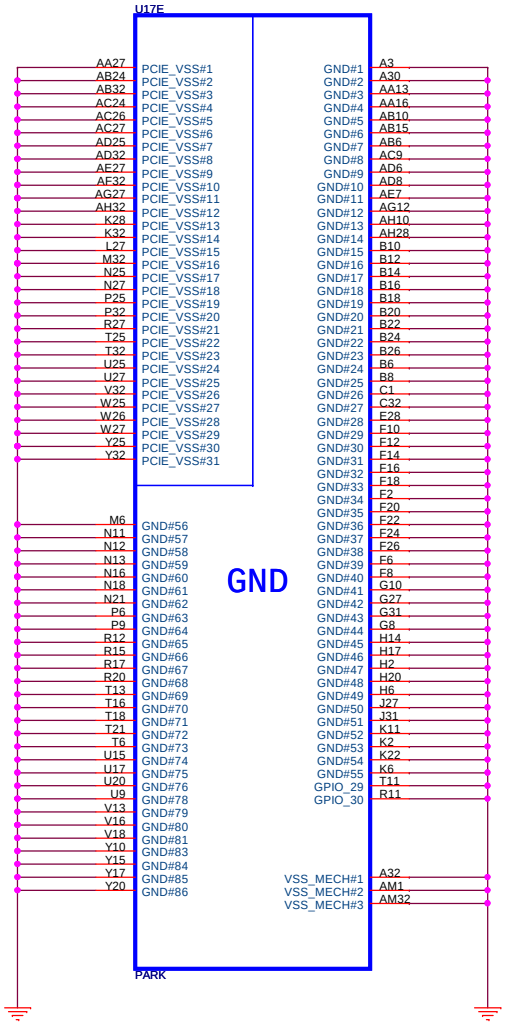
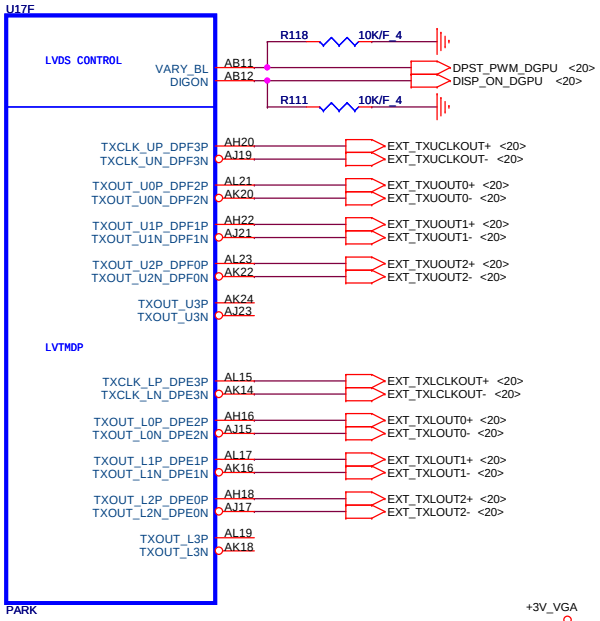
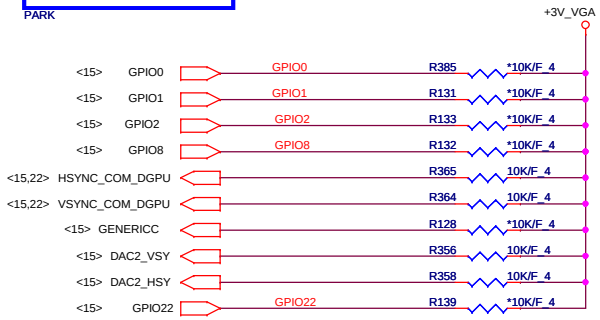
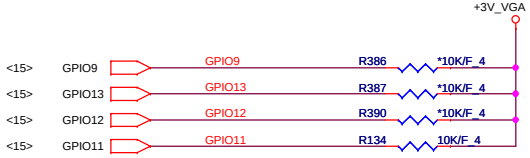
w/s 10 / 10









CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	**Transmitter Power Savings Enable** 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	**PCI Express Transmitter De-emphasis Enable** 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPIO2	Enable CLKREQ# Power Management 0 - CLKREQ# power management capability is disabled 1 - CLKREQ# power management capability is enabled	0
RSVD BIF_VGA_DIS RSVD	GPIO8 GPIO9 GPIO21	VGA ENABLED	0 0 0
BIOS_ROM_EN ROMIDCFG(2:0) VIP_DEVICE_STRAP_ENA	GPIO_22_ROMCSB GPIO[13:11] V2SYNC	ENABLE EXTERNAL BIOS ROM SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT IGNORE VIP DEVICE STRAPS	0 0 0 1 0
RSVD AUD[1] AUD[0]	GENERICC HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO21_BB_EN

Memory Aperture size

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

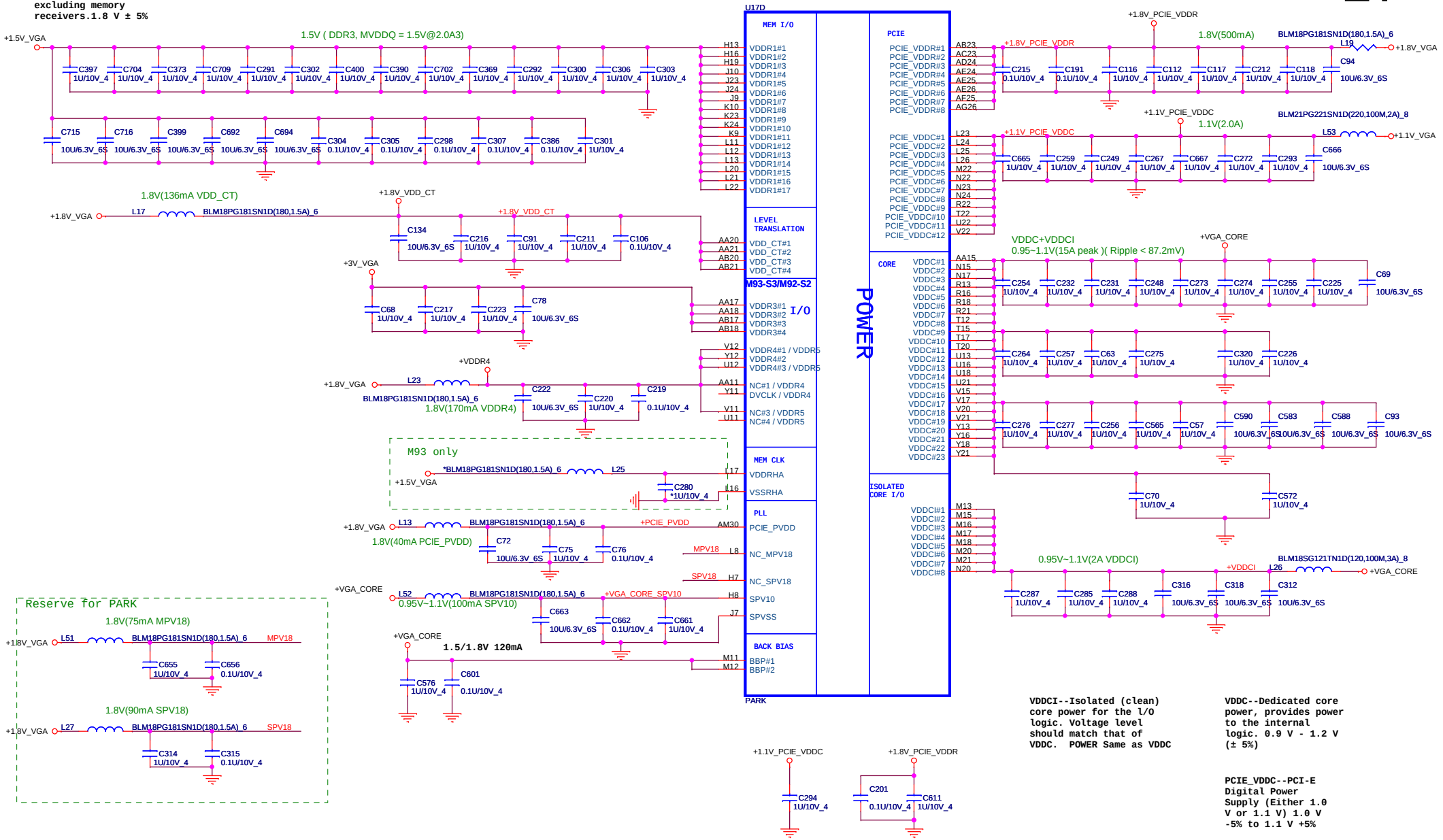
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.

PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	M93_GND / LVDS /Straps	1A
Date: Thursday, November 12, 2009	Sheet 16 of 40	

VDD_CT -- Level translation between core and I/O, excluding memory receivers.1.8 V ± 5%

PCIE_VDDR--PCI-E I/O power. 1.8 V ± 5%



VDDCI--Isolated (clean) core power for the l/O logic. Voltage level should match that of VDDC. POWER Same as VDDC

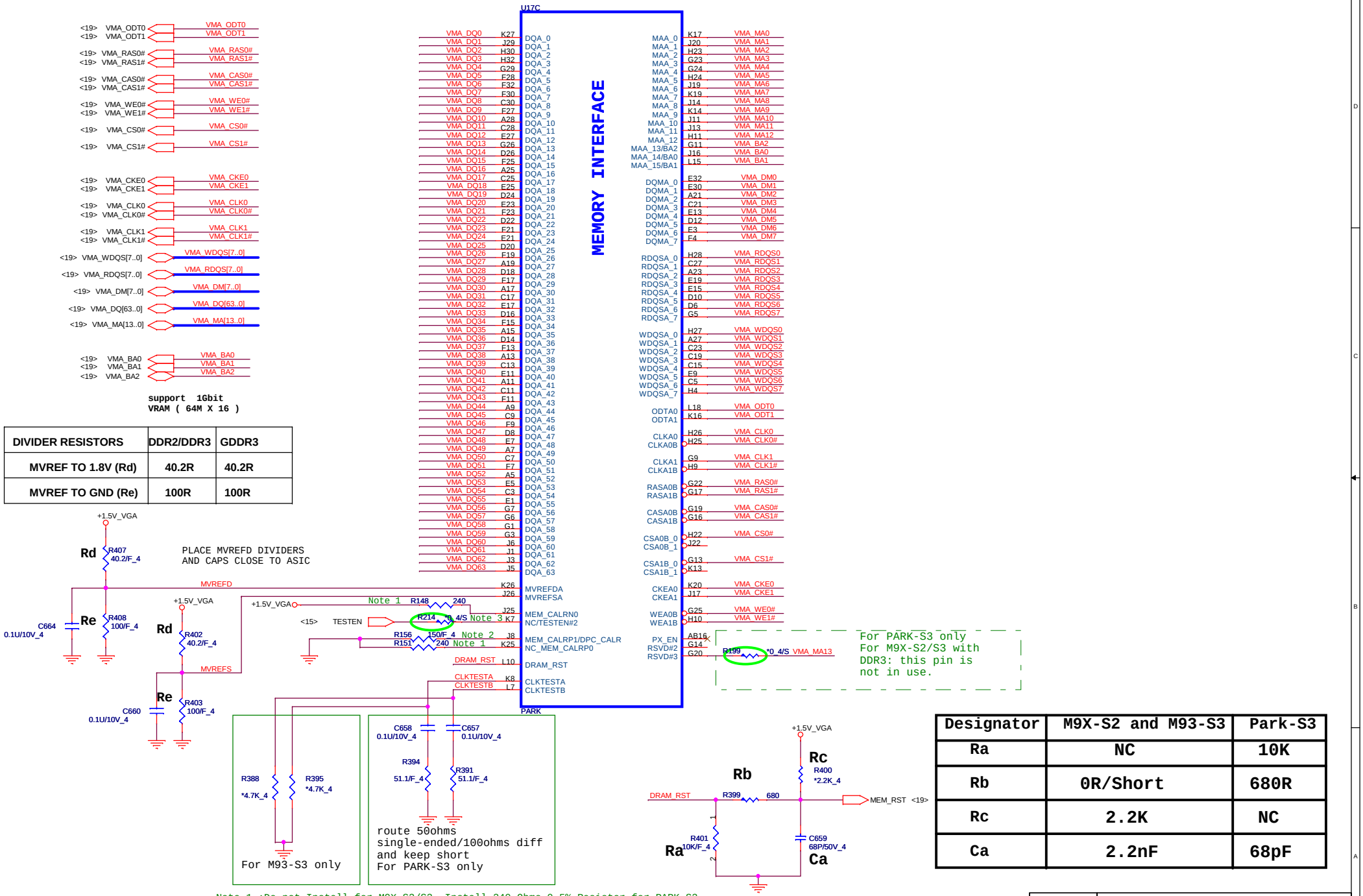
VDDC--Dedicated core power, provides power to the internal logic. 0.9 V - 1.2 V (± 5%)

PCIE_VDDC--PCI-E Digital Power Supply (Either 1.0 V or 1.1 V) 1.0 V -5% to 1.1 V +5%

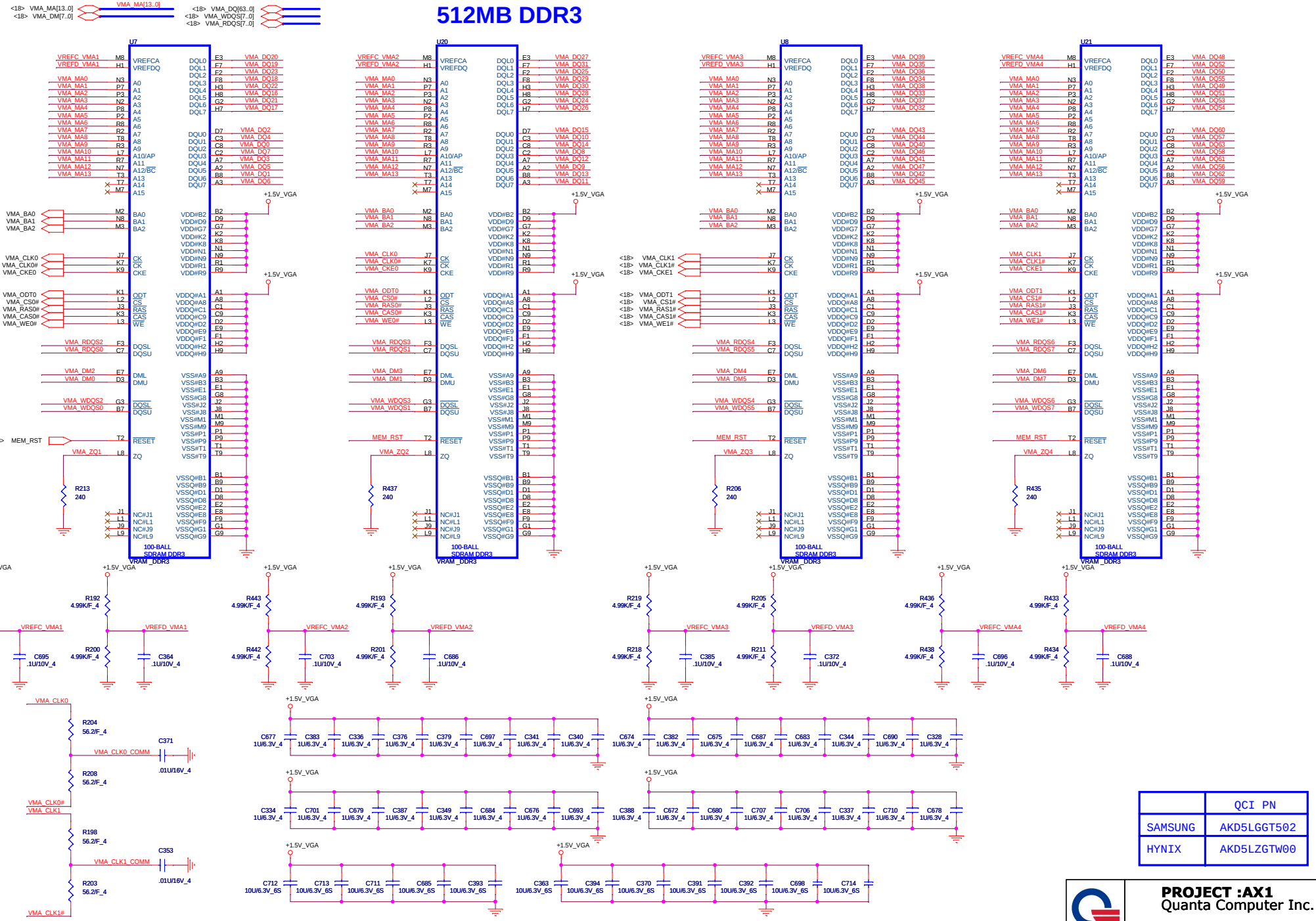
PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	M93_Power_and_NC	1A

Date: Tuesday, November 10, 2009 | Sheet 17 of 40


U17C
MEMORY INTERFACE
DQA_0
DQA_1
DQA_2
DQA_3
DQA_4
DQA_5
DQA_6
DQA_7
DQA_8
DQA_9
DQA_10
DQA_11
DQA_12
DQA_13
DQA_14
DQA_15
DQA_16
DQA_17
DQA_18
DQA_19
DQA_20
DQA_21
DQA_22
DQA_23
DQA_24
DQA_25
DQA_26
DQA_27
DQA_28
DQA_29
DQA_30
DQA_31
DQA_32
DQA_33
DQA_34
DQA_35
DQA_36
DQA_37
DQA_38
DQA_39
DQA_40
DQA_41
DQA_42
DQA_43
DQA_44
DQA_45
DQA_46
DQA_47
DQA_48
DQA_49
DQA_50
DQA_51
DQA_52
DQA_53
DQA_54
DQA_55
DQA_56
DQA_57
DQA_58
DQA_59
DQA_60
DQA_61
DQA_62
DQA_63
MVREFDA
MVREFSA
MEM_CALRN0
NC/TESTEN#2
MEM_CALRP1/DPC_CALR
NC_MEM_CALRP0
DRAM_RST
CLKTESTA
CLKTESTB
PARK
MAA_0
MAA_1
MAA_2
MAA_3
MAA_4
MAA_5
MAA_6
MAA_7
MAA_8
MAA_9
MAA_10
MAA_11
MAA_12
MAA_13/BA2
MAA_14/BA0
MAA_15/BA1
DQMA_0
DQMA_1
DQMA_2
DQMA_3
DQMA_4
DQMA_5
DQMA_6
DQMA_7
RDQSA_0
RDQSA_1
RDQSA_2
RDQSA_3
RDQSA_4
RDQSA_5
RDQSA_6
RDQSA_7
WDQSA_0
WDQSA_1
WDQSA_2
WDQSA_3
WDQSA_4
WDQSA_5
WDQSA_6
WDQSA_7
ODTA0
ODTA1
CLKA0
CLKA0B
CLKA1
CLKA1B
RASA0B
RASA1B
CASA0B
CASA1B
CSA0B_0
CSA0B_1
CSA1B_0
CSA1B_1
CKEA0
CKEA1
WEA0B
WEA1B
PX_EN
RSVD#2
RSVD#3
VMA_ODT0
VMA_ODT1
VMA_RAS0#
VMA_RAS1#
VMA_CAS0#
VMA_CAS1#
VMA_WE0#
VMA_WE1#
VMA_CS0#
VMA_CS1#
VMA_CKE0
VMA_CKE1
VMA_CLK0
VMA_CLK0#
VMA_CLK1
VMA_CLK1#
VMA_WDQS[7..0]
VMA_RDQS[7..0]
VMA_DM[7..0]
VMA_DQ[63..0]
VMA_MA[13..0]
VMA_BA0
VMA_BA1
VMA_BA2
support 1Gbit
VRAM (64M X 16)
DIVIDER RESISTORS
DDR2/DDR3
GDDR3
MVREF TO 1.8V (Rd)
40.2R
40.2R
MVREF TO GND (Re)
100R
100R
+1.5V_VGA
Rd
R407
40.2/F_4
PLACE MVREFD DIVIDERS
AND CAPS CLOSE TO ASIC
MVREFD
Re
R408
100/F_4
C664
0.1U/10V_4
Rd
R402
40.2/F_4
MVREFS
Re
R403
100/F_4
C660
0.1U/10V_4
Note 1
R148
240
R214
*0_4/S
Note 3
TESTEN
R156
150/F_4
Note 2
R151
240
Note 1
DRAM_RST
CLKTESTA
CLKTESTB
R388
*4.7K_4
R395
*4.7K_4
For M93-S3 only
C658
0.1U/10V_4
C657
0.1U/10V_4
R394
51.1/F_4
R391
51.1/F_4
route 50ohms
single-ended/100ohms diff
and keep short
For PARK-S3 only
R199
*0_4/S
VMA_MA13
For PARK-S3 only
For M9X-S2/S3 with
DDR3: this pin is
not in use.
Rb
Rc
R400
*2.2K_4
DRAM_RST
R399
680
MEM_RST
Ra
R401
10K/F_4
C659
68P/50V_4
Ca
Designator
M9X-S2 and M93-S3
Park-S3
Ra
NC
10K
Rb
0R/Short
680R
Rc
2.2K
NC
Ca
2.2nF
68pF
Note 1 :Do not Install for M9X-S2/S3, Install 240 Ohms 0.5% Resistor for PARK-S3.
Note 2 :For M9X-S2/S3,J8 Pin Connect to VSS through 240 Ohms(0.5%) resistor.
For Park-S3,J8 Pin Connect to VSS through 150 Ohms(1%) resistor for DPC_CALR
Note 3 :For M9X-92/93, K7 Pin (NC_MEM_CALRP1) is Not connected.
For PARK-S3, K7 Pin (TESTEN#2) connect to TEST_EN Signal At AF24
PROJECT :AX1
Quanta Computer Inc.
Size
Custom
Document Number
M93_MEM_Interface
Rev
1A
Date: Thursday, November 12, 2009
Sheet 18 of 40

512MB DDR3



	QCI PN
SAMSUNG	AKD5LGGT502
HYNIX	AKD5LZGTW00

PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	M93/VRAM_A0,A1	1A

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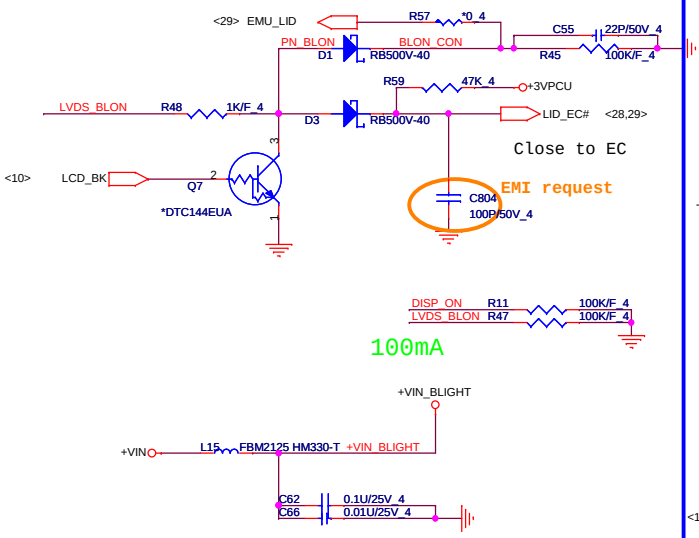
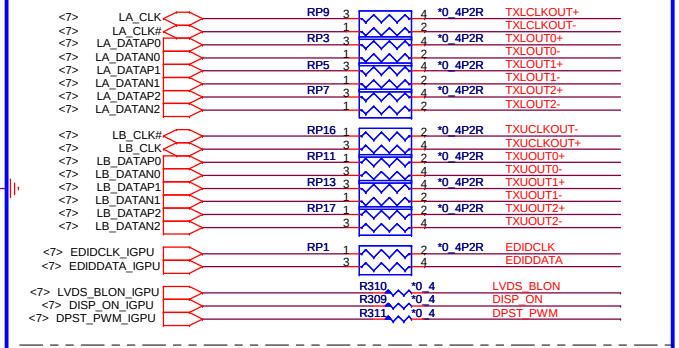
LID Switch

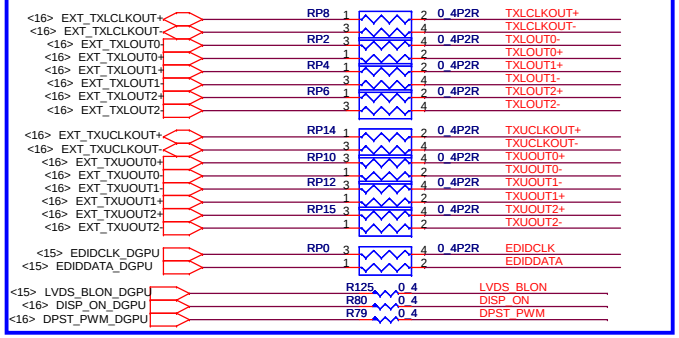


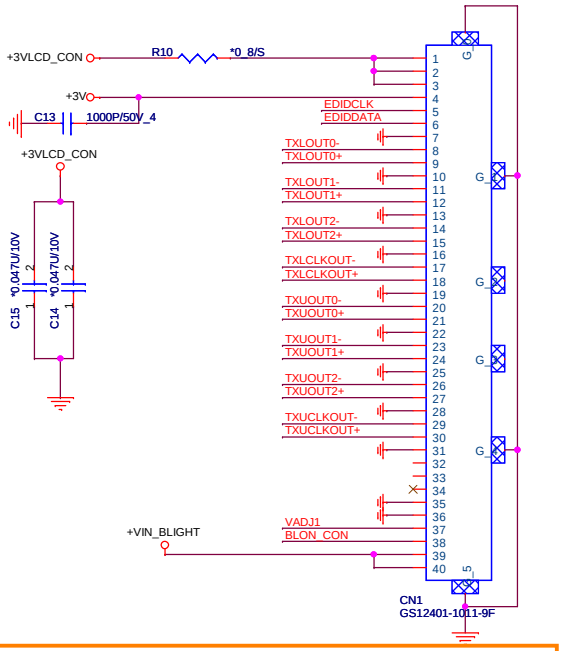
1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near PCH, then place these series Resistors near PCH

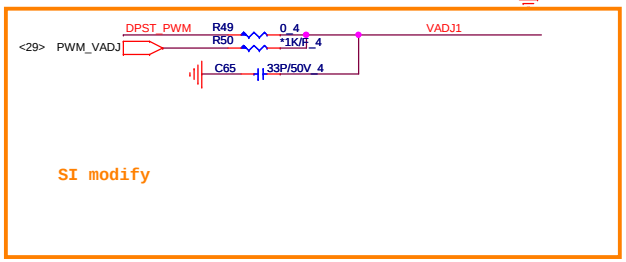
OPTION SIGNAL FROM PCH FOR UMA VGA



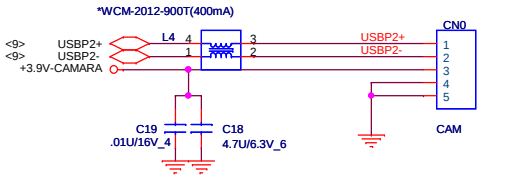
OPTION SIGNAL FROM ATI M93 to VGA

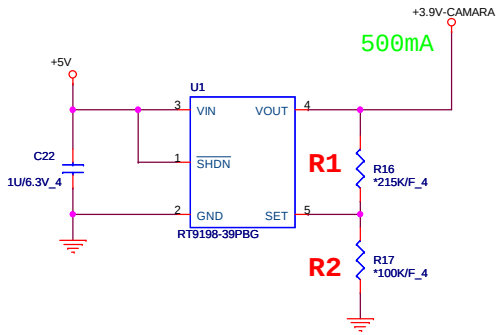


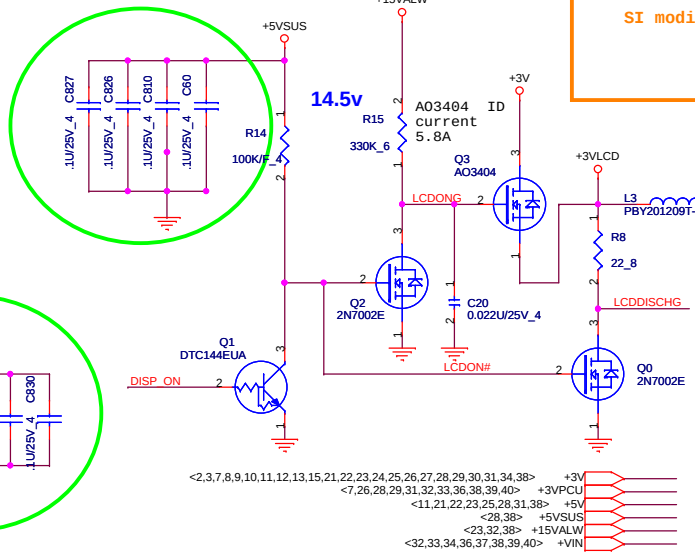




CAMERA







PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A
Date: Thursday, November 12, 2009	Sheet 20 of 40	

Signals		PDT	CHR	PIM
PC1	Ra	NC	NC	NC
HDMI_CFG0	Rb	NC	NC	NC
HDMI_CFG1	Rc	4.7K	NC	NC
REXT	Rd	499	1.2K	4.7K
PC1	Re	NC	4.7K	4.7K
HDMI_OE#	Rf	NC	4.7K	NC
PC0	Rg	4.7K	4.7K	4.7K

9/16 : PIM: need use ALP411LS000 or ALP411LS004 for capella

CHR : need Na R1182, add R1027 for capella

Vendor:PDT P/N:AL008101000
Vendor:CHR P/N:AL007318002
Vendor:PIM P/N:ALP411LS004

PV2 modify, close to U5

For UMA HDMI function

PV EMI change PN to CX601T02125

EMI FCM1608KF-601T02

PV EMI request

U5 *PS8101

POWER / CONTROL / GND

EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V

FOR UMA ONLY
FROM LEVEL SHIFTER

FOR DISCRETE ONLY
FROM M93/PARK

PLACE CLOSE HDMI CONN

FOR DISCRETE ONLY

SI modify

DISCRETE HDMI I2C SELECT
Close to HDMI Connector

FOR DISCRETE ONLY

UMA & DISCRETEHDMI HPD SENSE

UMA use +3V for the detect pin
Dis use +3V_VGA for the detect pin

reserved for EMI

CN20 HDMI CONN DFHD19MR017

PROJECT	:AX1
Quanta Computer Inc.	
Size	Custom
Document Number	HDMI CONN
Rev	1A
Date:	Monday, November 16, 2009
Sheet	21 of 40

CRT PORT

1A

FUSE1A6V_POLY

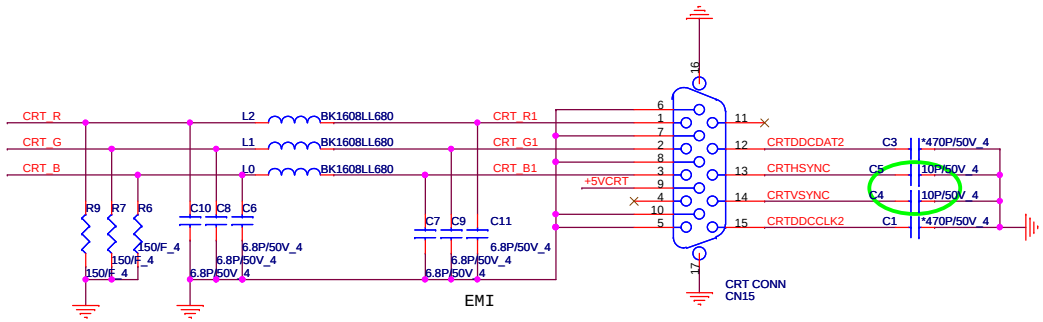
40 MIL

40 mils F0

+5V 2 1 +5VCRT +5VCRT

C0 0.1U/10V_4

SSM14 spec is 40V 1A

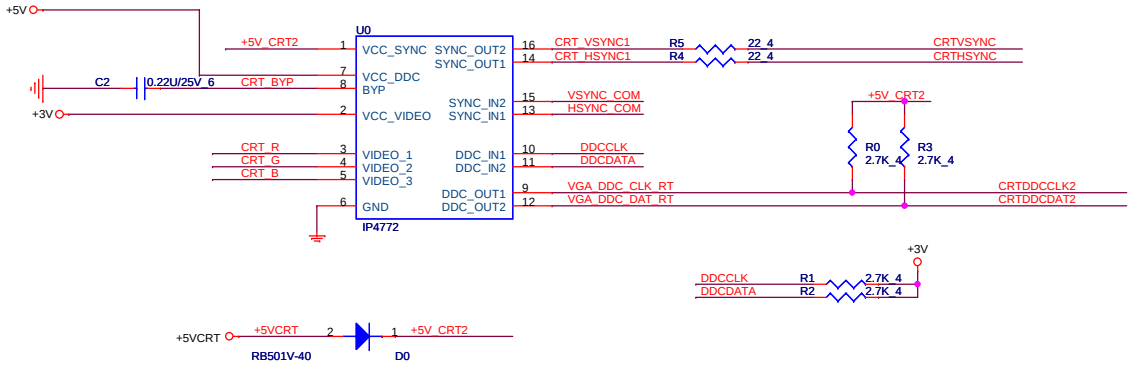


FOR UMA

<7> CRT_R_IGPU — R23 *0_4 — CRT_R
<7> CRT_G_IGPU — R26 *0_4 — CRT_G
<7> CRT_B_IGPU — R29 *0_4 — CRT_B
<7> HSYNC_COM_IGPU — R21 *0_4 — HSYNC_COM
<7> VSYNC_COM_IGPU — R19 *0_4 — VSYNC_COM
<7> DDCCLK_IGPU — R32 *0_4 — DDCCLK
<7> DDCDATA_IGPU — R35 *0_4 — DDCDATA

FOR DISCRETE

<15> CRT_R_DGPU — R22 0_4 — CRT_R
<15> CRT_G_DGPU — R25 0_4 — CRT_G
<15> CRT_B_DGPU — R28 0_4 — CRT_B
<15,16> HSYNC_COM_DGPU — R20 0_4 — HSYNC_COM
<15,16> VSYNC_COM_DGPU — R18 0_4 — VSYNC_COM
<15> DDCCLK_DGPU — R31 0_4 — DDCCLK
<15> DDCDATA_DGPU — R34 0_4 — DDCDATA

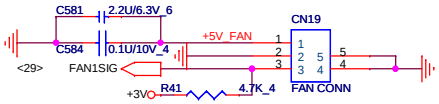


PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT	1A

Date: Thursday, December 03, 2009 Sheet 22 of 40

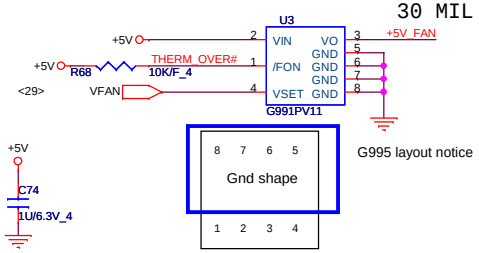
CPU FAN



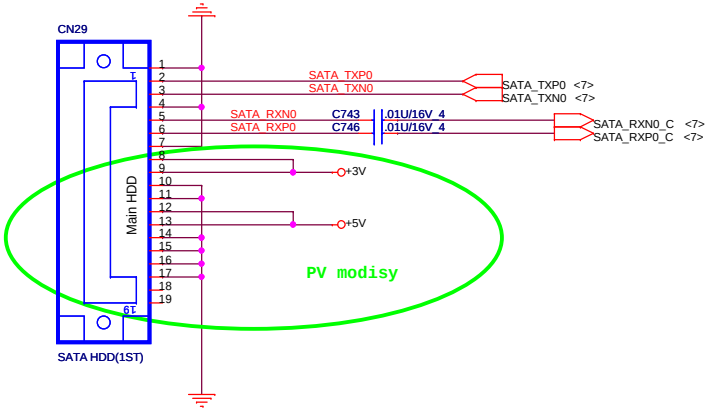
DFHD03MR008

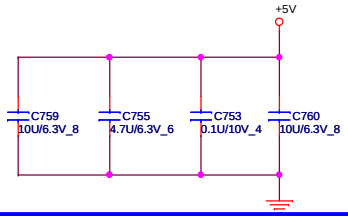
FANPWR = 1.6*VSET

30 MIL

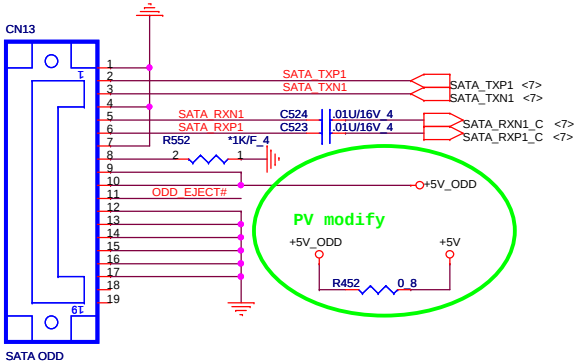


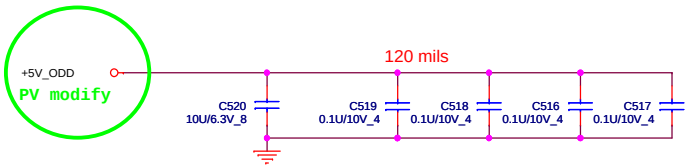
SATA HDD CONNECTOR



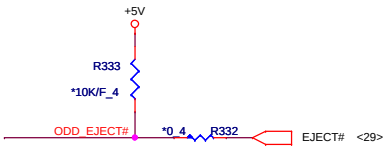


SATA ODD CONNECTOR

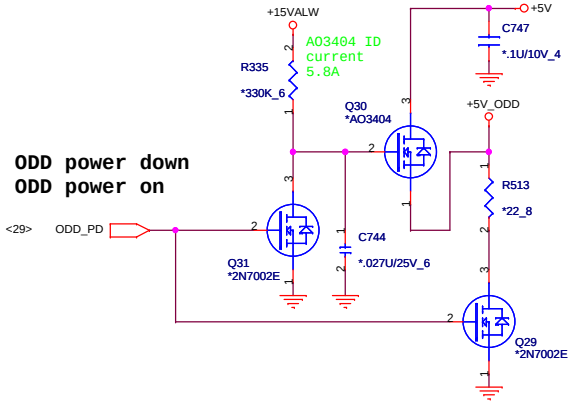




SI Add



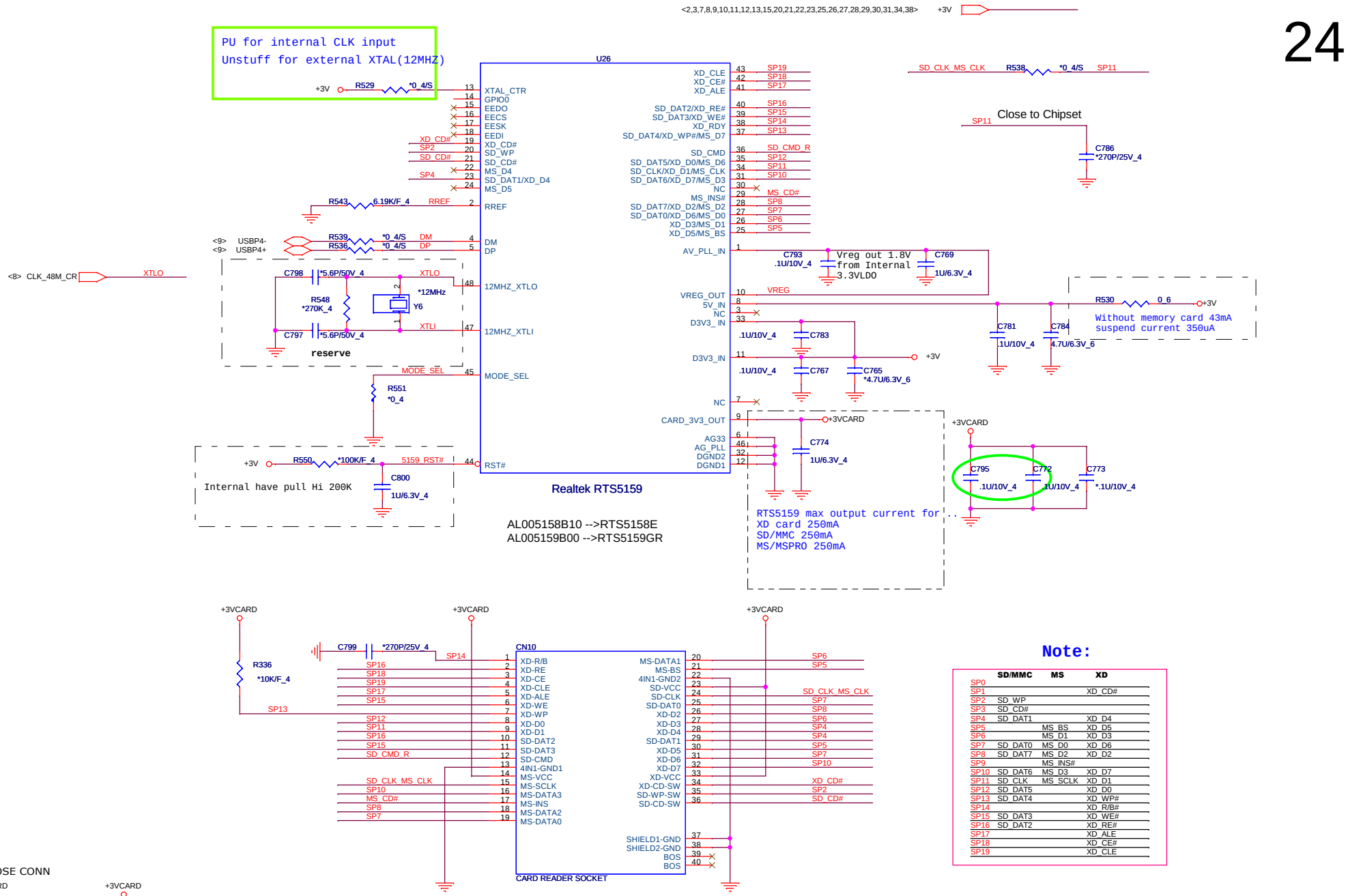
High : ODD power down
Low : ODD power on

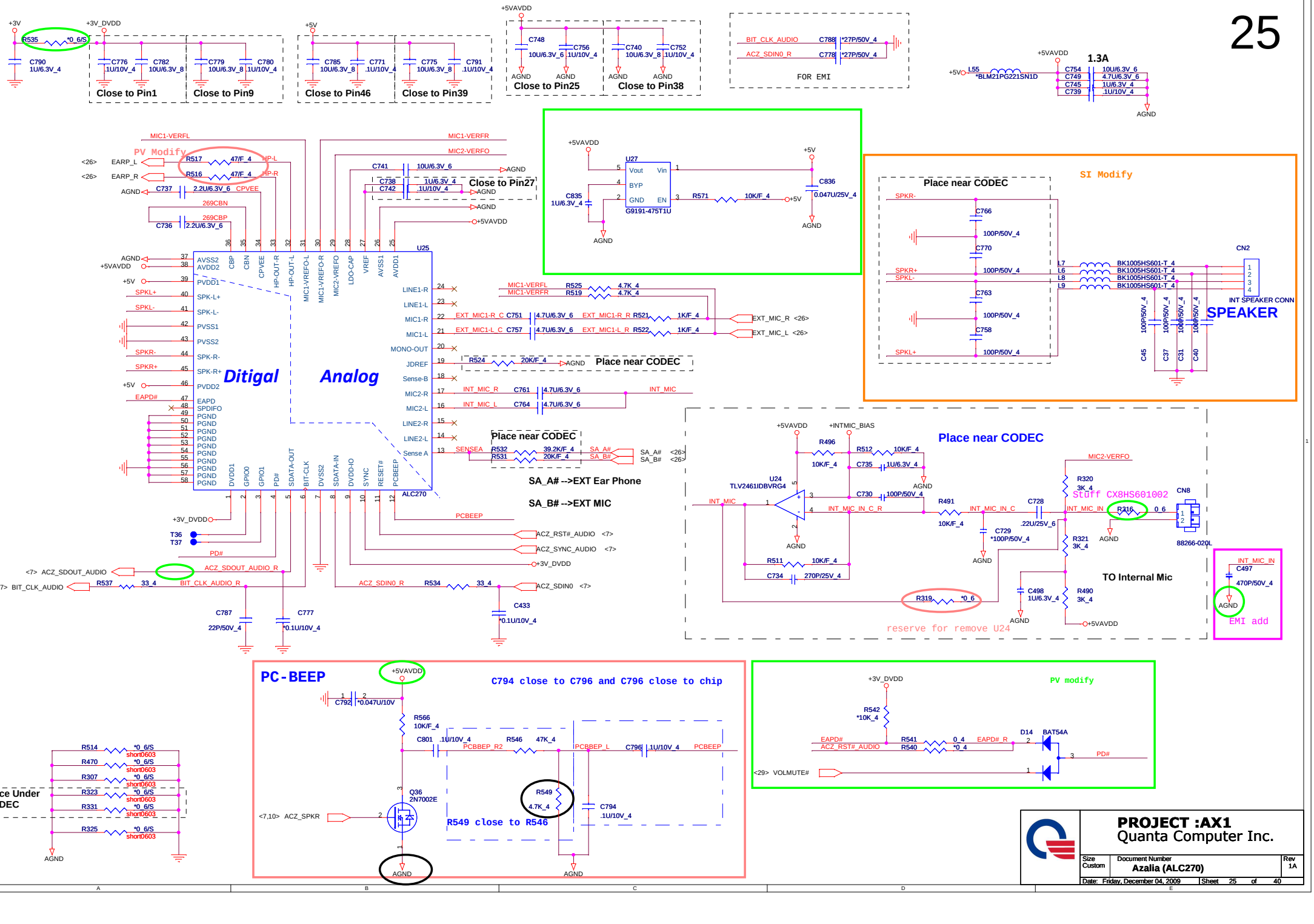


PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDD/ODD/FAN	1A

Date: Thursday, November 12, 2009 | Sheet 23 of 40


PU for internal CLK input
Unstuff for external XTAL(12MHZ)
U26
Realtek RTS5159
AL005158B10 -->RTS5158E
AL005159B00 -->RTS5159GR
RTS5159 max output current for ..
XD card 250mA
SD/MMC 250mA
MS/MSPRO 250mA
Close to Chipset
Vreg out 1.8V
from Internal
3.3VLDO
Without memory card 43mA
suspend current 350uA
Internal have pull Hi 200K
reserve
CN10
CARD READER SOCKET
5 IN1 CARD-READER (PUSH-PUSH)
Support SD/SD PRO/MMC/MS/MS PRO/xD Cards
CLOSE CONN
Note:
SD/MMC MS XD
SP0
SP1 XD_CD#
SP2 SD_WP
SP3 SD_CD#
SP4 SD_DAT1 XD_D4
SP5 MS_BS XD_D5
SP6 MS_D1 XD_D3
SP7 SD_DAT0 MS_D0 XD_D6
SP8 SD_DAT7 MS_D2 XD_D2
SP9 MS_INS#
SP10 SD_DAT6 MS_D3 XD_D7
SP11 SD_CLK MS_SCLK XD_D1
SP12 SD_DAT5 XD_D0
SP13 SD_DAT4 XD_WP#
SP14 XD_R/B#
SP15 SD_DAT3 XD_WE#
SP16 SD_DAT2 XD_RE#
SP17 XD_ALE
SP18 XD_CE#
SP19 XD_CLE



PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia (ALC270)	1A

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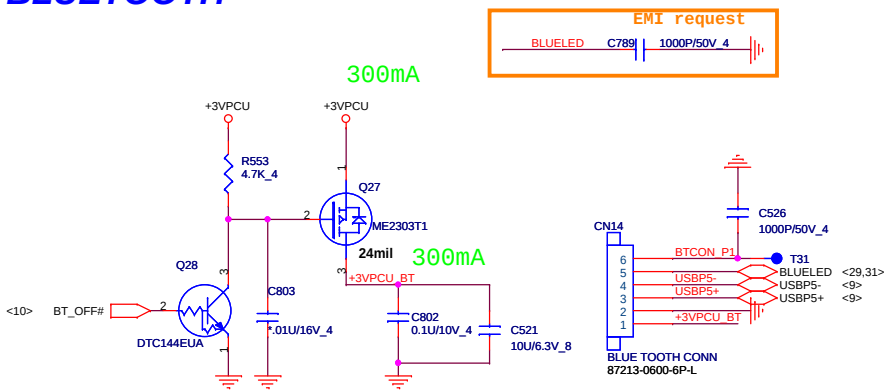
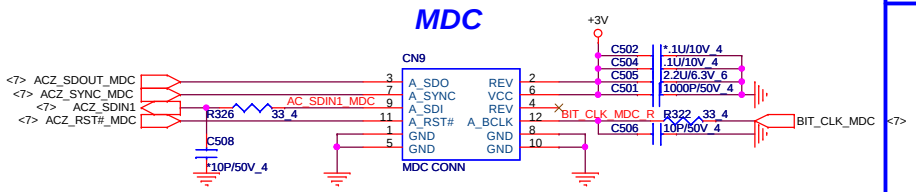
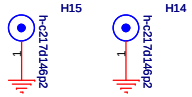
BLUETOOTH



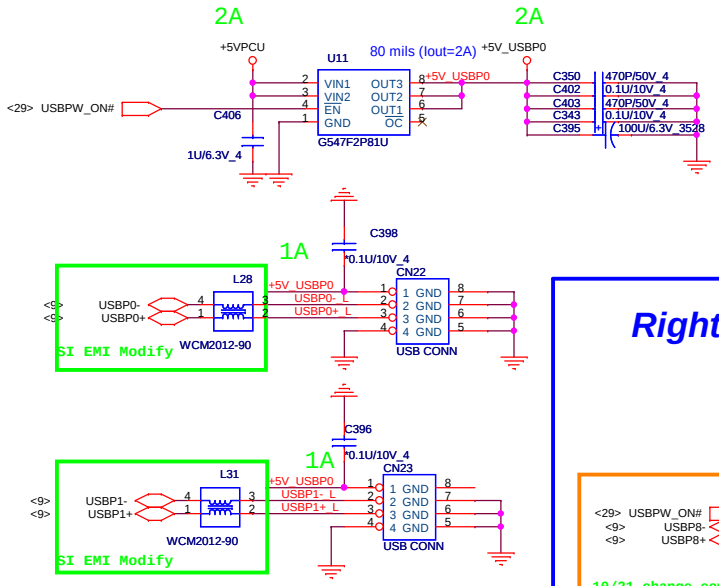
Modem CONN



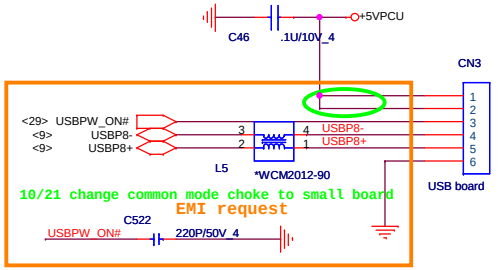


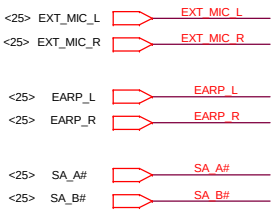
Nut PN:MBCA6002013

LEFT SIDE USBX1



Right SIDE USBX1

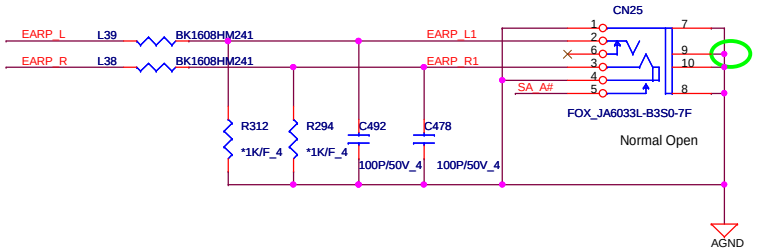




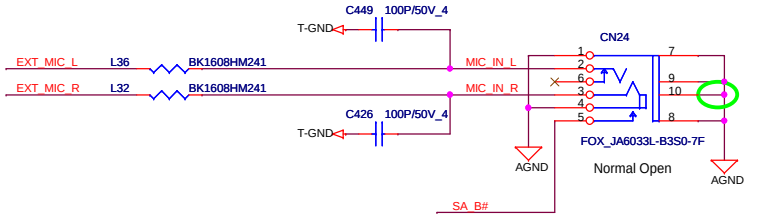
SA_A# -->EXT Ear Phone

SA_B# -->EXT MIC

Line out

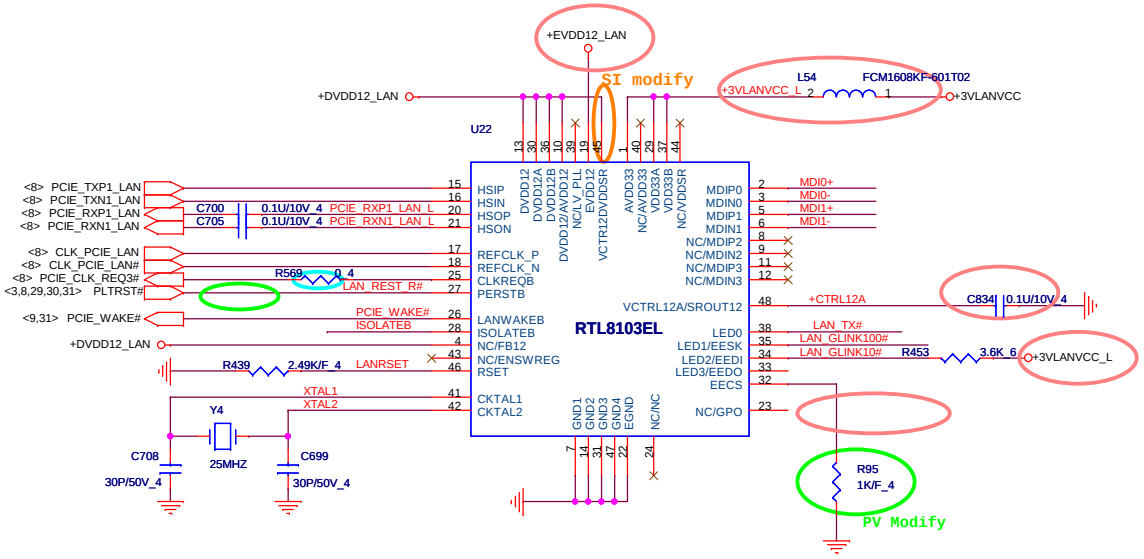


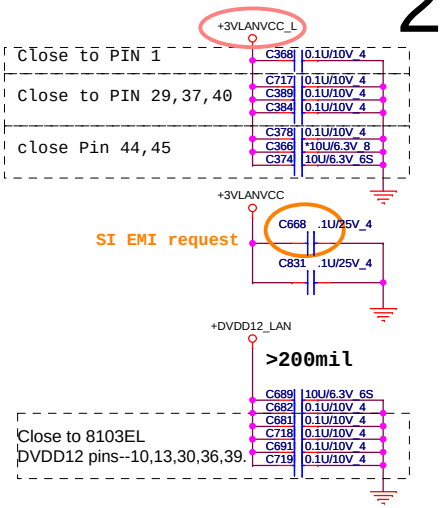
MIC

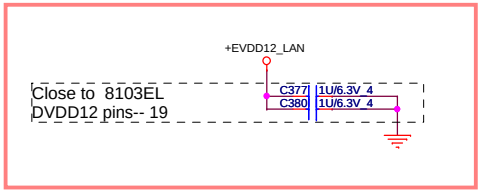


PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB/BT/Modem/Audio JacK	1A
Date: Monday, November 30, 2009	Sheet 26 of 40	

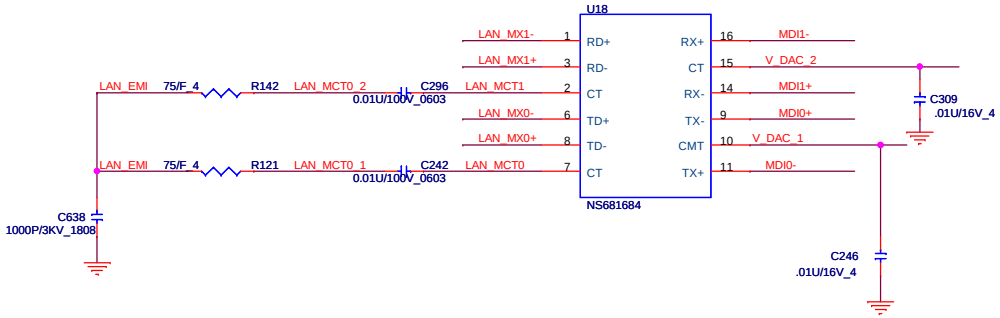


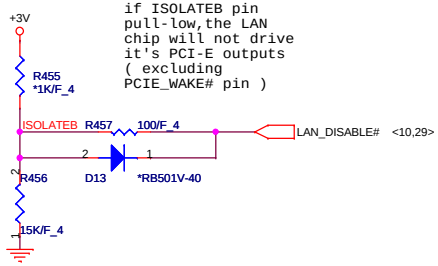




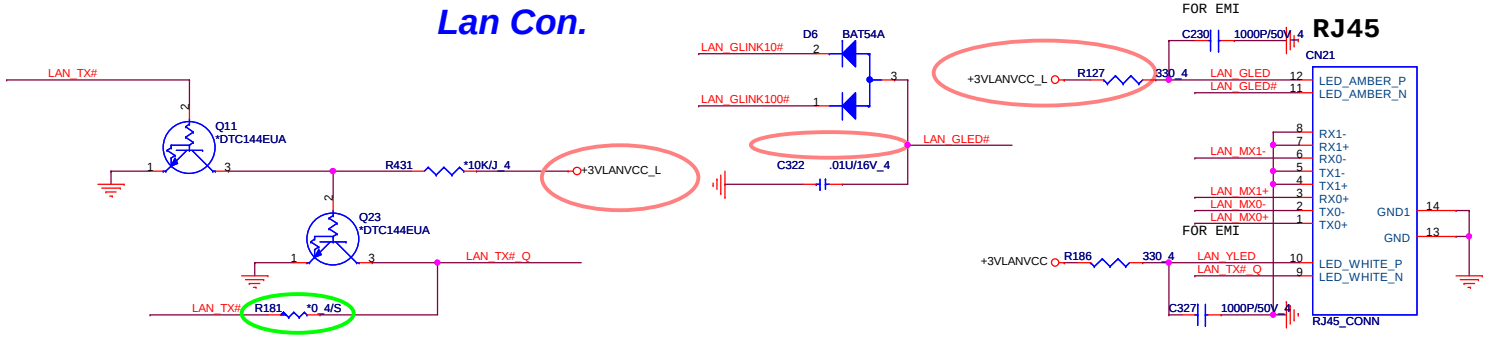
Transformer for 10/100

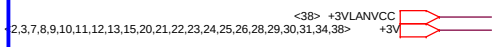
PV modify





Lan Con.





PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL8111DL/8103EL	1A

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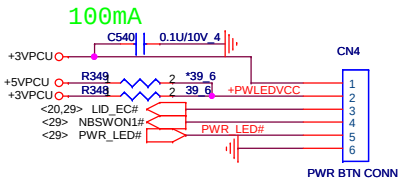
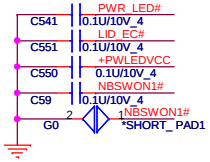
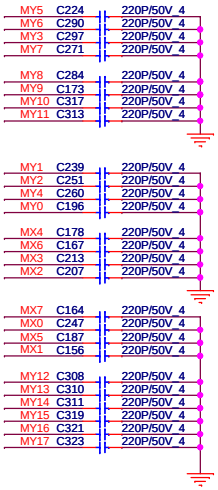
POWER BOTTON CONNECT

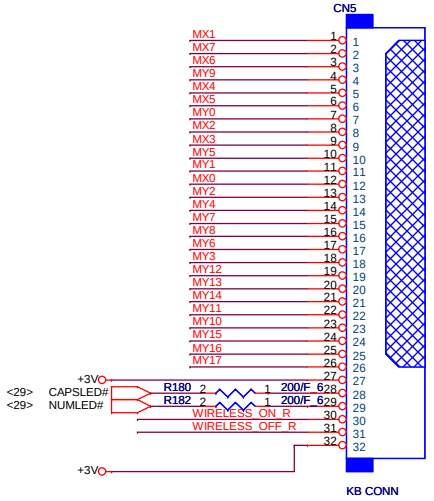


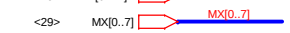
1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND



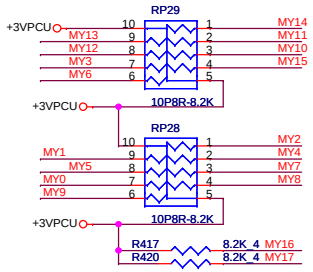
KEYBOARD Con.



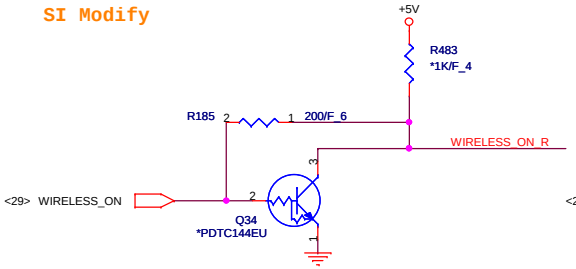


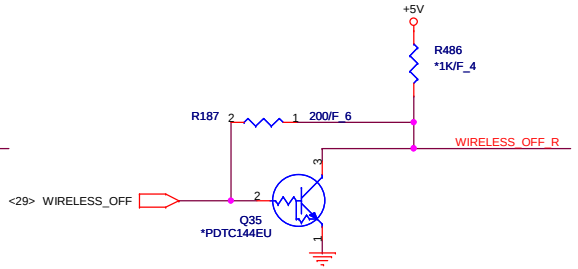


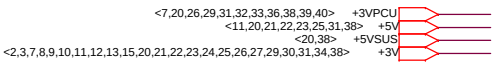
KEYBOARD PULL-UP



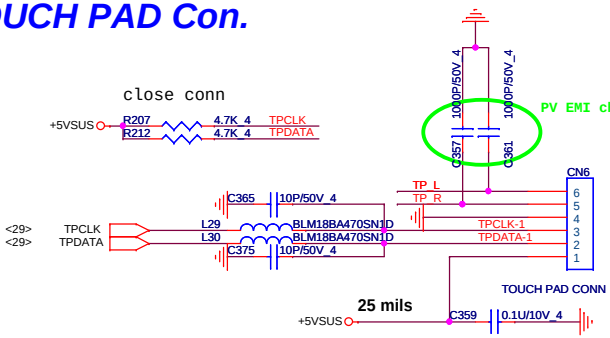
SI Modify



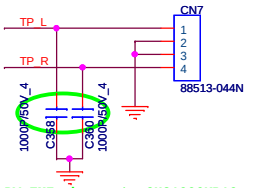




TOUCH PAD Con.



To TOUCH PAD SW board



PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED/KB/SW/TP	1A

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500mA

U4

KB3926QF D2

SI Add

for Battery charge/charge and cap board

for VGA/CPU thermal

SI modify

for EMI

For KB3926 B, C version

adapter Type check

Change to 1SS355 as Current loss

thermal shutdown circuit

SI Modify

adapter select for EC

Hi ==> 120W

Low ==> 65W/90W

512K byte SPI EC ROM

Socket: DG008000031

MXIC AKE3KZP0001

WINBOND AKE37ZN0N00

AMIT AKE38ZN0800

Project Model	GPIO42
AX 14"	High
AX 15.6"	Low
AX 17.3"	Middle (1.5V)

GPIO42 control fan table

Change to RB500 as Current loss

Add Pin 117,103 for DSM,116 for Bluetooth

Delete T10 and tie pin 117 from Lan for DSM

AC present: AC_IN-->high, CPU_PROCHOT-->low , H_PROCHOT#-->high

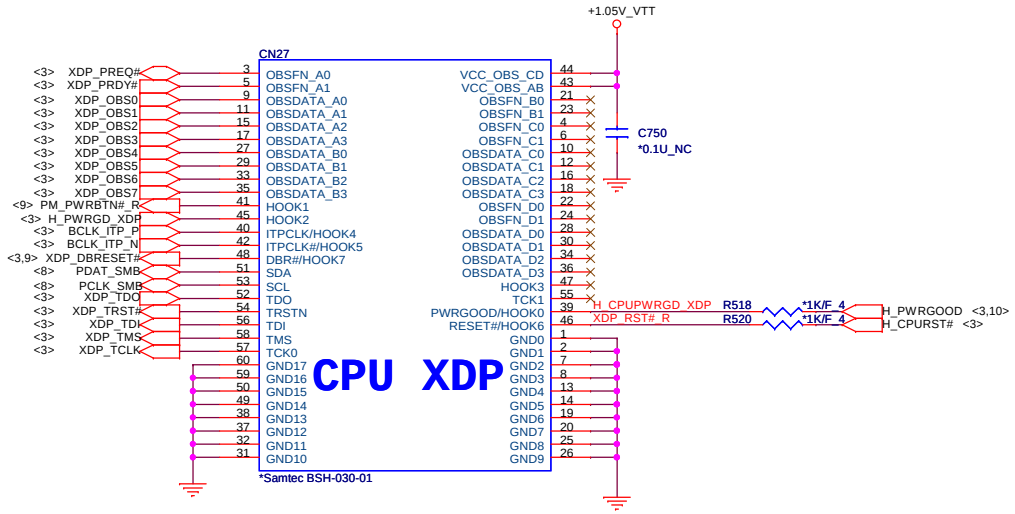
Remove AC: AC_IN-->low, CPU_PROCHOT-->low , H_PROCHOT#-->low

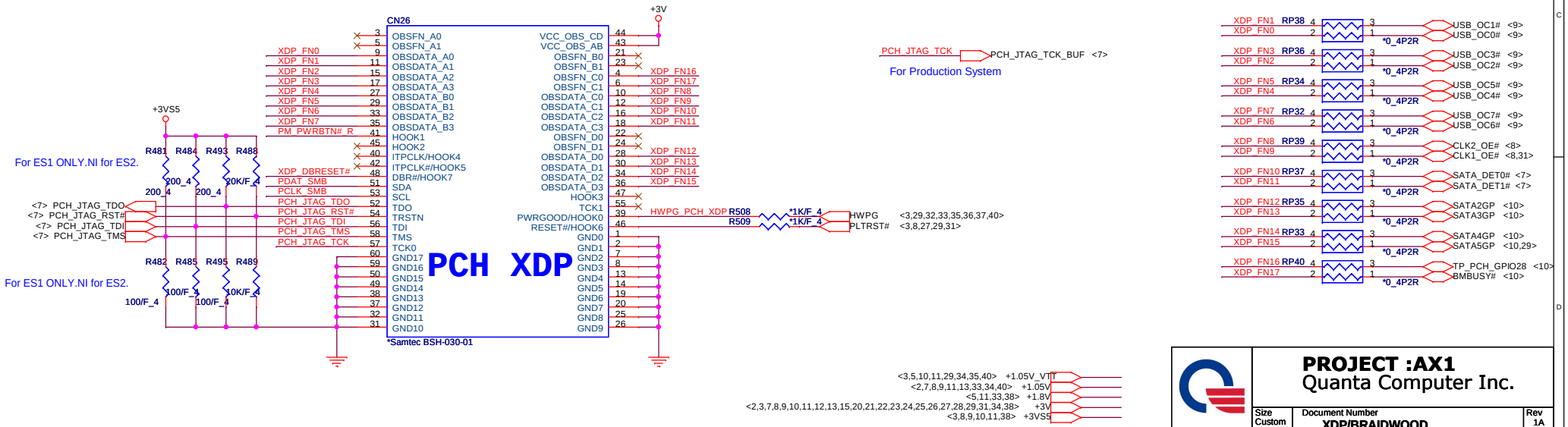
Remove AC and re-cove prochot: AC_IN-->low, CPU_PROCHOT--> high, H_PROCHOT#--> high

PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC (KB3926)/ROM	1A

Date: Thursday, December 03, 2009 | Sheet 29 of 40





PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	XDP/BRAIDWOOD	1A

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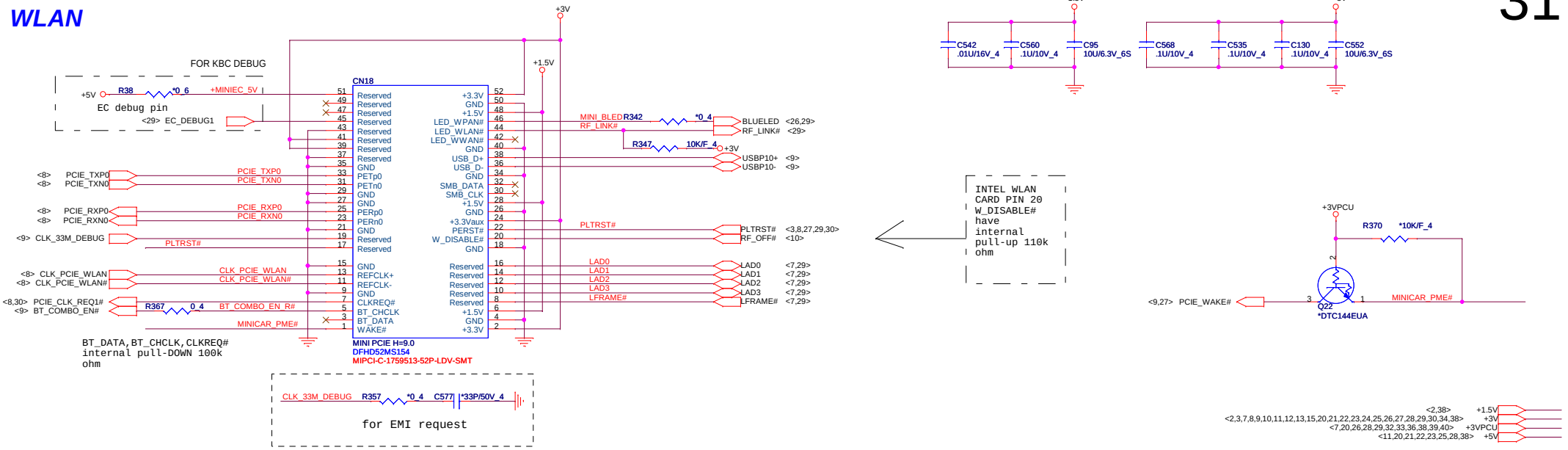
Mini PCI-E Card 1
WLAN



INTEL WLAN CARD PIN 20 W_DISABLE# have internal pull-up 110k ohm

<2,38> +1.5V
<2,3,7,8,9,10,11,12,13,15,20,21,22,23,24,25,26,27,28,29,30,34,38> +3V
<7,20,26,28,29,32,33,36,38,39,40> +3VPCU
<11,20,21,22,23,25,28,38> +5V

PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI PCIE CONN X1	1A

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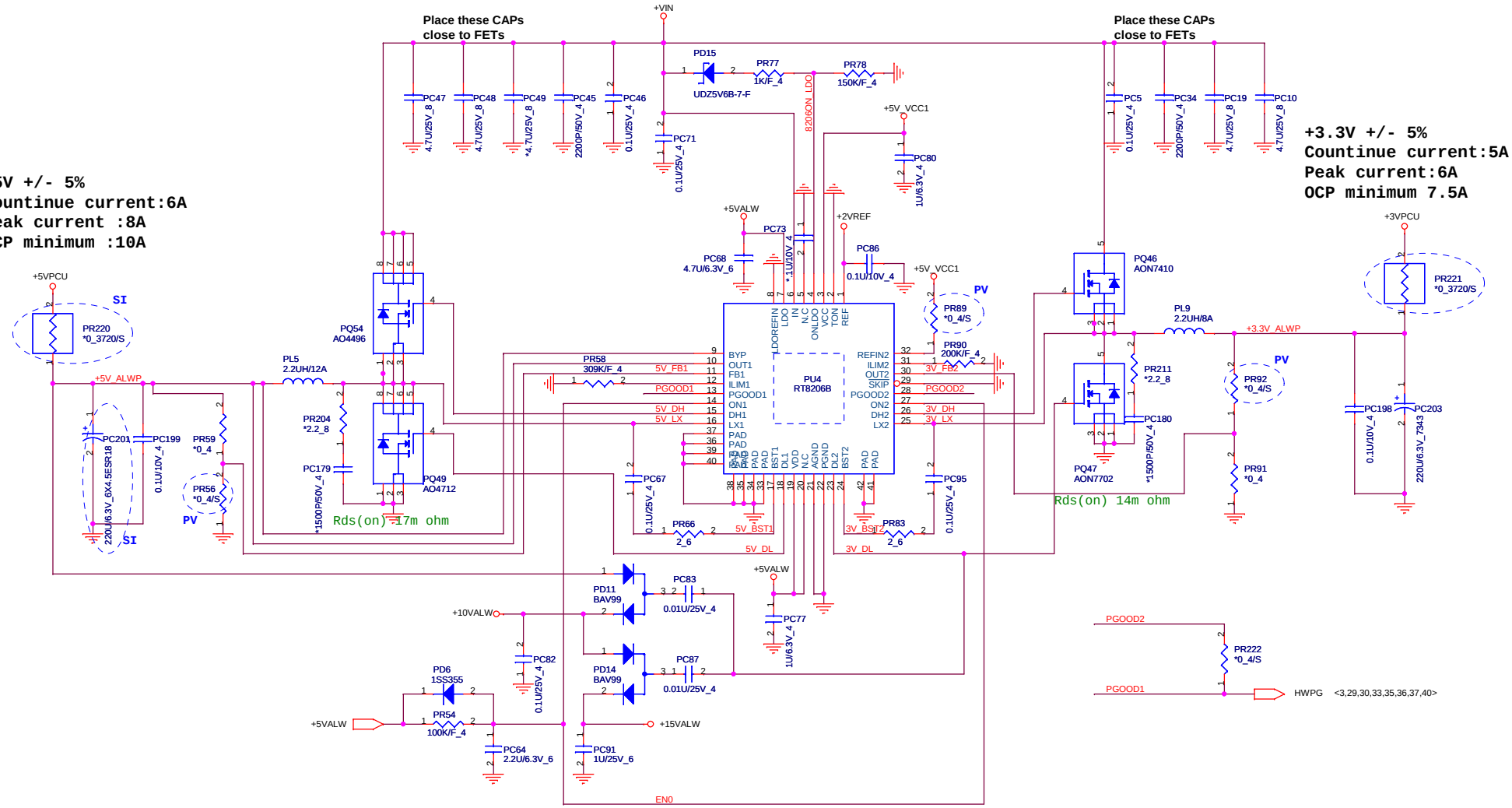
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

+5V +/- 5%
Countinue current:6A
Peak current :8A
OCP minimum :10A

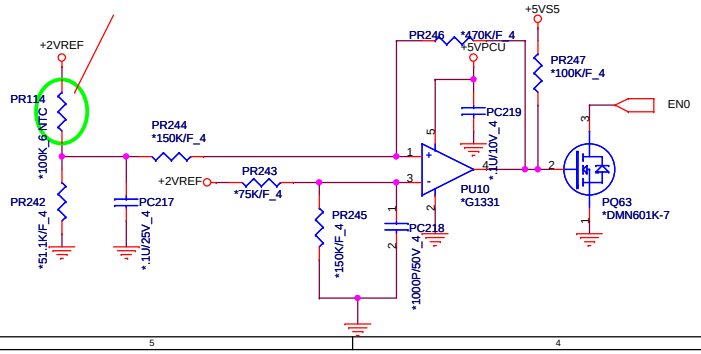
+3.3V +/- 5%
Countinue current:5A
Peak current:6A
OCP minimum 7.5A

Place these CAPs close to FETs

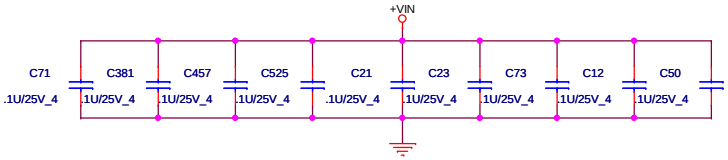
Place these CAPs close to FETs



NTC need place under CPU Socket
CPU Thermal protection at 90 +/-3 degrreC



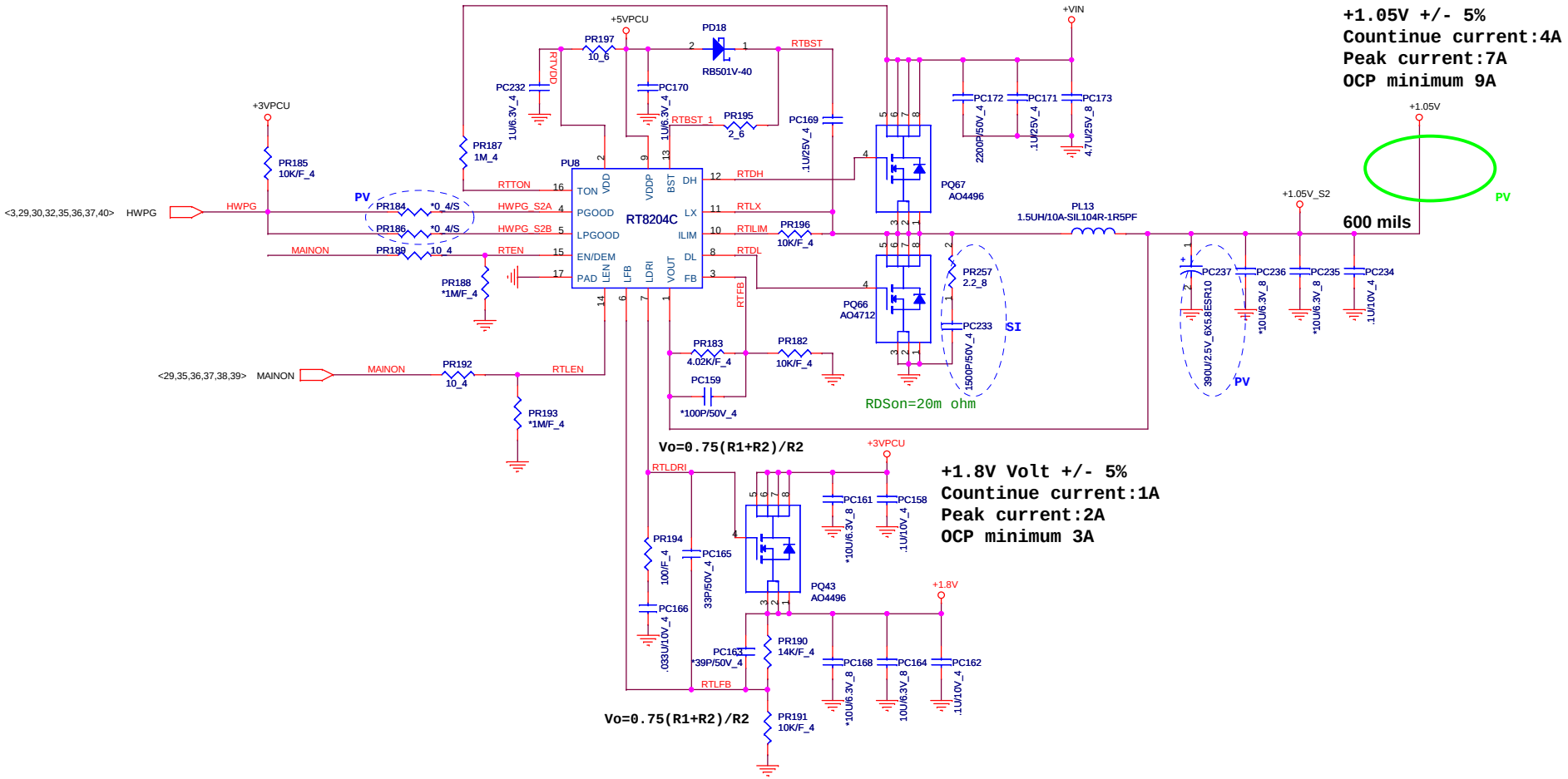
EMI request



PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+5V/+3V (RT8206B)	1A

Date: Thursday, November 12, 2009 | Sheet 32 of 40



PROJECT	AX1
Company	Quanta Computer Inc.
Size	Custom
Document Number	+1.05V/+1.8V (RT8204C)
Rev	1A
Date	Thursday, November 12, 2009
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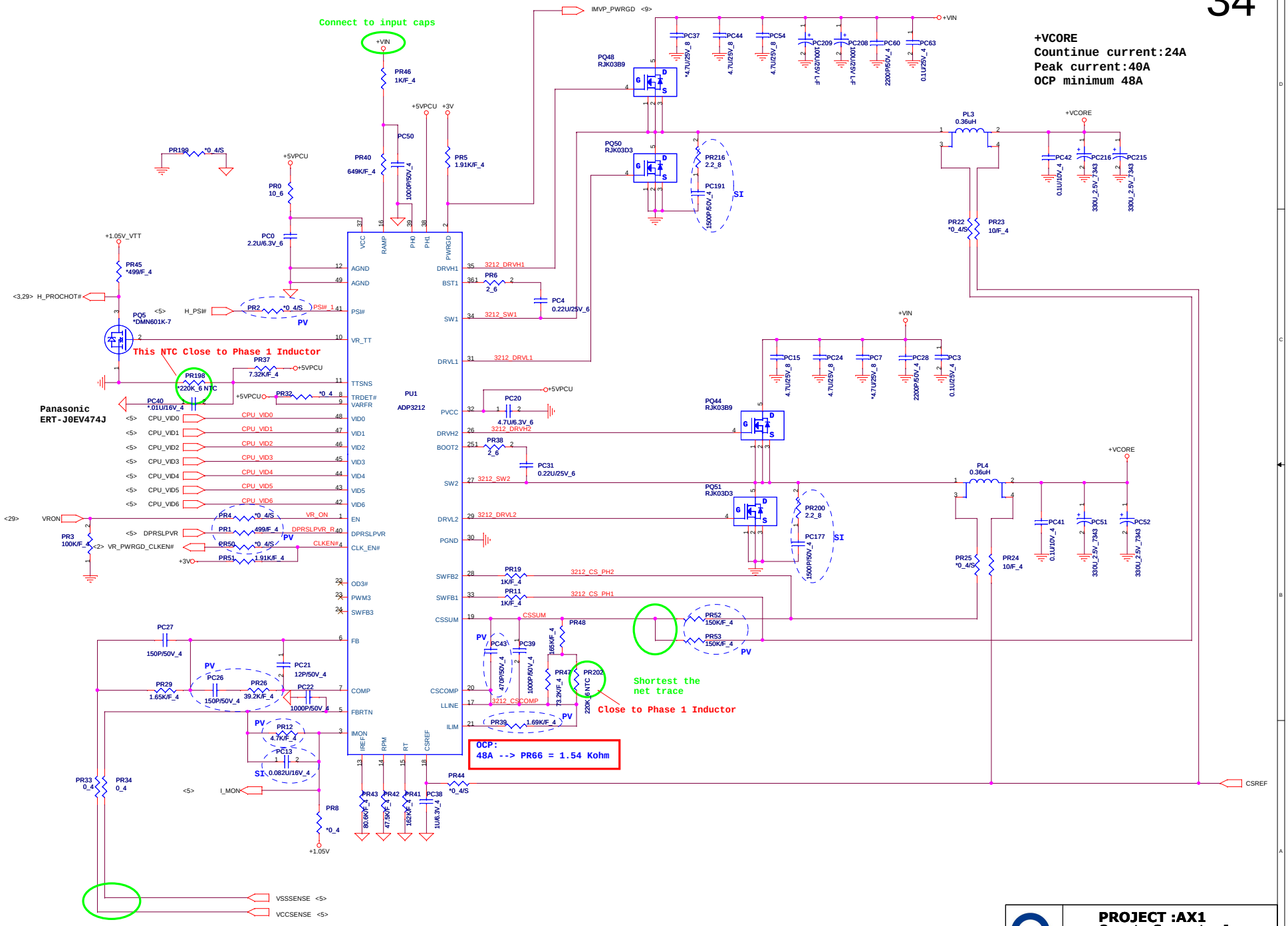

PROJECT :AX1 Quanta Computer Inc.		
Size: Custom	Document Number: CPU Core (ADP3212)	Rev: 1A
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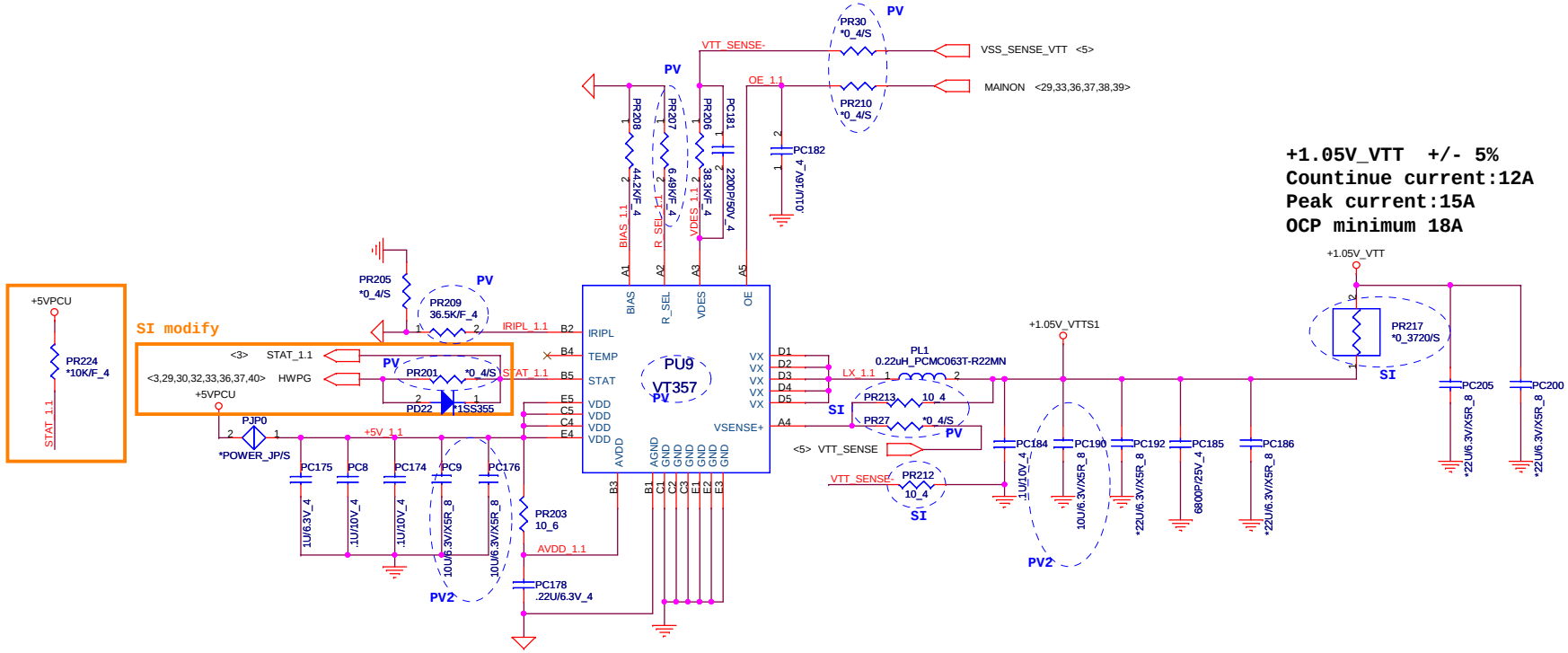

PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.05V_VTT (VT358)	1A

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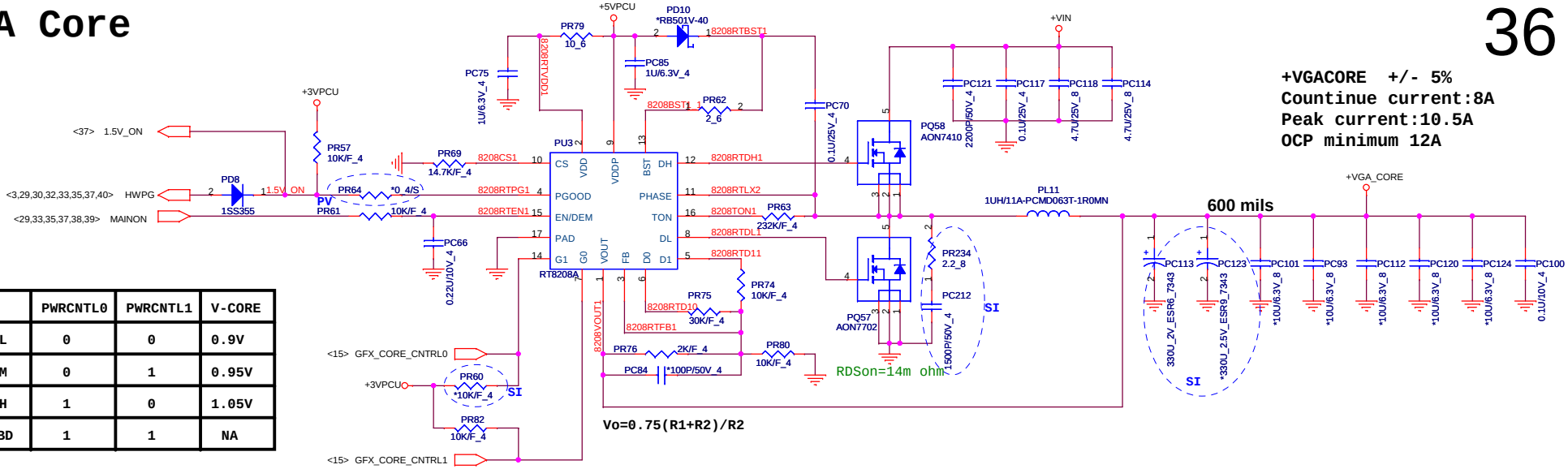
VGA Core

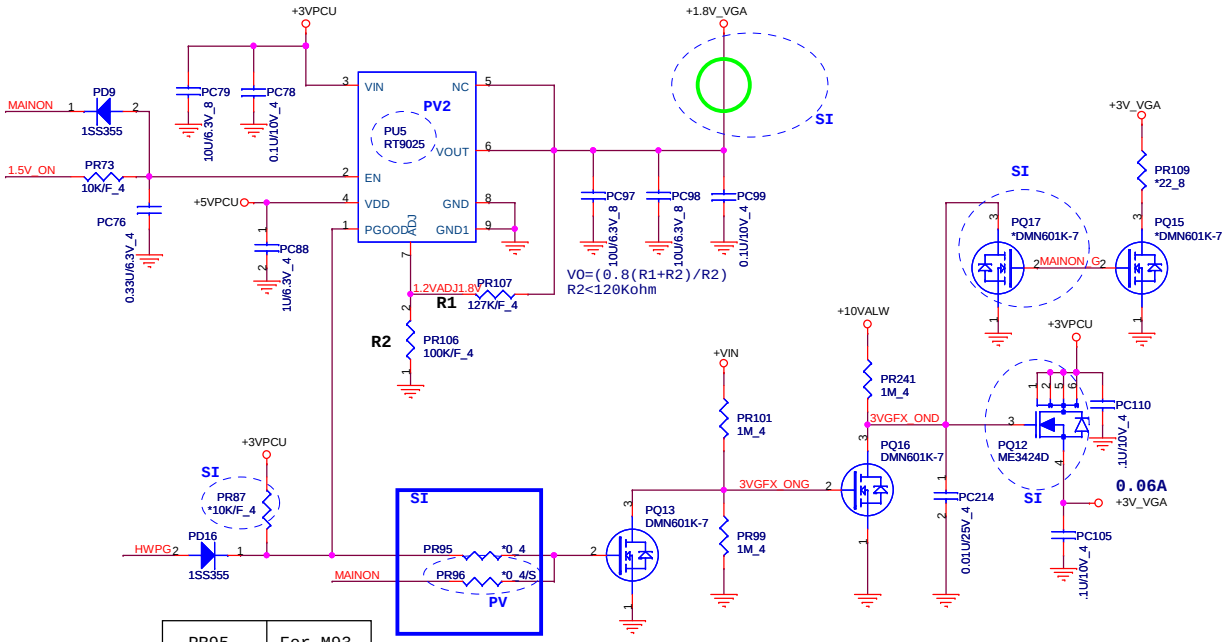
+VGACORE +/- 5%
Countinue current:8A
Peak current:10.5A
OCP minimum 12A



Vo=0.75(R1+R2)/R2

	PWRCNTL0	PWRCNTL1	V-CORE
L	0	0	0.9V
M	0	1	0.95V
H	1	0	1.05V
TBD	1	1	NA

+1.8V +/- 5%
Countinue current:1.2A
Peak current:3A



PR95	For M93
PR96	For PARK

PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8208/1.8V)	1A

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+1.5V +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A

(VTT/2A)
(3mA)

PU0 RT8207GQW

Discrete Only

+1.1V +/- 5%
Countinue current:2A
Peak current:3A

PU11 RT9025

R1 38.3K/F_4
R2 PR250 100K/F_4

VO=(0.8(R1+R2)/R2)
R2<120Kohm

PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (RT8207)	1A

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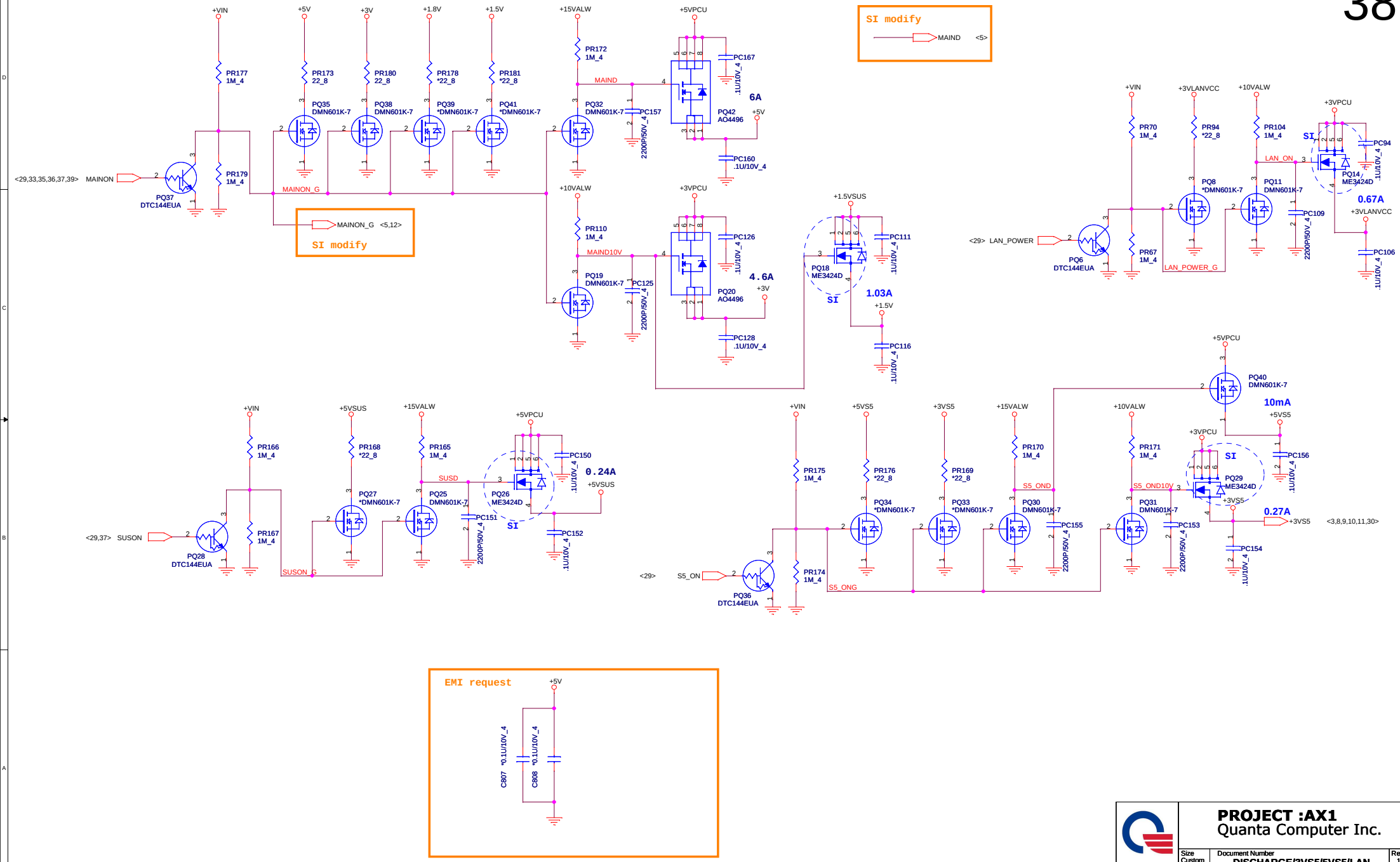

PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHARGE/3VS5/5VS5/LAN	1A

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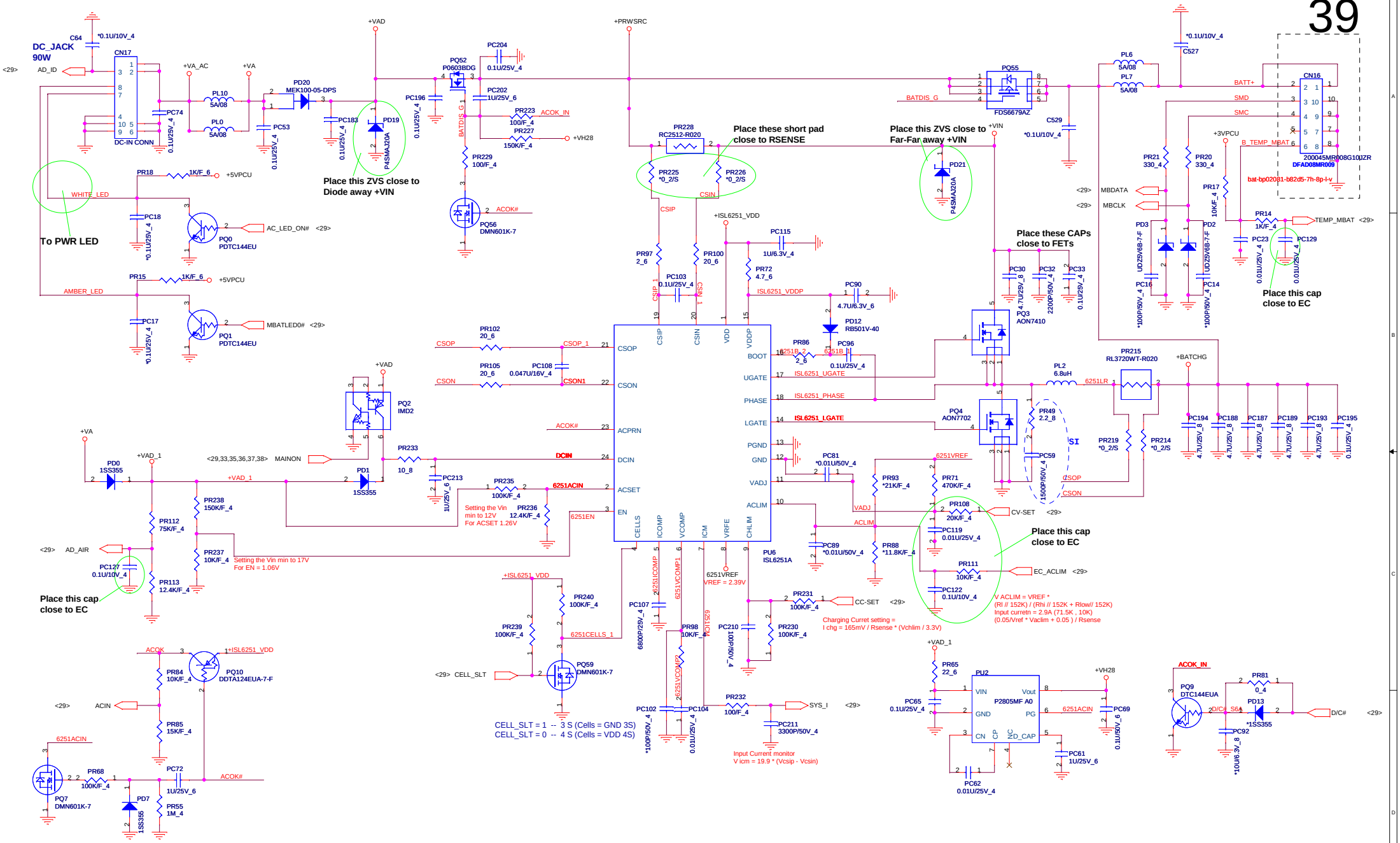
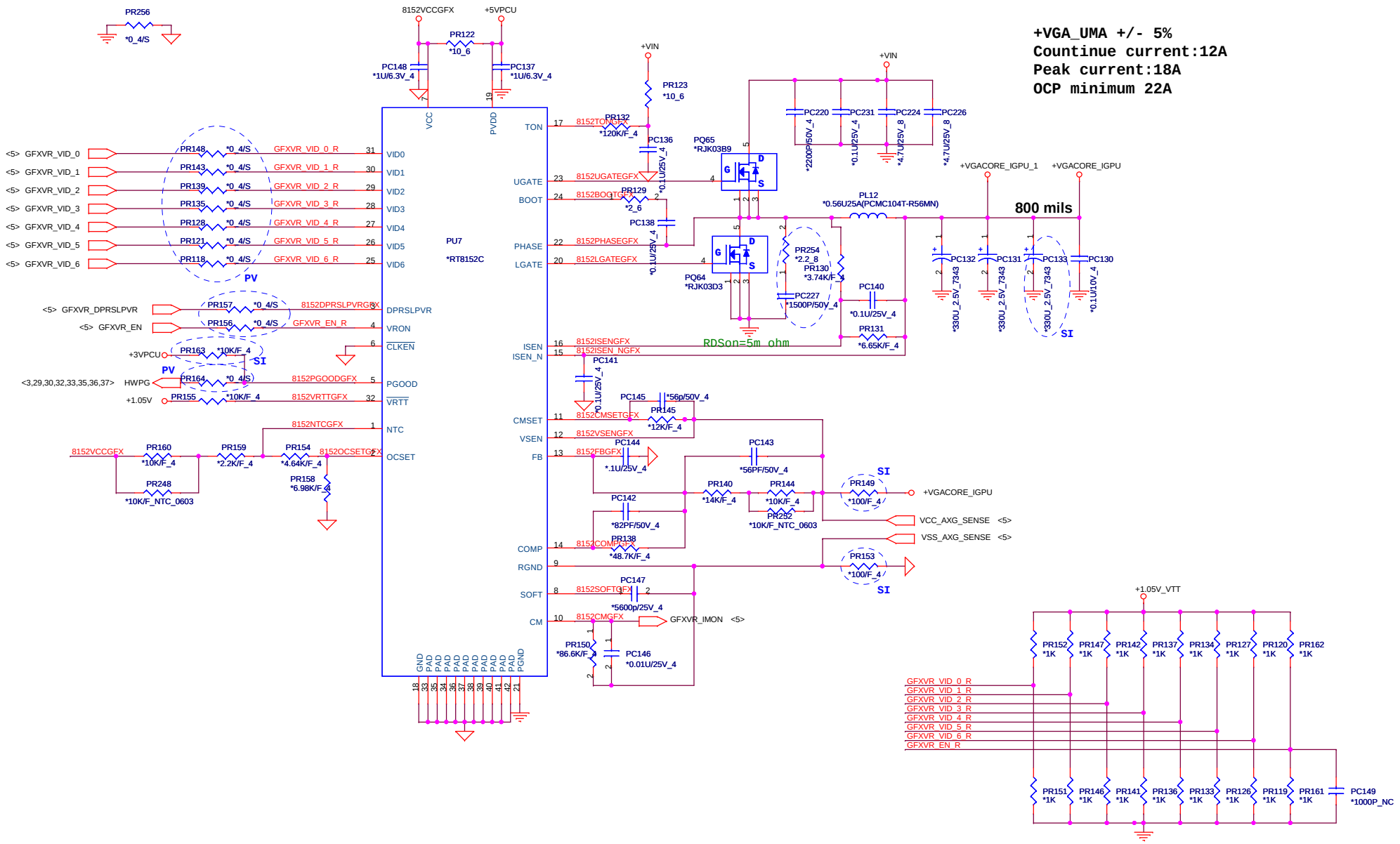


Size: Custom	Document Number: CHARGER (ISL6251)		Rev: 1A
Date: Thursday, November 12, 2009	Sheet 39 of 40		

PROJECT :AX1
Quanta Computer Inc.

+VGA_UMA +/- 5%
Countinue current:12A
Peak current:18A
OCP minimum 22A



PROJECT :AX1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	UMA GPU CORE (RT8152C)	1A

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