ZZZ1
DAZ

ZZZ2
12.1W_PCB_LA5191P
Part Number = DA80000EF10

ZZZ3
12.1W_PCB_LS5191P
Part Number = DA60000C410

ZZZ4
12.1W_PCB_LS5192P
Part Number = DA40000K110

ZZZ5
12.1W_PCB_LS5193P
Part Number = DA40000K010

ZZZ6
12.1W_PCB_LS5194P
Part Number = DA20000GH10

KIUE0

Schematics Document

Mobile Penryn PGA with Intel Cantiga_GM45+ICH9-M core logic

REV:1.0

Security Classification	Compal Secret Data		
Issued Date		Deciphered Date	

Compal Electronics,Ltd.

Title: Cover Sheet

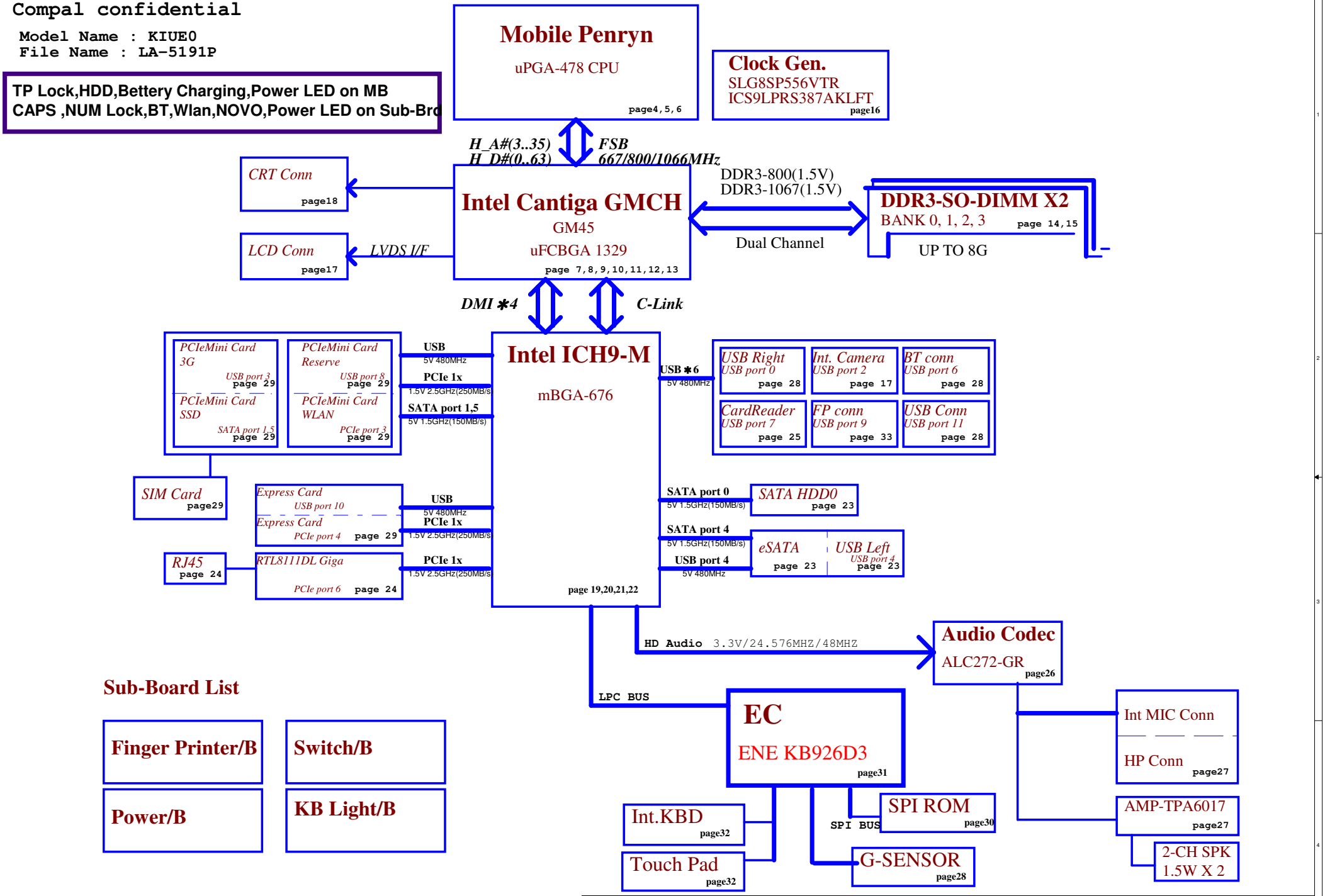
Size: Custom | Document Number: KIUE0_LA-5191P | Rev: 1.0

Date: Thursday, June 25, 2009 | Sheet 1 of 43

Compal confidential

Model Name : KIUE0
File Name : LA-5191P

TP Lock,HDD,Bettery Charging,Power LED on MB
CAPS ,NUM Lock,BT,Wlan,NOVO,Power LED on Sub-Brd



Sub-Board List

- Finger Printer/B
- Switch/B
- Power/B
- KB Light/B

Security Classification	Compal Secret Data		
Issued Date	2008/03/24	Deciphered Date	2008/04/

Compal Electronics, Inc.

Title: MB Block Diagram

Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 Sheet 2 of 43

Voltage Rails

Power Plane	Description	S1	S3	S5	G3
VIN	Adapter power supply (19V)	ON	ON	ON	OFF
B+	AC or battery power rail for power circuit.	ON	ON	ON	OFF
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF	OFF
+1.5V	1.8V power rail for DDR	ON	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON	OFF
VL	3.3V always on power rail	ON	ON	ON	ON
+3V_SB	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3V_WLAN	3.3V power rail for LAN	ON	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON	OFF
+5VL	5V always on power rail	ON	ON	ON	ON
+5V_SB	5V power rail for SB	ON	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON	OFF
+RTCVCC	RTC power	ON	ON	ON	ON
+GPU_CORE	Core voltage for VGA chip	ON	ON	OFF	OFF
+1.8VS	1.8V power rail for NB	ON	OFF	OFF	OFF

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#		
Full ON	HIGH	HIGH	HIGH	HIGH		
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH		
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH		
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH		
S5 (Soft OFF)	LOW	LOW	LOW	LOW		
G3	LOW	LOW	LOW	LOW		

BTO Option Table

Function	CRT	LAN	Finger printer	BLUE TOOTH	3G SIM slot	Mini card
description	(Q)	(C)	(F)	(B)	(3)	(D2)
explain						
BTO						

External PCI Devices

EC SM Bus1 address

Power	Device	Address
+3VALW	EC KB926 D3	
+3VALW	Smart Battery	

EC SM Bus2 address

Power	Device	Address
+3VALW	EC KB926 D3	
+3VALW	CPU THM Sen SMSC SMC1402	

ICH9M SM Bus address

Power	Device	Address
+3V_SB	ICH9M	
+3VS	Clock Generator (SLG8SP556V)	
+3VS	DDR DIMM0	
+3VS	DDR DIMM1	
+3VS	Express	

Security Classification	Compal Secret Data		
Issued Date	2008/03/24	Deciphered Date	2008/04/

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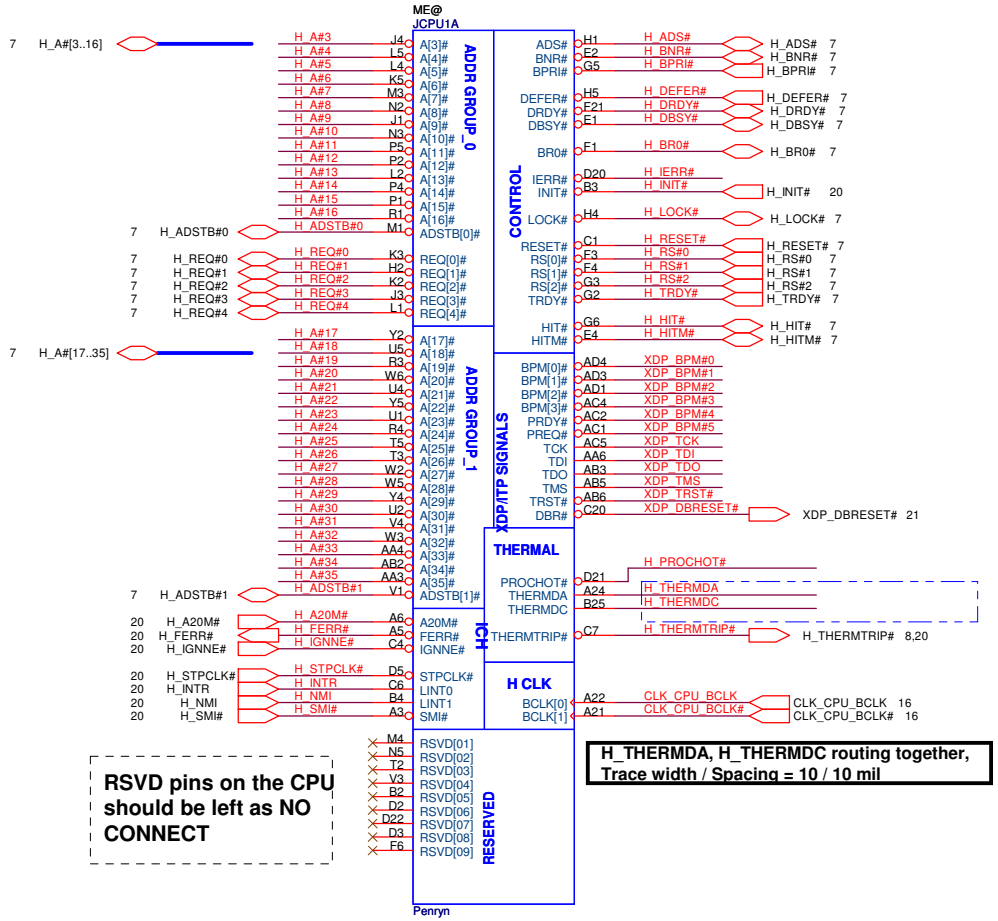
Title: MB Notes List

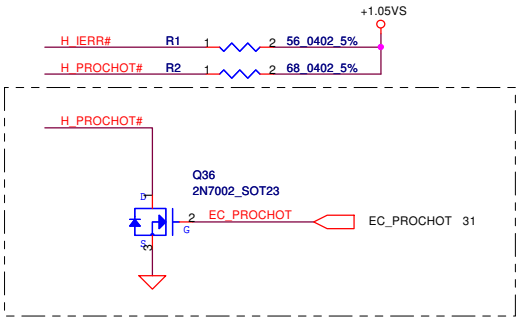
Size: B | Document Number: KIUE0_LA-5191P | Rev: 1.0

Date: Wednesday, June 24, 2009 | Sheet 3 of 43

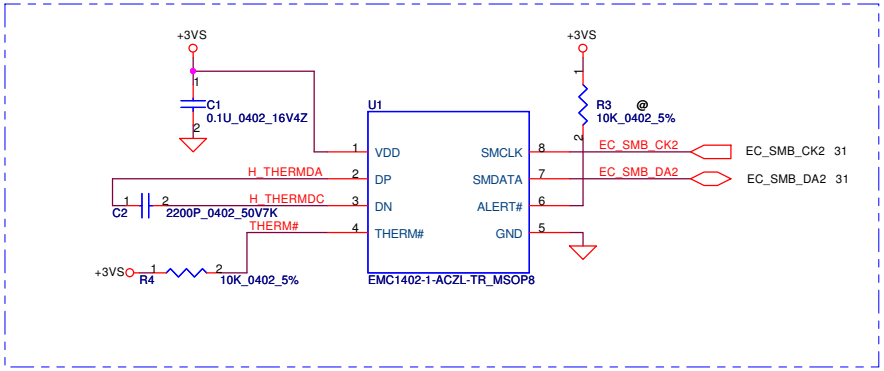


RSVD pins on the CPU should be left as NO CONNECT

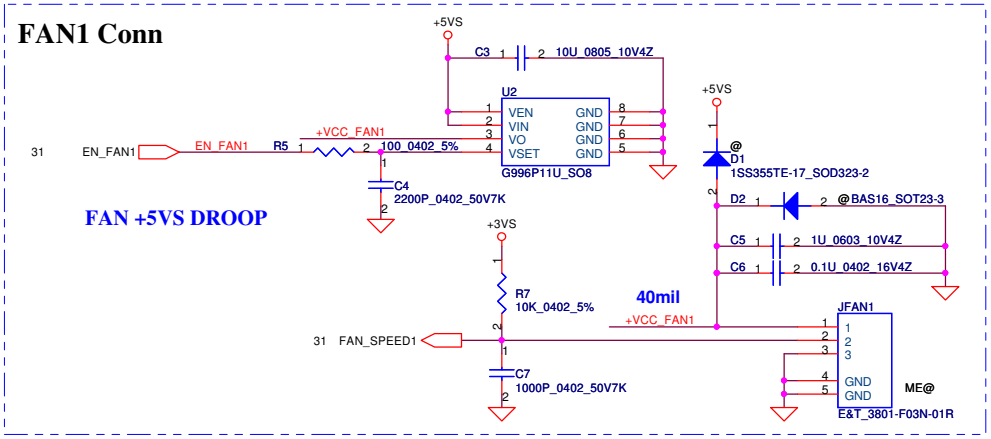
H_THERMDA, H_THERMDC routing together, Trace width / Spacing = 10 / 10 mil



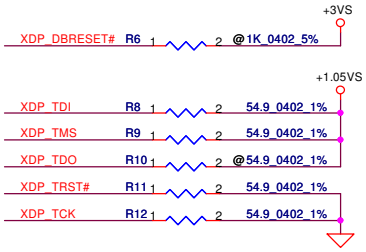
Hardware force mechanism for throttling



Address:100_1100



XDP Reserve for debug , Please close to CPU side



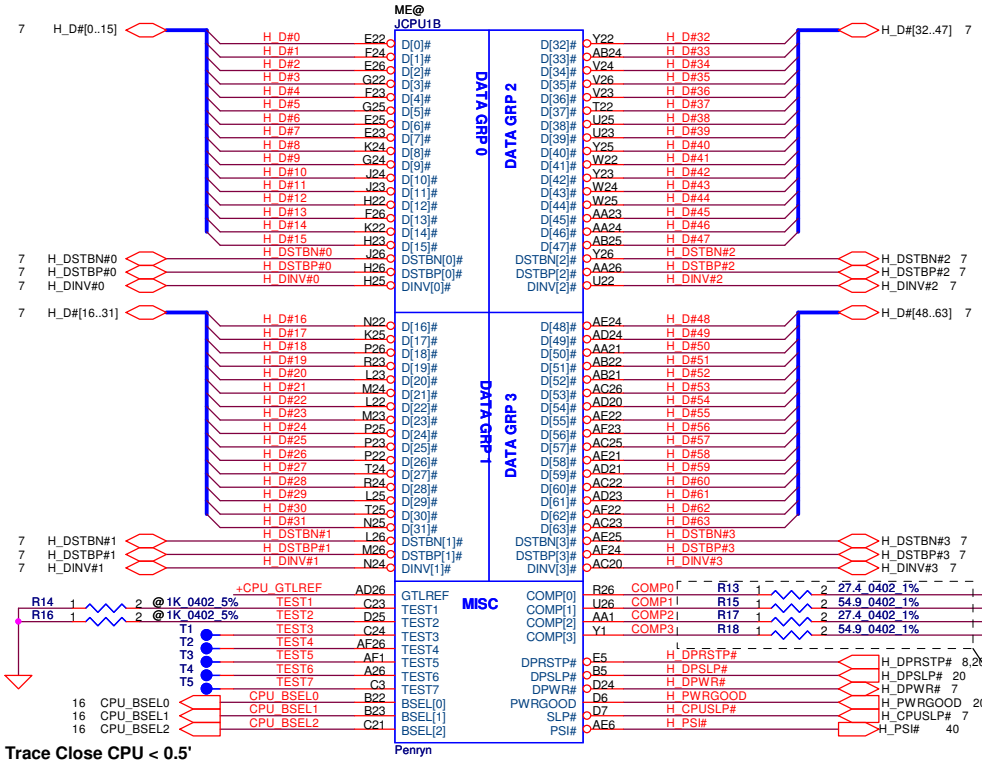
Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

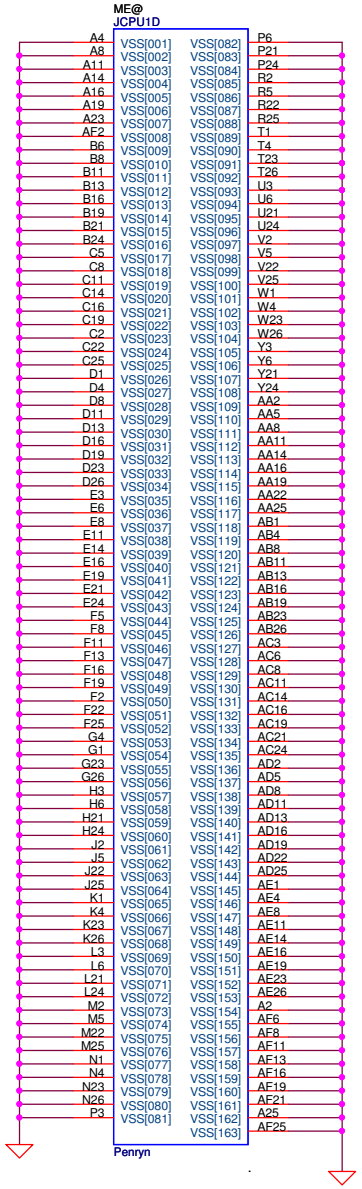
Compal Electronics,Ltd.

Title: Penryn(1/3)

Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

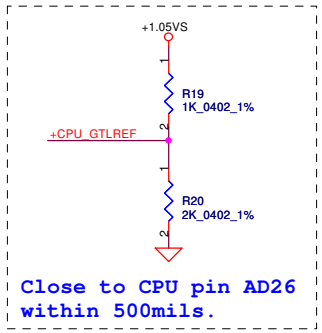
Date: Wednesday, June 24, 2009 Sheet 4 of 43





layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0
1067	266	0	0	0



Layout note: Z0=55 ohm
0.5" max for GTLREF.

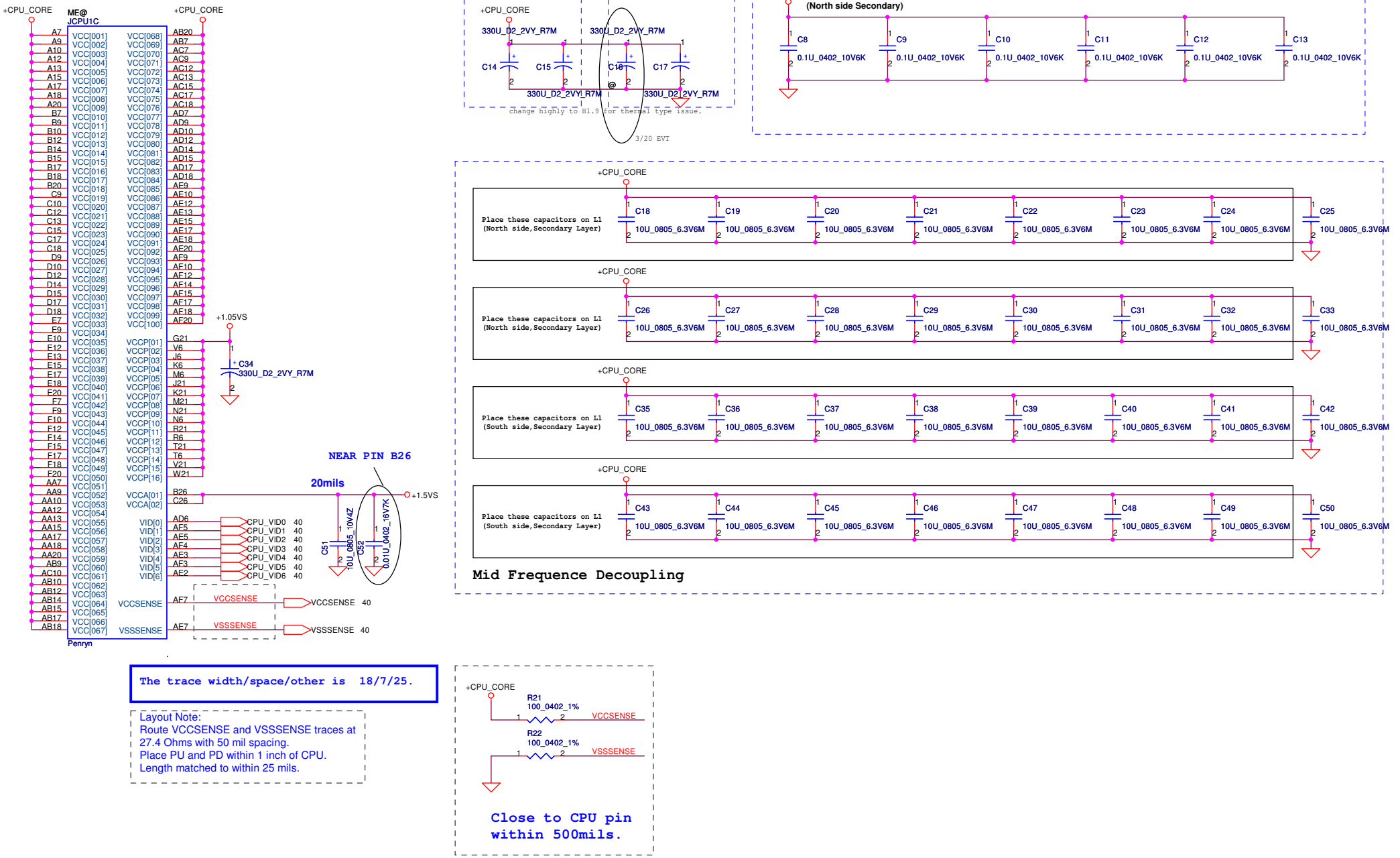
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Penryn (2/3)**

Size	Document Number	Rev
B	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 Sheet 5 of 43



The trace width/space/other is 18/7/25.

Layout Note:
Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing.
Place PU and PD within 1 inch of CPU.
Length matched to within 25 mils.

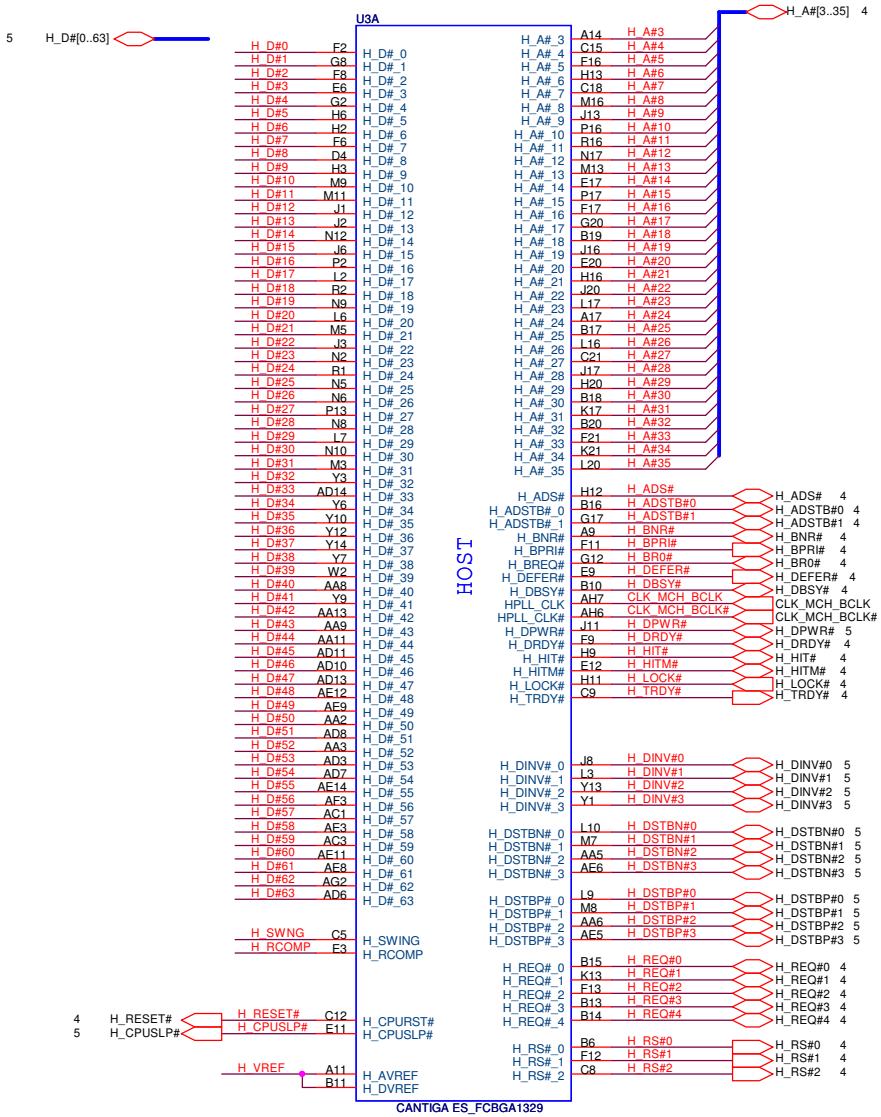
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

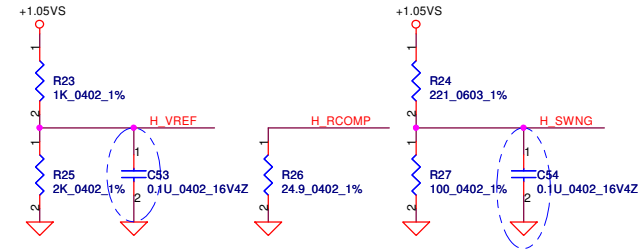
Title: Penryn (3/3)

Size: Custom | Document Number: KIUE0_LA-5191P | Rev: 1.0

Date: Wednesday, June 24, 2009 | Sheet 6 of 43



Layout Note:
H_RCOMP / H_VREF / H_SWNG trace width and spacing is 10/20



within 100 mils from NB **Near B3 pin**

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Cantiga GMCH(1/6)-GTL**

Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 Sheet 7 of 43

Strap Pin Table

CFG[2:0]		011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	Internal pull-up	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG6	Internal pull-up	0 = iTPM Host Interface is enabled can support disble by SW. 1 = iTPM Host Interface is Disabled *(Default)
CFG7	Internal pull-up	0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel Management Engine Crypto TLS cipher suite with confidentiality *(Default)
CFG9	Internal pull-up	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG10	Internal pull-up	0 = PCIe Loopback Enable 1 = Disable*(Default)
CFG[13:12]	Internal pull-up	01 = All Z Mode Enabled 00 = Reserved 10 = XOR Mode Enabled 11 = Normal Operation*(Default)
CFG16	Internal pull-up	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG19	Internal pull-down	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIE/SDVO select)	Internal pull-down	0 = Only PCIE or [SDVO/DP/HDMI] is operational. * (Default) 1 = PCIE/[SDVO/DP/HDMI] are operating simu.

U3B

RSVD: RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 RSVD7 RSVD8 RSVD9 RSVD10 RSVD11 RSVD12 RSVD13 RSVD14 RSVD15 RSVD16 RSVD17 RSVD20 RSVD22 RSVD23 RSVD24 RSVD25

DDR CLK/ CONTROL/ COMPENSATION: SA_CK_0 SA_CK_1 SB_CK_0 SB_CK_1 SA_CK#_0 SA_CK#_1 SB_CK#_0 SB_CK#_1 SA_CKE_0 SA_CKE_1 SB_CKE_0 SB_CKE_1 SA_CS#_0 SA_CS#_1 SB_CS#_0 SB_CS#_1 SA_ODT_0 SA_ODT_1 SB_ODT_0 SB_ODT_1 SM_RCOMP SM_RCOMP# SM_RCOMP_VOH SM_RCOMP_VOL SM_VREF SM_PWROK SM_REXT SM_DRAMRST#

CLK: DPLL_REF_CLK DPLL_REF_CLK# DPLL_REF_SSCLK DPLL_REF_SSCLK# PEG_CLK PEG_CLK#

DMI: DMI_RXN_0 DMI_RXN_1 DMI_RXN_2 DMI_RXN_3 DMI_RXP_0 DMI_RXP_1 DMI_RXP_2 DMI_RXP_3 DMI_TXN_0 DMI_TXN_1 DMI_TXN_2 DMI_TXN_3 DMI_TXP_0 DMI_TXP_1 DMI_TXP_2 DMI_TXP_3

CFG: CFG_0 CFG_1 CFG_2 CFG_3 CFG_4 CFG_5 CFG_6 CFG_7 CFG_8 CFG_9 CFG_10 CFG_11 CFG_12 CFG_13 CFG_14 CFG_15 CFG_16 CFG_17 CFG_18 CFG_19 CFG_20

PM: PM_SYNC# PM_DPRSTP# PM_EXT_TS#_0 PM_EXT_TS#_1 PWROK RSTIN# THERMTRIP# DPRSLPVR

GRAPHICS VID: GFX_VID_0 GFX_VID_1 GFX_VID_2 GFX_VID_3 GFX_VID_4 GFX_VR_EN

ME: CL_CLK CL_DATA CL_PWROK CL_RST# CL_VREF

MISC: DDPC_CTRLCLK DDPC_CTRLDATA SDVO_CTRLCLK SDVO_CTRLDATA CLKREQ# ICH_SYNC# TSATN#

HDA: HDA_BCLK HDA_RST# HDA_SDI HDA_SDO HDA_SYNC

NC: NC_1 NC_2 NC_3 NC_4 NC_5 NC_6 NC_7 NC_8 NC_9 NC_10 NC_11 NC_12 NC_13 NC_14 NC_15 NC_16 NC_17 NC_18 NC_19 NC_20 NC_21 NC_22 NC_23 NC_24 NC_25 NC_26

CANTIGA ES_FCBGA1329

For DDR3 : 1.5V power rail
For DDR2 : 1.8V power rail

For Crestline: 20ohm
For Calero: 80.6ohm
For Cantiga: 80.6ohm

SM_DRAMRST# is only for DDR3.
DDR2 left it No Connect

For independent Power Rail : connect to PWM CORE VID
For Common Power Rail : left it No Connect

For AMT function

Notice: Please check HDA power rail to select HDA controller.

Strap Pin Table

SDVO_CTRLDATA (Internal pull-down)	0 = SDVO interface disabled *(Default) 1 = SDVO interface enabled
DDPC_CTRLDATA (Internal pull-down)	0 = Digital display (iHDMI/DP) interface disabled (Default) 1 = Digital display (iHDMI/DP) interface enabled

Layout Note:
V_DDR_MCH_REF trace width and spacing is 20/20.
CLOSE TO PIN.AV21

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: Cantiga(2/7)-DMI/DDR/STRP

Size: Custom | Document Number: KIUE0_LA-5191P | Rev: 1.0

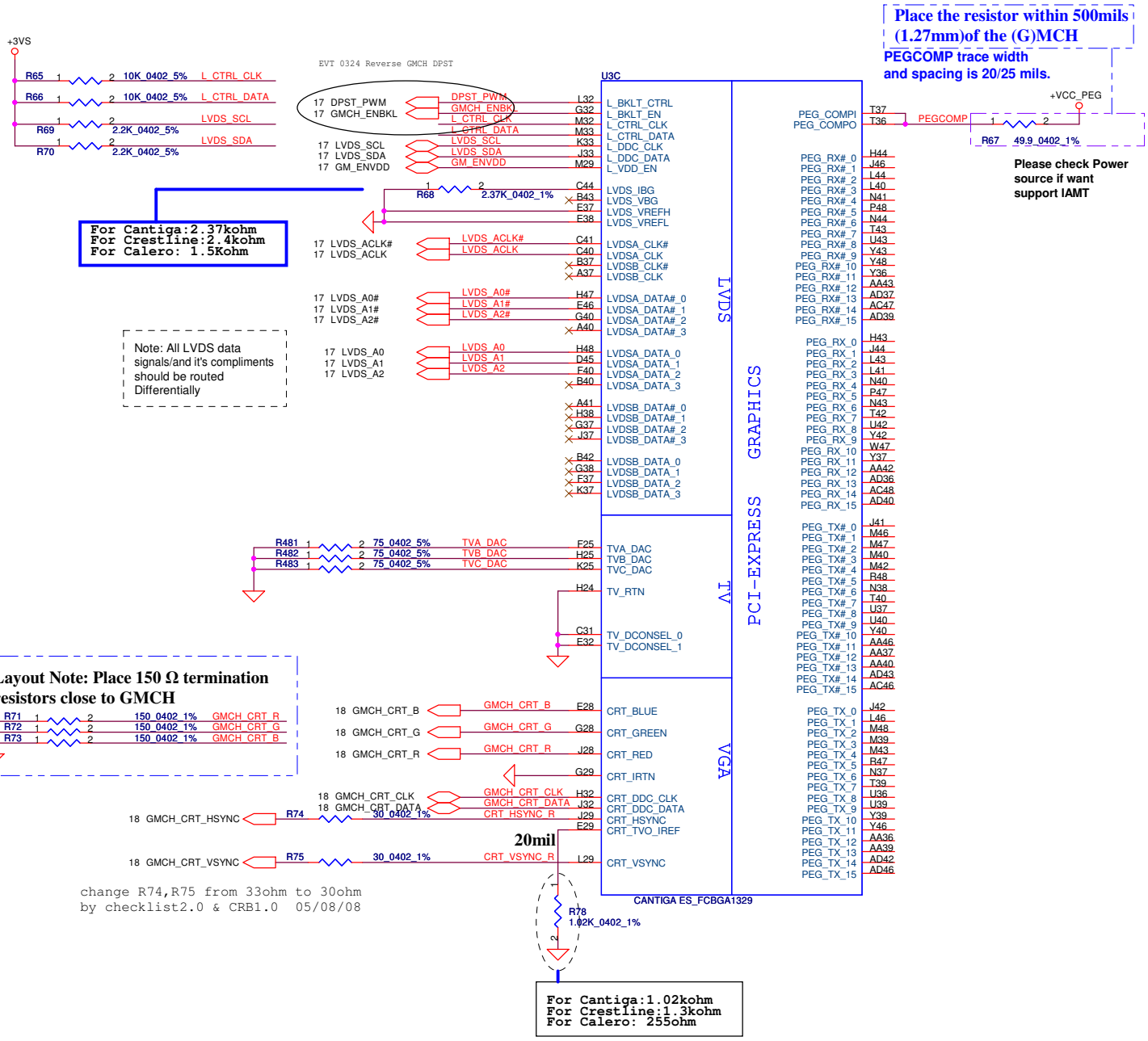
Date: Wednesday, June 24, 2009 | Sheet 8 of 43

Compal Electronics, Inc.

Title: **Cantiga GMCH (2/6)-DDRII**

Size	Document Number	Rev
B	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 Sheet 9 of 43



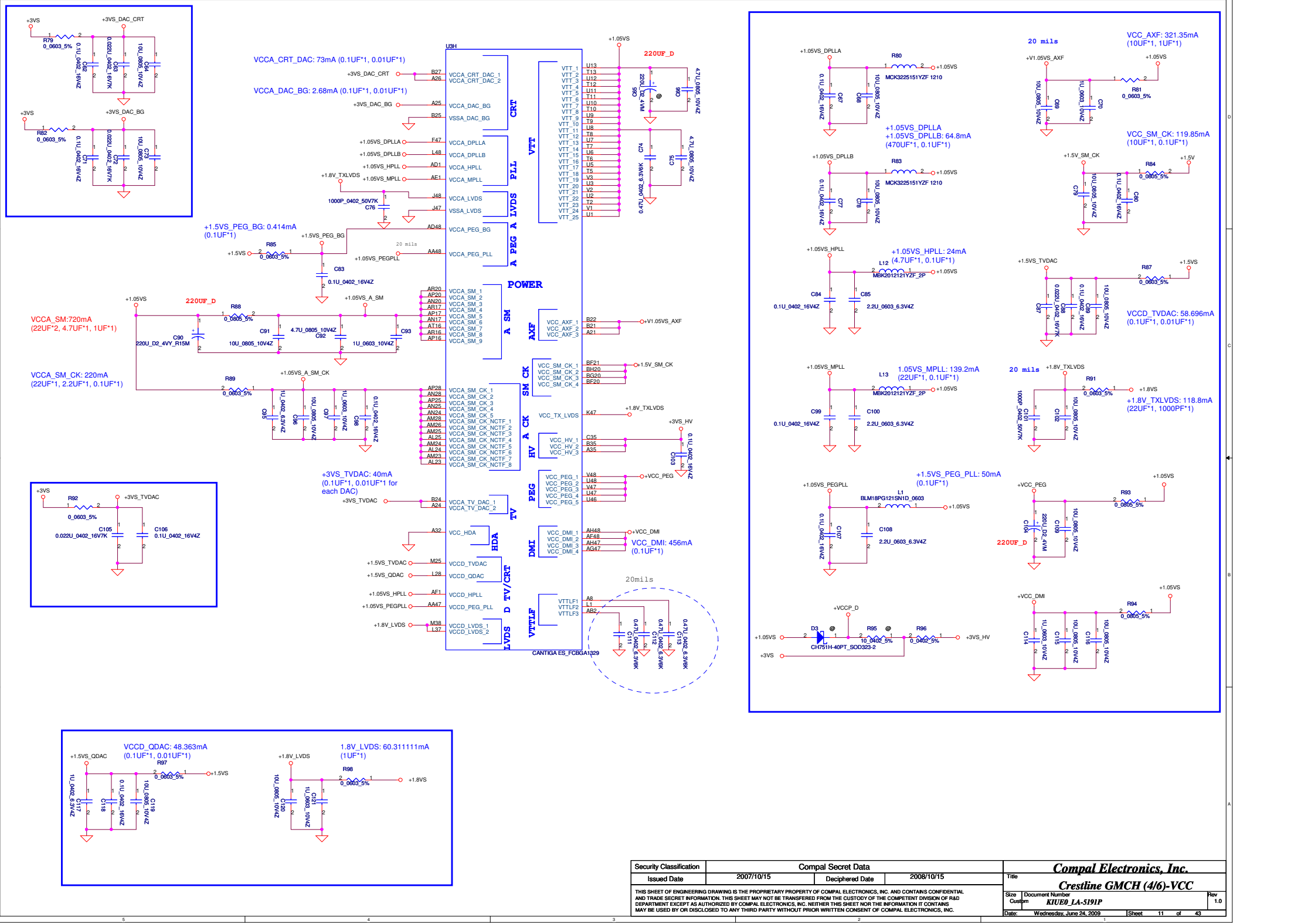
Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

Compal Electronics,Ltd.

Title: Cantiga(3/6)-VGA/LVDS/TV

Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 Sheet 10 of 43



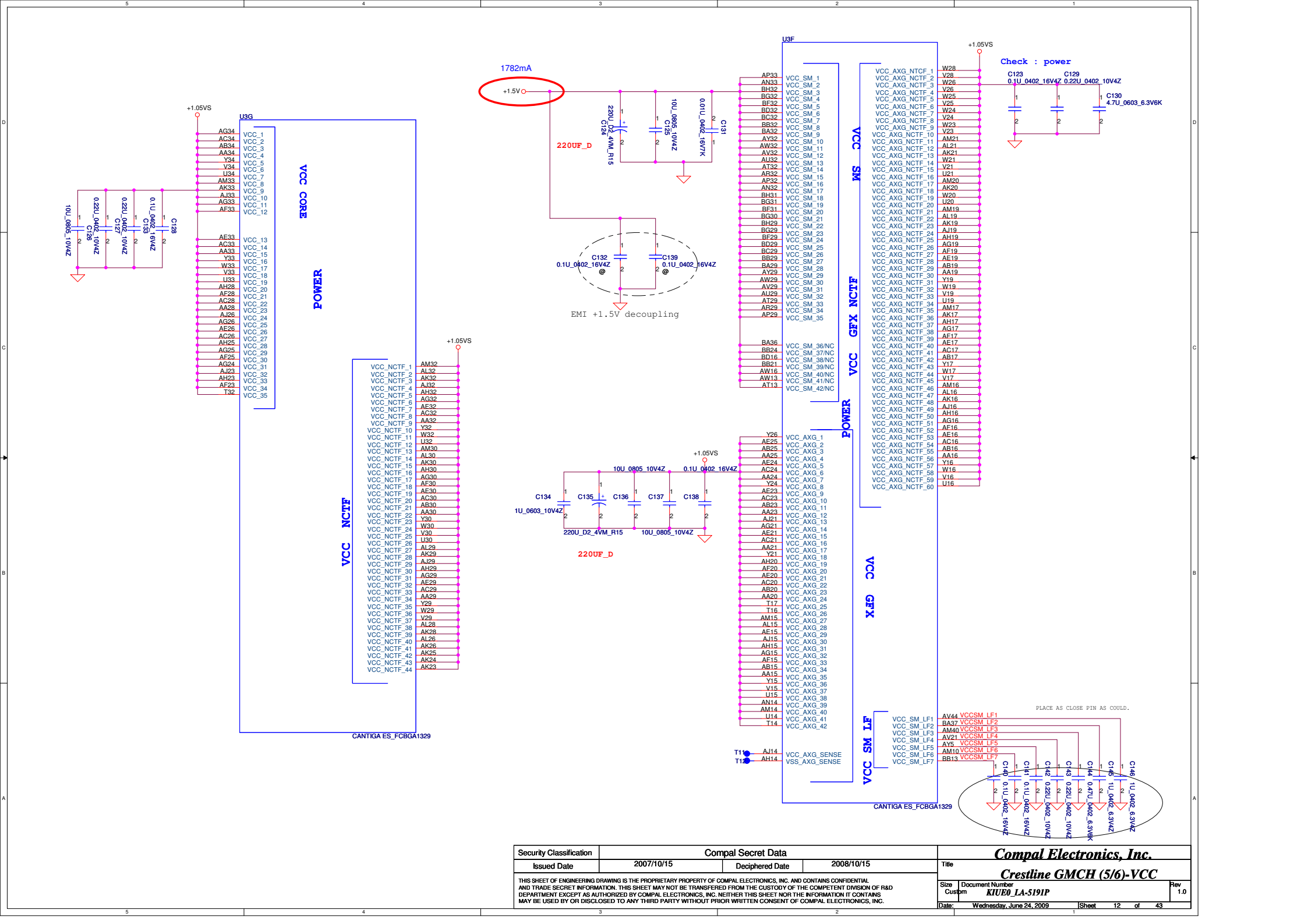
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Crestline GMCH (4/6)-VCC**

Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 | Sheet 11 of 43



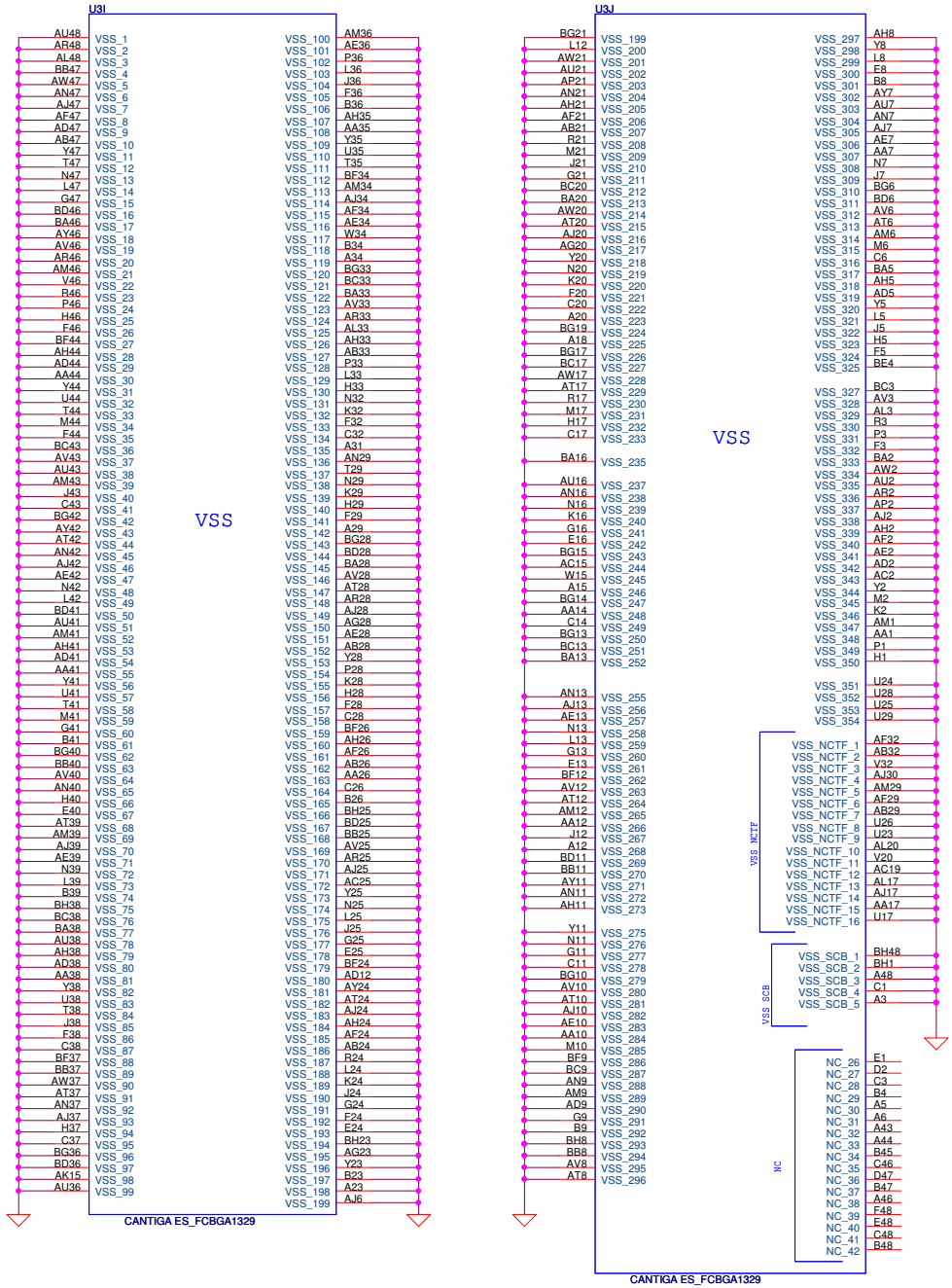
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Crestline GMCH (5/6)-VCC**

Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 Sheet 12 of 43



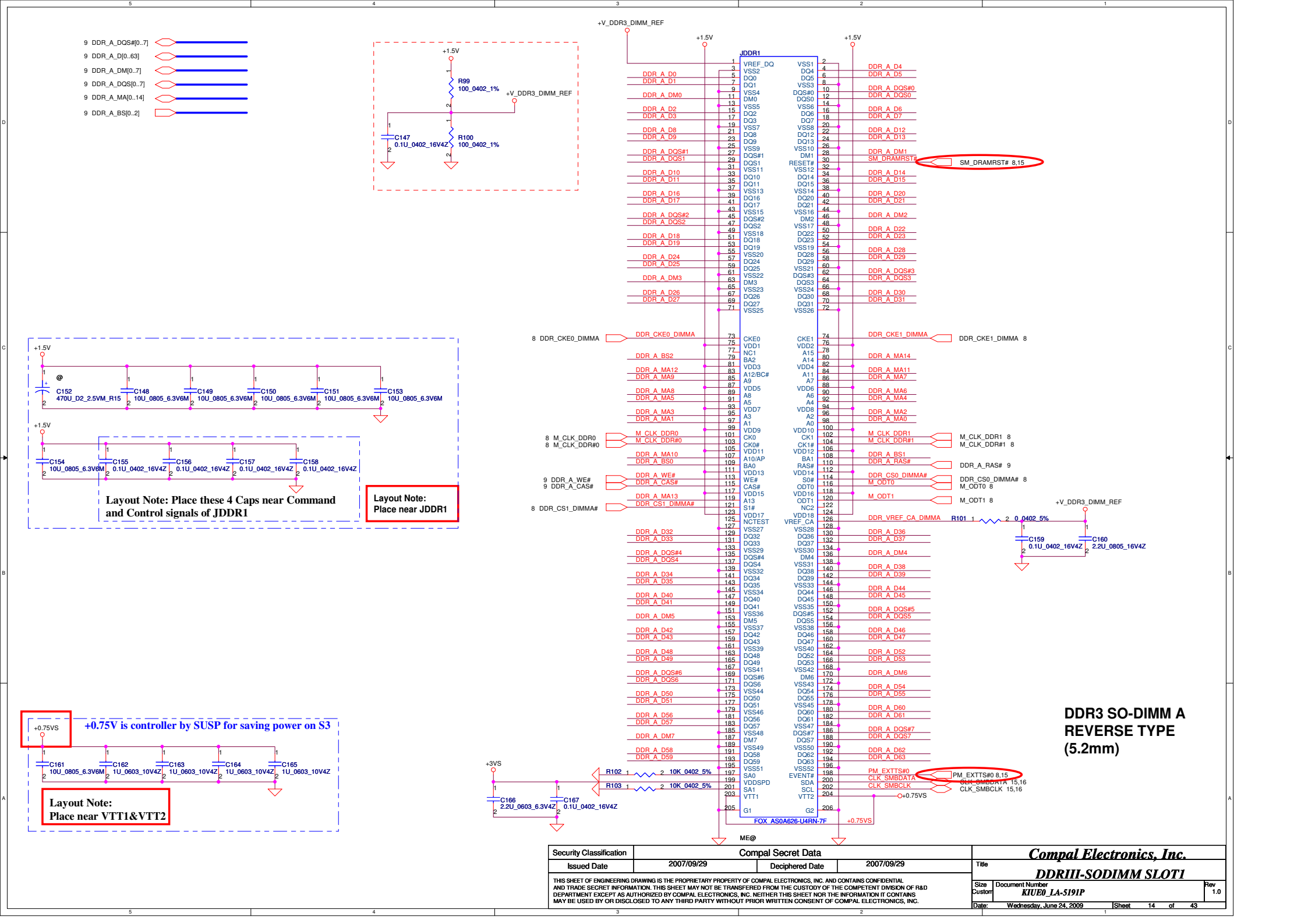
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.

Title: **Cantiga GMCH (6/6)-GND**

Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 | Sheet 13 of 43


9 DDR_A_DQS#[0..7]
9 DDR_A_D[0..63]
9 DDR_A_DM[0..7]
9 DDR_A_DQS[0..7]
9 DDR_A_MA[0..14]
9 DDR_A_BS[0..2]
+1.5V
R99
100_0402_1%
+V_DDR3_DIMM_REF
C147
0.1U_0402_16V4Z
R100
100_0402_1%
+V_DDR3_DIMM_REF
+1.5V
+1.5V
JDDR1
DDR_A_D0
DDR_A_D1
DDR_A_DM0
DDR_A_D2
DDR_A_D3
DDR_A_D8
DDR_A_D9
DDR_A_DQS#1
DDR_A_DQS1
DDR_A_D10
DDR_A_D11
DDR_A_D16
DDR_A_D17
DDR_A_DQS#2
DDR_A_DQS2
DDR_A_D18
DDR_A_D19
DDR_A_D24
DDR_A_D25
DDR_A_DM3
DDR_A_D26
DDR_A_D27
DDR_A_D4
DDR_A_D5
DDR_A_DQS#0
DDR_A_DQS0
DDR_A_D6
DDR_A_D7
DDR_A_D12
DDR_A_D13
DDR_A_DM1
SM_DRAMRST#
DDR_A_D14
DDR_A_D15
DDR_A_D20
DDR_A_D21
DDR_A_DM2
DDR_A_D22
DDR_A_D23
DDR_A_D28
DDR_A_D29
DDR_A_DQS#3
DDR_A_DQS3
DDR_A_D30
DDR_A_D31
SM_DRAMRST# 8,15
8 DDR_CKE0_DIMMA
DDR_CKE0_DIMMA
DDR_CKE1_DIMMA
DDR_CKE1_DIMMA 8
DDR_A_BS2
DDR_A_MA12
DDR_A_MA9
DDR_A_MA8
DDR_A_MA5
DDR_A_MA3
DDR_A_MA1
DDR_A_MA14
DDR_A_MA11
DDR_A_MA7
DDR_A_MA6
DDR_A_MA4
DDR_A_MA2
DDR_A_MA0
8 M_CLK_DDR0
8 M_CLK_DDR#0
M_CLK_DDR0
M_CLK_DDR#0
M_CLK_DDR1
M_CLK_DDR#1
M_CLK_DDR1 8
M_CLK_DDR#1 8
DDR_A_MA10
DDR_A_BS0
DDR_A_BS1
DDR_A_RAS#
DDR_A_RAS# 9
9 DDR_A_WE#
9 DDR_A_CAS#
DDR_A_WE#
DDR_A_CAS#
DDR_CS0_DIMMA#
M_ODT0
DDR_CS0_DIMMA# 8
M_ODT0 8
DDR_A_MA13
DDR_CS1_DIMMA#
M_ODT1
M_ODT1 8
8 DDR_CS1_DIMMA#
DDR_VREF_CA_DIMMA
R101 1 2 0_0402_5%
+V_DDR3_DIMM_REF
C159
0.1U_0402_16V4Z
C160
2.2U_0805_16V4Z
DDR_A_D32
DDR_A_D33
DDR_A_DQS#4
DDR_A_DQS4
DDR_A_D34
DDR_A_D35
DDR_A_D40
DDR_A_D41
DDR_A_DM5
DDR_A_D42
DDR_A_D43
DDR_A_D48
DDR_A_D49
DDR_A_DQS#6
DDR_A_DQS6
DDR_A_D50
DDR_A_D51
DDR_A_D56
DDR_A_D57
DDR_A_DM7
DDR_A_D58
DDR_A_D59
DDR_A_D36
DDR_A_D37
DDR_A_DM4
DDR_A_D38
DDR_A_D39
DDR_A_D44
DDR_A_D45
DDR_A_DQS#5
DDR_A_DQS5
DDR_A_D46
DDR_A_D47
DDR_A_D52
DDR_A_D53
DDR_A_DM6
DDR_A_D54
DDR_A_D55
DDR_A_D60
DDR_A_D61
DDR_A_DQS#7
DDR_A_DQS7
DDR_A_D62
DDR_A_D63
PM_EXTTS#0 8,15
CLK_SMBDATA 15,16
CLK_SMBCLK 15,16
+0.75VS
+3VS
R102 1 2 10K_0402_5%
R103 1 2 10K_0402_5%
C166
2.2U_0603_6.3V4Z
C167
0.1U_0402_16V4Z
FOX_AS0A626-U4RN-7F
+0.75VS
ME@
+1.5V
@
C152
470U_D2_2.5VM_R15
C148
10U_0805_6.3V6M
C149
10U_0805_6.3V6M
C150
10U_0805_6.3V6M
C151
10U_0805_6.3V6M
C153
10U_0805_6.3V6M
+1.5V
C154
10U_0805_6.3V6M
C155
0.1U_0402_16V4Z
C156
0.1U_0402_16V4Z
C157
0.1U_0402_16V4Z
C158
0.1U_0402_16V4Z
Layout Note: Place these 4 Caps near Command and Control signals of JDDR1
Layout Note: Place near JDDR1
+0.75VS
+0.75V is controller by SUSP for saving power on S3
C161
10U_0805_6.3V6M
C162
1U_0603_10V4Z
C163
1U_0603_10V4Z
C164
1U_0603_10V4Z
C165
1U_0603_10V4Z
Layout Note: Place near VTT1&VTT2
DDR3 SO-DIMM A
REVERSE TYPE
(5.2mm)
Security Classification
Compal Secret Data
Issued Date
2007/09/29
Deciphered Date
2007/09/29
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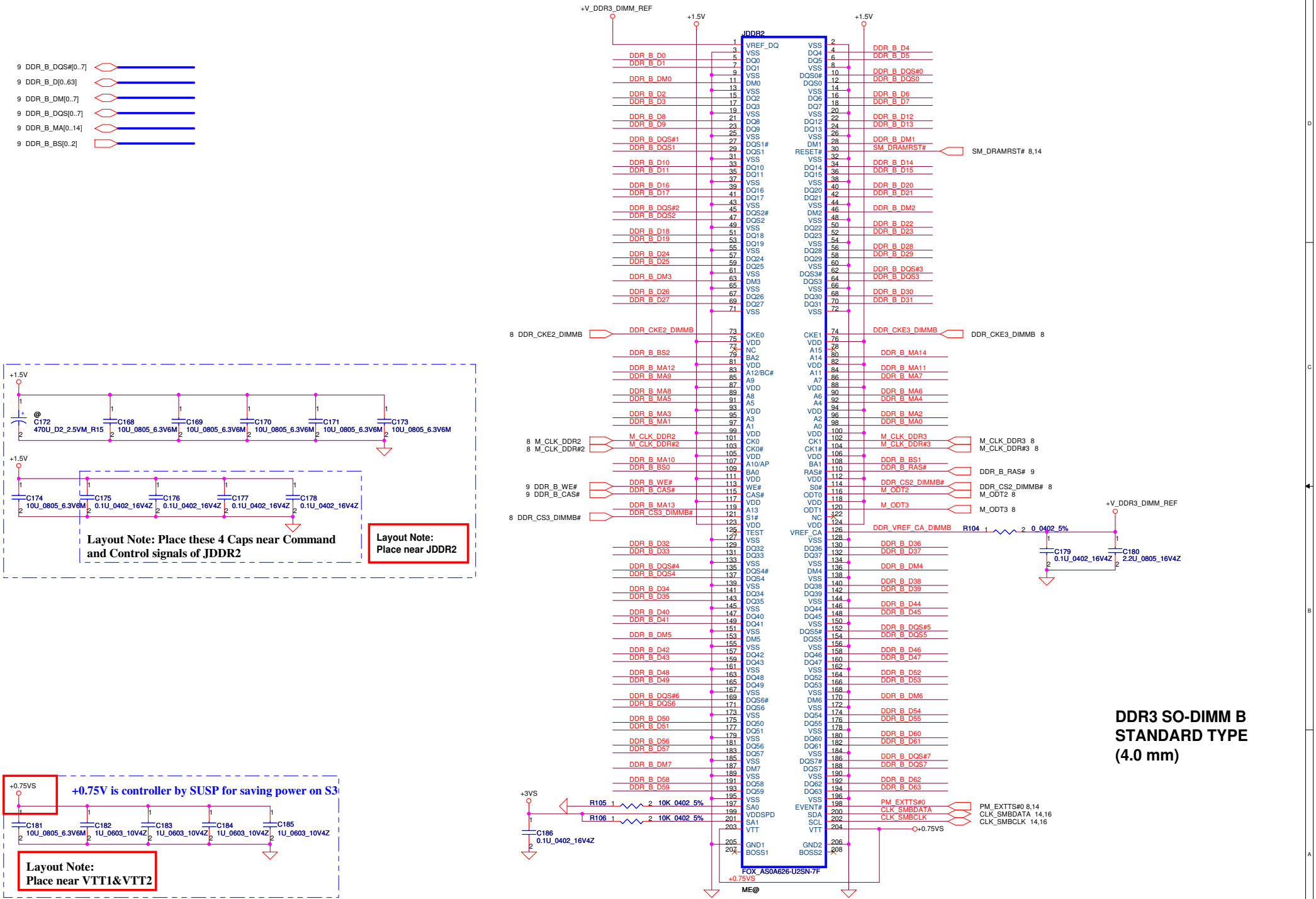
Compal Electronics, Inc.
Title
DDRIII-SODIMM SLOT1
Size
Custom
Document Number
KIUE0_LA-5191P
Rev
1.0
Date:
Wednesday, June 24, 2009
Sheet
14
of
43



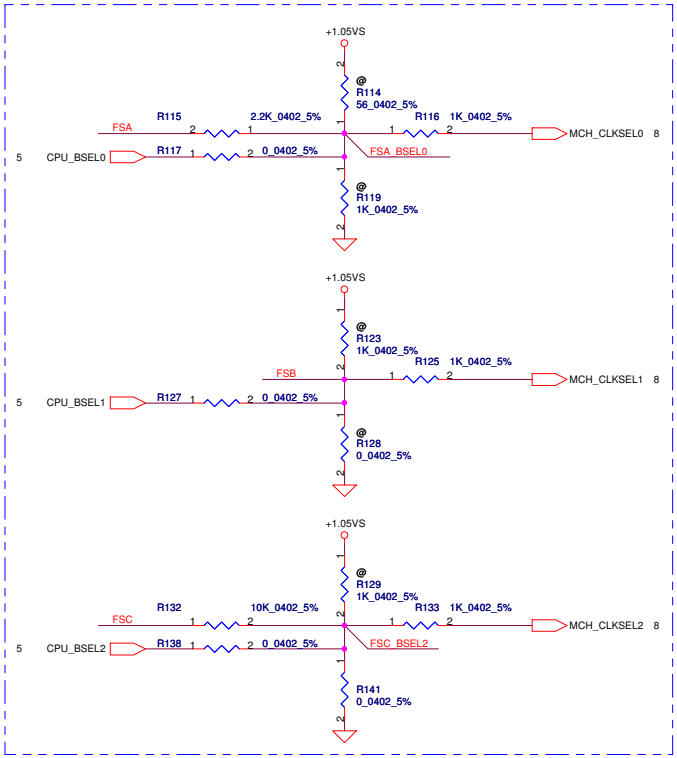
Security Classification	Compal Secret Data		
Issued Date	2007/09/29	Deciphered Date	2007/09/29

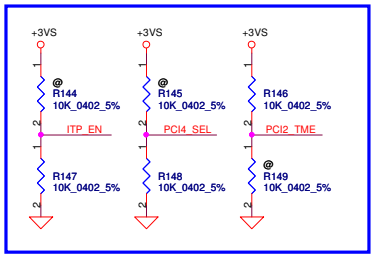
Compal Electronics, Inc.			
Title	DDRIII-SODIMM SLOT2		
Size	Document Number KIUE0_LA-5191P		Rev 1.0
Date: Wednesday, June 24, 2009		Sheet 15 of 43	

FSC CLKSEL2	FSB CLKSEL1	FSA CLKSEL0	CPU MHz	SRC MHz	PCI MHz	REF MHz	DOT_96 MHz	USB MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					

SA000020K00 (Silego : SLG8SP556VTR)

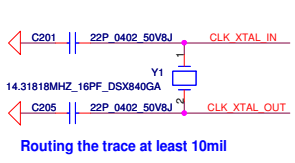
SA000020H00 (ICS : ICS9LPRS387AKLFT)



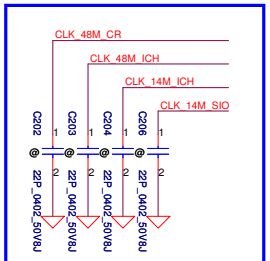


For ITP_EN, 0 =SRC8/SRC8#(100MHz); 1 = ITP/ITP#(266MHz)

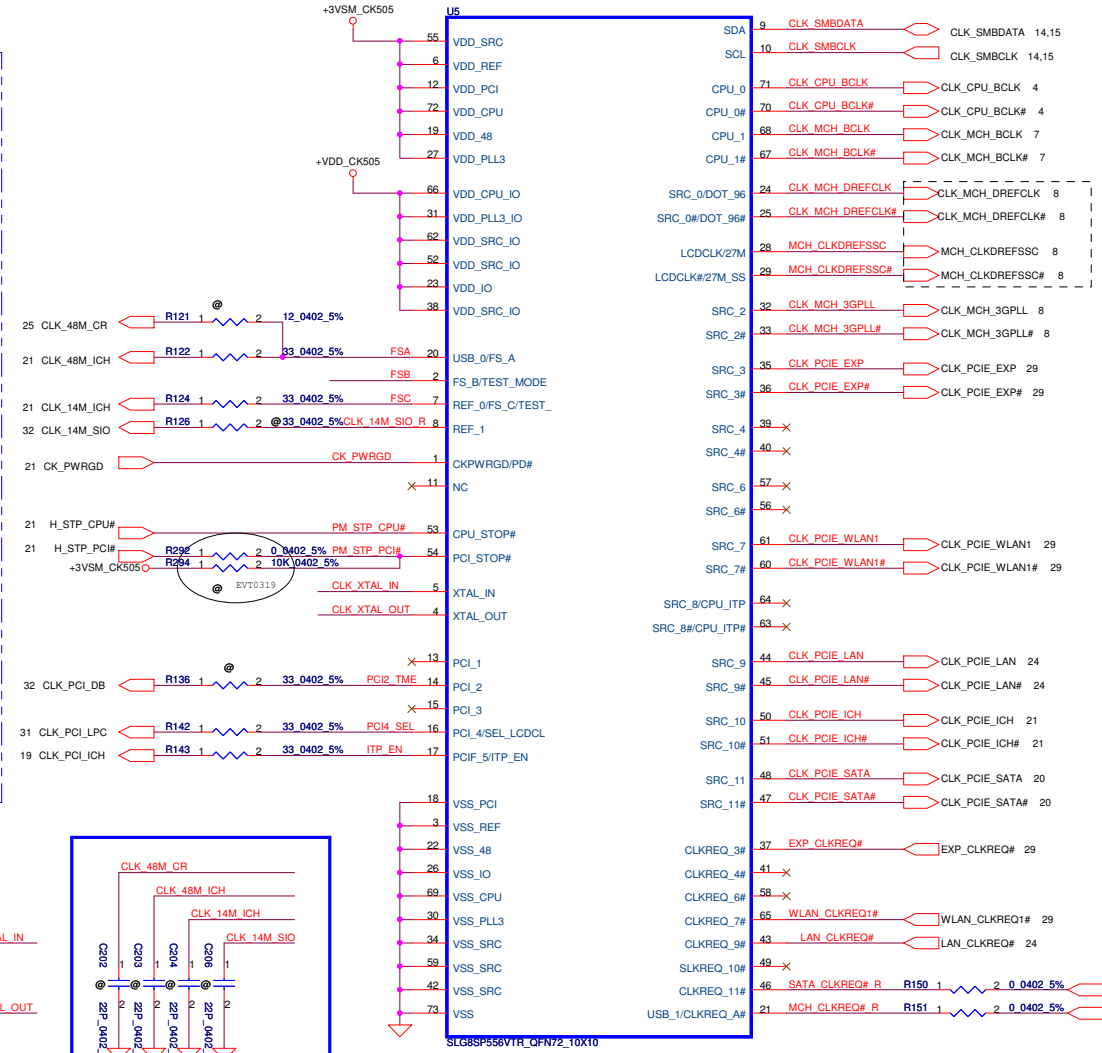
For PCI4_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#(UMA)
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS(DISCRETE)



Routing the trace at least 10mil



place CAPs near Resistors of U10
For 3G RF noise .



SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_EXP#
SRC4	
SRC6	
SRC7	PCIE_WLAN1
SRC8	
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_SATA

REQ PORT LIST

PORT	DEVICE
REQ_3#	PCIE_EXP#
REQ_4#	
REQ_6#	
REQ_7#	PCIE_WLAN1
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_SATA
REQ_A#	MCH_3GPLL

Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

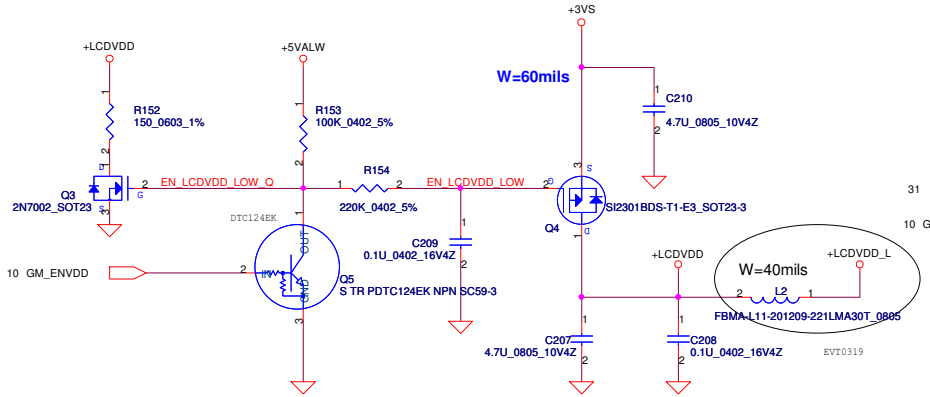
Compal Electronics,Ltd.

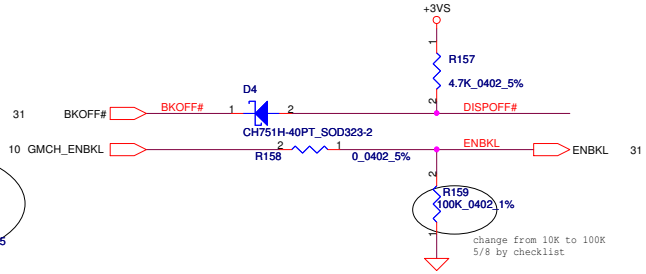
Title: Clock Generator CK505

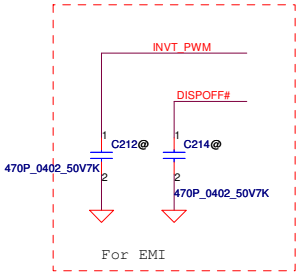
Size: Custom | Document Number: KIUE0_LA-5191P | Rev: 1.0

Date: Wednesday, June 24, 2009 | Sheet 16 of 43

LCD POWER CIRCUIT

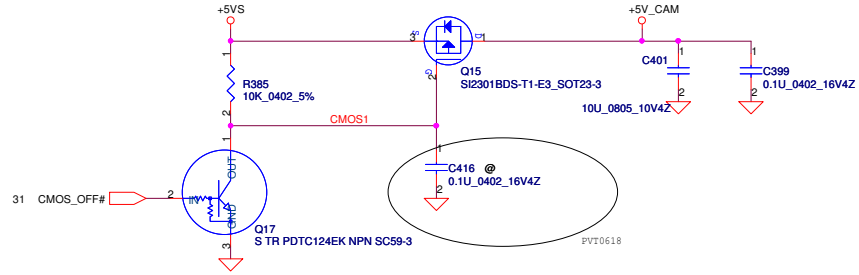


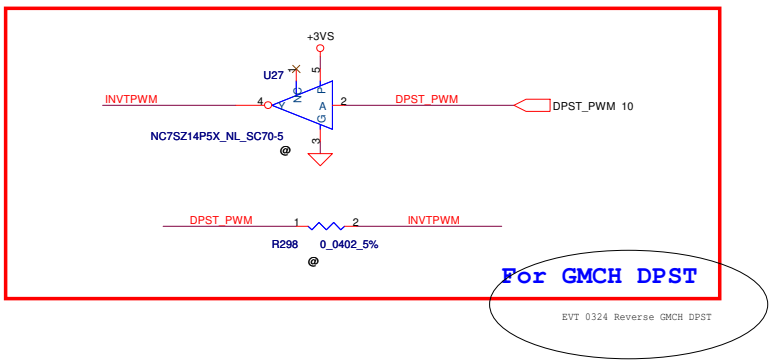


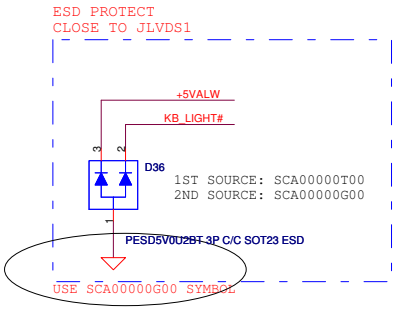


PANEL Logic Power 250mA (typ 3.15v)

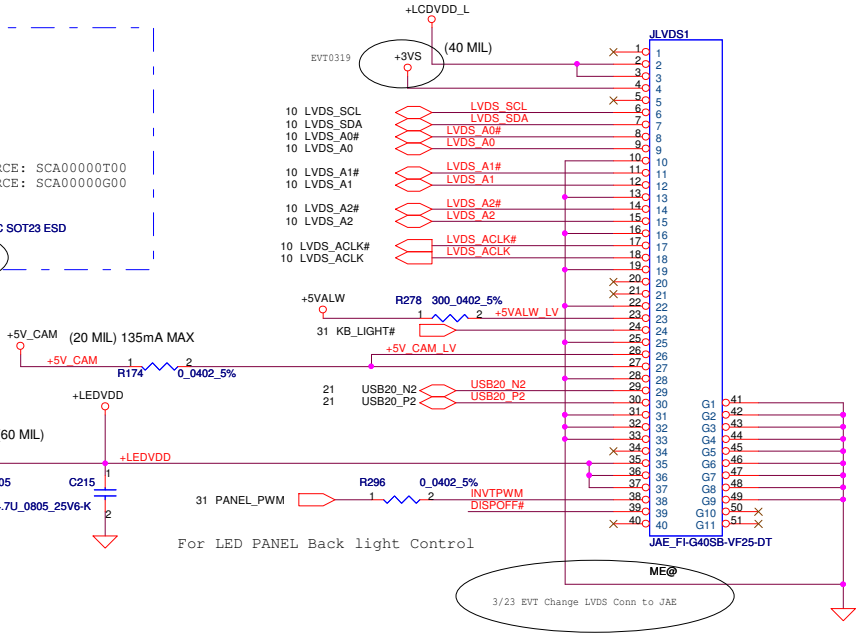
CMOS Camera POWER CIRCUIT







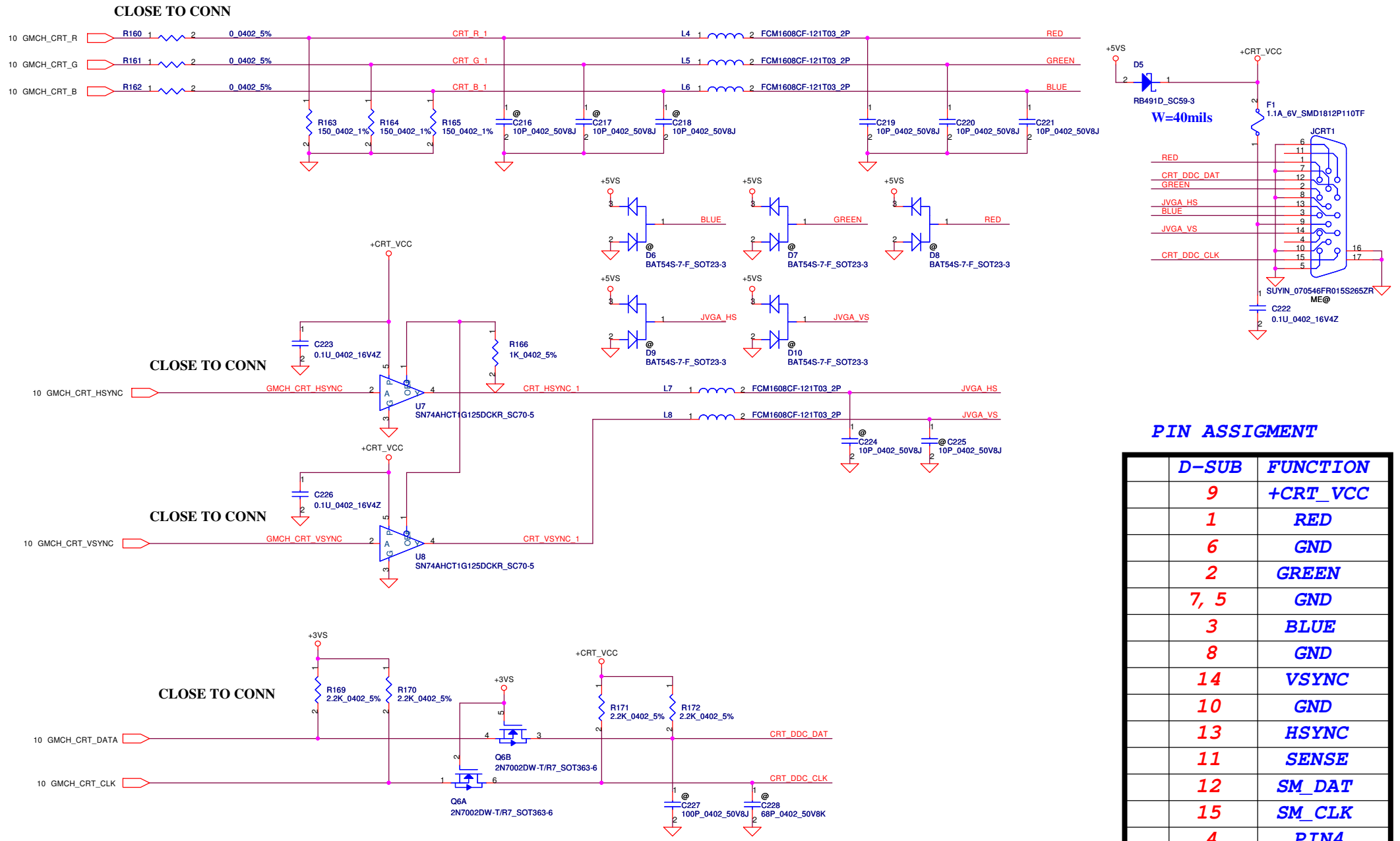
COMBINE CABLE LEFT for LVDS/KB_LI/CMOS LCD/PANEL BD. Conn.



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: LVDS & DVI Connector			
Size: B	Document Number: KIUE0_LA-5191P		Rev: 1.0
Date: Wednesday, June 24, 2009	Sheet 17 of 43		

CRT Connector



PIN ASSIGMENT

	D-SUB	FUNCTION
	9	+CRT_VCC
	1	RED
	6	GND
	2	GREEN
	7, 5	GND
	3	BLUE
	8	GND
	14	VSYNC
	10	GND
	13	HSYNC
	11	SENSE
	12	SM_DAT
	15	SM_CLK
	4	PIN4

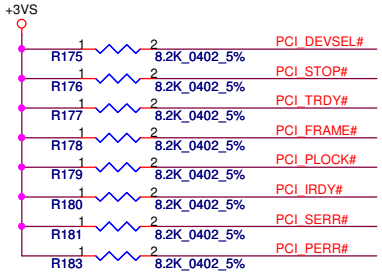
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

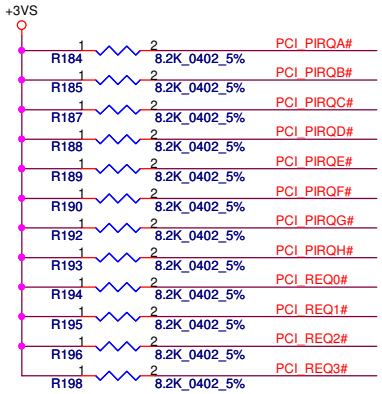
Compal Electronics, Inc.

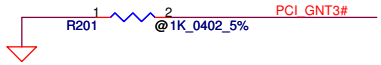
Title: CRT & TV-OUT Connector

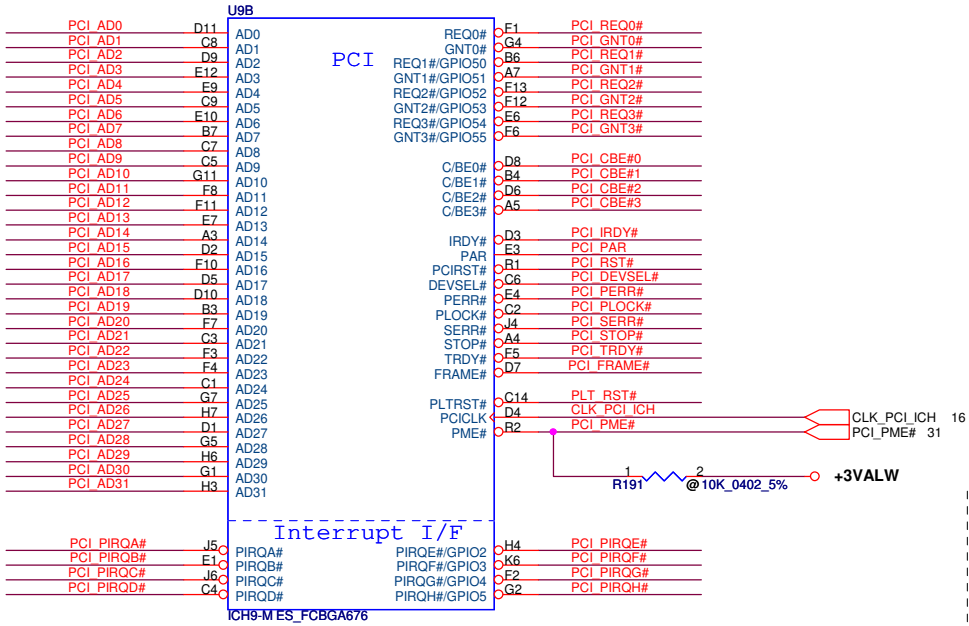
Size: Custom | Document Number: KIUE0_LA-5191P | Rev: 1.0

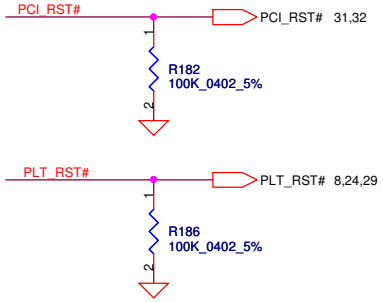
Date: Wednesday, June 24, 2009 | Sheet 18 of 43

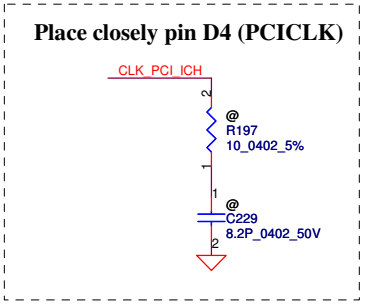


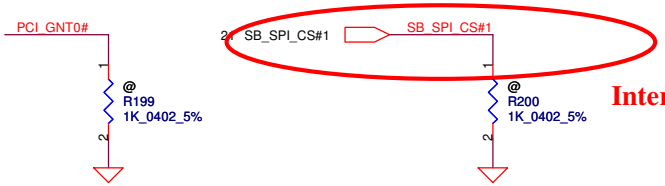










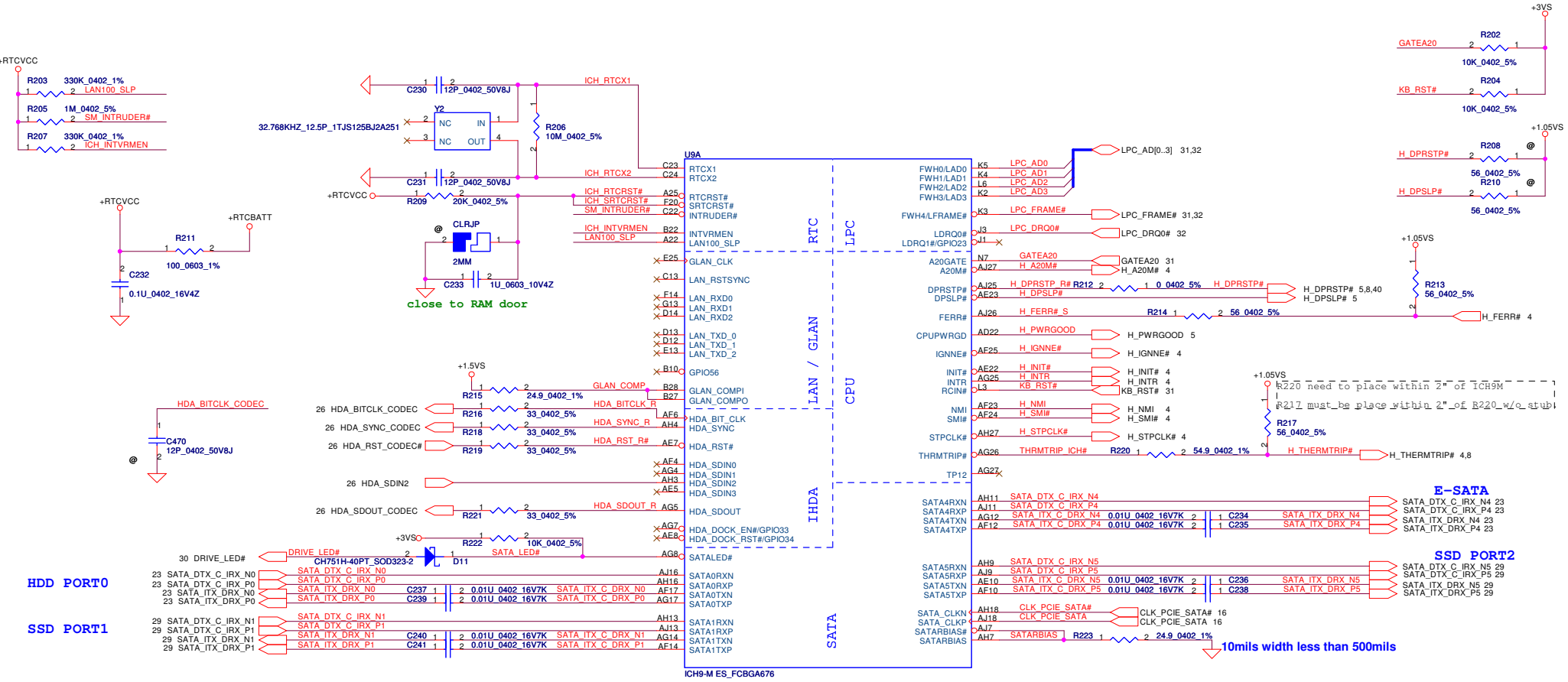


A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: ICH9M(1/4)-PCI			
Size	Document Number: KIUE0_LA-5191P		Rev: 1.0
Date: Wednesday, June 24, 2009	Sheet 19 of 43		



XOR Chain Entrance Strap		
ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation
1	1	Set PCIE port config bit 1

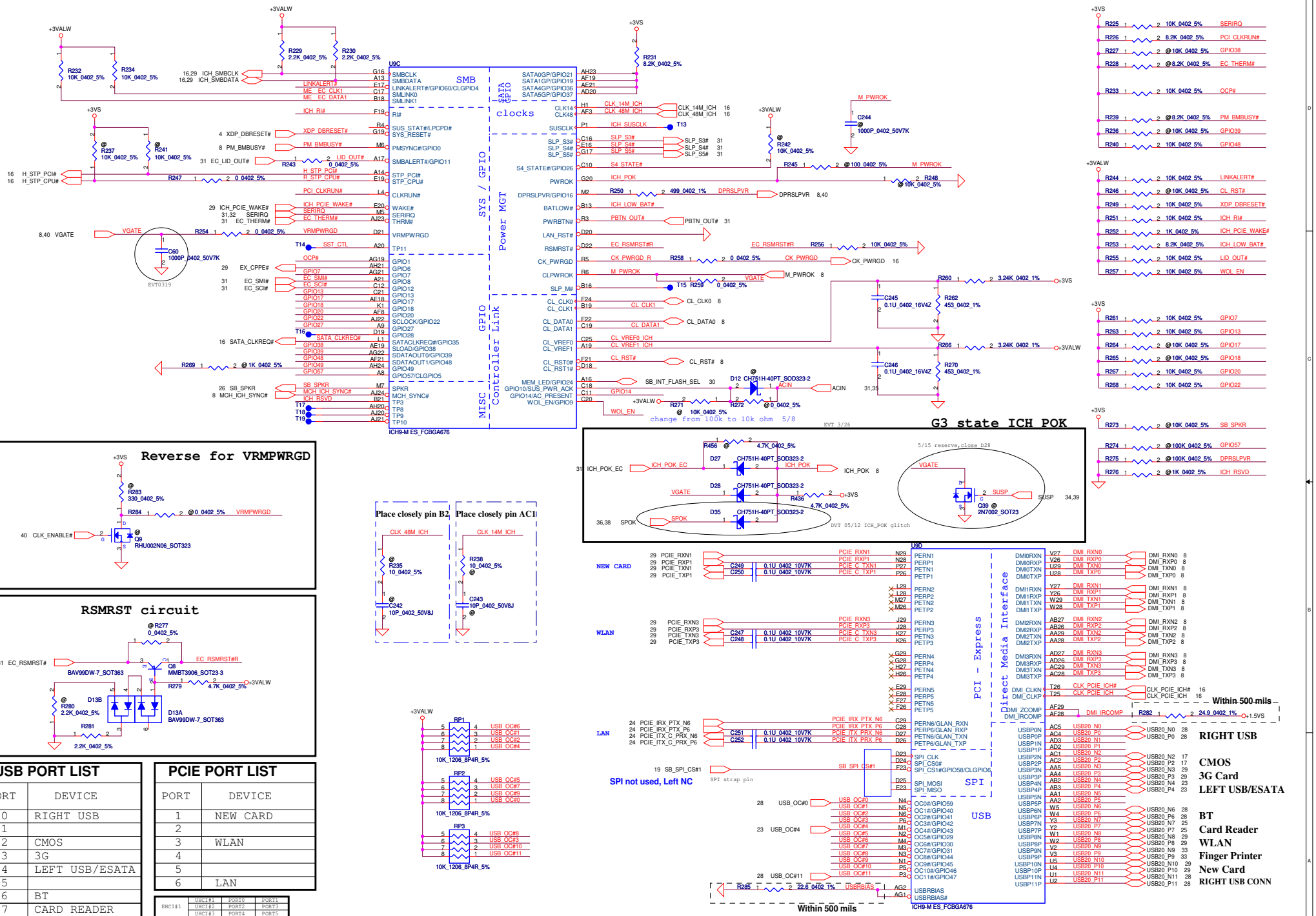
SATA PORT LIST	
PORT	DEVICE
0	HDD
1	Mini-Card SSD PORT1
4	E-SATA
5	Mini-Card SSD PORT2

Compal Electronics, Inc.

Title: ICH9M(2/4)-LAN,IDELPC,RTC

Size: Custom | Document Number: KIUE0_LA-5191P | Rev: 1.0

Date: Wednesday, June 24, 2009 | Sheet 20 of 43



USB PORT LIST

PORT	DEVICE
0	RIGHT USB
1	
2	CMOS
3	3G
4	LEFT USB/ESATA
5	
6	BT
7	CARD READER
8	WIRELESS
9	Finger Print
10	NEW CARD
11	RIGHT USB CONN

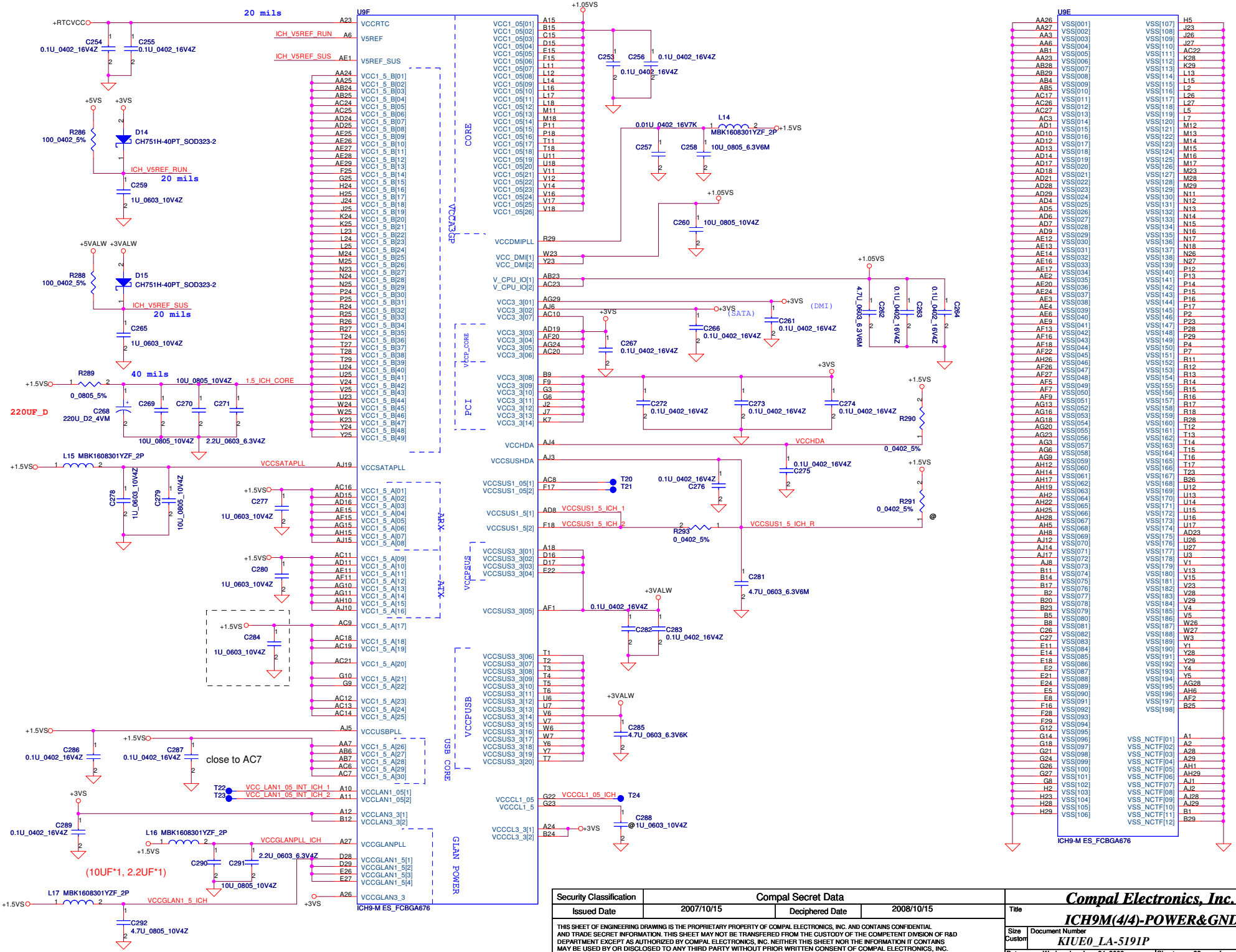
PCIE PORT LIST

PORT	DEVICE
1	NEW CARD
2	
3	WLAN
4	
5	
6	LAN

EHCI#1	USB_OC#1	PORT0	PORT1
	USB_OC#2	PORT2	PORT3
	USB_OC#3	PORT4	PORT5
EHCI#2	USB_OC#4	PORT6	PORT7
	USB_OC#5	PORT8	PORT9
	USB_OC#6	PORT10	PORT11

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

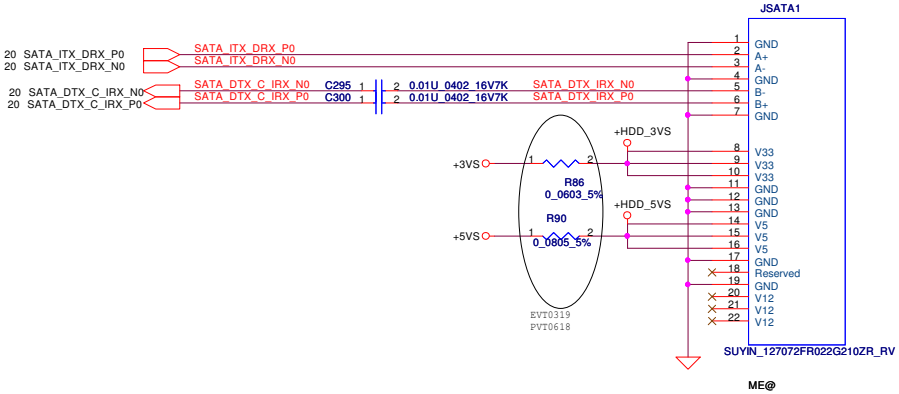
Compal Electronics, Inc.			
Title	ICH9M(3/4)-USB,GPIO,PCIE		
Size C	Document Number KIUE0_LA-5191P		Rev 1.0
Date: Wednesday, June 24, 2009	Sheet 21 of 43		

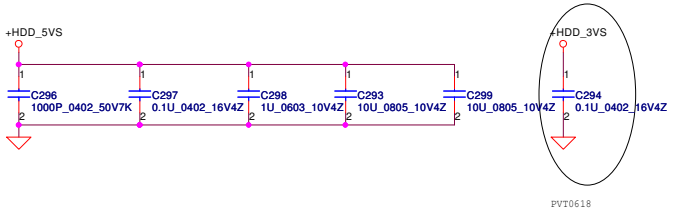


Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

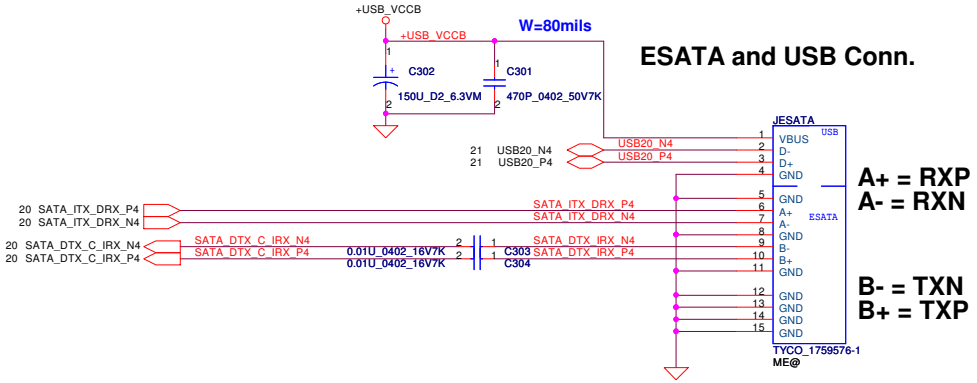
Compal Electronics, Inc.			
Title: ICH9M(4/4)-POWER&GND			
Size: Custom	Document Number: KIUE0_LA-5191P		Rev: 1.0
Date: Wednesday, June 24, 2009	Sheet 22 of 43		

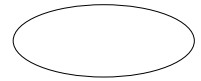
SATA HDD Conn.



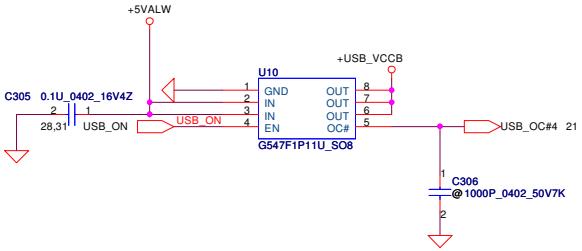


ESATA and USB Conn.



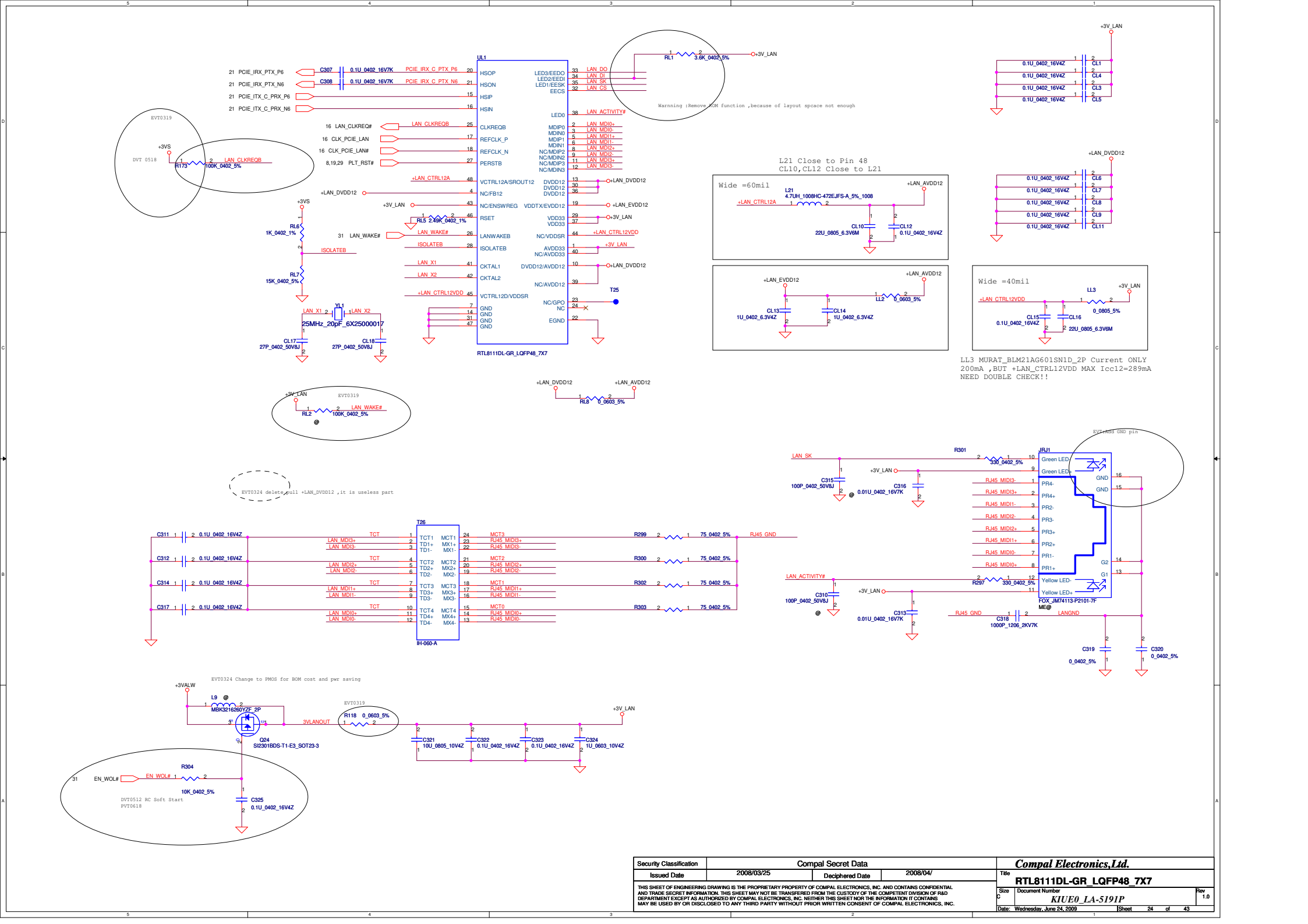


3/26 Remove ESD Diode ,by AndyYL



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title: HDD & ODD Connector			
Size: B	Document Number: KIUE0_LA-5191P		Rev: 1.0
Date: Wednesday, June 24, 2009	Sheet 23 of 43		



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Issued Date	2008/03/25	Deciphered Date	2008/04/

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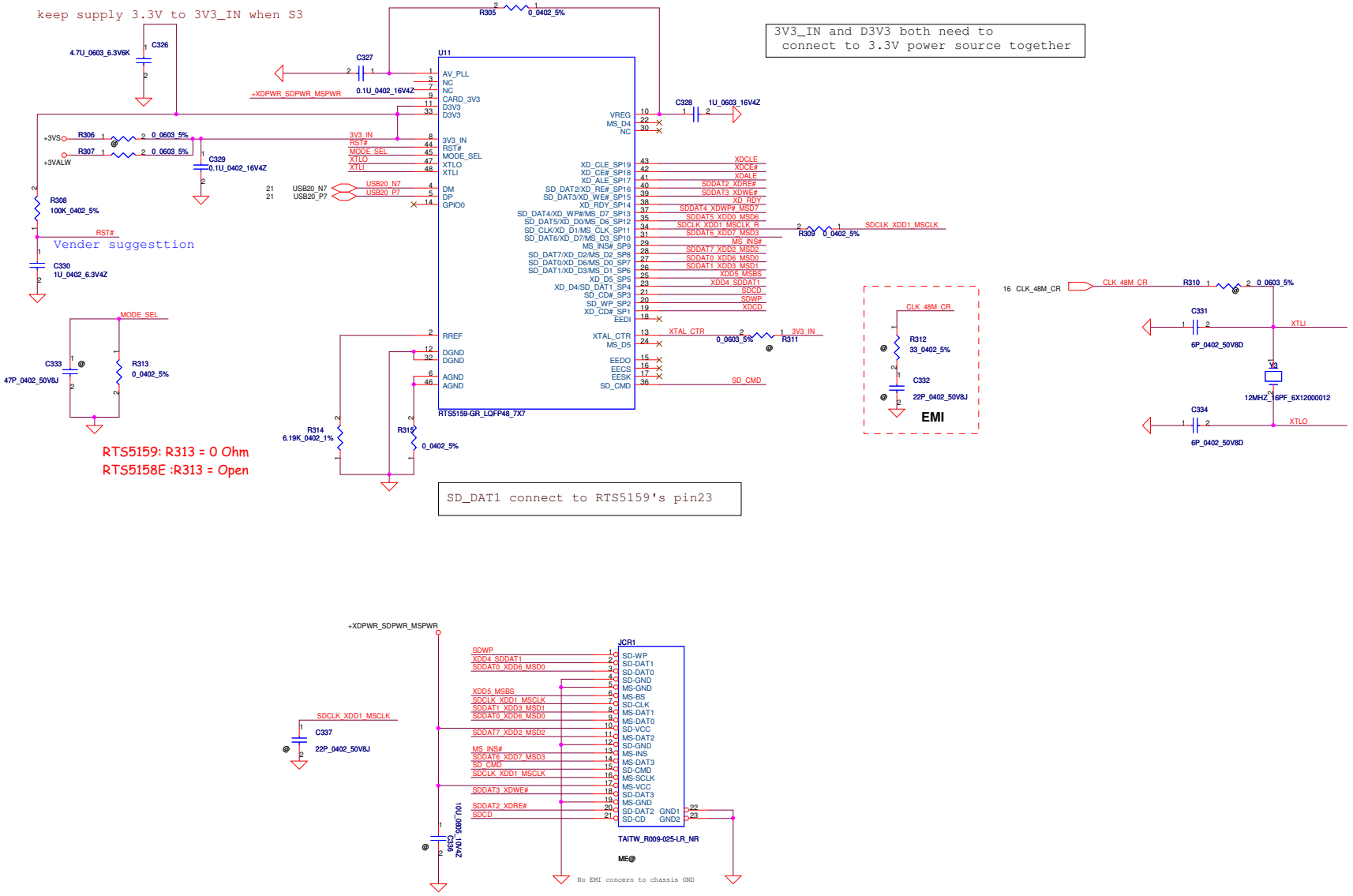
Title: RTL8111DL-GR_LQFP48_7X7

Size	Document Number	Rev
C	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 Sheet 24 of 43



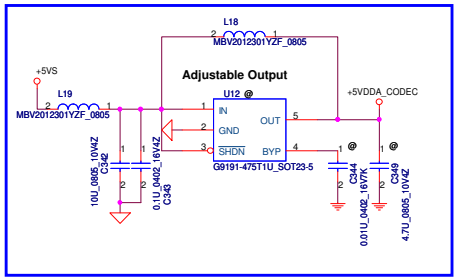
Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

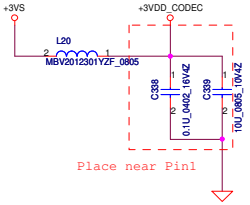
Compal Electronics,Ltd.

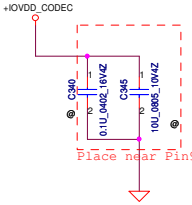
Title: RTS5159-VCC-GRT CARD READER

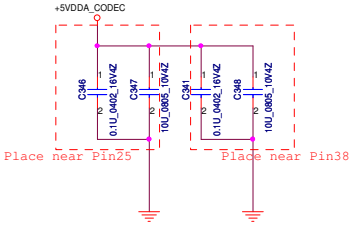
Size	Document Number	Rev
C	KIUE0_LA-5191P	1.0

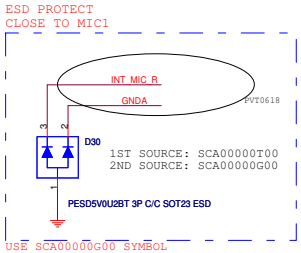
Date: Wednesday, June 24, 2009 Sheet 25 of 43

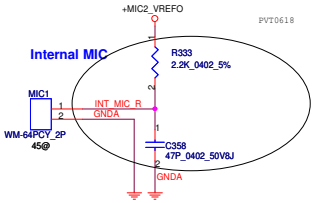


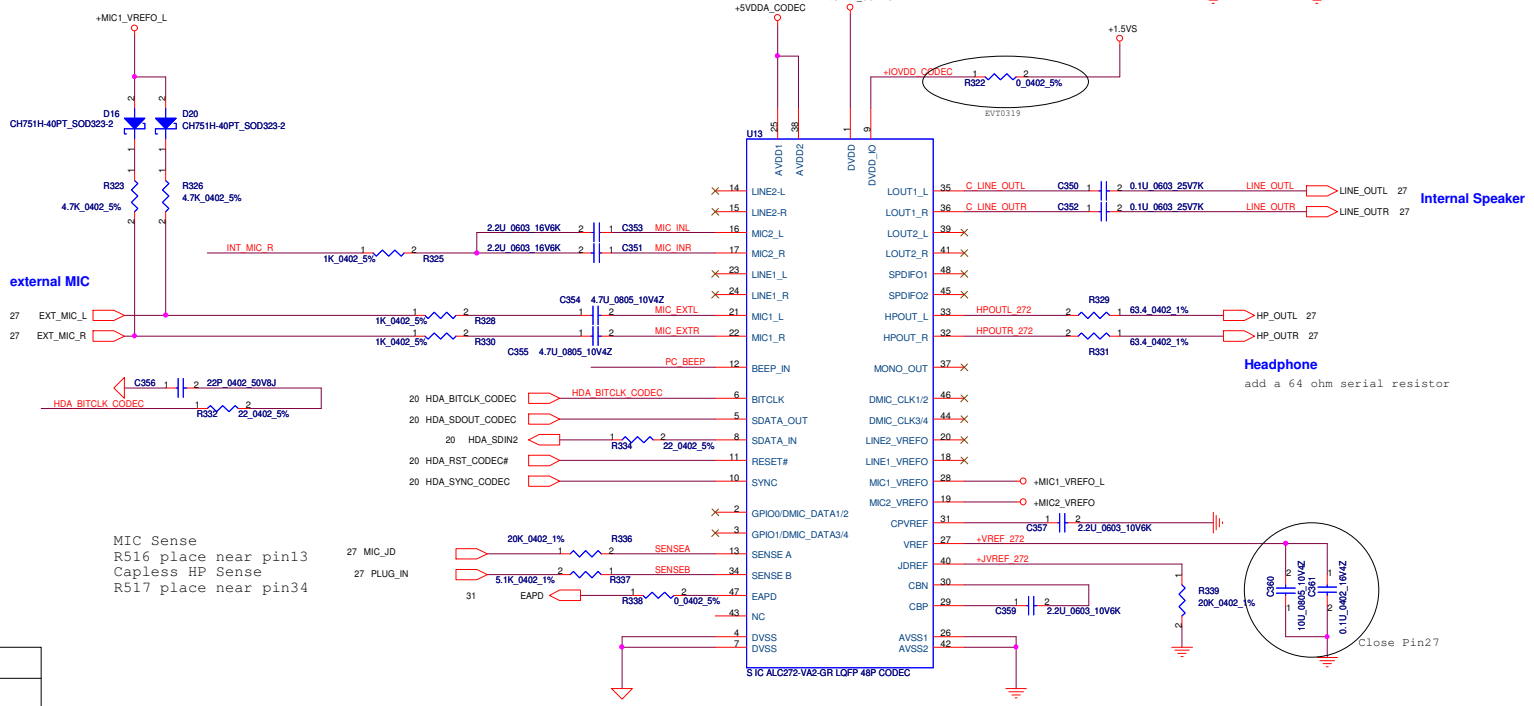








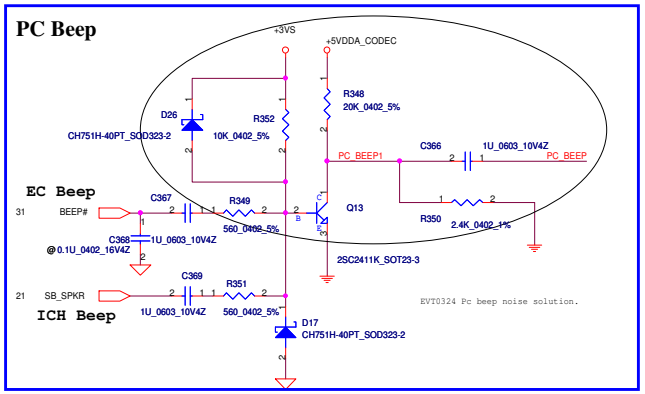


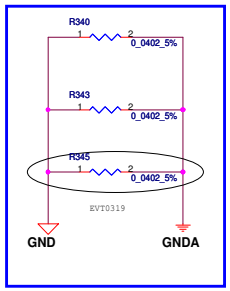


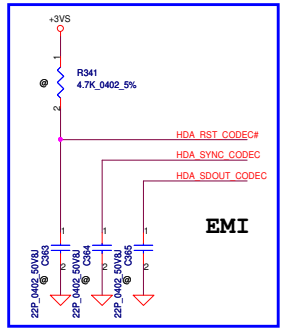
MIC Sense
R516 place near pin13
Capless HP Sense
R517 place near pin34

27 MIC_JD
27 PLUG_IN
20K_0402_1% R336
5.1K_0402_1% R337
31 EAPD
R338 0_0402_5%
SENSEA
SENSEB

Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	NOT USE
MIC1(Pin21/22)	External	Mic in
MONO-OUT(Pin37)	Internal	NOT USE
MIC2(Pin16/17)	Internal	Internal Mic







Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

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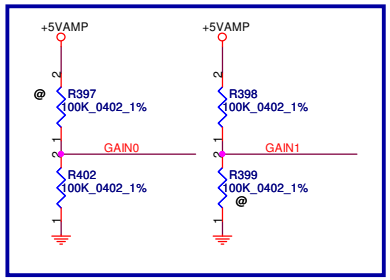
Compal Electronics,Ltd.

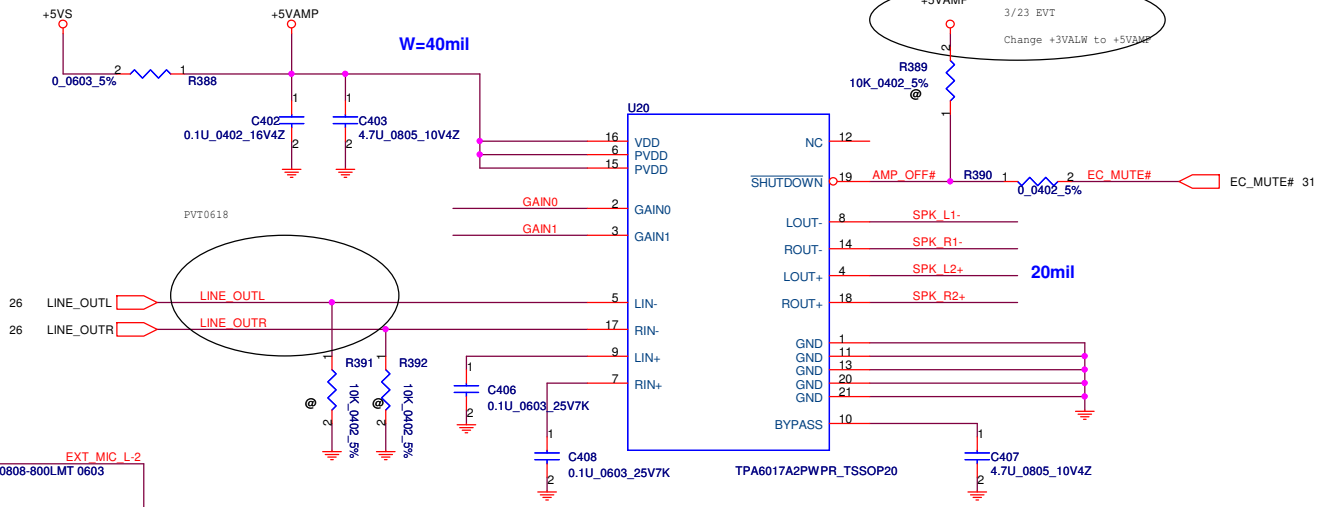
Title: HD Audio Codec_ALC272

Size: C | Document Number: KIUE0_LA-5191P | Rev: 1.0

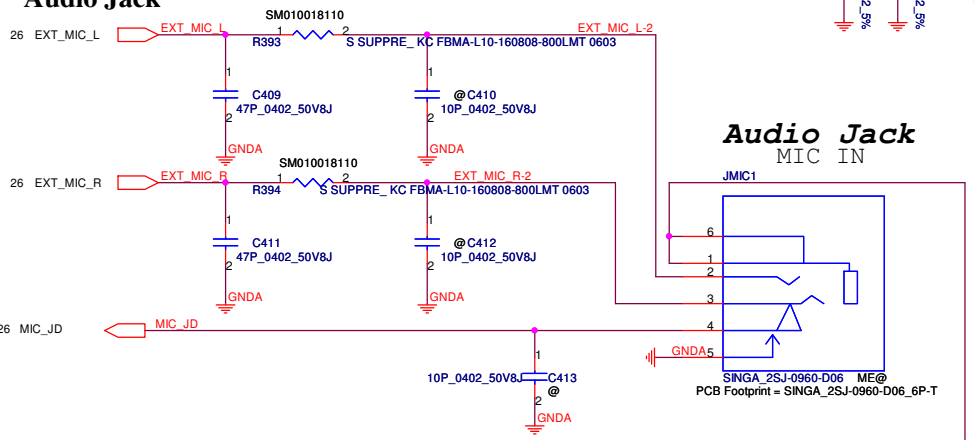
Date: Wednesday, June 24, 2009 | Sheet 26 of 43

GAIN0	GAIN1	
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



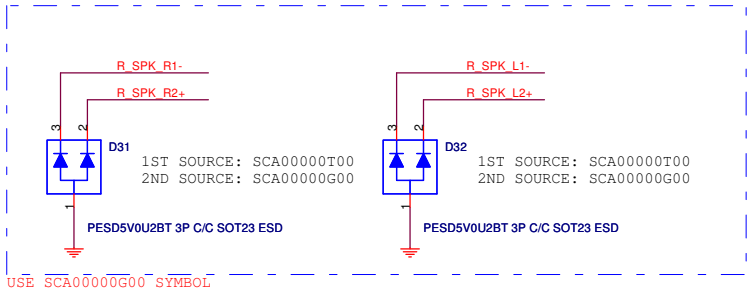


Audio Jack

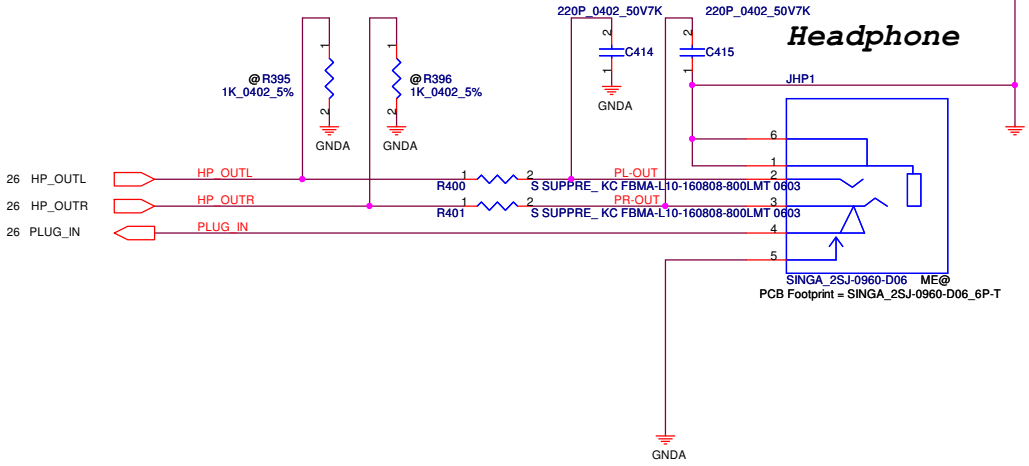


Audio Jack
MIC IN

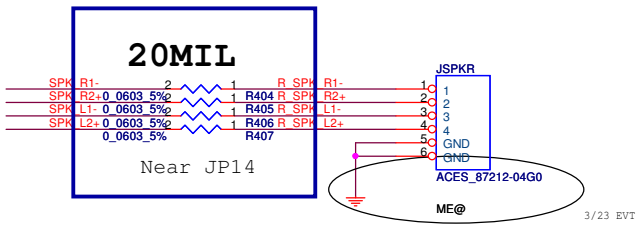
ESD PROTECT



Headphone



SPEAKER JACK

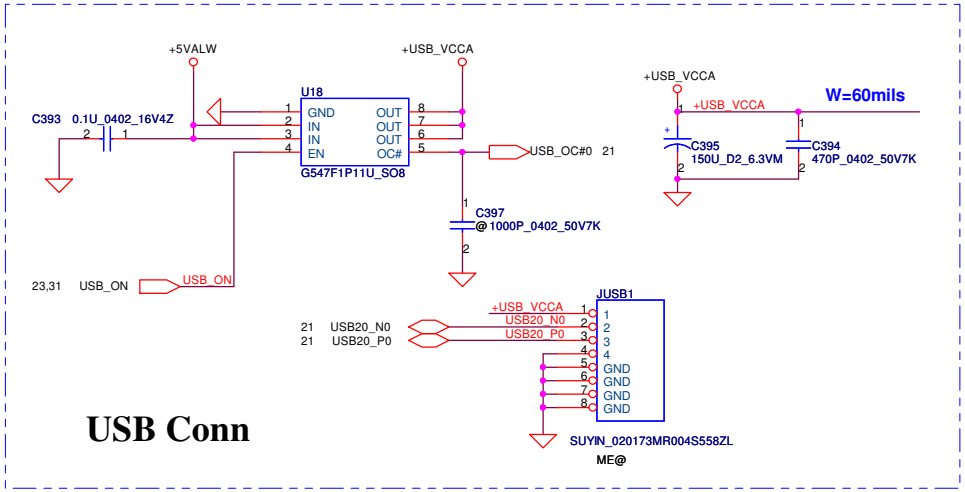


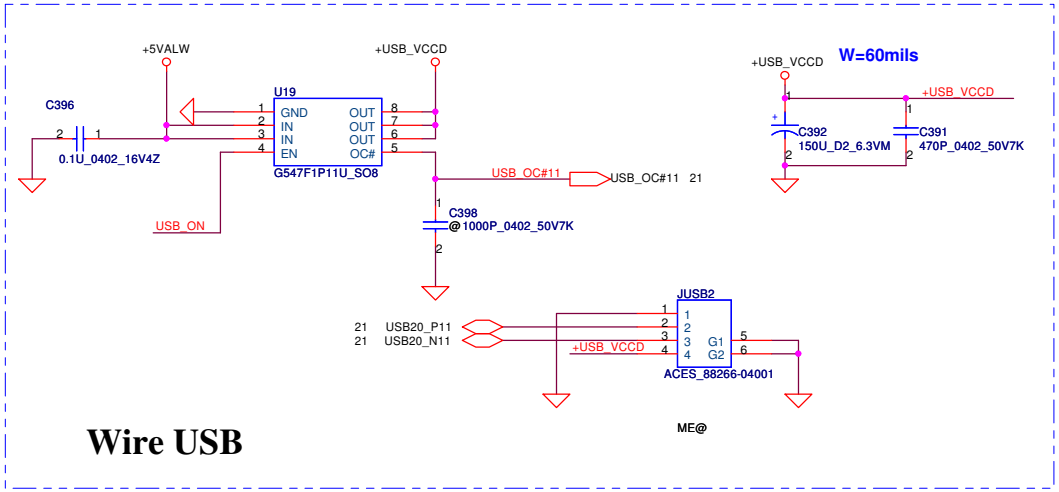
Compal Electronics,Ltd.

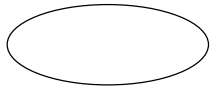
Title: AMP,Audio speaker CONN

Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 Sheet 27 of 43

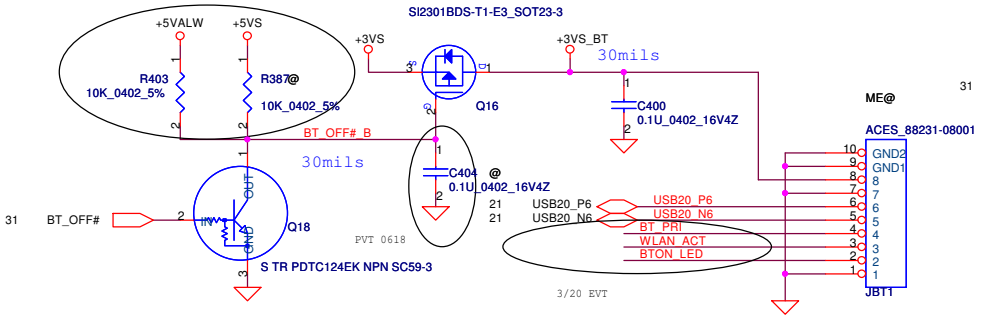


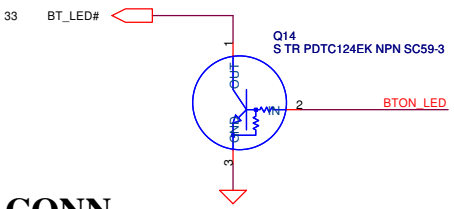




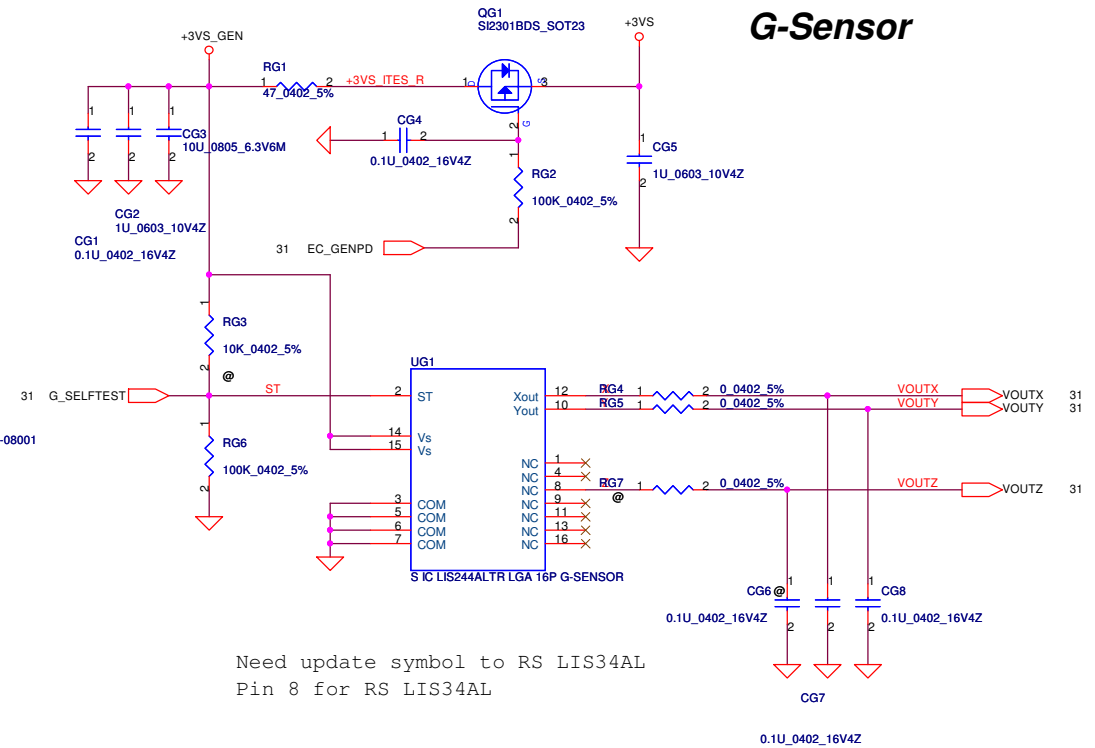
3/26 Remove ESD Diode ,by AndyYL

5/14 Change to +5VALW for floating





G-Sensor



Need update symbol to RS LIS34AL
Pin 8 for RS LIS34AL

BT MODULE CONN

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

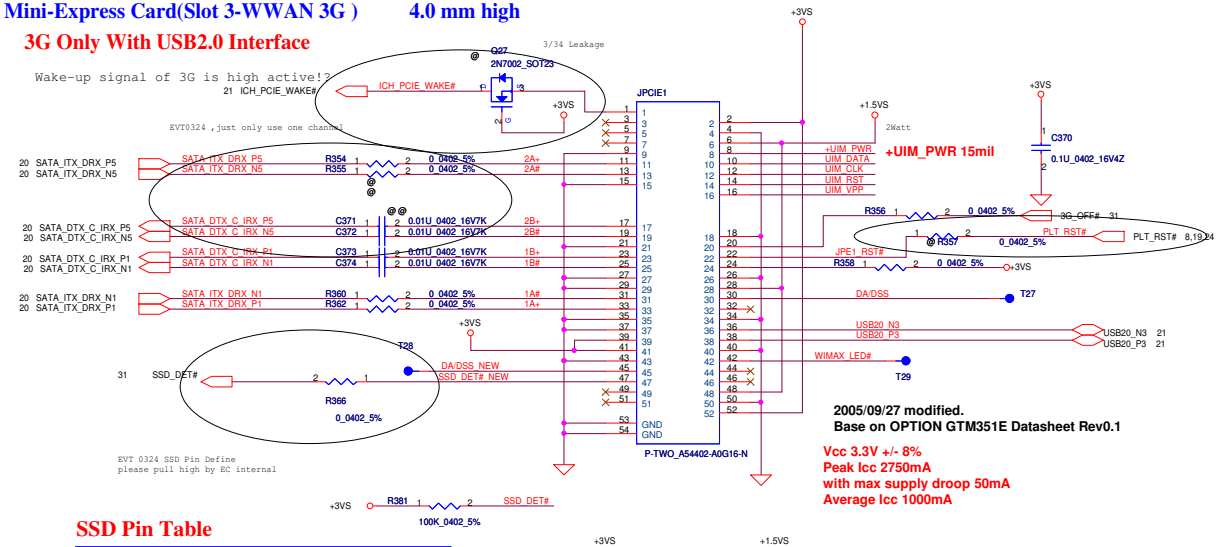
Title: USB/CMOS/BT/G-SENSOR

Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 Sheet 28 of 43

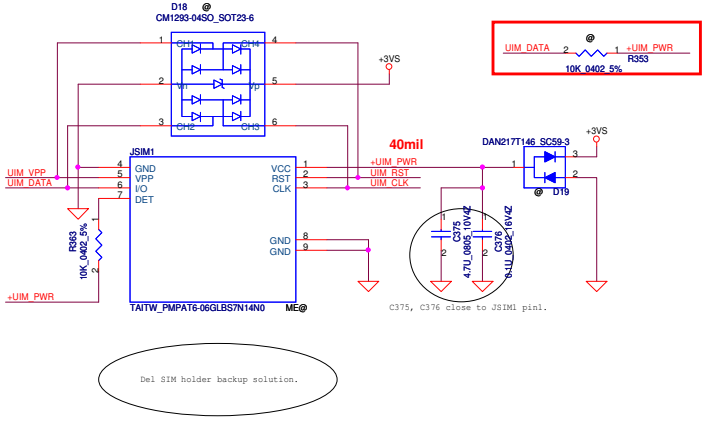
Mini-Express Card(Slot 3-WWAN 3G) 4.0 mm high

3G Only With USB2.0 Interface



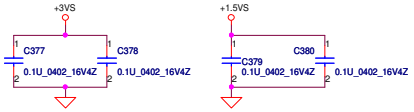
2005/09/27 modified.
Base on OPTION GTM351E Datasheet Rev0.1

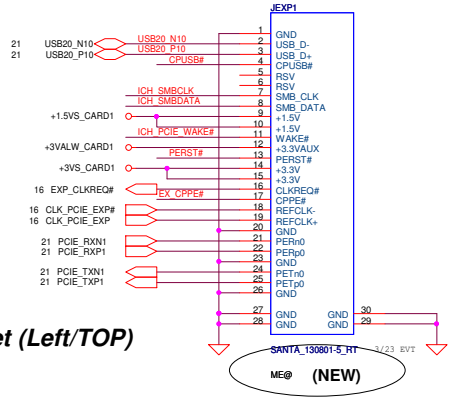
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA



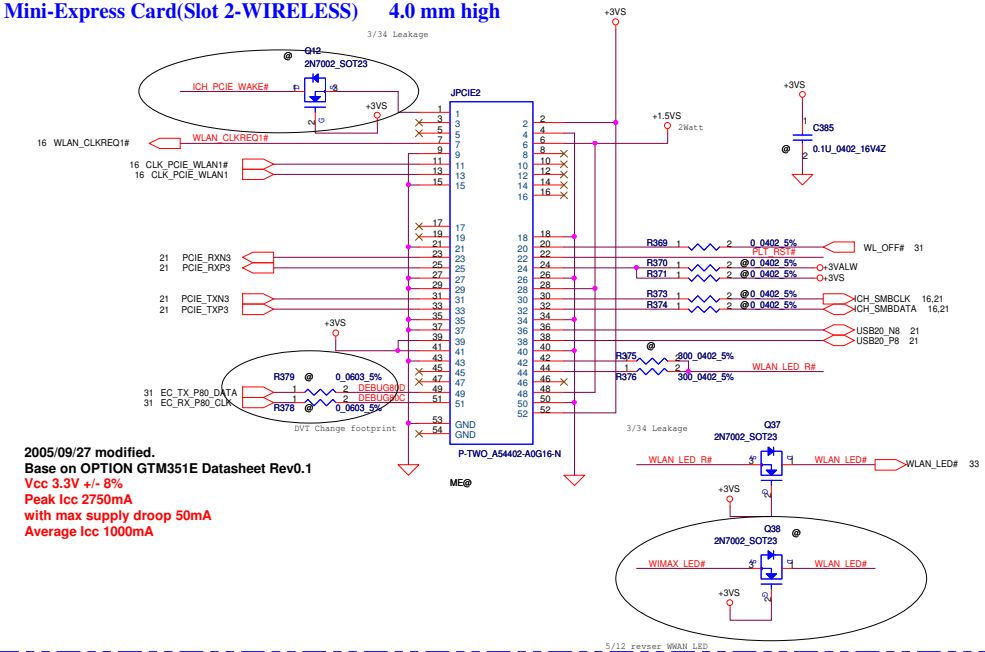
SSD Pin Table

Pin Number	SATA Assignment
11	
13	
17	
19	
23	+B (port 1)
25	-B (port 1)
30	DA/DSS
31	-A (port 1)
32	Presence Detection
33	+A (port 1)





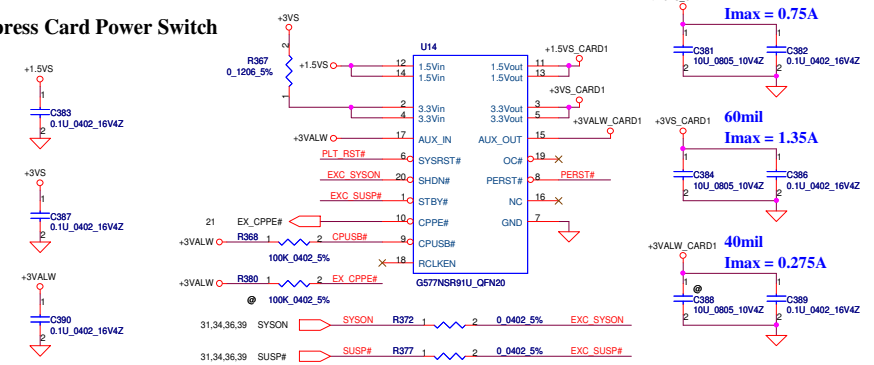
Mini-Express Card(Slot 2-WIRELESS) 4.0 mm high



2005/09/27 modified.
Base on OPTION GTM351E Datasheet Rev0.1
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

New Card 34mm Socket (Left/TOP)

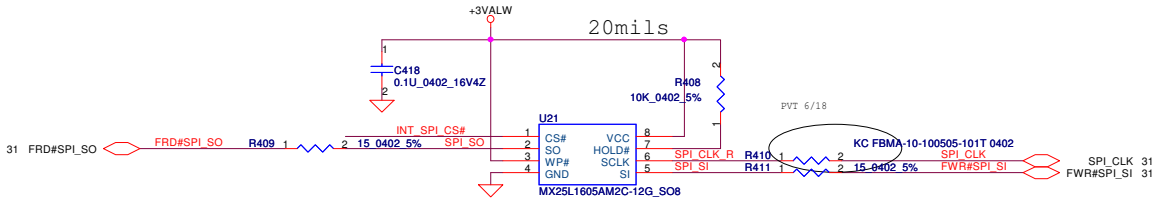
Express Card Power Switch



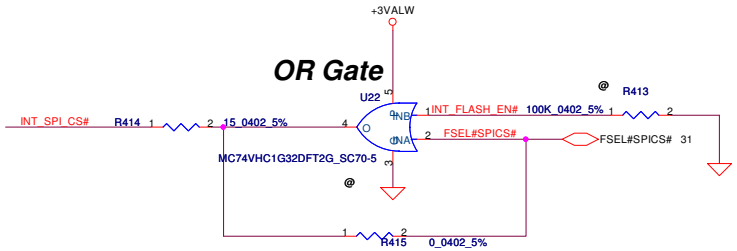
Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

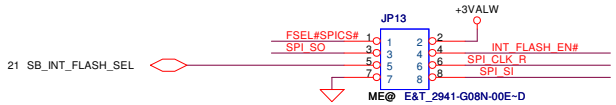
Compal Electronics, Inc.			
Title	Mini-Card/3G/TV /BT		
Size	Document Number	Rev	
	KIUE0_LA-5191P	1.0	
Date: Thursday, June 25, 2009	Sheet 29 of 43		

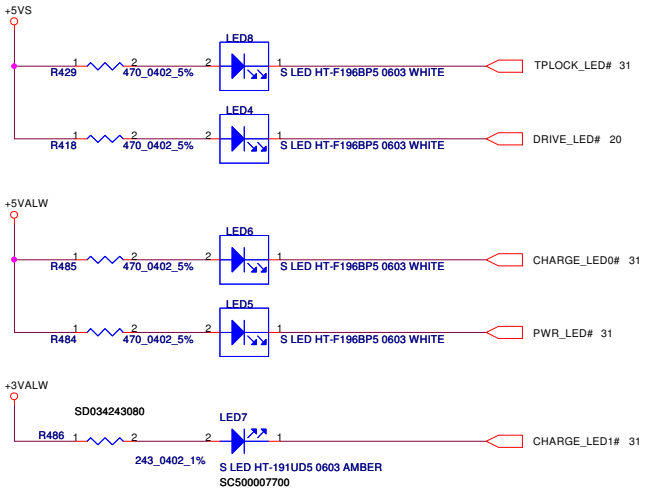
FOR EC 16M SPI ROM



INPUT		OUTPUT
A	B	Y
L	L	L
H	L	H
L	H	H
H	H	H

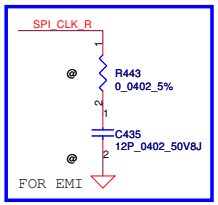


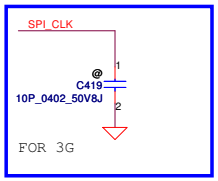




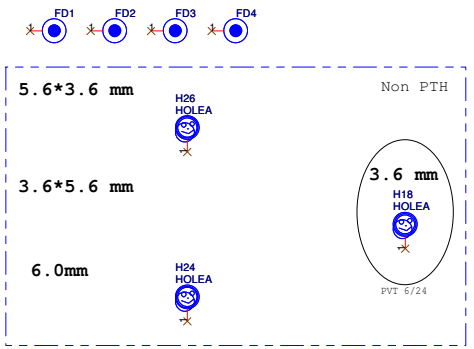
+5VLAW 470 ohm	typ	max
White LED(Vf)	2.8	3.15
current	4.6mA	3.9mA

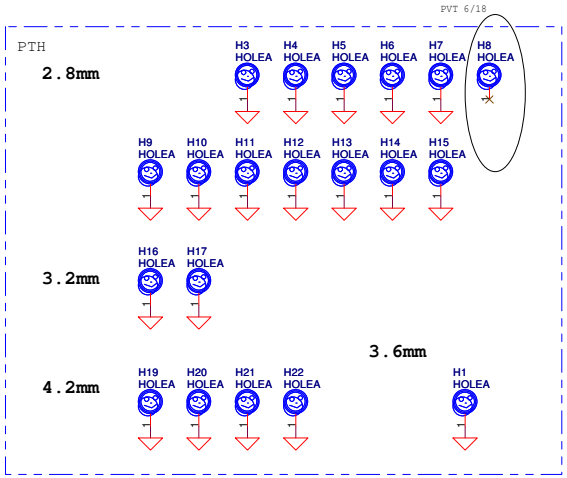
+3.3 VALW 243 ohm	typ	max
Amber LED(Vf)	1.9	2.4
current	5.7mA	3.7mA





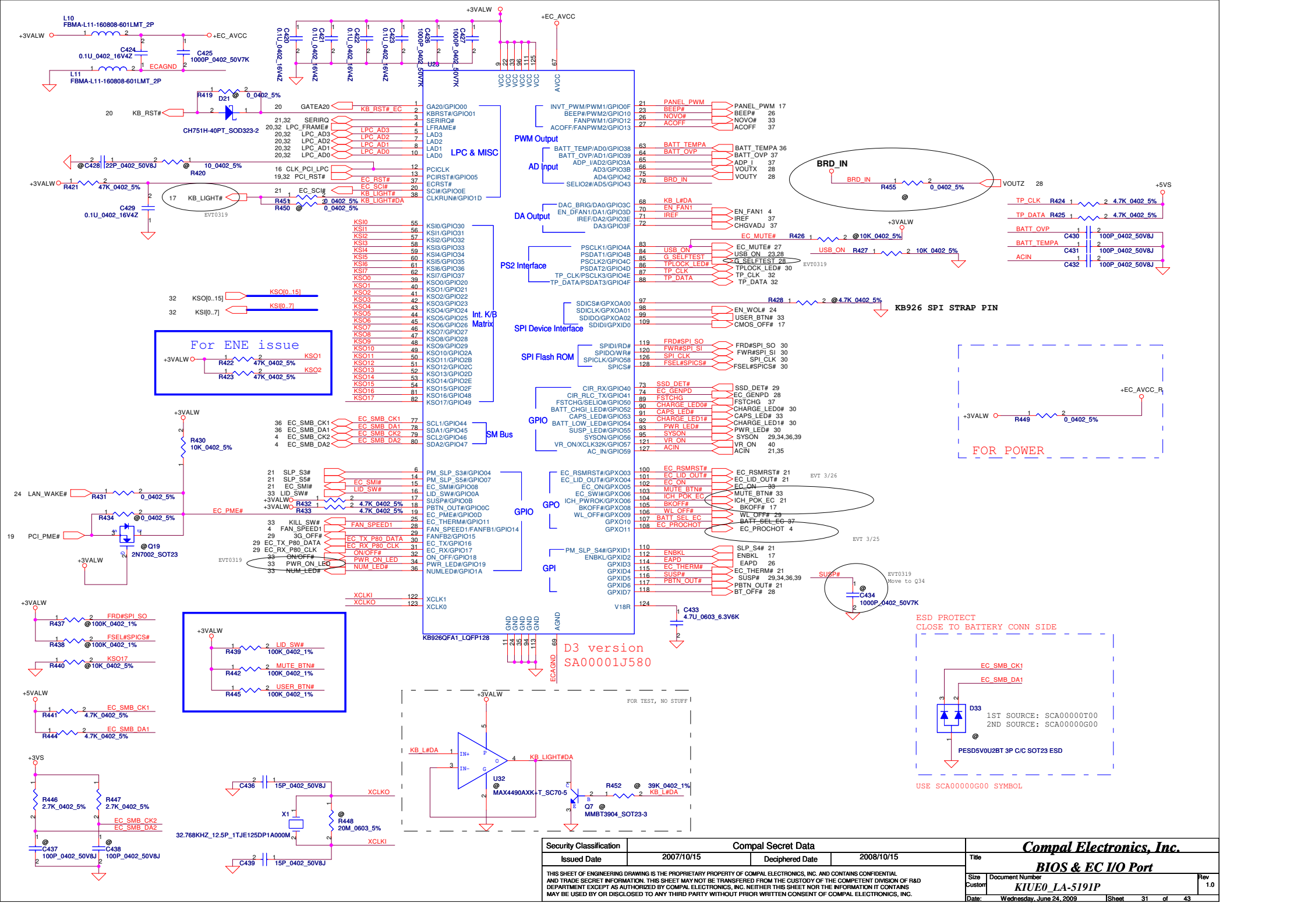
EVT 3/26 **Close EC Pin**





Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

Compal Electronics, Inc.			
Title	LED/EC SPI ROM		
Size B	Document Number KIUE0_LA-5191P		Rev 1.0
Date: Wednesday, June 24, 2009		Sheet 30 of 43	



Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

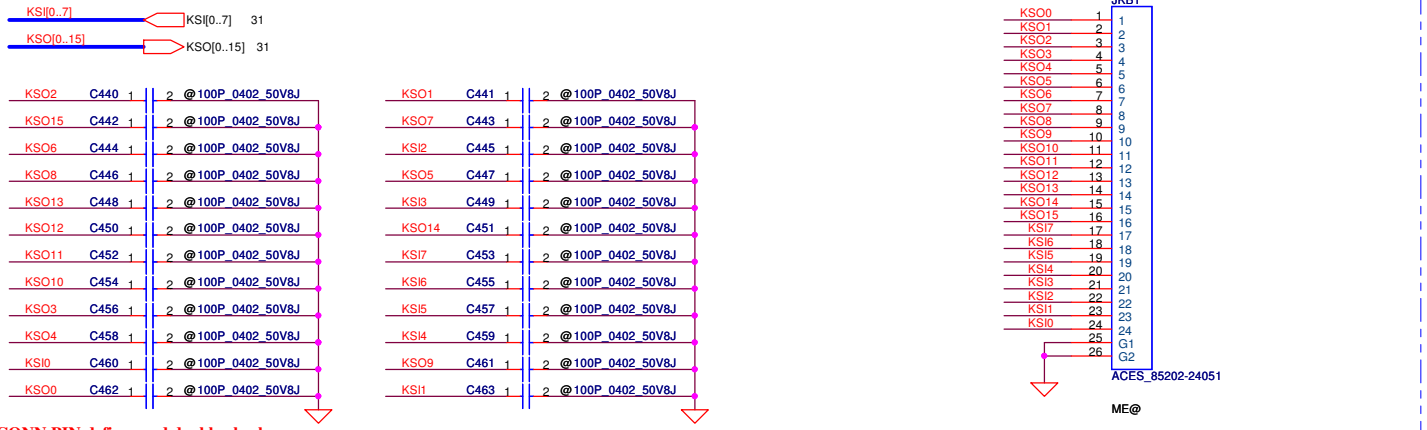
Compal Electronics, Inc.

Title: **BIOS & EC I/O Port**

Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

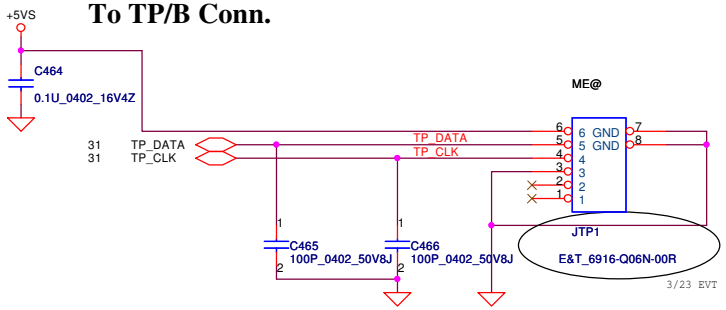
Date: Wednesday, June 24, 2009 Sheet 31 of 43

INT_KBD Conn.



CONN PIN define need double check

To TP/B Conn.

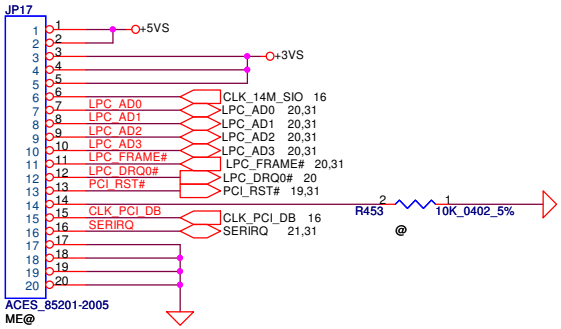


EC DEBUG PORT

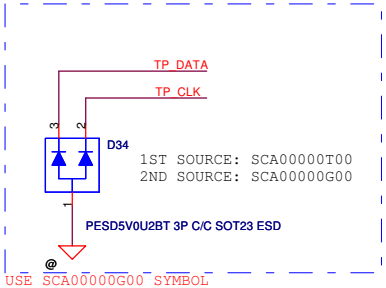
EVT0319

Delete this connector.
It same as MiniPCIE Debug Card.

FOR LPC SIO DEBUG PORT



ESD PROTECT
CLOSE TO JTP1

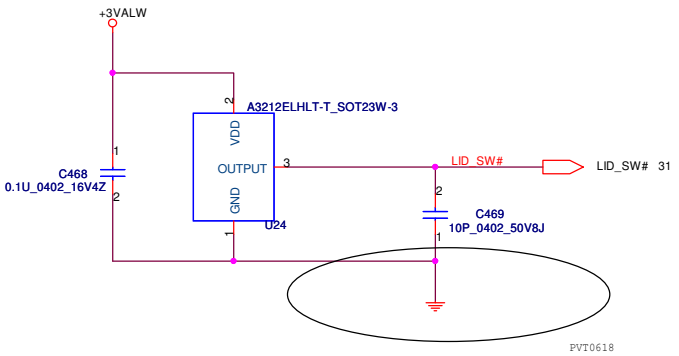


USE SCA00000G00 SYMBOL

Security Classification	Compal Secret Data		
Issued Date	2007/10/15	Deciphered Date	2008/10/15

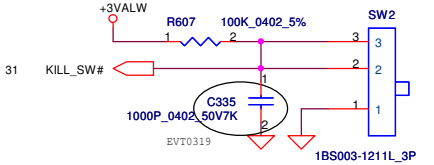
Compal Electronics, Inc.			
Title: KB /SW /LPC Debug Conn.			
Size: B	Document Number: KIUE0_LA-5191P		Rev: 1.0
Date: Wednesday, June 24, 2009	Sheet 32 of 43		

Lid Switch



Kill Switch

EE parts.
1st: DE100000100
2nd: DE100000I00

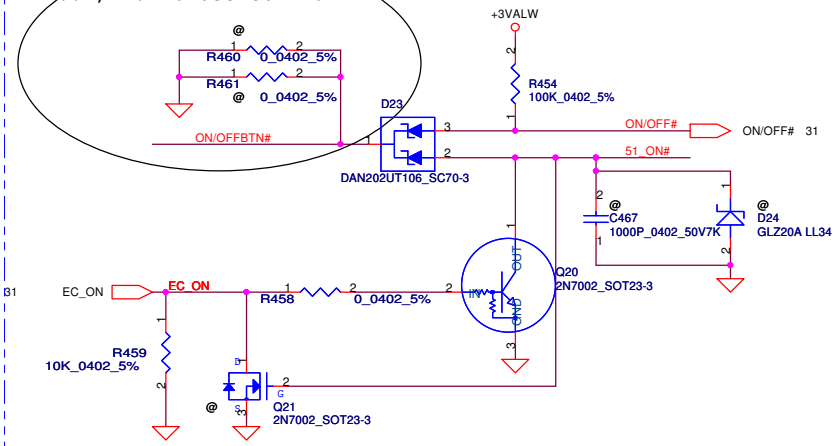


ON/OFF switch

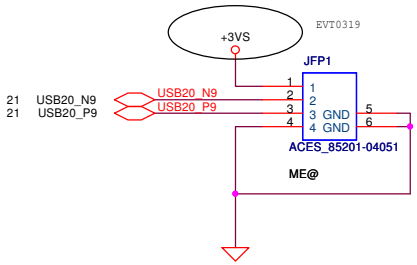
EVT0324 for debug only

DVT 0512

R460 ,R461 Close to D23

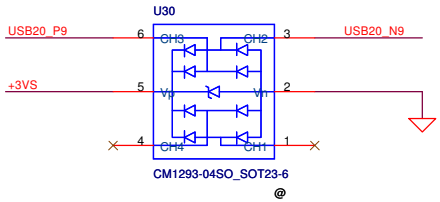


FP Board Conn 4 pin



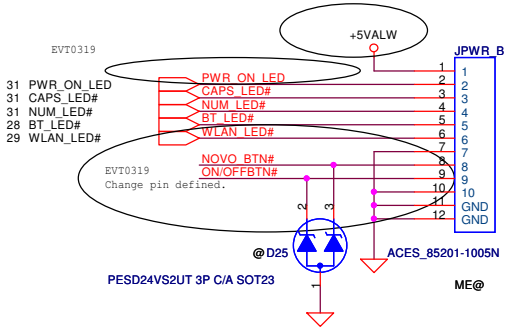
3/26_EVT

ESD PROTECT

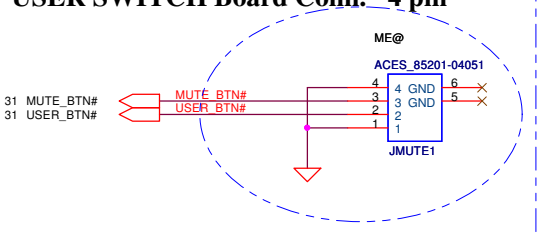


3/26 Please CLose JFP1

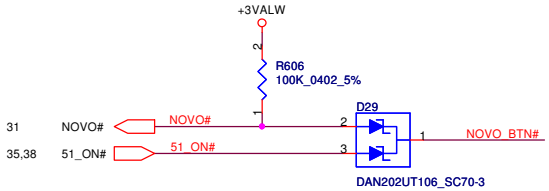
Power Board Conn. 10 pin



USER SWITCH Board Conn. 4 pin



Reverse for CABLE Pin define



Security Classification	Compal Secret Data		
Issued Date	2008/03/25	Deciphered Date	2008/04/

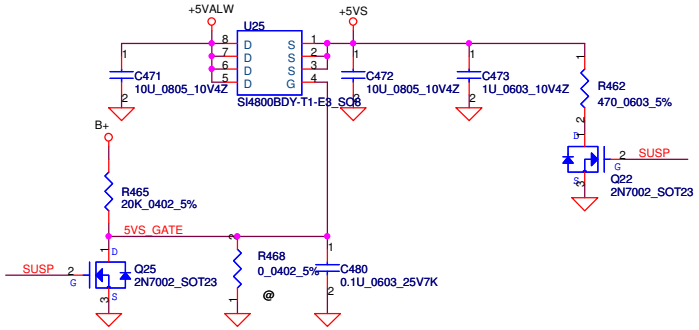
Compal Electronics,Ltd.

Title: **Audio Jack & SW connector**

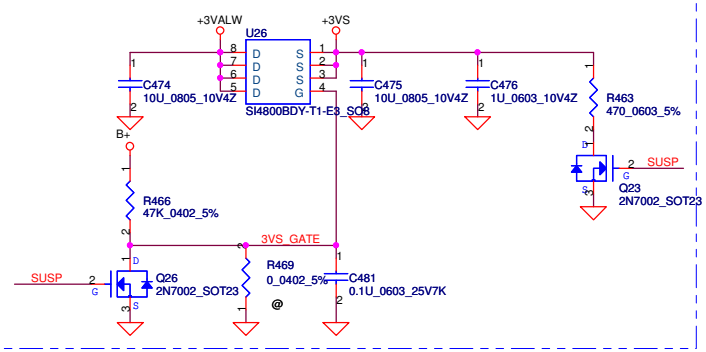
Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 | Sheet 33 of 43

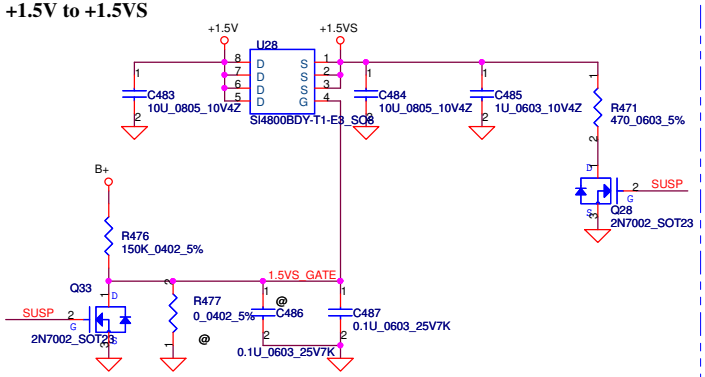
+5VALW TO +5VS

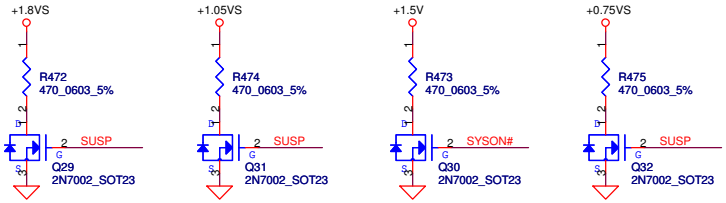


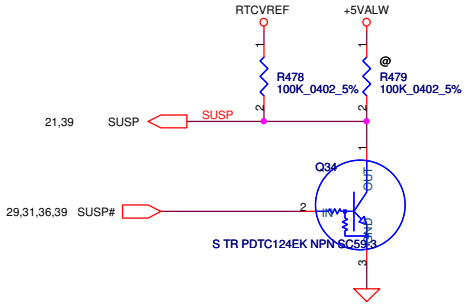
+3VALW TO +3VS

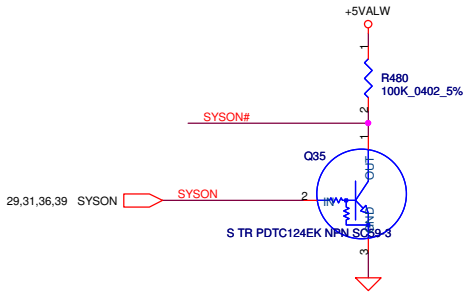


+1.5V to +1.5VS









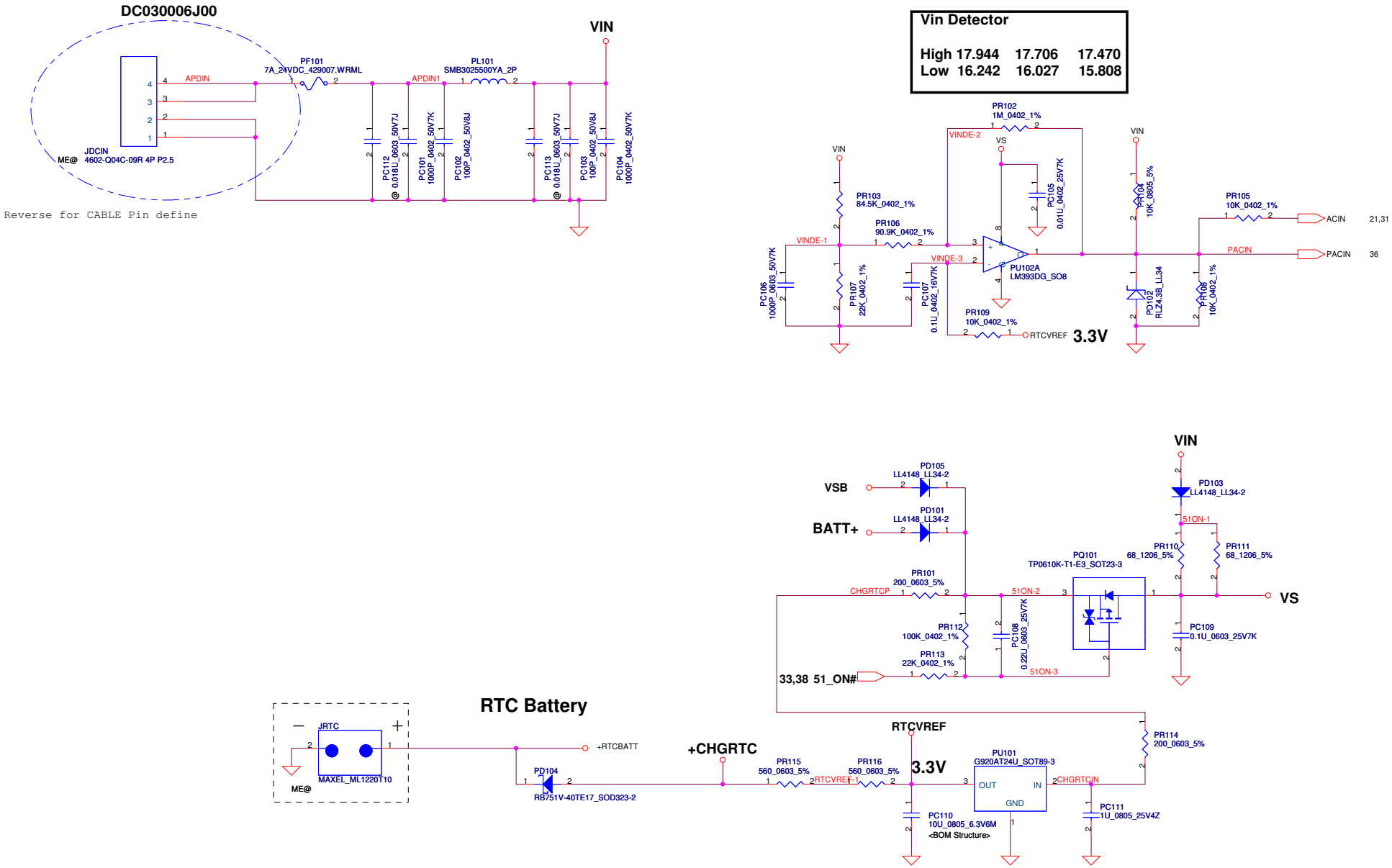
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	KIUE0_LA-5191P	1.0

Date: Wednesday, June 24, 2009 | Sheet 34 of 43



Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

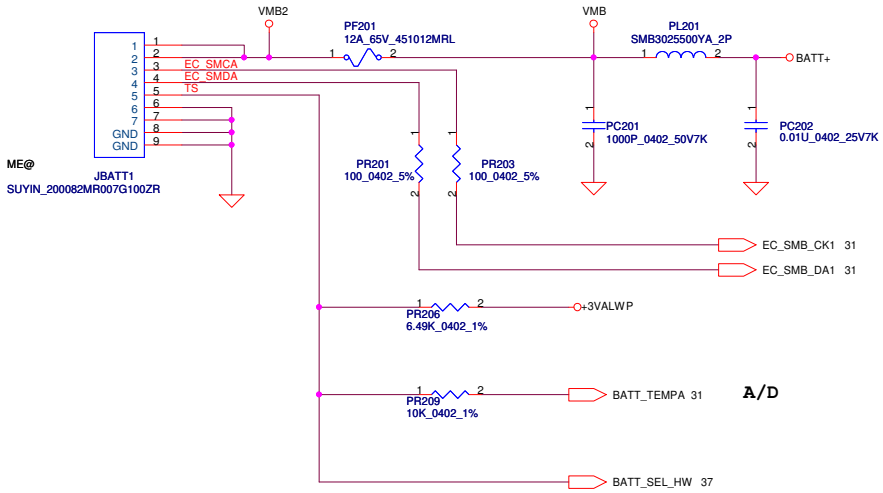
Compal Electronics, Inc.

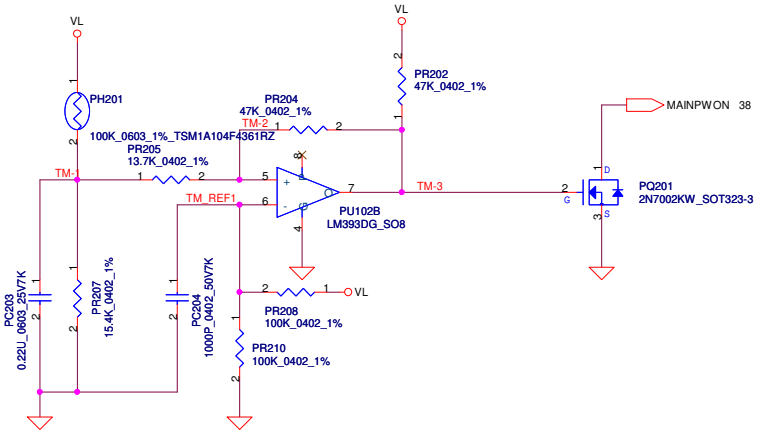
Title: DCIN & DETECTOR

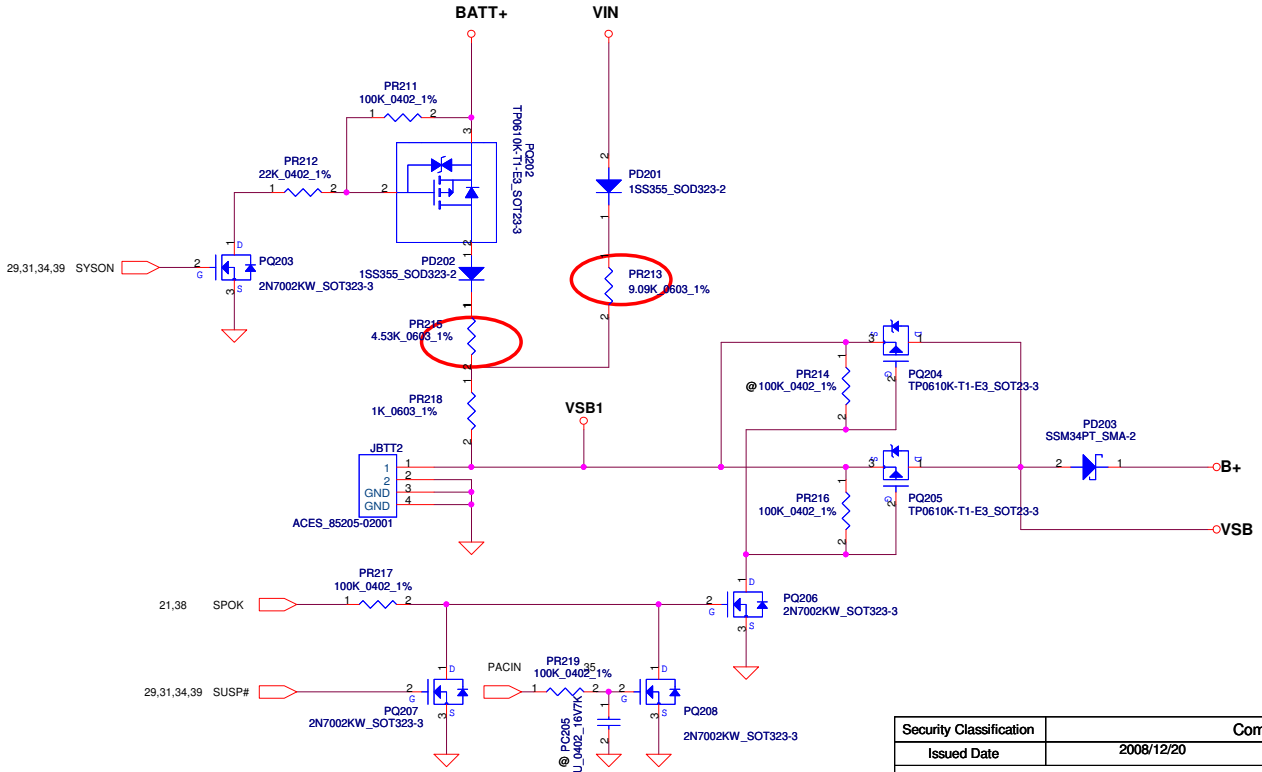
Size	Document Number	Rev
Custom		0.1

Date: Wednesday, June 24, 2009 | Sheet 35 of 42

PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C







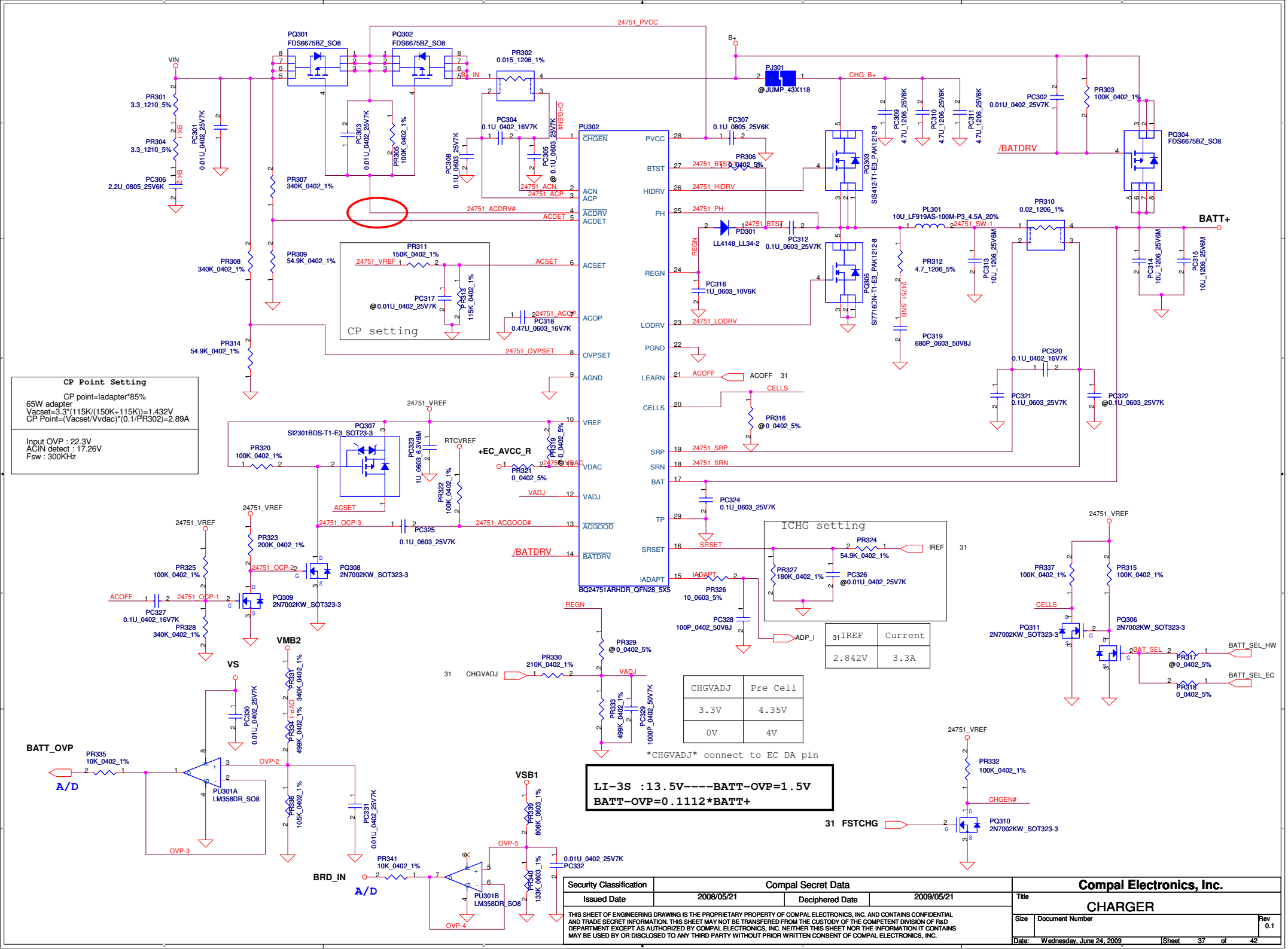
Security Classification	Compal Secret Data		
Issued Date	2008/12/20	Deciphered Date	2009/12/20

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
		0.1

Date: Wednesday, June 24, 2009 | Sheet 36 of 42


CP Point Setting
CP point=Iadapter*85%
65W adapter
Vacset=3.3*(115K/(150K+115K))=1.432V
CP Point=(Vacset/Vvdac)*(0.1/PR302)=2.89A
Input OVP : 22.3V
ACIN detect : 17.26V
Fsw : 300KHz
CP setting
ICHG setting
IREF | Current
2.842V | 3.3A
CHGVADJ | Pre Cell
3.3V | 4.35V
0V | 4V
"CHGVADJ" connect to EC DA pin
LI-3S :13.5V----BATT-OVP=1.5V
BATT-OVP=0.1112*BATT+
Security Classification | Compal Secret Data
Issued Date | 2008/05/21 | Deciphered Date | 2009/05/21
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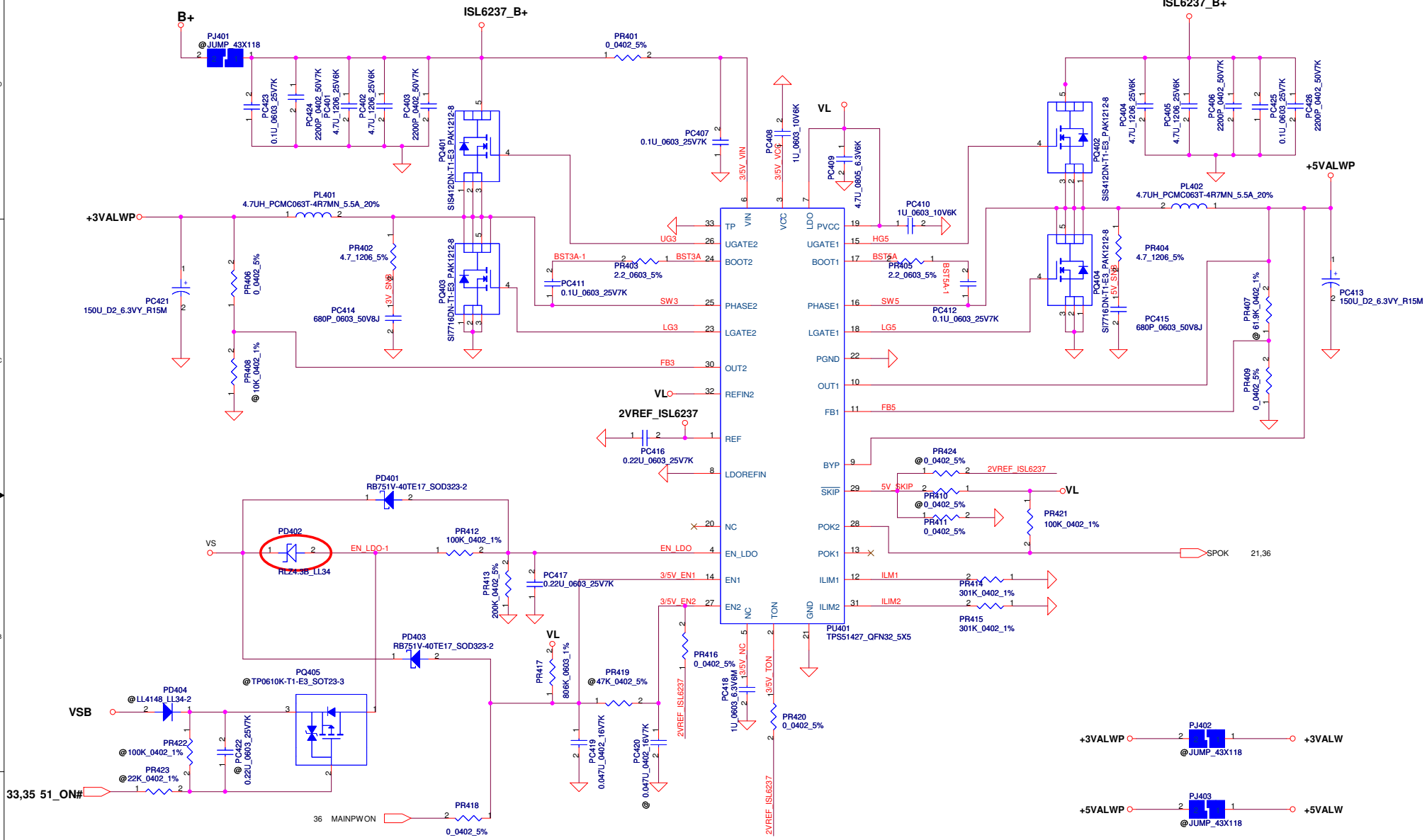
Compal Electronics, Inc.
Title
CHARGER
Size | Document Number | Rev 0.1
Date: Wednesday, June 24, 2009 | Sheet 37 of 42



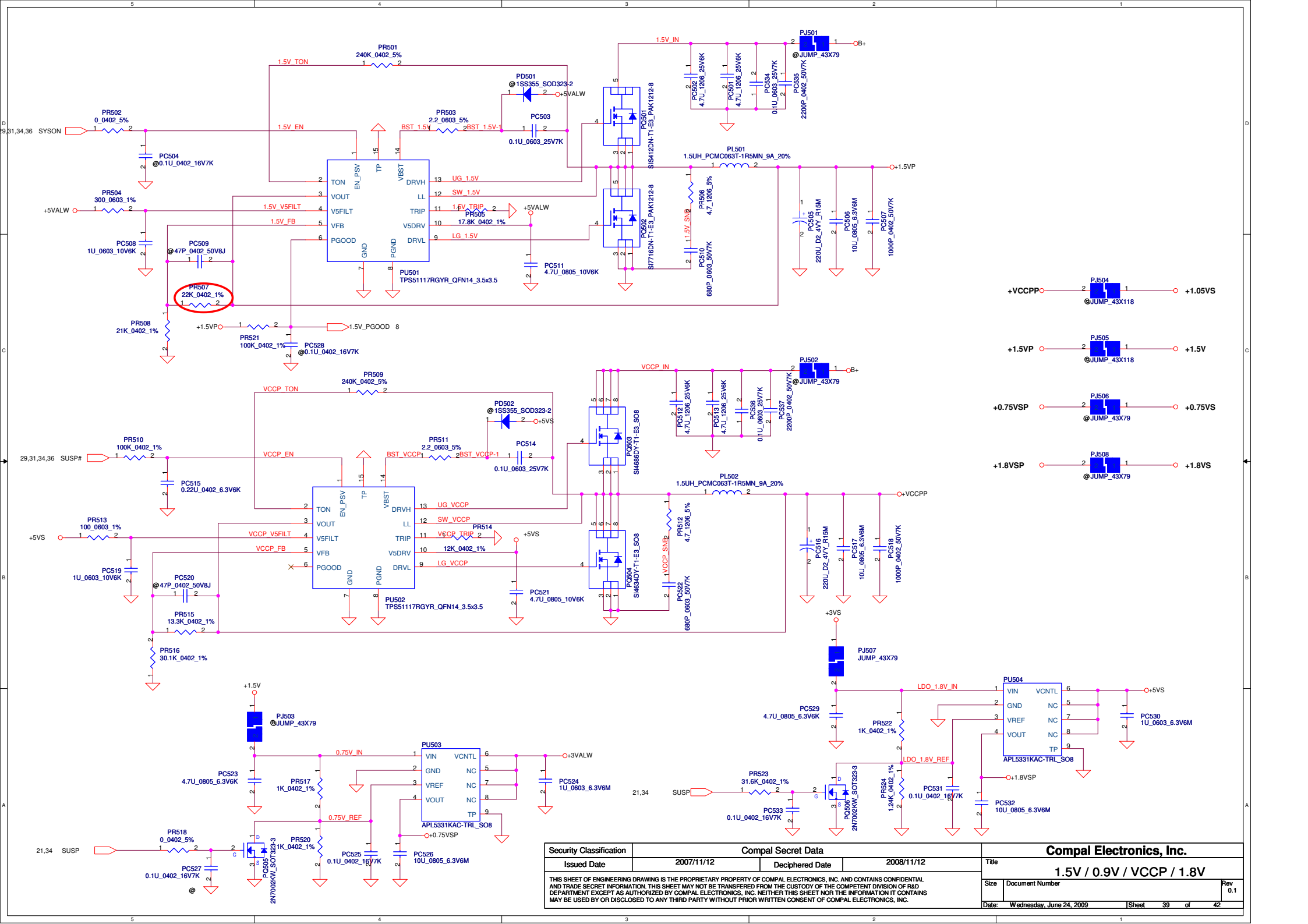
Security Classification	Compal Secret Data		
Issued Date	2007/06/22	Deciphered Date	2008/06/22

Compal Electronics, Inc.

Title: 3VALW/5VALW

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, June 24, 2009 | Sheet 38 of 42



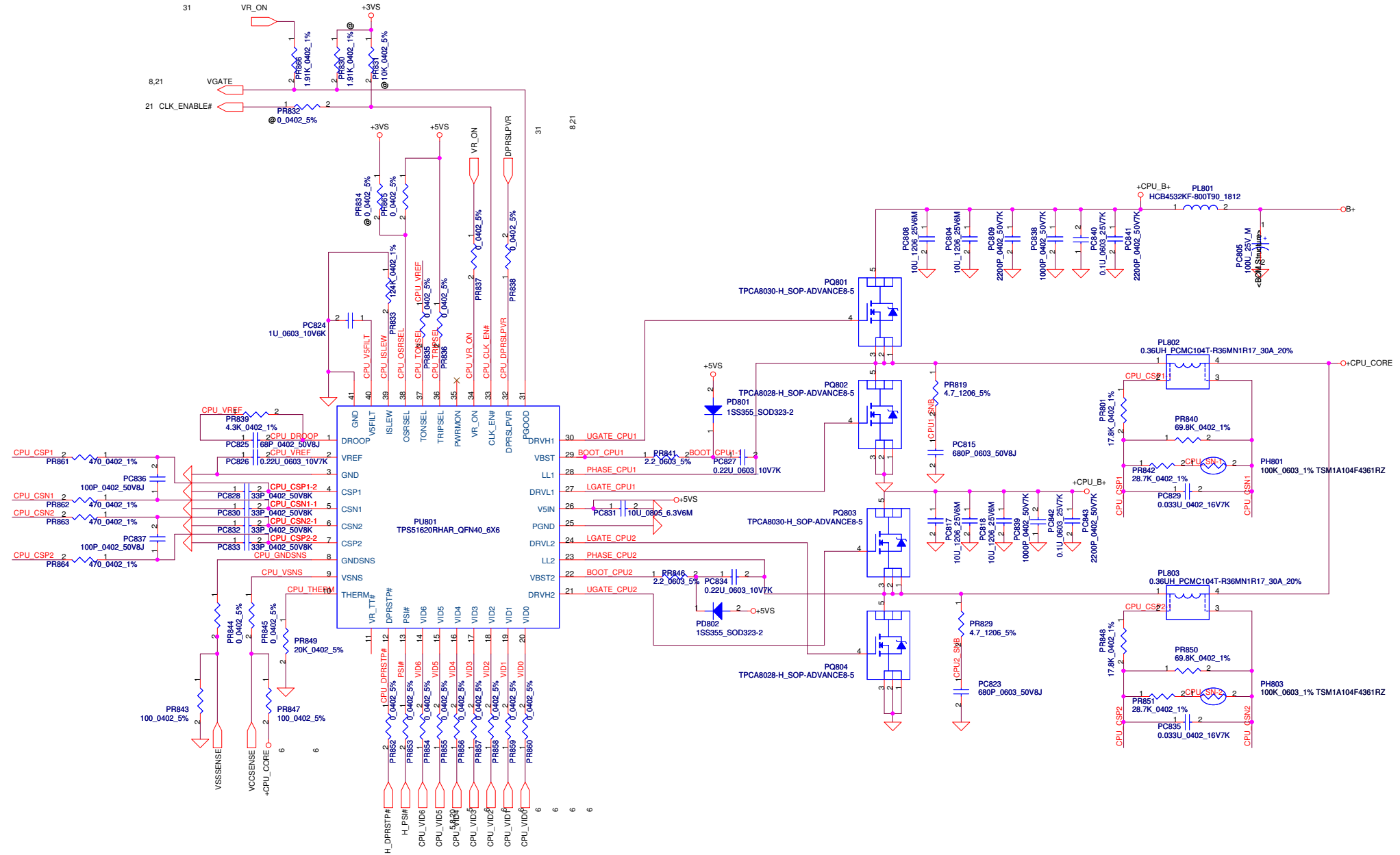
Security Classification	Compal Secret Data		
Issued Date	2007/11/12	Deciphered Date	2008/11/12

Compal Electronics, Inc.

Title: 1.5V / 0.9V / VCCP / 1.8V

Size	Document Number	Rev
		0.1

Date: Wednesday, June 24, 2009 | Sheet 39 of 42



Security Classification	Compal Secret Data		
Issued Date	2008/05/21	Deciphered Date	2009/05/21

Compal Electronics, Inc.

Title: **+CPU_CORE**

Size	Document Number	Rev
Custom		0.1

Date: Wednesday, June 24, 2009 | Sheet 40 of 42

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Change design	add bridge battery charge circuit		P.37	add PR215 and PR218 and change PR213 from 2K to 2.2K	2009.3.20	DVT
2	Change design	Change design		P.36	JDCIN turn off 180 degree	2009.3.20	DVT
3	Change design	Change design		P.37	change JBTT2 from lie to stand	2009.3.24	DVT
4	Change design	Change design		P.37	add PR219 and PC205	2009.3.25	DVT
5	Change design	Change design		P.39	change PR403 and PR405 from 0 to 2.2 ohm	2009.3.25	DVT
6	Change design	Change design		P.40	change PR503 and PR511 from 0 to 2.2 ohm	2009.3.25	DVT
7	Change design	Change design		P.41	change PR841 and PR846 from 0 to 2.2 ohm	2009.3.25	DVT
8	Change design	Change design		P.40	change PR514 from 15.4K to 12K ohm	2009.3.25	DVT
9	Change design	Change design		P.38	add PR339 PR340 PR341 and PC332	2009.5.5	PVT
10	Change design	Change design		P.41	change PR839 from 5.76K to 4.3K ohm	2009.5.15	PVT
11	Change design	Change design		P.40	change PR504 and PR513 from 422 to 300 ohm	2009.5.15	PVT
12	Change design	Change design		P.38	delect PR338	2009.6.18	Pre_MP
13	Change design	Modify bridge battery charge current					
14							
15							
16							
17							
18							
19							
20							
21							

Compal Electronics, Inc.
Title: PIR (PWR)
Size: Custom | Document Number: KIWAX_LA-5081P | Rev: 0.1
Date: Wednesday, June 24, 2009 | Sheet 41 of 42

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: HW PIR

Size	Document Number	Rev
Custom		1.0

Date: Wednesday, June 24, 2009 Sheet 42 of 43

Version change list (P.I.R. List)

for EE

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Detect Bridge Bettery life	Can't detect Bridge bettery	0.3	31	ADD R455	5/5	DVT
2	Esay rework for PORT 80	Not easy debug with system builded	0.3	29	CHANGE R378,R379 SIZE From 0402 to 0603 (NC)	5/13	DVT
3	BT Pwer MOS Floating	BT Pwr MOS Floating	0.3	28	NC R387, ADD R403	5/13	DVT
4	WWAN Noise Solution	Reserve C470	0.3		ADD C470 (NC)	5/13	DVT
5	Material LT	LIS34ALTR LT more than 4 months	0.3	28	CHANGE UG1 From LIS34ALTR to LIS244ALTR	5/13	DVT
6	DFB Design	COST DOWN	0.3	17	DELETE R167,R168,R287,R361	5/13	DVT
7	WWLAN LED	Reverse WWAN LED SWITCH	0.3	29	ADD Q38 (NC)	5/13	DVT
8	ICH_POK Glitch	Glitch will cause abnormal Power sequence	0.3	21	ADD D35,Q39 (NC),R456 (NC)	5/13	DVT
9	EMI Solution	EMI issue	0.3	17	ADD D36	5/13	DVT
10	Soft Start circuit	OCP	0.3	24	ADD R304,C325 (NC),C122	5/13	DVT
11	Debug use only		0.3	33	DELETE J3,J4,SW1,ADD R460 (NC),R461(NC)	5/13	DVT
12	BOM Option	Reserve R121	0.3	16	CHANGE R122 From 12 Ohm to 33 Ohm	5/16	DVT
13	BOM Option	ALC272-GR EOL	0.3	20	CHANGE SA00002CI00 to SA00002CI10	5/25	DVT
14	BOM Option	DELETE ROHM MATERIAL FROM 1st BOM	0.3		CHANGE SBX01240010 to SB00000AG00	5/25	DVT
15	BOM Modify		1.0	23	CHANGE R90 SIZE From 0603 to 0805, DELETE R335,R342,R416	6/23	PVT
16	Stepping to V1.0	Update LA5191PR10 to Stepping to V1.0	1.0	01	Update DAZ P/N to V1.0 and ADD Sub-Bard P/N LS5191/LS5192/LS5193/LS5194	6/23	PVT
17	Soft START Circuit	OCP for LAN	1.0	24	Change R304 from 0 Ohm to 10K Ohm , Delete C122	6/23	PVT
18	Mic Pull high change		1.0	26	Change R333 From 4.7K Ohm to 2.2K Ohm	6/23	PVT
19	AUDIO LINE OUT CAP	Remove Duplicated Cap	1.0	27	DELETE C404,C405	6/23	PVT
20	EMI SOLUTION	SPI CLK	1.0	30	Change R410 From 15 Ohm to KC FBMA-10-100505-101T 0402	6/23	PVT
21	Soft START Circuit	OCP for Bluetooth	1.0	28	ADD C404 (NC)	6/23	PVT
21							

Compal Electronics, Inc.

Title: HW PIR

Size: Custom | Document Number: KIUE0_LA-5191P | Rev: 1.0

Date: Thursday, June 25, 2009 | Sheet 43 of 43