MODEL NAME : VBW00
PROJECT CODE : ANRVBW0100
PCB NO : DA8000WK000 LA-9981P M/B
DA40001FO00 LS-9101P POWER BUTTON/B
DA40001FP00 LS-9102P USB/B
DA40001FQ00 LS-9103P TP BUTTON/B

Dell / Compal Confidential

Schematic Document

Intel Shark Bay ULT
OAK Value2
UMA/DIS AMD Sun XT

2013-03-09 Rev: 0.2

X76@ : 76 level
46@ : 46 level
@ : Nopop component
CONN@ : Connector component
XDP@ : XDP function
UMA@ : Only for UMA
DIS@ : Only for Discrete
SUN@ : SUN XT
EMI@ : EMI parts
@EMI@ : Reserve EMI parts
ESD@ : ESD parts
RF@ : RF parts

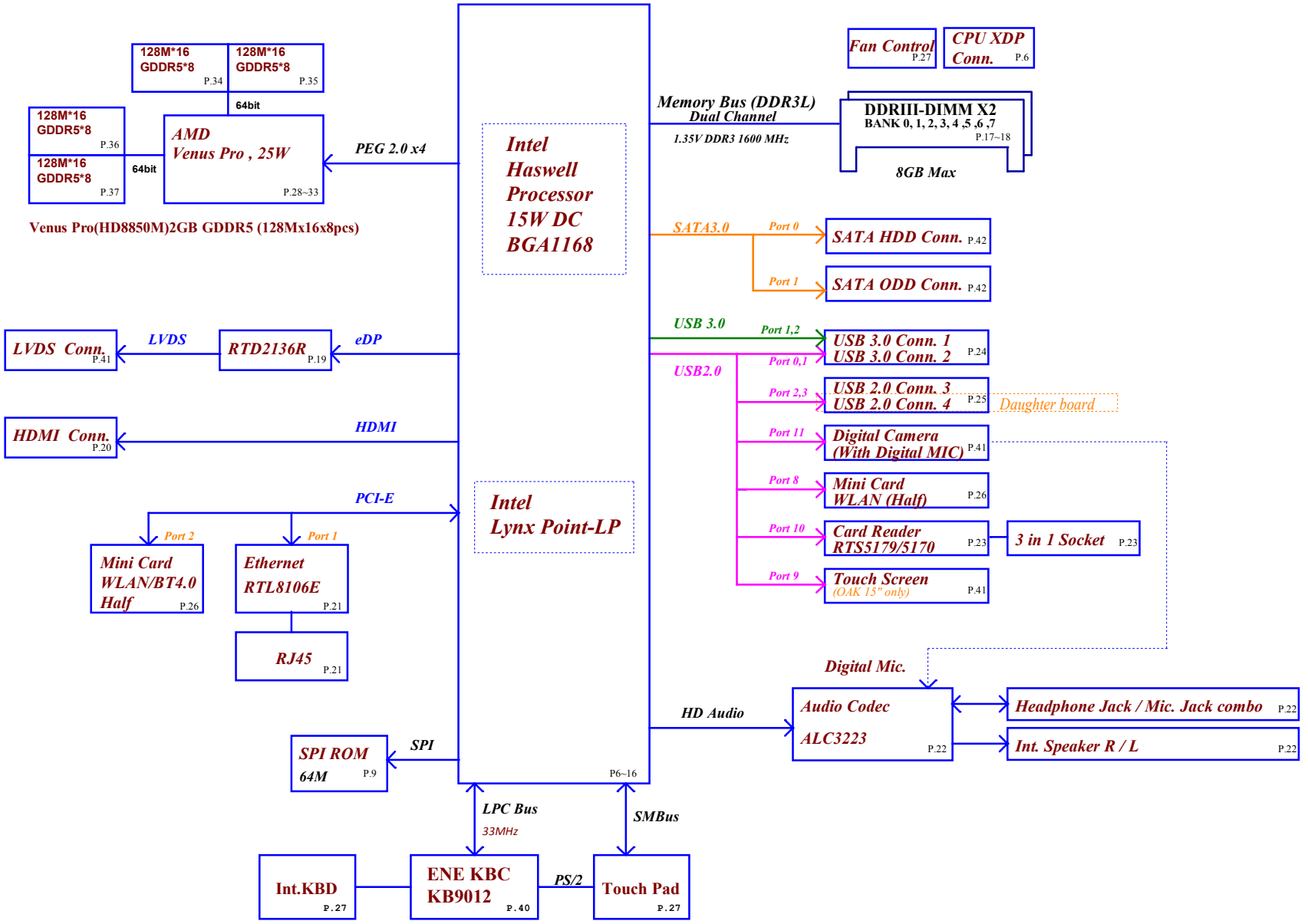
BOM config
UMA : UMA@,EMI@,ESD@,RF@,XDP@
DIS SUN : SUN@,DIS@,EMI@,ESD@,RF@,XDP@

ZZZ R1@
PCB VBW01 LA9981P/LS9101P/LS9102P/LS9103P
DA8000WK000

Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.

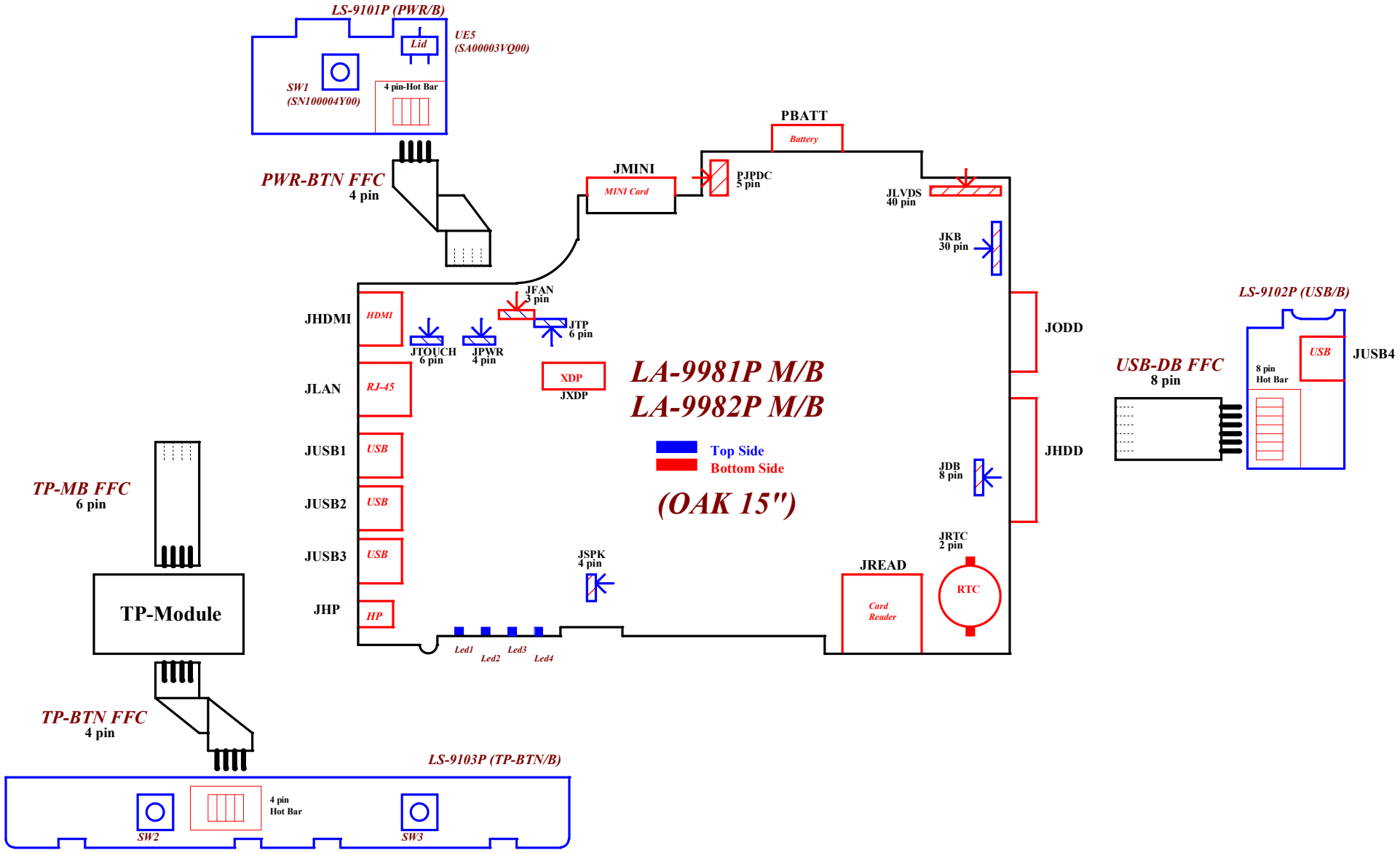
Title: Cover Page
Size: Custom | Document Number: LA-9981P | Rev: 0.2
Date: Saturday, March 09, 2013 | Sheet 1 of 55



Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.			
Title: Block diagram			
Size	Document Number: LA-9981P		Rev: 0.2
Date: Saturday, March 09, 2013	Sheet 2 of 55		

Compal Confidential
Project Code : VAW00 / VAW01
File Name : LA-9981P / LA-9982P



Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: DB block diagram

Size | Document Number: LA-9981P | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 3 of 55

Board ID Table for AD channel

Vcc	3.3V +/- 1%
Ra	100K +/- 1%

Board ID	Rb	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

SMBUS Control Table

	SOURCE	BATT	Charger	RTD2136S	VGA	DDR3L	XDP	WLAN mini card	Touch pad
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V						
EC_SMB_CK2 EC_SMB_DA2	KB9012			V	V				
SMBCLK SMBDATA	ULT					V	V	V	V
SML0CLK SML0DATA	ULT								
SML1CLK SML1DATA	ULT								

Link

BOARD ID Table

ID	PCB Revision			
	UMA	Sun XT	Venus Pro	Venus XT
0	0.1			
1		0.1		
2			0.1	
3				0.1
4	0.2			
5		0.2		
6			0.2	
7				0.2
8	0.3			
9		0.3		
10			0.3	
11				0.3
12	1.0			
13		1.0		
14			1.0	
15				1.0

Symbol Note :

: means Digital Ground

: means Analog Ground

CLOCK SIGNAL	
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU (N14P)
CLKOUT_PCIE5	

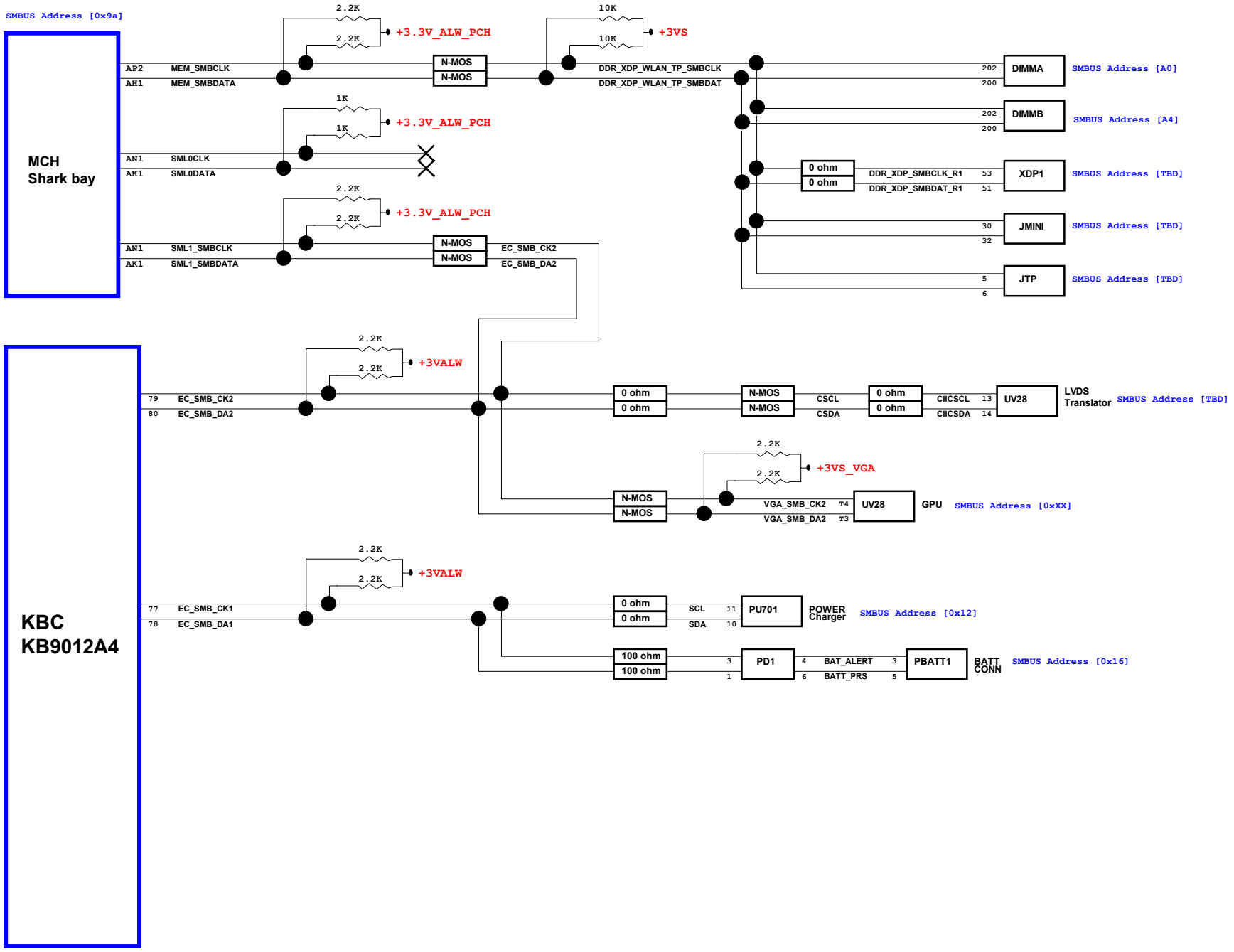
ULT	USB3.0	
	Port1	USB connector 2
	Port2	USB connector 1
	Port3	
	Port4	
	USB2.0	
	Port0	USB connector 2
	Port1	USB connector 1
	Port2	USB connector 3
	Port3	USB connector 4 (DB)
	Port4	MINI Card (WLAN)
	Port5	Touch Screen Panel
	Port6	Card Reader
	Port7	Camera
	PCI EXPRESS	
	Lane 1	
	Lane 2	
	Lane 3	10/100 LAN
	Lane 4	MINI Card (WLAN)
	Lane 5	PEG (N14P)
	Lane 6	PEG (N14P)
	SATA	
	SATA0	HDD
	SATA1	ODD
	SATA2	
	SATA3	

Compal Electronics, Inc.

Title: Notes List

Size | Document Number: LA-9981P | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 4 of 55



Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.			
Title: SMBus block diagram			
Size	Document Number: LA-9981P		Rev: 0.2
Date: Saturday, March 09, 2013	Sheet 5 of 55		

UC1 4200U/i5G2R1@

i5-4200U-15W-GT2-QS

CL80647014777O2-QEVE-C0-1.6G_BGA1168~D

SA00006SM0L

UC1 4010U/i3G2R1@

i3-4010U-15W-GT2-QS

CL80647014782O2-QEVG-C0-1.7G_BGA1168~D

SA00006SX0L

UC1 4500U/i7G2R1@

i7-4500U-15W-GT2-QS

CL80647014772O2-QEVD-C0-1.8G_BGA1168~D

SA00006SL0L

UC1A HASWELL_MCP_E

DDI1_LANE_N0 DDI1_LANE_P0 DDI1_LANE_N1 DDI1_LANE_P1 DDI1_LANE_N2 DDI1_LANE_P2 DDI1_LANE_N3 DDI1_LANE_P3

DDI1_TXN0 DDI1_TXP0 DDI1_TXN1 DDI1_TXP1 DDI1_TXN2 DDI1_TXP2 DDI1_TXN3 DDI1_TXP3

DDI2_TXN0 DDI2_TXP0 DDI2_TXN1 DDI2_TXP1 DDI2_TXN2 DDI2_TXP2 DDI2_TXN3 DDI2_TXP3

EDP_TXN0 EDP_TXP0 EDP_TXN1 EDP_TXP1 EDP_TXN2 EDP_TXP2 EDP_TXN3 EDP_TXP3

EDP_CPU_LANE_N0 EDP_CPU_LANE_P0 EDP_CPU_LANE_N1 EDP_CPU_LANE_P1

EDP_AUXN EDP_AUXP EDP_CPU_AUX# EDP_CPU_AUX

EDP_RCOMP EDP_DISP_UTIL EDP_COMP EDP_BIA_PWM

1 OF 19 Rev1p2

COMPENSATION PU FOR eDP

+VCCIOA_OUT

24.9_0402_1%~D RC71

RC72 0_0402_5%

CAD Note:Trace width=20 mils ,Spacing=25mil, Max length=100 mils.

CC13 0.1U_0402_10V7K +3VS

UC4 74CBTLV3126BQ_DHVQFN14_2P5X3

PCH_JTAG_TDO TDO_XDP RC43 0_0402_5%

PCH_JTAG_TDI TDI_XDP RC44 0_0402_5% TDI_XDP_R RC45 0_0402_5%

PCH_JTAG_TMS TMS_XDP RC46 0_0402_5%

RUNPWROK TRST#_XDP

XDP_TDO XDP_TDI XDP_TMS XDP_TRST#

CC14 0.1U_0402_10V7K CC15 0.1U_0402_10V7K +1.05VS

Place near JXDP1

JXDP1 SAMTE_BSH-030-01-L-D-A CONN@

H_CPUPWRGD RC48 RC49 CFG0 CFG1 CFG2 CFG3 CFG4 CFG5 CFG6 CFG7

XDP_PREQ# XDP_PRDY# XDP_OBS0_R XDP_OBS1_R H_VCCST_PWRGD_XDP CFD_PWRBTN#_XDP CPU_PWR_DEBUG#_R SYS_PWROK_XDP

PBTN_OUT# SYS_PWROK CPU_PWR_DEBUG# SYS_PWROK

DDR_XDP_SMBDAT_R1 DDR_XDP_SMBCLK_R1 PCH_JTAG_TCK XDP_TCLK

RP46 0_8P4R_5%

CLK_XDP RC139 CLK_CPU_ITP

CLK_XDP# RC140 CLK_CPU_ITP#

XDP_RST#_R XDP_DBRESET# PLT_RST# RC51 1K_0402_5% RC362 1K_0402_1% CC17 0.1U_0402_10V7K +3VS

TDO_XDP TRST#_XDP TDI_XDP TMS_XDP CFG3_R RC56 1K_0402_5%

reference Shark Bay ULT Validation Customer Debug Port Implementation Requirement Rev 1.0

+1.05VS RC58 49.9_0402_1% H_CATERR# H_PROCHOT# RC60 62_0402_5%

PCH_JTAG_RST# XDP_TRST# RC57

PCH_JTAG_TCK XDP_TCLK RC59

PCH_JTAG_TDO TDO_XDP RC62

PCH_JTAG_TDI XDP_TDI_R RC63

PCH_JTAG_TCK XDP_TCLK RC65

+3VALW_PCH RC64 1K_0402_5% SYS_PWROK_XDP CC16 0.1U_0402_10V7K

Place near JXDP1.47

XDP_DBRESET# SYS_RESET# RC26 0_0402_5% SYS_RESET# <10>

H_CPUPWRGD RC66 10K_0402_5%

CAD Note: Avoid stub in the PWRGD path while placing resistors RC115

DDR3 COMPENSATION SIGNALS

200_0402_1% RC68 SM_RCOMP0

120_0402_1% RC69 SM_RCOMP1

100_0402_1% RC70 SM_RCOMP2

CAD Note: Trace width=12~15 mil, Spcing=20 mils Max trace length= 500 mil

UC1B HASWELL_MCP_E

CPU_DETECT# H_CATERR# PECI_EC H_PROCHOT# H_PROCHOT#_R RC67 56_0402_5% H_CPUPWRGD

PROC_DETECT CATERR PECI PROCHOT PROCPWRGD

SM_RCOMP0 SM_RCOMP1 SM_RCOMP2 SM_DRAMRST SM_PG_CNTL1

DDR3_DRAMRST#_CPU DDR_PG_CTRL

MISC JTAG THERMAL PWR DDR3

PRDY PREQ PROC_TCK PROC_TMS PROC_TRST PROC_TDI PROC_TDO

XDP_PRDY# XDP_PREQ# XDP_TCK XDP_TMS XDP_TRST# XDP_TDI XDP_TDO

PCH_JTAG_RST# R2341 0_0402_5%

XDP_OBS0_R XDP_OBS1_R RC141 0_0402_5%

BPM#0 BPM#1 BPM#2 BPM#3 BPM#4 BPM#5 BPM#6 BPM#7

T111 T112 T113 T114 T115 T116

2 OF 19 Rev1p2

PU/PD for JTAG signals

XDP_TMS XDP_TDI XDP_PREQ# TDO_XDP RP44 51_8P4R_5%

XDP_TDO XDP_TCK XDP_TRST# RP45 51_8P4R_5%

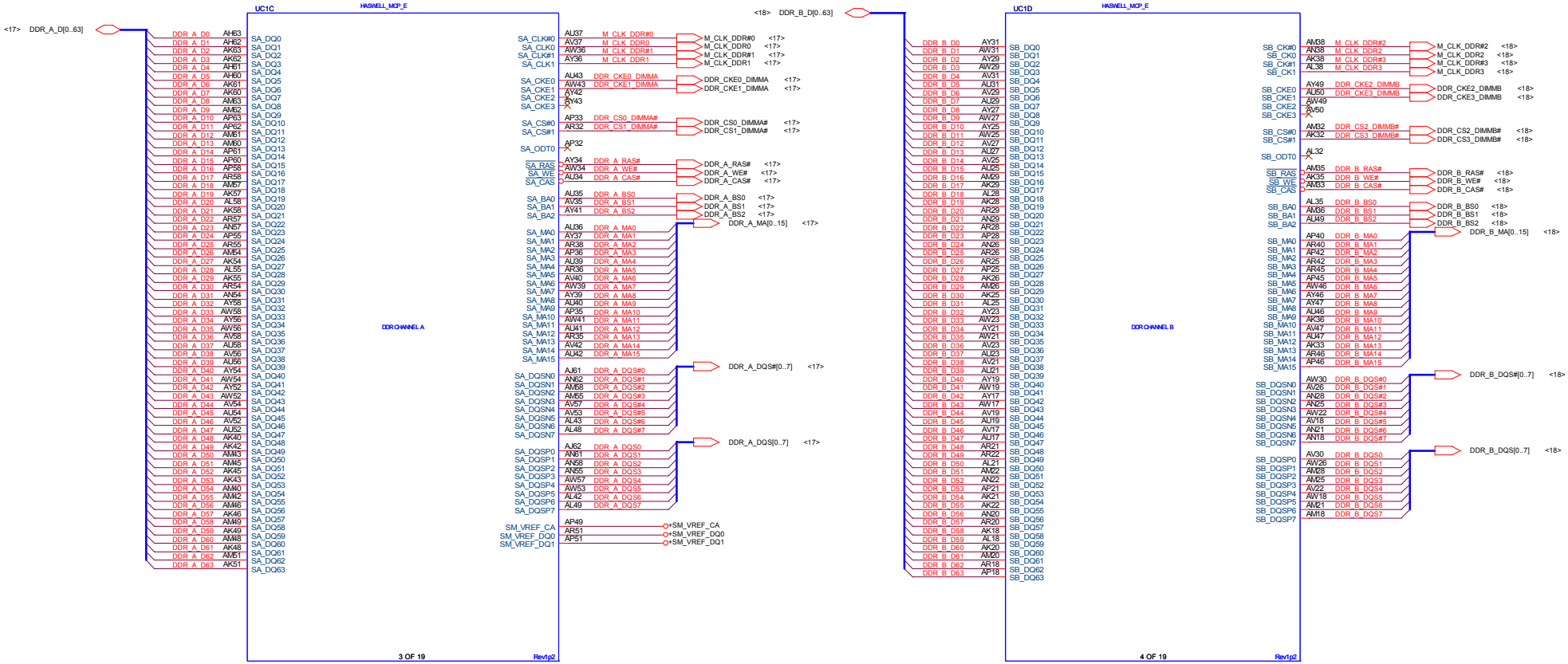
Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

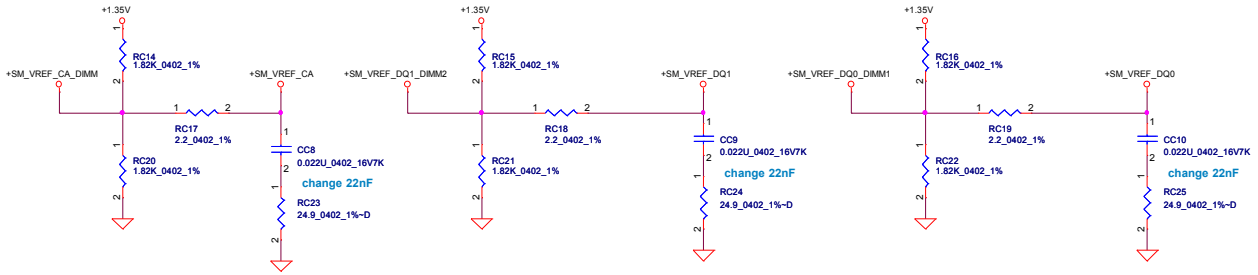
Compal Electronics, Inc.

Title: MCP(1,2/19) eDP,XDP,MISC

Size: Document Number: LA-9981P Rev: 0.2

Date: Saturday, March 09, 2013 Sheet 6 of 55





confirm by intel request PDG P141

Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

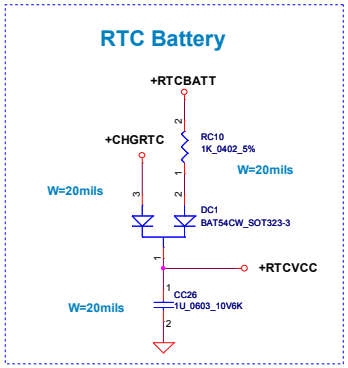
Compal Electronics, Inc.

Title: MCP(3,4/19) DDR3

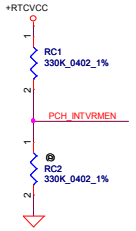
Size: | Document Number: LA-9981P | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 7 of 55

RTC Battery

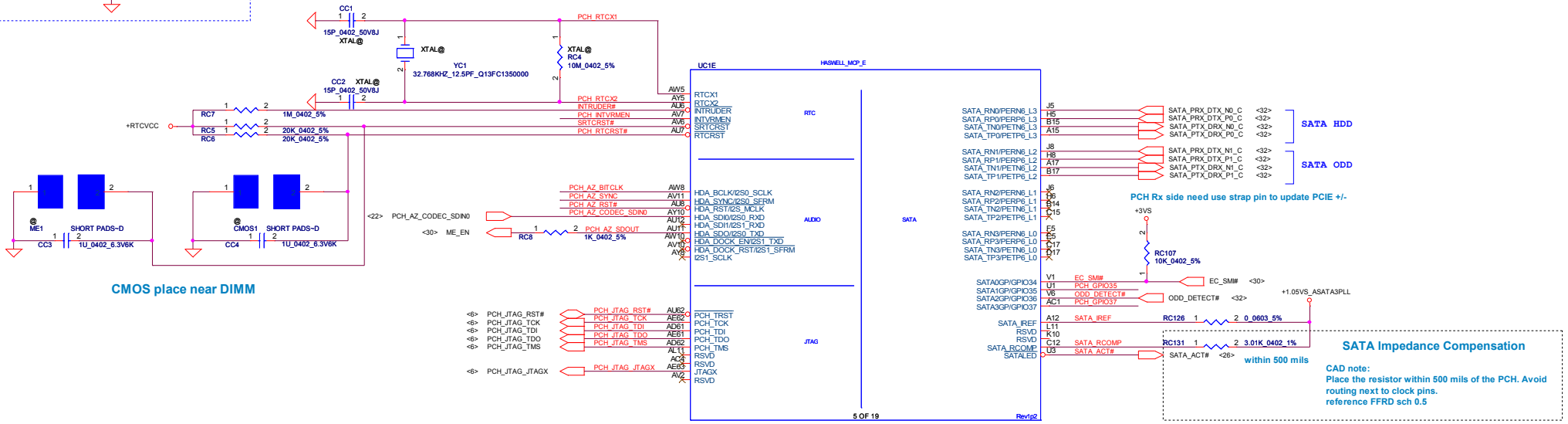


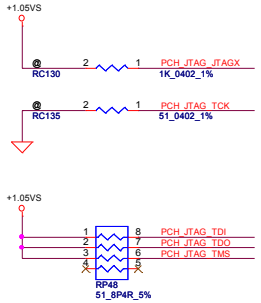
For GCLK



INTVRMEN - INTEGRATED SUS 1.05V VRM ENABLE
High - Enable Internal VRs
Low - Enable External VRs

FLASH DESCRIPTOR SECURITY OVERRIDE
LOW = DESABLED (DEFAULT)
HIGH = ENABLED

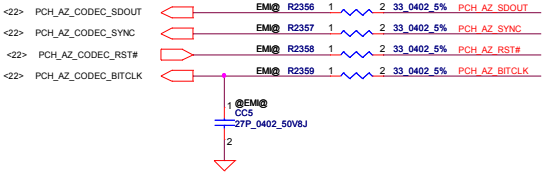




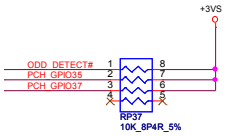
CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

HDA for Codec



EMI depop location



Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

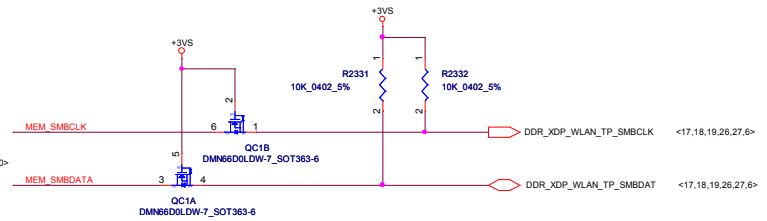
Compal Electronics, Inc.

Title: MCP(5/19) RTC,SATA,HDA,JTAG

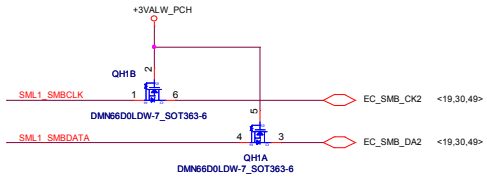
Size | Document Number: LA-9981P | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 8 of 55

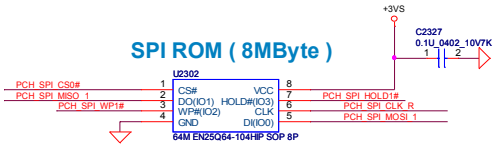
MEM Bus : DDR/XDP/WLAN/TP



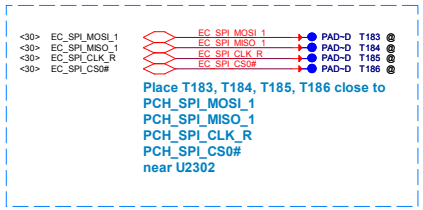
SML1 Bus : EC/Sensors

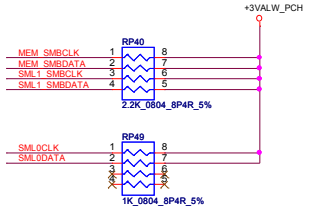


SPI ROM (8MByte)

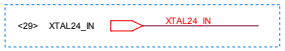


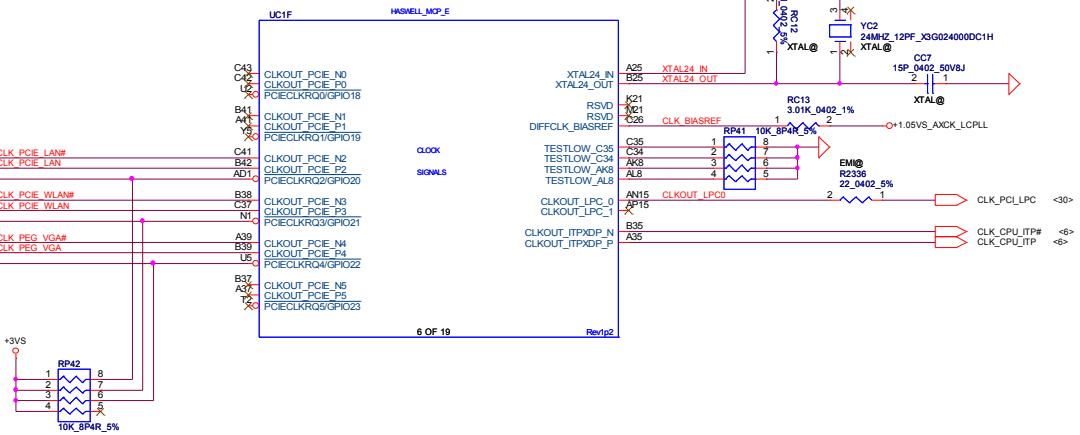
PN : SA000046400 ,64M,EN25Q64-104HIP





For GCLK

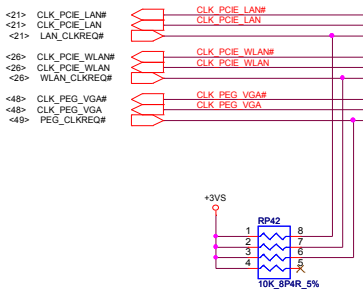




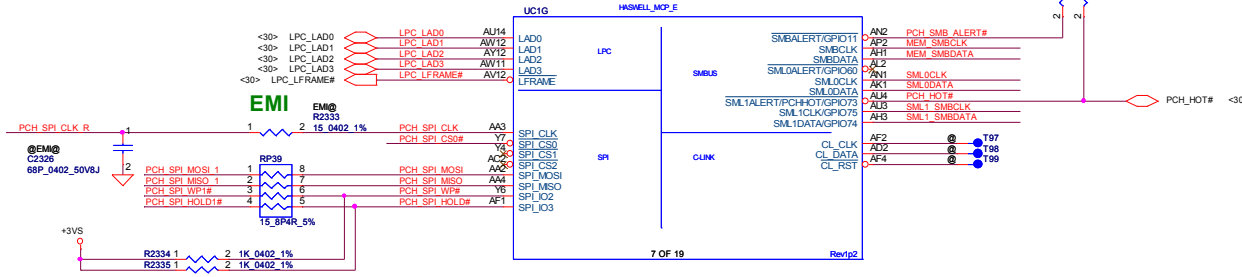
10/100 LAN ------->

WLAN(Mini Card)--->

dGPU--->



EMI



Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

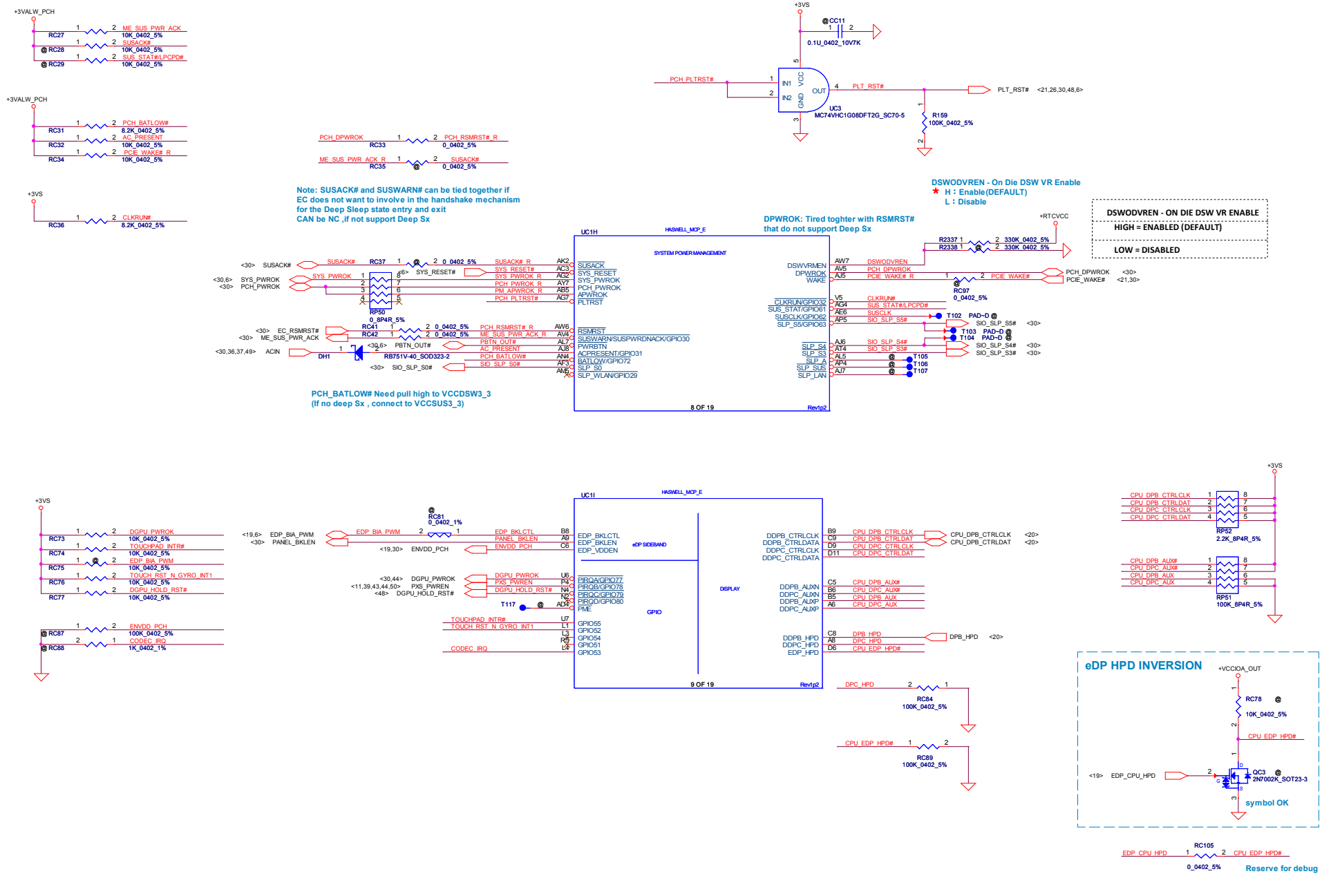
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc.

Title: MCP(6,7/19) CLK,SMB,SPI,LPC

Size | Document Number: LA-9981P | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 9 of 55



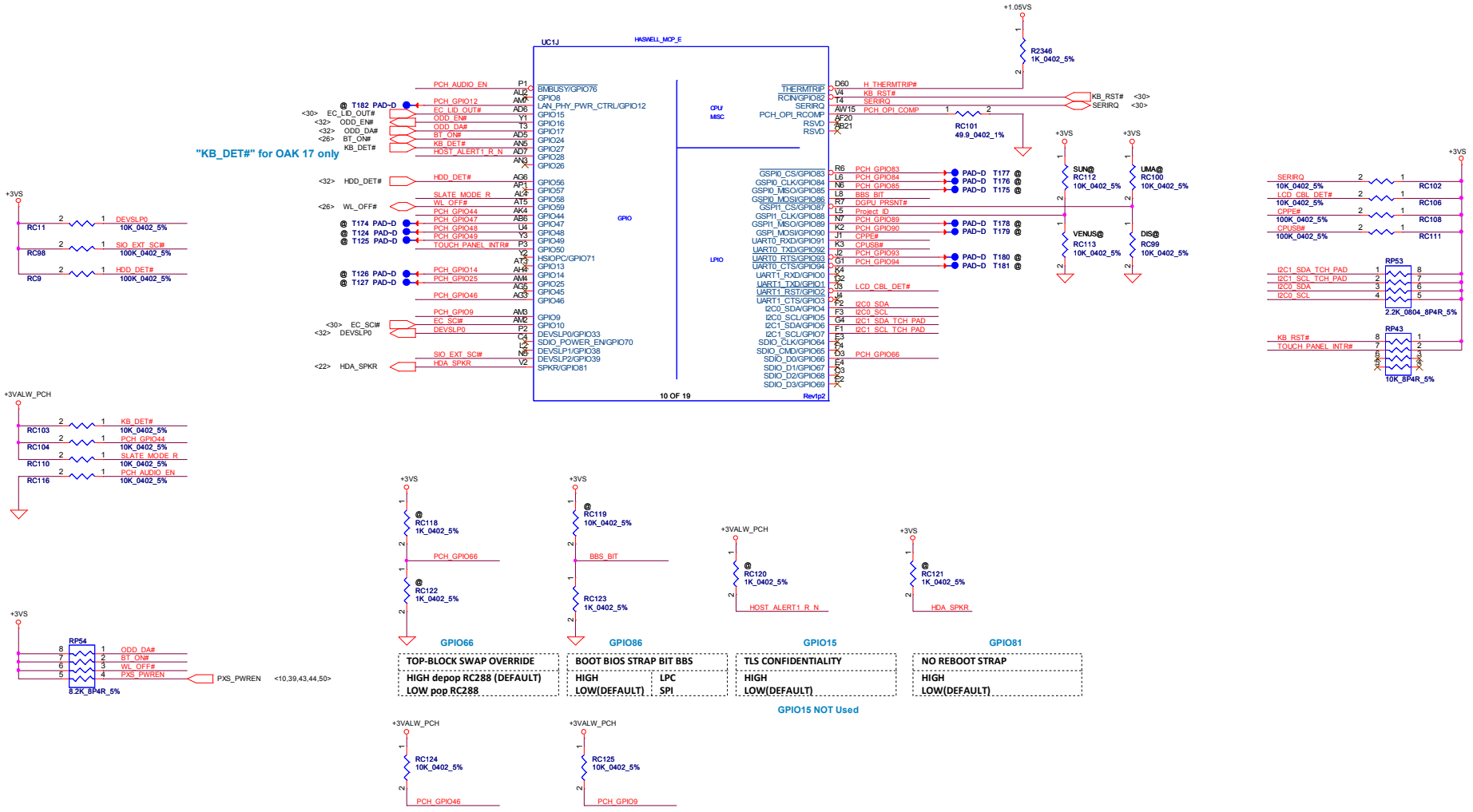
Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: MCP(8,9/19) DDI,EDP,GPIO

Size	Document Number	Rev
	LA-9981P	0.2

Date: Saturday, March 09, 2013 Sheet 10 of 55



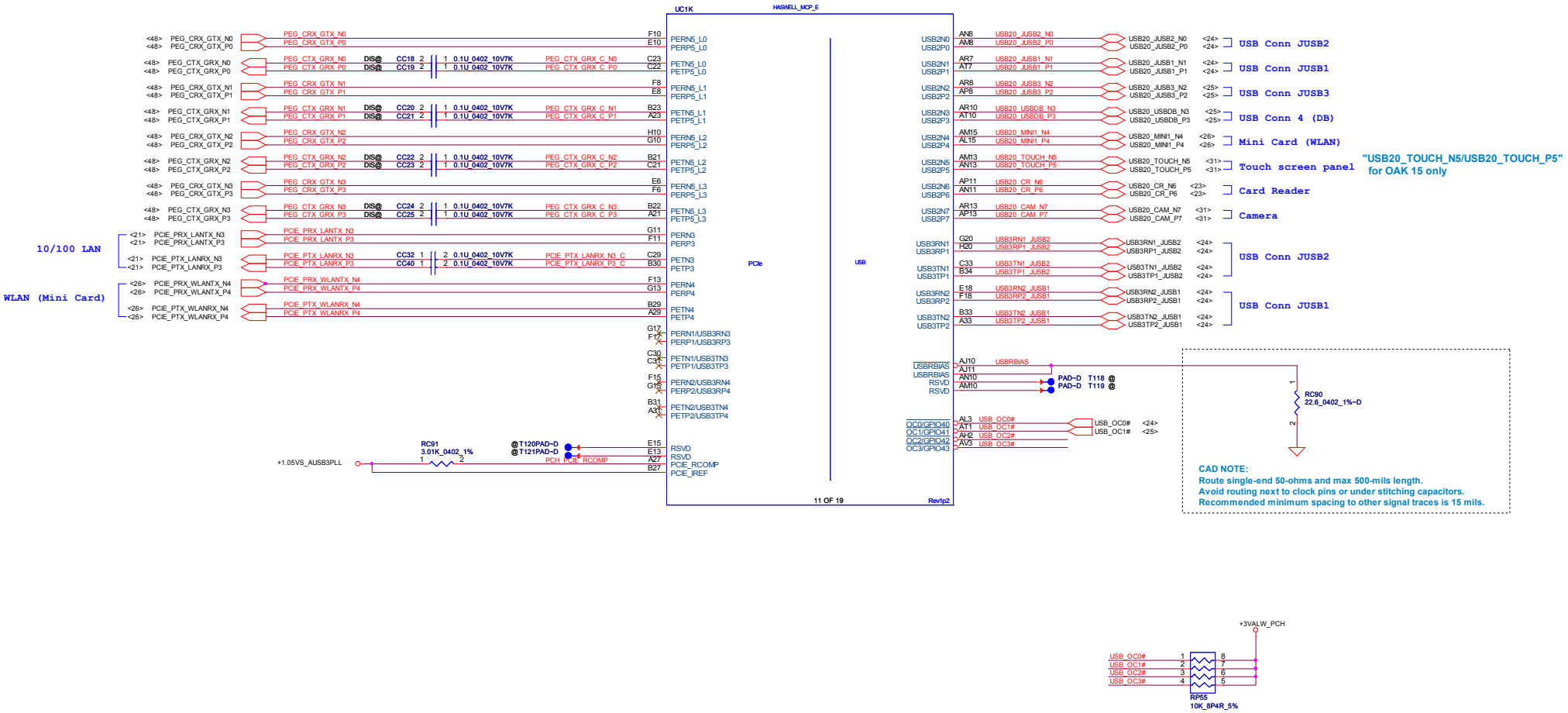
Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: **MCP(10/19) GPIO,LPIO,MISC**

Size	Document Number	Rev
	LA-9981P	0.2

Date: Saturday, March 09, 2013 | Sheet 11 of 55



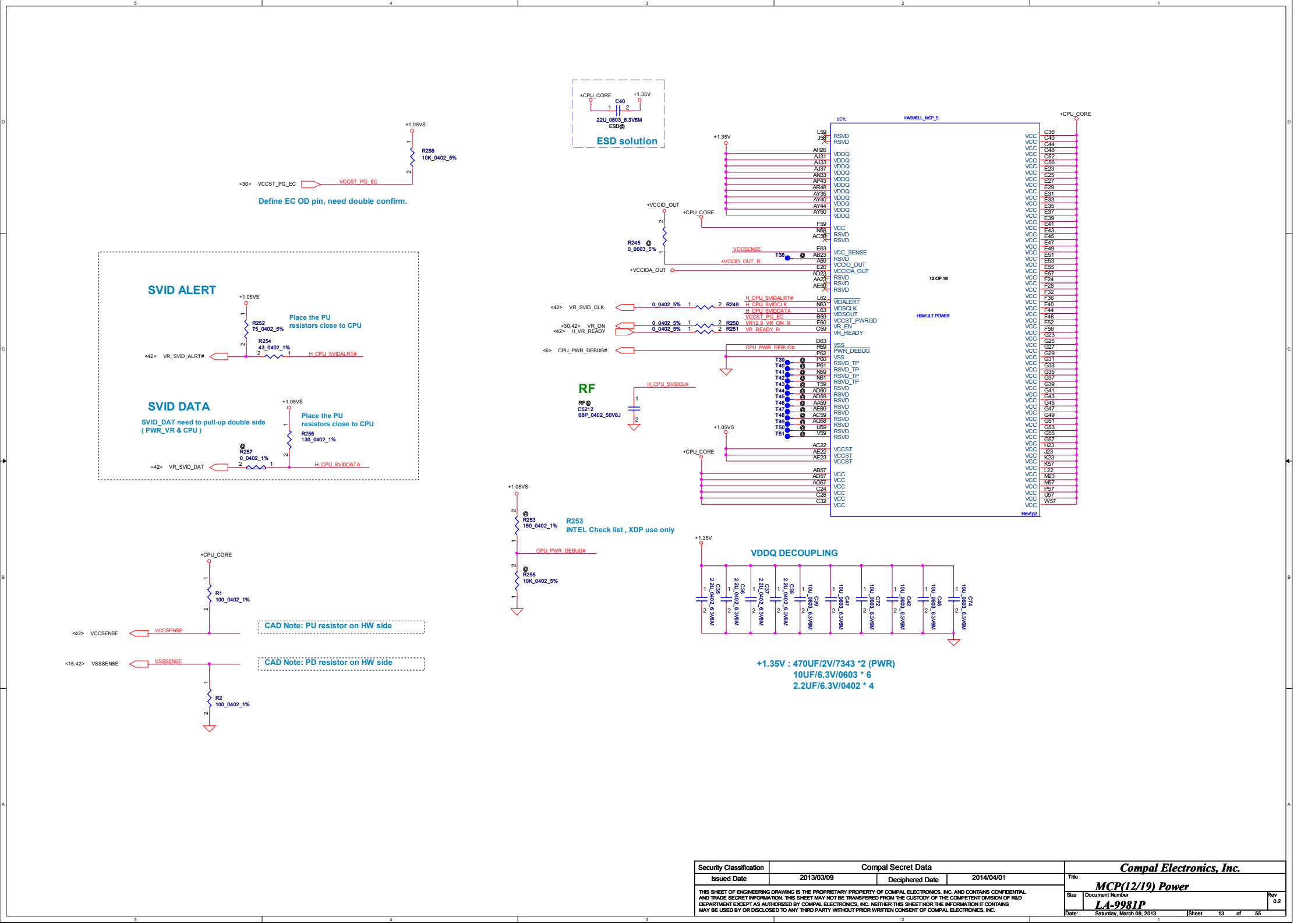
Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: MCP(11/19) PCIE,USB

Size: | Document Number: LA-9981P | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 12 of 55



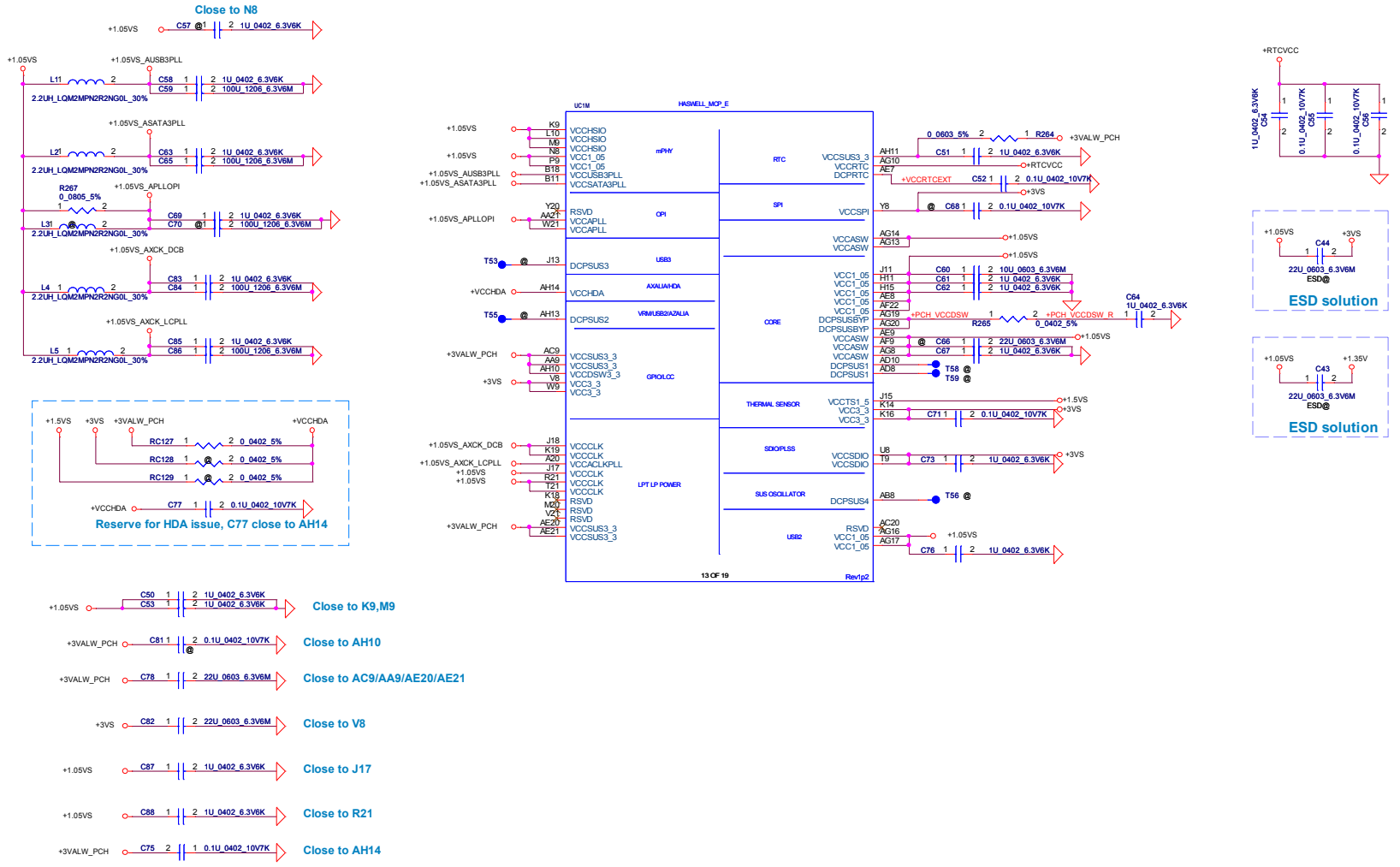
Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: **MCP(12/19) Power**

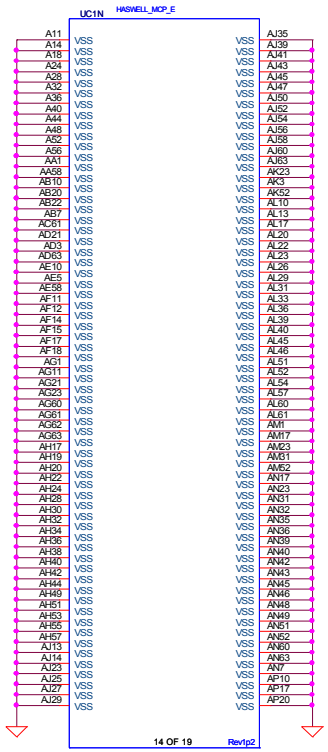
Size	Document Number	Rev
	LA-9981P	0.2

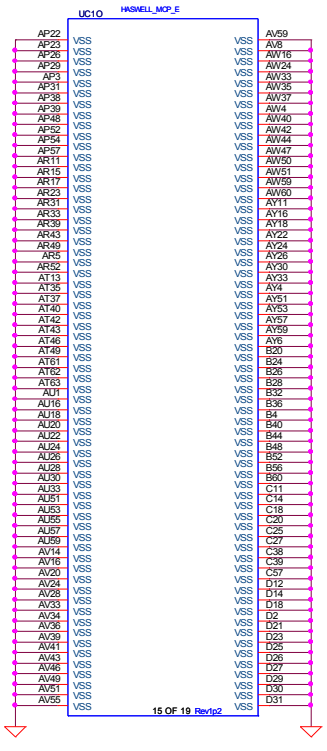
Date: Saturday, March 09, 2013 Sheet 13 of 55

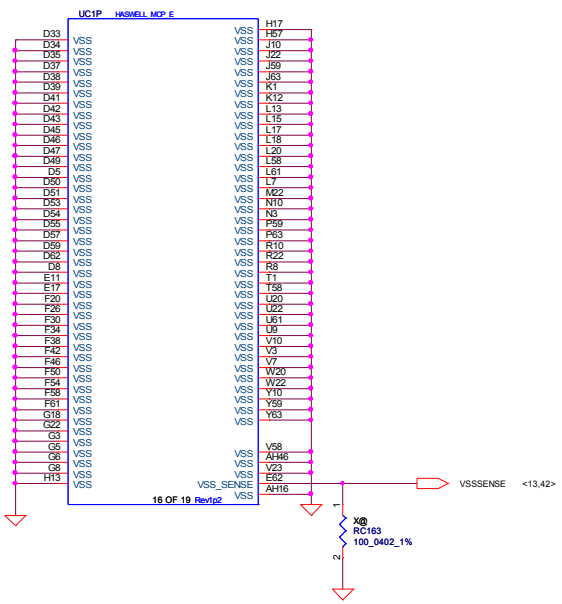


Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.			
Title	MCP(13/19) Power		
Size	Document Number		Rev
	LA-9981P		0.2
Date:	Saturday, March 09, 2013	Sheet 14 of 55	



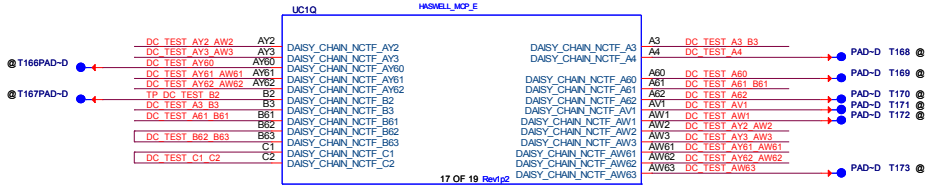


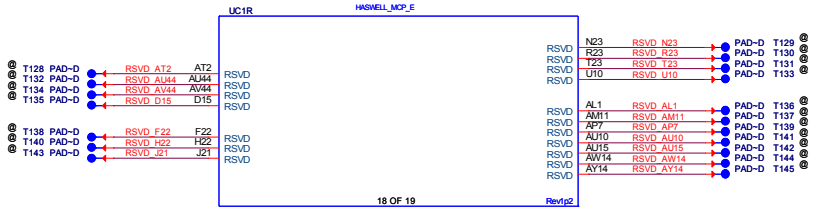


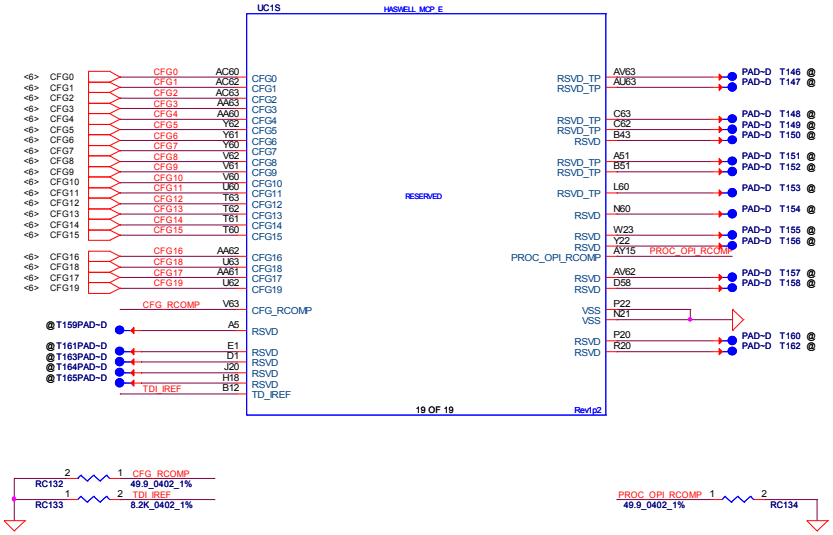
CAD Note: RC163 SHOULD BE PLACED CLOSE TO CPU

Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

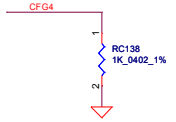
Compal Electronics, Inc.			
Title	MCP(14,15,16/19) VSS		
Size	Document Number		Rev
	LA-9981P		0.2
Date:	Saturday, March 09, 2013	Sheet	15 of 55







CFG STRAPS for CPU



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: MCP(17,18,19/19) CFG,RSVD

Size: | Document Number: LA-9981P | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 16 of 55

H=4mm

2-3A to 1 DIMMs/channel

Populate RD1, De-Populate RD7 for Intel DDR3 VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3 VREFDQ multiple methods M3

All VREF traces should have 10 mil trace width

Layout Note: Place near JDIMM1

Note: Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note: Place near JDIMM1.203,204

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN

DDR3L SODIMM ODT GENERATION

ESD solution

Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: DDRIII DIMMA

Size: | Document Number: LA-9981P | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 17 of 55

H=4mm

2-3A to 1 DIMMs/channel

Populate RD4, De-Populate RD8 for Intel DDR3 VREFDQ multiple methods M1
Populate RD8, De-Populate RD4 for Intel DDR3 VREFDQ multiple methods M3

<7> DDR_B_DQS#[0..7]
<7> DDR_B_D[0..63]
<7> DDR_B_DQS[0..7]
<7> DDR_B_MA[0..15]

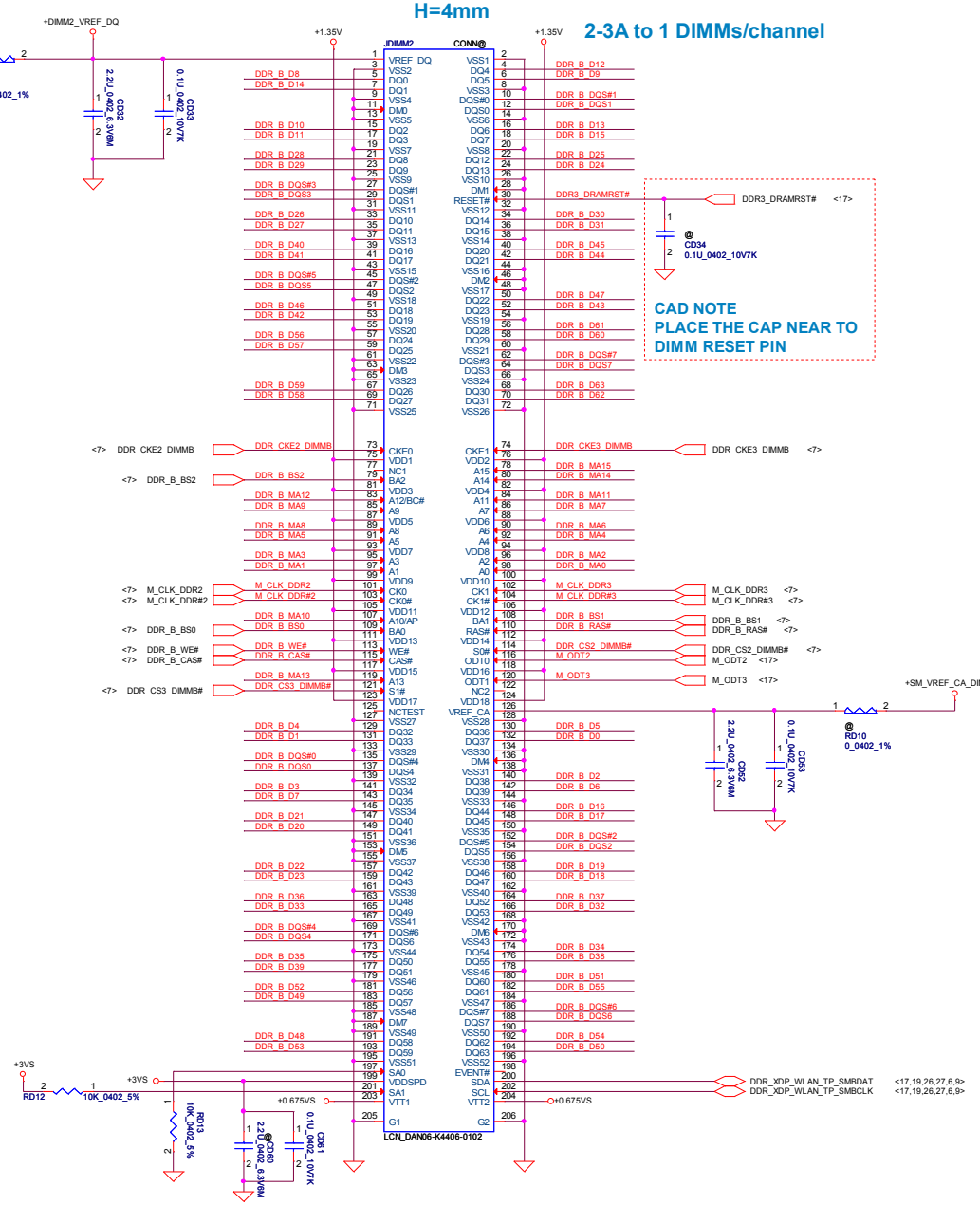
All VREF traces should have 10 mil trace width

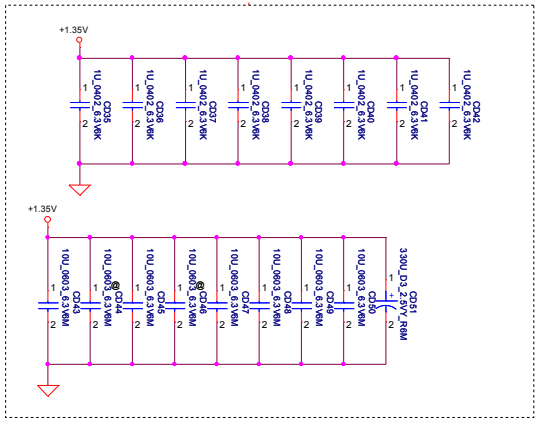
Layout Note: Place near JDIMM2

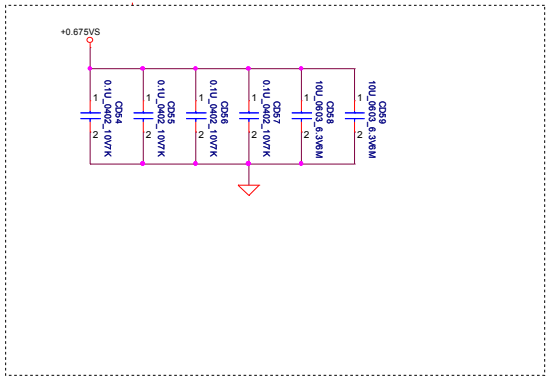
Note: Check voltage tolerance of VREF_DQ at the DIMM socket

Layout Note: Place near JDIMM2.203,204

CAD NOTE
PLACE THE CAP NEAR TO DIMM RESET PIN







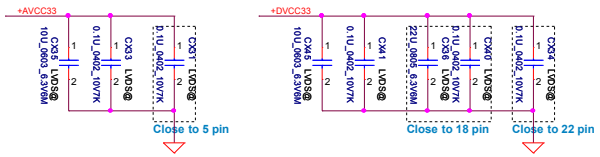
Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

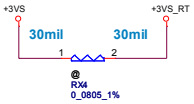
Compal Electronics, Inc.

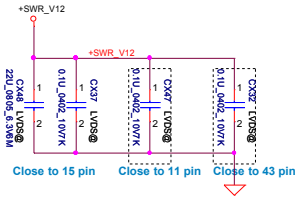
Title: DDRIII DIMMB

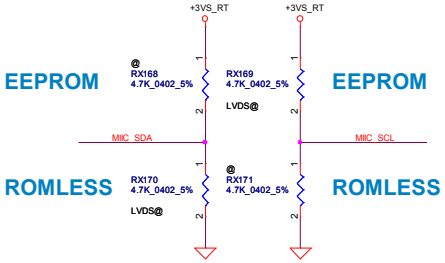
Size	Document Number	Rev
	LA-9981P	0.2

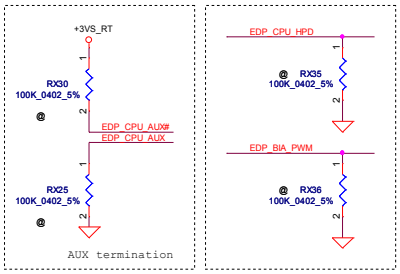
Date: Saturday, March 09, 2013 Sheet 18 of 55

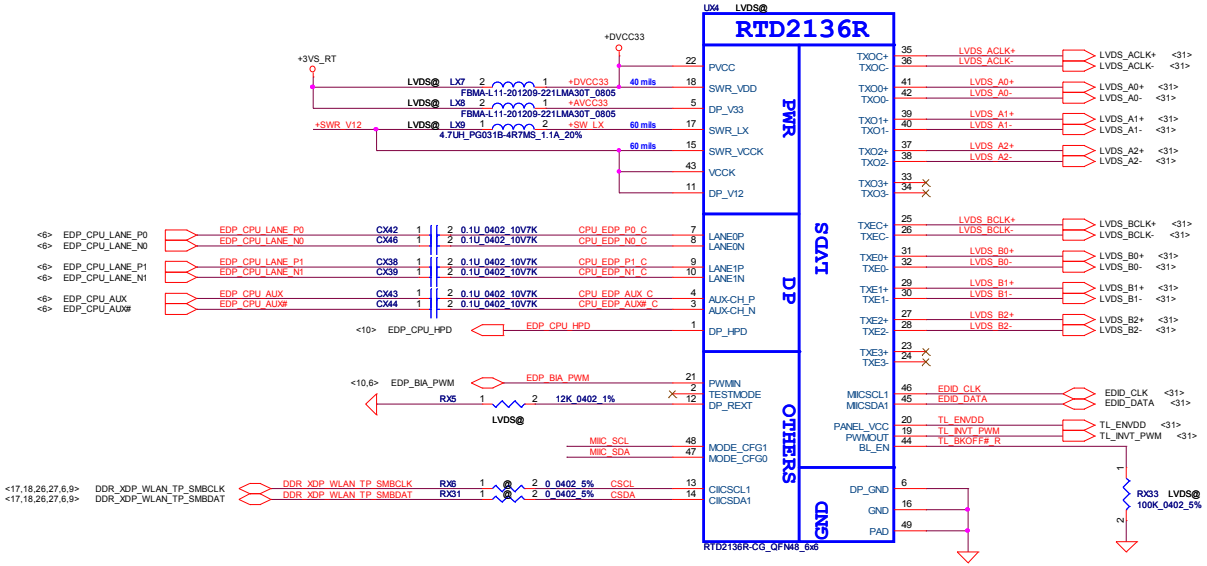




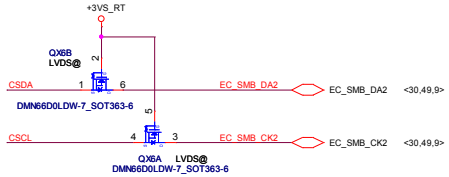


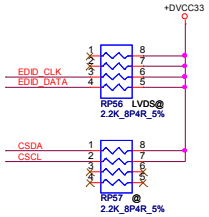




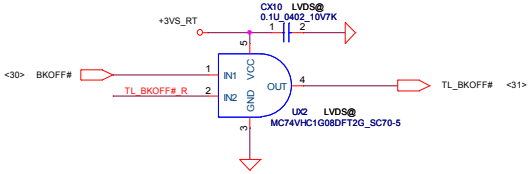


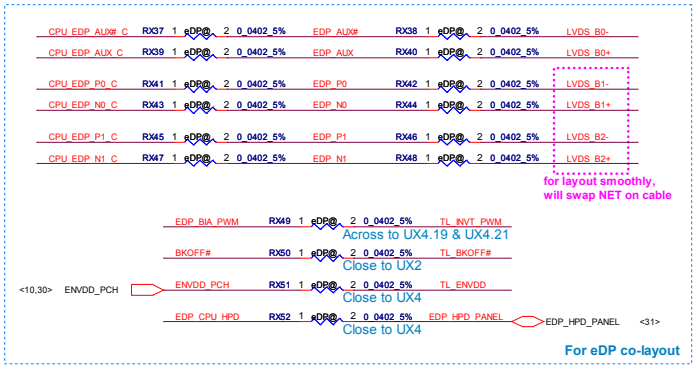
RTD2136S : SA00004NW10
RTD2136R : SA000067100





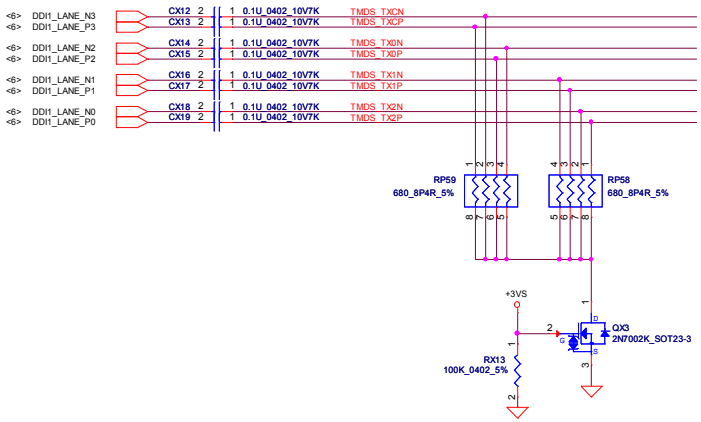
Vendor advise reserve it

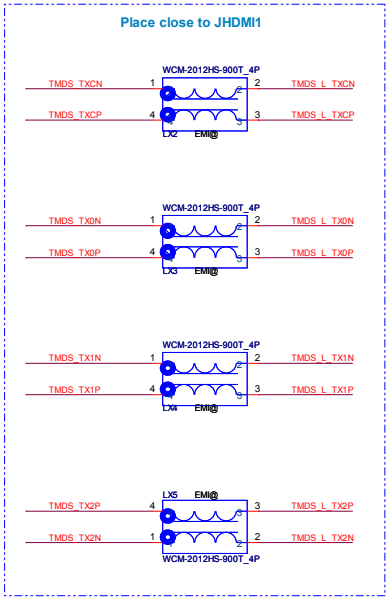


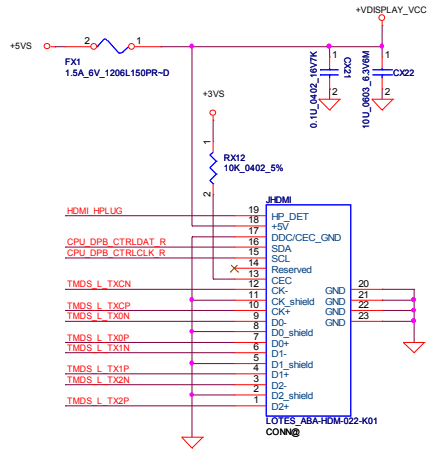


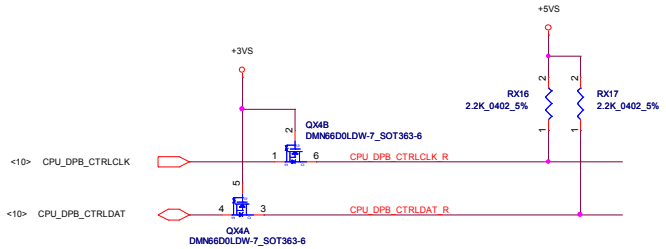
Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

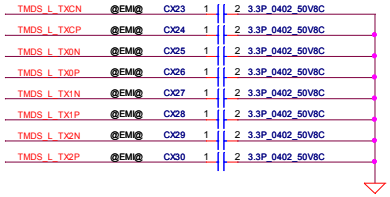
Compal Electronics, Inc.		
Title: eDP to LVDS converter		
Size	Document Number: LA-9981P	Rev: 0.2
Date: Saturday, March 09, 2013	Sheet 19 of 55	

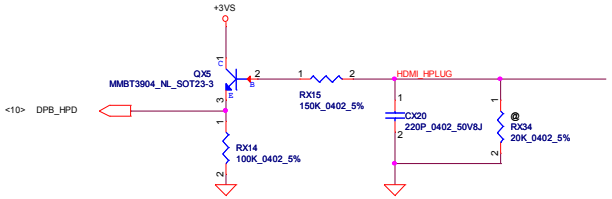












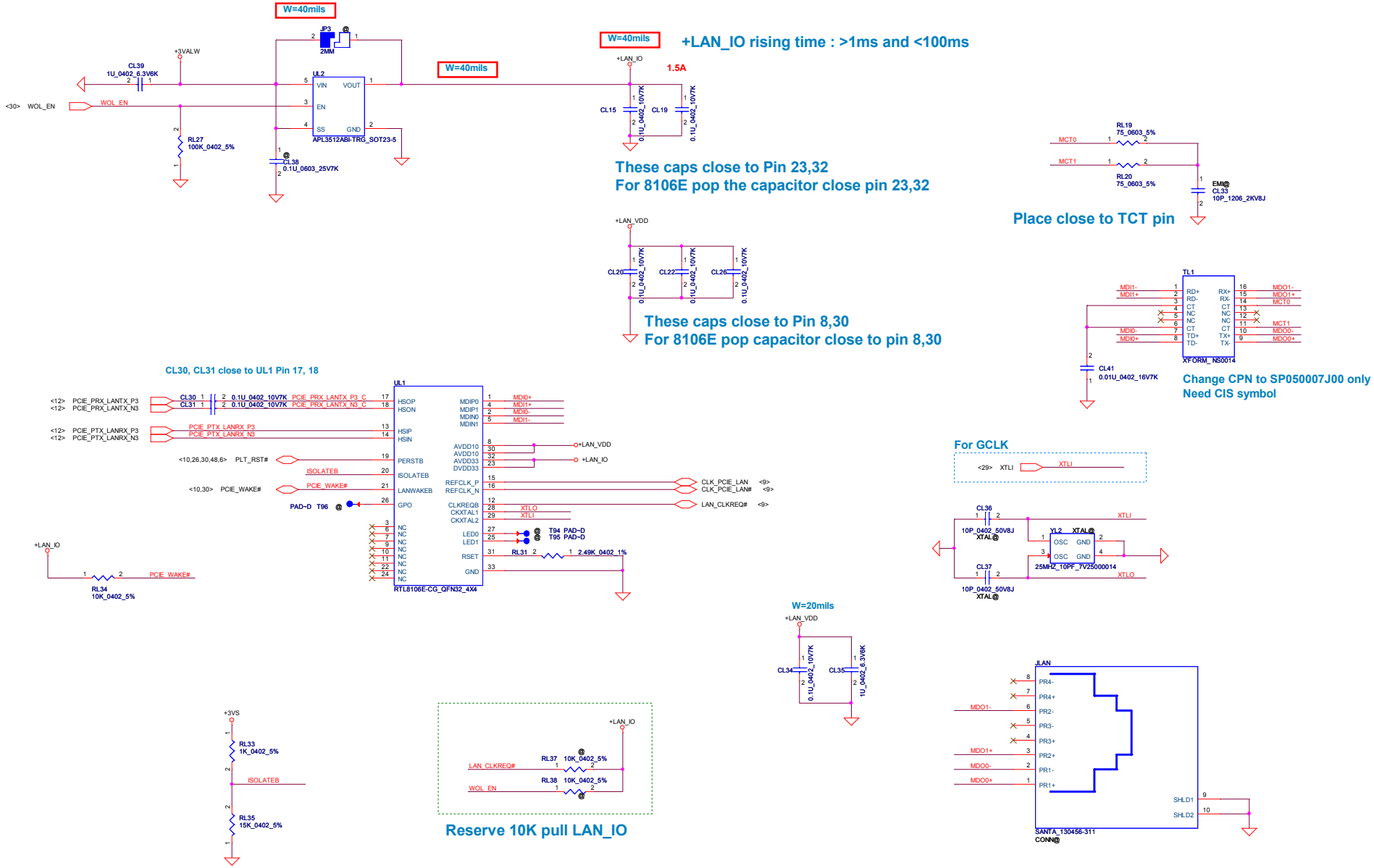
Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: HDMI

Size | Document Number: LA-9981P | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 20 of 55



Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.	
Title	LAN RTL8106E
Size	Document Number: LA-9981P
Rev	0.2
Date: Saturday, March 09, 2013	Sheet 21 of 55

Reserve for HDA issue

CA71, CA51 place close to Pin 26

CA53, CA55 change Value from 10U_0603_6.3V6M~D to 4.7U_0603_6.3V6K

CA57,CA58 close to UA1 pin1

RA51, RA33 place close to UA1

JACK_PLUG Delay circutis

Reserve for cancel Delay circutis

Place on the moat between GND & GNDA.

SM01000BV00
need CIS symbol

EC Beep

MCU Beep

PC Beep

Close to UA1
Pin11,13,14,16

close to Codec

Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

iPhone and Nokia type Combo Jack

40mil

40mil

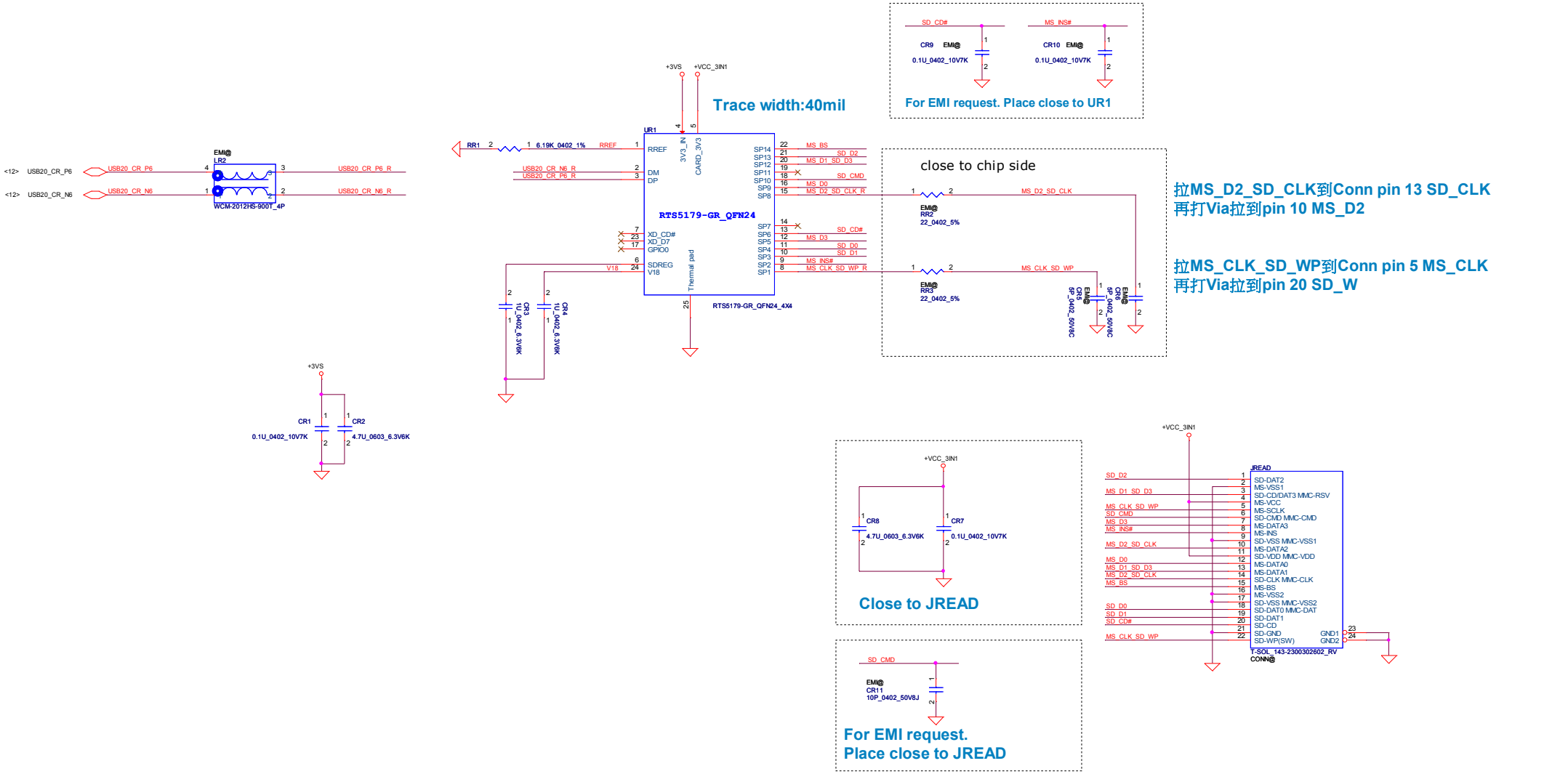
Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: Audio Codec ALC3223

Size: | Document Number: LA-9981P | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 22 of 55



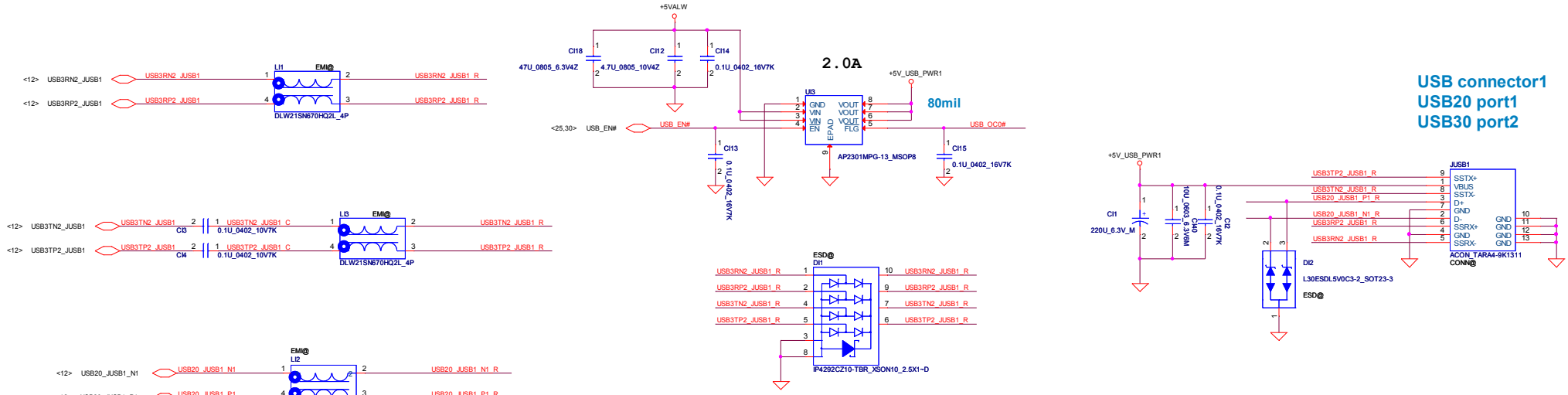
Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

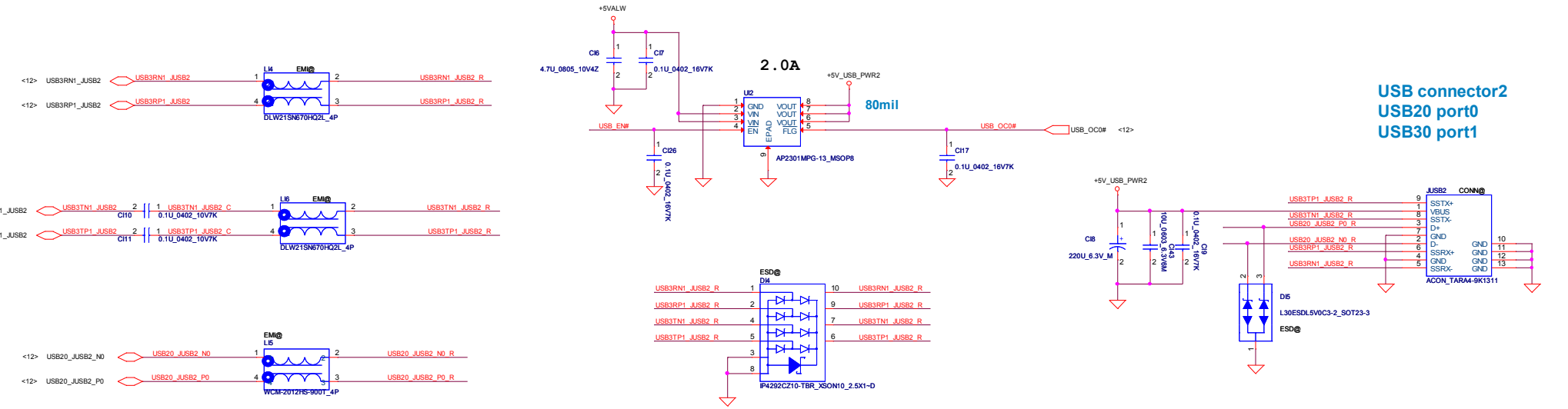
Compal Electronics, Inc.

Title: **Card Reader RTS5179**

Size	Document Number	Rev
	LA-9981P	0.2

Date: Saturday, March 09, 2013 Sheet 23 of 55





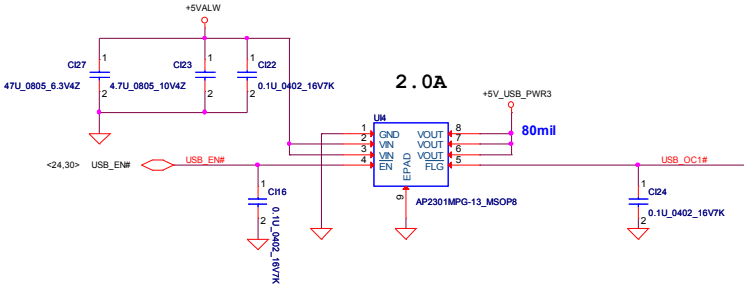
Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

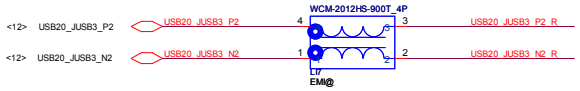
Compal Electronics, Inc.

Title: **USB3.0**

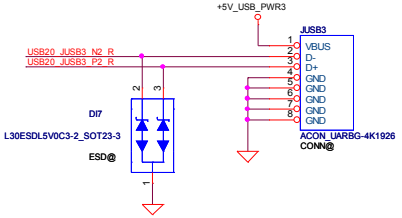
Size: | Document Number: **LA-9981P** | Rev: 0.2

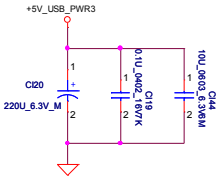
Date: Saturday, March 09, 2013 | Sheet 24 of 55



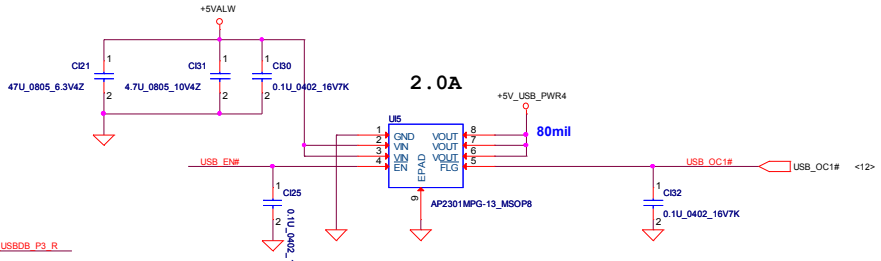


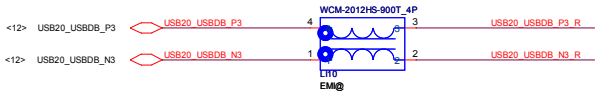
USB connector3
USB20 port2



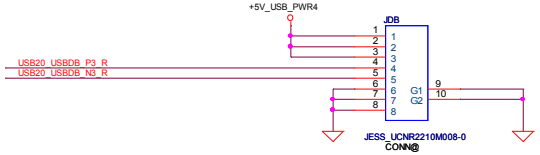


Place close to JUSB3





USB connector4
USB20 port3



2nd: SP01001EX00
Main: SP01001AA00
Change CONN symbol for DFB

Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

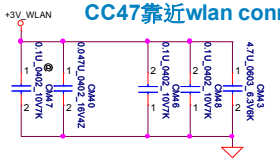
Compal Electronics, Inc.

Title: MB to USB2.0 DB

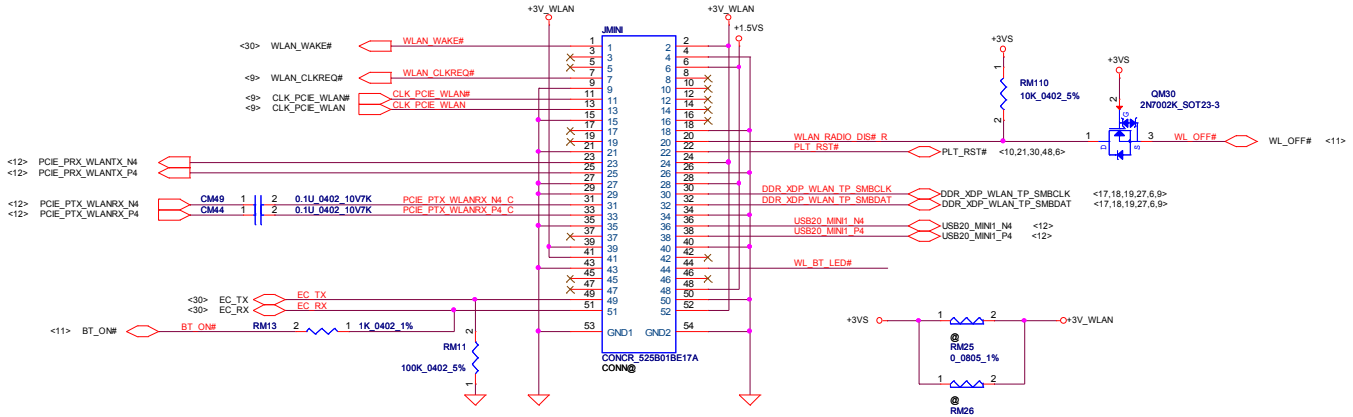
Size: | Document Number: LA-9981P | Rev: 0.2

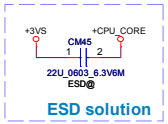
Date: Saturday, March 09, 2013 | Sheet 25 of 55

CC47靠近wlan connector



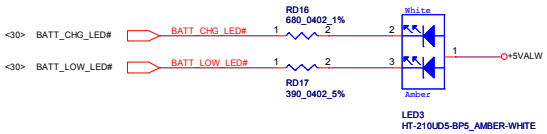
Mini WLAN/WIMAX H=6.7





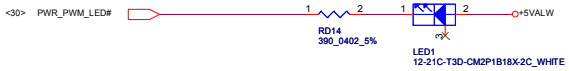
HDD LED

Battery LED

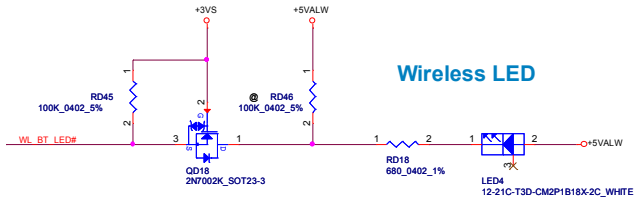


10mils, All pins

Power LED



Wireless LED



Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

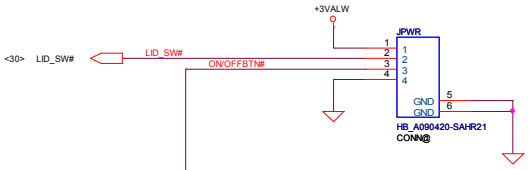
Compal Electronics, Inc.

Title: Mini Card/LED

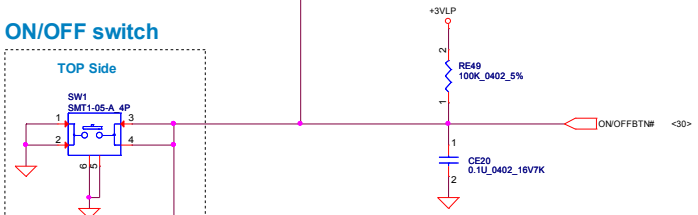
Size: | Document Number: LA-9981P | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 26 of 55

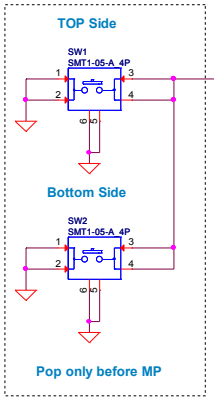
POWER/B



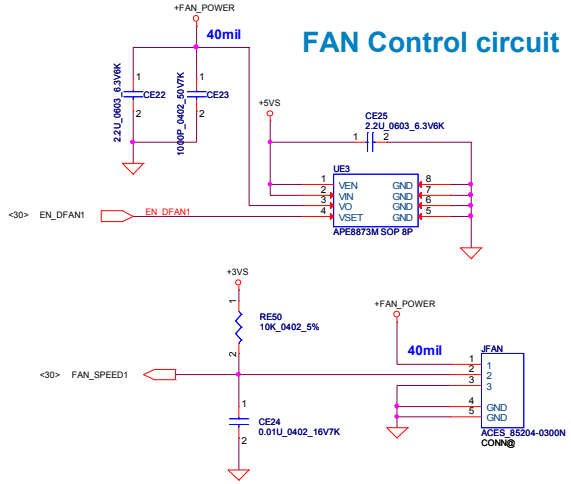
Power ON Circuit



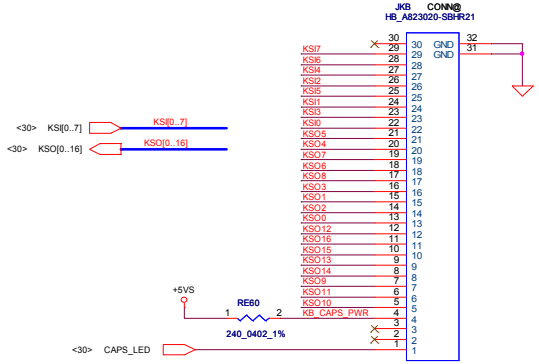
ON/OFF switch



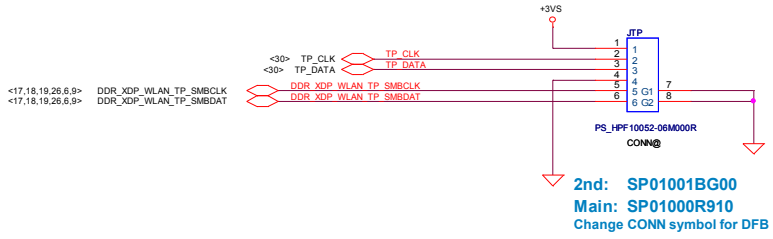
FAN Control circuit



INT_KBD Connector



Touch pad

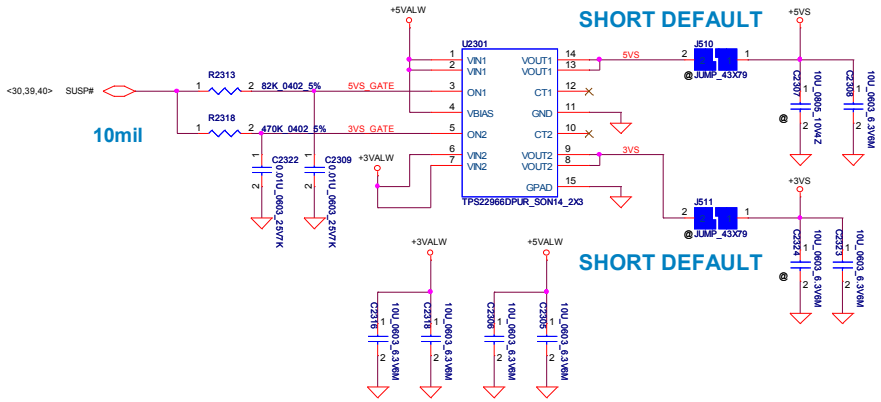


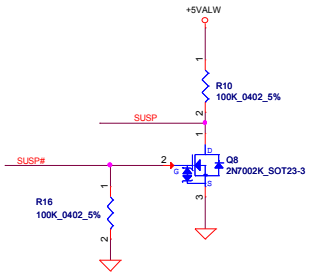
2nd: SP01001BG00
Main: SP01000R910
Change CONN symbol for DFB

Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

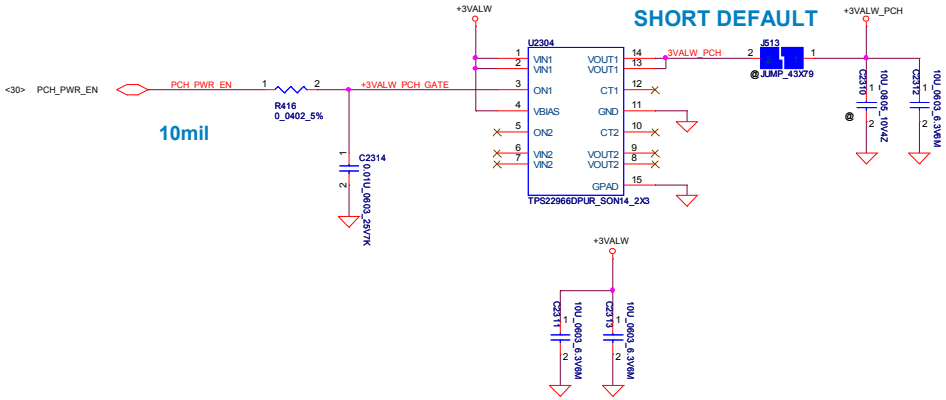
Compal Electronics, Inc.	
Title	FAN/TP/PWR SW
Size	Document Number: LA-9981P
Rev	0.2
Date: Saturday, March 09, 2013	Sheet 27 of 55

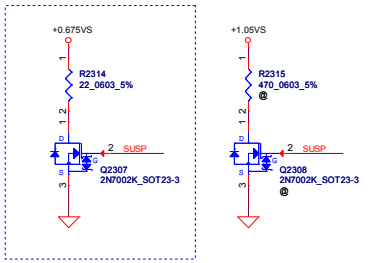
+5VS and +3VS switch





+3VALW_PCH switch





For Intel S3 Power Reduction

Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: DC/DC Interface

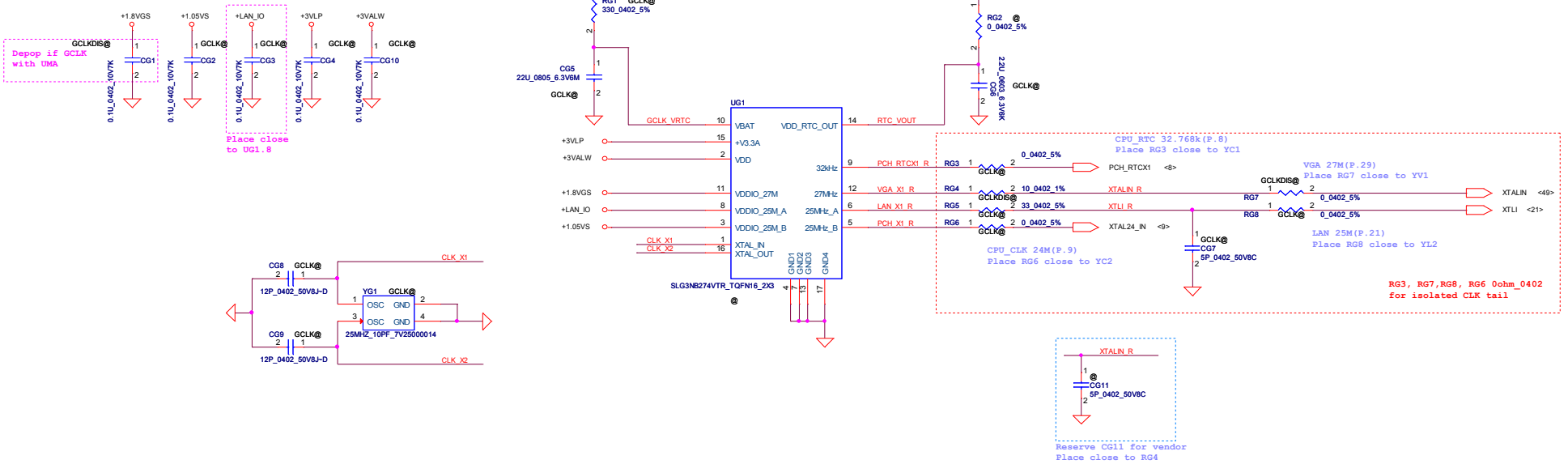
Size | Document Number: LA-9981P | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 28 of 55

UG1 GCLKUMA@ SLG3NB244VTR TQFN 16P CLK GEN

UG2 GCLKDIS@ SLG3NB244VTR TQFN 16P CLK GEN

SLG3NB3374V is for DIS by output 24M*1,25M*1, 27M*1, 32K*1
SLG3NB3375V is for UMA by output 24M81, 25M*1, 32K*1



Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: **GCLK**

Size | Document Number: **LA-9981P** | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 23 of 55

SD034120280	12K_0402_1%
SD034100300	27K_0402_1%
SD034430280	33K_0402_1%
SD034430280	43K_0402_1%
SD034560280	56K_0402_1%
SD034750280	75K_0402_1%
SD034100380	100K_0402_1%

Board ID
Venus DIS@
UMA UMA@

RE5 UMA@ 75K_0402_1%
SD034750280

+3VALW
RE3 100K_0402_1%
Ra
AD_BID0
Rb
RE5 33K_0402_1% DIS@
CE8 0.1U_0402_10V7K

+3VS
TP_CLK 4.7K_0402_5% RE9
TP_DATA 4.7K_0402_5% RE10

+3VALW
CE1 0.1U_0402_10V7K
CE2 0.1U_0402_10V7K
@EMI@ CE5 1000P_0402_50V7K
@EMI@ CE6 1000P_0402_50V7K
EMI@ LE1 FBMA-L11-160808-800LMT_0603
+EC_VCCA
CE7 0.1U_0402_10V7K
+3VLP
ECAGND <36>

UE1

"KB_LED_PWM" for OAK 17 only

PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
SM Bus
GPIO
GPO
GPI
LPC & MISC

GATEA20/GPIO00
KBRST#/GPIO01
SERIRQ
LPC_LFRAME#
LPC_AD3
LPC_AD2
LPC_AD1
LPC_AD0
CLK_PCI_EC
PCIRST#/GPIO05
EC_RST#
EC_SCI#/GPIO0E
GPIO1D
KSI0/GPIO30
KSI1/GPIO31
KSI2/GPIO32
KSI3/GPIO33
KSI4/GPIO34
KSI5/GPIO35
KSI6/GPIO36
KSI7/GPIO37
KSO0/GPIO20
KSO1/GPIO21
KSO2/GPIO22
KSO3/GPIO23
KSO4/GPIO24
KSO5/GPIO25
KSO6/GPIO26
KSO7/GPIO27
KSO8/GPIO28
KSO9/GPIO29
KSO10/GPIO2A
KSO11/GPIO2B
KSO12/GPIO2C
KSO13/GPIO2D
KSO14/GPIO2E
KSO15/GPIO2F
KSO16/GPIO48
KSO17/GPIO49
EC_SMB_CK1/GPIO44
EC_SMB_DA1/GPIO45
EC_SMB_CK2/GPIO46
EC_SMB_DA2/GPIO47
PM_SLP_S3#/GPIO04
PM_SLP_S5#/GPIO07
EC_SMI#/GPIO08
GPIO0A
GPIO0B
GPIO0C
GPIO0D
EC_INVT_PWM/GPIO11
FAN_SPEED1/GPIO14
EC_PME#/GPIO15
EC_TX/GPIO16
EC_RX/GPIO17
PCH_PWROK/GPIO18
SUSP_LED#/GPIO19
NUM_LED#/GPIO1A
XCLKI/GPIO5D
XCLKO/GPIO5E
GPIO0F
BEEP#/GPIO10
GPIO12
ACOFF/GPIO13
BATT_TEMP/GPIO38
GPIO39
ADP_I/GPIO3A
GPIO3B
GPIO42
IMON/GPIO43
DAC_BRIG/GPIO3C
EN_DFAN1/GPIO3D
IREF/GPIO3E
CHGVADJ/GPIO3F
EC_MUTE#/GPIO4A
USB_EN#/GPIO4B
CAP_INT#/GPIO4C
EAPD/GPIO4D
TP_CLK/GPIO4E
TP_DATA/GPIO4F
CPU1.5V_S3_GATE/GPXIOA00
WOL_EN/GPXIOA01
ME_EN/GPXIOA02
VCIN0_PH/GPXIOD00
SPID/GPIO5B
SPIDO/GPIO5C
SPICLK/GPIO5B
SPICS#/GPIO5A
ENBKL/GPIO40
PECI_KB930/GPIO41
FSTCHG/GPIO50
BATT_CHG_LED#/GPIO52
CAPS_LED#/GPIO53
PWR_LED#/GPIO54
BATT_LOW_LED#/GPIO55
SYSON/GPIO56
VR_ON/GPIO57
PM_SLP_S4#/GPIO59
EC_RSMRST#/GPXIOA03
EC_LID_OUT#/GPXIOA04
PROCHOT_IN/GPXIOA05
H_PROCHOT#_EC/GPXIOA06
VCOUT0_PH/GPXIOA07
BKOFF#/GPXIOA08
PBTN_OUT#/GPXIOA09
PCH_APWROK/GPXIOA10
SA_PGOOD/GPXIOA11
AC_IN/GPXIOD01
EC_ON/GPXIOD02
ON/OFFBTN#/GPXIOD03
LID_SW#/GPXIOD04
SUSP#/GPXIOD05
GPXIOD06
PECI_KB9012/GPXIOD07
V18R
+1.05V_PGOOD
VCCST_PG_EC
KB9012QF-A4_LQFP128_14X14

KB_RST# SERIRQ LPC_LFRAME# LPC_LAD3 LPC_LAD2 LPC_LAD1 LPC_LAD0
CLK_PCI_LPC PLT_RST# EC_RST# EC_SCI# TOUCH_RST
@EMI@ CE12 0.1U_0402_10V7K
@EMI@ R2354 0_0402_5%
RE8 47K_0402_5%
CE11 0.1U_0402_10V7K
"TOUCH_RST" for OAK 15 only

KSI[0..7]
KSO[0..16]

LID_SW#
WLAN_WAKE#
RE71 10K_0402_5%
RE70 10K_0402_5%

RP36 2.2K_0804_8P4R_5%
EC_SMB_CK1 EC_SMB_DA1 EC_SMB_CK2 EC_SMB_DA2

RE37 0_0402_5%

Reserve for ESD
CE27 ESD@ 0.1U_0402_10V7K SIO_SLP_S3#
CE28 ESD@ 0.1U_0402_10V7K SIO_SLP_S5#
Please close to EC

PCH_PWROK
RE18 10K_0402_5%

FAN_SPEED1
CE29 220P_0402_50V8J
Please close to EC

SIO_SLP_S3# SIO_SLP_S5# EC_SMI# PS_ID CE_EN DGPU_PWROK ENVDD_PCH DBC_EN FAN_SPEED1 PCIE_WAKE# EC_TX EC_RX PCH_PWROK ME_SUS_PWR_ACK RUNPWROK

+1.05V_PGOOD VCCST_PG_EC

KB_LED_PWM BEEP# USB_EN# ACOFF
BATT_TEMP ADP_I AD_BID0 PANEL_BKLEN
CE9 100P_0402_50V8J ECAGND
PCH_HOT# RE7 0_0402_5%
EN_INVPWR EN_DFAN1 EC_ENVDD LCD_TEST
EC_MUTE# SIO_SLP_S4# IMVP_PWRGD SYS_PWROK TP_CLK TP_DATA
SUSACK# WOL_EN ME_EN VCIN0_PH
EC_SPI_MOSI_1 EC_SPI_MISO_1 EC_SPI_CLK_R EC_SPI_CS0#
WLAN_WAKE# SIO_SLP_S0# BATT_CHG_LED# CAPS_LED PWR_PWM_LED# BATT_LOW_LED#
SYSON
VR_ON_EC
CPU_DETECT# RE11 100K_0402_5%
EC_RSMRST# EC_LID_OUT# VCIN1_PH VCOUT1_PH VCOUT0_PH# BKOFF# PBTN_OUT# PCH_PWR_EN RE38 43_0402_1%
ACIN_65W
ACIN EC_ON ON/OFFBTN# LID_SW# SUSP# 65W/90W# PECI_EC RE43 43_0402_1%
+V18R CE16 4.7U_0805_10V4Z
ECAGND LE2 FBMA-L11-160808-800LMT_0603
20mil

VR_ON CE34 ESD@ 0.1U_0402_10V7K
Place CE34 between DE1 and RE12

VR_ON VCCST_PG_EC DE1 ESD@ L03ESDL5V0CG3-2_SOT-523-3
Place DE1 close to UE1

VR_ON RE12 0_0402_5% RE1 10K_0402_5% CE26 0.1U_0402_10V7K SYSON
EC_RSMRST# RE2 10K_0402_5%

ESD@ CE30 0.1U_0402_10V7K LID_SW#
ESD@ CE31 0.1U_0402_10V7K PCH_PWROK
ESD@ CE32 0.1U_0402_10V7K SYS_PWROK
ESD@ CE33 0.1U_0402_10V7K CPU_DETECT#
Place CE30,CE31,CE32,CE33 close to UE1

ACIN CE18 100P_0402_50V8J

ME_FWP PCH has internal 20K PD.
(suspend power rail)
ME_EN RE326 1K_0402_5%

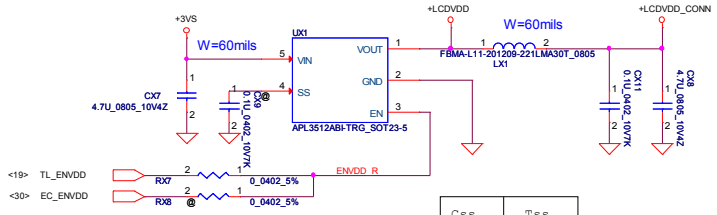
+3VS
<42> VR_HOT# VR_HOT#
@ RE44 0_0402_1%
<36,6> H_PROCHOT# H_PROCHOT#
UE2 SN74LVC1G06DCKR_SC70-5
CE15 0.1U_0402_10V7K
CE19 47P_0402_50V8J
VCOUT1_PH RE47 100K_0402_5%

KB9012A3 change to
KB9012A4 SA00004OB30

Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

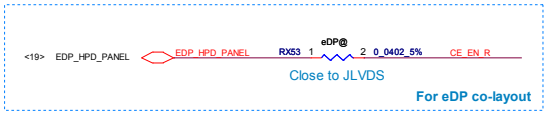
Compal Electronics, Inc.
Title: EC ENE-KB9012
Size: Document Number: LA-9981P
Rev: 0.2
Date: Saturday, March 09, 2013
Sheet 30 of 55

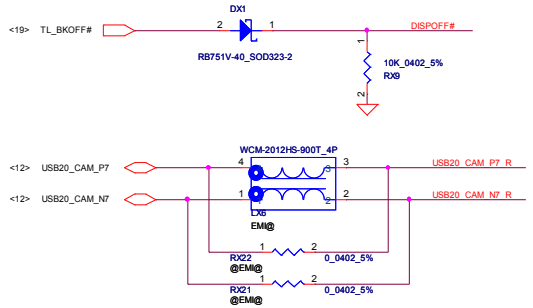
LCD PWR CTRL



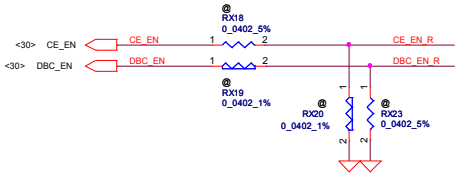
Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

SS table

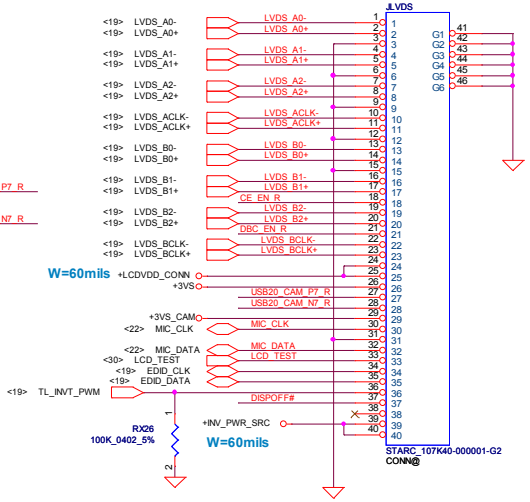


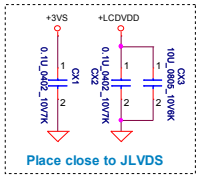


CE_EN_R only for reserve.

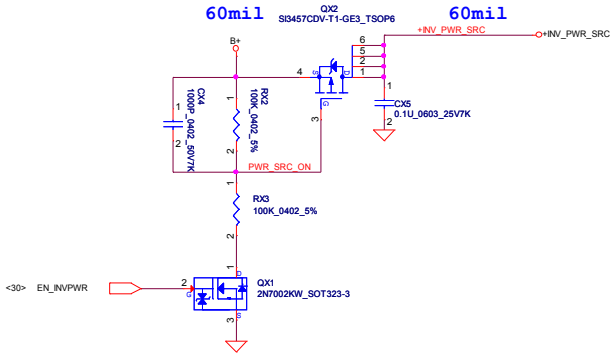


LVDS Connector

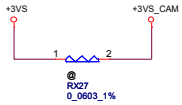




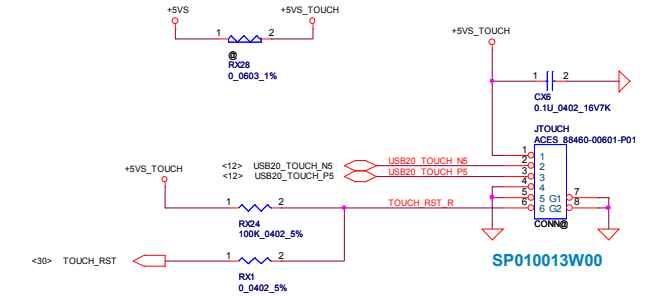
LCD backlight PWR CTRL



Webcam PWR CTRL



* Touch Screen Panel



OAK 15 only

Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

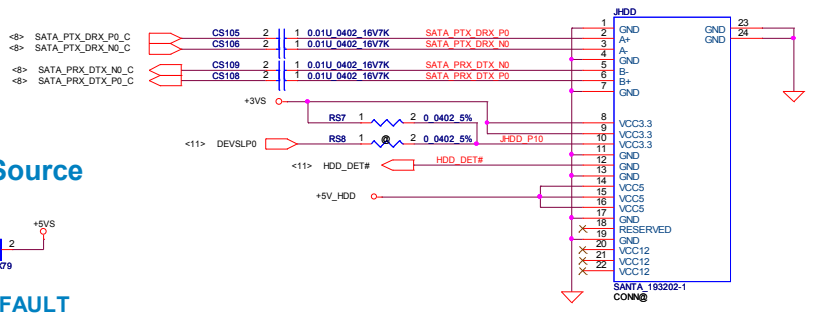
Compal Electronics, Inc.

Title: LVDS/webcam/touch

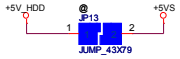
Size | Document Number: LA-9981P | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 31 of 55

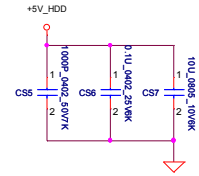
SATA HDD Connector



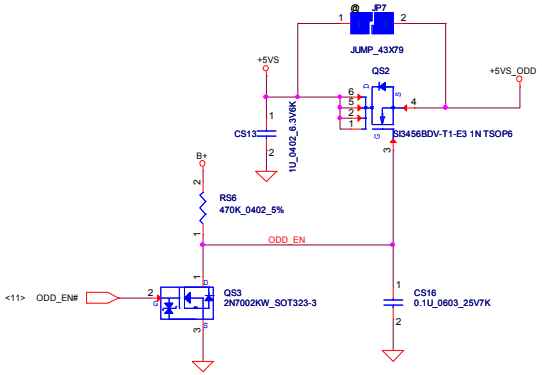
+5V_HDD Source



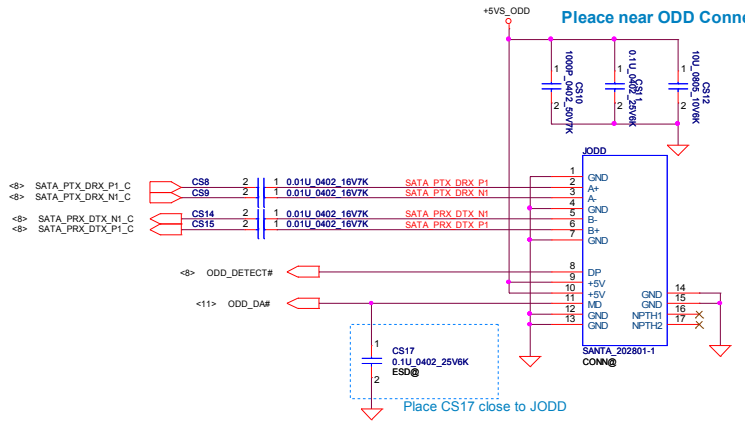
SHORT DEFAULT



ODD Power Control



SATA ODD Connector



Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

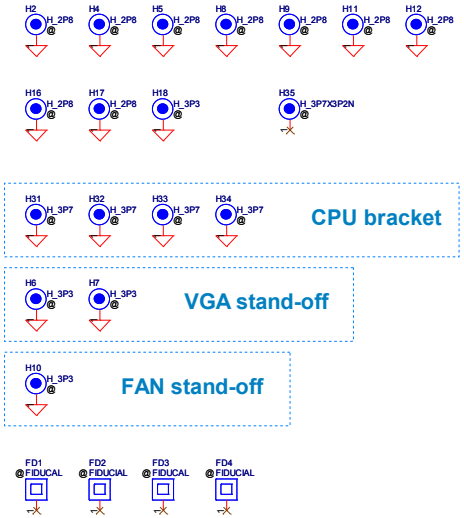
Compal Electronics, Inc.

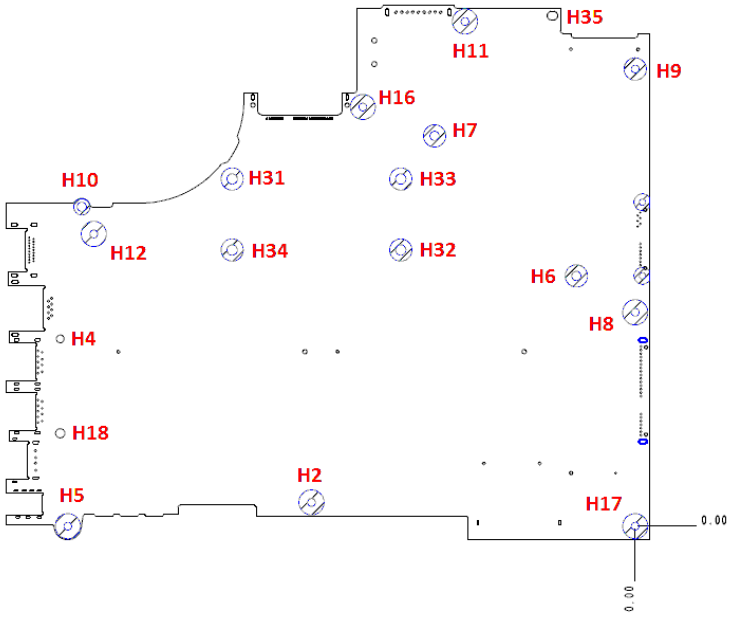
Title: **HDD/ODD**

Size | Document Number: **LA-9981P** | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 32 of 55

Screw Hole





Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: Screw Hole

Size | Document Number: LA-9981P | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 33 of 55

Version Change List (P. I. R. List)

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	34	Card Reader	2012/04/27	HW	The Card reader USB signal is incorrect.	SWAP UR1 USB signal P/N	0.2
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							
18							
19							
20							
21							
22							
23							
24							
25							
26							
27							
28							
29							
30							
31							
32							
33							
34							
35							
36							
37							
38							
39							
40							
41							

Compal Electronics, Inc.

Title: HW-PIR Page.1

Size | Document Number: LA-9981P | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 34 of 55

Version Change List (P. I. R. List)

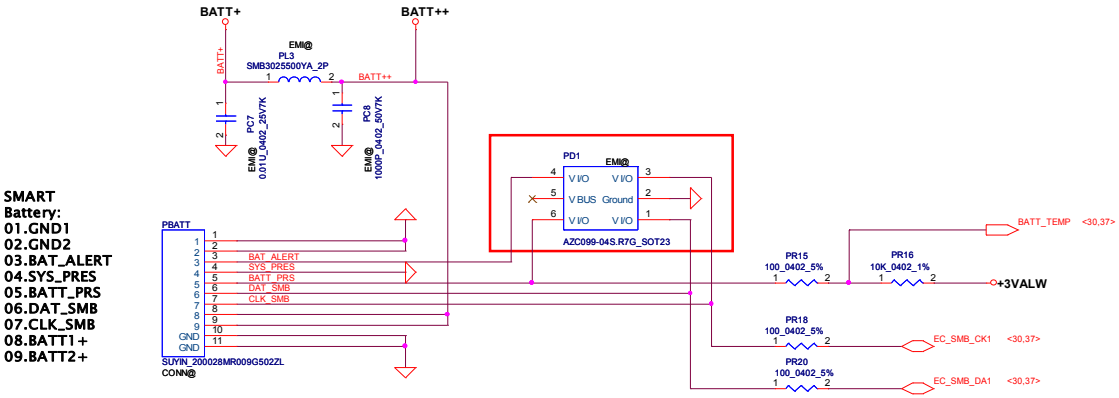
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
40							
41							
42							
43							
44							
45							
46							
47							
48							
49							
50							
51							
52							
53							
54							

Compal Electronics, Inc.

Title: HW-PIR Page.2

Size | Document Number: LA-9981P | Rev: 0.2

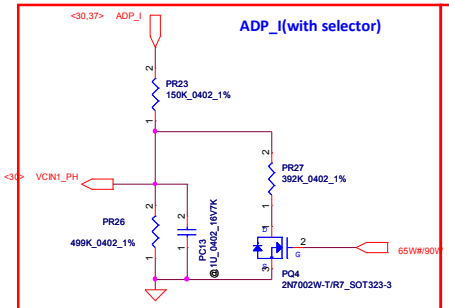
Date: Saturday, March 09, 2013 | Sheet 35 of 55



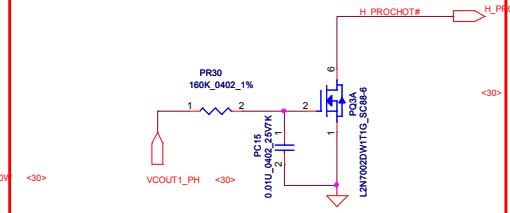
SMART Battery:
01.GND1
02.GND2
03.BAT_ALERT
04.SYS_PRES
05.BATT_PRS
06.DAT_SMB
07.CLK_SMB
08.BATT1+
09.BATT2+

Other component (37.1)

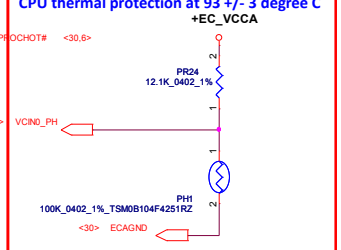
ADP_I(with selector)



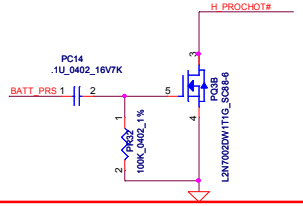
Delay adaptor OC H_PROCHOT# 2ms while hybrid power transition



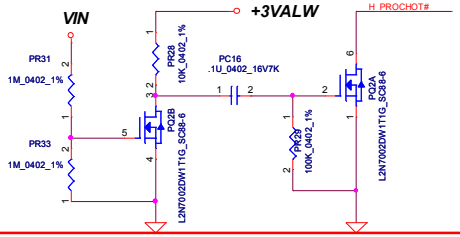
PH1 under CPU bottem side : CPU thermal protection at 93 +/- 3 degree C



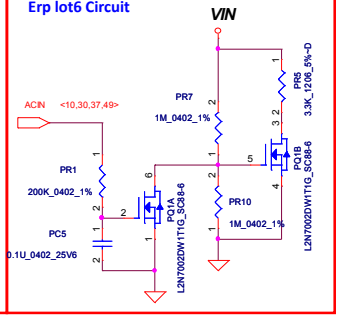
Adapter protection:
if battery removed, adaptor only,
then trigger the H_PROCHOT#,
keep @ in BOM since battery can not
be removed by end user

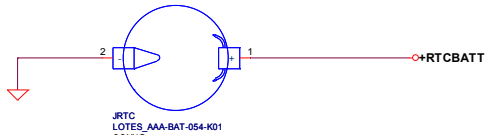


Battery protection:
asserts H_PROCHOT# when adaptor is
unplugged, keep low for 10ms
till SW PROCHOT# is issued by EC



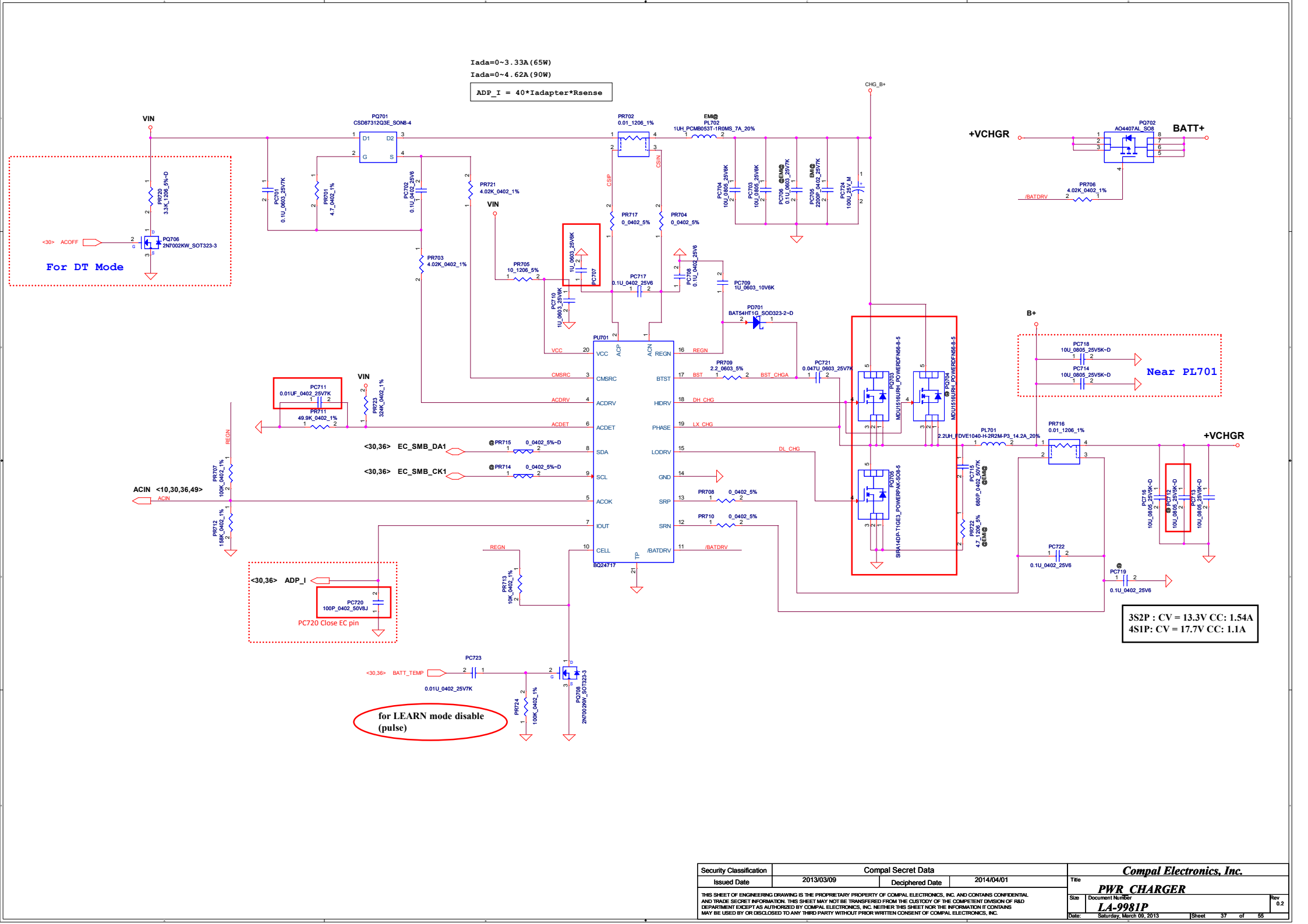
Erp lot6 Circuit





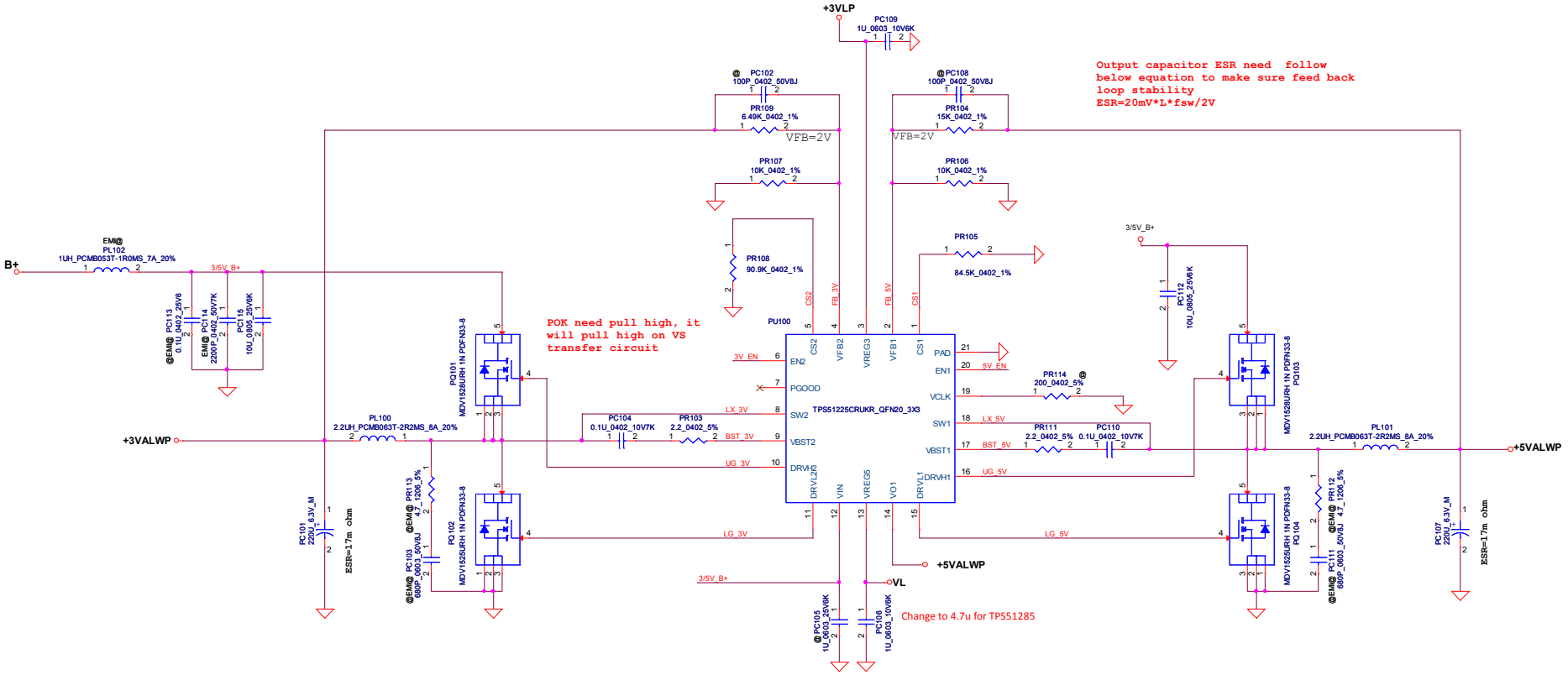
Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.			
Title	PWR_DCIN/BATT CONN/OTP		
Size	Document Number		Rev
	LA-9981P		0.2
Date: Saturday, March 09, 2013	Sheet 36 of 55		



Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

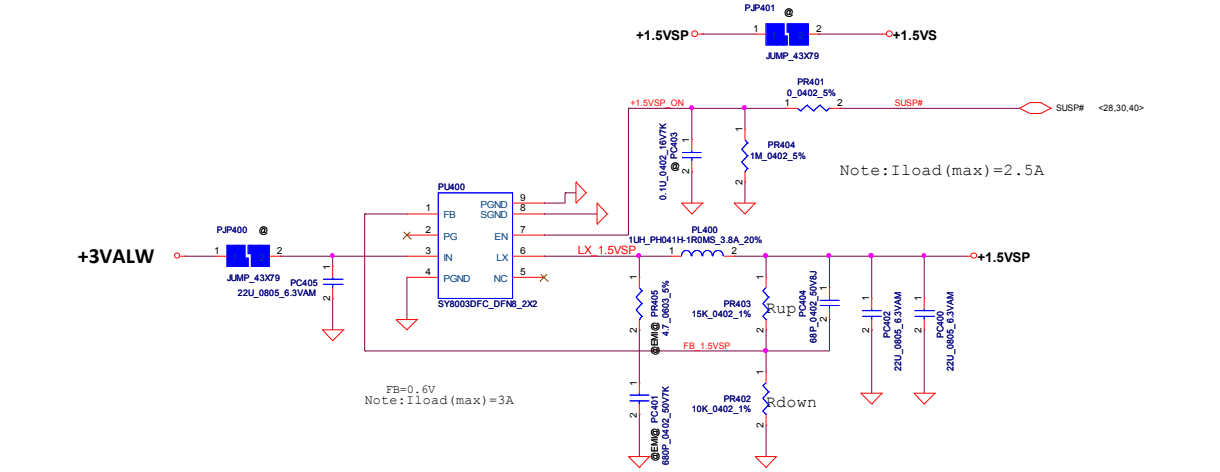
Compal Electronics, Inc.			
Title	PWR_CHARGER		
Size	Document Number	LA-9981P	Rev 0.2
Date: Saturday, March 09, 2013	Sheet 37 of 55		

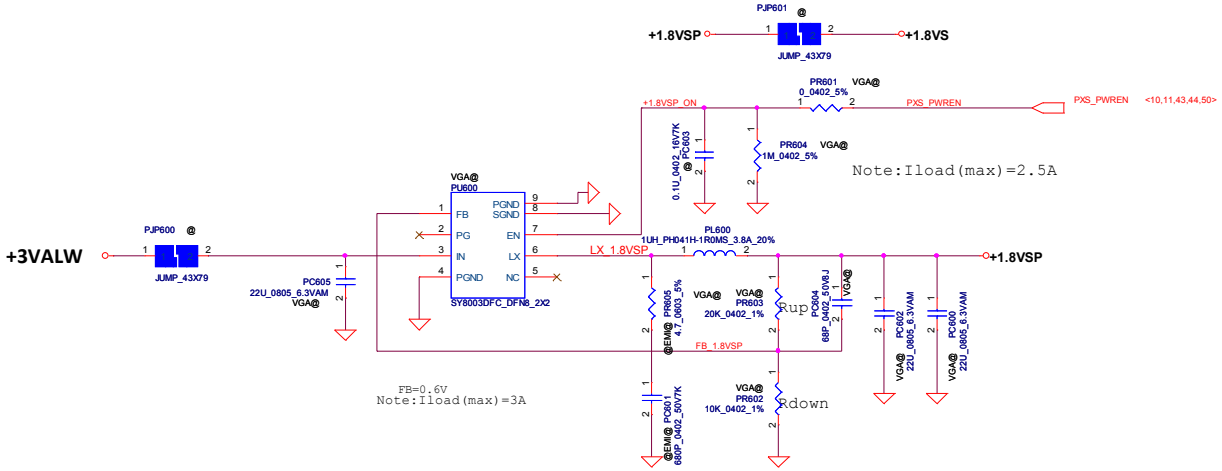


Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title	PWR_3.3VALWP/5VALWP	
Size	Document Number LA-9981P	Rev 0.2
Date: Saturday, March 09, 2013	Sheet 38 of 55	

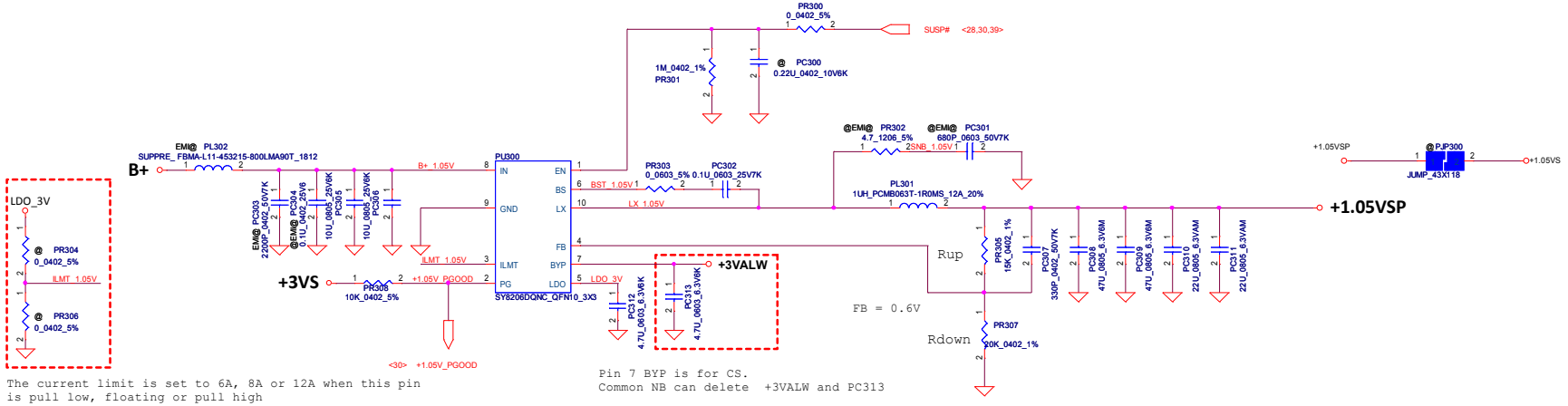




Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.	
Title	PWR_1.5VSP/1.8VSP
Size	Document Number: LA-9981P
Rev	0.2
Date: Saturday, March 09, 2013	Sheet 39 of 55

EN pin don't floating
If have pull down resistor at HW side, pls delete PR301



The current limit is set to 6A, 8A or 12A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC313

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=1.05V

+1.05VSP
TDC 5A
Peak Current 6.6A
OCP current 8A

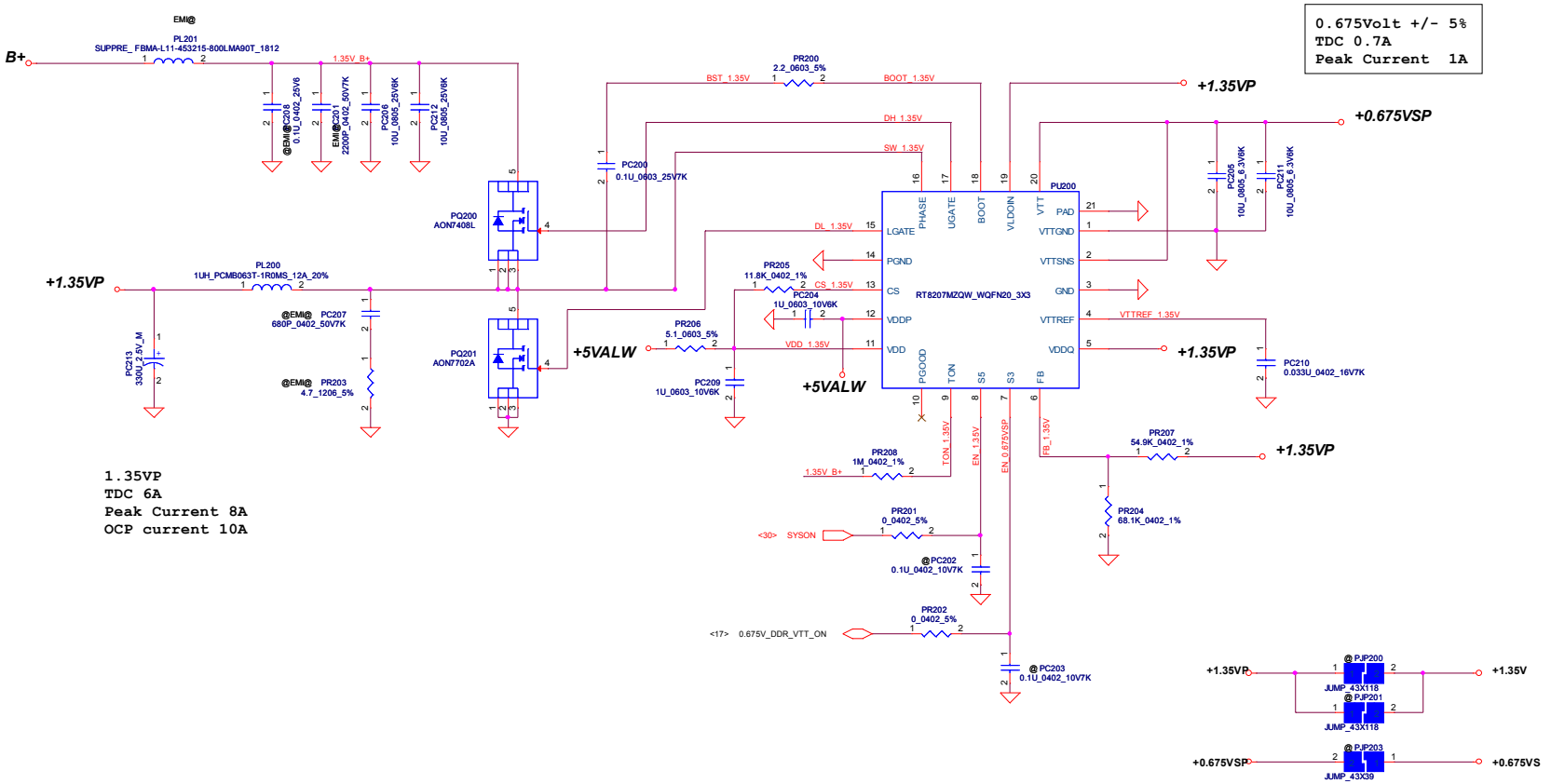
Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: PWR_+VCCIO

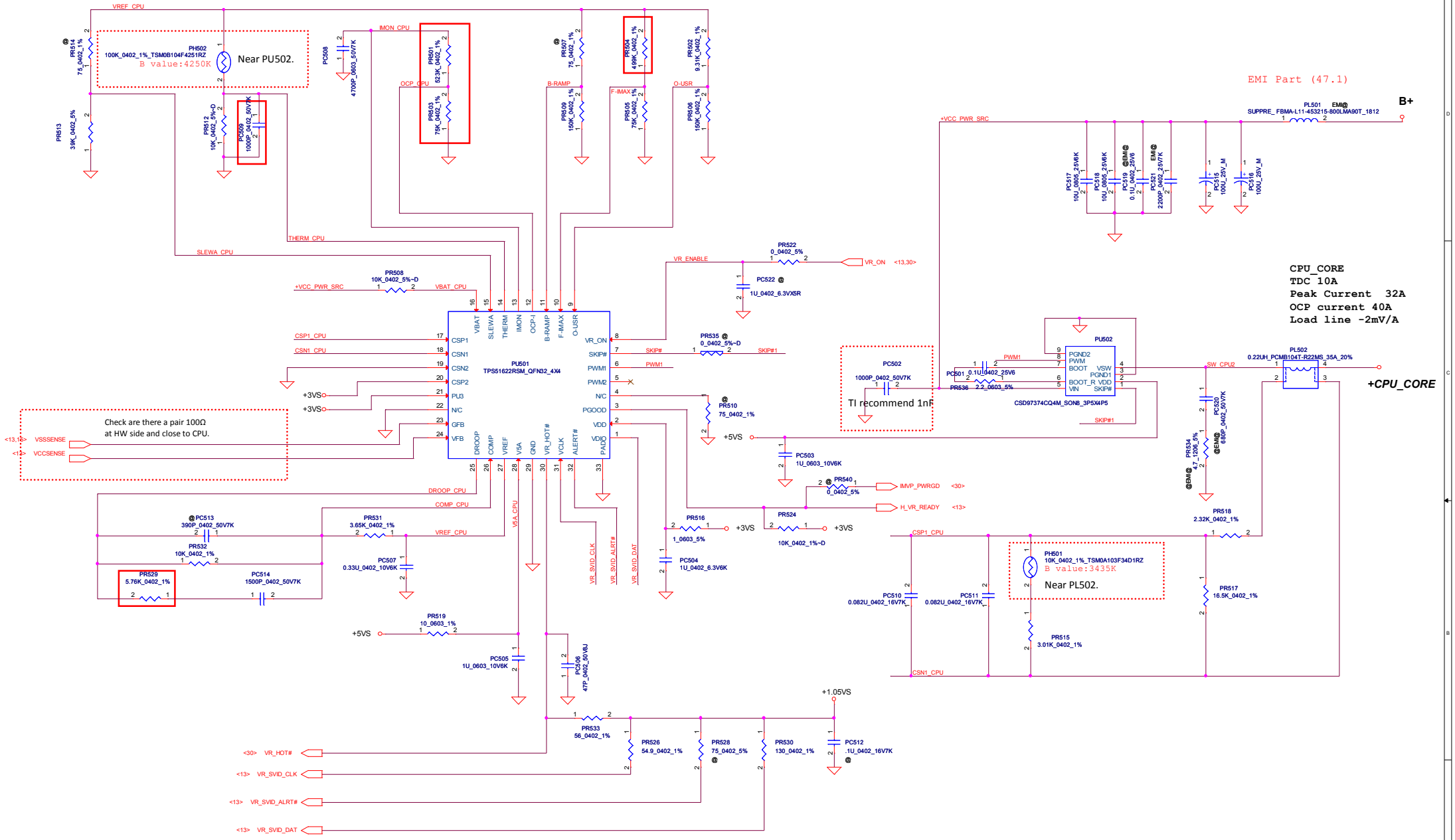
Size: C | Document Number | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 40 of 55



Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.	
Title	PWR_+1.35VP/0.675VSP
Size	Document Number: LA-9981P
Rev	0.2
Date:	Saturday, March 09, 2013
Sheet	41 of 55



Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

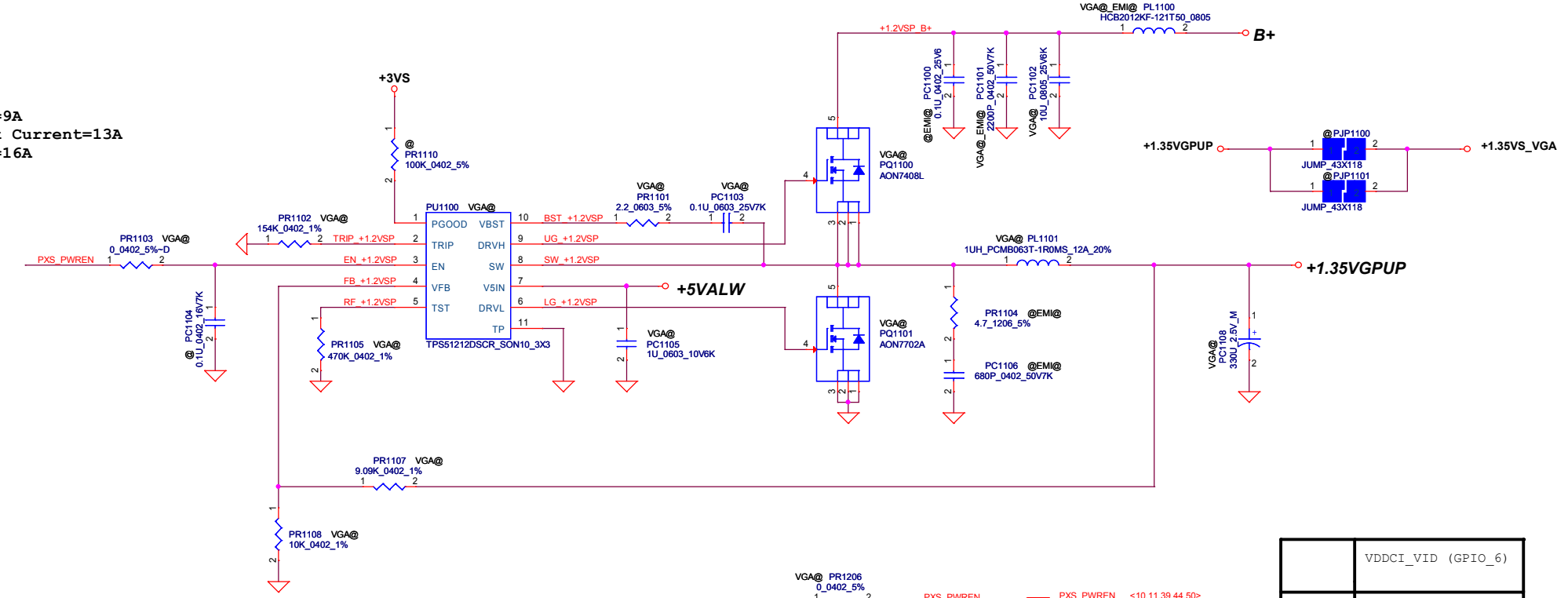
Compal Electronics, Inc.

Title: PWR_VCORE

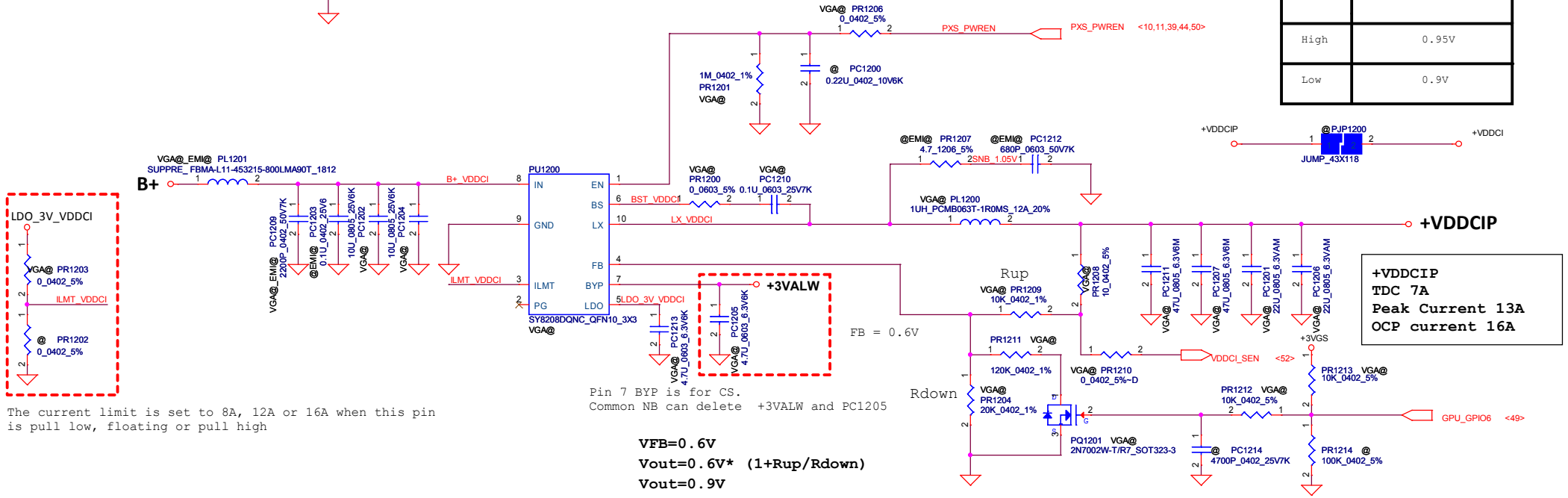
Size: | Document Number: LA-9981P | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 42 of 55

TDC=9A
Peak Current=13A
OCP=16A



	VDDCI_VID (GPIO_6)
High	0.95V
Low	0.9V



+VDDCIP
TDC 7A
Peak Current 13A
OCP current 16A

LDO_3V_VDDCI
VGA@ PR1203 0_0402_5%
ILMT_VDDCI
@ PR1202 0_0402_5%

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC1205

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)
Vout=0.9V

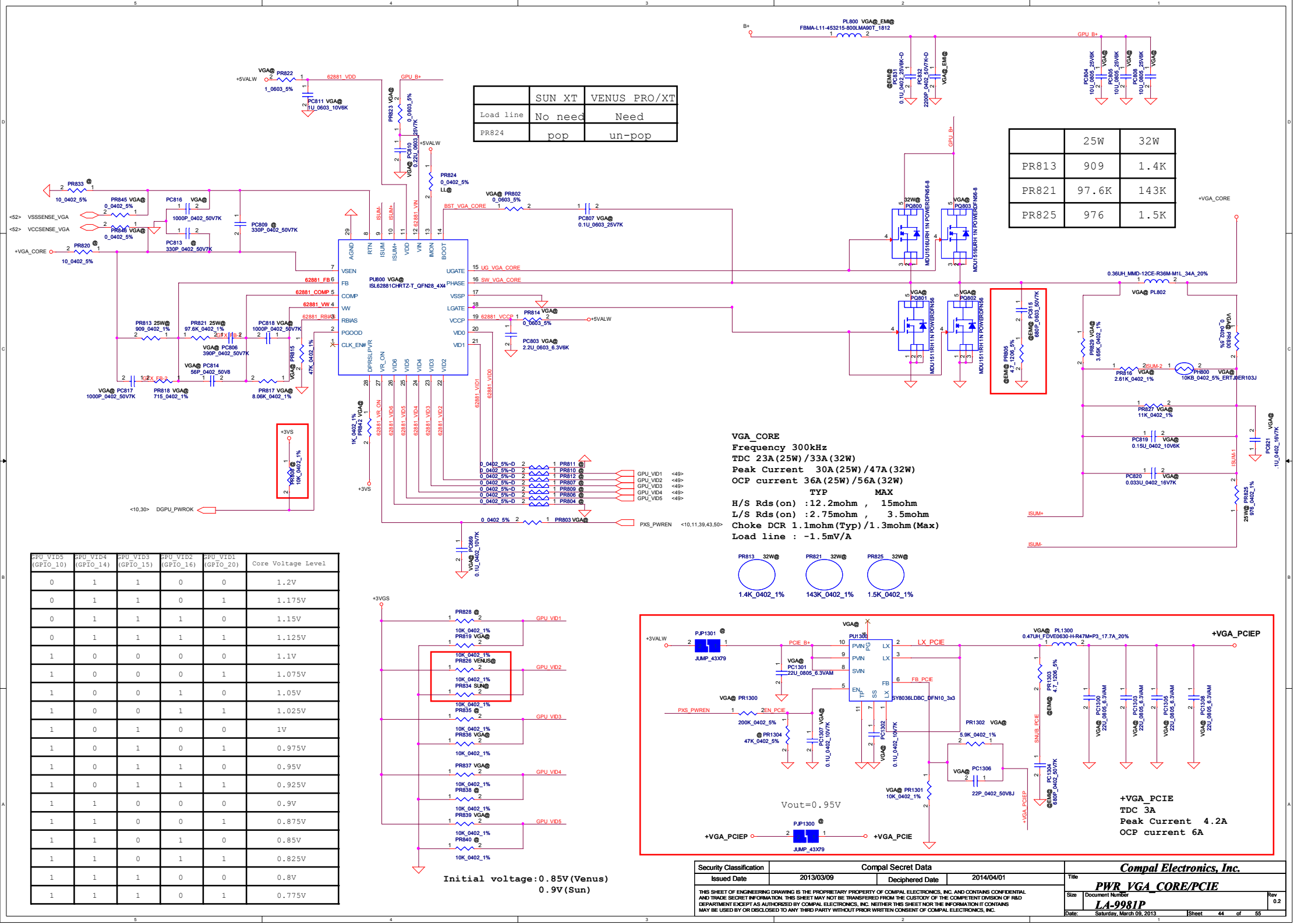
Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: PWR +1.35VGPU/VDDCIP

Size	Document Number	Rev
	LA-9981P	0.2

Date: Saturday, March 09, 2013 Sheet 43 of 55



	SUN XT	VENUS PRO/XT
Load line	No need	Need
PR824	pop	un-pop

	25W	32W
PR813	909	1.4K
PR821	97.6K	143K
PR825	976	1.5K

VGA_CORE
Frequency 300kHz
TDC 23A(25W)/33A(32W)
Peak Current 30A(25W)/47A(32W)
OCP current 36A(25W)/56A(32W)

	TYP	MAX
H/S Rds(on)	:12.2mohm ,	15mohm
L/S Rds(on)	:2.75mohm ,	3.5mohm

Choke DCR 1.1mohm(Typ)/1.3mohm(Max)
Load line : -1.5mV/A

GPU_VID5 (GPIO_10)	GPU_VID4 (GPIO_14)	GPU_VID3 (GPIO_15)	GPU_VID2 (GPIO_16)	GPU_VID1 (GPIO_20)	Core Voltage Level
0	1	1	0	0	1.2V
0	1	1	0	1	1.175V
0	1	1	1	0	1.15V
0	1	1	1	1	1.125V
1	0	0	0	0	1.1V
1	0	0	0	1	1.075V
1	0	0	1	0	1.05V
1	0	0	1	1	1.025V
1	0	1	0	0	1V
1	0	1	0	1	0.975V
1	0	1	1	0	0.95V
1	0	1	1	1	0.925V
1	1	0	0	0	0.9V
1	1	0	0	1	0.875V
1	1	0	1	0	0.85V
1	1	0	1	1	0.825V
1	1	1	0	0	0.8V
1	1	1	0	1	0.775V

Initial voltage:0.85V(Venus)
0.9V(Sun)

+VGA_PCIE
TDC 3A
Peak Current 4.2A
OCP current 6A

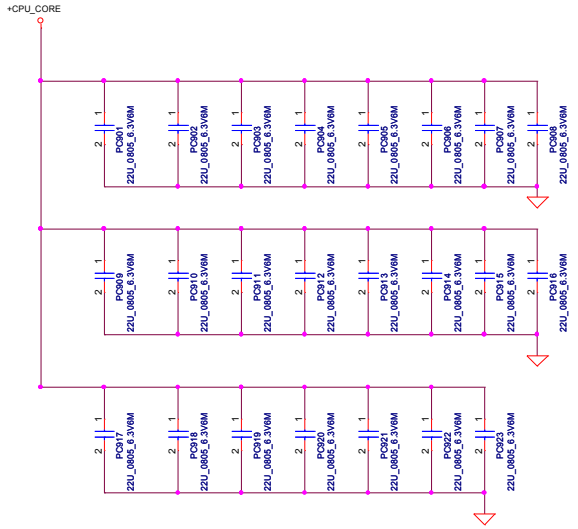
Security Classification	Compal Secret Data
Issued Date	2013/03/09
Deciphered Date	2014/04/01

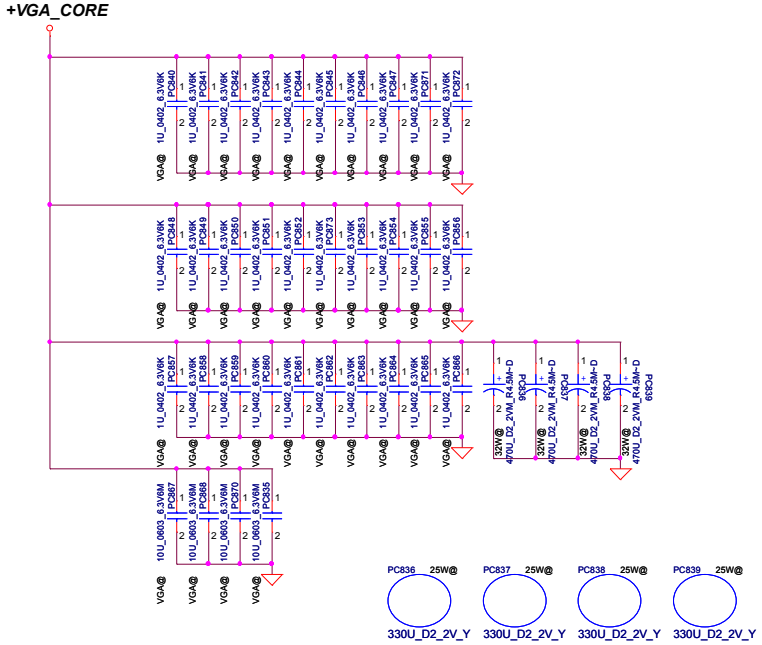
Compal Electronics, Inc.

Title: PWR_VGA_CORE/PCIE

Size: | Document Number: LA-9981P | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 44 of 55





Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

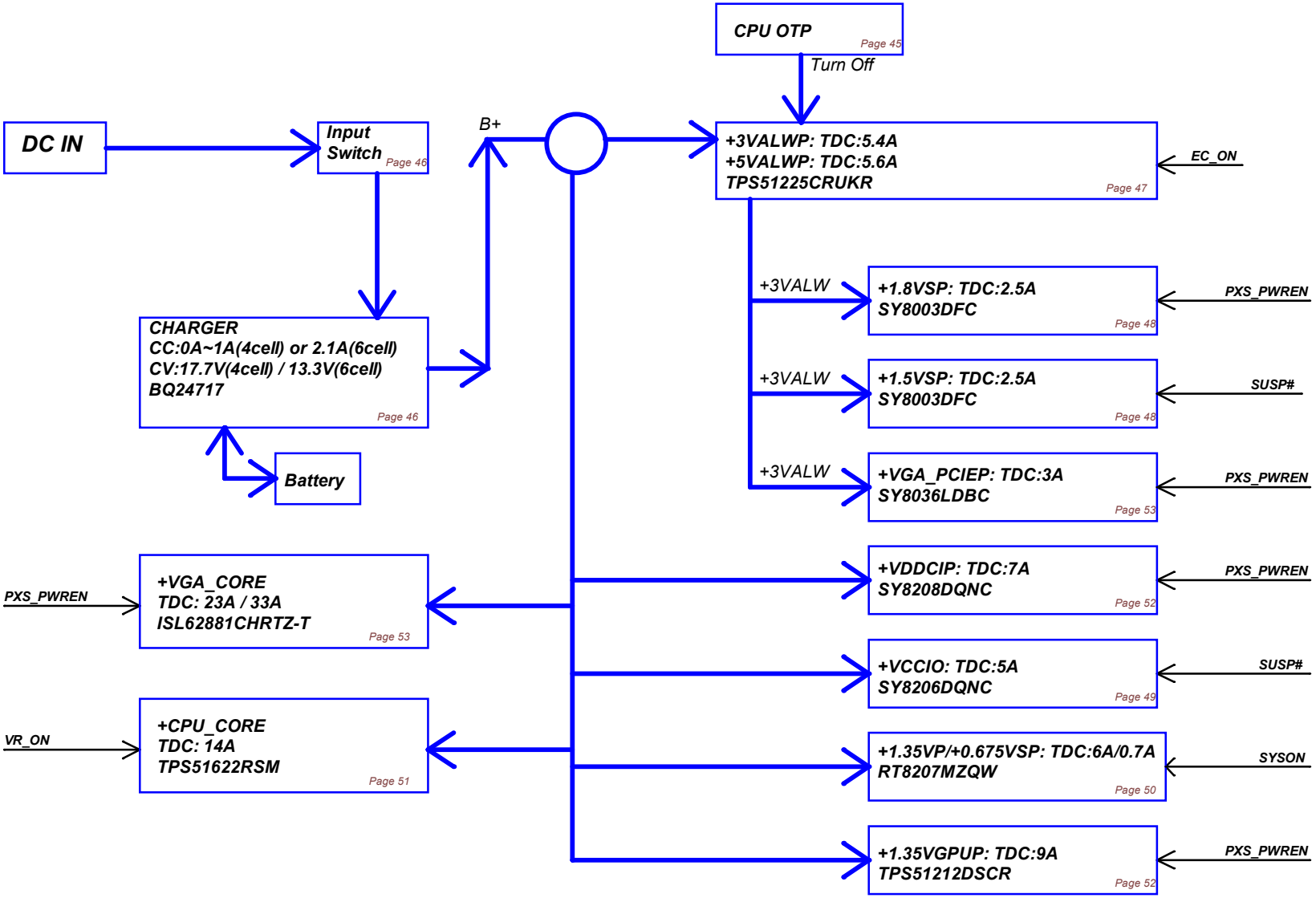
Compal Electronics, Inc.

Title: **PWR_PROCESSOR DECOUPLING**

Size	Document Number	Rev
	LA-9981P	0.2

Date: Saturday, March 09, 2013 | Sheet 45 of 55

Power block



Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: PWR_POWER BLOCK DIAGRAM

Size | Document Number: LA-9981P | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 46 of 55

Version Change List (P. I. R. List) Page 1

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	45	CHARGER	13/01/30	Morris	adjust design parameter from vendor recommend	delete PD702 change PC712 to unpop change PQ704 to unpop change PC707 from 0.1uF_0402 to 1uF_0603 change PC720 from 0.1uF to 100pF change PC711 from 1000pF to 0.01uF change PQ705 from SB00000SD00 to SB00000WY00	0.2
2	50	VCORE	13/01/30	Morris	adjust design parameter from vendor recommend	change PC509 from 0.1uF to 1000pF change PR529 from 3.83K to 5.76K change PR504 from 523K to 499K	0.2
3	44	DCIN/BATT CONN/OTP	13/01/30	Morris	change from ESD request	change PD1 from SC300002E00 to SC300001G00	0.2
4	46	3.3VALWP/5VALWP	13/02/01	Morris	add ESD diode from ESD request	add PD101(SCA00002A00)	0.2
5	50	VCORE	13/02/21	Morris	adjust design parameter from fine tune result	change PR501 from 422K to 523K change PR503 from 56K to 75K	0.2
6	52	VGA_CORE/PCIE	13/02/21	Morris	unpop from EE request	unpop PR808	0.2
7	52	VGA_CORE/PCIE	13/03/05	Morris	adjust output voltage from vender request	unpop PR826 and pop PR834 (only for Sun XT)	0.2

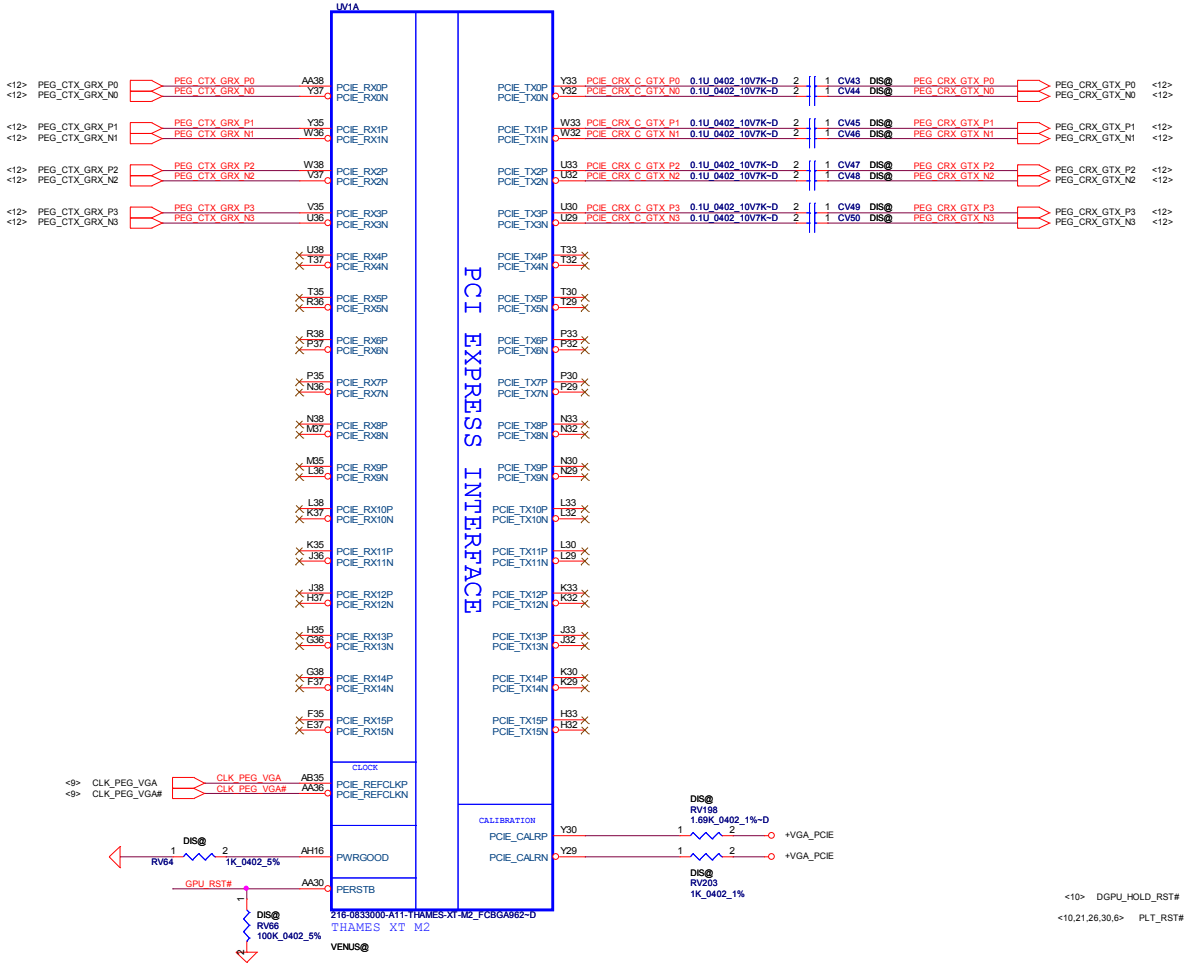
Compal Electronics, Inc.

Title: PWR-PIR

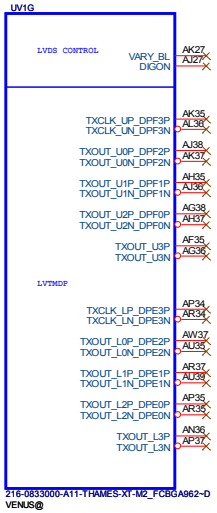
Size | Document Number: LA-9981P | Rev: 0.2

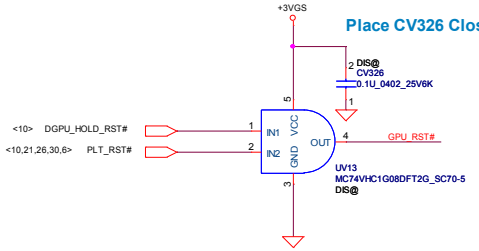
Date: Saturday, March 09, 2013 | Sheet 47 of 55

GFX PCIE LANE REVERSAL



LVDS Interface





Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: ATI_Sun XT_M2_PCIE/LVDS

Size	Document Number	Rev
	LA-9981P	0.2

Date: Saturday, March 09, 2013 Sheet 48 of 55

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING 0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS 0: disable 1: enable	X
RSVD	GPIO2	Advertises PCIE speed when compliance test 0: 2.5GT/s 1: 5GT/s	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0: disable 1: enable	X
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XXX
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD	H2SYNC		0
RSVD	GENERICC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21	H2SYNC	GENERICC	GPIO2	GPIO8

TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50%Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)

SUN GPIO N.C. PIN

GPIO1	GPU_GPIO1
GPIO2	GPU_GPIO2
GPIO7	N.C
GPIO11	GPU_GPIO11
GPIO12	GPU_GPIO12
GPIO13	GPU_GPIO13
GPIO14	N.C
GPIO18	N.C

Vendor	RV241	RV242	Bits [3:1]
★ 128MX16 (1GB) DDR3 H5TC2G63FFR-11C Hynix 2Gb SA00006H40L(R1) SA00006H41L(R3)	NC	4.75K	000
128MX16 (1GB) DDR3 K4W2G1646E-BC11 Samsung 2Gb SA00005SH0L(R1) SA00005SH1L(R3)	8.45K	2K	001
128MX16 (1GB) DDR3 MT41J128M16JT-107G:K Micron 2Gb SA00005XB0L(R1) SA00005XB1L(R3)	4.75K	NC	111

Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: ATI_Sun XT_M2_Main_MSIC

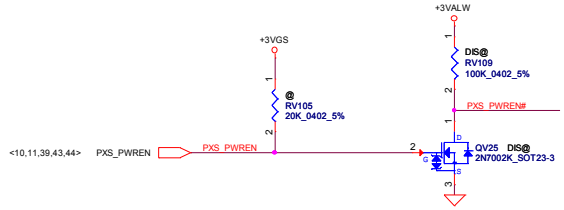
Size: | Document Number: LA-9981P | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 49 of 55

PX_MODE=1 for Normal Operation
PX_MODE=0 for BACO mode to shut down power rails expcept VDDR3,PCIE_VDDC and 1.8V rail

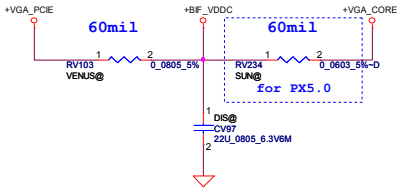
Note:

PX4.0 +VGA_CORE,VDDCI,+1.5VGS ON
PX4.0 +3VGS, +1.0VGS,+1.8VGS OFF
PX5.0 +3VGS,+VGA_CORE,VDDCI,+1.5VGV,+1.0VGS,+1.8VGS OFF

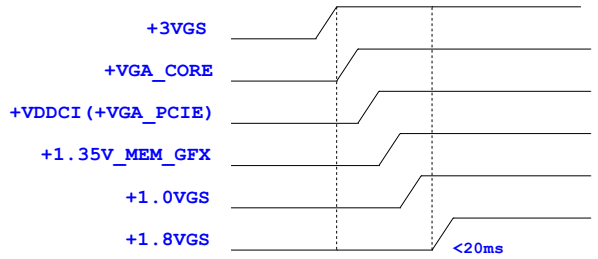


for PX4.0 and PX5.0

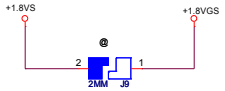
Switch circuits in BACO desingns for Thames/Seymour only 55mA@1.0V, in BACO mode



Power seguence of Sun XT,Venus Pro,Venus XT

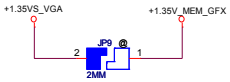


+1.8VS TO +1.8VGS



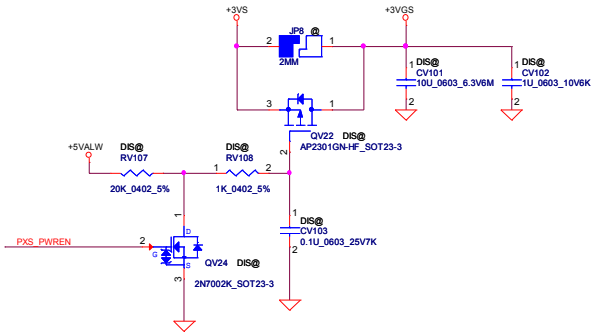
SHORT DEFAULT

+1.35VS_VGA TO +1.35V_MEM_GFX



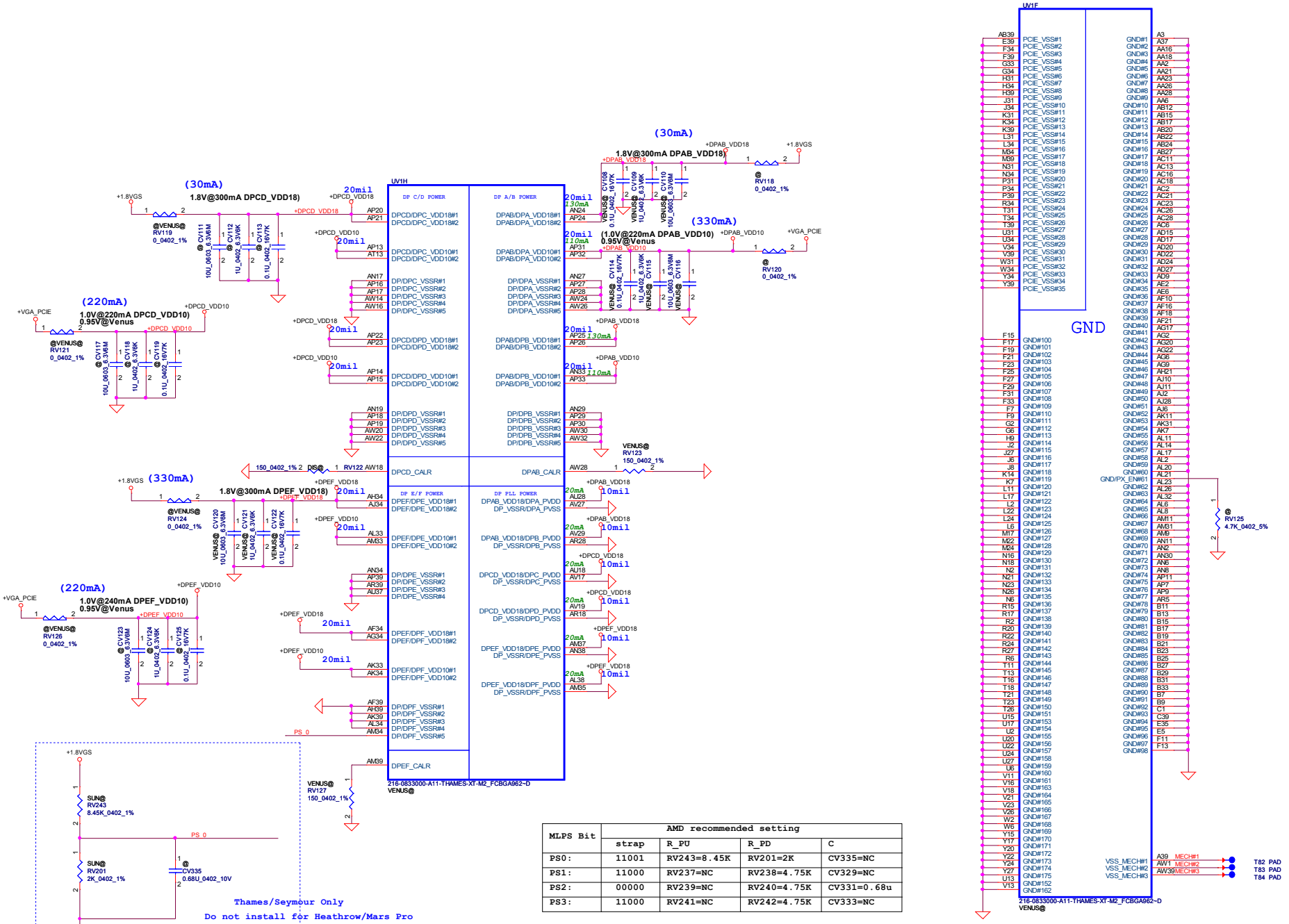
SHORT DEFAULT

+3VS TO +3VGS



Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.	
Title	ATI_Sun XT_M2_BACO POWER
Size	Document Number: LA-9981P
Rev	0.2
Date:	Saturday, March 09, 2013
Sheet	50 of 55



MLPS Bit	AMD recommended setting			
	strap	R_PU	R_PD	C
PS0:	11001	RV243=8.45K	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75K	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75K	CV331=0.68u
PS3:	11000	RV241=NC	RV242=4.75K	CV333=NC

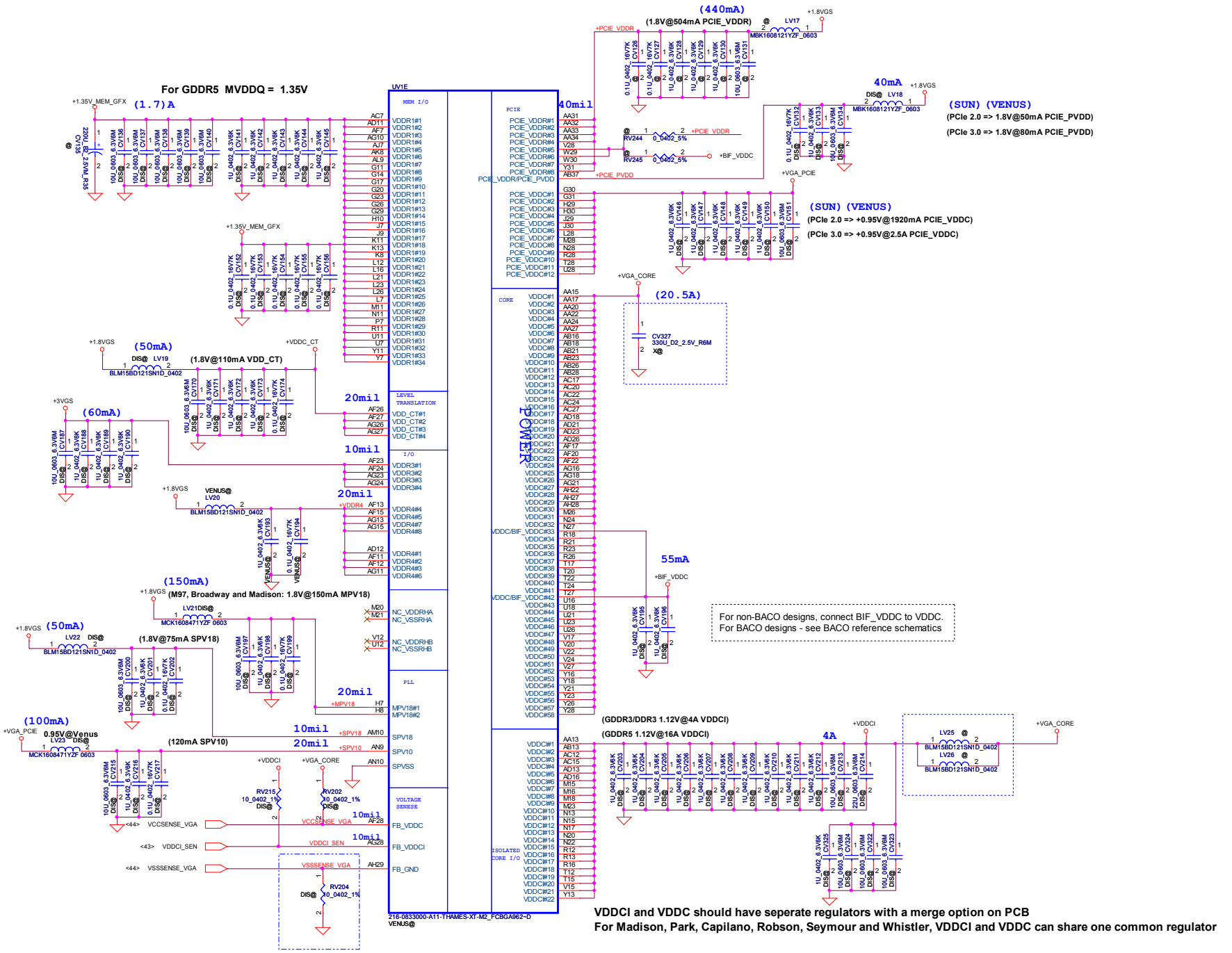
Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: ATI_Sun XT_M2_PWR_GND

Size	Document Number	Rev
	LA-9981P	0.2

Date: Saturday, March 09, 2013 | Sheet 51 of 55



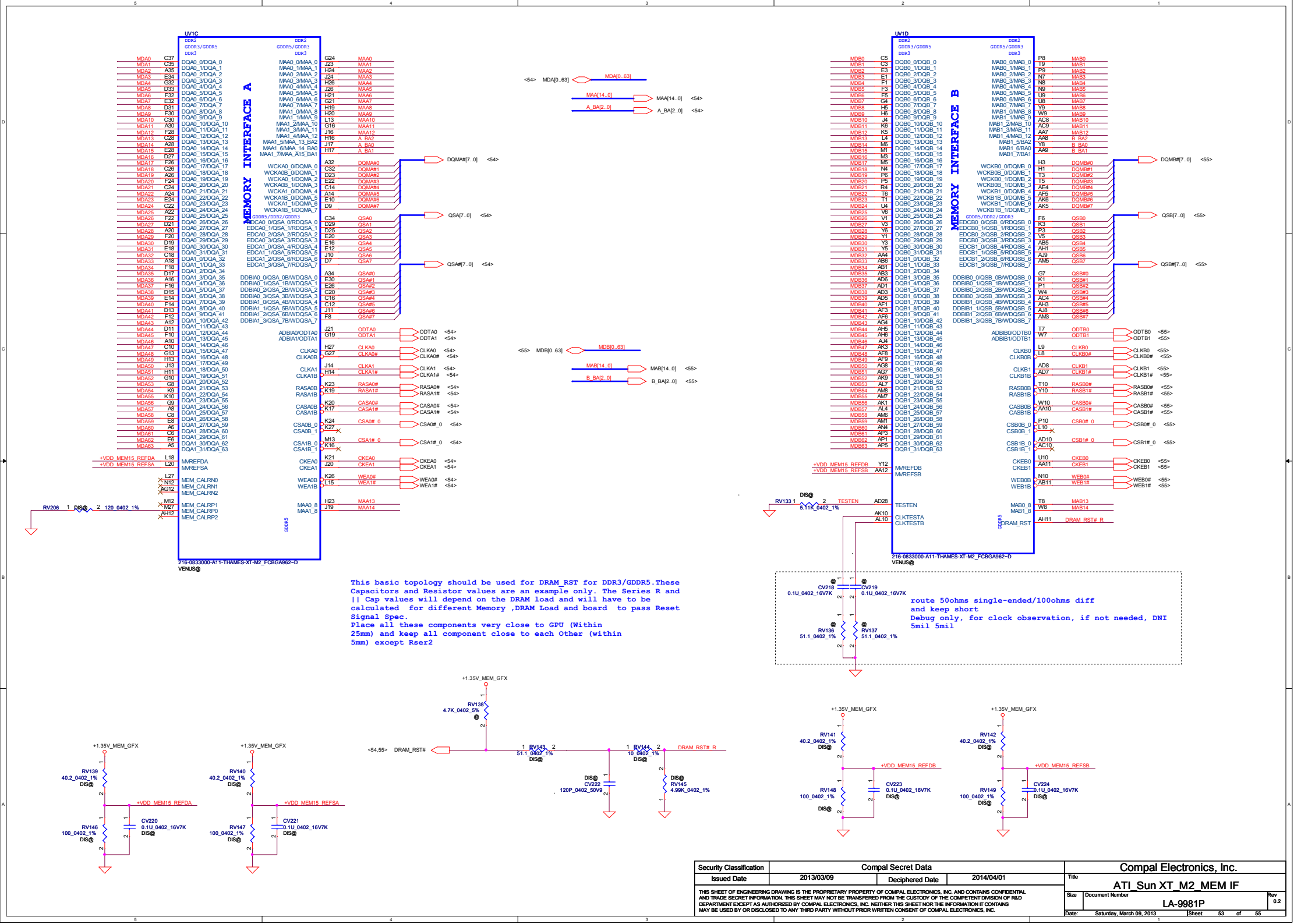
Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: ATI_Sun XT_M2_Power

Size	Document Number	Rev
	LA-9981P	0.2

Date: Saturday, March 09, 2013 Sheet 52 of 55



Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

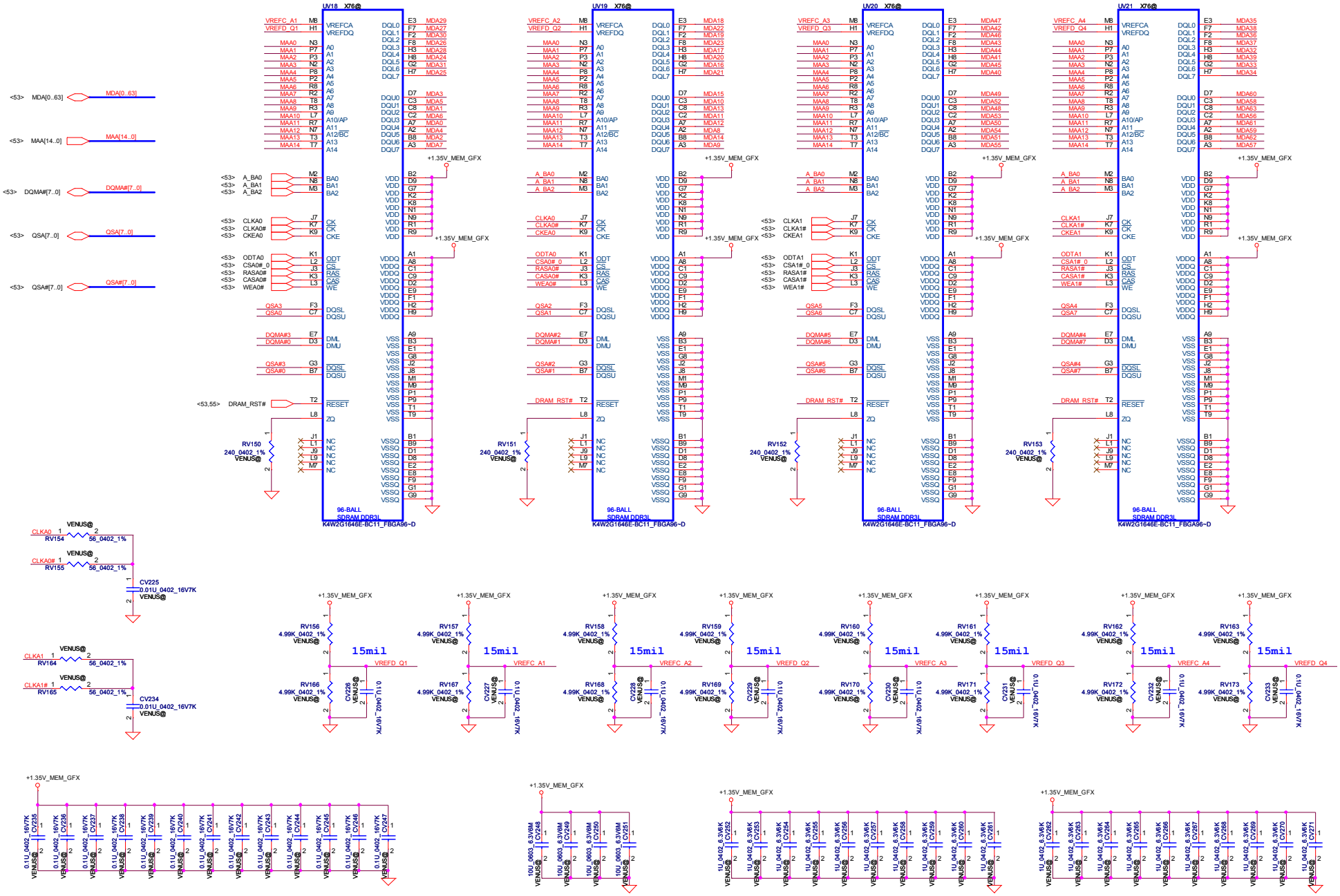
Compal Electronics, Inc.

Title: ATI_Sun XT_M2_MEM IF

Size: | Document Number: LA-9981P | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 53 of 55

CHANNEL A: 256MB DDR3



Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

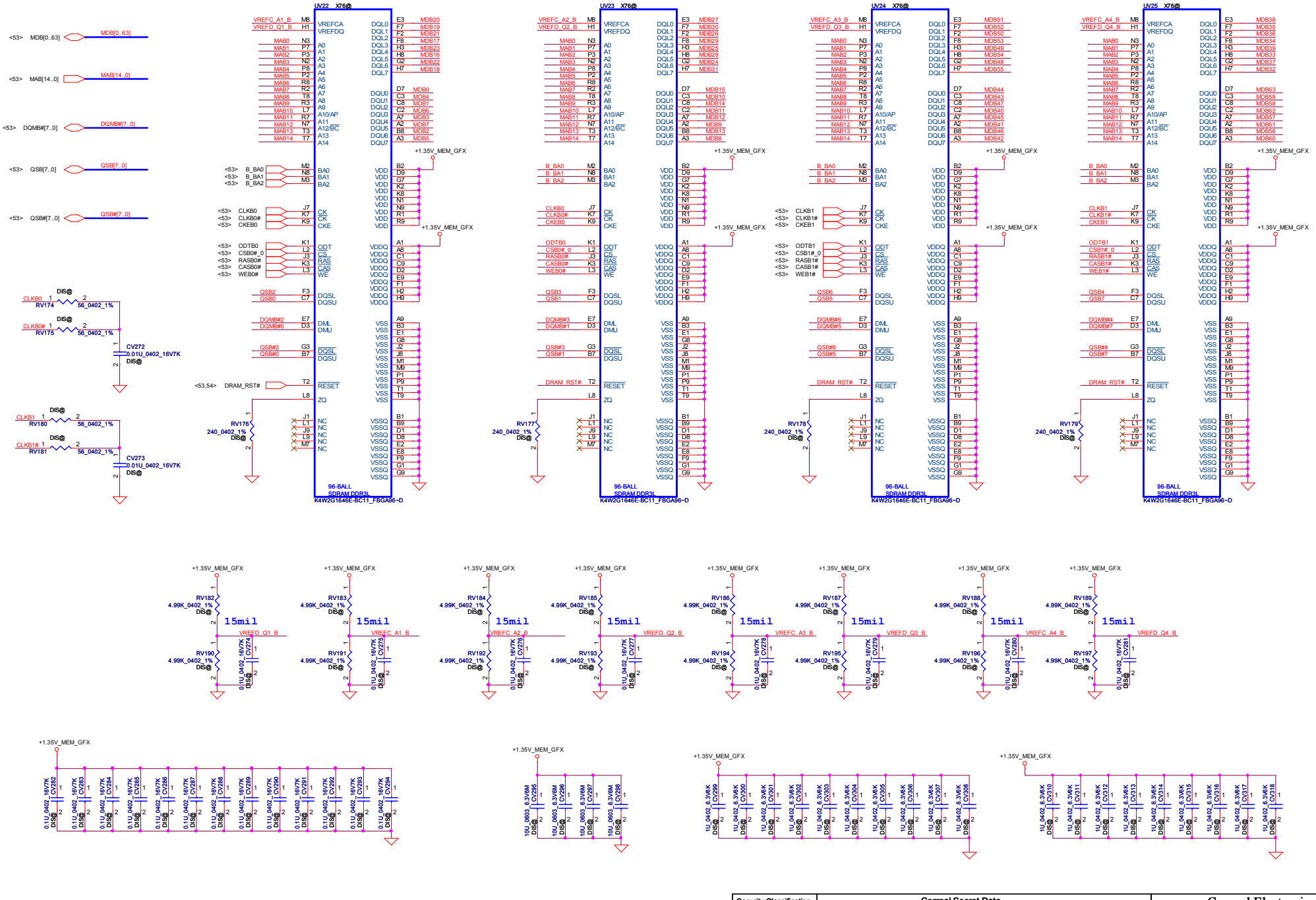
Compal Electronics, Inc.

Title: ATI_Sun XT_M2_VRAM_A

Size: | Document Number: LA-9981P | Rev: 0.2

Date: Saturday, March 09, 2013 | Sheet 54 of 55

CHANNEL B: 256MB DDR3



Security Classification	Compal Secret Data		
Issued Date	2013/03/09	Deciphered Date	2014/04/01

Compal Electronics, Inc.

Title: ATI_Sun XT_M2_VRAM_B

Size	Document Number	Rev
	LA-9981P	0.2

Date: Saturday, March 09, 2013 Sheet 55 of 55