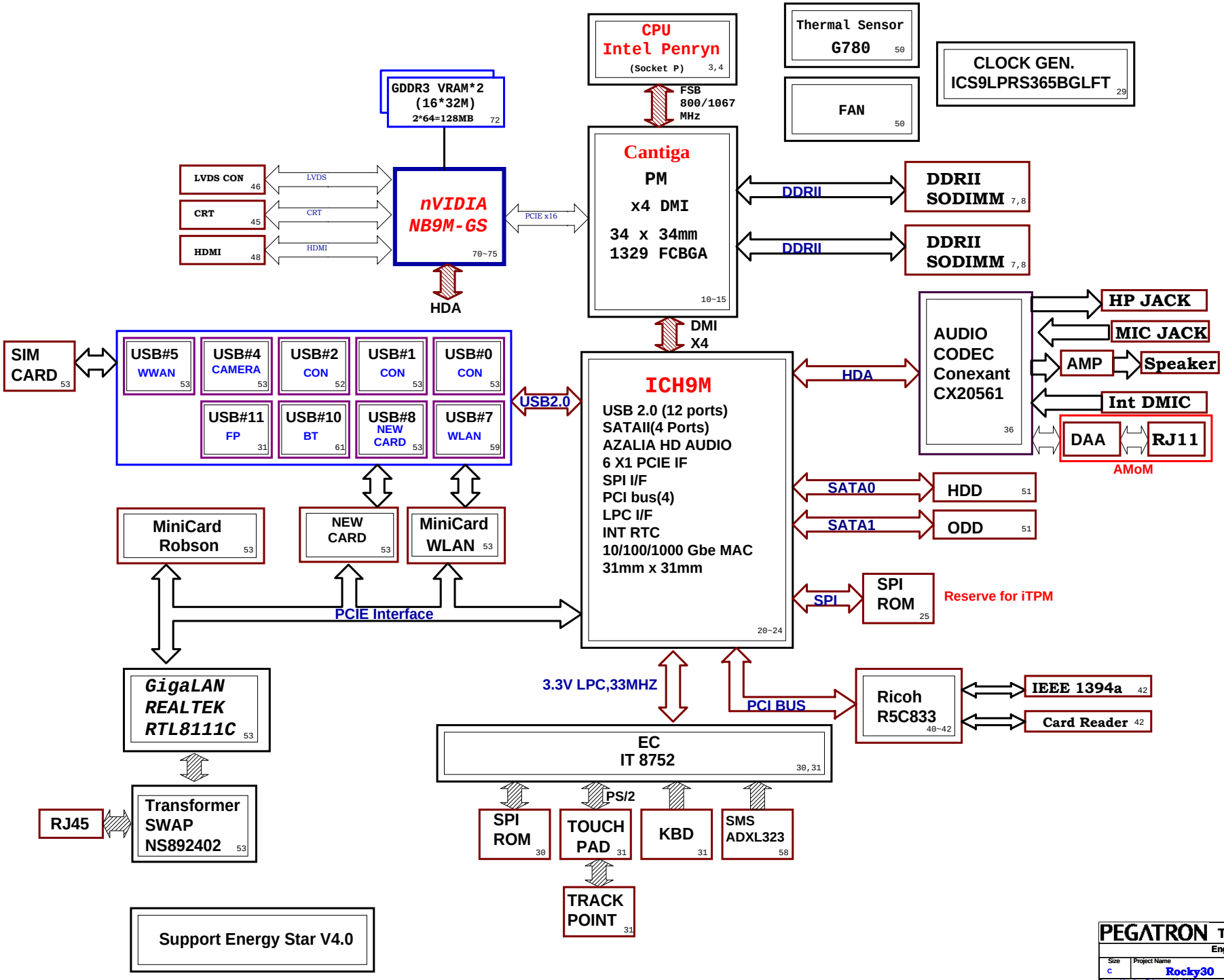
B3 NOTE 13" Block Diagram Discrete VGA
2007/01/30



PEGATRON Title : Block Diagram
Engineer: Peter Lo

Size	Project Name	Rev
C	Rocky30	1.1

Date: Monday, February 04, 2008 Sheet 1 of 94

Rocky30 Schematic Index

Page	System page Ref.
01	Block Diagram
02	Schematic Information
03-05	CPU-Penryn
07-09	DDR2 SO-DIMM
10-15	Cantiga
20-24	ICH9M
25	SPI ROM
29	CLK-ICS9LPR365
30-31	EC_IT8752
32	POWER-ON SEQUENCE
33	*
34	*
35	*
36	AUD_CODEC CX20561
37	AUDIO_AMP-G1431F2U & HP
38	MICROPHONE & LINE-IN-R01
39	*
40	CARDBUS R5C833(PCI I/F)
41	CARDBUS R5C833(1394 & SD)
42	IEEE1394A & CardReader
43	*
44	Debug
45	CRT
46	LVDS & INVERTER CONNECTOR
48	HDMI
50	THER SENSOR & FAN
51	HDD & CDROM
52	USB Port
53	IO Board
54	*
56	LED&PWRSW
57	DISCHARGE
58	SMS
59	MINI CARD-WLAN
60	DC-IN & BATTERY CONN
61	Blue Tooth
62	*
65	MDC NUT & Hinksink NUT
66	*
68	*
70-75	NB9M-GS
79	History
80	POWER_VCORE
81	POWER_SYSTEM
82	POWER_I/O_1.8VS & VCCP
83	POWER_I/O_DDR & VTT
84	PWR_-****
85	PWR_VGA_CORE & +1.1V
86	86_PWR_-****
87	PWR-SHUTDOWN#(Empty)
88	POWER_CHARGER
89	TFT-LCD DRIVE(Empty)
90	POWER_DETECT
91	POWER_LOAD SWITCH
92	POWER_PROTECT
93	POWER_SIGNAL
94	POWER_FLOWCHART

ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	GPI	PM_SYNC#	+3VS
GPIO 01	GPI	-	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#	+3VS
GPIO 06	GPI		+3VS
GPIO 07	GPI		+3VS
GPIO 08	GPI	EXT_SMI#	+3VSUS
GPIO 09	Native	UWB_ON	+3VSUS
GPIO 10	GPI	-	+3VSUS
GPIO 11	Native	EXT_SCI#	+3VSUS
GPIO 12	GPO	-	+3VSUS
GPIO 13	GPI	CB_SD#	+3VSUS
GPIO 14	GPI	RTLAN_DSM#	+3VSUS
GPIO 15	Native	-	+3VSUS
GPIO 16	Native	PM_DPRSLPVR	+3VS
GPIO 17	GPI	WLAN_LED	+3VS
GPIO 18	GPO	-	+3VS
GPIO 19	GPI	-	+3VS
GPIO 20	GPO	-	+3VS
GPIO 21	GPI	-	+3VS
GPIO 22	GPI	BT_DET#	+3VS
GPIO 23	Native	-	+3VS
GPIO 24	GPO	WLAN_ON	+3VSUS
GPIO 25	Native	-	+3VSUS
GPIO 26	Native	-	+3VSUS
GPIO 27	GPO	BT_ON	+3VSUS
GPIO 28	GPO	-	+3VSUS
GPIO 29	Native	USB_OC5#	+3VSUS
GPIO 30	Native	USB_OC6#	+3VSUS
GPIO 31	Native	USB_OC7#	+3VSUS
GPIO 32	GPO	-	+3VS
GPIO 33	GPO	-	+3VS
GPIO 34	GPO	-	+3VS
GPIO 35	GPO	CLK_SATA_REQ#	+3VS
GPIO 36	GPI	-	+3VS
GPIO 37	GPI	PCB_ID0	+3VS
GPIO 38	GPI	PCB_ID1	+3VS
GPIO 39	GPI	PCB_ID2	+3VS
GPIO 40	Native	USB_OC1#	+3VSUS
GPIO 41	Native	USB_OC2#	+3VSUS
GPIO 42	Native	USB_OC3#	+3VSUS
GPIO 43	Native	USB_OC4#	+3VSUS
GPIO 44	Native	USB_OC8#	N/A
GPIO 45	Native	USB_OC9#	N/A
GPIO 46	Native	USB_OC10#	N/A
GPIO 47	Native	USB_OC11#	N/A
GPIO 48	GPI	-	+3VS
GPIO 49	GPO	GPU_RST#	+3VS
GPIO 50	Native	PCI_REQ#1	+3VS
GPIO 51	Native	-	+3VS
GPIO 52	Native	PCI_REQ#2	+3VS
GPIO 53	Native	-	+3VS
GPIO 54	Native	PCI_REQ#3	+3VS
GPIO 55	Native	-	+3VS
GPIO 56	GPI	-	+3VSUS
GPIO 57	GPI	-	+3VSUS
GPIO 58	GPI	-	+3VSUS
GPIO 59	Native	USB_OC0#	+3VSUS
GPIO 60	Native	RTLAN_DSM_EN	+3VSUS

EC GPIO	Use As	Signal Name	Power
GPA0	GPO	PWR_LED#	
GPA1	GPO	CHG_LED#	
GPA2	GPO	BATSEL_3S#	
GPA3	-	NOVO_CARE_LED#	
GPA4	GPO	LCD_BL_PWM	
GPA5	GPO	FAN_PWM	
GPA6	GPO	-	
GPA7	GPO	-	
GPB0	GPO	CHG_EN#	
GPB1	GPO	PRECHG	
GPB2	GPI	-	
GPB3	ALT	SMB0_CLK	
GPB4	ALT	SMB0_DAT	
GPB5	OD	A20GATE	
GPB6	OD	RCIN#	
GPB7	GPO	PM_RSMRST#	
GPC0	GPI	-	
GPC1	ALT	SMB1_CLK	
GPC2	ALT	SMB1_DAT	
GPC3	GPO	PM_PWRBTN#	
GPC4	ALT	AC_IN_OC#	
GPC5	GPO	OP_SD#	
GPC6	ALT	BAT1_IN_OC#	
GPC7	GPO	RFON_SW#	
GPD0	GPI	PWRLIMIT#	
GPD1	ALT	PM_SUSC#	
GPD2	ALT	BUF_PLT_RST#	
GPD3	OD	EXT_SCI#	
GPD4	OD	EXT_SMI#	
GPD5	GPO	LCD_BACKOFF#	
GPD6	ALT	FAN0_TACH	
GPD7	GPI	-	
GPE0	GPO	VSUS_ON	
GPE1	GPO	SUSC_EC#	
GPE2	GPO	SUSB_EC#	
GPE3	GPO	CPU_VRON	
GPE4	ALT	PWR_SW#	
GPE5	ALT	-	
GPE6	GPI	LID_SW#	
GPE7	GPO	MEDIA_KEY#	
GPF0	GPI	-	
GPF1	GPI	NOVO_CARE#	
GPF2	ALT	TP1_CLK	
GPF3	ALT	TP1_DAT	
GPF4	ALT	TP_CLK	
GPF5	ALT	TP_DAT	
GPF6	GPO	THRO_CPU	
GPF7	GPO	SUSPEND_LED#	
GPG0	GPI	PM_THERM#_EC	
GPG1	ALT	PM_SUSB#	
GPG2	GPO	BAT1_CNT2#	
-	-	-	
-	-	-	

EC GPIO	Use As	Signal Name	Power
-	-	-	
GPG6	GPO	-	
-	-	-	
GPH0	OD	PM_CLKRUN#	
GPH1	ALT	3G_ON#	
GPH2	ALT	LOGO_LED#	
GPH3	GPO	BAT_LEARN	
GPH4	GPO	-	
GPH5	GPO	NUM_LED#	
GPH6	GPO	CAP_LED#	
-	-	-	
GPI0	GPI	NV_OVERT#	
GPI1	GPI	SUS_PWRGD	
GPI2	GPI	ALL_SYSTEM_PWRGD	
GPI3	GPI	VRM_PWRGD	
GPI4	GPI	XOUT	
GPI5	GPI	YOUT	
GPI6	GPI	-	
GPI7	GPI	-	
GPJ0	GPO	EC_CLK_EN	
GPJ1	GPO	PM_PWROK	
GPJ2	GPI	-	
GPJ3	-	-	
GPJ4	GPO	BL_DA	
GPJ5	GPO	-	
GPK0	GPI	-	
GPK1	GPI	-	
GPK2	GPI	-	
GPK3	GPI	-	
GPK4	GPI	-	
GPK5	GPI	-	
GPL0	GPI	APS_PWR_CNT#	
GPL1	GPI	APS_ST#	
GPL2	GPO	USB_PWR_EN#	
GPL3	GPO	-	
GPL4	GPO	-	
GPL5	GPO	AC_ID	
GPL6	GPO	AC_65W	
GPL7	GPO	CHG_LOW_LED#	
GPK6	GPO	-	
GPK7	GPI	-	

PEGATRON Title : Schematic Information

Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.1

Date: Saturday, January 26, 2008 Sheet 2 of 94

10 H_D#[63:0] H_D#[63:0]

10 H_A#[35:3] H_A#[35:3]

10 H_REQ#[4:0] H_REQ#[4:0]

Reserved for the S3 reboot issue.

H_CPURST# — @ C0302 10PF/50V

R1.1

U0301A

ADDR GROUP 0: H_A#3 J4, H_A#4 L5, H_A#5 L4, H_A#6 K5, H_A#7 M3, H_A#8 N2, H_A#9 J1, H_A#10 N3, H_A#11 P5, H_A#12 P2, H_A#13 L2, H_A#14 P4, H_A#15 P1, H_A#16 R1, 10 H_ADSTB#0 M1

ADDR GROUP 1: H_A#17 Y2, H_A#18 U5, H_A#19 R3, H_A#20 W6, H_A#21 U4, H_A#22 Y5, H_A#23 U1, H_A#24 R4, H_A#25 T5, H_A#26 T3, H_A#27 W2, H_A#28 W5, H_A#29 Y4, H_A#30 U2, H_A#31 V4, H_A#32 W3, H_A#33 AA4, H_A#34 AB2, H_A#35 AA3, 10 H_ADSTB#1 V1

REQ: H_REQ#0 K3, H_REQ#1 H2, H_REQ#2 K2, H_REQ#3 J3, H_REQ#4 L1

CONTROL: ADS# H1 — H_ADS# 10; BNR# E2 — H_BNR# 10; BPRI# G5 — H_BPRI# 10; DEFER# H5 — H_DEFER# 10; DRDY# F21 — H_DRDY# 10; DBSY# E1 — H_DBSY# 10; BR0# F1 — H_BR0# 10; IERR# D20 — H_IERR# — R0309 1 2 56Ohm — +VCCP_CPU; INIT# B3 — H_INIT# 20; LOCK# H4 — H_LOCK# 10; RESET# C1 — H_CPURST# 10; RS[0]# F3 — H_RS#0 10; RS[1]# F4 — H_RS#1 10; RS[2]# G3 — H_RS#2 10; TRDY# G2 — H_TRDY# 10; HIT# G6 — H_HIT# 10; HITM# E4 — H_HITM# 10

T0318, T0319

T0352

Place Series Resistor on H_CPURST# Without Stub

XDP/ITP SIGNALS: BPM[0]# AD4 — T0330; BPM[1]# AD3 — XDP_BPM#1; BPM[2]# AD1 — T0331; BPM[3]# AC4 — T0332; PRDY# AC2 — T0333; PREQ# AC1 — H_PREQ#; TCK AC5 — H_TCK; TDI AA6 — H_TDI; TDO AB3 — H_TDO; TMS AB5 — H_TMS; TRST# AB6 — H_TRST#; DBR# C20 — H_DBR#

THERMAL: PROCHOT# D21 — H_PROCHOT_S# — To Thermal sensor page; THRMDA A24 — CPU_THRM_DA 50; THRMDC B25 — CPU_THRM_DC 50; THERMTRIP# C7 — H_THRMTRIP# 5,11,20,31

H CLK: BCLK[0] A22 — CLK_CPU_BCLK 29; BCLK[1] A21 — CLK_CPU_BCLK# 29 — T0302, T0303

RESERVED: RSVD1 T2, RSVD2 V3, RSVD3 B2, RSVD4 C3, RSVD5 D2, RSVD6 D22, RSVD7 D3, RSVD8 E6, RSVD9 M4, RSVD10 N5

T0308 T0309 T0310 T0311 T0312 T0313 T0314 T0315 T0316 T0317

SOCKET478BR

+VCCP_CPU

R0315 1KOhm 1%

R0316 2KOhm 1%

C0301 0.1UF/10V @

GTL_REF: R0317 @ 1% 1KOhm; R0318 @ 1% 1KOhm

T0304 T0305 T0306 T0307

Zo=55 ohm, 0.5" max for GTLREF

U0301B

DATA GRP 0: D[0]# E22, D[1]# F24, D[2]# E26, D[3]# G22, D[4]# E23, D[5]# G25, D[6]# E25, D[7]# E23, D[8]# K24, D[9]# G24, D[10]# J24, D[11]# J23, D[12]# H22, D[13]# F26, D[14]# K22, D[15]# H23

DATA GRP 1: D[16]# N22, D[17]# K25, D[18]# P26, D[19]# R23, D[20]# L23, D[21]# M24, D[22]# L22, D[23]# M23, D[24]# P25, D[25]# P23, D[26]# P22, D[27]# T24, D[28]# R24, D[29]# L25, D[30]# T25, D[31]# N25

DATA GRP 2: D[32]# Y22, D[33]# AB24, D[34]# V24, D[35]# V26, D[36]# V23, D[37]# T22, D[38]# U25, D[39]# U23, D[40]# Y25, D[41]# W22, D[42]# Y23, D[43]# W24, D[44]# W25, D[45]# AA23, D[46]# AA24, D[47]# AB25

DATA GRP 3: D[48]# AE24, D[49]# AD24, D[50]# AA21, D[51]# AB22, D[52]# AB21, D[53]# AC26, D[54]# AD20, D[55]# AE22, D[56]# AF23, D[57]# AC25, D[58]# AE21, D[59]# AD21, D[60]# AC22, D[61]# AD23, D[62]# AF22, D[63]# AC23

DSTBN[0]# J26 — 10 H_DSTBN#0; DSTBP[0]# H26 — 10 H_DSTBP#0; DINV[0]# H25 — 10 H_DINV#0

DSTBN[1]# L26 — 10 H_DSTBN#1; DSTBP[1]# M26 — 10 H_DSTBP#1; DINV[1]# N24 — 10 H_DINV#1

DSTBN[2]# Y26 — H_DSTBN#2 10; DSTBP[2]# AA26 — H_DSTBP#2 10; DINV[2]# U22 — H_DINV#2 10

DSTBN[3]# AE25 — H_DSTBN#3 10; DSTBP[3]# AF24 — H_DSTBP#3 10; DINV[3]# AC20 — H_DINV#3 10

MISC: GTLREF AD26, TEST1 C23, TEST2 D25, TEST3 C24, TEST4 AF26, TEST5 AF1, TEST6 A26

BSEL[0] B22 — 29 CPU_BSEL0; BSEL[1] B23 — 29 CPU_BSEL1; BSEL[2] C21 — 29 CPU_BSEL2

COMP[0] R26 — H_COMP0 — R0311 1 2 27.4Ohm 1%; COMP[1] U26 — H_COMP1 — R0312 1 2 54.9Ohm 1%; COMP[2] AA1 — H_COMP2 — R0313 1 2 27.4Ohm 1%; COMP[3] Y1 — H_COMP3 — R0314 1 2 54.9Ohm 1%

DPRSTP# E5 — H_DPRSTP# 11,20,80; DPSLP# B5 — H_DPSLP# 20; DPWR# D24 — H_DPWR# 10; PWRGOOD D6; SLP# D7 — H_CPUSLP# 10; PSI# AE6 — PM_PSI# 80

H_PWRGD 20

Place Series Resistor on H_PWRGD Without Stub

R0319 2 1 200Ohm @ — +VCCP_CPU

SOCKET478BR

Comp0,2 connect with Zo=27.4 ohm, make trace length shorter than 0.5". Comp 1,3 connect with Z0=55 ohm, make trace length shorter than 0.5".

BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1067	L	L	L

Default Strapping When Not Used

+VCCP_CPU

XDP_BPM#1 R0301 1 2 54.9Ohm 1% @

H_PREQ# R0302 1 2 54.9Ohm 1%

H_TDI R0303 1 2 54.9Ohm 1%

H_TDO R0304 1 2 54.9Ohm 1% @

H_TMS R0305 1 2 54.9Ohm 1%

H_DBR# R0306 1 2 1KOhm 1% @ — +3VS

H_TCK R0307 1 2 54.9Ohm 1%

H_TRST# R0308 1 2 54.9Ohm 1%

Place R0304 & R0306 for XDP function

+VCCP_CPU

R0310 68Ohm

H_PROCHOT_S#

30,88 PWRLIMIT# — D0301 RB751V-40 @

Q0301 2N7002E-T1-E3

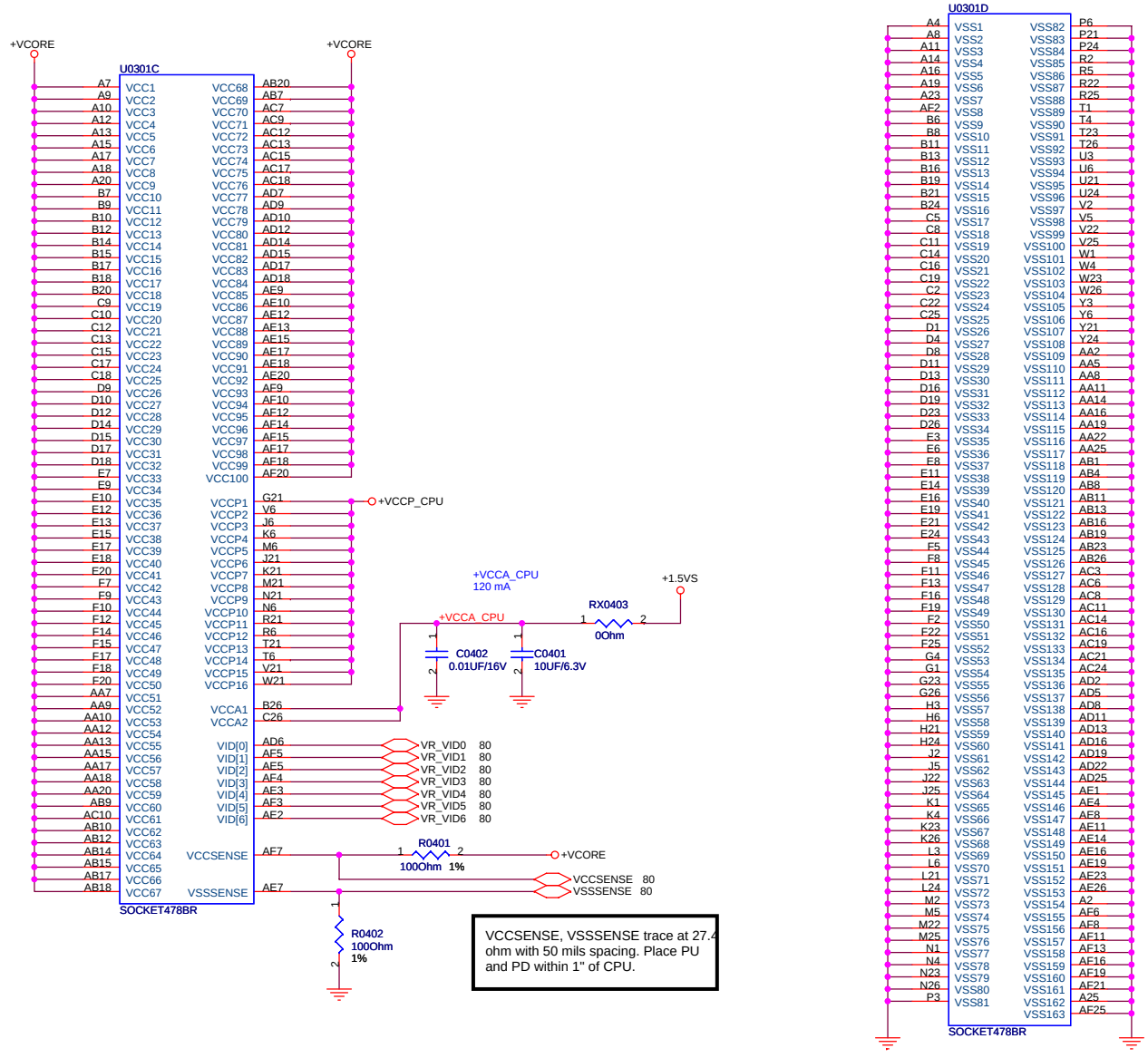
G — THRO_CPU 30

PEGATRON Title : Penryn CPU (1)

Engineer: Peter Lo

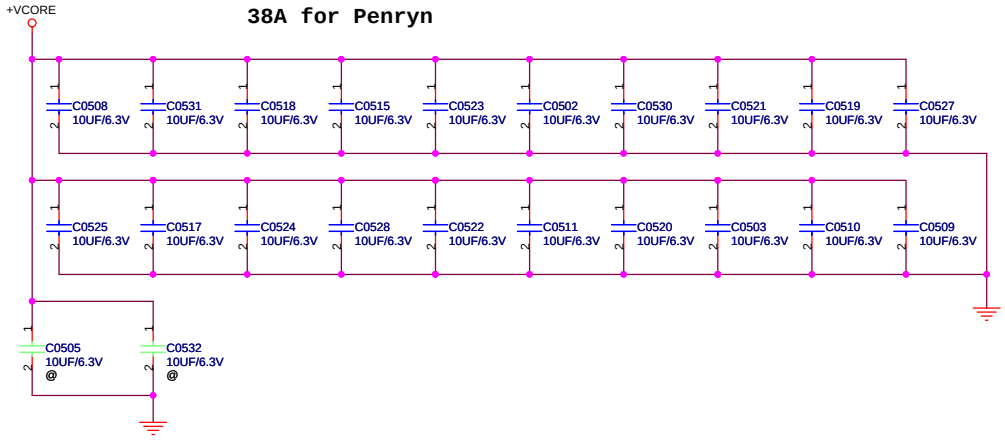
Size	Project Name	Rev
Custom	Rocky30	1.1

Date: Monday, February 04, 2008 Sheet 3 of 94

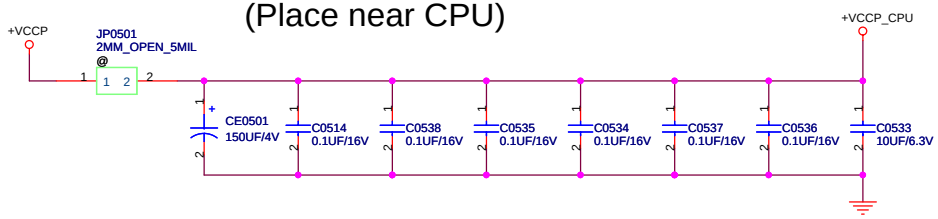


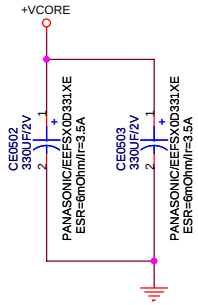
PEGATRON	Title : Penryn CPU (2)	
	Engineer: Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.1
Date: Monday, February 04, 2008	Sheet 4 of 94	

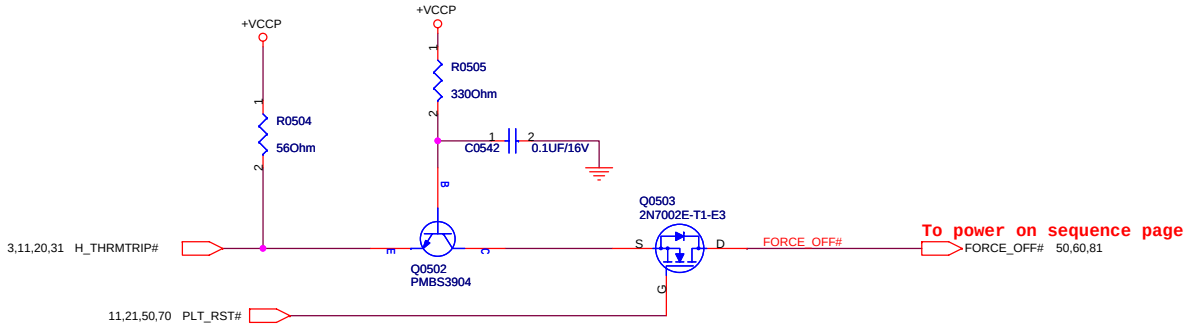
38A for Penryn



+VCCP Decoupling Capacitor (Place near CPU)







Thermal Trip signal(From CPU to ICH-9M and sequence)

PEGATRON	Title : CPU CAPS	
	Engineer: Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.1
Date: Monday, February 04, 2008	Sheet 5 of 94	

PEGATRON	Title :
	Engineer: Peter Lo
Size: A	Project Name: Rocky30
Rev: 1.1	
Date: Saturday, January 26, 2008	Sheet 6 of 94

+3VS → +3VS 3,8,11,14,15,20,22,23,24,25,29,30,31,40,41,45,46,48,50,51,53,54,57,58,59,61,70,74,75,91,92

+1.8V → +1.8V 8,9,11,13,83,91

M_VREF_MCH → M_VREF_MCH 8,9,11

SMBus Slave Address:A0H

temp_5886_tl01
(12G025M22000LVwith 12G025C2200WLV
co-lay symbol)

SMBus Slave Address: A0H

9,12 M_A_A[0..14]

M_A_DQ[0..63] 12

J0701A

M_A_A0	102	A0	DQ0	5	M_A_DQ11
M_A_A1	101	A1	DQ1	7	M_A_DQ14
M_A_A2	100	A2	DQ2	17	M_A_DQ10
M_A_A3	99	A3	DQ3	19	M_A_DQ15
M_A_A4	98	A4	DQ4	4	M_A_DQ9
M_A_A5	97	A5	DQ5	6	M_A_DQ8
M_A_A6	94	A6	DQ6	14	M_A_DQ13
M_A_A7	92	A7	DQ7	16	M_A_DQ12
M_A_A8	93	A8	DQ8	23	M_A_DQ18
M_A_A9	91	A9	DQ9	25	M_A_DQ22
M_A_A10	105	A10/AP	DQ10	35	M_A_DQ23
M_A_A11	90	A11	DQ11	37	M_A_DQ16
M_A_A12	89	A12	DQ12	20	M_A_DQ17
M_A_A13	116	A13	DQ13	22	M_A_DQ20
M_A_A14	86	A14	DQ14	36	M_A_DQ19
	84	A15	DQ15	38	M_A_DQ21
9,12 M_A_BS2	85	A16_BA2	DQ16	43	M_A_DQ31
			DQ17	45	M_A_DQ30
9,12 M_A_BS0	107	BA0	DQ18	55	M_A_DQ27
9,12 M_A_BS1	106	BA1	DQ19	57	M_A_DQ26
9,11 M_CS#0	110	S0#	DQ20	44	M_A_DQ29
9,11 M_CS#1	115	S1#	DQ21	46	M_A_DQ25
11 M_CLK_DDR0	30	CK0	DQ22	56	M_A_DQ24
11 M_CLK_DDR#0	32	CK0#	DQ23	58	M_A_DQ28
11 M_CLK_DDR1	164	CK1	DQ24	61	M_A_DQ0
11 M_CLK_DDR#1	166	CK1#	DQ25	63	M_A_DQ3
9,11 M_CKE0	79	CKE0	DQ26	73	M_A_DQ1
9,11 M_CKE1	80	CKE1	DQ27	75	M_A_DQ5
9,12 M_A_CAS#	113	CAS#	DQ28	62	M_A_DQ7
9,12 M_A_RAS#	108	RAS#	DQ29	64	M_A_DQ6
9,12 M_A_WE#	109	WE#	DQ30	74	M_A_DQ2
M_A_SA0	198	SA0	DQ31	76	M_A_DQ4
M_A_SA1	200	SA1	DQ32	123	M_A_DQ51
8,24,25,29 SMB_CLK_M	197	SCL	DQ33	125	M_A_DQ54
8,24,25,29 SMB_DAT_M	195	SDA	DQ34	135	M_A_DQ50
			DQ35	137	M_A_DQ55
9,11 M_ODT0	114	ODT0	DQ36	124	M_A_DQ49
9,11 M_ODT1	119	ODT1	DQ37	126	M_A_DQ48
			DQ38	134	M_A_DQ52
12 M_A_DM[0..7]			DQ39	136	M_A_DQ53
M_A_DM1	10	DM0	DQ40	141	M_A_DQ35
M_A_DM2	26	DM1	DQ41	143	M_A_DQ34
M_A_DM3	52	DM2	DQ42	151	M_A_DQ39
M_A_DM0	67	DM3	DQ43	153	M_A_DQ38
M_A_DM6	130	DM4	DQ44	140	M_A_DQ33
M_A_DM4	147	DM5	DQ45	142	M_A_DQ36
M_A_DM5	170	DM6	DQ46	152	M_A_DQ37
M_A_DM7	185	DM7	DQ47	154	M_A_DQ32
			DQ48	157	M_A_DQ47
12 M_A_DQS[0..7]			DQ49	159	M_A_DQ41
M_A_DQS1	13	DQS0	DQ50	173	M_A_DQ43
M_A_DQS2	31	DQS1	DQ51	175	M_A_DQ42
M_A_DQS3	51	DQS2	DQ52	158	M_A_DQ45
M_A_DQS0	70	DQS3	DQ53	160	M_A_DQ44
M_A_DQS6	131	DQS4	DQ54	174	M_A_DQ40
M_A_DQS4	148	DQS5	DQ55	176	M_A_DQ46
M_A_DQS5	169	DQS6	DQ56	179	M_A_DQ63
M_A_DQS7	188	DQS7	DQ57	181	M_A_DQ56
M_A_DQS#1	11	DQS#0	DQ58	189	M_A_DQ62
M_A_DQS#2	29	DQS#1	DQ59	191	M_A_DQ58
M_A_DQS#3	49	DQS#2	DQ60	180	M_A_DQ60
M_A_DQS#0	68	DQS#3	DQ61	182	M_A_DQ61
M_A_DQS#6	129	DQS#4	DQ62	192	M_A_DQ59
M_A_DQS#4	146	DQS#5	DQ63	194	M_A_DQ57
M_A_DQS#5	167	DQS#6			
M_A_DQS#7	186	DQS#7			

DDR2_DIMM_200P

M_CLK_DDR0 — C0701 10PF/50V @ — M_CLK_DDR#0

M_CLK_DDR1 — C0702 10PF/50V @ — M_CLK_DDR#1

Place near SO-DIMM_0

R0703 10KOhm

R0704 10KOhm

Layout Note: Place these caps near SO DIMM 0

Layout Note: Place these caps near SO DIMM 0

+1.8V — C0703 0.1UF/10V — C0704 0.1UF/10V — C0705 0.1UF/10V — C0706 0.1UF/10V

+3VS — C0707 2.2UF/6.3V — C0708 0.1UF/10V

11 PM_EXTTS#0 — RX0702 0Ohm @ — PM_EXTTS#0_R

M_VREF_MCH — C0709 2.2UF/6.3V — C0710 0.1UF/10V

VREF -> 10/10 mils

J0701B

	112	VDD1	VSS16	18	
	111	VDD2	VSS17	24	
	117	VDD3	VSS18	41	
	96	VDD4	VSS19	53	
	95	VDD5	VSS20	42	
	118	VDD6	VSS21	54	
	81	VDD7	VSS22	59	
	82	VDD8	VSS23	65	
	87	VDD9	VSS24	60	
	103	VDD10	VSS25	66	
	88	VDD11	VSS26	127	
	104	VDD12	VSS27	139	
			VSS28	145	
	199	VDDSPD	VSS29	165	
			VSS30	171	
	83	NC1	VSS31	172	
	120	NC2	VSS32	177	
	50	NC3	VSS33	187	
	69	NC4	VSS34	178	
	163	NCTEST	VSS35	190	
			VSS36	9	
	1	VREF	VSS37	21	
			VSS38	33	
	201	GND0	VSS39	155	
	202	GND1	VSS40	34	
			VSS41	132	
	203	NP_NC1	VSS42	144	
	204	NP_NC2	VSS43	156	
			VSS44	168	
	47	VSS1	VSS45	2	
	133	VSS2	VSS46	3	
	183	VSS3	VSS47	15	
	77	VSS4	VSS48	27	
	12	VSS5	VSS49	39	
	48	VSS6	VSS50	149	
	184	VSS7	VSS51	161	
	78	VSS8	VSS52	28	
	71	VSS9	VSS53	40	
	72	VSS10	VSS54	138	
	121	VSS11	VSS55	150	
	122	VSS12	VSS56	162	
	196	VSS13	VSS57		
	193	VSS14			
	8	VSS15			

DDR2_DIMM_200P

SO-DIMM 0 is placed nearer the GMCH than SO-DIMM 1

+1.8V — C0716 2.2UF/6.3V — C0717 2.2UF/6.3V — C0718 2.2UF/6.3V — C0719 2.2UF/6.3V

+1.8V — CE0701 220UF/4V @ +/-ESR=40mOhm/Ir=1900mA

PLACE NEAR SO-DIMM_0 / SO-DIMM_1

PEGATRON

Title : DDR2 SO-DIMM_0

Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.1

Date: Monday, February 04, 2008 Sheet 7 of 94

+3VS → +3VS 3,7,11,14,15,20,22,23,24,25,29,30,31,40,41,45,46,48,50,51,53,54,57,58,59,61,70,74,75,91,92

+1.8V → +1.8V 7,9,11,13,83,91

M_VREF_MCH → M_VREF_MCH 7,9,11

temp_5886_tl02
(12G025032005LV with 12G025022004LV
CO-LAY symbol)

9,12 M_B_A[0..14]

M_B_DQ[0..63] 12

J0801A

SMBus Slave Address:A4H

M_CLK_DDR3 — C0801 10PF/50V @ — M_CLK_DDR#3

M_CLK_DDR2 — C0802 10PF/50V @ — M_CLK_DDR#2

Place near SO-DIMM_1

+3VS — R0804 10KOhm — M_B_SA0

+3VS — R0803 10KOhm — M_B_SA1

7,24,25,29 SMB_CLK_M

7,24,25,29 SMB_DAT_M

9,11 M_ODT2

9,11 M_ODT3

12 M_B_DM[0..7]

12 M_B_DQS[0..7]

12 M_B_DQS#[0..7]

DDR2_DIMM_200P

+1.8V

Layout Note: Place these Caps near the SO-DIMM_1

C0816 2.2UF/6.3V — C0817 2.2UF/6.3V — C0818 2.2UF/6.3V — C0819 2.2UF/6.3V

+1.8V

Layout Note: Place these Caps near SO DIMM 1

C0803 0.1UF/10V — C0804 0.1UF/10V — C0805 0.1UF/10V — C0806 0.1UF/10V

+3VS

C0807 2.2UF/6.3V — C0808 0.1UF/10V

11 PM_EXTTS#1 — RX0802 @ 0Ohm — PM_EXTTS#1_R

M_VREF_MCH

C0809 2.2UF/6.3V — C0810 0.1UF/10V

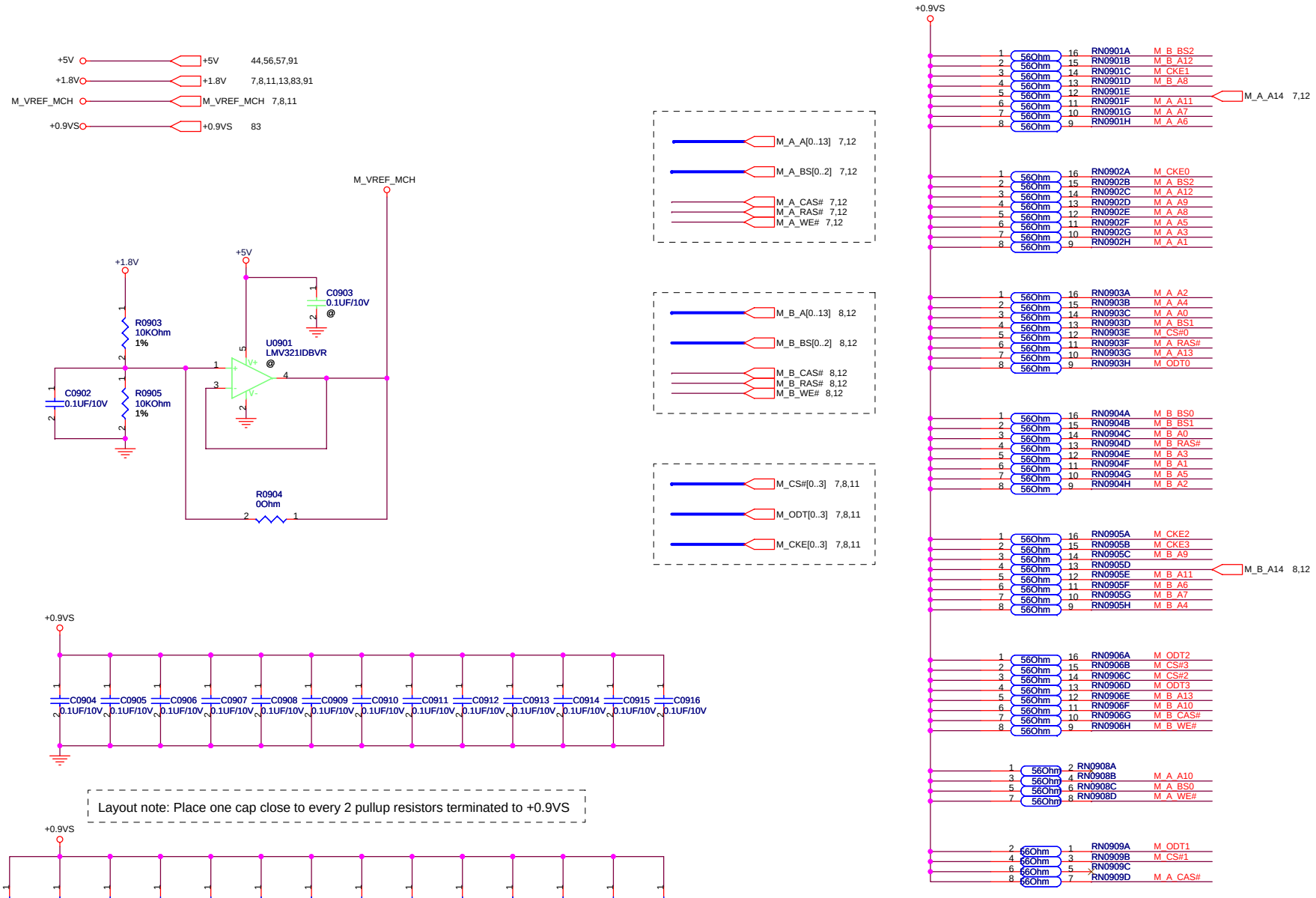
Layout Note: Place these Caps near SO DIMM 1

VREF -> 10/10 mils

J0801B

DDR2_DIMM_200P

PEGATRON	Title : DDR2 SO-DIMM_1
	Engineer: Peter Lo
Size: Custom	Project Name: Rocky30
Rev: 1.1	
Date: Monday, February 04, 2008	Sheet 8 of 94

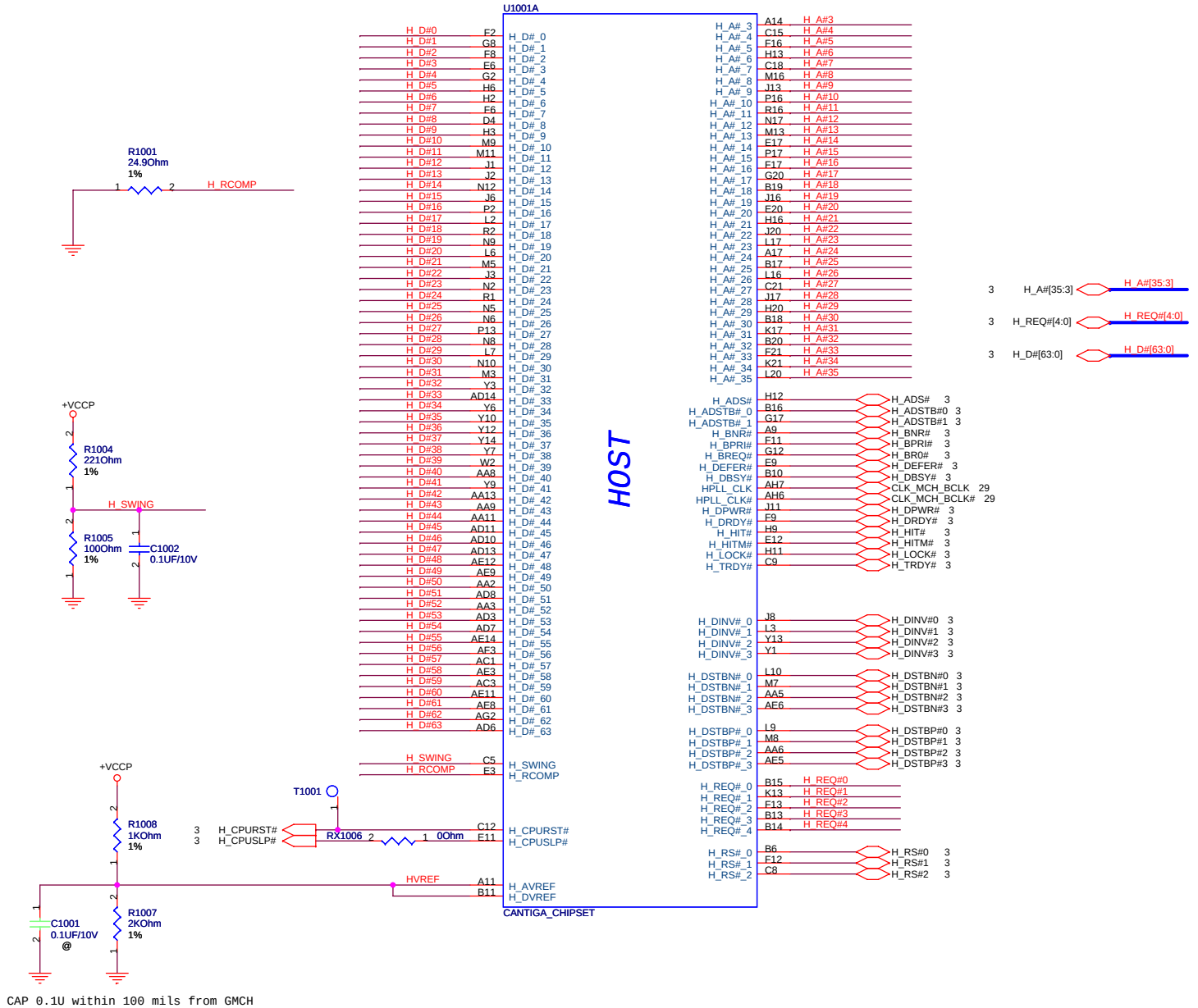


PEGATRON **Title :** DDR2 VREF & Termination

Engineer: *Peter Lo*

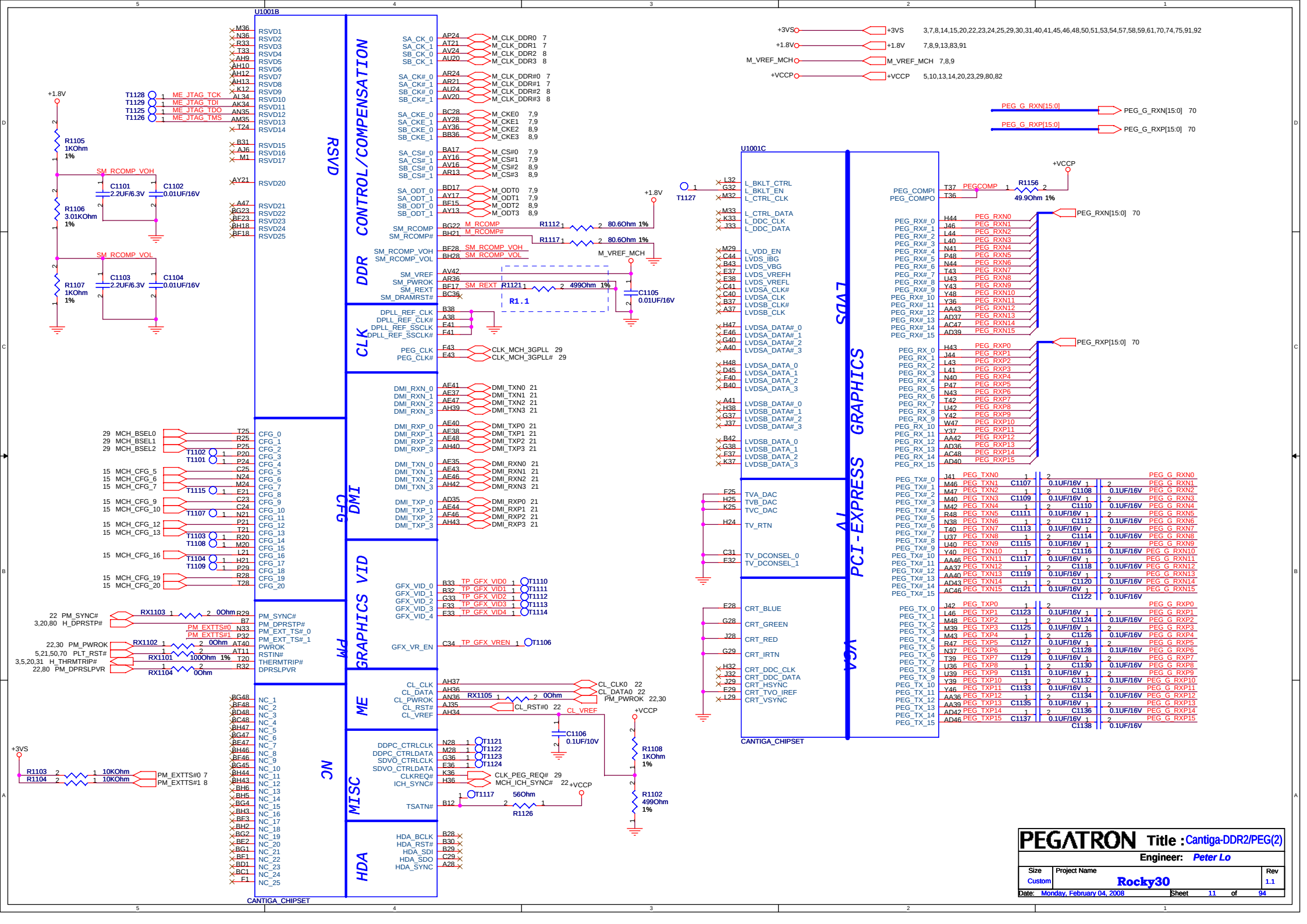
Size	Project Name	Rev
Custom	Rocky30	1.1

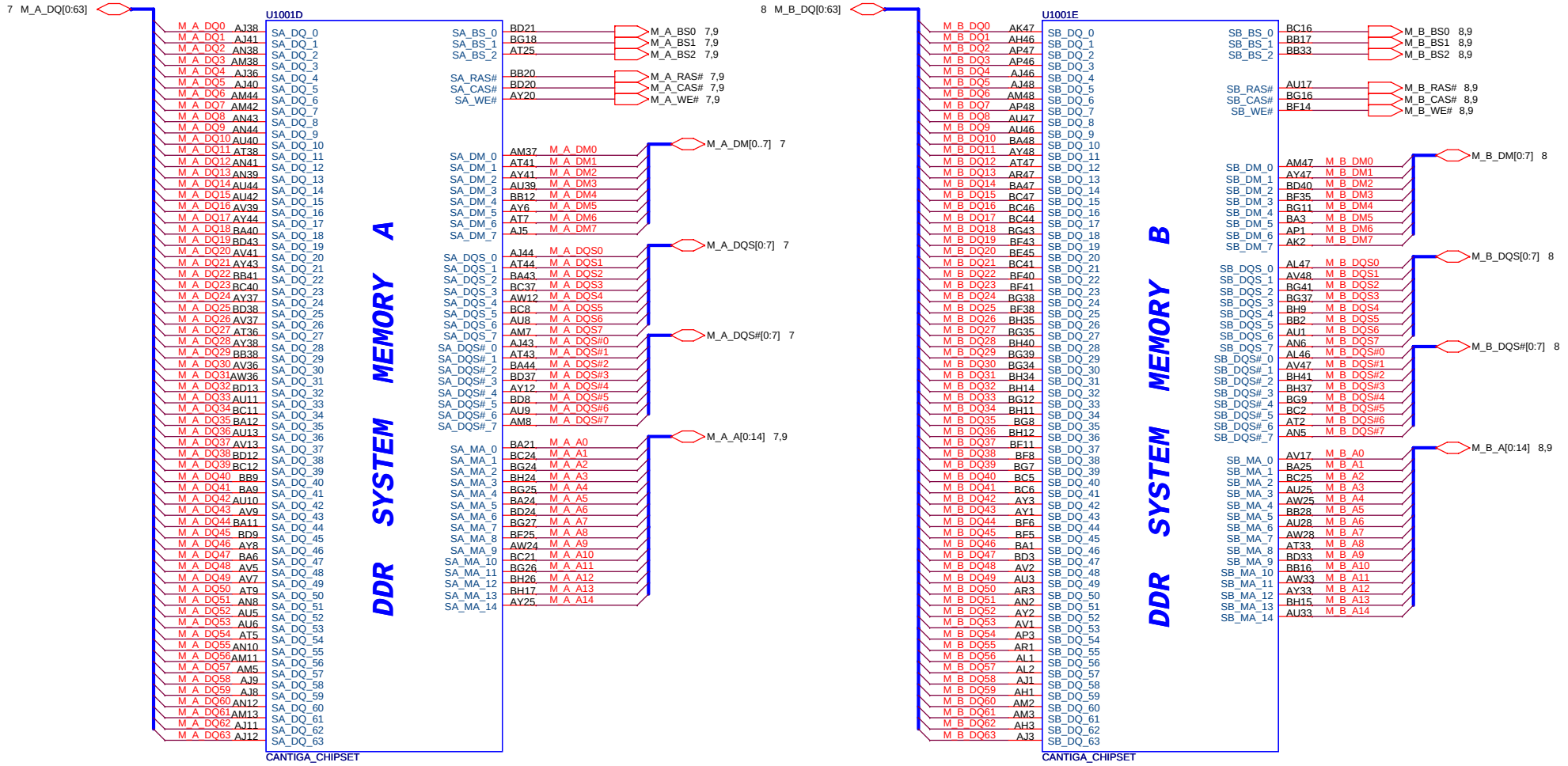
Date: Monday, February 04, 2008 Sheet 9 of 94



CAP 0.1U within 100 mils from GMCH

PEGATRON	Title :	Cantiga – CPU (1)	
	Engineer:	Peter Lo	
Size: Custom	Project Name: Rocky30		Rev: 1.1
Date: Monday, February 04, 2008	Sheet 10 of 94		


U1001B
RSVD
CONTROL/COMPENSATION
DDR
CLK
DMI
CFG
VID
GRAPHICS
PM
ME
MISC
HDA
NC
CANTIGA_CHIPSET
U1001C
LVDS
PCI-EXPRESS GRAPHICS
TV
VGA
CANTIGA_CHIPSET
PEGATRON
Title : Cantiga-DDR2/PEG(2)
Engineer: Peter Lo
Size: Custom
Project Name: Rocky30
Rev: 1.1
Date: Monday, February 04, 2008
Sheet 11 of 94

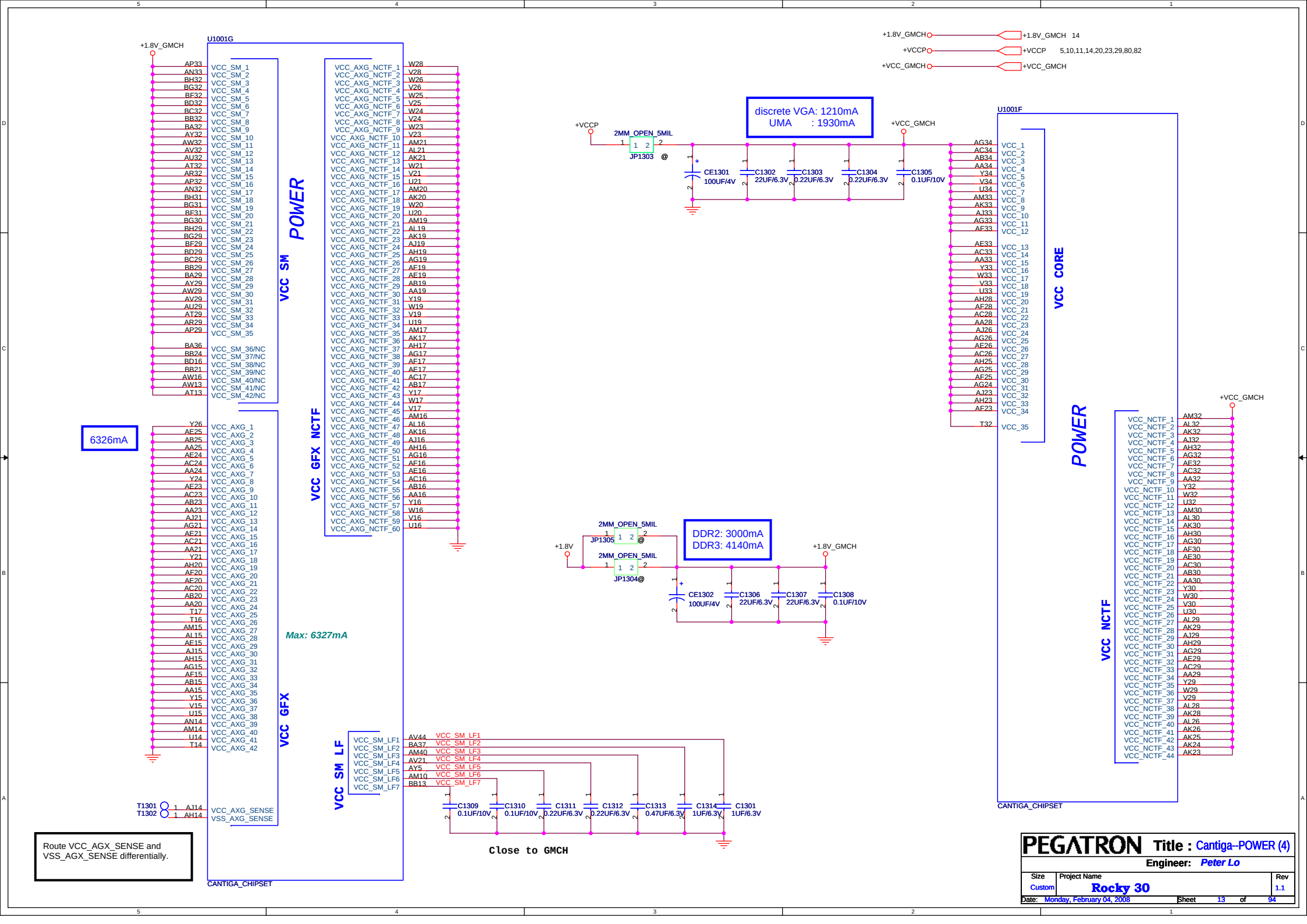


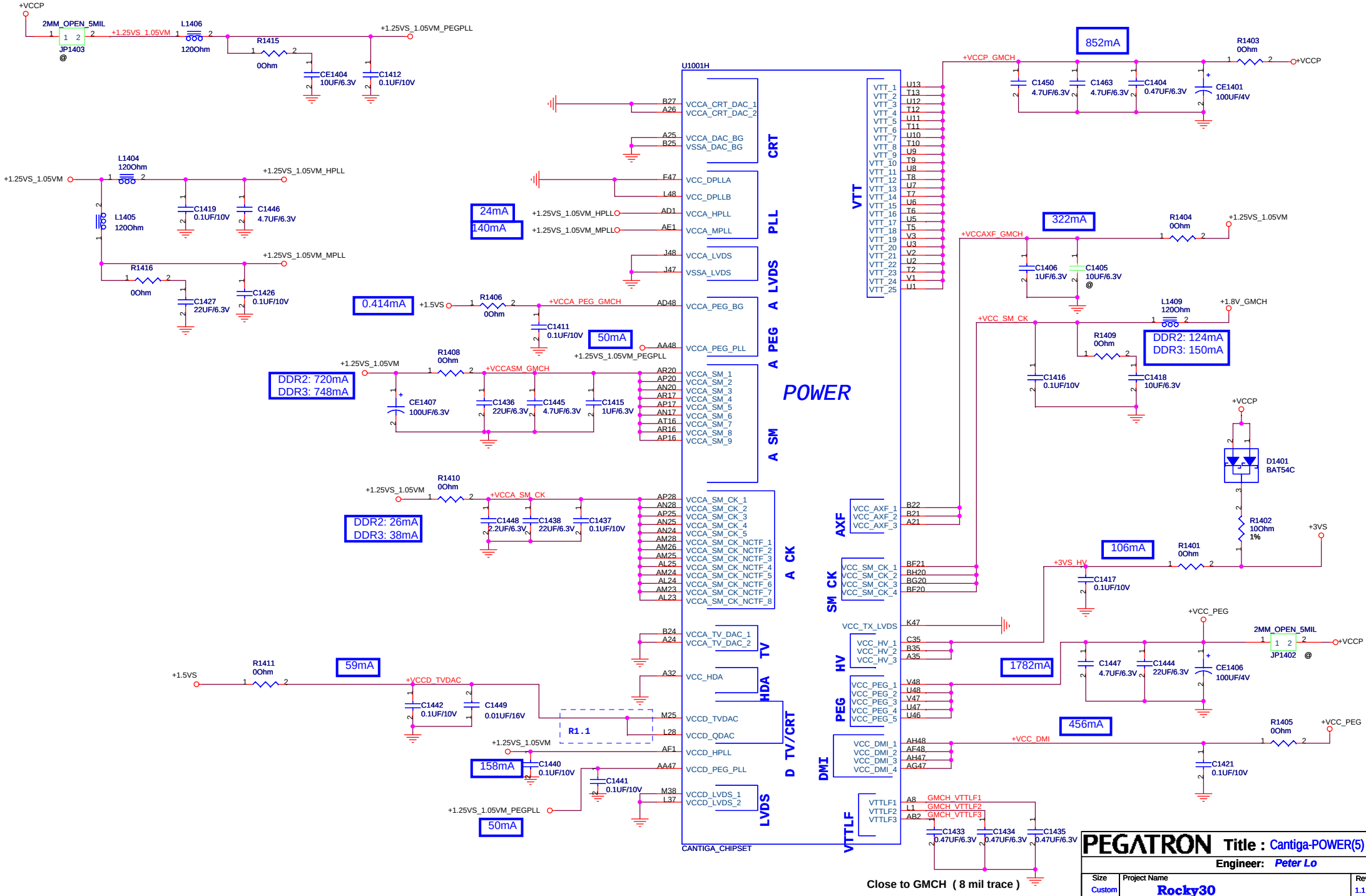
PEGATRON **Title :** Cantiga--DDR2 (3)

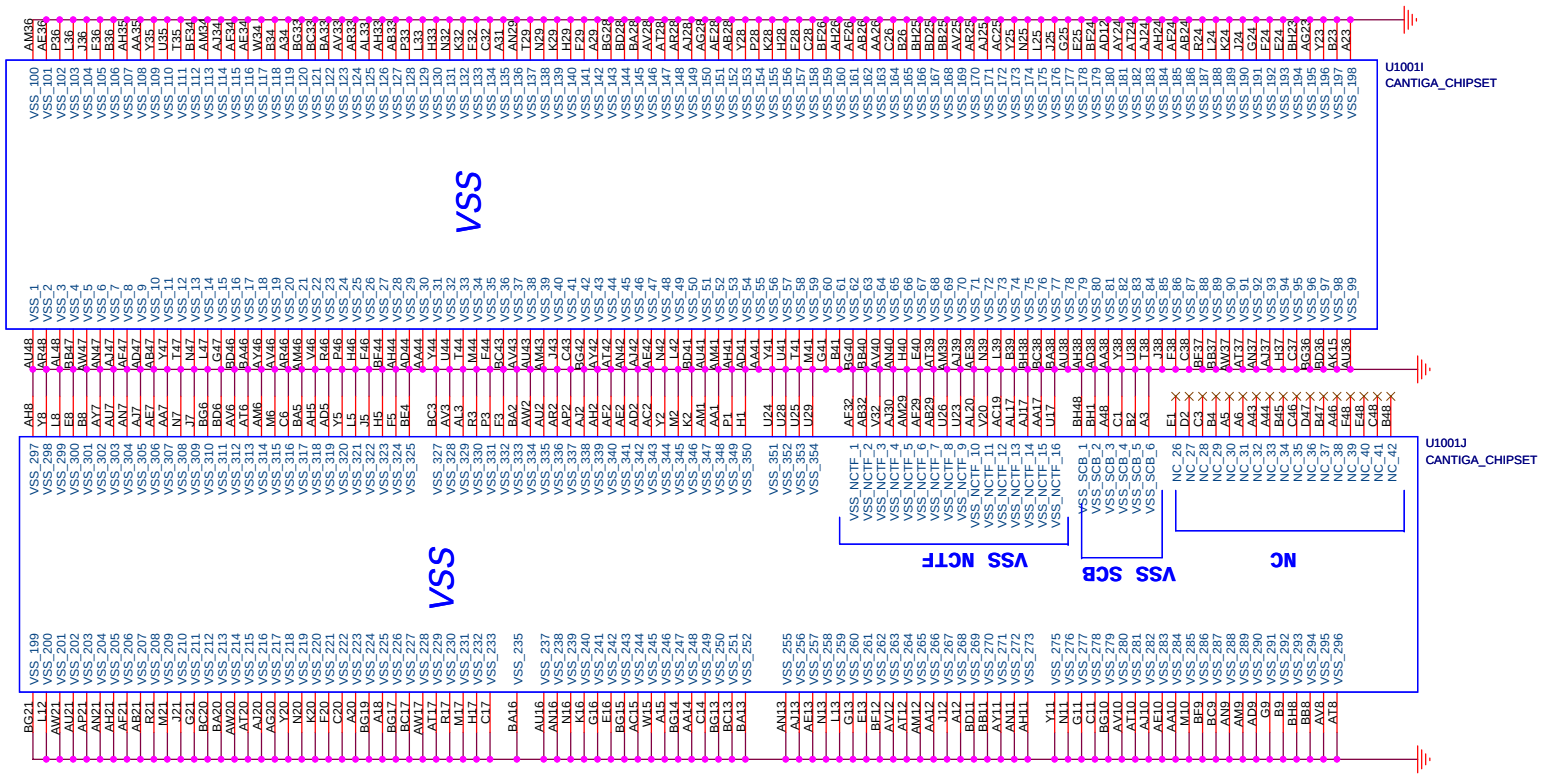
Engineer: *Peter Lo*

Size	Project Name	Rev
Custom	**Rocky30**	1.1

Date: Monday, February 04, 2008 Sheet 12 of 94


U1001G
+1.8V_GMCH
VCC_SM_1 VCC_SM_2 VCC_SM_3 VCC_SM_4 VCC_SM_5 VCC_SM_6 VCC_SM_7 VCC_SM_8 VCC_SM_9 VCC_SM_10 VCC_SM_11 VCC_SM_12 VCC_SM_13 VCC_SM_14 VCC_SM_15 VCC_SM_16 VCC_SM_17 VCC_SM_18 VCC_SM_19 VCC_SM_20 VCC_SM_21 VCC_SM_22 VCC_SM_23 VCC_SM_24 VCC_SM_25 VCC_SM_26 VCC_SM_27 VCC_SM_28 VCC_SM_29 VCC_SM_30 VCC_SM_31 VCC_SM_32 VCC_SM_33 VCC_SM_34 VCC_SM_35
VCC_SM_36/NC VCC_SM_37/NC VCC_SM_38/NC VCC_SM_39/NC VCC_SM_40/NC VCC_SM_41/NC VCC_SM_42/NC
VCC SM POWER
VCC_AXG_NCTF_1 VCC_AXG_NCTF_2 VCC_AXG_NCTF_3 VCC_AXG_NCTF_4 VCC_AXG_NCTF_5 VCC_AXG_NCTF_6 VCC_AXG_NCTF_7 VCC_AXG_NCTF_8 VCC_AXG_NCTF_9 VCC_AXG_NCTF_10 VCC_AXG_NCTF_11 VCC_AXG_NCTF_12 VCC_AXG_NCTF_13 VCC_AXG_NCTF_14 VCC_AXG_NCTF_15 VCC_AXG_NCTF_16 VCC_AXG_NCTF_17 VCC_AXG_NCTF_18 VCC_AXG_NCTF_19 VCC_AXG_NCTF_20 VCC_AXG_NCTF_21 VCC_AXG_NCTF_22 VCC_AXG_NCTF_23 VCC_AXG_NCTF_24 VCC_AXG_NCTF_25 VCC_AXG_NCTF_26 VCC_AXG_NCTF_27 VCC_AXG_NCTF_28 VCC_AXG_NCTF_29 VCC_AXG_NCTF_30 VCC_AXG_NCTF_31 VCC_AXG_NCTF_32 VCC_AXG_NCTF_33 VCC_AXG_NCTF_34 VCC_AXG_NCTF_35 VCC_AXG_NCTF_36 VCC_AXG_NCTF_37 VCC_AXG_NCTF_38 VCC_AXG_NCTF_39 VCC_AXG_NCTF_40 VCC_AXG_NCTF_41 VCC_AXG_NCTF_42 VCC_AXG_NCTF_43 VCC_AXG_NCTF_44 VCC_AXG_NCTF_45 VCC_AXG_NCTF_46 VCC_AXG_NCTF_47 VCC_AXG_NCTF_48 VCC_AXG_NCTF_49 VCC_AXG_NCTF_50 VCC_AXG_NCTF_51 VCC_AXG_NCTF_52 VCC_AXG_NCTF_53 VCC_AXG_NCTF_54 VCC_AXG_NCTF_55 VCC_AXG_NCTF_56 VCC_AXG_NCTF_57 VCC_AXG_NCTF_58 VCC_AXG_NCTF_59 VCC_AXG_NCTF_60
VCC GFX NCTF
6326mA
VCC_AXG_1 VCC_AXG_2 VCC_AXG_3 VCC_AXG_4 VCC_AXG_5 VCC_AXG_6 VCC_AXG_7 VCC_AXG_8 VCC_AXG_9 VCC_AXG_10 VCC_AXG_11 VCC_AXG_12 VCC_AXG_13 VCC_AXG_14 VCC_AXG_15 VCC_AXG_16 VCC_AXG_17 VCC_AXG_18 VCC_AXG_19 VCC_AXG_20 VCC_AXG_21 VCC_AXG_22 VCC_AXG_23 VCC_AXG_24 VCC_AXG_25 VCC_AXG_26 VCC_AXG_27 VCC_AXG_28 VCC_AXG_29 VCC_AXG_30 VCC_AXG_31 VCC_AXG_32 VCC_AXG_33 VCC_AXG_34 VCC_AXG_35 VCC_AXG_36 VCC_AXG_37 VCC_AXG_38 VCC_AXG_39 VCC_AXG_40 VCC_AXG_41 VCC_AXG_42
VCC GFX
Max: 6327mA
T1301 T1302
VCC_AXG_SENSE VSS_AXG_SENSE
VCC_SM_LF1 VCC_SM_LF2 VCC_SM_LF3 VCC_SM_LF4 VCC_SM_LF5 VCC_SM_LF6 VCC_SM_LF7
VCC SM LF
C1309 0.1UF/10V C1310 0.1UF/10V C1311 0.22UF/6.3V C1312 0.22UF/6.3V C1313 0.47UF/6.3V C1314 1UF/6.3V C1301 1UF/6.3V
Close to GMCH
CANTIGA_CHIPSET
Route VCC_AGX_SENSE and VSS_AGX_SENSE differentially.
+1.8V_GMCH +1.8V_GMCH 14
+VCCP +VCCP 5,10,11,14,20,23,29,80,82
+VCC_GMCH +VCC_GMCH
discrete VGA: 1210mA
UMA : 1930mA
+VCCP
2MM_OPEN_5MIL JP1303 @
CE1301 100UF/4V C1302 22UF/6.3V C1303 0.22UF/6.3V C1304 0.22UF/6.3V C1305 0.1UF/10V
+VCC_GMCH
U1001F
VCC_1 VCC_2 VCC_3 VCC_4 VCC_5 VCC_6 VCC_7 VCC_8 VCC_9 VCC_10 VCC_11 VCC_12 VCC_13 VCC_14 VCC_15 VCC_16 VCC_17 VCC_18 VCC_19 VCC_20 VCC_21 VCC_22 VCC_23 VCC_24 VCC_25 VCC_26 VCC_27 VCC_28 VCC_29 VCC_30 VCC_31 VCC_32 VCC_33 VCC_34 VCC_35
VCC CORE
2MM_OPEN_5MIL JP1305 @
2MM_OPEN_5MIL JP1304@
+1.8V
DDR2: 3000mA
DDR3: 4140mA
+1.8V_GMCH
CE1302 100UF/4V C1306 22UF/6.3V C1307 22UF/6.3V C1308 0.1UF/10V
VCC_NCTF_1 VCC_NCTF_2 VCC_NCTF_3 VCC_NCTF_4 VCC_NCTF_5 VCC_NCTF_6 VCC_NCTF_7 VCC_NCTF_8 VCC_NCTF_9 VCC_NCTF_10 VCC_NCTF_11 VCC_NCTF_12 VCC_NCTF_13 VCC_NCTF_14 VCC_NCTF_15 VCC_NCTF_16 VCC_NCTF_17 VCC_NCTF_18 VCC_NCTF_19 VCC_NCTF_20 VCC_NCTF_21 VCC_NCTF_22 VCC_NCTF_23 VCC_NCTF_24 VCC_NCTF_25 VCC_NCTF_26 VCC_NCTF_27 VCC_NCTF_28 VCC_NCTF_29 VCC_NCTF_30 VCC_NCTF_31 VCC_NCTF_32 VCC_NCTF_33 VCC_NCTF_34 VCC_NCTF_35 VCC_NCTF_36 VCC_NCTF_37 VCC_NCTF_38 VCC_NCTF_39 VCC_NCTF_40 VCC_NCTF_41 VCC_NCTF_42 VCC_NCTF_43 VCC_NCTF_44
VCC NCTF
+VCC_GMCH
CANTIGA_CHIPSET
PEGATRON
Title : Cantiga--POWER (4)
Engineer: Peter Lo
Size: Custom
Project Name: Rocky 30
Rev: 1.1
Date: Monday, February 04, 2008
Sheet 13 of 94


+VCCP
2MM_OPEN_5MIL
JP1403
@
+1.25VS_1.05VM
L1406
120Ohm
R1415
0Ohm
CE1404
10UF/6.3V
C1412
0.1UF/10V
+1.25VS_1.05VM_PEGPLL
L1404
120Ohm
L1405
120Ohm
C1419
0.1UF/10V
C1446
4.7UF/6.3V
+1.25VS_1.05VM_HPLL
+1.25VS_1.05VM_MPLL
R1416
0Ohm
C1427
22UF/6.3V
C1426
0.1UF/10V
U1001H
CRT
PLL
LVDS
A PEG
A SM
A CK
TV
HDA
D TV/CRT
LVDS
CANTIGA_CHIPSET
B27
A26
VCCA_CRT_DAC_1
VCCA_CRT_DAC_2
A25
B25
VCCA_DAC_BG
VSSA_DAC_BG
24mA
140mA
F47
L48
VCC_DPLLA
VCC_DPLLB
AD1
AE1
VCCA_HPLL
VCCA_MPLL
J48
J47
VCCA_LVDS
VSSA_LVDS
0.414mA
+1.5VS
R1406
0Ohm
+VCCA_PEG_GMCH
C1411
0.1UF/10V
50mA
AD48
AA48
VCCA_PEG_BG
VCCA_PEG_PLL
+1.25VS_1.05VM_PEGPLL
DDR2: 720mA
DDR3: 748mA
R1408
0Ohm
+VCCASM_GMCH
CE1407
100UF/6.3V
C1436
22UF/6.3V
C1445
4.7UF/6.3V
C1415
1UF/6.3V
AR20
AP20
AN20
AR17
AP17
AN17
AT16
AR16
AP16
VCCA_SM_1
VCCA_SM_2
VCCA_SM_3
VCCA_SM_4
VCCA_SM_5
VCCA_SM_6
VCCA_SM_7
VCCA_SM_8
VCCA_SM_9
DDR2: 26mA
DDR3: 38mA
R1410
0Ohm
+VCCA_SM_CK
C1448
2.2UF/6.3V
C1438
22UF/6.3V
C1437
0.1UF/10V
AP28
AN28
AP25
AN25
AN24
AM28
AM26
AM25
AL25
AM24
AL24
AM23
AL23
VCCA_SM_CK_1
VCCA_SM_CK_2
VCCA_SM_CK_3
VCCA_SM_CK_4
VCCA_SM_CK_5
VCCA_SM_CK_NCTF_1
VCCA_SM_CK_NCTF_2
VCCA_SM_CK_NCTF_3
VCCA_SM_CK_NCTF_4
VCCA_SM_CK_NCTF_5
VCCA_SM_CK_NCTF_6
VCCA_SM_CK_NCTF_7
VCCA_SM_CK_NCTF_8
B24
A24
VCCA_TV_DAC_1
VCCA_TV_DAC_2
59mA
+1.5VS
R1411
0Ohm
+VCCD_TVDAC
C1442
0.1UF/10V
C1449
0.01UF/16V
A32
VCC_HDA
M25
L28
VCCD_TVDAC
VCCD_QDAC
R1.1
+1.25VS_1.05VM
AF1
AA47
VCCD_HPLL
VCCD_PEG_PLL
158mA
C1440
0.1UF/10V
C1441
0.1UF/10V
M38
L37
VCCD_LVDS_1
VCCD_LVDS_2
+1.25VS_1.05VM_PEGPLL
50mA
POWER
VTT
VTT_1
VTT_2
VTT_3
VTT_4
VTT_5
VTT_6
VTT_7
VTT_8
VTT_9
VTT_10
VTT_11
VTT_12
VTT_13
VTT_14
VTT_15
VTT_16
VTT_17
VTT_18
VTT_19
VTT_20
VTT_21
VTT_22
VTT_23
VTT_24
VTT_25
U13
T13
U12
T12
U11
T11
U10
T10
U9
T9
U8
T8
U7
T7
U6
T6
U5
T5
V3
U3
V2
U2
T2
V1
U1
AXF
VCC_AXF_1
VCC_AXF_2
VCC_AXF_3
B22
B21
A21
SM CK
VCC_SM_CK_1
VCC_SM_CK_2
VCC_SM_CK_3
VCC_SM_CK_4
BF21
BH20
BG20
BF20
HV
VCC_TX_LVDS
K47
VCC_HV_1
VCC_HV_2
VCC_HV_3
C35
B35
A35
PEG
VCC_PEG_1
VCC_PEG_2
VCC_PEG_3
VCC_PEG_4
VCC_PEG_5
V48
U48
V47
U47
U46
DMI
VCC_DMI_1
VCC_DMI_2
VCC_DMI_3
VCC_DMI_4
AH48
AF48
AH47
AG47
VTTLF
VTTLF1
VTTLF2
VTTLF3
A8
L1
AB2
GMCH_VTTLF1
GMCH_VTTLF2
GMCH_VTTLF3
C1433
0.47UF/6.3V
C1434
0.47UF/6.3V
C1435
0.47UF/6.3V
852mA
+VCCP_GMCH
C1450
4.7UF/6.3V
C1463
4.7UF/6.3V
C1404
0.47UF/6.3V
R1403
0Ohm
CE1401
100UF/4V
322mA
+VCCAXF_GMCH
C1406
1UF/6.3V
C1405
10UF/6.3V
@
R1404
0Ohm
+1.25VS_1.05VM
+VCC_SM_CK
C1416
0.1UF/10V
R1409
0Ohm
L1409
120Ohm
+1.8V_GMCH
DDR2: 124mA
DDR3: 150mA
C1418
10UF/6.3V
+VCCP
D1401
BAT54C
R1402
10Ohm
1%
+3VS
106mA
R1401
0Ohm
+3VS_HV
C1417
0.1UF/10V
1782mA
+VCC_PEG
2MM_OPEN_5MIL
JP1402
@
+VCCP
C1447
4.7UF/6.3V
C1444
22UF/6.3V
CE1406
100UF/4V
456mA
+VCC_DMI
R1405
0Ohm
+VCC_PEG
C1421
0.1UF/10V
Close to GMCH (8 mil trace)
PEGATRON
Title : Cantiga-POWER(5)
Engineer: Peter Lo
Size
Custom
Project Name
Rocky30
Rev
1.1
Date: Saturday, January 26, 2008
Sheet 14 of 94



11 MCH_CFG_5 — R1509 2.21KOhm 1% @

CFG5 : DMI STRAP
HIGH = DMI X 4 (Default)
LOW = DMI X 2

11 MCH_CFG_6 — R1514 2.21KOhm 1% @

CFG6 : Integrated TPM Host Interface
HIGH = iTPM disable (Default)
LOW = iTPM enable

11 MCH_CFG_7 — R1511 2.21KOhm 1% @

CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite
HIGH = With confidentiality (Default)
LOW = Without confidentiality

11 MCH_CFG_9 — R1512 2.21KOhm 1% @

CFG9 : PCIE GRAPHIC LANE
LOW = Reverse Lanes
HIGH = Normal Operation (Default)

11 MCH_CFG_16 — R1507 2.21KOhm 1% @

CFG16 : FSB Dynamic ODT
HIGH = Ensable (Default)
LOW = Disable

11 MCH_CFG_10 — R1508 2.21KOhm 1% @

CFG10 : PCIe Loopback
HIGH = Disable (Default)
LOW = Enable

11 MCH_CFG_12 — R1513 2.21KOhm 1% @

11 MCH_CFG_13 — R1510 2.21KOhm 1% @

CFG [13:12] : XOR/ALL-Z
00 = Reserved
01= XOR Mode Enabled
10= All-Z Mode Enabled
11= Normal Operation (Default)

+3VS — R1503 4.02KOhm 1% @ — 11 MCH_CFG_19

CFG19 : DMI Lane Reversal
LOW = NORMAL (default)
HIGH = Reverse Lanes

+3VS — R1506 4.02KOhm 1% @ — 11 MCH_CFG_20

CFG20 : SDVO/PCIE CONCURRENT MODE
LOW = ONLY SDVO or PCIE is Operational (Default)
HIGH = SDVO and PCIE are operating simultaneously via the PEG port

PEGATRON	Title : Cantiga-GND	
	Engineer: Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.1
Date: Monday, February 04, 2008	Sheet 15 of 94	

PEGATRON Title : ***

Engineer: *Peter Lo*

Size	Project Name	Rev
B	Rocky30	1.1

Date: Saturday, January 26, 2008 Sheet 16 of 94

PEGATRON Title : ***

Engineer: *Peter Lo*

Size	Project Name	Rev
B	Rocky30	1.1

Date: Saturday, January 26, 2008 Sheet 17 of 94

PEGATRON Title : ***

Engineer: *Peter Lo*

Size	Project Name	Rev
B	Rocky30	1.1

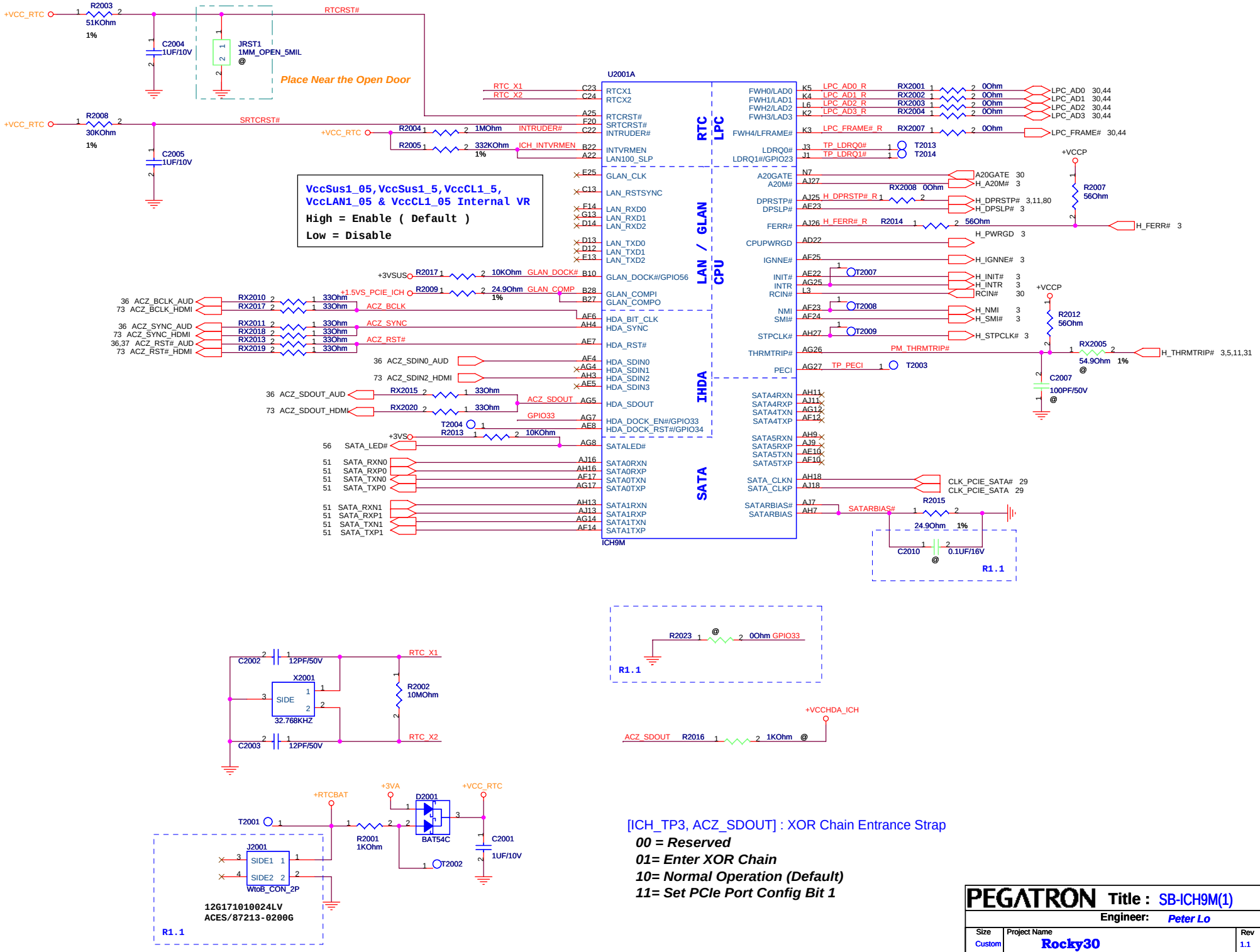
Date: Saturday, January 26, 2008 Sheet 18 of 94

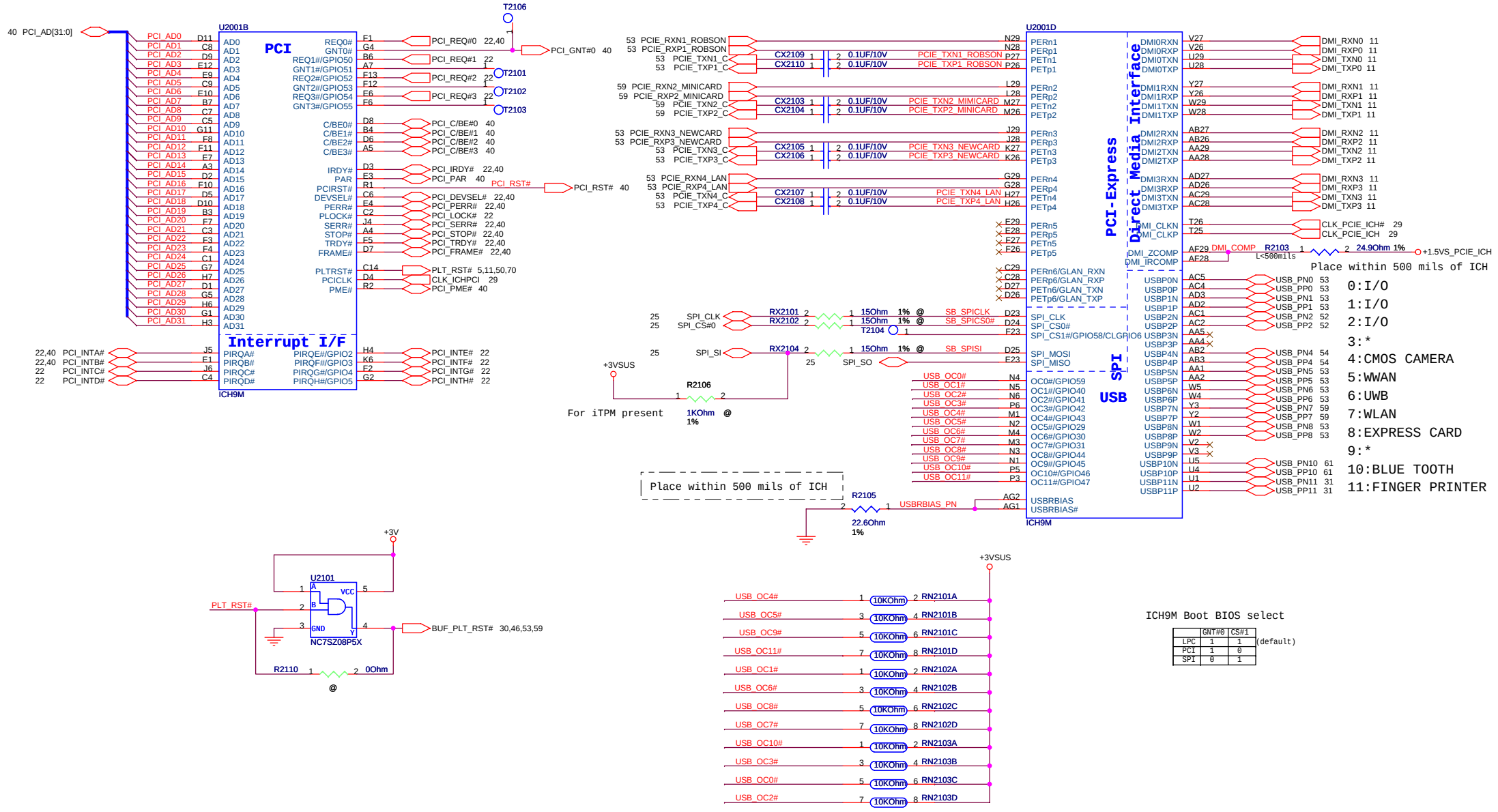
PEGATRON Title : ***

Engineer: *Peter Lo*

Size	Project Name	Rev
B	Rocky30	1.1

Date: Saturday, January 26, 2008 Sheet 19 of 94


R2003
51KOhm
1%
+VCC_RTC
C2004
1UF/10V
JRST1
1MM_OPEN_5MIL
@
RTCRST#
Place Near the Open Door
R2008
30KOhm
1%
SRTCRST#
C2005
1UF/10V
U2001A
RTC_X1
RTC_X2
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
R2004
1MOhm
R2005
332KOhm
1%
ICH_INTVRMEN
RTC
LPC
VccSus1_05,VccSus1_5,VccCL1_5,
VccLAN1_05 & VccCL1_05 Internal VR
High = Enable (Default)
Low = Disable
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO56
GLAN_COMPI
GLAN_COMPO
R2017
10KOhm
GLAN_DOCK#
R2009
24.9Ohm
1%
GLAN_COMP
+1.5VS_PCIE_ICH
+3VSUS
LAN / GLAN
CPU
RX2010
RX2017
RX2011
RX2018
RX2013
RX2019
33Ohm
ACZ_BCLK
ACZ_SYNC
ACZ_RST#
36 ACZ_BCLK_AUD
73 ACZ_BCLK_HDMI
36 ACZ_SYNC_AUD
73 ACZ_SYNC_HDMI
36,37 ACZ_RST#_AUD
73 ACZ_RST#_HDMI
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
36 ACZ_SDIN0_AUD
73 ACZ_SDIN2_HDMI
36 ACZ_SDOUT_AUD
73 ACZ_SDOUT_HDMI
RX2015
RX2020
ACZ_SDOUT
GPIO33
T2004
R2013
10KOhm
+3VS
IHDA
SATALED#
56 SATA_LED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
51 SATA_RXN0
51 SATA_RXP0
51 SATA_TXN0
51 SATA_TXP0
51 SATA_RXN1
51 SATA_RXP1
51 SATA_TXN1
51 SATA_TXP1
SATA
ICH9M
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
LPC_AD0_R
LPC_AD1_R
LPC_AD2_R
LPC_AD3_R
LPC_FRAME#_R
TP_LDRQ0#
TP_LDRQ1#
RX2001
RX2002
RX2003
RX2004
RX2007
0Ohm
T2013
T2014
LPC_AD0 30,44
LPC_AD1 30,44
LPC_AD2 30,44
LPC_AD3 30,44
LPC_FRAME# 30,44
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
PECI
RX2008
H_DPRSTP# R
H_FERR# R
R2014
56Ohm
T2007
T2008
T2009
T2003
PM_THRMTRIP#
TP_PECI
A20GATE 30
H_A20M# 3
H_DPRSTP# 3,11,80
H_DPSLP# 3
H_FERR# 3
H_PWRGD 3
H_IGNNE# 3
H_INIT# 3
H_INTR 3
RCIN# 30
H_NMI 3
H_SMI# 3
H_STPCLK# 3
H_THRMTRIP# 3,5,11,31
+VCCP
R2007
56Ohm
R2012
56Ohm
RX2005
54.9Ohm
1%
C2007
100PF/50V
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
CLK_PCIE_SATA# 29
CLK_PCIE_SATA 29
R2015
24.9Ohm
1%
C2010
0.1UF/16V
R1.1
C2002
12PF/50V
X2001
SIDE
32.768KHZ
C2003
12PF/50V
R2002
10MOhm
R2023
0Ohm GPIO33
R1.1
ACZ_SDOUT
R2016
1KOhm
+VCCHDA_ICH
+RTCBAT
+3VA
+VCC_RTC
T2001
R2001
1KOhm
D2001
BAT54C
T2002
C2001
1UF/10V
J2001
SIDE1
SIDE2
WtoB_CON_2P
12G171010024LV
ACES/87213-0200G
R1.1
[ICH_TP3, ACZ_SDOUT] : XOR Chain Entrance Strap
00 = Reserved
01= Enter XOR Chain
10= Normal Operation (Default)
11= Set PCIe Port Config Bit 1
PEGATRON
Title : SB-ICH9M(1)
Engineer: Peter Lo
Size
Custom
Project Name
Rocky30
Rev
1.1
Date: Monday, February 04, 2008
Sheet 20 of 94



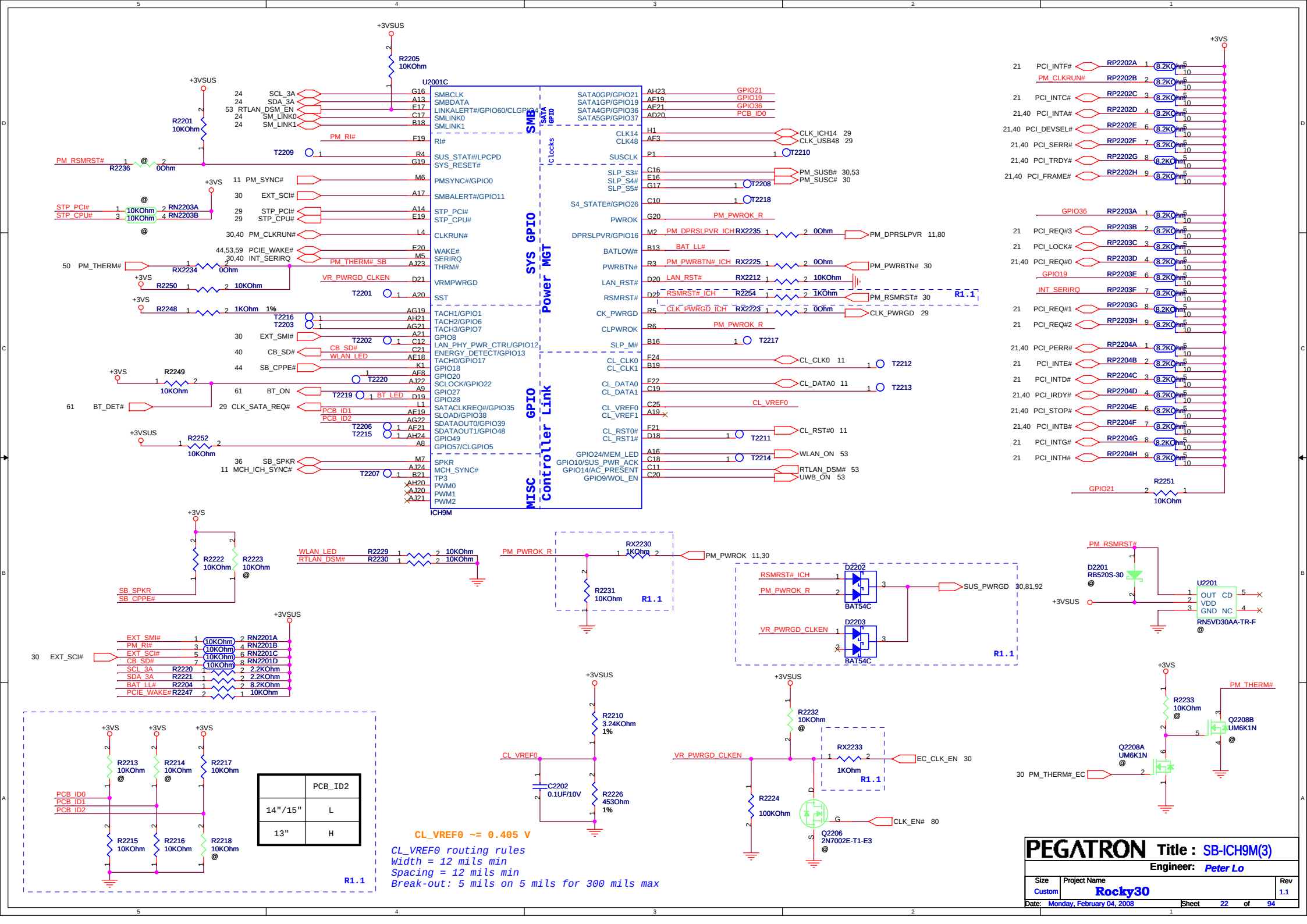
	GNT#0	CS#1	
LPC	1	1	(default)
PCI	1	0	
SPI	0	1	

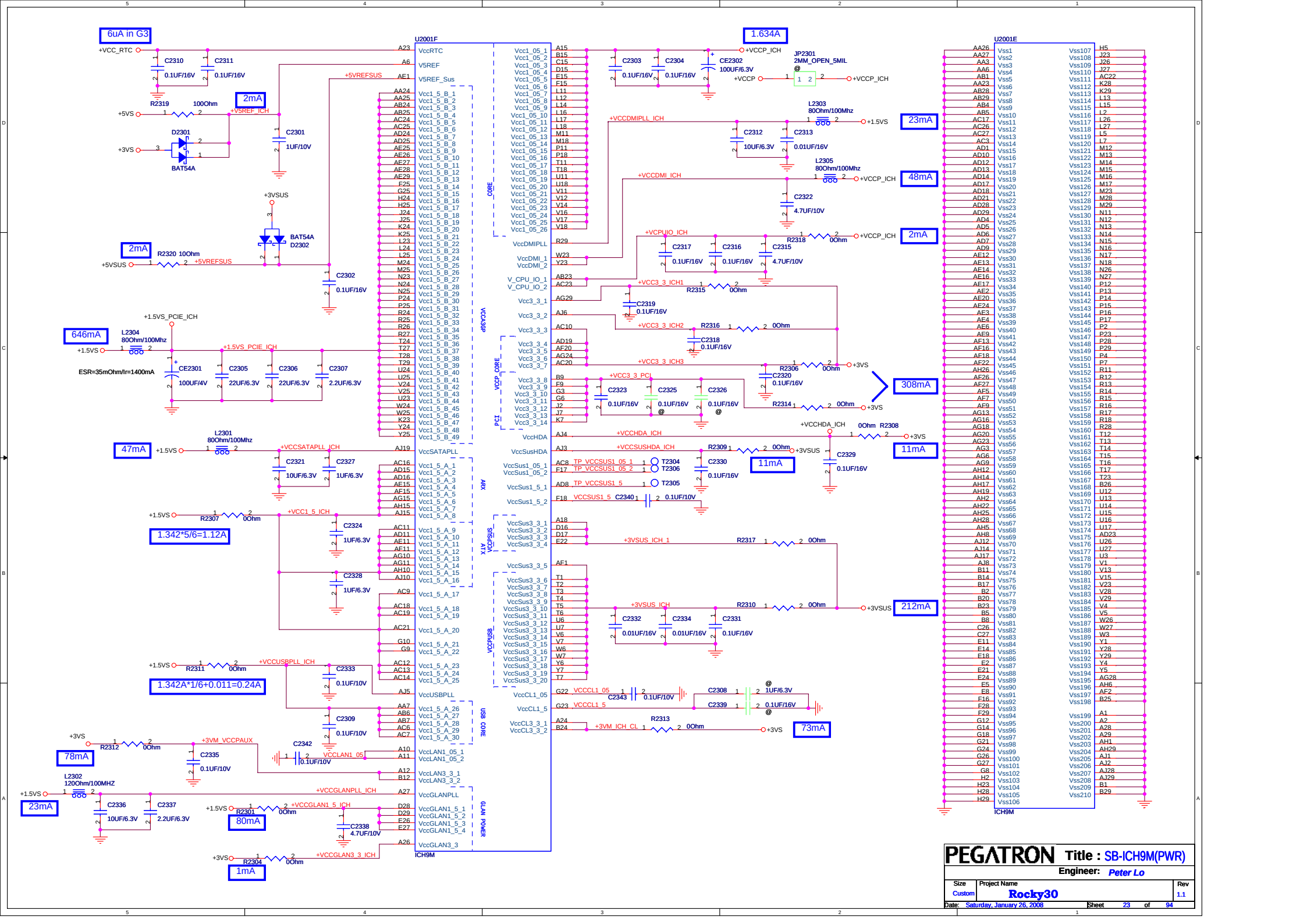
PEGATRON Title : SB-ICH9M(2)

Engineer: Peter Lo

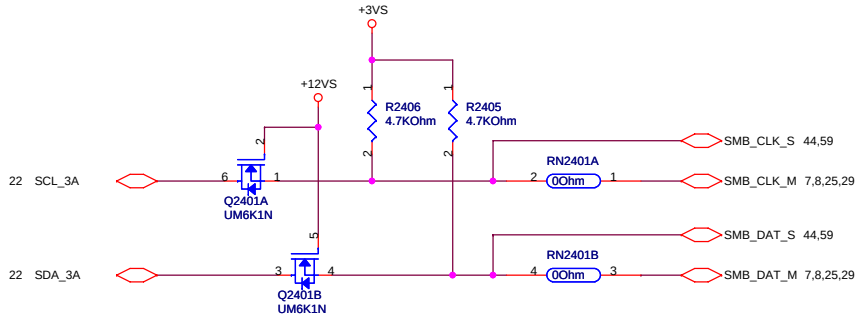
Size	Project Name	Rev
Custom	Rocky30	1.1

Date: Monday, February 04, 2008 Sheet 21 of 94


U2001C
ICH9M
SMB
GPIO
SATA GPIO
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
I C Locks
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO4
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STP_PCI#
STP_CPU#
CLKRUN#
WAKE#
SERIRQ
THRM#
VRMPWRGD
SST
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LAN_PHY_PWR_CTRL/GPIO12
ENERGY_DETECT/GPIO13
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
GPIO27
GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
PWM0
PWM1
PWM2
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_RST1#
GPIO24/MEM_LED
GPIO10/SUS_PWR_ACK
GPIO14/AC_PRESENT
GPIO9/WOL_EN
R2205 10KOhm
R2201 10KOhm
R2236 0Ohm
T2209
RN2203A 10KOhm
RN2203B 10KOhm
R2250 10KOhm
R2248 1KOhm 1%
T2216
T2203
T2202
R2249 10KOhm
T2220
T2219
BT_LED
R2252 10KOhm
T2206
T2215
T2207
RX2234 0Ohm
T2201
T2210
T2208
T2218
RX2235 0Ohm
RX2225 0Ohm
RX2212 10KOhm
RX2254 1KOhm
RX2223 0Ohm
T2217
T2212
T2213
T2211
T2214
PM_RI#
PM_RSMRST#
PM_SYNC#
EXT_SCI#
STP_PCI#
STP_CPU#
PM_CLKRUN#
PCIE_WAKE#
INT_SERIRQ
PM_THERM#
VR_PWRGD_CLKEN
EXT_SMI#
CB_SD#
WLAN_LED
SB_CPPE#
BT_ON
BT_DET#
CLK_SATA_REQ#
PCB_ID1
PCB_ID2
SB_SPKR
MCH_SYNC#
PM_PWROK_R
PM_DPRSLPVR_ICH
BAT_LL#
PM_PWRBTN_ICH
LAN_RST#
RSMRST#_ICH
CLK_PWRGD_ICH
CL_CLK0
CL_DATA0
CL_VREF0
CL_RST#0
WLAN_ON
RTLAN_DSM#
UWB_ON
CLK_ICH14
CLK_USB48
PM_SUSB#
PM_SUSC#
PM_DPRSLPVR
PM_PWRBTN#
PM_RSMRST#
CLK_PWRGD
PCI_INTF#
PM_CLKRUN#
PCI_INTC#
PCI_INTA#
PCI_DEVSEL#
PCI_SERR#
PCI_TRDY#
PCI_FRAME#
PCI_REQ#3
PCI_LOCK#
PCI_REQ#0
PCI_REQ#1
PCI_REQ#2
PCI_PERR#
PCI_INTE#
PCI_INTD#
PCI_IRDY#
PCI_STOP#
PCI_INTB#
PCI_INTG#
PCI_INTH#
RP2202A
RP2202B
RP2202C
RP2202D
RP2202E
RP2202F
RP2202G
RP2202H
RP2203A
RP2203B
RP2203C
RP2203D
RP2203E
RP2203F
RP2203G
RP2203H
RP2204A
RP2204B
RP2204C
RP2204D
RP2204E
RP2204F
RP2204G
RP2204H
8.2KOhm
R2251 10KOhm
R2222 10KOhm
R2223 10KOhm
R2229 10KOhm
R2230 10KOhm
RX2230 1KOhm
R2231 10KOhm
R1.1
D2202
D2203
BAT54C
SUS_PWRGD
D2201 RB520S-30
U2201
RN5VD30AA-TR-F
RN2201A 10KOhm
RN2201B 10KOhm
RN2201C 10KOhm
RN2201D 10KOhm
R2220 2.2KOhm
R2221 2.2KOhm
R2204 8.2KOhm
R2247 10KOhm
R2213 10KOhm
R2214 10KOhm
R2217 10KOhm
R2215 10KOhm
R2216 10KOhm
R2218 10KOhm
PCB_ID0
PCB_ID1
PCB_ID2
14"/15" L
13" H
R2210 3.24KOhm 1%
C2202 0.1UF/10V
R2226 453Ohm 1%
R2232 10KOhm
RX2233 1KOhm
R2224 100KOhm
Q2206 2N7002E-T1-E3
EC_CLK_EN
CLK_EN#
R2233 10KOhm
Q2208B UM6K1N
Q2208A UM6K1N
CL_VREF0 ~= 0.405 V
CL_VREF0 routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out: 5 mils on 5 mils for 300 mils max
PEGATRON
Title : SB-ICH9M(3)
Engineer: Peter Lo
Size Custom
Project Name Rocky30
Rev 1.1
Date: Monday, February 04, 2008
Sheet 22 of 94


6uA in G3
U2001F
+VCC_RTC
C2310
C2311
0.1UF/16V
R2319
100Ohm
2mA
+5VS
+3VS
D2301
BAT54A
C2301
1UF/10V
+5VREFSUS
+V5REF_ICH
+3VSUS
BAT54A
D2302
2mA
R2320 10Ohm
+5VSUS
C2302
0.1UF/16V
646mA
L2304
80Ohm/100Mhz
+1.5VS
+1.5VS_PCIE_ICH
ESR=35mOhm/Ir=1400mA
CE2301
100UF/4V
C2305
22UF/6.3V
C2306
22UF/6.3V
C2307
2.2UF/6.3V
47mA
L2301
80Ohm/100Mhz
+VCCSATAPLL_ICH
C2321
10UF/6.3V
C2327
1UF/6.3V
+VCC1_5_ICH
R2307
0Ohm
1.342*5/6=1.12A
C2324
1UF/6.3V
C2328
1UF/6.3V
+VCCUSBPLL_ICH
R2311
0Ohm
1.342A*1/6+0.011=0.24A
C2333
0.1UF/10V
C2309
0.1UF/10V
78mA
+3VM_VCCPAUX
R2312
0Ohm
C2335
0.1UF/10V
C2342
VCCLAN1_05
0.1UF/10V
23mA
L2302
120Ohm/100MHZ
C2336
10UF/6.3V
C2337
2.2UF/6.3V
+VCCGLANPLL_ICH
80mA
R2301
0Ohm
+VCCGLAN1_5_ICH
C2338
4.7UF/10V
1mA
R2304
0Ohm
+VCCGLAN3_3_ICH
ICH9M
1.634A
C2303
C2304
0.1UF/16V
CE2302
100UF/6.3V
+VCCP_ICH
JP2301
2MM_OPEN_5MIL
+VCCP
+VCCDMIPLL_ICH
L2303
80Ohm/100Mhz
+1.5VS
C2312
10UF/6.3V
C2313
0.01UF/16V
23mA
+VCCDMI_ICH
L2305
80Ohm/100Mhz
C2322
4.7UF/10V
48mA
+VCPUIO_ICH
C2317
C2316
C2315
4.7UF/10V
R2318
0Ohm
2mA
+VCC3_3_ICH1
R2315
0Ohm
C2319
0.1UF/16V
+VCC3_3_ICH2
R2316
0Ohm
C2318
0.1UF/16V
+VCC3_3_ICH3
R2306
0Ohm
C2320
0.1UF/16V
+3VS
308mA
+VCC3_3_PCI
C2323
C2325
C2326
0.1UF/16V
R2314
0Ohm
+VCCHDA_ICH
0Ohm R2308
C2329
0.1UF/16V
11mA
+VCCSUSHDA_ICH
R2309
0Ohm
C2330
0.1UF/16V
11mA
TP_VCCSUS1_05_1
TP_VCCSUS1_05_2
TP_VCCSUS1_5
T2304
T2306
T2305
VCCSUS1_5
C2340
0.1UF/10V
+3VSUS_ICH_1
R2317
0Ohm
212mA
+3VSUS_ICH
R2310
0Ohm
+3VSUS
C2332
C2334
C2331
0.01UF/16V
0.01UF/16V
0.1UF/16V
VCCCL1_05
C2343
0.1UF/10V
C2308
1UF/6.3V
C2339
0.1UF/16V
73mA
+3VM_ICH_CL
R2313
0Ohm
+3VS
U2001E
ICH9M
PEGATRON
Title : SB-ICH9M(PWR)
Engineer: Peter Lo
Size
Custom
Project Name
Rocky30
Rev
1.1
Date: Saturday, January 26, 2008
Sheet 23 of 94

ICH9-M



ICH9M

NEWCARD,WLAN

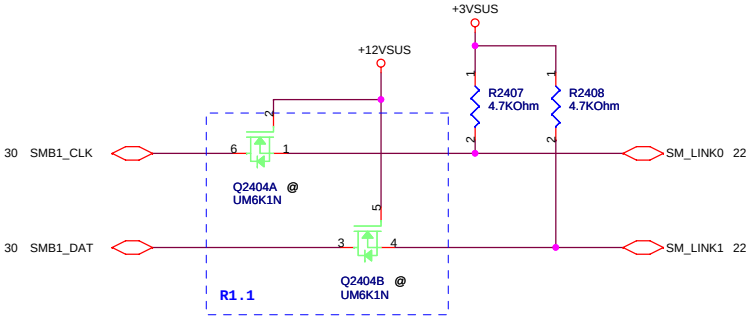
CLOCK GEN
SO-DIMM0 , SO-DIMM1

NEWCARD,WLAN

CLOCK GEN
SO-DIMM0 , SO-DIMM1

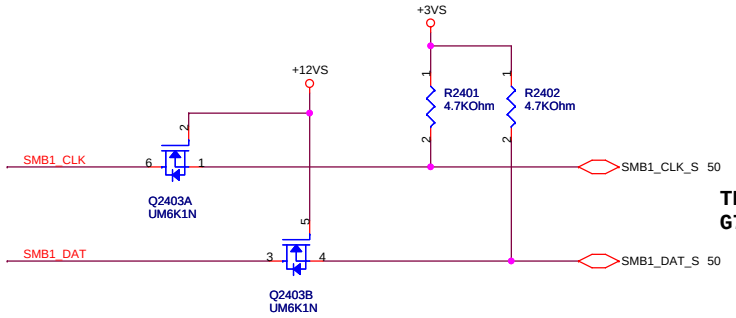
EC

Don't support iAMT
Remove ME-EC SMBus.



EC

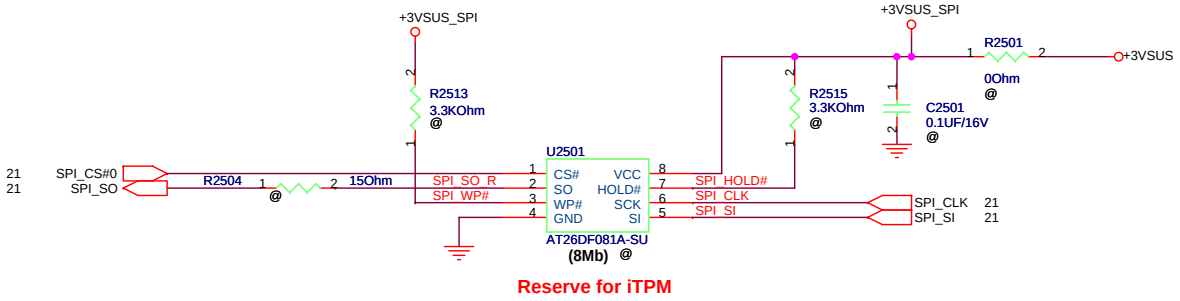
SB



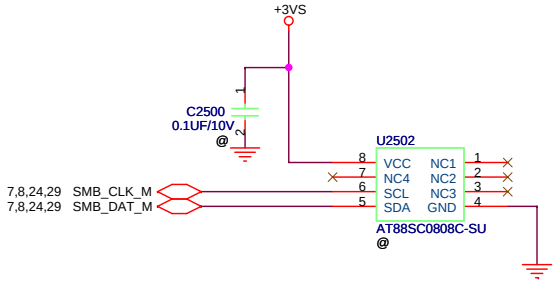
EC

THERMAL IC
G781,G781-1

PEGATRON	Title : ICH9M-Other	
	Engineer: Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.1
Date: Monday, February 04, 2008	Sheet 24 of 94	



Reserve for iTPM



PEGATRON **Title :** SPI ROM

Engineer: *Peter Lo*

Size	Project Name	Rev
B	Rocky30	1.1

Date: Monday, February 04, 2008 Sheet 25 of 94

PEGATRON Title :

Engineer: *Peter Lo*

Size	Project Name	Rev
A	**Rocky30**	1.1

Date: Saturday, January 26, 2008 Sheet 26 of 94

PEGATRON Title :

Engineer: *Peter Lo*

Size	Project Name	Rev
A	**Rocky30**	1.1

Date: Saturday, January 26, 2008 Sheet 27 of 94

PEGATRON Title :

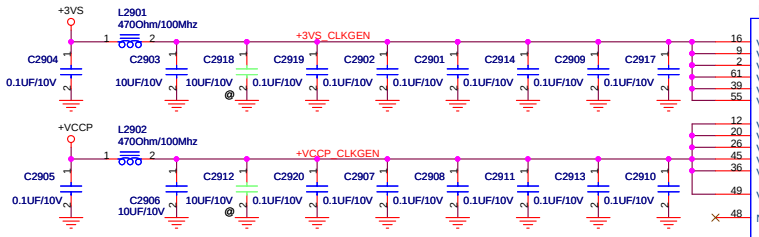
Engineer: *Peter Lo*

Size	Project Name	Rev
A	**Rocky30**	1.1

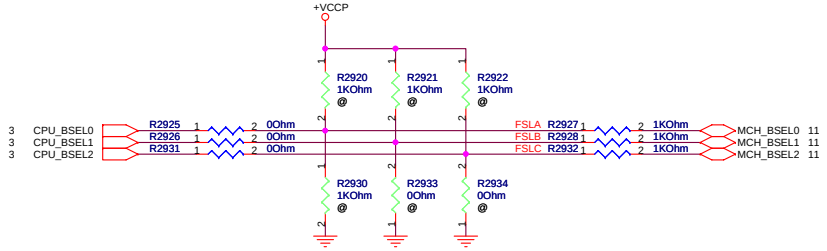
Date: Saturday, January 26, 2008 Sheet 28 of 94

+VCCP +VCCP 5,10,11,13,14,20,23,80,82

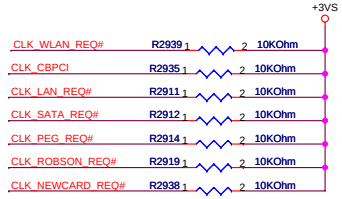
+3VS +3VS 3,7,8,11,14,15,20,22,23,24,25,30,31,40,41,45,46,48,50,51,53,54,57,58,59,61,70,74,75,91,92



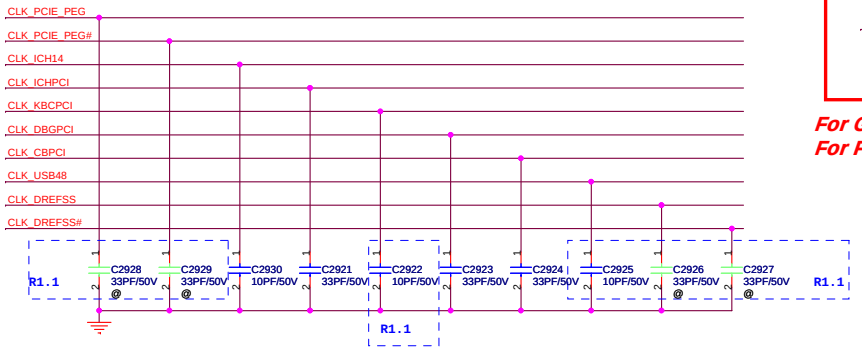
C2917,C2918,C2919 near CLK Gen.



	FSLC	FSLB	FSLA
BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0



C2921, C2922, C2923, C2924, C2925, C2926, C2927, C2928, C2929, C2930 near CLK Gen.

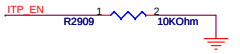


CR#_A	0 = SRC 0 1 = SRC 2	SATA
CR#_B	0 = SRC 1 1 = SRC 4	MCH
CR#_C	0 = SRC 0 1 = SRC 2	
CR#_D	0 = SRC 1 1 = SRC 4	
CR#_E	SRC 6	WLAN
CR#_F	SRC 8	LAN
CR#_G	SRC 9	New Card
CR#_H	SRC 10	Robson

Latched Input Select

0 = SRC 8
1 = CPU_ITP CLK

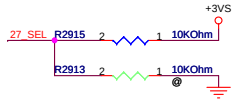
Decide pin 46,47



27_Select =0,
pin#13/14=DOT96;
pin#17/18=LCD_SST;

27_Select =1,
pin#13/14=SRC0;
pin#17/18=27MHz non-spread SE clock;

Decide pin 13/14,17/18



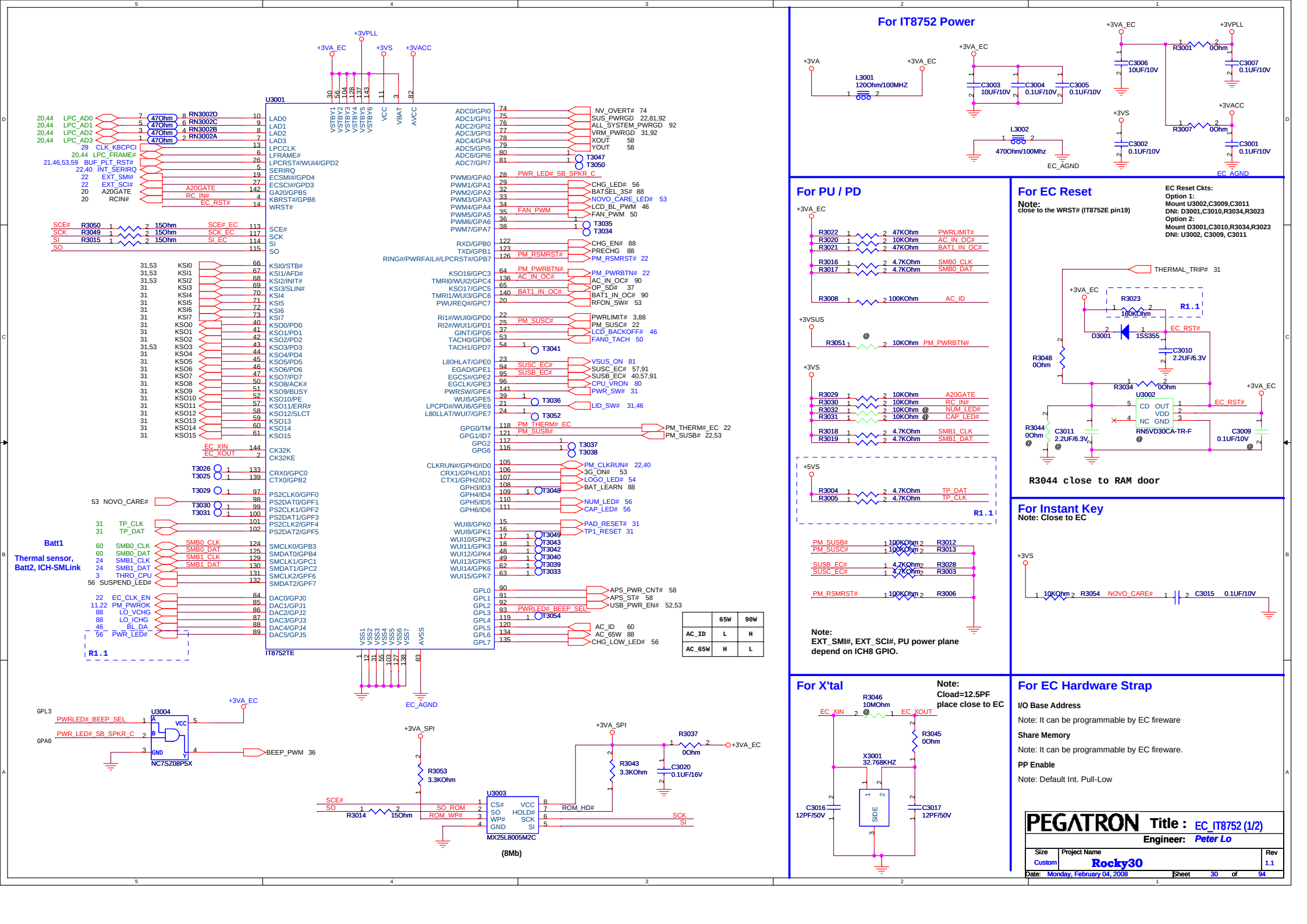
For GM/GL, need to PD for 96MHz output.
For PM, need to PU for 27MHz output.

PEGATRON Title : ICS9LPR365

Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.1

Date: Monday, February 04, 2008 Sheet 29 of 94



For IT8752 Power

For PU / PD

Note:
EXT_SMI#, EXT_SCI#, PU power plane depend on ICH8 GPIO.

For EC Reset

Note:
close to the WRST# (IT8752E pin19)

EC Reset Ckts:
Option 1:
Mount U3002,C3009,C3011
DNI: D3001,C3010,R3034,R3023
Option 2:
Mount D3001,C3010,R3034,R3023
DNI: U3002, C3009, C3011

R3044 close to RAM door

For Instant Key

Note: Close to EC

For X'tal

Note:
Cload=12.5PF
place close to EC

For EC Hardware Strap

I/O Base Address

Note: It can be programmable by EC fireware

Share Memory

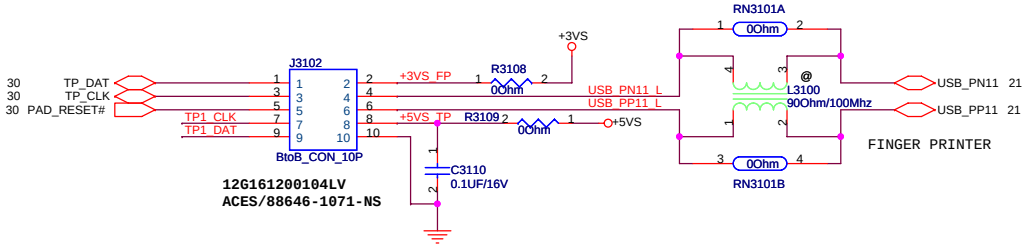
Note: It can be programmable by EC fireware.

PP Enable

Note: Default Int. Pull-Low

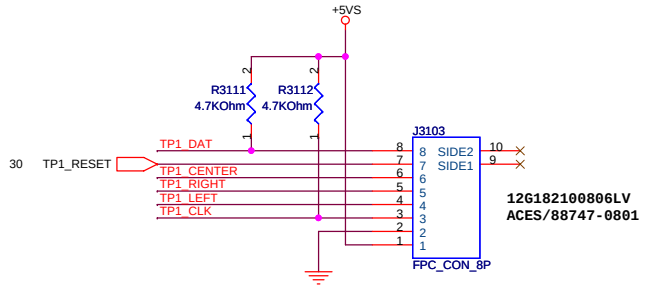
PEGATRON	Title : EC_IT8752 (1/2)	
	Engineer: Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.1
Date: Monday, February 04, 2008	Sheet 30 of 94	

TOUCH PAD CONN

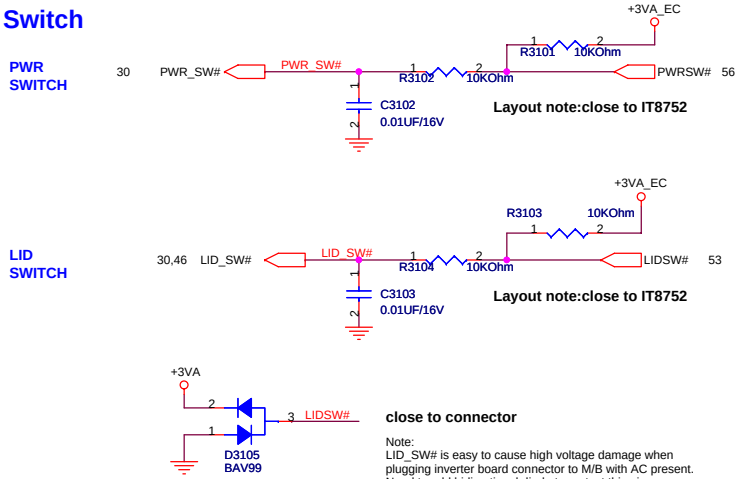


TP : Touch Pad
TP1: Track Point

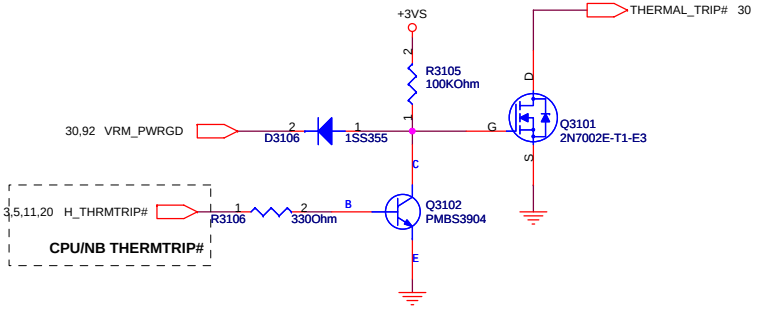
TRACK POINT CONN



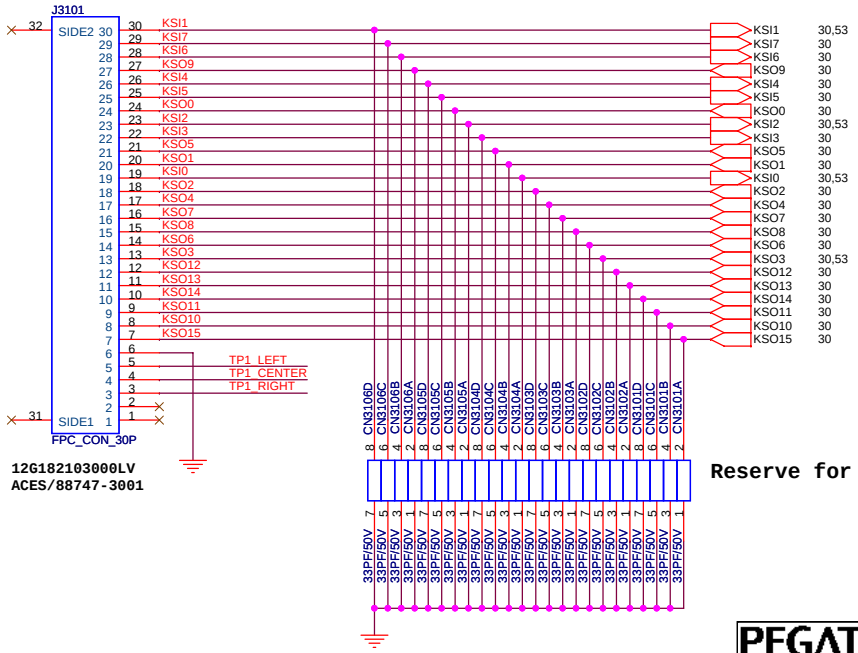
For Switch



For Thermal Control Method



Keyboard Connector



PEGATRON	Title : EC_IT8752 (2/2)	
	Engineer: Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.1
Date: Monday, February 04, 2008	Sheet 31 of 94	

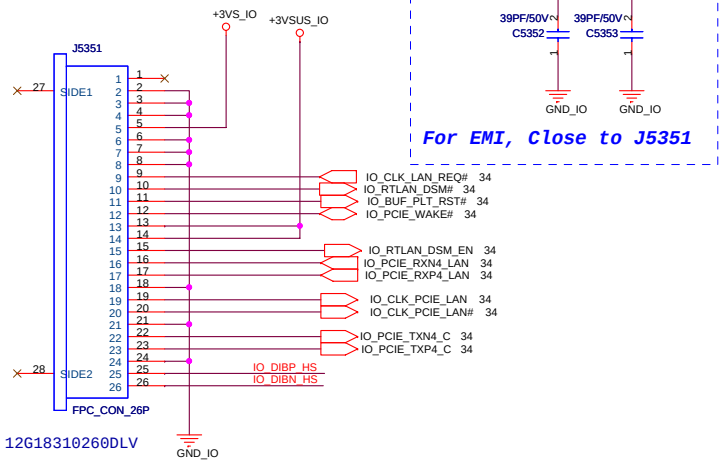
PEGATRON Title : **

Engineer: *Peter Lo*

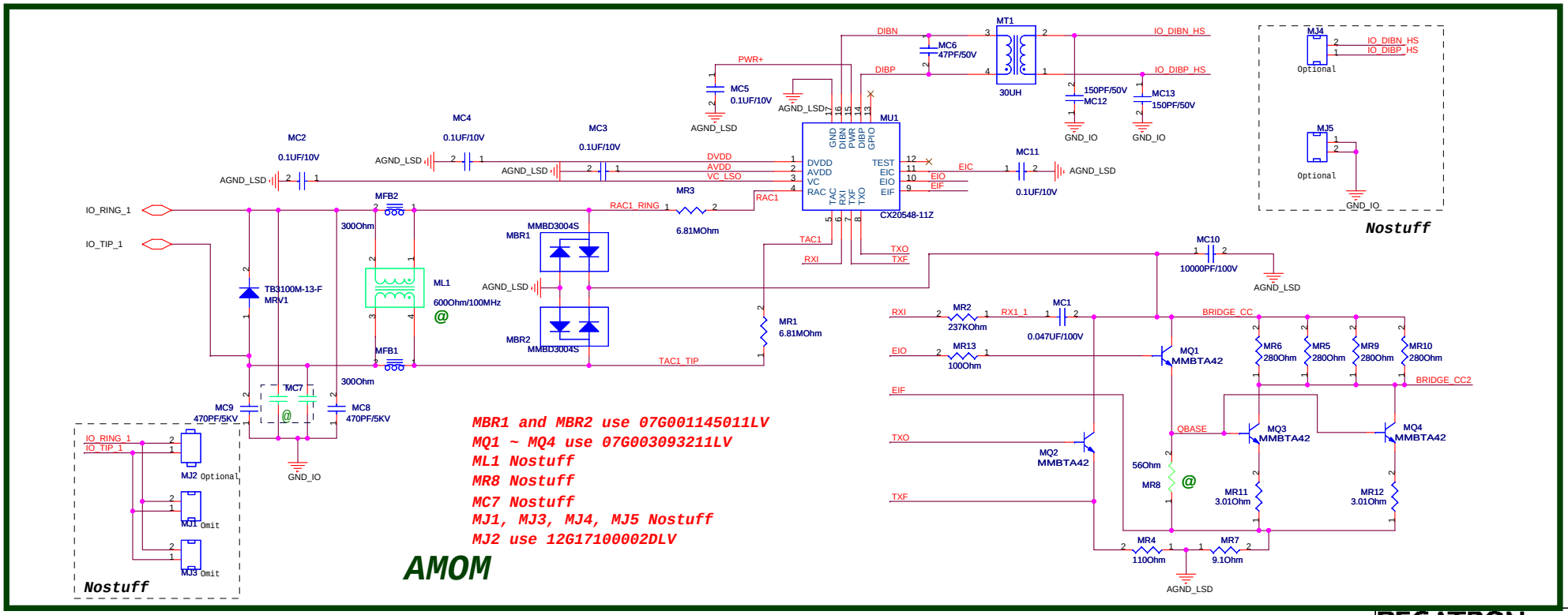
Size	Project Name	Rev
Custom	Rocky30	1.1

Date: Saturday, January 26, 2008 Sheet 32 of 94

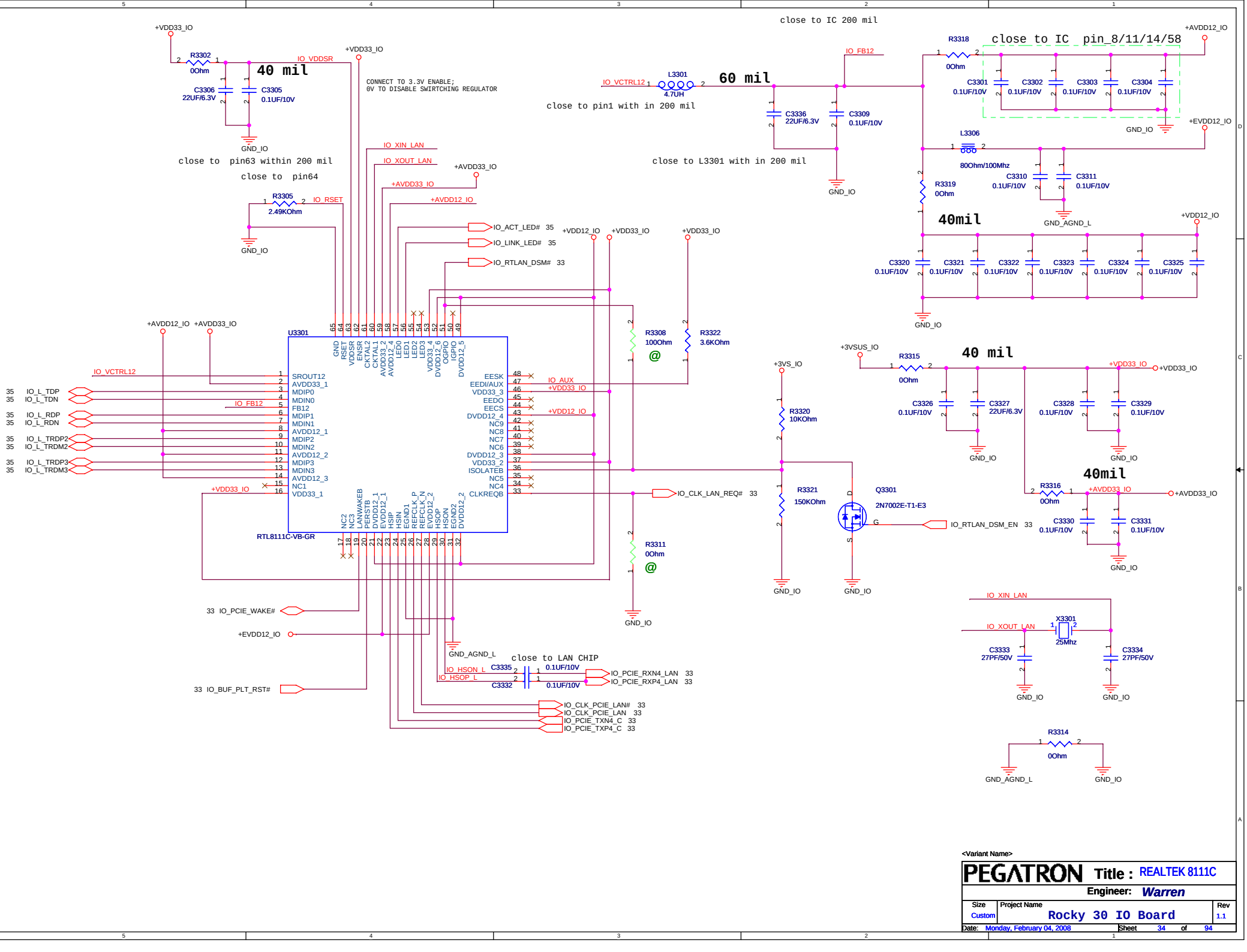
IO BOARD

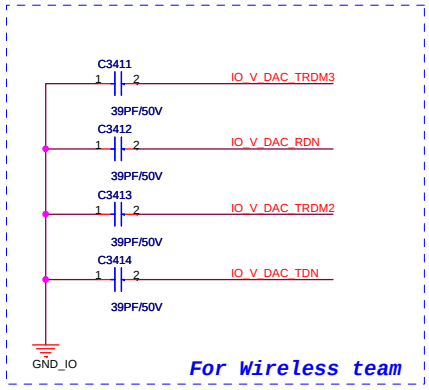


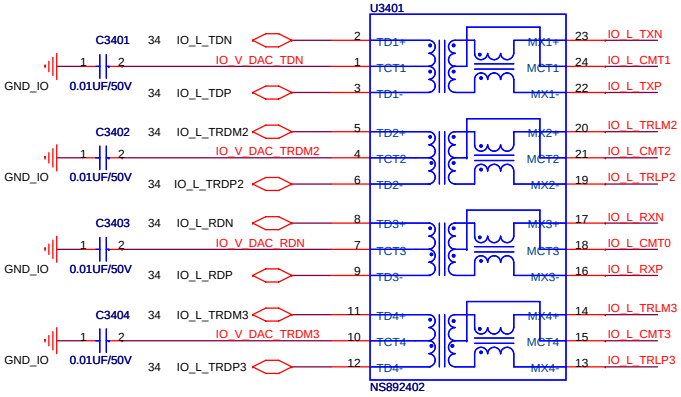
12G18310260DLV



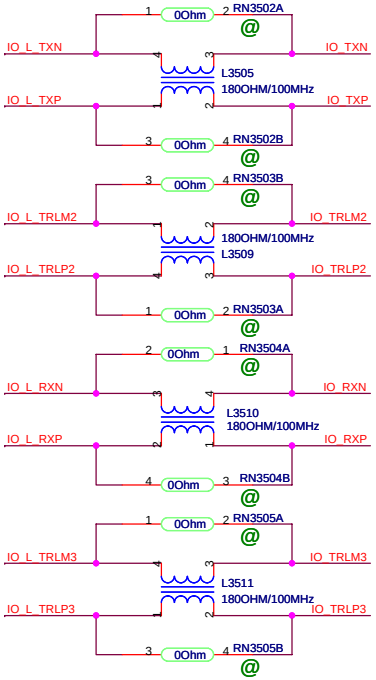
PEGATRON	Title : IO BRD CONN&DAA	
	Engineer: Warren	
Size: Custom	Project Name: Rocky 30 IO Board	Rev: 1.1
Date: Monday, February 04, 2008	Sheet 33 of 94	

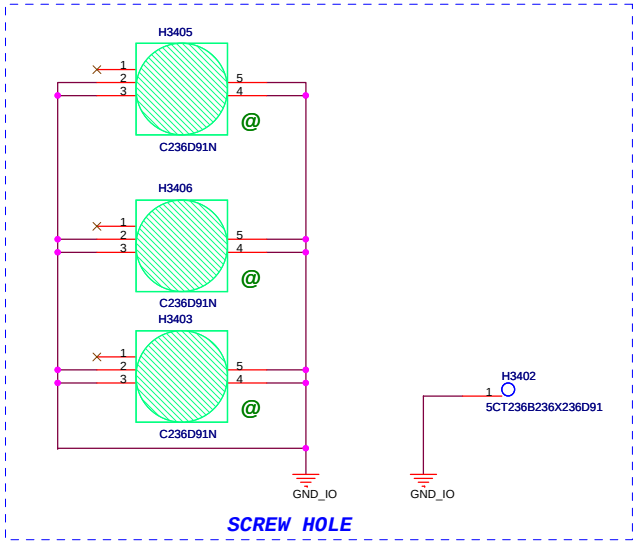

close to IC 200 mil
close to IC pin_8/11/14/58
close to pin1 with in 200 mil
close to L3301 with in 200 mil
close to pin63 within 200 mil
close to pin64
close to LAN CHIP
CONNECT TO 3.3V ENABLE;
0V TO DISABLE SWIRTCHING REGULATOR
40 mil
60 mil
40mil
RTL8111C-VB-GR
U3301
+VDD33_IO
+AVDD12_IO
+VDD12_IO
+EVDD12_IO
+3VS_IO
+3VSUS_IO
GND_IO
GND_AGND_L
IO_VCTRL12
IO_FB12
IO_XIN_LAN
IO_XOUT_LAN
IO_RSET
IO_AUX
IO_ACT_LED# 35
IO_LINK_LED# 35
IO_RTLAN_DSM# 33
IO_CLK_LAN_REQ# 33
IO_RTLAN_DSM_EN 33
33 IO_PCIE_WAKE#
33 IO_BUF_PLT_RST#
IO_HSON_L
IO_HSOP_L
IO_PCIE_RXN4_LAN 33
IO_PCIE_RXP4_LAN 33
IO_CLK_PCIE_LAN# 33
IO_CLK_PCIE_LAN 33
IO_PCIE_TXN4_C 33
IO_PCIE_TXP4_C 33
R3302 0Ohm
R3305 2.49KOhm
R3308 100Ohm @
R3322 3.6KOhm
R3311 0Ohm @
R3320 10KOhm
R3321 150KOhm
R3315 0Ohm
R3316 0Ohm
R3318 0Ohm
R3319 0Ohm
R3314 0Ohm
L3301 4.7UH
L3306 80Ohm/100Mhz
Q3301 2N7002E-T1-E3
X3301 25Mhz
C3306 22UF/6.3V
C3305 0.1UF/10V
C3336 22UF/6.3V
C3309 0.1UF/10V
C3301 0.1UF/10V
C3302 0.1UF/10V
C3303 0.1UF/10V
C3304 0.1UF/10V
C3310 0.1UF/10V
C3311 0.1UF/10V
C3320 0.1UF/10V
C3321 0.1UF/10V
C3322 0.1UF/10V
C3323 0.1UF/10V
C3324 0.1UF/10V
C3325 0.1UF/10V
C3326 0.1UF/10V
C3327 22UF/6.3V
C3328 0.1UF/10V
C3329 0.1UF/10V
C3330 0.1UF/10V
C3331 0.1UF/10V
C3333 27PF/50V
C3334 27PF/50V
C3335 0.1UF/10V
C3332 0.1UF/10V
SROUT12
AVDD33_1
MDIP0
MDIN0
FB12
MDIP1
MDIN1
AVDD12_1
MDIP2
MDIN2
AVDD12_2
MDIP3
MDIN3
AVDD12_3
NC1
VDD33_1
EESK
EEDI/AUX
VDD33_3
EEDO
EECS
DVDD12_4
NC9
NC8
NC7
NC6
DVDD12_3
VDD33_2
ISOLATEB
NC5
NC4
CLKREQB
GND
RSET
VDDSR
RXSR
CKTAL2
CKTAL1
AVDD33_2
AVDD12_4
LED0
LED1
LED2
LED3
VDD33_4
DVDD12_6
OGPIO
IGPIO
DVDD12_5
NC2
NC3
LANWAKEB
PERSTB
DVDD12_1
EVDD12_1
HSIP
HSIN
EGND1
REFCLK_P
REFCLK_N
EVDD12_2
HSOP
HSON
EGND2
DVDD12_2
Variant Name
PEGATRON
Title : REALTEK 8111C
Engineer: Warren
Size Custom
Project Name Rocky 30 IO Board
Rev 1.1
Date: Monday, February 04, 2008
Sheet 34 of 94

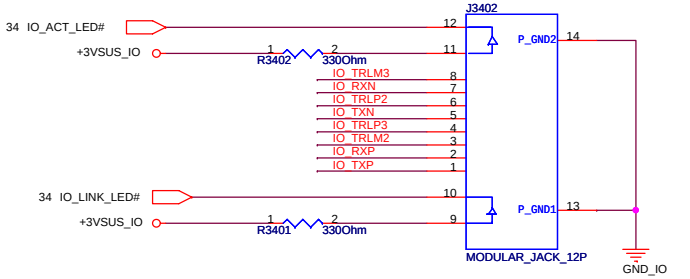




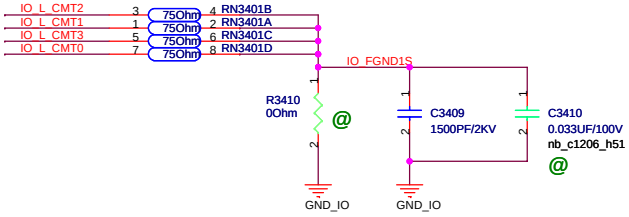
Transformer close CN3402

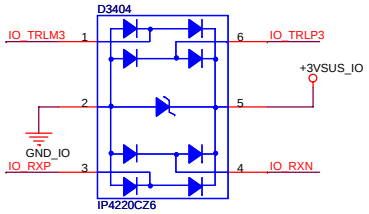


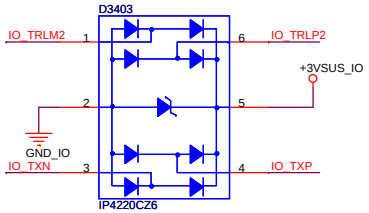




12G148301089LV
ALLTOP/C100Q2-10806-L







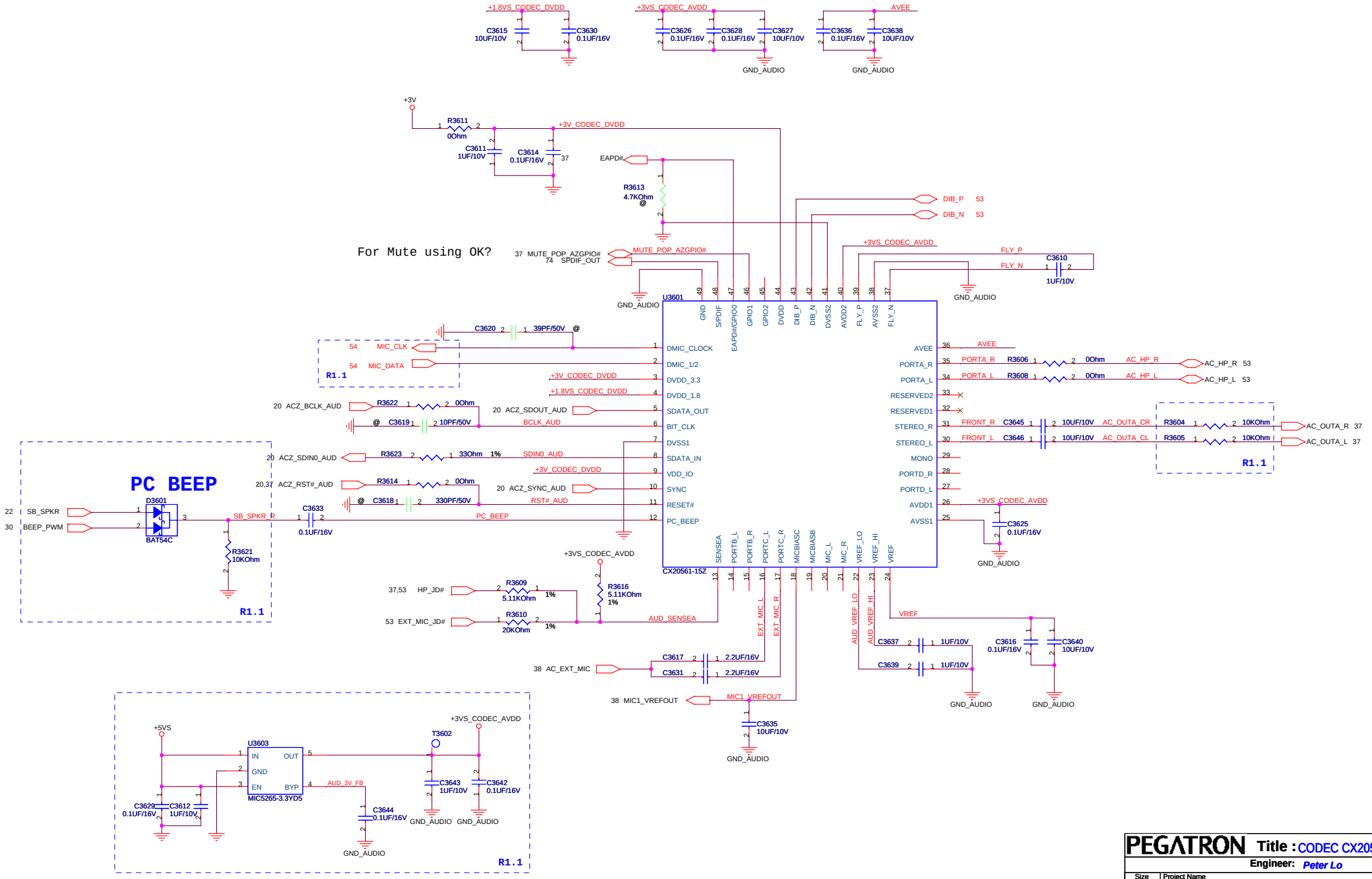
<Variant Name>

PEGATRON **Title :** LAN-RJ45

Engineer: *Warren*

Size	Project Name	Rev
Custom	Rocky 30 IO Board	1.1

Date: Monday, February 04, 2008 Sheet 35 of 94



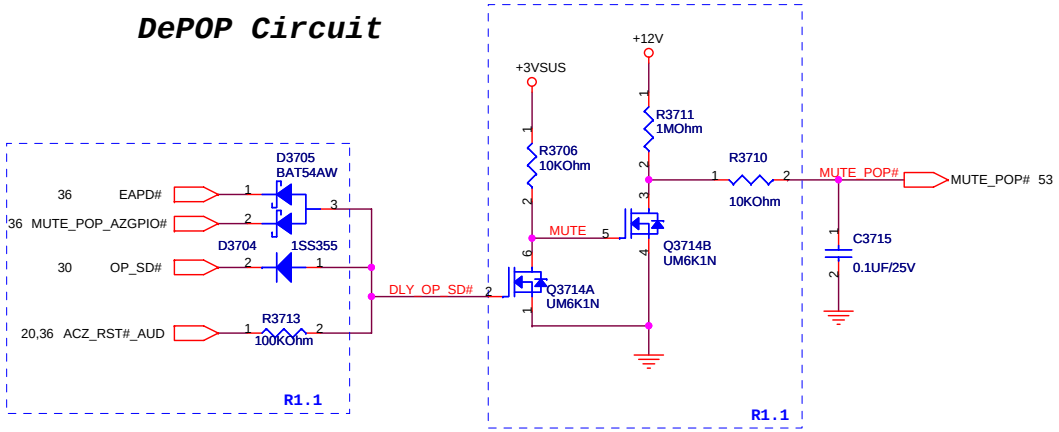
PEGATRON Title : CODEC CX20561

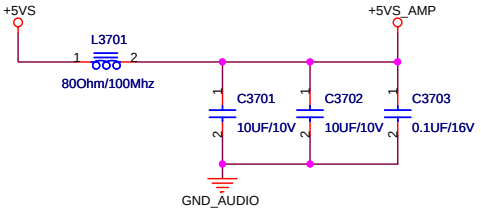
Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.1

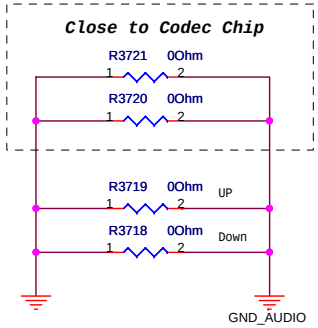
Date: Monday, February 04, 2008 Sheet 36 of 94

DePOP Circuit



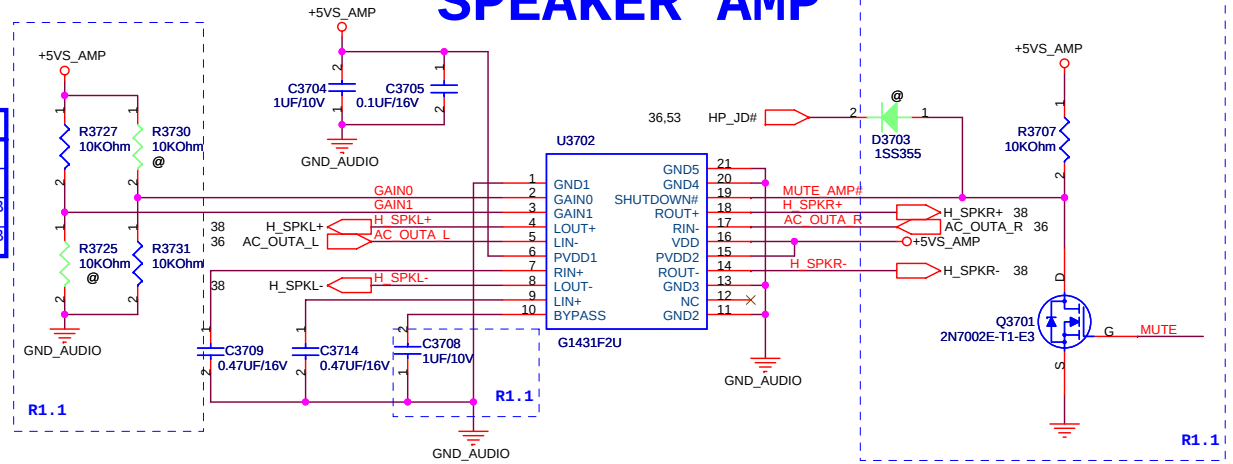


JACK GND



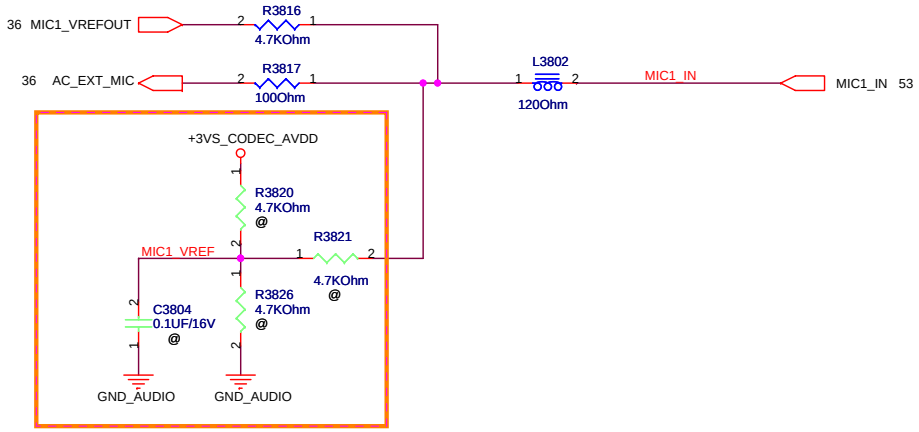
SPEAKER AMP

GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB



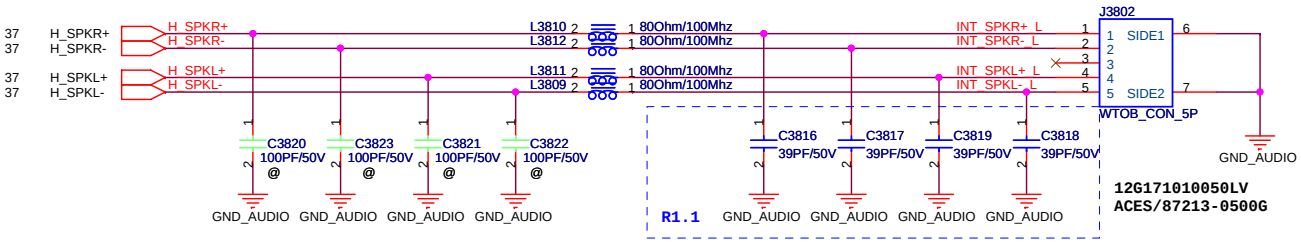
PEGATRON	Title : AUDIO AMP	
	Engineer: Peter Lo	
Size: B	Project Name: Rocky30	Rev: 1.1
Date: Monday, February 04, 2008	Sheet 37 of 94	

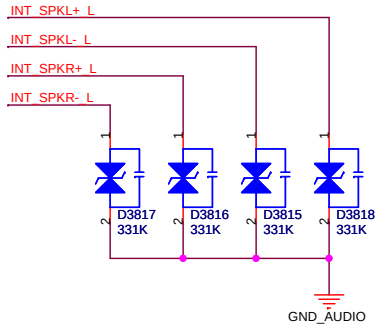
EXT MICROPHONE



Reserved the external MIC bias(T filter).

SPEAKER CONNECTOR





PEGATRON Title : MIC&LINEIN

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.1

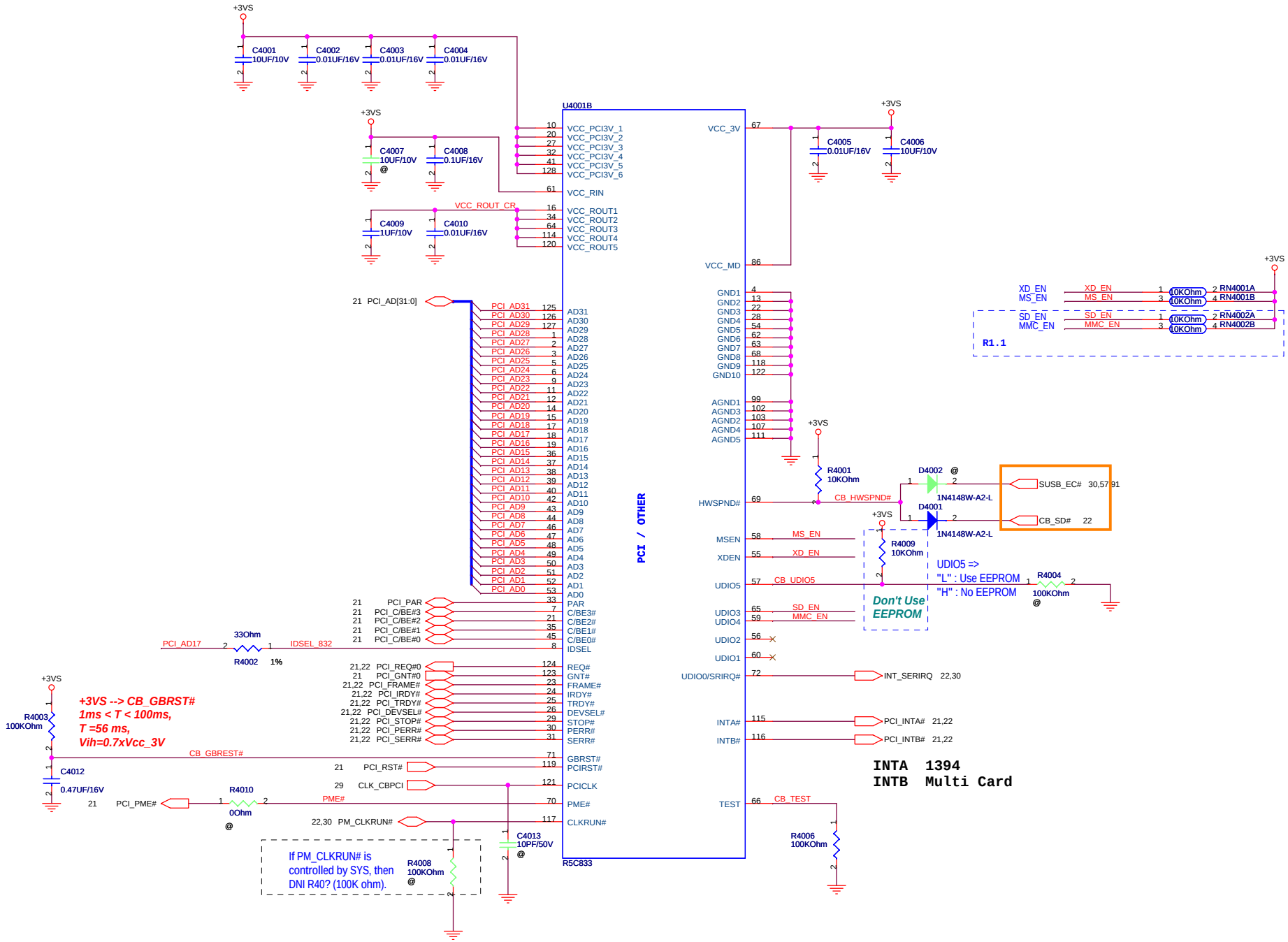
Date: Monday, February 04, 2008 Sheet 38 of 94

PEGATRON Title : FM2010 DSP

Engineer: *Peter Lo*

Size	Project Name	Rev
Custom	Rocky30	1.1

Date: Saturday, January 26, 2008 Sheet 39 of 94

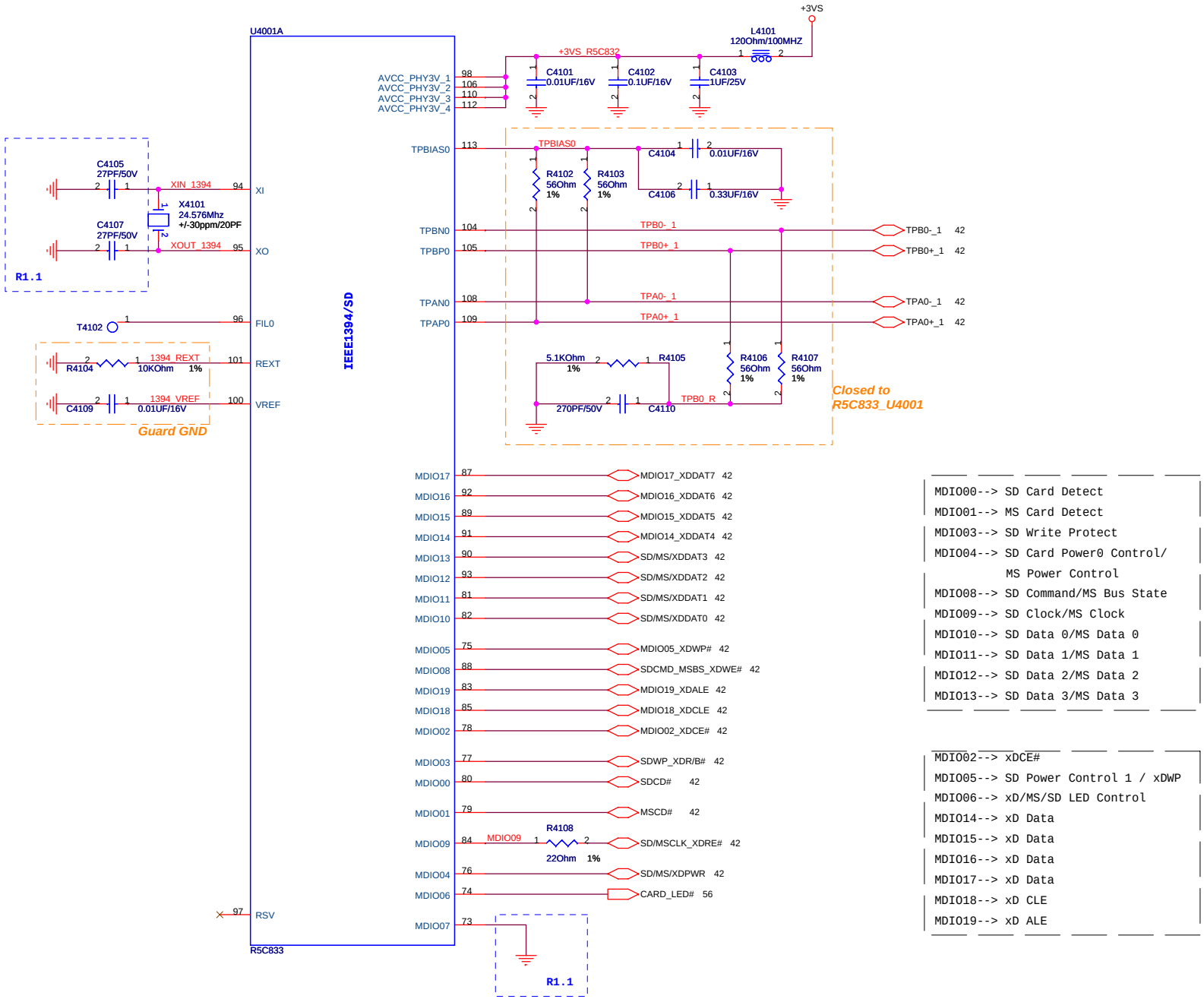


PEGATRON Title : CARDBUS R5C833 (1)

Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.1

Date: Monday, February 04, 2008 Sheet 40 of 94




```
MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
          MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3
```

```
MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE
```

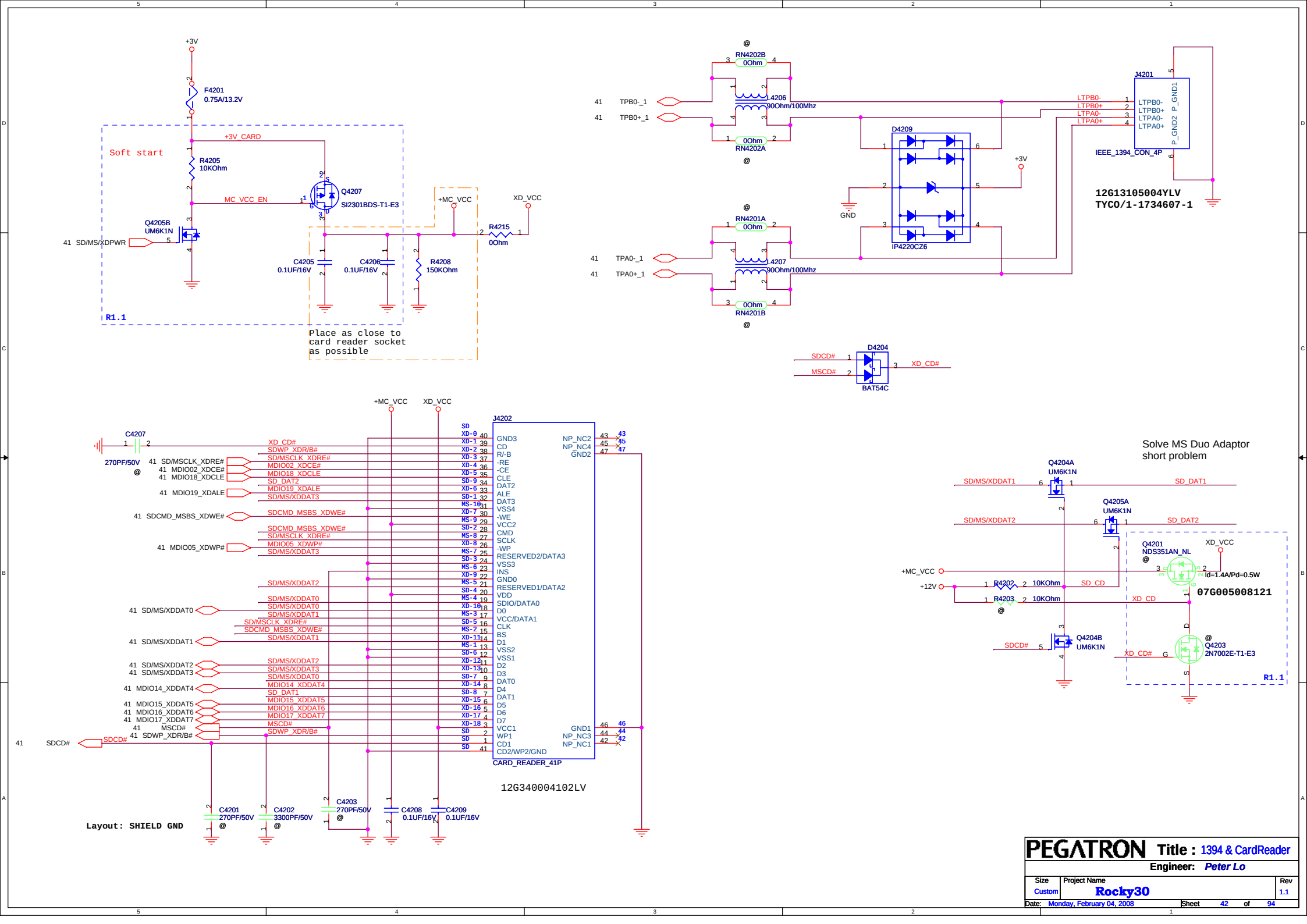
PEGATRON

Title : CARDBUS R5C833 (2)

Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.1

Date: Monday, February 04, 2008 Sheet 41 of 94



PEGATRON Title : 1394 & CardReader

Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.1

Date: Monday, February 04, 2008 Sheet 42 of 94

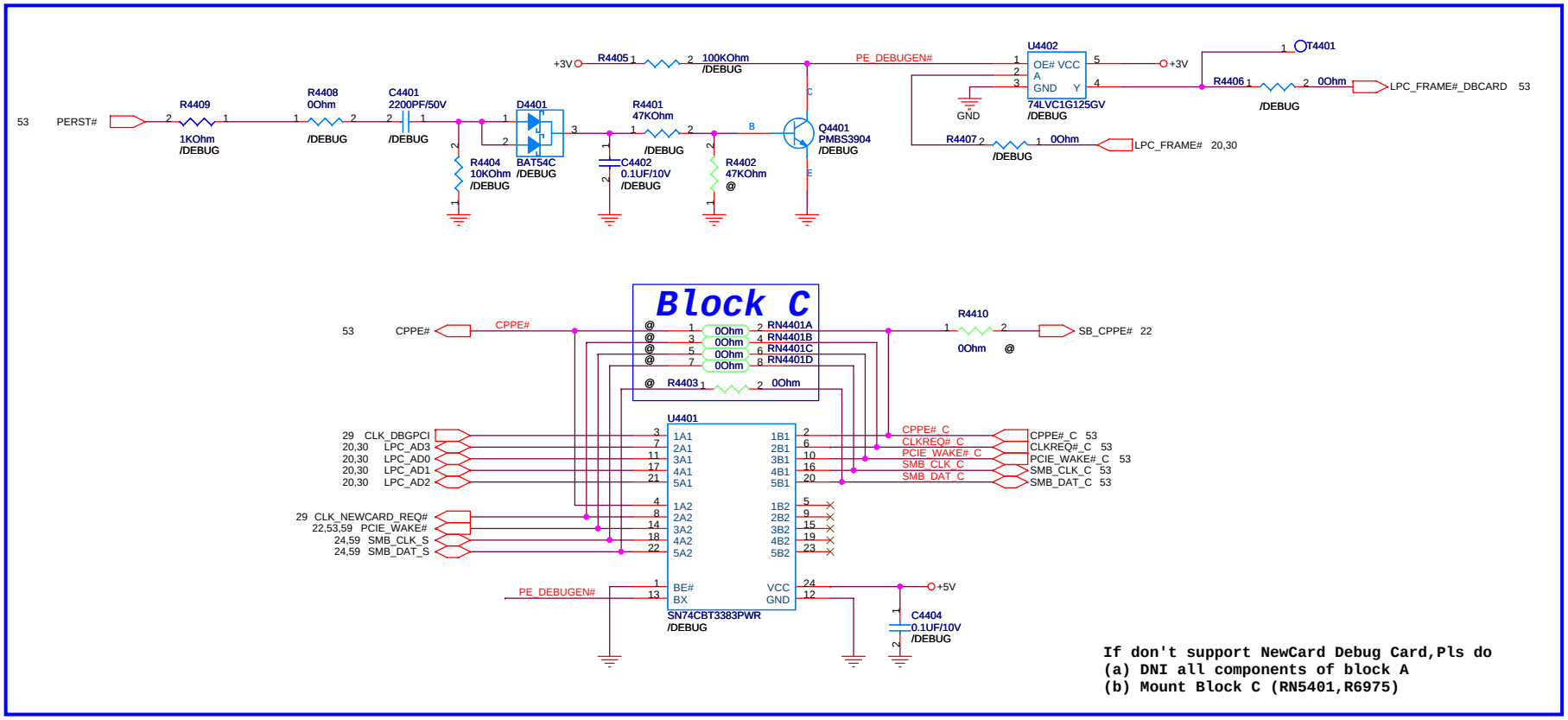
PEGATRON Title : *****

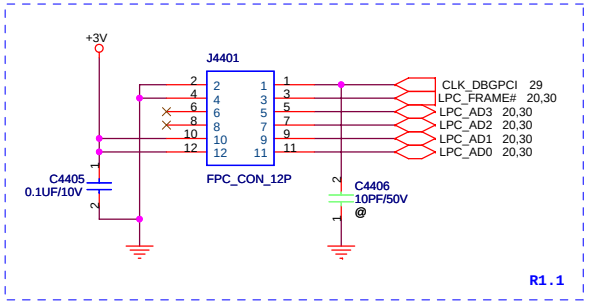
Engineer: *Peter Lo*

Size	Project Name	Rev
Custom	Rocky30	1.1

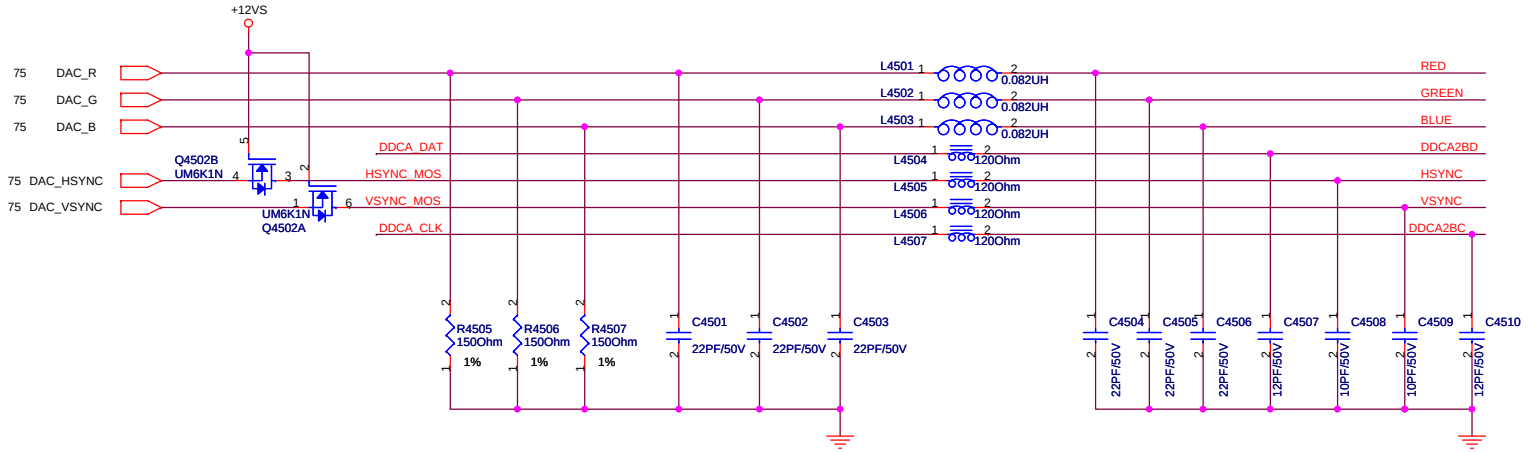
Date: Saturday, January 26, 2008 Sheet 43 of 94

Block A

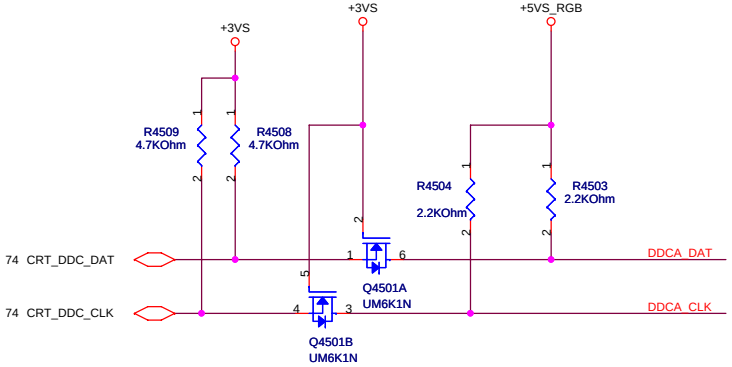


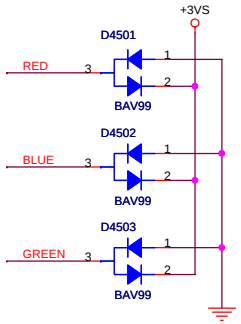


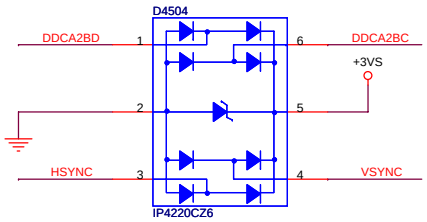
PEGATRON	Title : DEBUG	
	Engineer: Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.1
Date: Monday, February 04, 2008	Sheet 44 of 94	

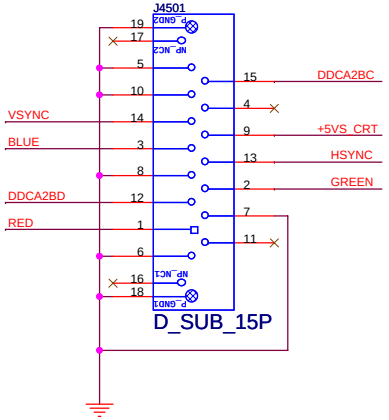


PLACE ESD Diodes near VGA port







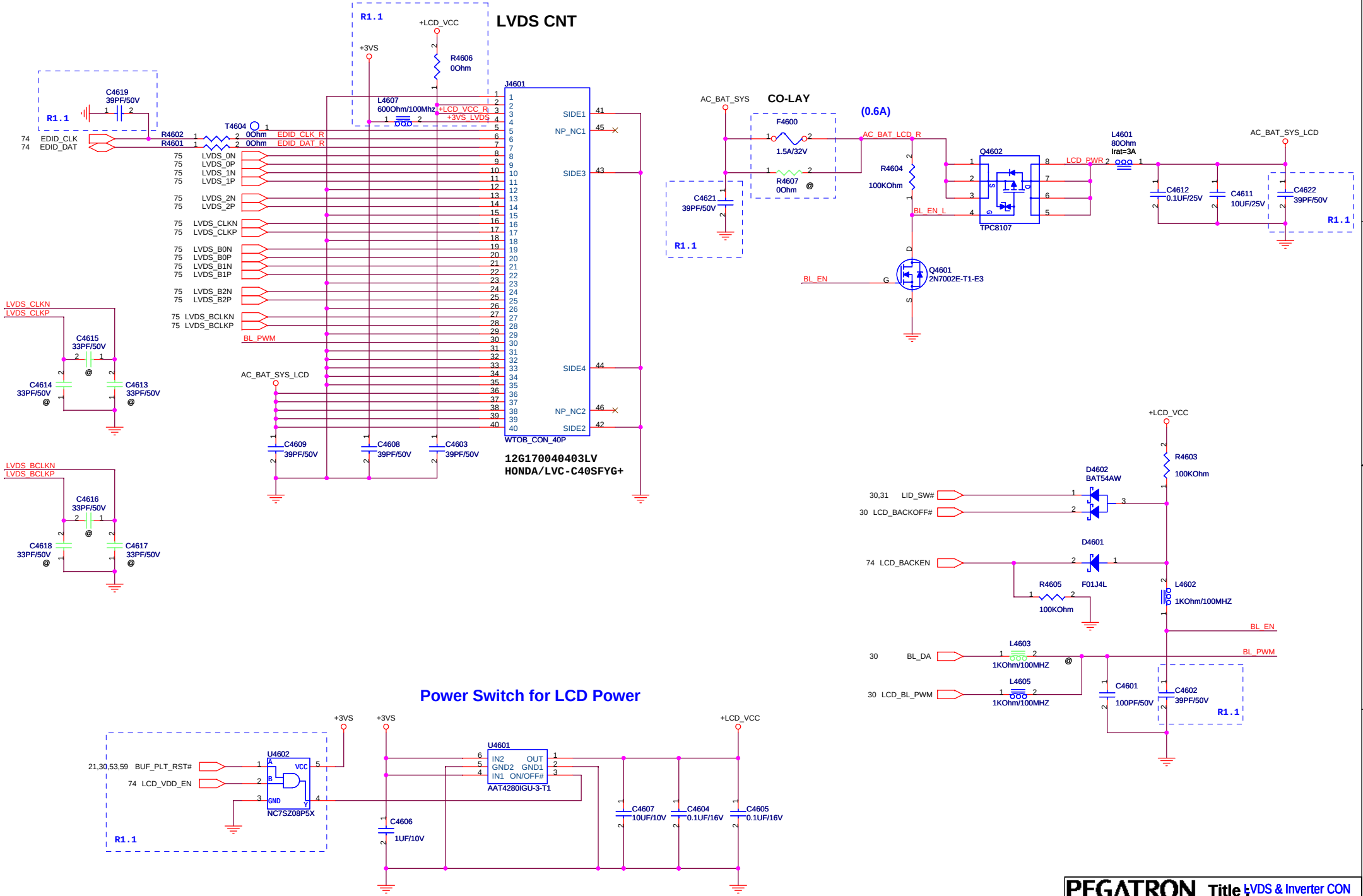


PEGATRON Title : CRT

Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.1

Date: Monday, February 04, 2008 Sheet 45 of 94



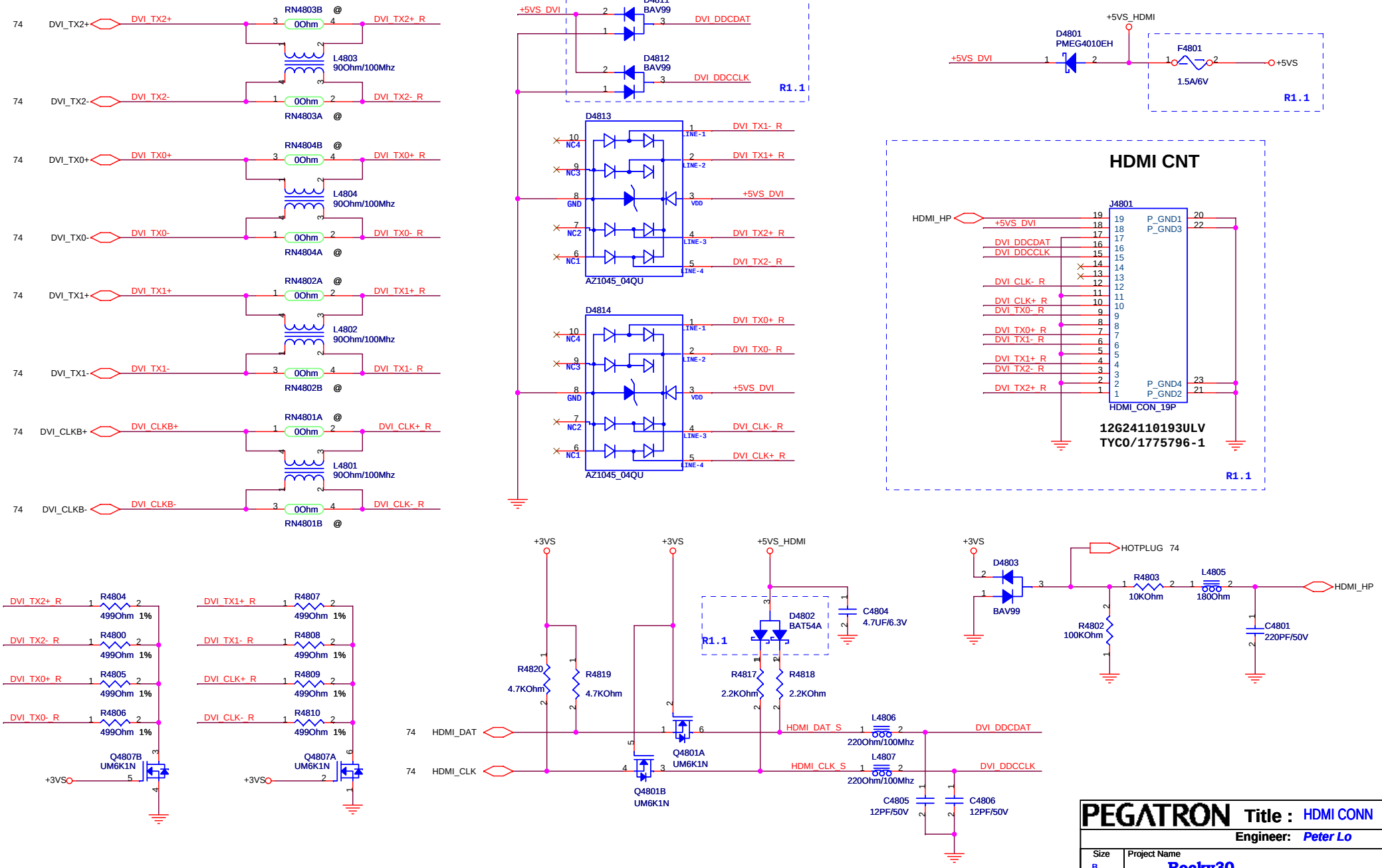
PEGATRON	Title: LVDS & Inverter CON	
	Engineer: Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.1
Date: Monday, February 04, 2008	Sheet 46 of 94	

PEGATRON Title : ***

Engineer: *Peter Lo*

Size	Project Name	Rev
C	Rocky30	1.1

Date: Saturday, January 26, 2008 Sheet 47 of 94



PEGATRON

Title : HDMI CONN

Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.1

Date: Monday, February 04, 2008 Sheet 48 of 94

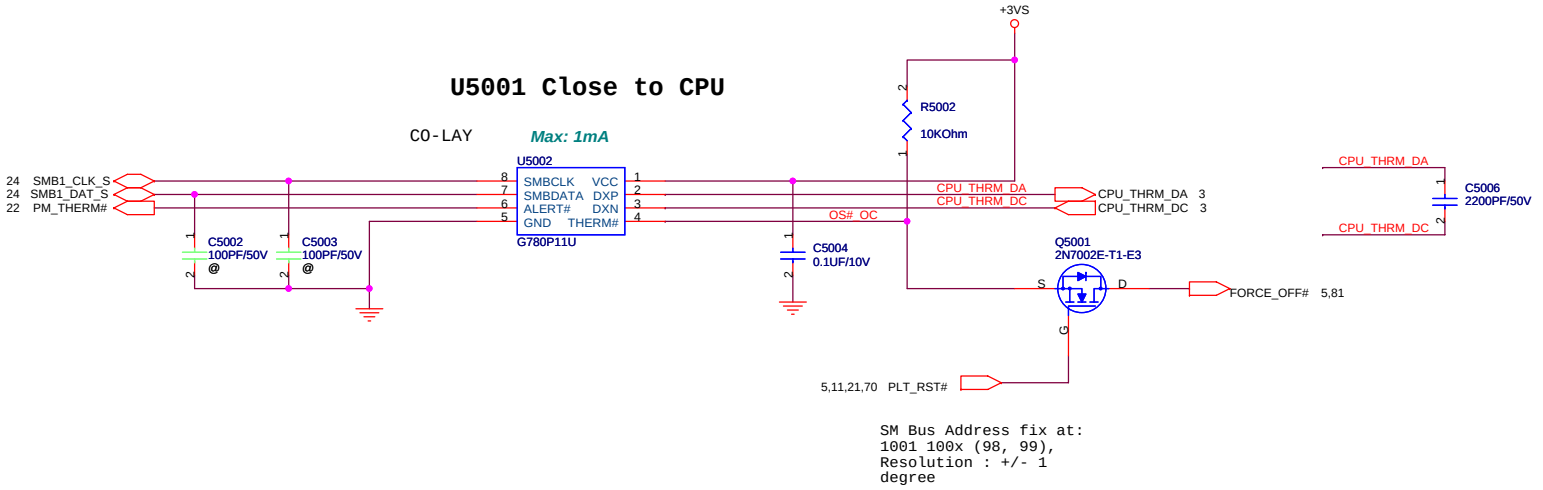
PEGATRON Title :

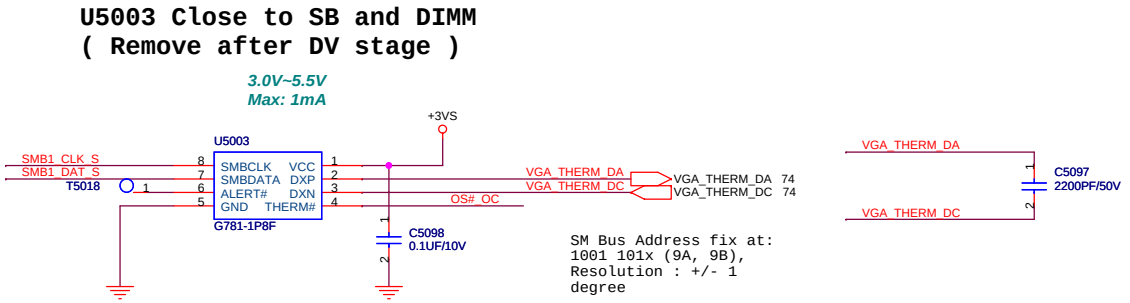
Engineer: *Peter Lo*

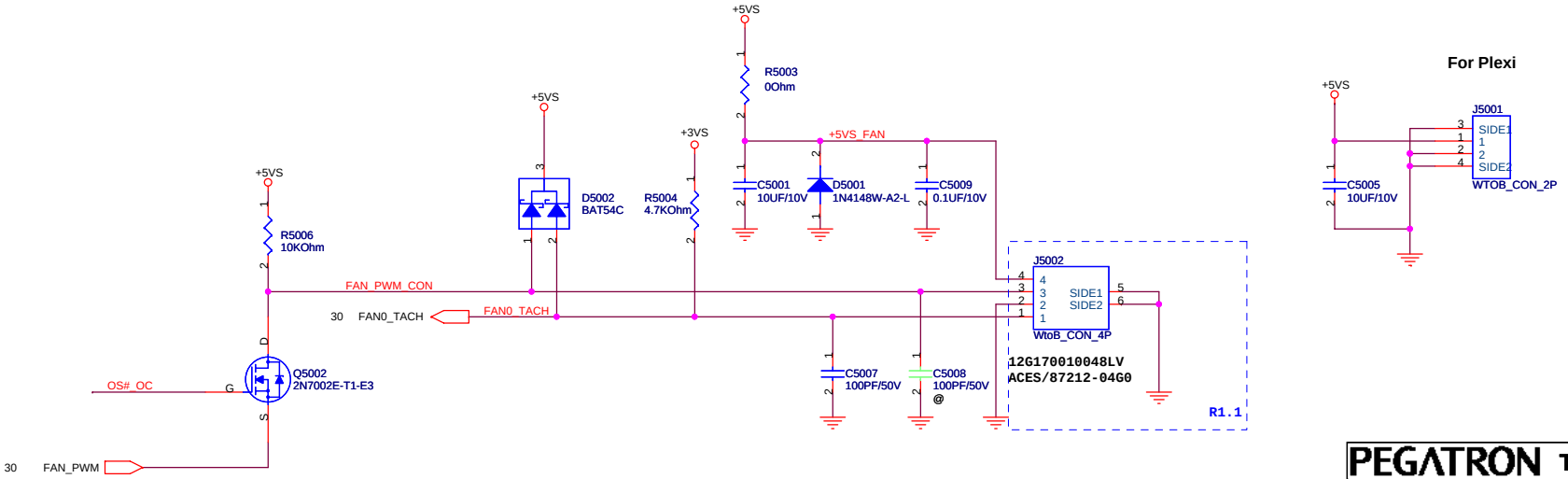
Size	Project Name	Rev
A	**Rocky30**	1.1

Date: Saturday, January 26, 2008 Sheet 49 of 94

Thermal Sensor

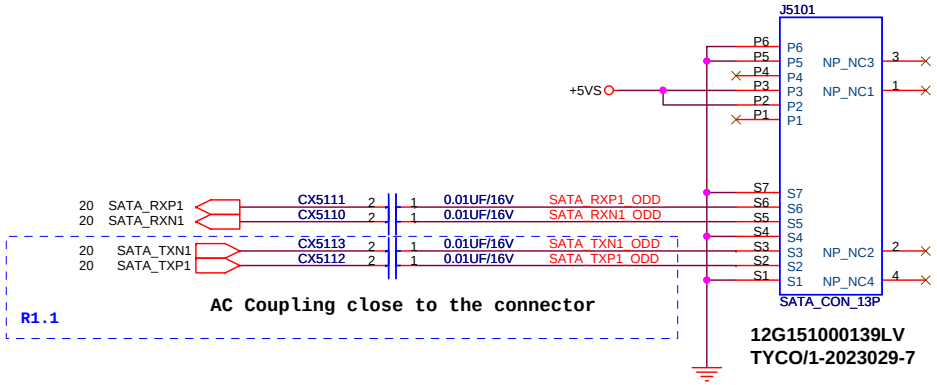




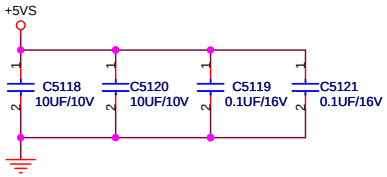


PEGATRON	Title : Thermal & Fan	
	Engineer: Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.1
Date: Monday, February 04, 2008	Sheet 50 of 94	

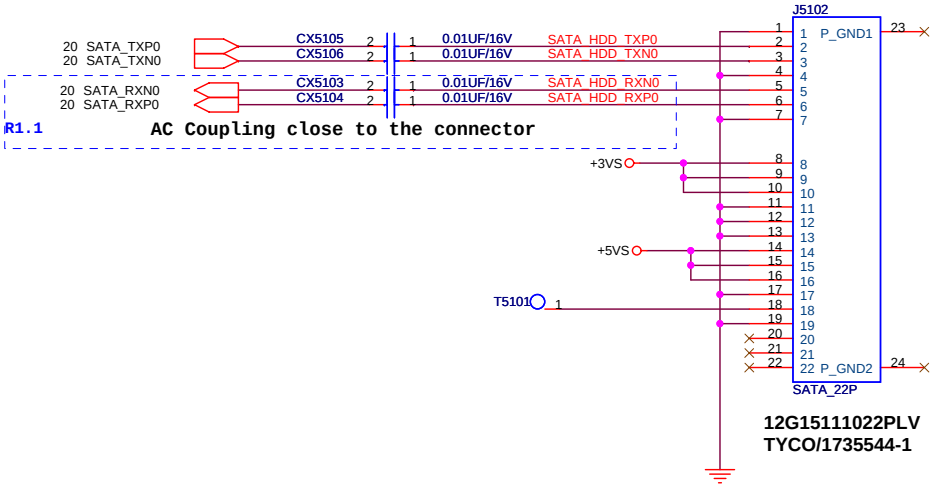
ODD CON



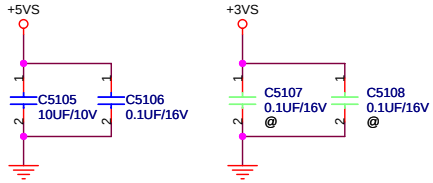
12G151000139LV
TYCO/1-2023029-7



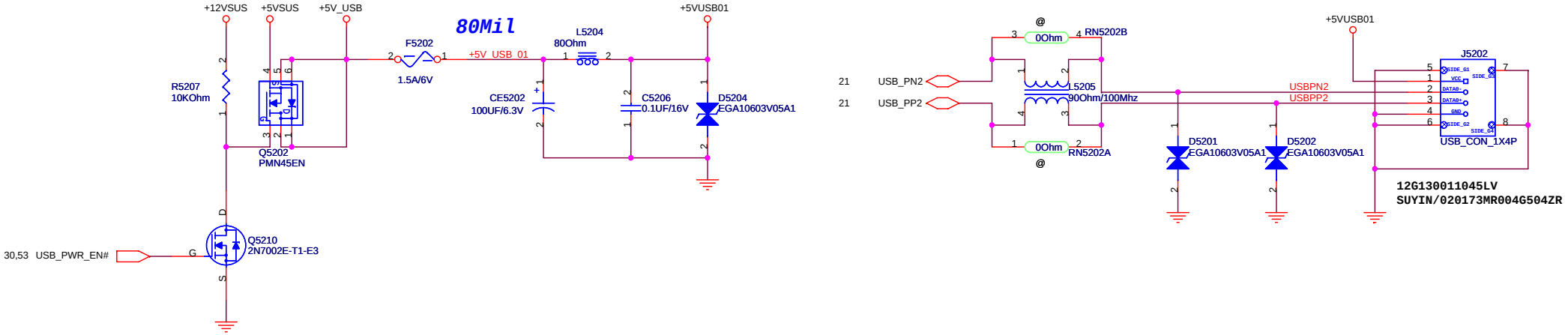
SATA HDD CON



12G15111022PLV
TYCO/1735544-1



PEGATRON	Title : Sata HDD & Swap Bay	
	Engineer: Peter Lo	
Size: B	Project Name: Rocky30	Rev: 1.1
Date: Monday, February 04, 2008	Sheet 51 of 94	



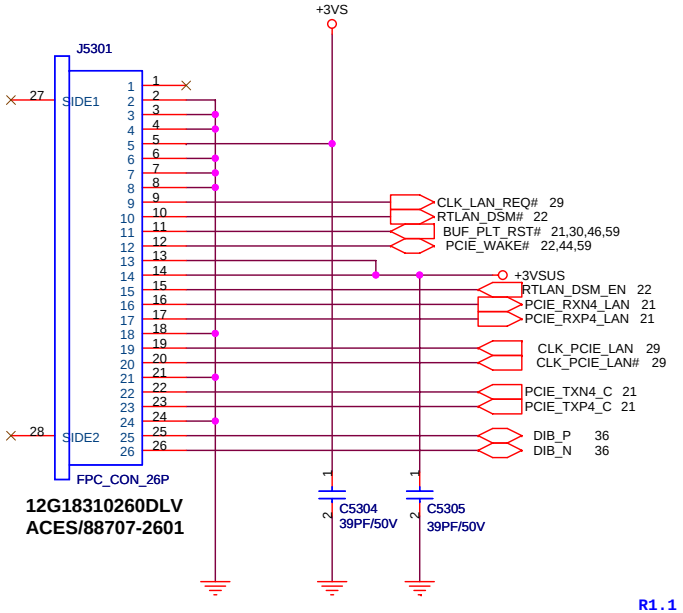
PEGATRON **Title :** USB CONN

Engineer: *Peter Lo*

Size	Project Name	Rev
B	Rocky30	1.1

Date: Monday, February 04, 2008 Sheet 52 of 94

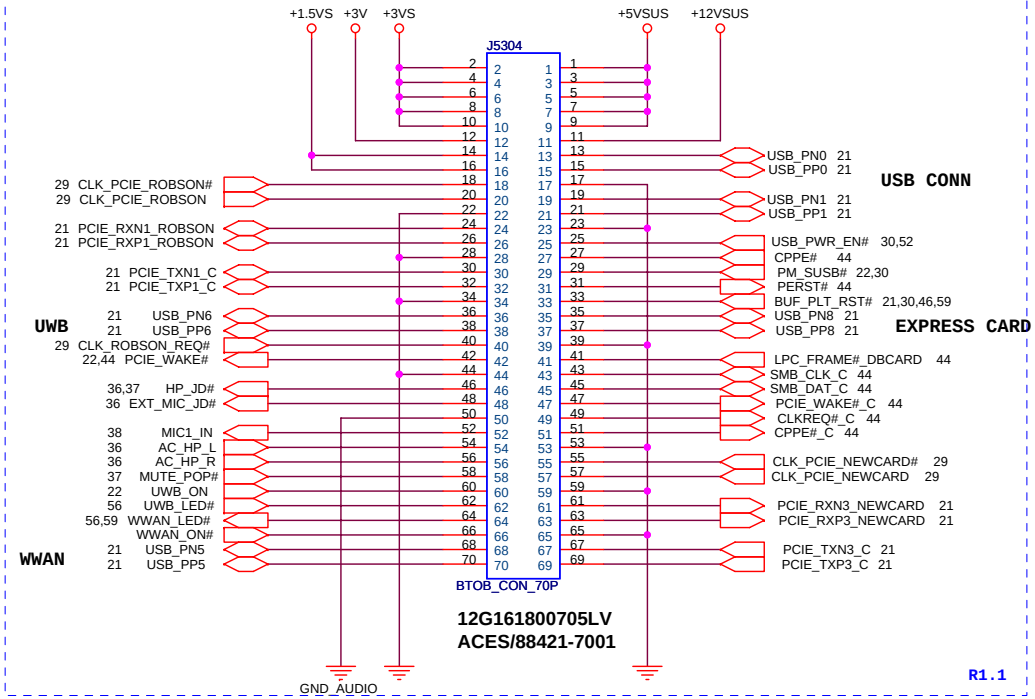
IO BOARD



12G18310260DLV
ACES/88707-2601

R1.1

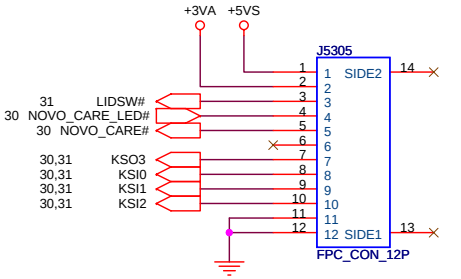
SMALL BOARD



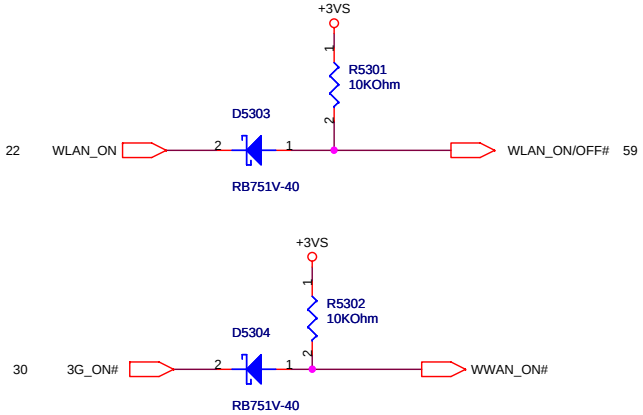
12G161800705LV
ACES/88421-7001

R1.1

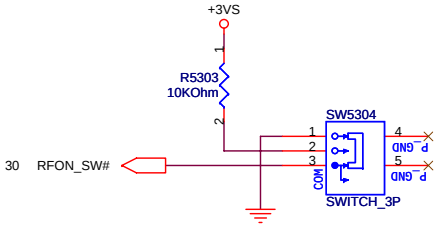
For Media Control Board



12G18310120BLV
ACES/88278-1200L

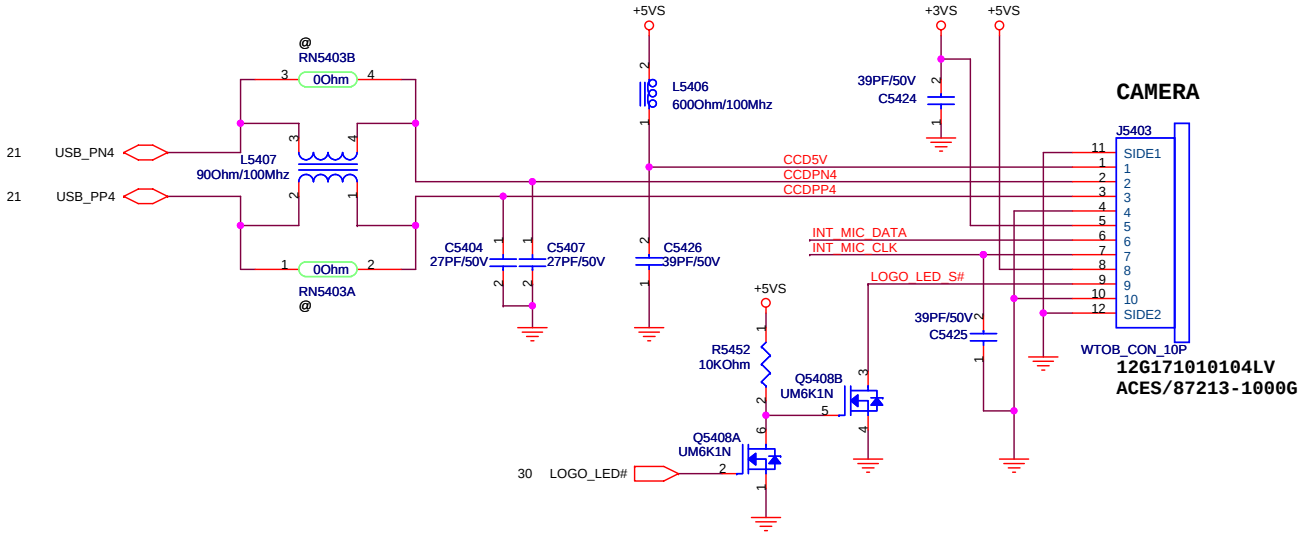


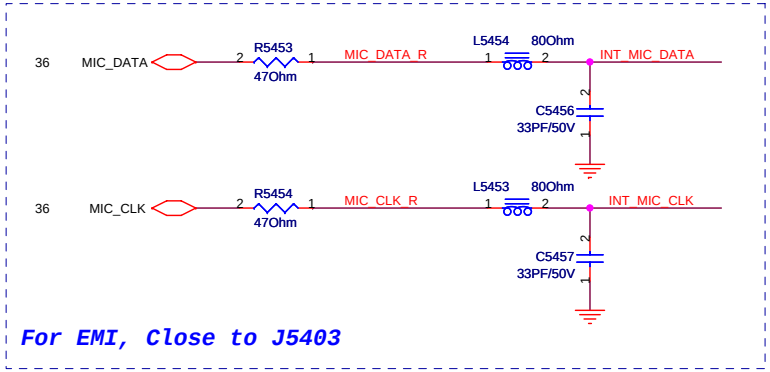
Wireless Switch



12G091070031LV
ALPS/SSSS710603

PEGATRON	Title : IO BOARD	
	Engineer: Peter Lo	
Size: B	Project Name: Rocky30	Rev: 1.1
Date: Monday, February 04, 2008	Sheet 53 of 94	



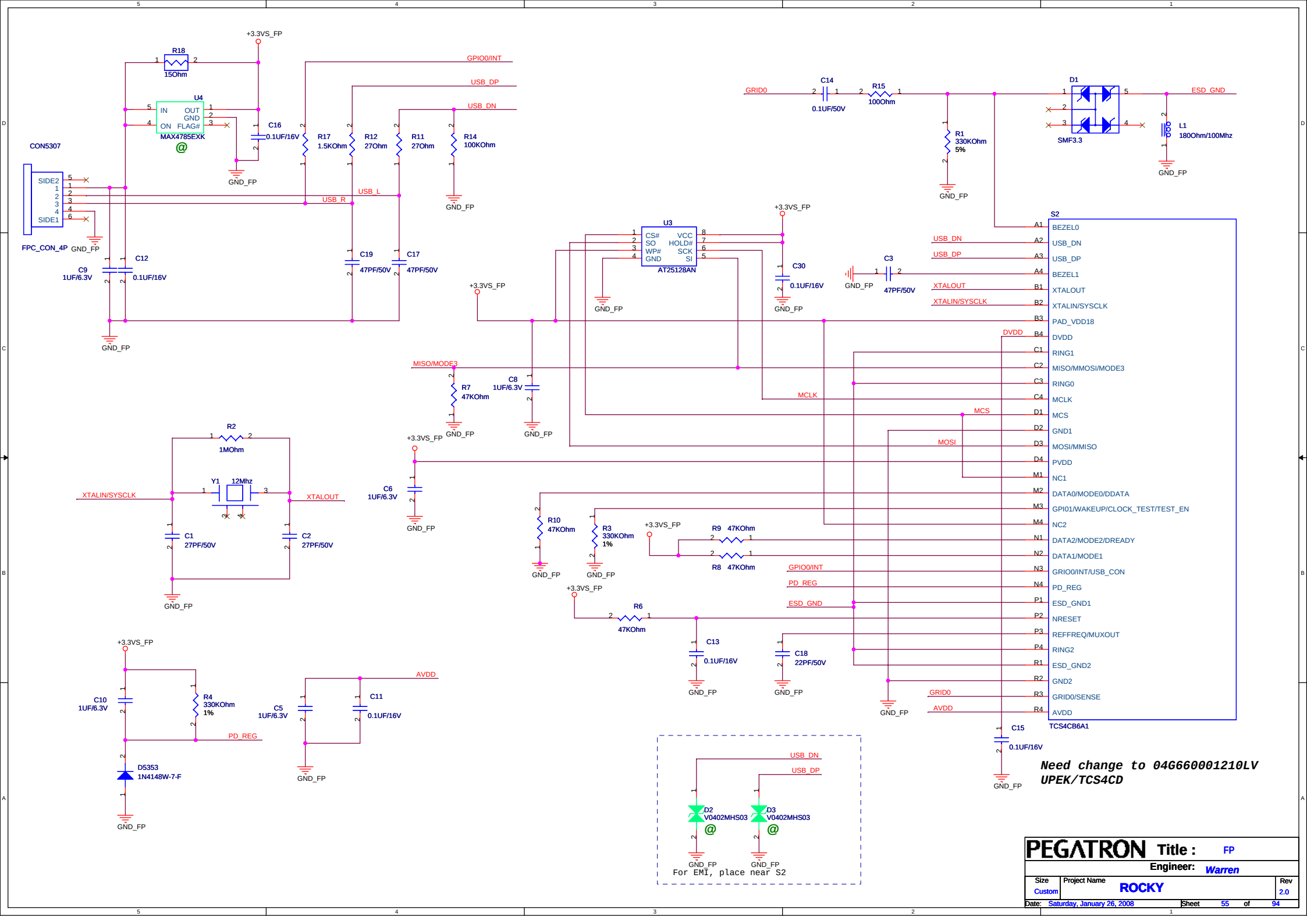


PEGATRON Title : CAMERA

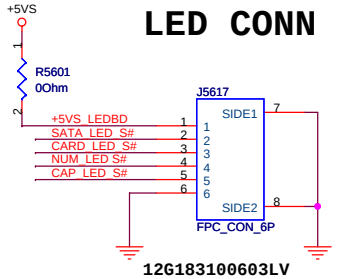
Engineer: Peter Lo

Size	Project Name	Rev
B	Rocky30	1.1

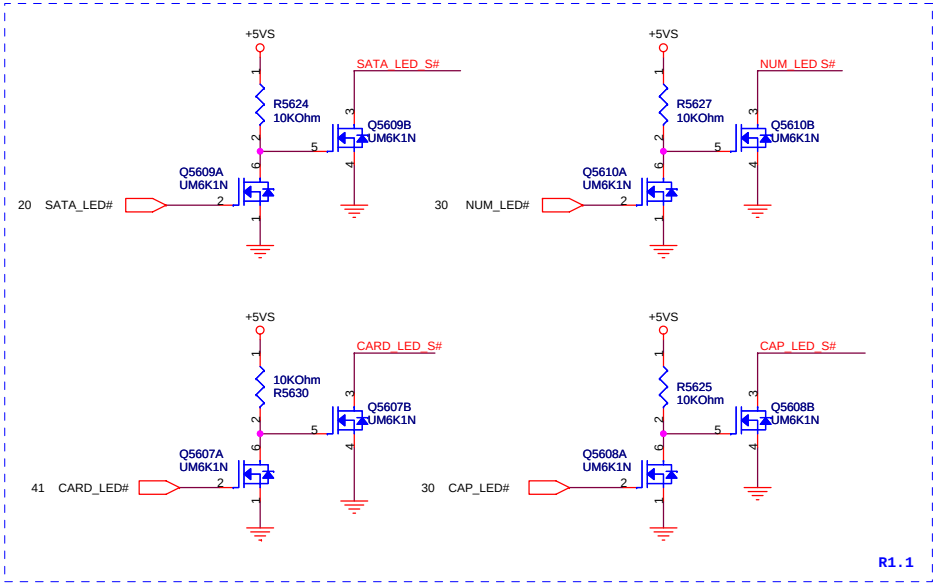
Date: Monday, February 04, 2008 Sheet 54 of 94

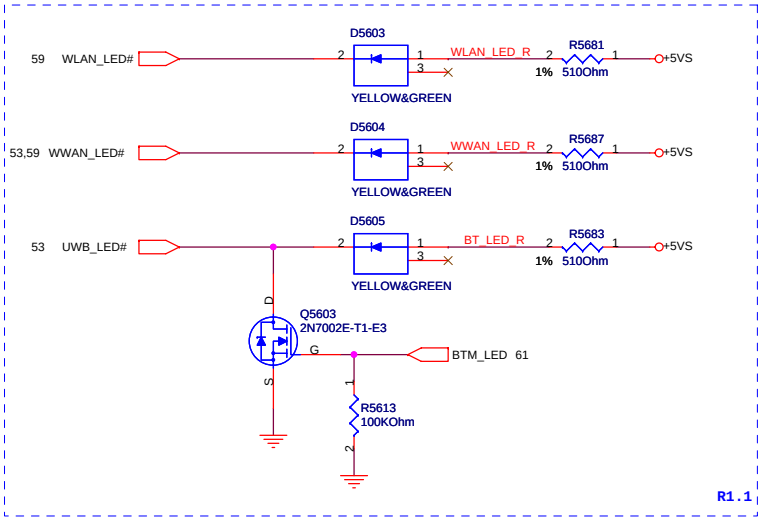

+3.3VS_FP
R18
15Ohm
U4
IN
OUT
GND
ON
FLAG#
MAX4785EXK
@
C16
0.1UF/16V
GND_FP
GPIO0/INT
USB_DP
USB_DN
R17
1.5KOhm
R12
27Ohm
R11
27Ohm
R14
100KOhm
CON5307
SIDE2
SIDE1
FPC_CON_4P
USB_L
USB_R
C9
1UF/6.3V
C12
0.1UF/16V
C19
47PF/50V
C17
47PF/50V
GRID0
C14
0.1UF/50V
R15
100Ohm
R1
330KOhm
5%
D1
SMF3.3
ESD_GND
L1
180Ohm/100Mhz
U3
CS#
SO
WP#
GND
VCC
HOLD#
SCK
SI
AT25128AN
C30
0.1UF/16V
C3
47PF/50V
S2
BEZEL0
USB_DN
USB_DP
BEZEL1
XTALOUT
XTALIN/SYSCLK
PAD_VDD18
DVDD
RING1
MISO/MMOSI/MODE3
RING0
MCLK
MCS
GND1
MOSI/MMISO
PVDD
NC1
DATA0/MODE0/DDATA
GPI01/WAKEUP/CLOCK_TEST/TEST_EN
NC2
DATA2/MODE2/DREADY
DATA1/MODE1
GRIO0/INT/USB_CON
PD_REG
ESD_GND1
NRESET
REFFREQ/MUXOUT
RING2
ESD_GND2
GND2
GRID0/SENSE
AVDD
TCS4CB6A1
C15
0.1UF/16V
MISO/MODE3
R7
47KOhm
C8
1UF/6.3V
MCLK
MCS
MOSI
R2
1MOhm
Y1
12Mhz
XTALIN/SYSCLK
XTALOUT
C1
27PF/50V
C2
27PF/50V
C6
1UF/6.3V
R10
47KOhm
R3
330KOhm
1%
R9
47KOhm
R8
47KOhm
GPIO0/INT
PD_REG
ESD_GND
R6
47KOhm
C13
0.1UF/16V
C18
22PF/50V
C10
1UF/6.3V
R4
330KOhm
1%
D5353
1N4148W-7-F
C5
1UF/6.3V
C11
0.1UF/16V
AVDD
D2
V0402MHS03
D3
V0402MHS03
For EMI, place near S2
Need change to 04G660001210LV
UPEK/TCS4CD
PEGATRON
Title : FP
Engineer: Warren
Size Custom
Project Name ROCKY
Rev 2.0
Date: Saturday, January 26, 2008
Sheet 55 of 94

LED CONN

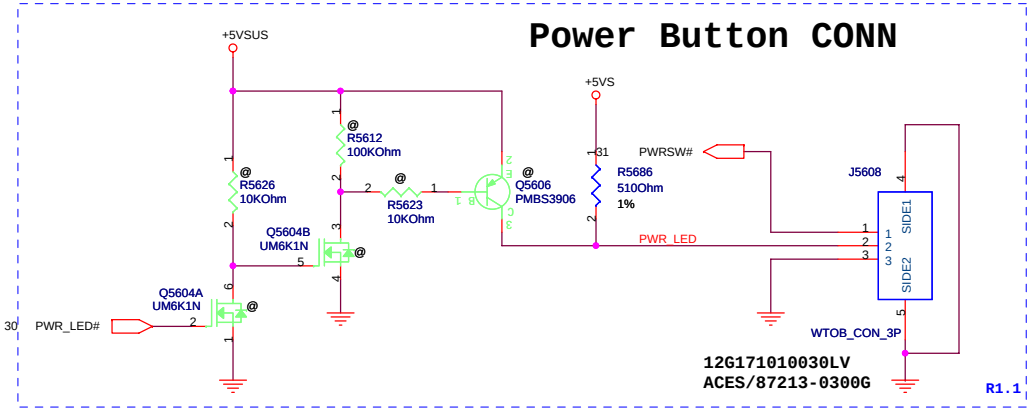


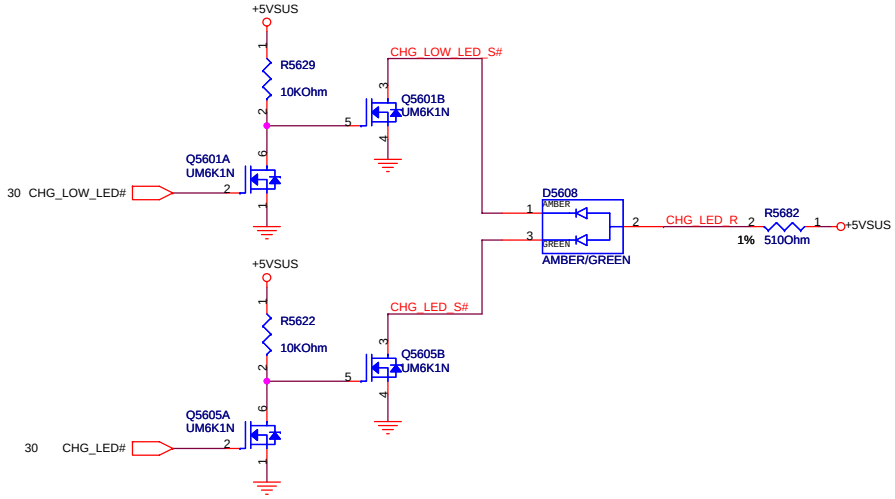
12G183100603LV
ACES/88278-06001

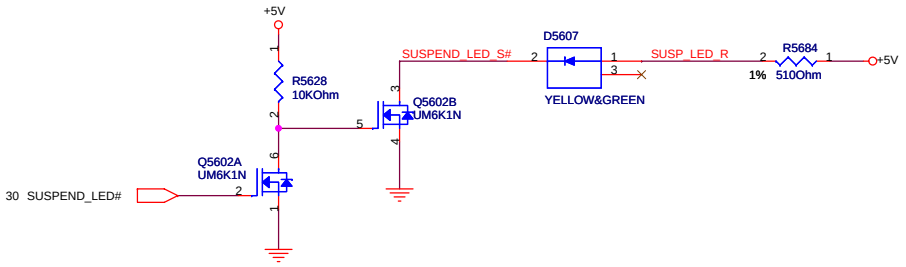




Power Button CONN





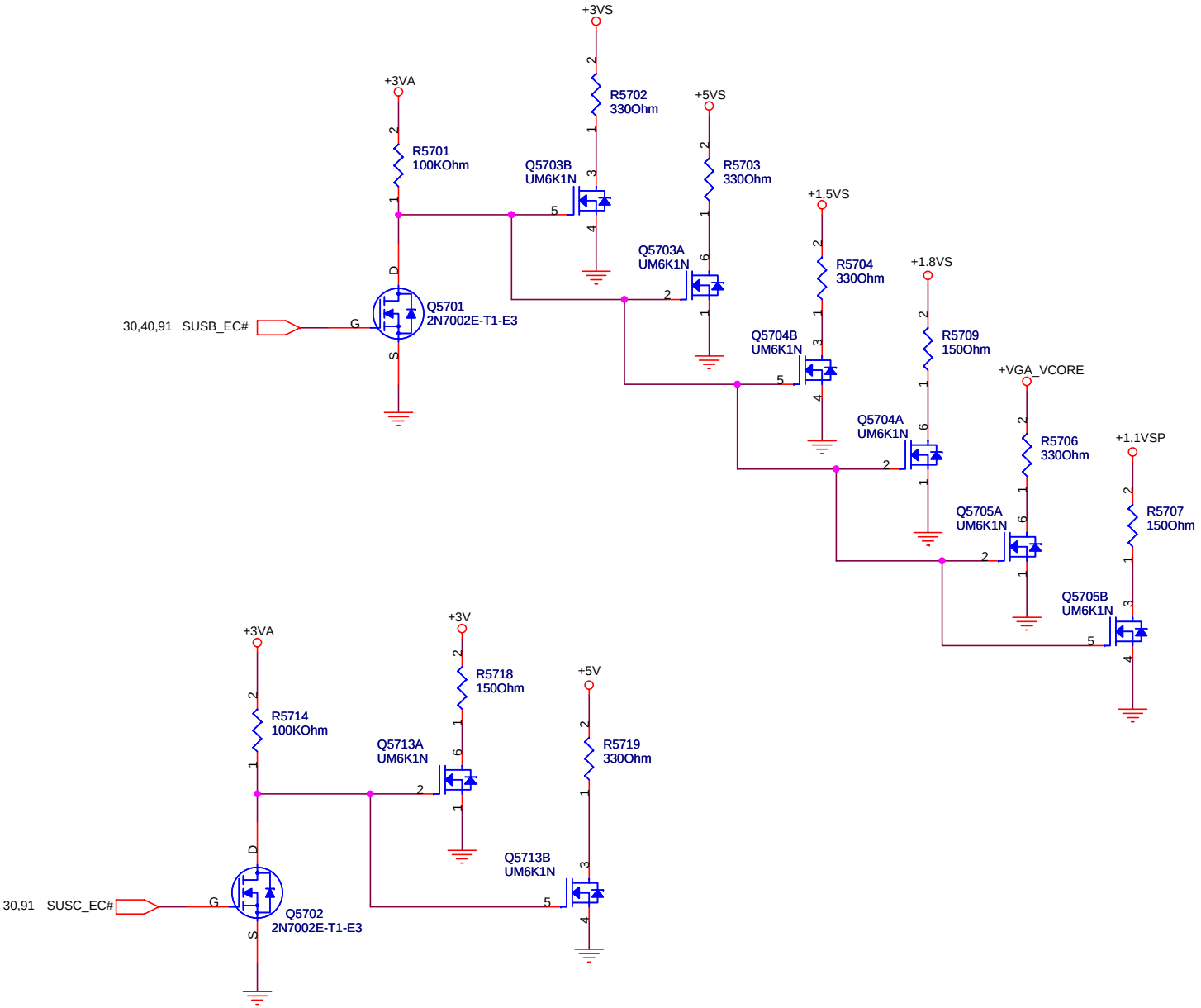


PEGATRON Title : LED/SW

Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.1

Date: Monday, February 04, 2008 Sheet 56 of 94

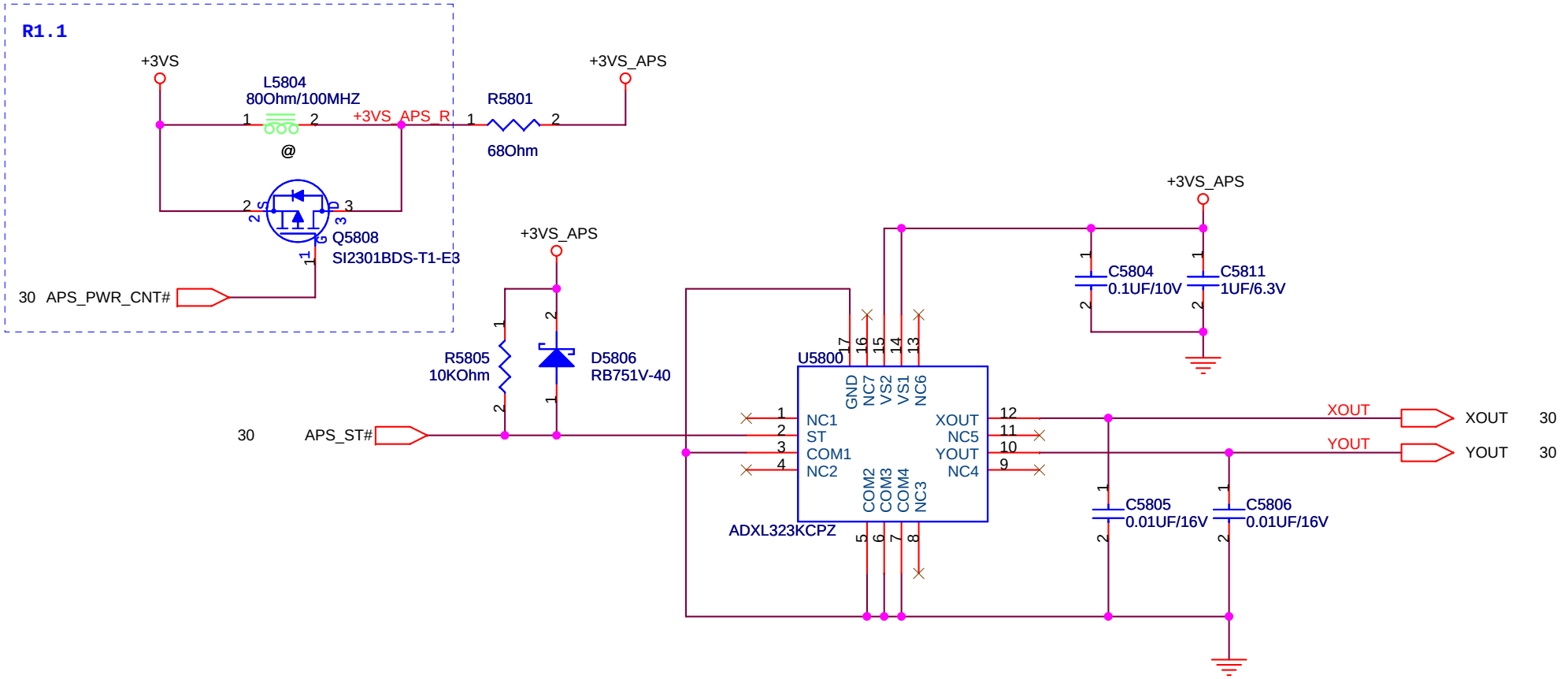


PEGATRON **Title :** DISCHARGE

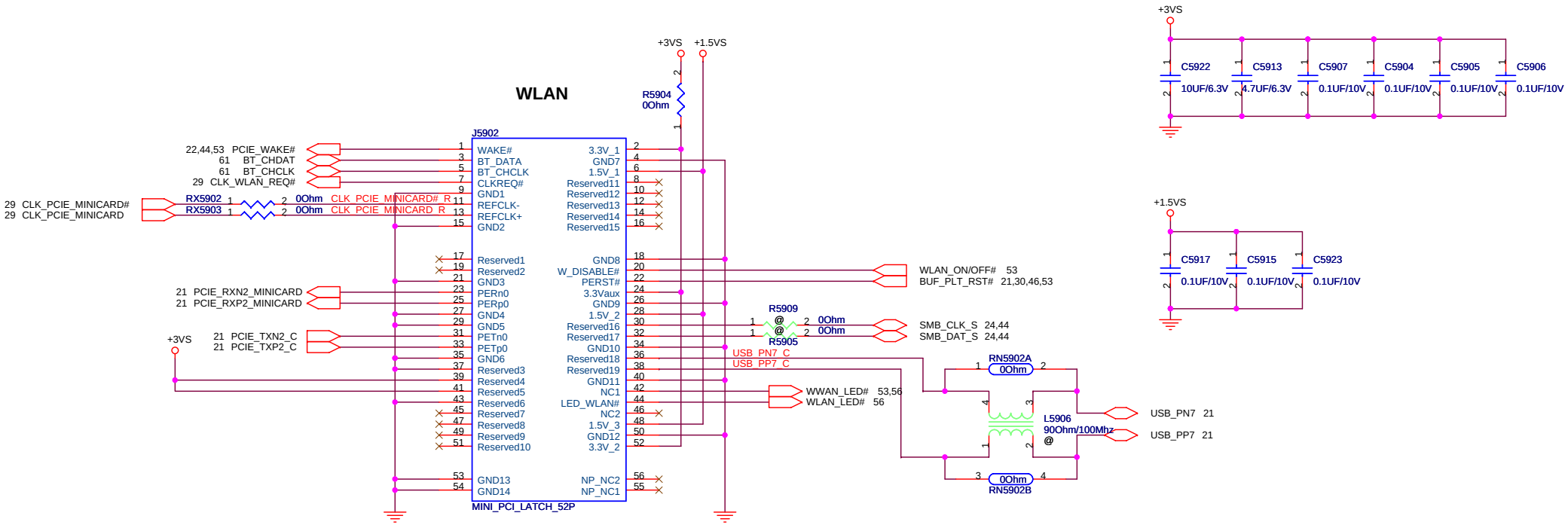
Engineer: *Peter Lo*

Size	Project Name	Rev
Custom	**Rocky30**	1.1

Date: Monday, February 04, 2008 Sheet 57 of 94



PEGATRON	Title : SMS	
	Engineer: *Peter Lo*	
Size: A	Project Name: Rocky30	Rev: 1.1
Date: Monday, February 04, 2008	Sheet 58 of 94	



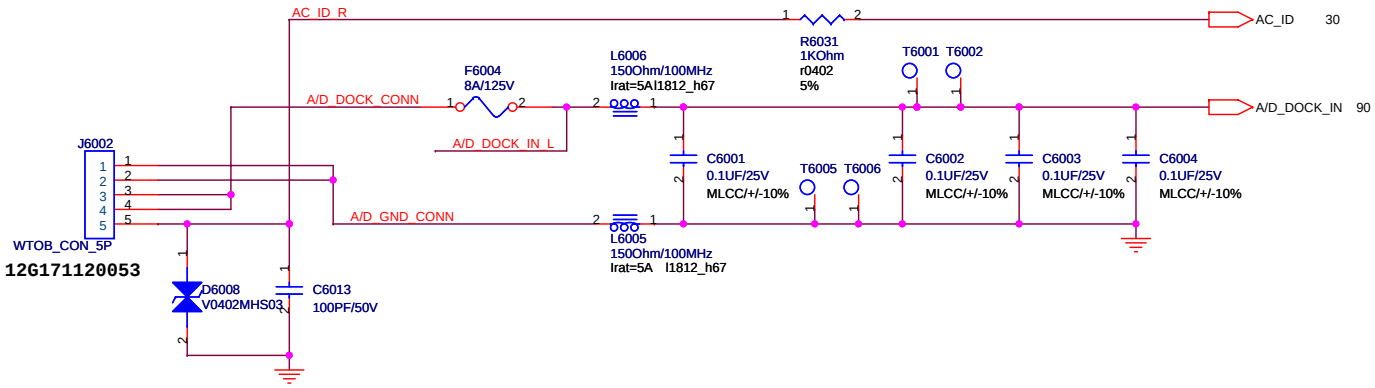
PEGATRON **Title :** Mini Card

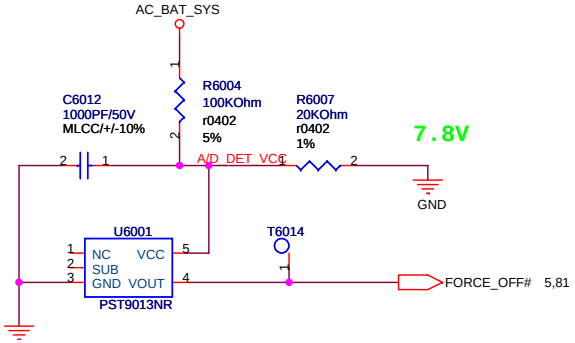
Engineer: *Peter Lo*

Size	Project Name	Rev
B	**Rocky30**	1.1

Date: Monday, February 04, 2008 Sheet 59 of 94

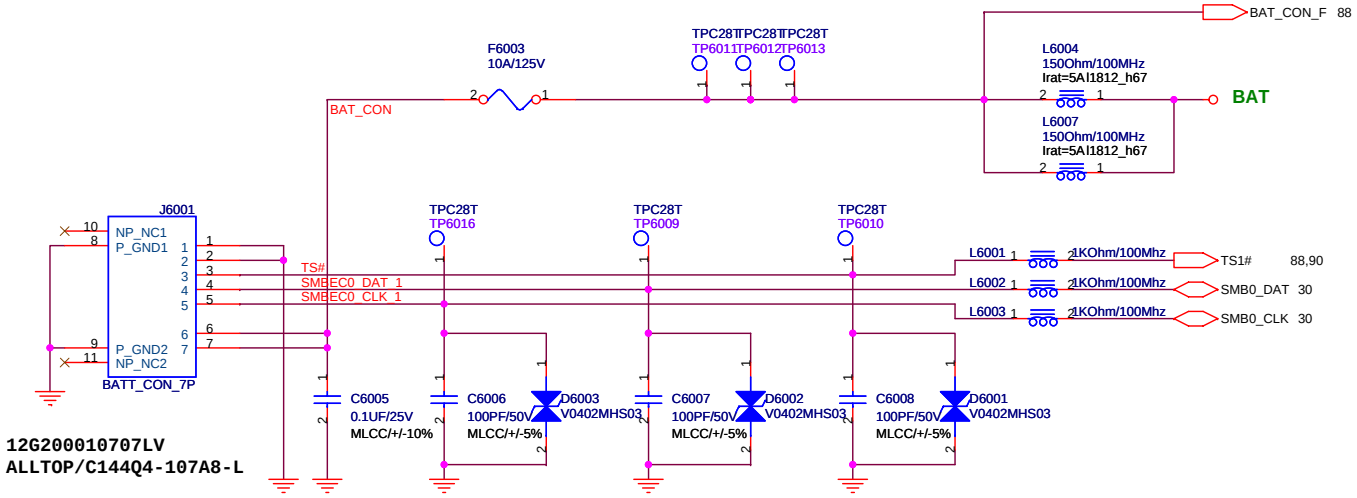
DC IN CONN





Without Battery & Pull out Adapter

Battery CONN



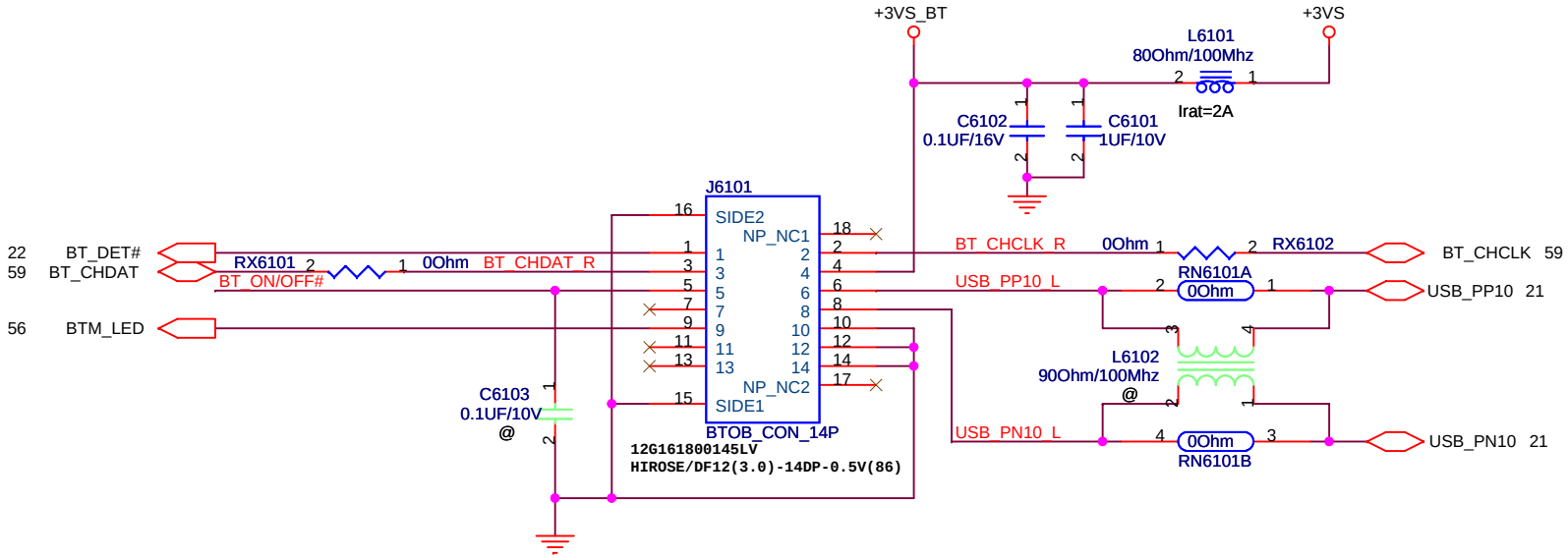
PEGATRON Title : DC Jack & Battery CONN

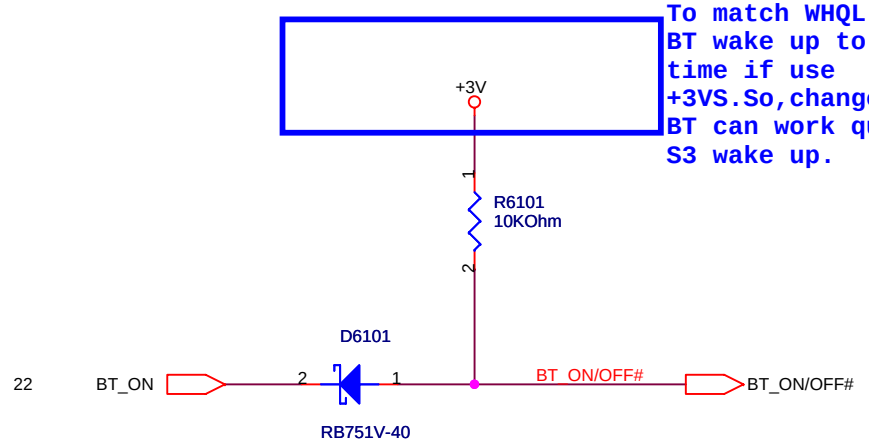
Engineer: Kevin Chang

Size	Project Name	Rev
Custom	Rocky 30	1.1

Date: Monday, February 04, 2008 Sheet 60 of 94

Blue Tooth





To match WHQL test.Due to BT wake up to spend much time if use +3VS.So,change to +3V,let BT can work quickly when S3 wake up.

From GPIO27 ICH9

PEGATRON	Title : BlueTooth		
	Engineer: Peter Lo		
Size: A4	Project Name: Rocky30		Rev: 1.1
Date: Monday, February 04, 2008	Sheet 61 of 94		

PEGATRON Title : ***

Engineer: *Peter Lo*

Size	Project Name	Rev
A4	**Rocky30**	1.1

Date: Saturday, January 26, 2008 Sheet 62 of 94

PEGATRON Title :***

Engineer: *Peter Lo*

Size	Project Name	Rev
A4	**Rocky30**	1.1

Date: Saturday, January 26, 2008 Sheet 63 of 94

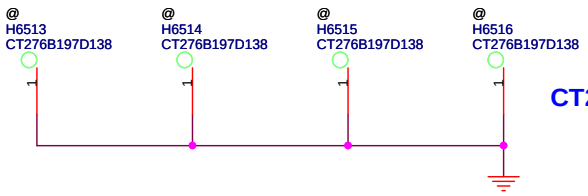
PEGATRON Title :

Engineer: *Peter Lo*

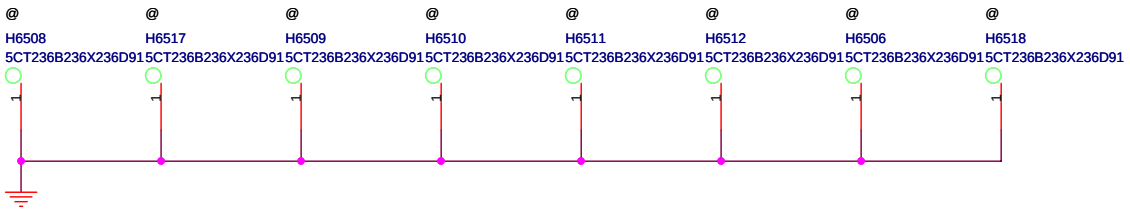
Size	Project Name	Rev
A	**Rocky30**	1.1

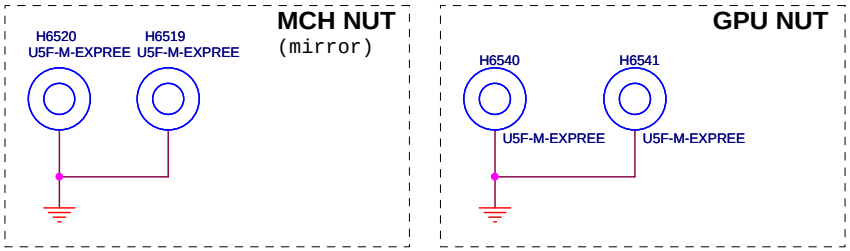
Date: Saturday, January 26, 2008 Sheet 64 of 94

CPU

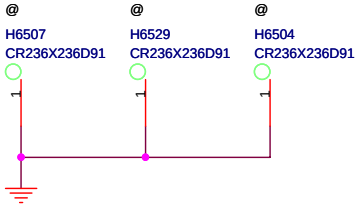


TOP 5CT236B236X236D91 PTH

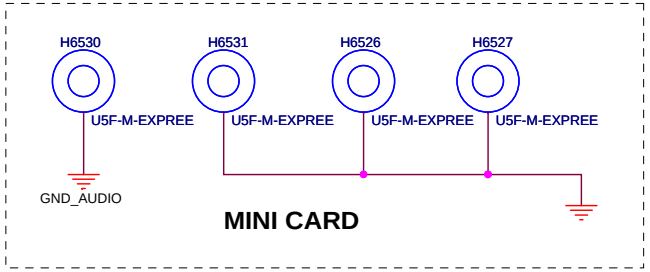




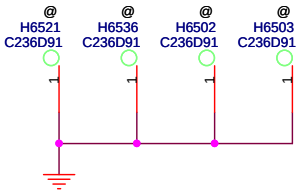
CR236X236D91 PTH



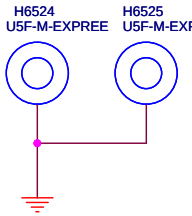
BOT 5CT236B236X236D91 PTH



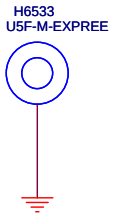
C236D91 PTH



For Fan Stand Off
C236B189D150 PTH (mirror)



For KB Stand Off
C236B189D150 PTH



For BT StandOff

TOOLING HOLE

For ICT

PEGATRON

Title MDC NUT & Hinksink NUT

Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.1

Date: Saturday, January 26, 2008 Sheet 65 of 94

PEGATRON Title : ***

Engineer: *Peter Lo*

Size	Project Name	Rev
Custom	Rocky30	1.1

Date: Saturday, January 26, 2008 Sheet 66 of 94

PEGATRON Title :***

Engineer: *Peter Lo*

Size	Project Name	Rev
Custom	Rocky30	1.1

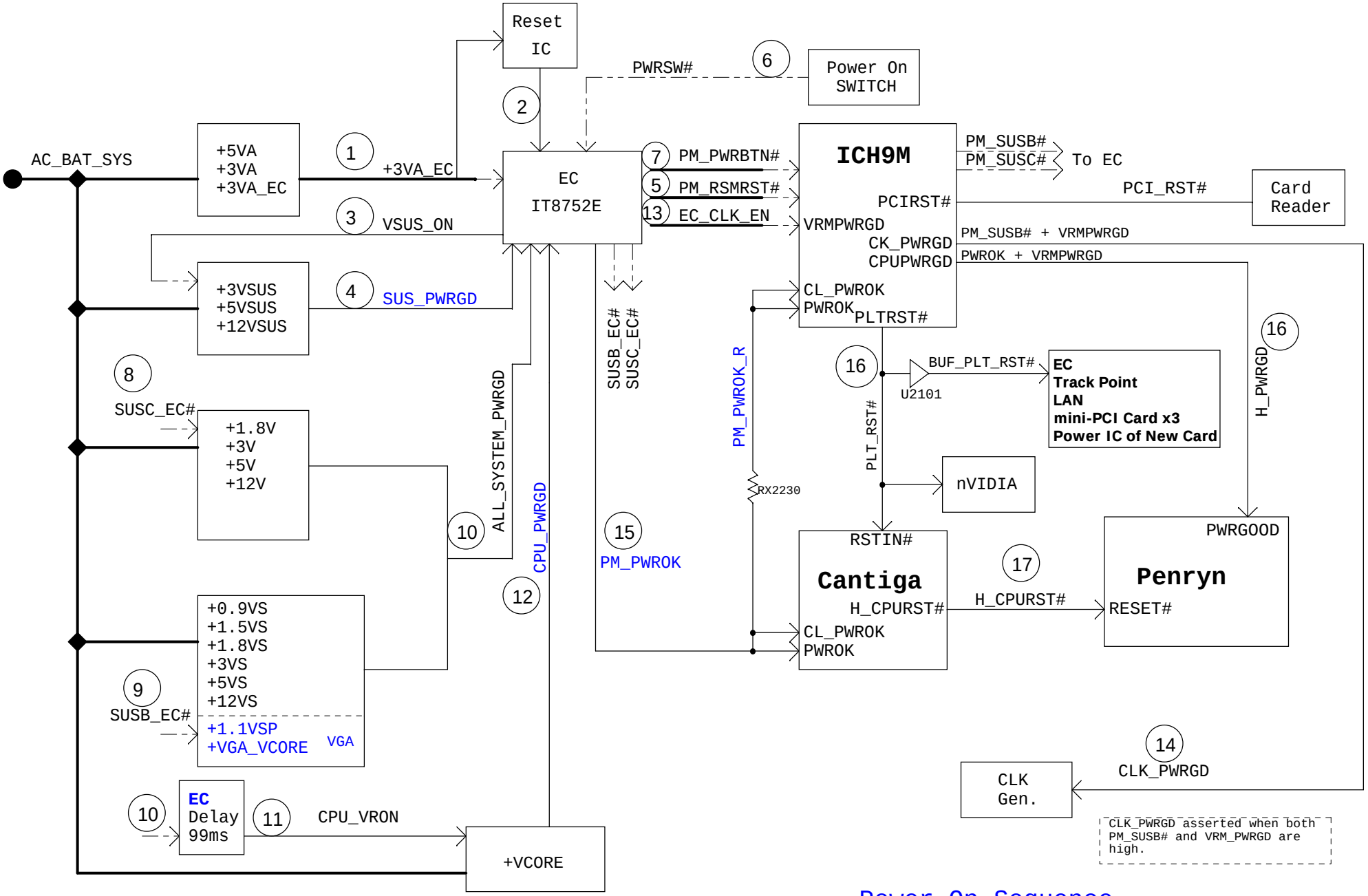
Date: Saturday, January 26, 2008 Sheet 67 of 94

PEGATRON Title : ***

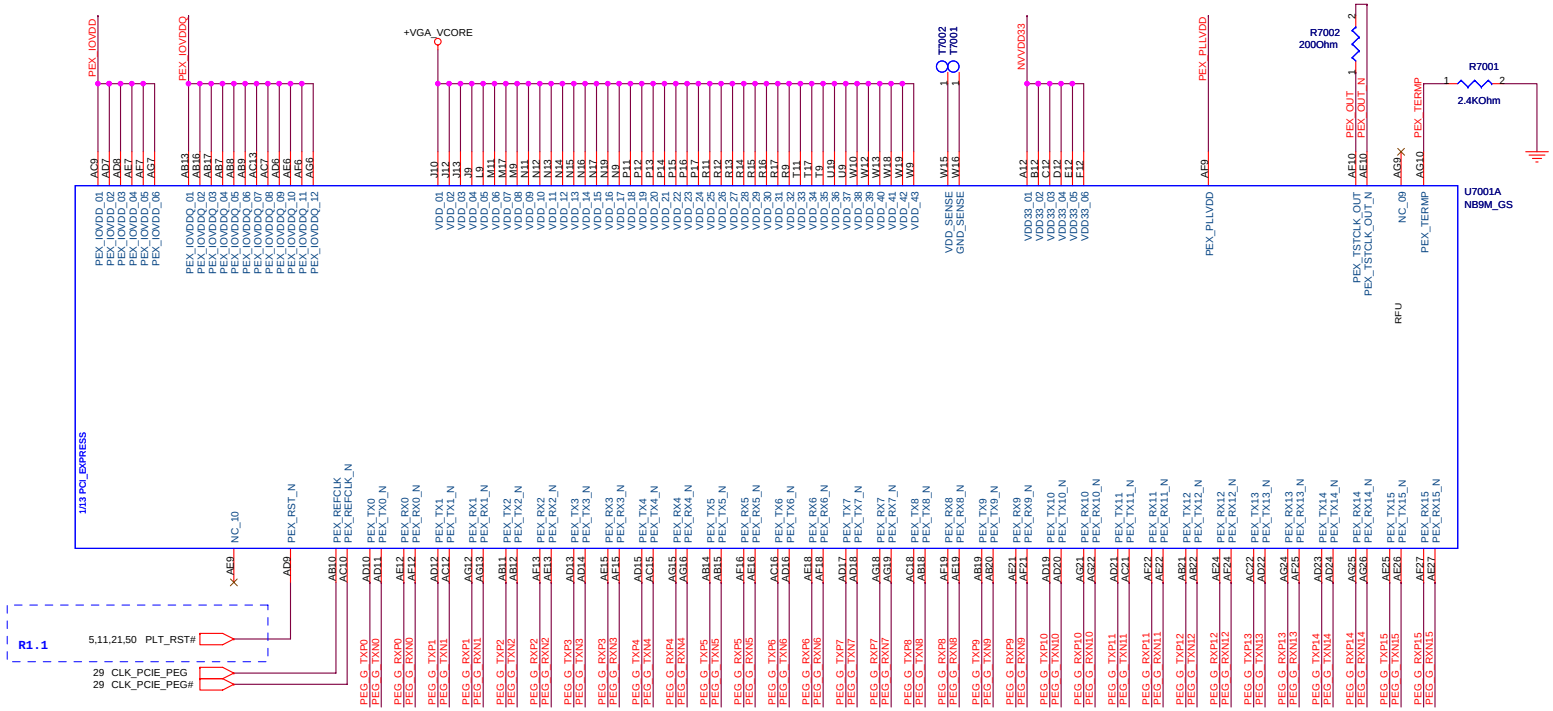
Engineer: *Peter Lo*

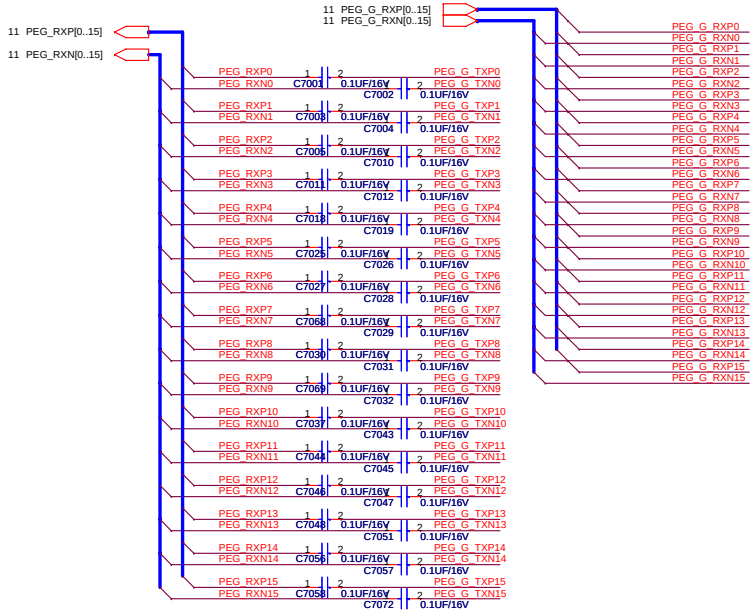
Size	Project Name	Rev
Custom	Rocky30	1.1

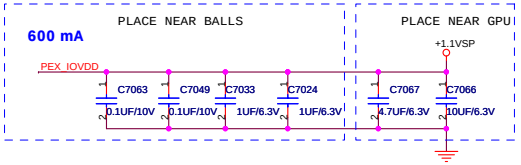
Date: Saturday, January 26, 2008 Sheet 68 of 94

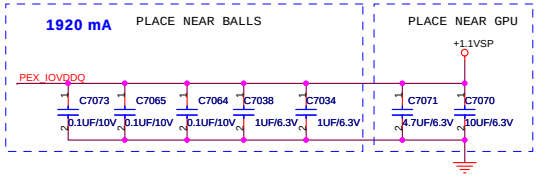


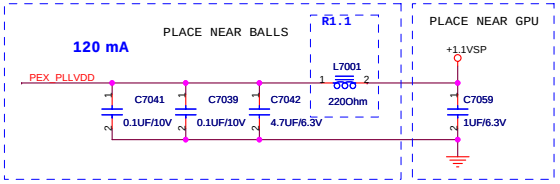
PEGATRON	Title : Power Sequence	
	Engineer: Peter Lo	
Size: Custom	Project Name: Rocky30	Rev: 1.1
Date: Saturday, January 26, 2008	Sheet 69 of 94	

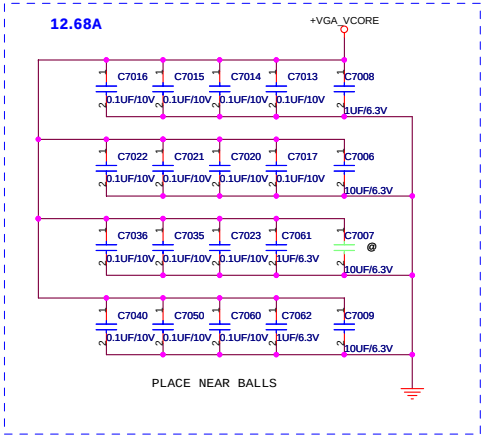


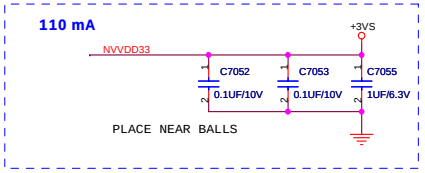










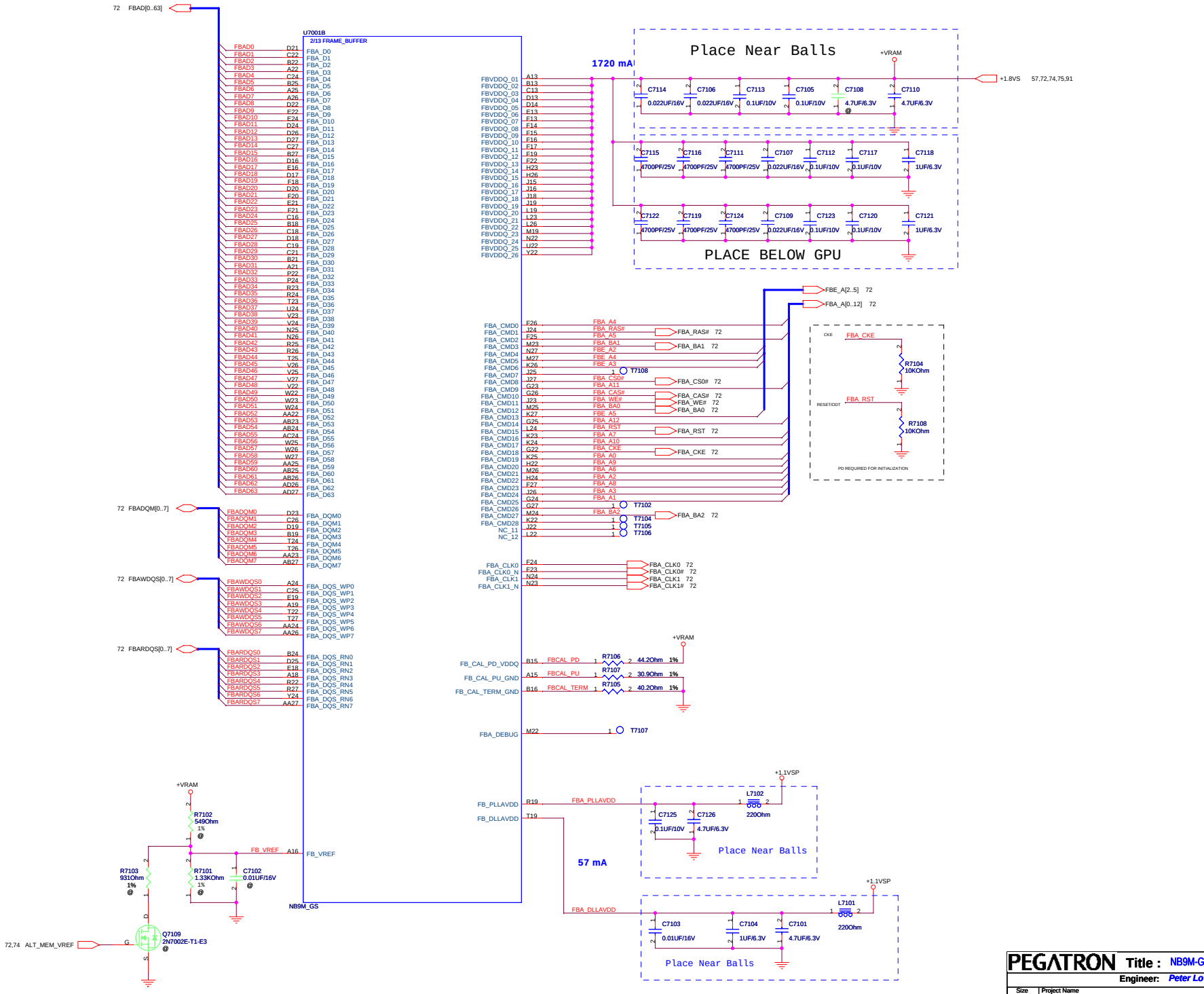


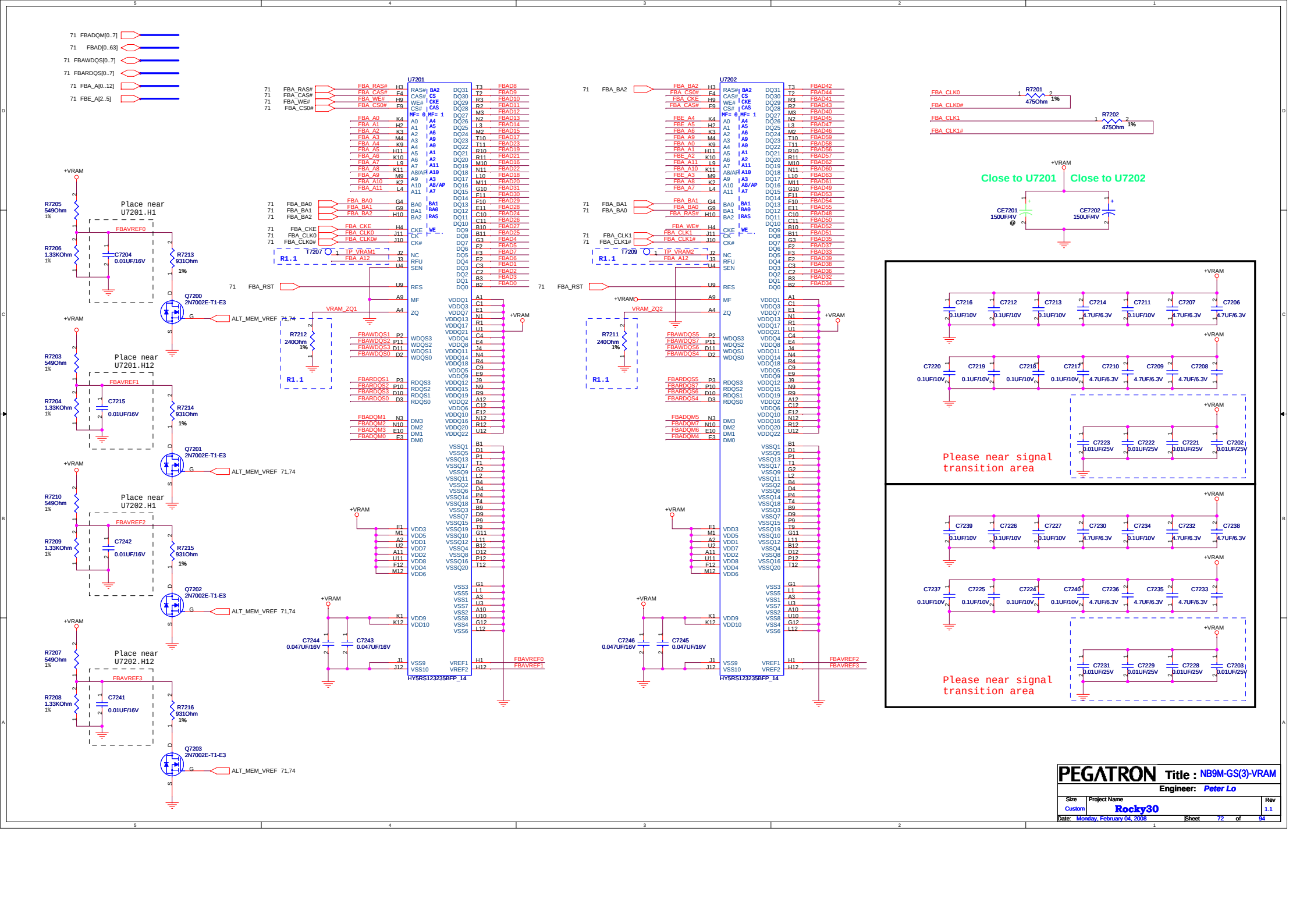
PEGATRON Title : NB9M-GS(1)

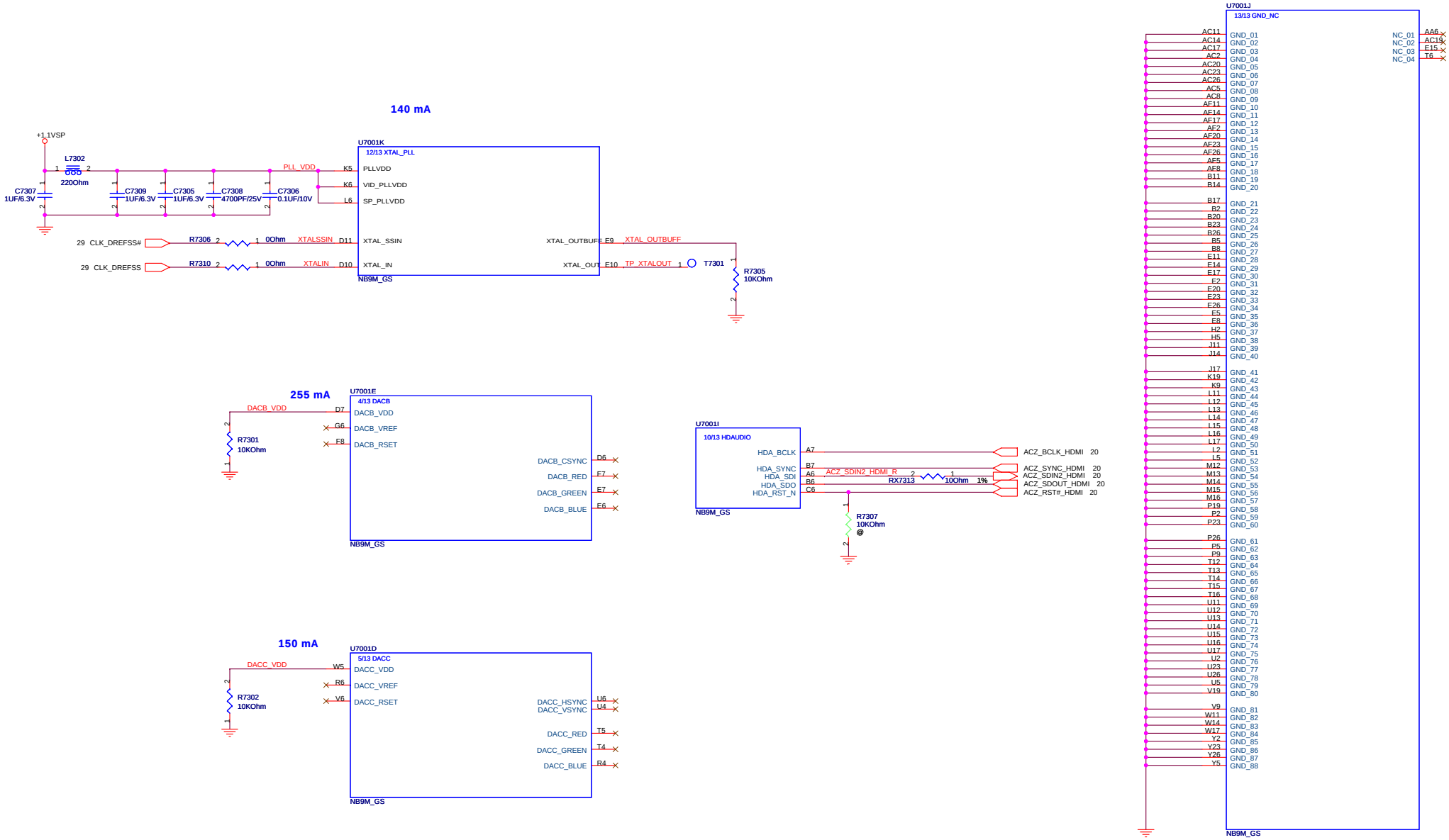
Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.1

Date: Monday, February 04, 2008 Sheet 70 of 94


72 FBAD[0..63]
U7001B
2/13 FRAME_BUFFER
NB9M_GS
1720 mA
Place Near Balls
+VRAM
+1.8VS 57,72,74,75,91
C7114 0.022UF/16V
C7106 0.022UF/16V
C7113 0.1UF/10V
C7105 0.1UF/10V
C7108 4.7UF/6.3V @
C7110 4.7UF/6.3V
C7115 4700PF/25V
C7116 4700PF/25V
C7111 4700PF/25V
C7107 0.022UF/16V
C7112 0.1UF/10V
C7117 0.1UF/10V
C7118 1UF/6.3V
C7122 4700PF/25V
C7119 4700PF/25V
C7124 4700PF/25V
C7109 0.022UF/16V
C7123 0.1UF/10V
C7120 0.1UF/10V
C7121 1UF/6.3V
PLACE BELOW GPU
FBE_A[2..5] 72
FBA_A[0..12] 72
CKE
FBA_CKE
R7104 10KOhm
RESET#/ODT
FBA_RST
R7108 10KOhm
PD REQUIRED FOR INITIALIZATION
T7108
T7102
T7104
T7105
T7106
T7107
72 FBADQM[0..7]
72 FBAWDQS[0..7]
72 FBARDQS[0..7]
FBA_CLK0 72
FBA_CLK0# 72
FBA_CLK1 72
FBA_CLK1# 72
FBA_RAS# 72
FBA_CAS# 72
FBA_WE# 72
FBA_BA0 72
FBA_BA1 72
FBA_BA2 72
FBA_CS0# 72
FBA_CKE 72
FBA_RST 72
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
FBCAL_PD R7106 44.2Ohm 1%
FBCAL_PU R7107 30.9Ohm 1%
FBCAL_TERM R7105 40.2Ohm 1%
FBA_DEBUG
+1.1VSP
FB_PLLAVDD
FB_DLLAVDD
FBA_PLLAVDD
FBA_DLLAVDD
L7102 220Ohm
C7125 0.1UF/10V
C7126 4.7UF/6.3V
57 mA
Place Near Balls
L7101 220Ohm
C7103 0.01UF/16V
C7104 1UF/6.3V
C7101 4.7UF/6.3V
Place Near Balls
+VRAM
R7102 549Ohm 1% @
FB_VREF
R7103 931Ohm 1% @
R7101 1.33KOhm 1% @
C7102 0.01UF/16V @
72,74 ALT_MEM_VREF
Q7109 2N7002E-T1-E3 @
PEGATRON Title : NB9M-GS(2)
Engineer: Peter Lo
Size C
Project Name Rocky30
Rev 1.1
Date: Monday, February 04, 2008
Sheet 71 of 94


71 FBADQM[0..7]
71 FBAD[0..63]
71 FBAWDQS[0..7]
71 FBARDQS[0..7]
71 FBA_A[0..12]
71 FBE_A[2..5]
U7201
U7202
HY5RS123235BFP_14
Place near U7201.H1
Place near U7201.H12
Place near U7202.H1
Place near U7202.H12
Q7200 2N7002E-T1-E3
Q7201 2N7002E-T1-E3
Q7202 2N7002E-T1-E3
Q7203 2N7002E-T1-E3
ALT_MEM_VREF 71,74
VRAM_ZQ1
VRAM_ZQ2
R7201 475Ohm 1%
R7202 475Ohm 1%
Close to U7201
Close to U7202
CE7201 150UF/4V
CE7202 150UF/4V
Please near signal transition area
Please near signal transition area
PEGATRON
Title : NB9M-GS(3)-VRAM
Engineer: Peter Lo
Size Custom
Project Name Rocky30
Rev 1.1
Date: Monday, February 04, 2008
Sheet 72 of 94



PEGATRON Title : NB9M-GS(4)

Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.1

Date: Monday, February 04, 2008 Sheet 73 of 94

DDCA: CRT
DDCB: HDMI
DDCC: LVDS/THERMAL

U7001M
9/13 I2C_GPIO_THERM_JTAG
NB9M_GS

50 VGA_THERM_DC — VGA_THERM_DC — D8 THERMDN
50 VGA_THERM_DA — VGA_THERM_DA — D9 THERMDP

T7415 TP_JTAG_TCK AF3 JTAG_TCK
T7416 TP_JTAG_TMS AF4 JTAG_TMS
T7417 TP_JTAG_TDI AG4 JTAG_TDI
T7402 TP_JTAG_TDO AE4 JTAG_TDO
R7409 1KOhm JTAG_TRST_N AG3 JTAG_TRST_N

+3VS — R7445 10KOhm I2CS_SCL_VGA T1 I2CS_SCL
R7444 10KOhm I2CS_SDA_VGA T2 I2CS_SDA

I2CA_SCL / I2CA_SDA: R1 I2CA_SCL_VGA, T3 I2CA_SDA_VGA — R7415 33Ohm 1%, R7416 33Ohm 1% — CRT_DDC_CLK 45, CRT_DDC_DAT 45
I2CB_SCL / I2CB_SDA: R2 I2CB_SCL_VGA, R3 I2CB_SDA_VGA — R7423 33Ohm 1%, R7425 33Ohm 1% — HDMI_CLK 48, HDMI_DAT 48
I2CC_SCL / I2CC_SDA: A2 I2CC_SCL_VGA, B1 I2CC_SDA_VGA — R7405 33Ohm, R7406 33Ohm — EDID_CLK 46, EDID_DAT 46
I2CD_SCL / I2CD_SDA: N2 I2CD_SCL_VGA, N3 I2CD_SDA_VGA — R7440 10KOhm, R7441 10KOhm — +3VS
I2CE_SCL / I2CE_SDA: Y6 I2CE_SCL_VGA, W6 I2CE_SDA_VGA — R7443 10KOhm, R7442 10KOhm

+3VS — R7404 2.2KOhm, R7403 2.2KOhm

GPIO0 N1 TP_GPU_GPIO0 — T7407
GPIO1 G1 HOTPLUG — HOTPLUG 48
GPIO2 C1 TP_GPU_GPIO2 — T7401
GPIO3 M2 LCD_VDD_EN
GPIO4 M3 LCD_BACKEN
GPIO5 K3 GPU_VID0 — GPU_VID0 85
GPIO6 K2 GPU_VID1 — GPU_VID1 85
GPIO7 J2 TP_GPU_VID2 — T7409
GPIO8 C2 NV_OVERT# R — R7401 0Ohm — NV_OVERT# 30
GPIO9 M1 TP_GPU_GPIO9 — T7403
GPIO10 D2 ALT_MEM_VREF_VGA — R7434 0Ohm — ALT_MEM_VREF 71,72
GPIO11 D1 TP_GPU_GPIO11 — T7405
GPIO12 J3 TP_GPU_GPIO12 — T7406
GPIO13 J1
GPIO14 K1
GPIO15 E3
GPIO16 G3
GPIO17 G2
GPIO18 F1
GPIO19 F2

R7414 2KOhm 1%, R7448 2KOhm 1%
+3VS — R7402 10KOhm @
C7423 0.1UF/10V
R7435 10KOhm

U7001L
11/13 MISC
NB9M_GS

+3VS — R7424 10KOhm 1%, R7428 10KOhm 1% @, R7430 45.3KOhm 1%
R7427 10KOhm 1% @, R7429 10KOhm 1%, R7431 10KOhm 1% @
STRAP0_VGA C7 STRAP0
STRAP1_VGA B9 STRAP1
STRAP2_VGA A9 STRAP2
R7407 40.2KOhm 1% F11 STRAP_REF_3V3
R7408 40.2KOhm 1% F10 STRAP_REF_MIOB
+3VS — R7410 24.3KOhm 1% @ — SPDIF_VGA F9 SPDIF
36 SPDIF_OUT — C7422 0.1UF/10V @ — R7419 3.4KOhm 1% @
C15 NC_05
D15 NC_06

ROM_CS_N B10 — T7410
ROM_SI A10 — ROM_SI_VGA
ROM_SO C10 — ROM_SO_VGA
ROM_SCLK C9 — ROM_SCLK_VGA
R7436 10KOhm 1% @, R7438 4.99KOhm 1%, R7432 10KOhm 1% @
I2CH_SCL A3
I2CH_SDA A4
R7437 15KOhm 1%, R7439 10KOhm 1% @, R7433 15KOhm 1%
BUFRST_N N5 — T7414
NC_07 J5
NC_08 F6
TESTMODE AD25 — R7411 10KOhm
GND_89 AC6
R7421 10KOhm, R7446 10KOhm
R7422 10KOhm @
I2CH_SCL_VGA
I2CH_SDA_VGA

LCD_VDD_EN — LCD_VDD_EN 46
LCD_BACKEN — LCD_BACKEN 46
R7412 10KOhm, R7413 10KOhm

C7402 0.1UF/10V
R7449 0Ohm
HDCP_WP
HDCP ROM
U7401 AT24C16BN-SH-B (VCC A0 WP A1 SCL A2 SDA GND)
R7450 10KOhm @
R1.1

IFPE_PLLVDD_VGA N6 — R7447 10KOhm
IFPE_IOVDD_VGA H6 — R7420 1KOhm

U7001G
8/13 IFPE
NB9M_GS
IFPE_PLLVDD N6
IFPE_RSET M6
IFPE_IOVDD H6
DVI / DP
E
TXC / TXC
TXD0 / TXD0
TXD1 / TXD1
TXD2 / TXD2
IFPE_AUX_N D4 / IFPE_AUX D3
IFPE_L3_N B4 / IFPE_L3 B3
IFPE_L2_N C4 / IFPE_L2 C3
IFPE_L1_N D5 / IFPE_L1 E4
IFPE_L0_N F4 / IFPE_L0 F5

STRAP2 (R7424)	
5K	GE
10K	GS

ROM-SI (R7437)	
10K	Qimonda 16M*32
15K	Hynix 16M*32
20K	Samsung 16M*32
30K	Qimonda 32M*32
35K	Hynix 32M*32
45K	Samsung 32M*32

HDMI

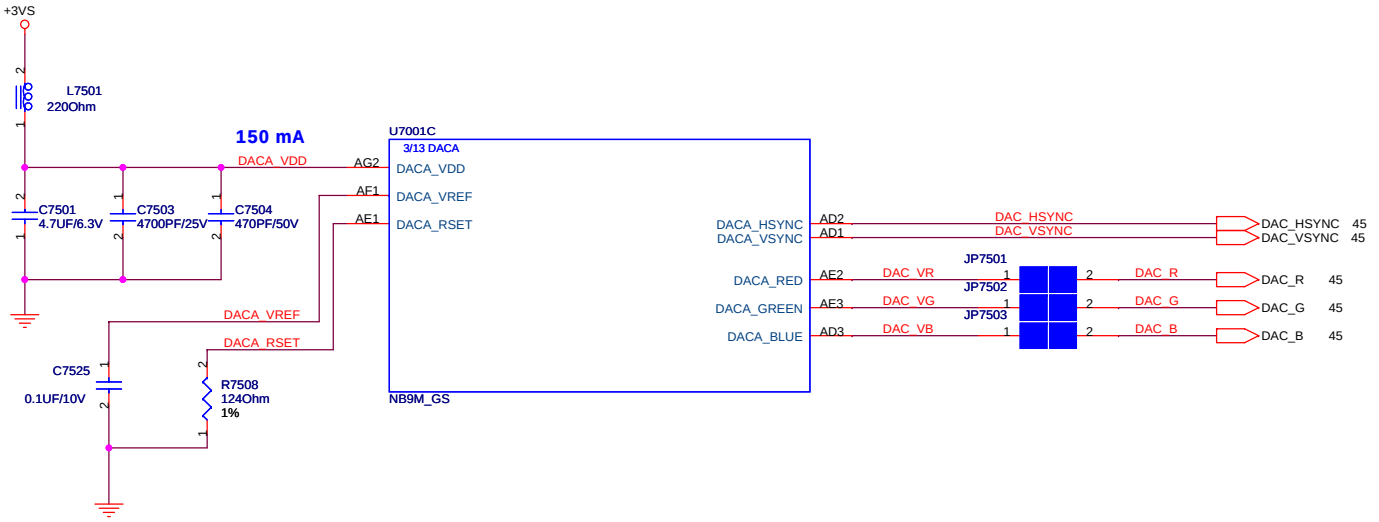
+1.8VS — L7402 220Ohm — 160 mA
C7411 1UF/6.3V, C7412 1UF/6.3V, C7413 4700PF/25V, C7414 470PF/50V
R7426 1KOhm
IFPC_PLLVDD P6 / IFPC_RSET R5

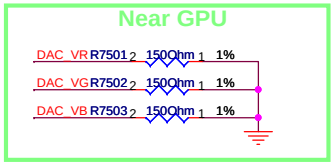
+1.1VSP — L7403 220Ohm — 385 mA
C7415 1UF/6.3V, C7416 4.7UF/6.3V, C7417 1UF/6.3V, C7418 1UF/6.3V, C7419 4700PF/25V, C7420 470PF/50V, C7421 470PF/50V
IFPC_IOVDD J6

U7001H
7/13 IFPC
NB9M_GS
C
DVI / DP
IFPC_AUX_N G5 / IFPC_AUX G4
TXC / TXC
TXD0 / TXD0
TXD1 / TXD1
TXD2 / TXD2
IFPC_L3_N / IFPC_L3
IFPC_L2_N / IFPC_L2
IFPC_L1_N / IFPC_L1
IFPC_L0_N / IFPC_L0

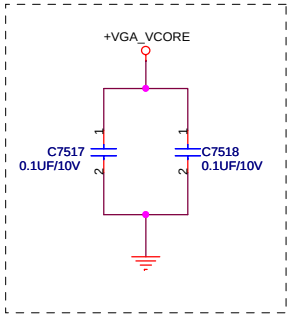
J4 DVI_CLKB-_C — C7409 0.1UF/10V — C7410 0.1UF/10V — H4 DVI_CLKB+_C — DVI_CLKB- 48, DVI_CLKB+ 48
K4 DVI_TX0-_C — C7403 0.1UF/10V — C7404 0.1UF/10V — L4 DVI_TX0+_C — DVI_TX0- 48, DVI_TX0+ 48
M4 DVI_TX1-_C — C7407 0.1UF/10V — C7408 0.1UF/10V — M5 DVI_TX1+_C — DVI_TX1- 48, DVI_TX1+ 48
N4 DVI_TX2-_C — C7405 0.1UF/10V — C7406 0.1UF/10V — P4 DVI_TX2+_C — DVI_TX2- 48, DVI_TX2+ 48

PEGATRON Title : NB9M-GS(5)
Engineer: Peter Lo
Size: Custom | Project Name: Rocky30 | Rev: 1.1
Date: Monday, February 04, 2008 | Sheet 74 of 94

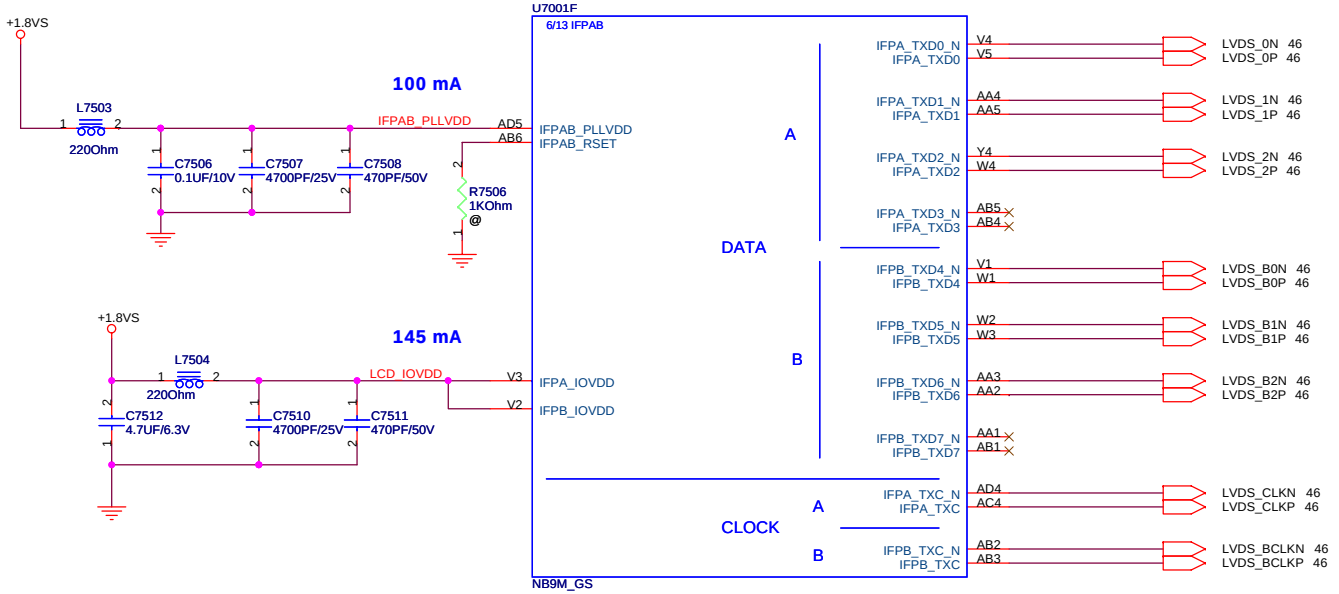




TRANSITION CAPS FOR VSYNC & HSYNC



LVDS



PEGATRON Title : NB9M-GS(6)

Engineer: Peter Lo

Size	Project Name	Rev
Custom	Rocky30	1.1

Date: Monday, February 04, 2008 Sheet 75 of 94

PEGATRON Title : ***

Engineer: *Peter Lo*

Size	Project Name	Rev
B	Rocky30	1.1

Date: Saturday, January 26, 2008 Sheet 76 of 94

PEGATRON Title : ***

Engineer: *Peter Lo*

Size	Project Name	Rev
B	Rocky30	1.1

Date: Saturday, January 26, 2008 Sheet 77 of 94

PEGATRON Title : ***

Engineer: *Peter Lo*

Size	Project Name	Rev
B	Rocky30	1.1

Date: Saturday, January 26, 2008 Sheet 78 of 94

PEGATRON

Title : History

Engineer: Peter Lo

Size	Project Name	Rev
A	Rocky30	1.1

Date: Saturday, January 26, 2008 Sheet 79 of 94

IMVP6 CPU VCORE REGULATOR

3.3V level logic level: DPRSLPVR, SHDN#

1.05V level logic: VID, PSI#, DPRSTP#

POUT=(VCSN2-VGNDS)x(CSP1-CNS1+CSP2-CSN2)/16.67mV

FSW=297.8kHz

Slewrate=12.5mV/us

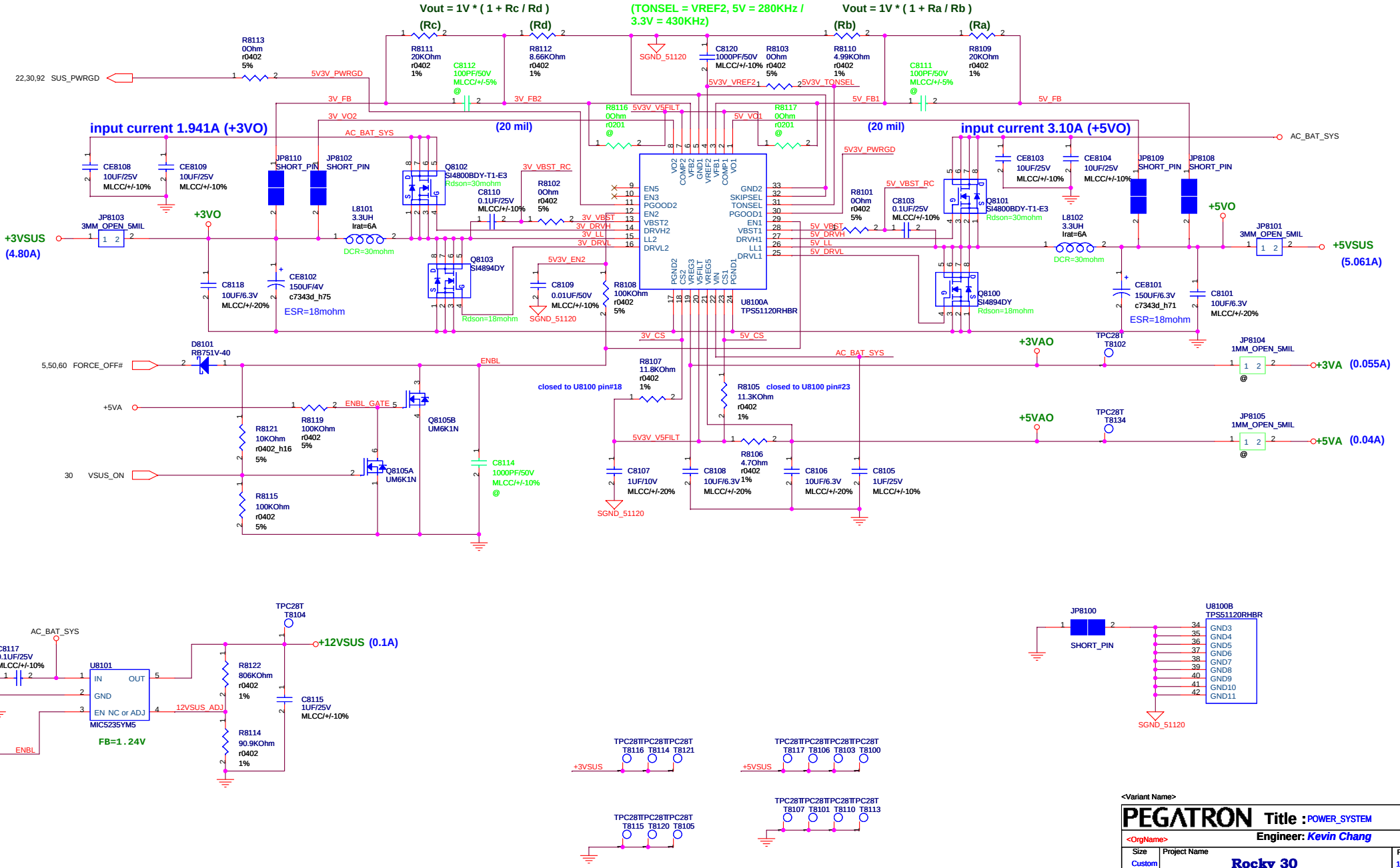
VPS=-2.1mV/A

Max input ripple: 5.59A

Max input ripple: 5.59A

PEGATRON	Title : POWER_VCORE
<OrgName>	Engineer: Kevin Chang
Size: Custom	Project Name: Rocky 30
Rev: 1.1	
Date: Monday, February 04, 2008	Sheet 80 of 94

+5V / +3.3V POWER SUPPLY



<Variant Name>

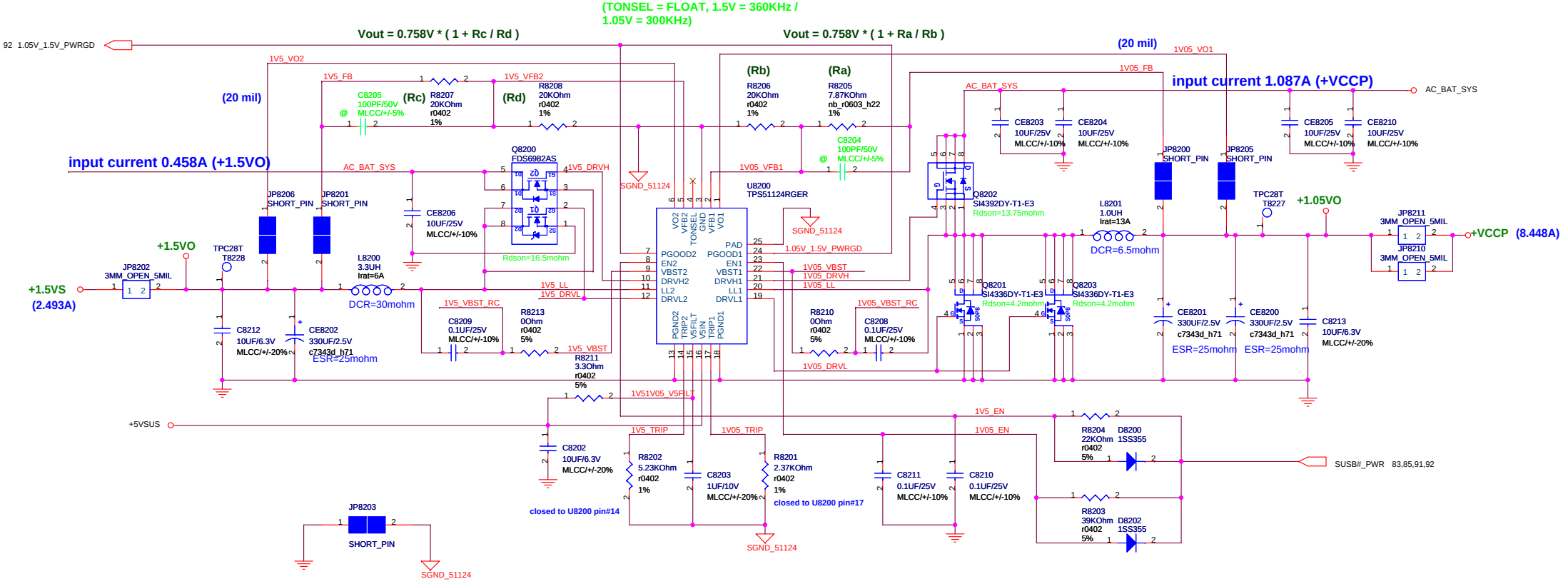
PEGATRON Title : POWER_SYSTEM

<OrgName> Engineer: Kevin Chang

Size	Project Name	Rev
Custom	Rocky 30	1.1

Date: Monday, February 04, 2008 Sheet 81 of 94

+1.5VS / +VCCP POWER SUPPLY



<Variant Name>

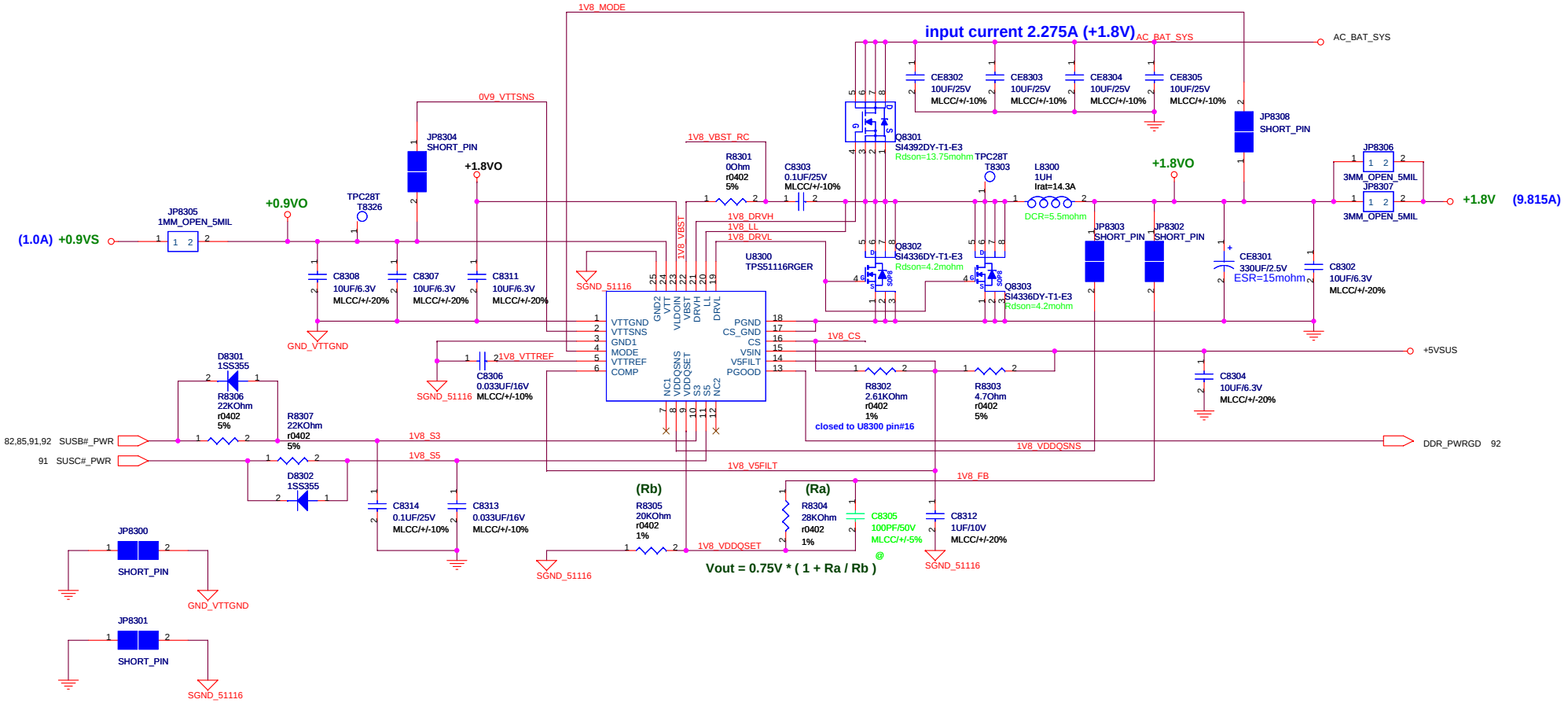
PEGATRON Title : POWER_I/O_1.5VS & 1.05VS

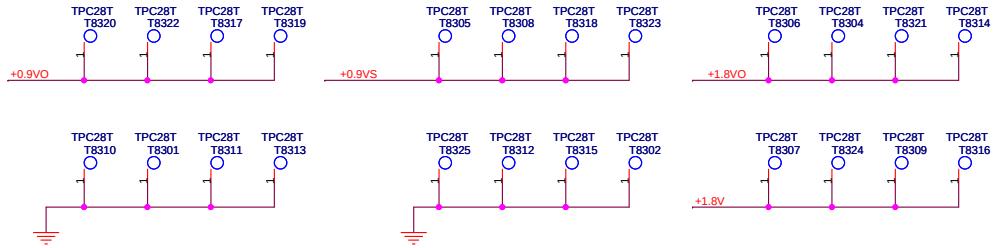
<OrgName> Engineer: Kevin Chang

Size	Project Name	Rev
Custom	Rocky 30	1.1

Date: Monday, February 04, 2008 Sheet 82 of 94

+1.8V / +0.9VS POWER SUPPLY





<Variant Name>

PEGATRON Title : POWER_I/O_DDR & VTT

<OrgName> Engineer: Kevin Chang

Size	Project Name	Rev
Custom	Rocky 30	1.1

Date: Monday, February 04, 2008 Sheet 83 of 94

PEGATRON Title : PWR_-****

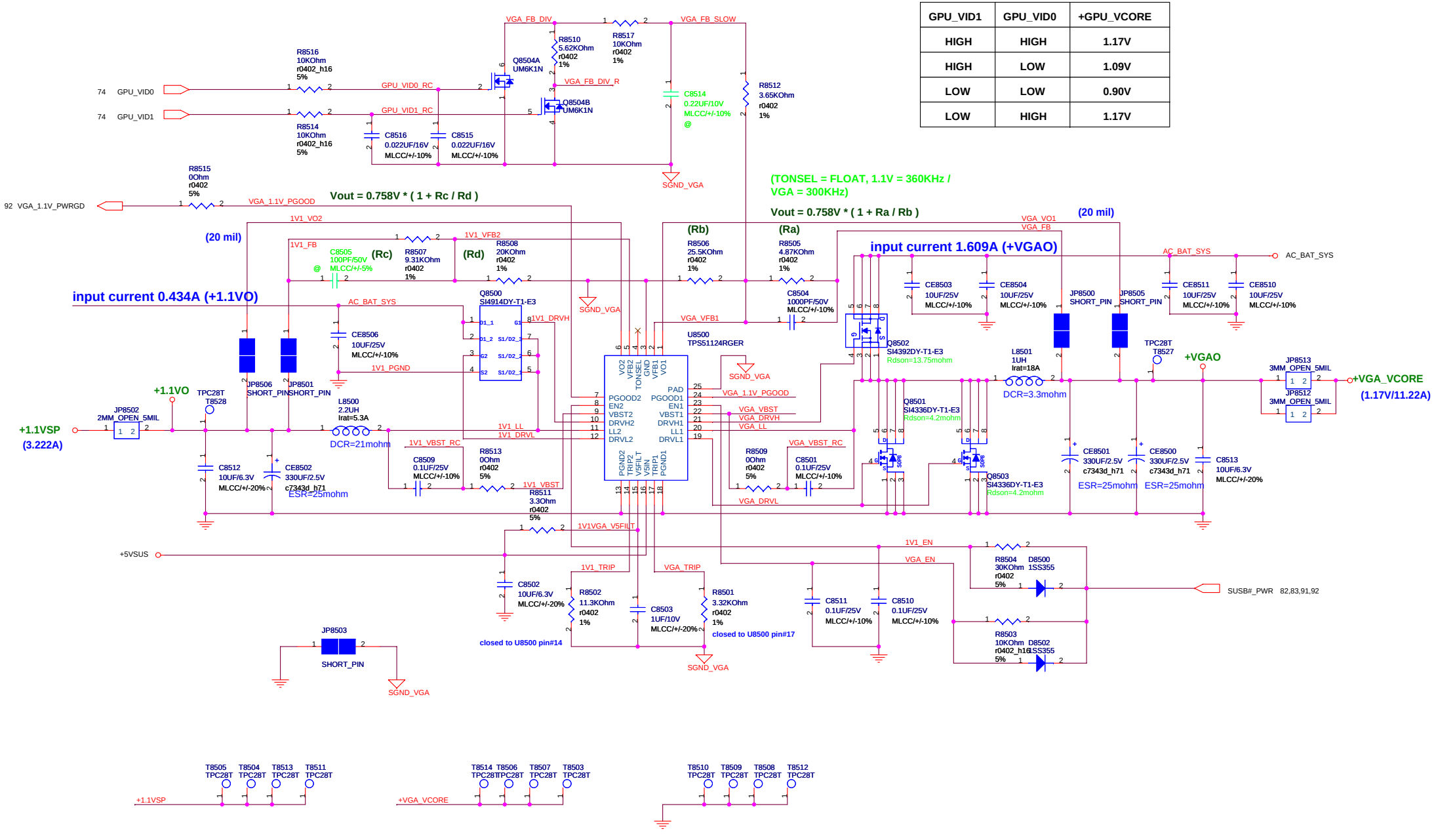
<OrgName> Engineer:

Size	Project Name	Rev
A4	Rocky30	1.1

Date: Saturday, January 26, 2008 Sheet 84 of 94

VGA / +1.1V POWER SUPPLY

GPU_VID1	GPU_VID0	+GPU_VCORE
HIGH	HIGH	1.17V
HIGH	LOW	1.09V
LOW	LOW	0.90V
LOW	HIGH	1.17V



PEGATRON Title : POWER_VGA & +1.1V

<OrgName> Engineer: Kevin Chang

Size	Project Name	Rev
Custom	Rocky 30	1.1

Date: Monday, February 04, 2008 Sheet 85 of 94

PEGATRON Title : PWR_-****

<OrgName> Engineer: Kevin Chang

Size	Project Name	Rev
A4	Rocky30	1.1

Date: Saturday, January 26, 2008 Sheet 86 of 94

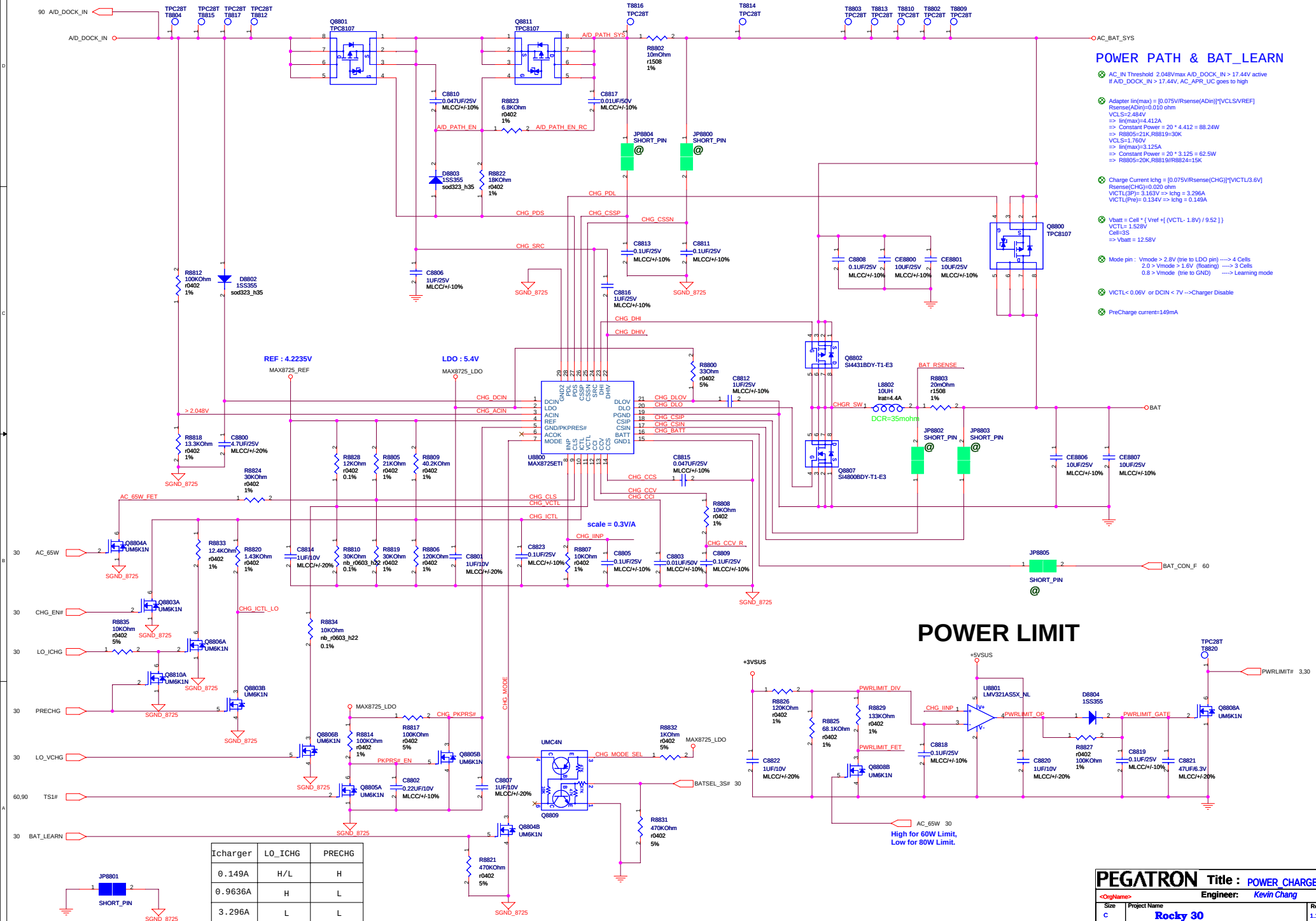
PEGATRON Title : POWER_SHUTDOWN#

<OrgName> Engineer: Kevin Chang

Size	Project Name	Rev
Custom	Rocky30	1.1

Date: Saturday, January 26, 2008 Sheet 87 of 94

BATTERY CHARGER



Icharger	LO_ICHG	PRECHG
0.149A	H/L	H
0.9636A	H	L
3.296A	L	L

PEGATRON	Title :	POWER_CHARGER
<OrgName>	Engineer:	Kevin Chang
Size: C	Project Name: Rocky 30	Rev: 1.1
Date: Monday, February 04, 2008	Sheet 88 of 94	

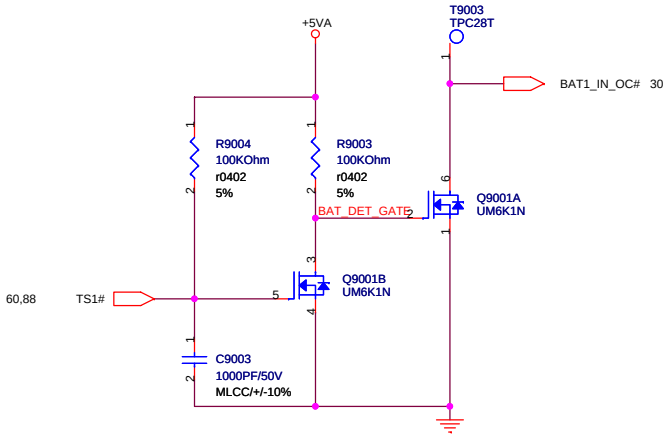
PEGATRON Title : TFT-LCD DRIVE

<OrgName> Engineer:

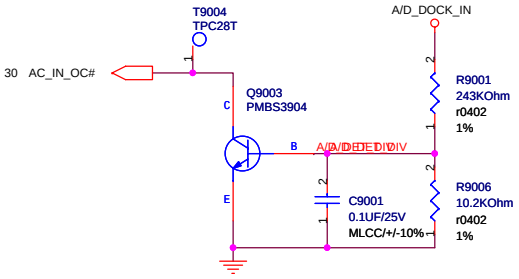
Size	Project Name	Rev
A4	Rocky30	1.1

Date: Saturday, January 26, 2008 Sheet 89 of 94

BATTERY IN DETECT

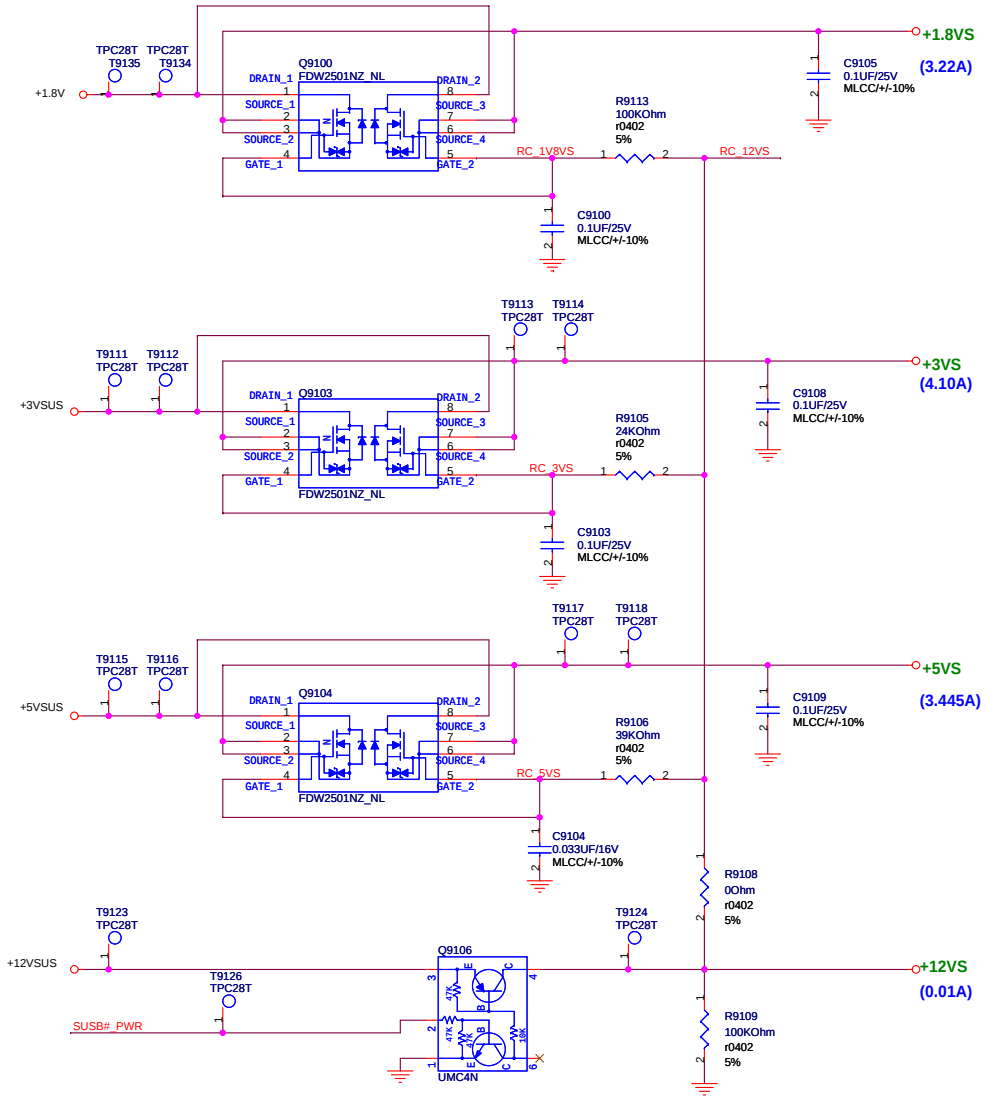


ADAPTER IN DETECT

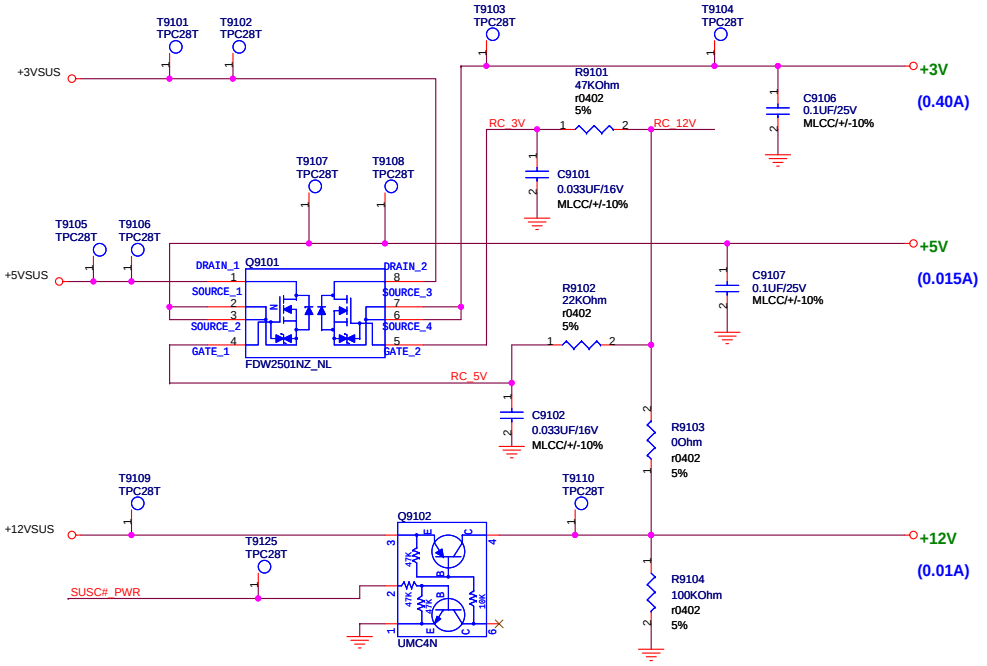


PEGATRON	Title : POWER_DETECT	
<OrgName>	Engineer: Kevin Chang	
Size: A3	Project Name: Rocky 30	Rev: 1.1
Date: Monday, February 04, 2008	Sheet 90 of 94	

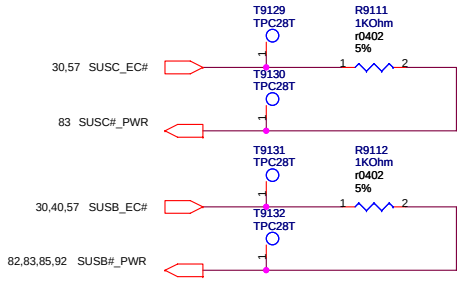
SUSB#_PWR Load SW



SUSC#_PWR Load SW



Enable Signal



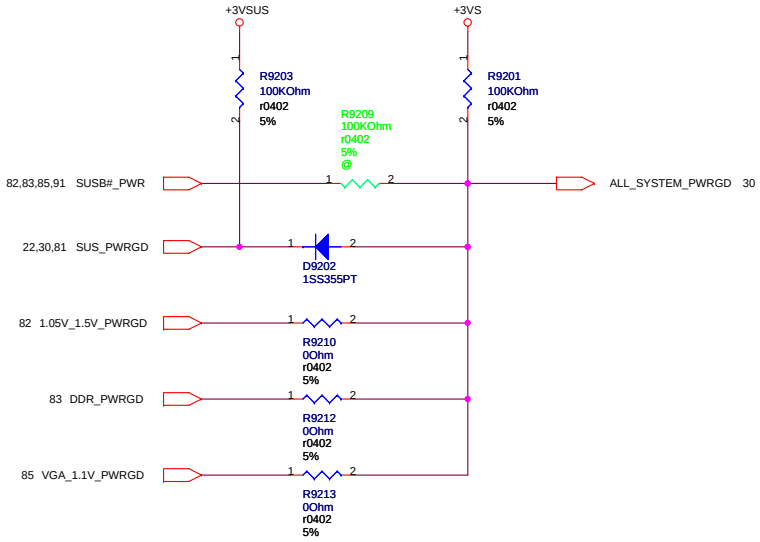
PEGATRON Title : POWER_LOAD SWITCH

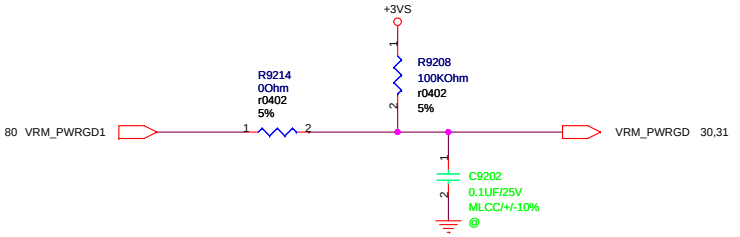
<OrgName> Engineer: Kevin Chang

Size	Project Name	Rev
Custom	Rocky 30	1.1

Date: Monday, February 04, 2008 Sheet 91 of 94

POWER GOOD DETECTER





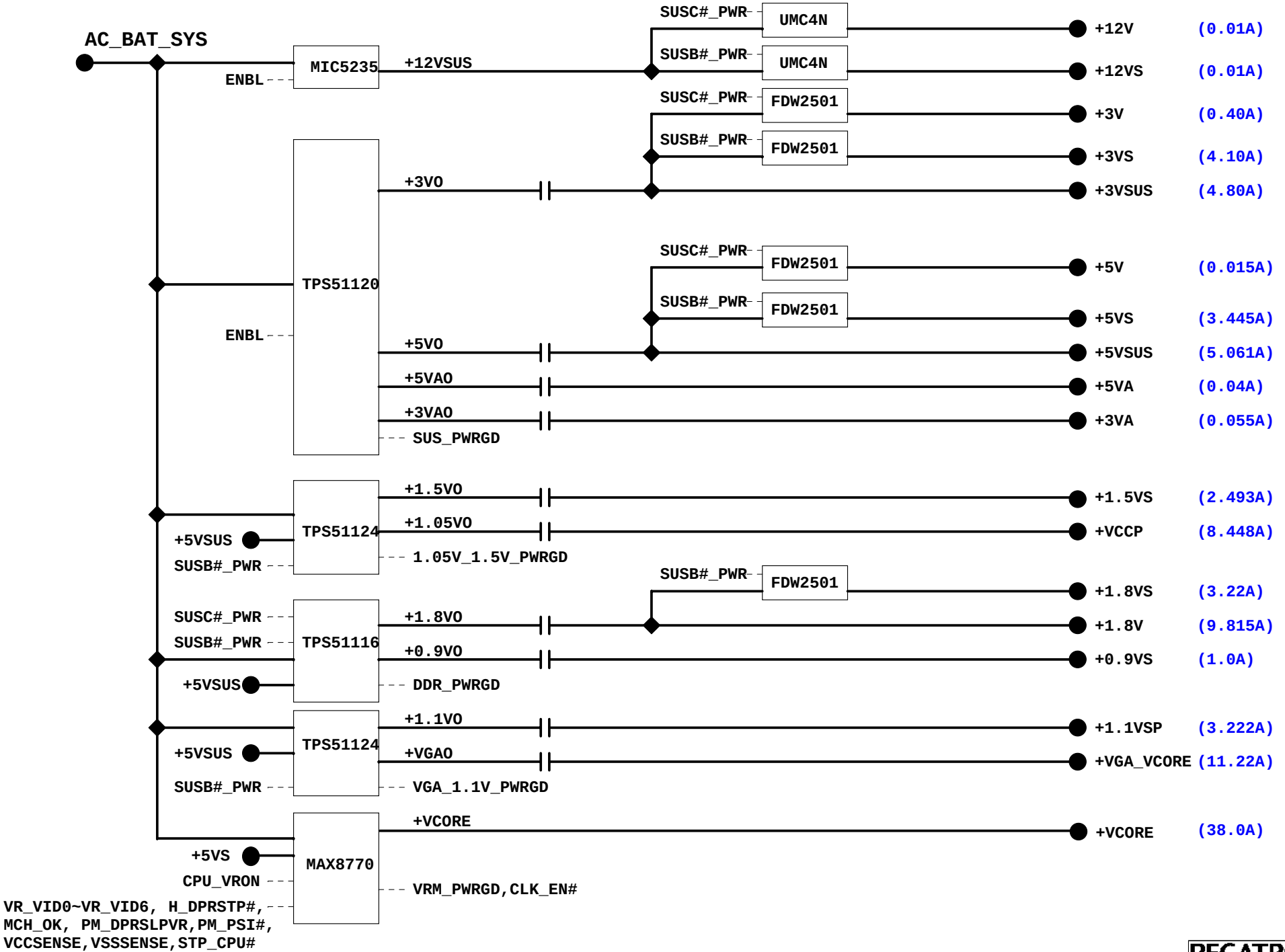
PEGATRON	Title : POWER_PROTECT	
<OrgName>	Engineer: Kevin Chang	
Size: Custom	Project Name: Rocky 30	Rev: 1.1
Date: Monday, February 04, 2008	Sheet 92 of 94	

PEGATRON **Title :** POWER_SIGNAL

<OrgName> **Engineer:** Kevin Chang

Size	Project Name	Rev
Custom	Rocky 30	1.1

Date: Monday, February 04, 2008 Sheet 93 of 94



PEGATRON	Title : POWER_FLOWCHART		
<OrgName>	Engineer: Kevin Chang		
Size: Custom	Project Name: Rocky 30		Rev: 1.1
Date: Saturday, January 26, 2008	Sheet 94 of 94		