

深圳市阿美林电子科技有限公司
Shenzhen Amelin Electronic Technology Co. Ltd.

APPROVAL SHEET
承 认 书

Customer 客户名称	
Part NO. 产品型号	AMLT10850B-V11-1Z
Product type 产品内容	Mode: Transmissive type .Normally white. TFT LCD Module LCD Module: Graphic 1024RGB*600Dot-matrix
Remarks 备注栏	<input type="checkbox"/> APPROVAL FOR SEPCIFICATIONS ONLY <input checked="" type="checkbox"/> APPROVAL FOR SEPCIFICATIONS AND SAMPLE
Signature by Customer: 客户确认签章	

Issued by	Checked by	Approved by	
		PD	QA

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RECORD OF REVISION

Version	Revision Date	Contents	Editor
A00	2014-6-17	New Release	CZS

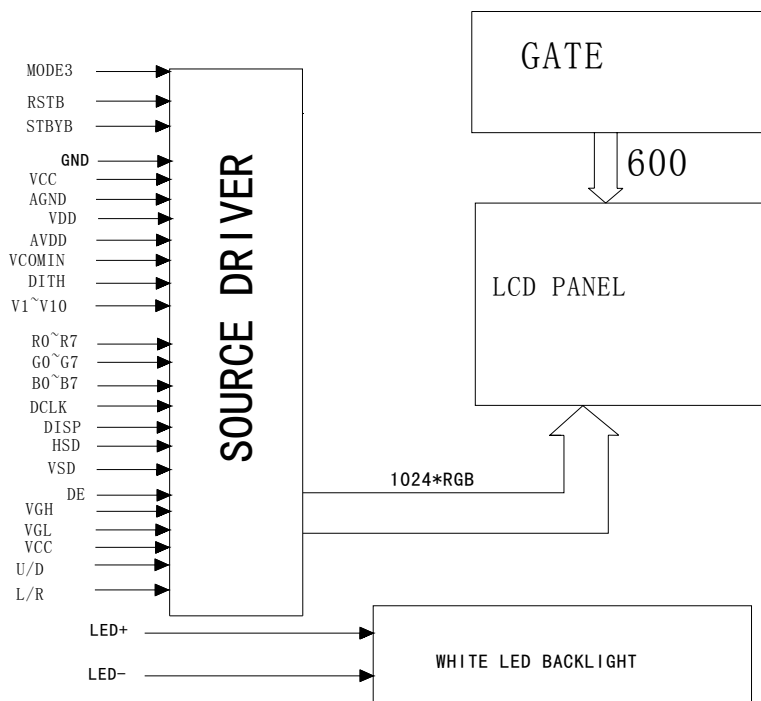
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1. PHYSICAL DATA

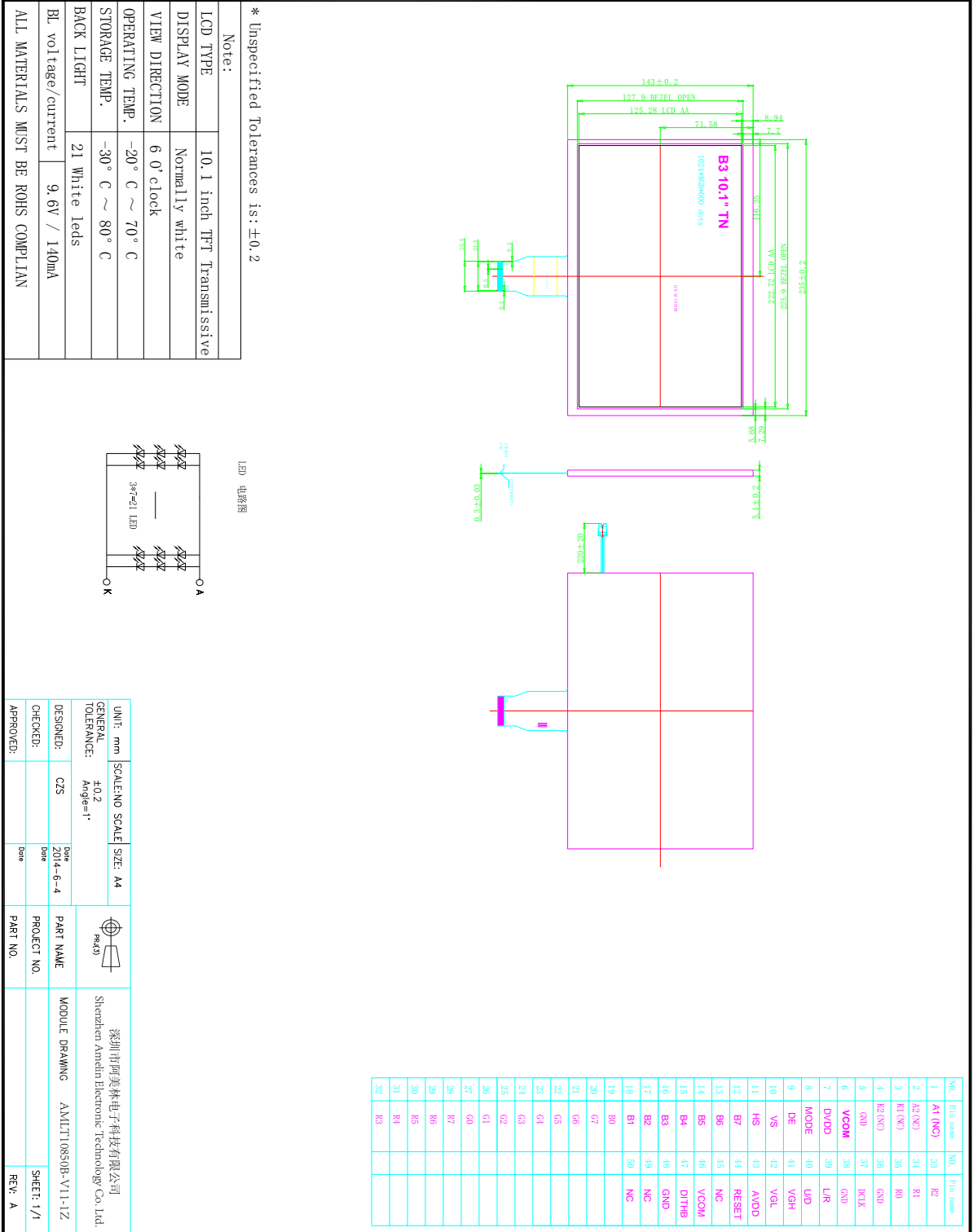
Item	Contents	Unit
LCD type	TFT TRANSMISSIVE	---
Viewing direction	6	o'clock
Module size (W×H×T)	235 × 143 × 5.1	mm ³
Active area(W×H)	222.72×125.28	mm ²
Number of dots(W×H)	1024(RGB) × 600	dots
Pixel Pitch(H×V)	0.2175×0.2088	mm
Driver IC	EK79001A	---
Colors	16M	---
Backlight Type	21white leds 9.6V 140mA	---
Interface Type	RGB	---

2. BLOCK DIAGRAM



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3. Mechanical Dimension



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4. Pin Descriptions

Pin No.	Symbol	Functional
1	LED A	LED Anode
2	LED A	LED Anode
3	LED K	LED Cathode
4	LED K	LED Cathode
5	GND	Digital Ground
6	VCOM	For external VCOM DC input
7	DVDD	Digital Power
8	MODE	DE/SYNC mode select MODE=H: DE mode(normally pull high) MODE=L: HSD/VSD mode
9	DE	Data enable signal
10	VSYNC	Vertical sync input.Negative polarity
11	HSYNC	Horizontal sync input.Negative polarity
12~19	B7~B0	Blue data Input
20~27	G7~G0	Green data Input
28~35	R7~R0	Red data Input
36	GND	Digital Ground
37	DCLK	Clock input
38	GND	Digital Ground
39	L/R	Source right or left sequence control SHLR=H: right shift, Left → Right SHLR=L: left right, Right → Left
40	U/D	Gate up or down scan control UPDN=H: up shift, Down → Up UPDN=L: down shift, Up → Down
41	VGH	Positive Power for TFT
42	VGL	Negative Power for TFT
43	AVDD	Analog Power
44	RSTB	Global reset pin.Active low to enter reset state Suggest to connecting with an RC reset circuit for stability. Normally pull high. (RC circuit :R=10KΩ , C=1uF)
45	NC	Not connect
46	VCOM	For external VCOM DC input
47	DITHB	Dithering setting
48	GND	Digital Ground
49	NC	Not connect
50	NC	Not connect

5. ABSOLUTE MAXIMUM RATINGS

5.1 (GND=AGND=0V)

Parameter	Symbol	Min	Max	Unit
Power supply1	V _{DD}	-0.5	+3.96	V
Power supply2	A _{vdd}	-0.5	+14.85	V
Logic output voltage	V _{out}	-0.5	+5.0	V
Input voltage	V _{in}	-0.5	A _{vdd} +0.5	V
Operating temperature	T _{OPR}	-20	70	°C
Storage temperature	T _{STG}	-30	80	°C

5.2 Input voltage refer list

Parameter	Symbol	Value	Unit	Remarks
TFT Gate ON Voltage	V _{GH}	21	V	
TFT Gate Off Voltage	V _{GL}	-8	V	
TFT Common Electrode Voltage	V _{COM}	3.8	V	
Analog Power Supply Voltage	A _{VDD}	10.85	V	

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6. DC ELECTRICAL CHARACTERISTICS

(VDD=2.3~3.6V, AVDD=6.5~13.5V, GND=AGND=0V, TA=-20°C~+85°C)

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Power supply voltage	VDD	2.3	-	3.6	V	-
Power supply voltage	AVDD	6.5	-	13.5	V	-
Power supply voltage	AVDDL	6.5	-	13.5	V	Full range application
		4	-	6.75	V	Half AVDD application
Power supply voltage	AGNDH	0			V	Full range application
		4	-	6.75	V	Half AVDD application
Low level input voltage	V _{IL}	0	-	0.3VDD	V	For digital circuit
High level input voltage	V _{IH}	0.7VDD	-	VDD	V	For digital circuit
Output low voltage	V _{OL}	-	-	GND+0.4	V	I _{OL} =400μA
Output high voltage	V _{OH}	VDD-0.4	-	-	V	I _{OH} =-400μA
Pull low/high resistance	R _i	200	250	300	kΩ	For the digital input pin @VDD=3.3V
Input leakage current	I _i	-	-	±1	μA	For digital circuit
Digital Operation current	I _{dd}	-	12	20	mA	Fclk=50MHz, LD=48KHz, VDD=3.3V, No load
Digital stand-by current	I _{st1}	-	10	50	μA	Clock & all functions are stopped
Analog Operating current	I _{dda}	-	8	10	mA	No load, Fclk=50MHz, LD=48KHz @ AVDD=10V, V1=8V, V14=0.4V
Analog Stand-by current	I _{st2}	-	10	50	μA	No load, clock & all functions are stopped
Input level of V1~V7	V _{ref1}	0.4AVDD	-	AVDD-0.1	V	Gamma correction voltage input
Input level of V8~V14	V _{ref2}	0.1	-	0.6AVDD	V	Gamma correction voltage input
Output Voltage deviation	V _{od1}	-	±20	±35	mV	V _o =AGND+0.1V~AGND+0.5V & V _o =AVDD-0.5V~AVDD-0.1V
Output Voltage deviation	V _{od2}	-	±15	±20	mV	V _o =AGND+0.5V~AVDD-0.5V
Output Voltage Offset between Chips	V _{oc}	-	-	±20	mV	V _o =AGND+0.5V~AVDD-0.5V
Dynamic Range of Output	V _{dr}	0.1	-	AVDD-0.1	V	SO1~SO1200
Sinking Current of Outputs	I _{OLy}	80	-	-	μA	SO1~SO1200; V _o =0.1V vs. 1.0V, AVDD=13.5V
Driving Current of Outputs	I _{OHy}	80	-	-	μA	SO1~SO1200; V _o =0.1V vs. 12.5V, AVDD=13.5V
Resistance of Gamma Table	R _g	0.7*R _n	1.0*R _n	1.3*R _n	Ω	R _n : Internal gamma resistor

7. TTL MODE AC ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
VDD Power On Slew rate	T _{POr}	-	-	20	ms	From 0V to 90% VDD
RSTB pulse width	T _{Rst}	50	-	-	μs	DCLK=65MHz
DCLK cycle time	T _{cpH}	14	-	-	ns	-
DCLK pulse duty	T _{cpw}	40	50	60	%	-
VSD setup time	T _{vst}	5	-	-	ns	-
VSD hold time	T _{vhd}	5	-	-	ns	-
HSD setup time	T _{hst}	5	-	-	ns	-
HSD hold time	T _{hhd}	5	-	-	ns	-
Data set-up time	T _{dsu}	5	-	-	ns	D0[7:0], D1[7:0], D2[7:0] to DCLK
Data hold time	T _{dhd}	5	-	-	ns	D0[7:0], D1[7:0], D2[7:0] to DCLK
DE setup time	T _{esu}	5	-	-	ns	-
DE hold time	T _{ehd}	5	-	-	ns	-
Output stable time	T _{sst}	-	-	6	μs	10% to 90% target voltage. CL=90pF, R=10K ohm (Cascade)
				3		

8. Data input format for RGB

8.1 For 24-Bit RGB input

Vertical timing

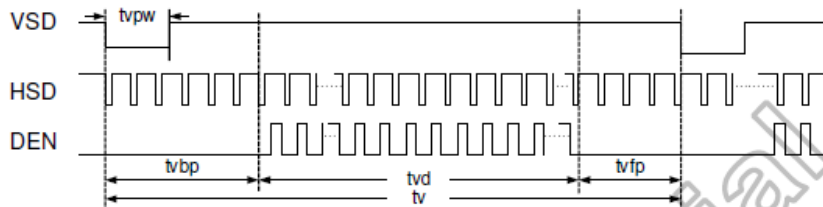


Figure 10.2: Vertical input timing diagram

Horizontal timing

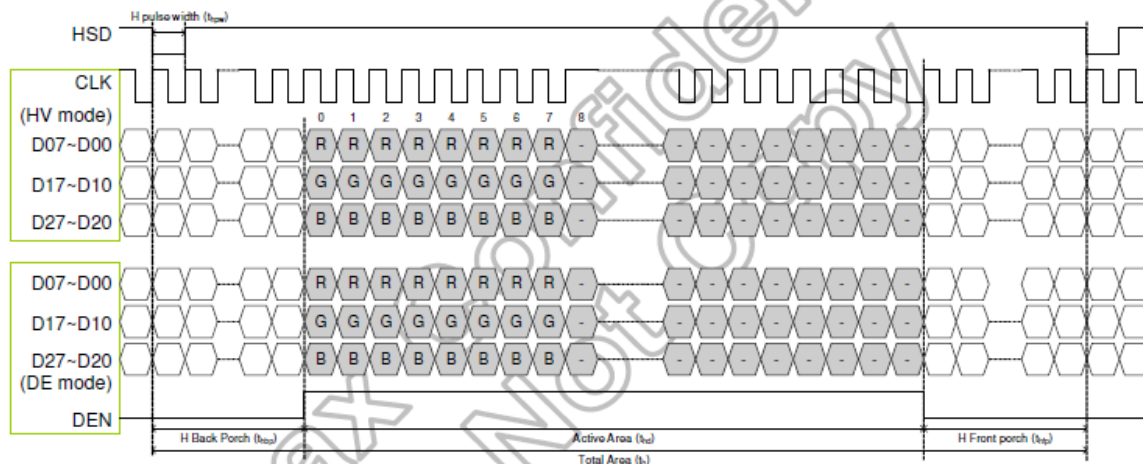


Figure 10.3: Horizontal input timing diagram

- DE mode

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK Frequency	fclk	40.8	51.2	67.2	MHz
Horizontal Display Area	thd		1024		DCLK
HSD Period	th	1114	1344	1400	DCLK
HSD Blanking	thb+ thfp	90	320	376	DCLK
Vertical Display Area	tvd		600		T _H
VSD Period	tvbp	610	635	800	T _H
VSD Blanking	tvbp+ tvfp	10	35	200	T _H

Table 10.4: DE mode (1024x600)

● HV mode

Horizontal timing

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
DCLK Frequency	fclk	44.9	51.2	63	MHz
Horizontal Display Area	thd		1024		DCLK
HSD Period	th	1200	1344	1400	DCLK
HSD Pulse Width	thpw	1	-	140	DCLK
HSD Back Porch	thbp		160		DCLK
HSD Front Porch	thfp	16	160	216	DCLK

Table 10.5: HV mode horizontal timing (1024x600)

Vertical Timing

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Vertical Display Area	tvd		600		T _H
VSD Period	tv	624	635	750	T _H
VSD Pulse Width	tvpw	1	-	20	T _H
VSD Back Porch	tvbp		23		T _H
VSD Front Porch	tvfp	1	12	127	T _H

Table 10.6: HV Mode Vertical Timing (1024x600)

9. Backlight Characteristic

Item	Symbol	Min	Typical	Max	Unit
LED module Forward voltage	V _{LED}	--	9.6		V
LED module current	I _{LED}	--	140	--	mA
L/G Surface Luminance ★1	L _S	--	TBD	--	mcD
LCM Surface brightness uniform ★2	L _D	80	--	--	%

★ 1 Test condition is:

(a) Center point on active area.

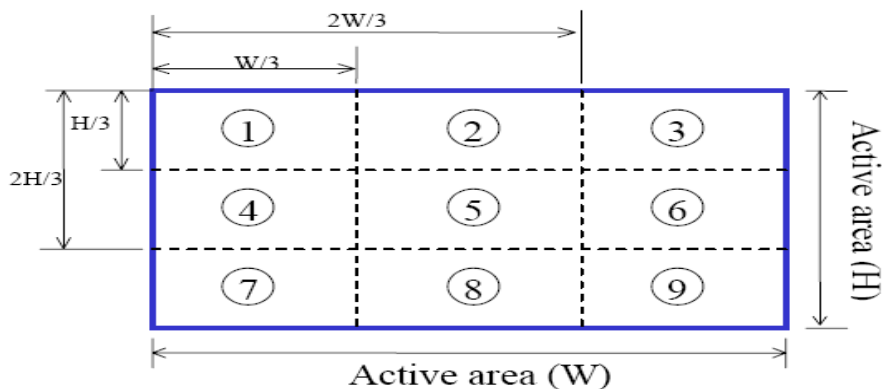
(b) Best Contrast.

★2 Uniform measure condition:

(1) Measure 9 point. Measure location show below;

(2) Uniform = (Min. brightness / Max. brightness) * 100%

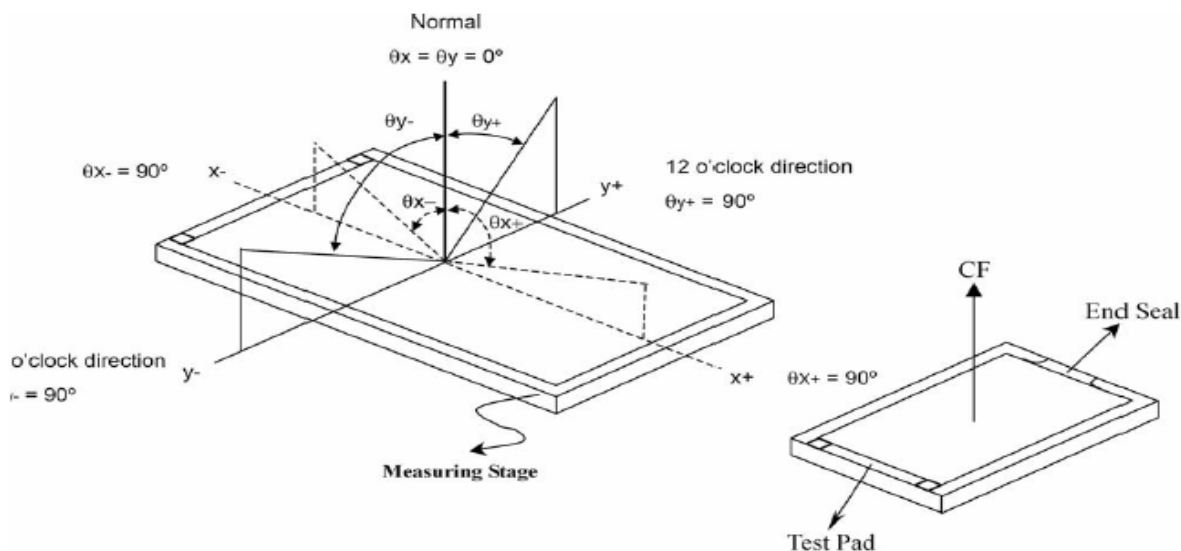
(3) Best Contrast.



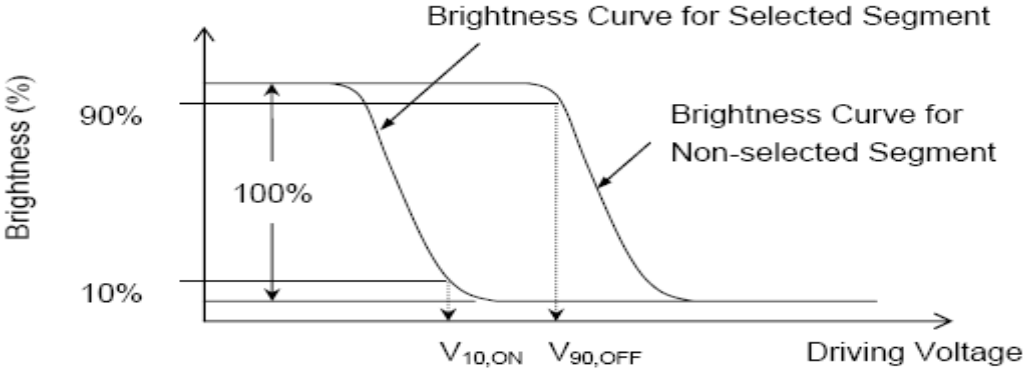
10. Electro-optical Characteristics

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing angle range	Hor.	$\phi 3$	$CR \geq 10$		70		Deg.	Note 3
		$\phi 9$			70		Deg.	
	Ver.	$\phi 12$			60		Deg.	
		$\phi 6$			70		Deg.	
Color gamut (C light)				50		%		
Luminance Contrast ratio		T (%)	$\phi 0^\circ$		600			Note 4
Response Time		TRT	Temp=25° C		8		ms	Note 2

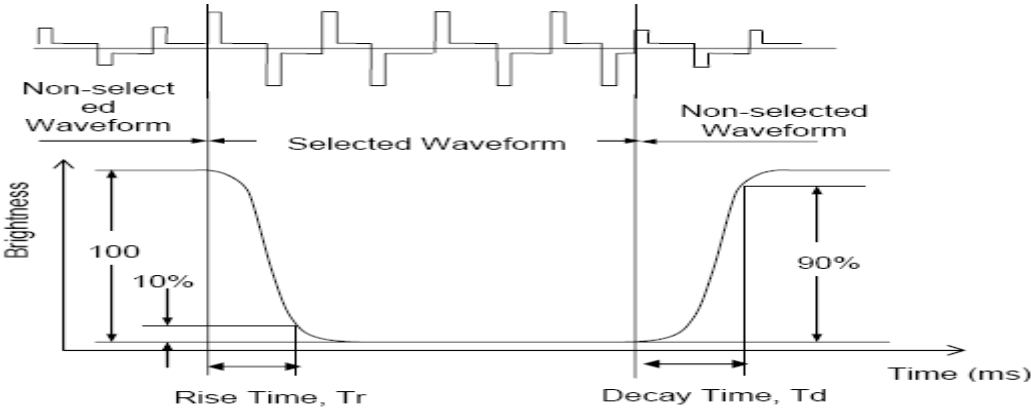
- For panel only
- Electro-Optical Characteristics Test Method



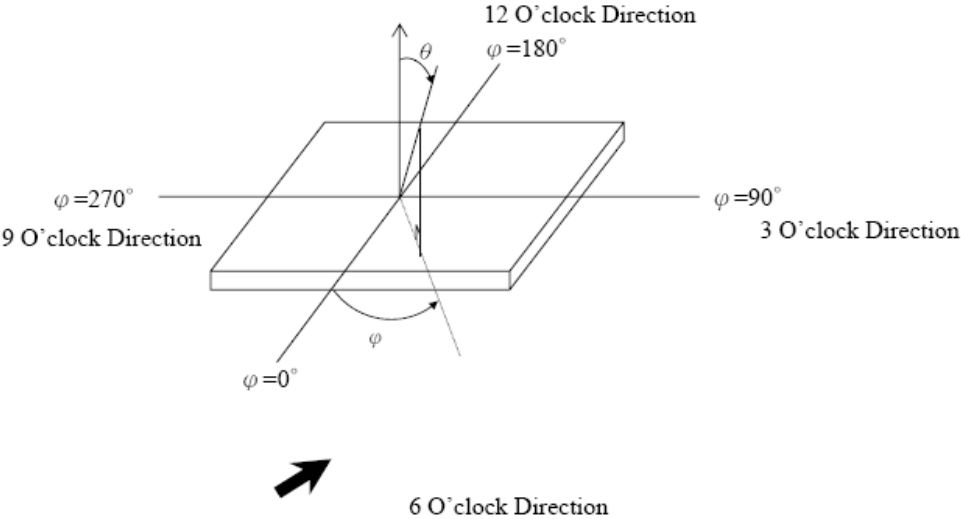
$$V_{OP} = (V_{10, ON} + V_{90, OFF})/2$$



.Note2.Definition of Optical Response Time:

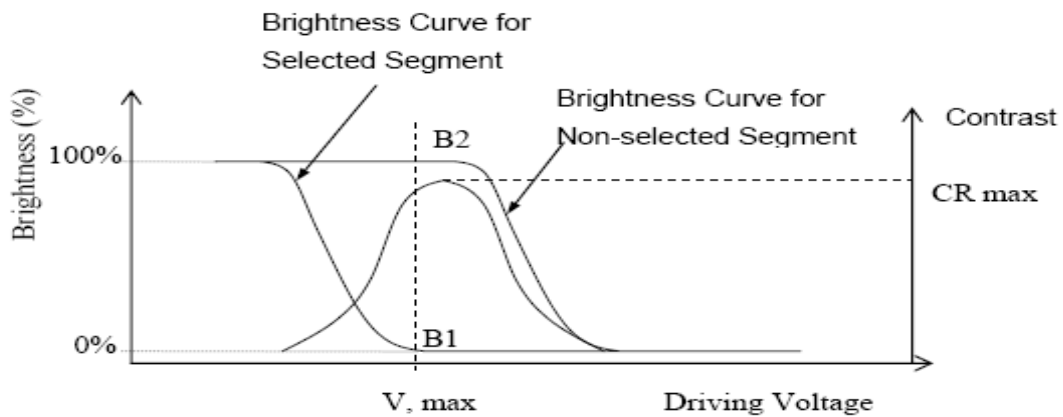


.Note3.Definition of Viewing Angle θ and ϕ :



Note4.Definition of Contrast ratio (CR):

$$CR = \frac{\text{Brightness of Non-selected Segment (B2)}}{\text{Brightness of Selected Segment (B1)}}$$



11. Reliability

11.1 Mtbf

The LCD module shall be designed to meet a minimum MTBF value of 50000 hours with normal

11.2 Test condition

N O.	ITEM	CONDITION	CRITERION
1	High Temperature Non-Operating Test	80°C*240Hrs	◦ No Defect Of Operational Function In Room Temperature Are Allowable ◦ IDD of LCM in Pre-and Post-Test Should Follow Specification
2	Low Temperature Non-Operating Test	-30°C*240Hrs	
3	High Temperature/Humidity Non Operating Test	60°C*90%RH*240Hrs	
4	High Temperature Operating Test	70°C*240Hrs	
5	Low Temperature Operating Test	-20°C*240Hrs	
6	Thermal Shock Test	-20 °C (30Min) ↔ 70 °C (30Min) *10CYCLES	

Notes:

1. Judgments should be made after exposure in room temperature for two hours.
2. The distill water is used for the high temperature/humidity test.
3. The sample above is individually for every reliability tests condition.

12. Inspection standards

- 1.AQL(Acceptable Quality Level)

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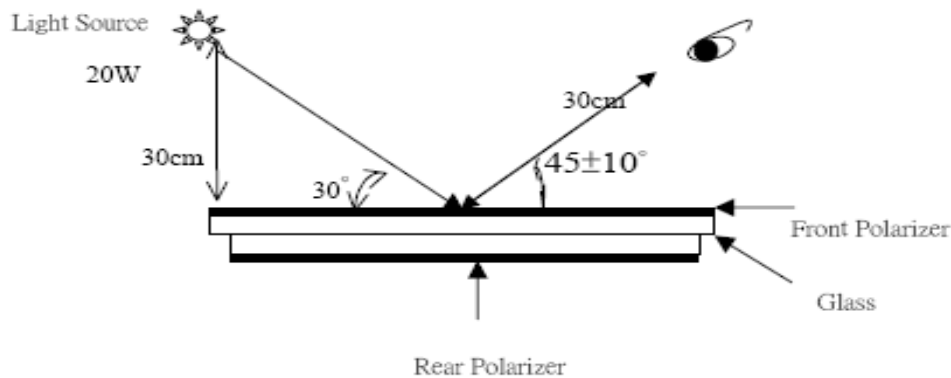
AQL of major and minor defect.

	MAJOR DEFECT	MINOR DEFECT
AQL	0.65	1.5

2. Basic conditions for inspection

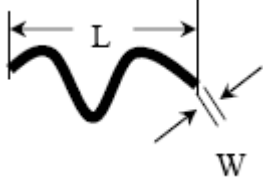
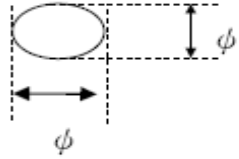
The LCM face to us, in normal environment, the lux is 1000 ± 200 . (Darkroom's lux: 100 ± 50), About an angle of incidence 30° , a distance of 30 cm with an angle of $45 \pm 10^\circ$ to check the products without uncovering the film!

(As shown below)



3. Inspection item and criteria

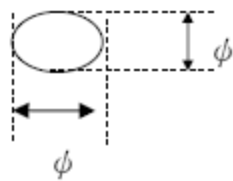
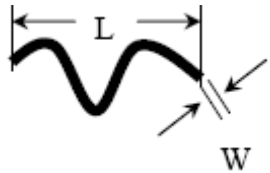
3.1 LCD appearance defect (View area)

NO	Defect item	Criteria		Remark
		Specification	Allowable	
1	Fiber, glass cratch, polarizer scratch/folded (minor defect)	$W \leq 0.03\text{mm}$	disregard	note1: L: Length, W: Width note2: disregard if out of AA 
		$0.03\text{mm} < W \leq 0.05\text{mm};$ $L \leq 3.0\text{mm}$	2	
		$0.05\text{mm} < W \leq 0.1\text{mm};$ $L \leq 3.0\text{mm}$	1	
		$W > 0.1\text{mm}; L > 3.0\text{mm}$	0	
2	Polarizer bubble, concave and convex (minor defect)	$\phi \leq 0.2\text{mm}$	disregard	note1: $\phi = (L+W)/2$, L: Length, W: Width note2: disregard if out of AA
		$0.2\text{mm} < \phi \leq 0.3\text{mm}$	2	
		$0.3\text{mm} < \phi \leq 0.5\text{mm}$	1	
		$0.5\text{mm} < \phi$	0	
3	Black dots, dirty dots, impurities, eye winker (minor defect)	$\phi \leq 0.15\text{mm}$	disregard	note2: disregard if out of AA 
		$0.15\text{mm} < \phi \leq 0.25\text{mm}$	2	
		$0.25\text{mm} < \phi \leq 0.3\text{mm}$	1	
		$0.3\text{mm} < \phi$	0	
4	Polarizer prick (minor defect)	$\phi \leq 0.1\text{mm}$	disregard	note1: $\phi = (L+W)/2$, L=Length, W=Width note2: the distance between two dots $> 5\text{mm}$
		$0.1\text{mm} < \phi \leq 0.25\text{mm}$	3	
		$\phi > 0.25\text{mm}$	0	

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3.2 Electrical criteria

NO	Defect item	Criteria	Remark	
1	No display (major defect)	No display 【Reject】		
2	Missing line (major defect)	Missing line 【Reject】		
3	Seg-com light and dark (major defect)	Seg-com light and dark 【Reject】	ND filter 2% test	
4	No display in immobility (major defect)	No display in immobility 【Reject】		
5	Flicker of Pattern (major defect)	Flicker of Pattern 【Reject】		
6	Mura (major defect)	ND filter 2% test		
7	Over current (major defect)	Over current 【Reject】		
8	Voltage out of specification (major defect)	Voltage out of specification 【Reject】		
9	Pattern blur, error code (major defect)	Pattern blur, error code 【Reject】		
10	Dark light, Flicker (major defect)	Dark light, Flicker 【Reject】		
11	Black/white dots 、 Dirty dots、 eye winker (major defect)	Specification	Allowable	Note1:disregard if out of AA 
		$\phi \leq 0.15\text{mm}$	disregard	
		$0.15\text{mm} < \phi \leq 0.25\text{mm}$	2	
		$0.25\text{mm} < \phi \leq 0.3\text{mm}$	1	
		$0.3\text{mm} < \phi$	0	
12	Fiber、glass crutch、Polarizer scratch/folded (major defect)	$W \leq 0.03\text{mm}$	disregard	Note1:L: Length, W: Width Note2: disregard if out of AA 
		$0.03\text{mm} < W \leq 0.05\text{mm}$ $L \leq 3.0\text{mm}$	2	
		$0.05\text{mm} < W \leq 0.1\text{mm}$ $L \leq 3.0\text{mm}$	1	
		$W > 0.1\text{mm}; L > 3.0\text{mm}$	0	

13.Precautions for using LCD modules.

13.1 Safety

- (1) Do not swallow any liquid crystal, even if there is no proof that liquid crystal is poisonous.
- (2) If the LCD panel breaks, be careful not to get liquid crystal to touch your skin.
- (3) If skin is exposed to liquid crystal, wash the area thoroughly with alcohol or soap.

13.2 Storage Conditions

- (4) Store the panel or module in a dark place where the temperature is $23 \pm 5^{\circ}\text{C}$ and the humidity is below $45 \pm 20\% \text{RH}$.
- (5) Store in anti-static electricity container.
- (6) Store in clean environment, free from dust, active gas, and solvent.
- (7) Do not place the module near organics solvents or corrosive gases.
- (8) Do not crush, shake, or jolt the module.

13.3 Handling Precautions

- (9) Avoid static electricity, which can damage the CMOS LSI.
- (10) The polarizing plate of the display is very fragile, please handle it very carefully.
- (11) Do not give external shock.
- (12) Do not apply excessive force on the surface.
- (13) Do not wipe the polarizing plate with a dry cloth, as it may easily scratch the surface of plate.
- (14) Do not use ketonic solvent & Aromatic solvent, use with a soft cloth soaked with a cleaning naphtha solvent.
- (15) Do not operate it above the absolute maximum rating.
- (16) Do not remove the panel or frame from the module.

13.4 Warranty

The period is within twelve months since the date of shipping out under normal using and storage conditions.