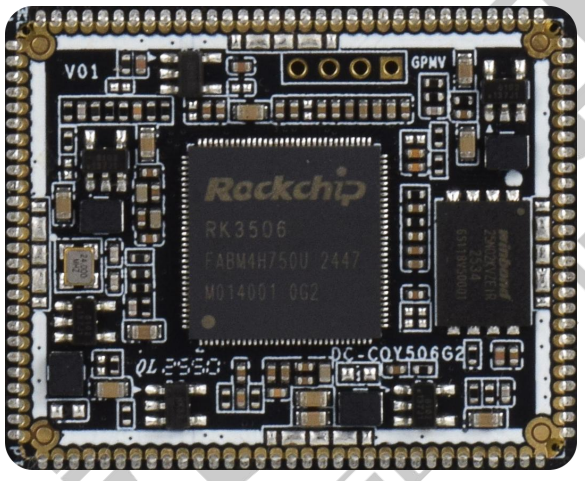
DC-CY506G2-V01

产品规格书



版本	日期	变更内容
V1.0	2026-1-10	初版

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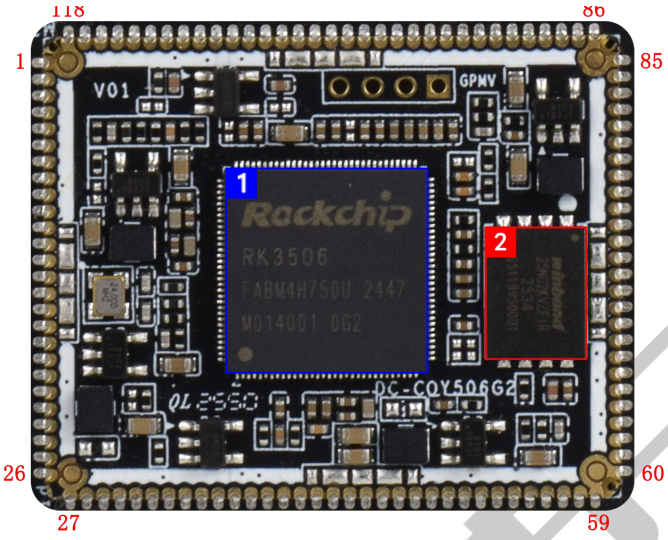
定昌电子 DINGCHANG DIANZI

第一章 产品概述

1.1、概述

DC-CY506G2，采用瑞芯微一款高性能三核 Cortex-A7 应用处理器 RK3506G2，专为智能语音交互、音频输入/输出处理、图像输出处理及其他数字多媒体应用而设计。内置 2D 硬件引擎与显示输出引擎，有效降低 CPU 开销，满足图像显示需求。

第二章 外观示意图

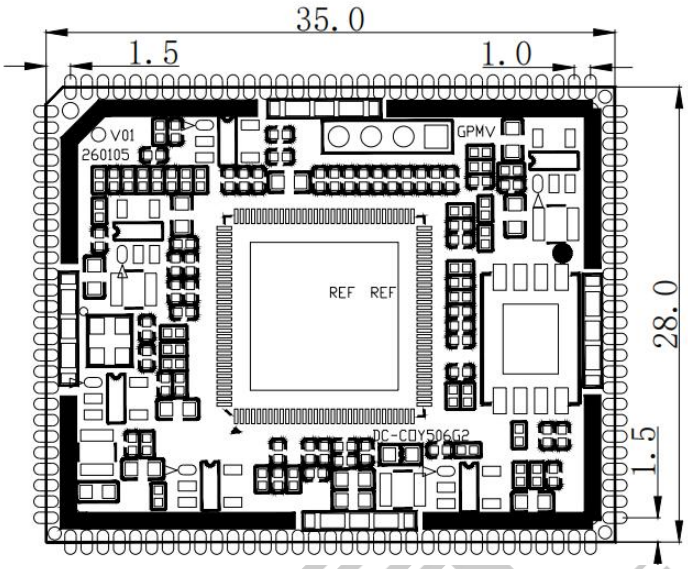


1 RK3506G2　　2 FLASH

第三章 主板规格

3.1、PCB 尺寸图

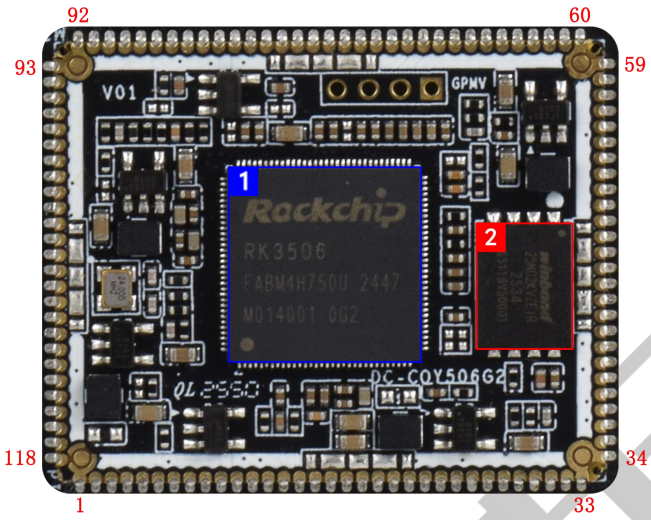
单位：mm



3.2、规格参数

主板尺寸： 35*28*4mm
主板高度： 正面≤1.5mm，背面≤2mm
PCB 层数： 4 层
PCB 尺寸： 35*28*1.6mm
PCB 颜色： 黑色
PCB 工艺： 沉金

第四章 引脚定义



1 RK3506G2 2 FLASH

NOTE:※ is RM_IO List of optional

Pin	Net Name	Corresponding to GPIO	Pad type	IO Pull	Default function description	IO Power domain
1	GND	GND			GND	
2	GND	GND			GND	
3 ※	CAN1_RX	GPIO1_B2_d	I		Support CAN 2.0B protoco	3.3V
4 ※	CAN1_TX	GPIO1_B3_d	O		Support CAN 2.0B protoco	3.3V
5	VO_LCDC_D15	GPIO1_B4_d	I/O		LCDC RGB interface data output, MCU interfacedata input/output	3.3V
6	VO_LCDC_D14	GPIO1_B5_d	I/O		LCDC RGB interface data output, MCU interfacedata input/output	3.3V
7	VO_LCDC_D13	GPIO1_B6_d	I/O		LCDC RGB interface data output, MCU interfacedata input/output	3.3V
8	VO_LCDC_D12	GPIO1_B7_d	I/O		LCDC RGB interface data output, MCU interfacedata input/output	3.3V
9	VO_LCDC_D11	GPIO1_C0_d	I/O		LCDC RGB interface data output, MCU interfacedata input/output	3.3V
10	VO_LCDC_D10	GPIO1_C1_d	I/O		LCDC RGB interface data output, MCU interfacedata input/output	3.3V
11	GND	GND			GND	
12 ※	UART4_TX	GPIO1_C2_d	O		UART4 serial data output	3.3V
13 ※	UART4_RX	GPIO1_C3_d	I		UART4 serial data input	3.3V
14	VO_LCDC_D7	GPIO1_C4_d	I/O		LCDC RGB interface data output, MCU interfacedata input/output	3.3V
15	GND	GND			GND	
16	VO_LCDC_D6	GPIO1_C5_d	I/O		LCDC RGB interface data output, MCU interfacedata input/output	3.3V
17	VO_LCDC_D5	GPIO1_C6_d	I/O		LCDC RGB interface data output, MCU interfacedata input/output	3.3V
18	VO_LCDC_D4	GPIO1_C7_d	I/O		LCDC RGB interface data output, MCU	3.3V

					interfacedata input/output	
19	VO_LCDC_D3	GPIO1_D0_d	I/O		LCDC RGB interface data output, MCU interfacedata input/output	3.3V
20 ※	VO_LCDC_D2	GPIO1_D1_d	I/O		LCDC RGB interface data output, MCU interfacedata input/output	3.3V
21 ※	VO_LCDC_D1	GPIO1_D2_d	O		UART5 serial data output	3.3V
22 ※	VO_LCDC_D0	GPIO1_D3_d	I		UART5 serial data input	3.3V
23	OSC_CLK_OUT	GPIO0_D0_d	O		TY8522C reset. Active-low,reset pin for chip.	
24	GND	GND			GND	
25 ※	UART0_RX/JTAG_TMS_M1	GPIO0_C7_u			UART0：UART0 serial data input JTAG:SWD interface data input/output for CPU	3.3V
26 ※	UART0_TX/JTAG_TCK_M1	GPIO0_C6_u			UART0:UART0 serial data output JTAG:SWD interface data input for CPU	3.3V
27	GND	GND			GND	
28	GND	GND			GND	
29 ※	CAN0_RX	GPIO0_C4_d	I		Support CAN 2.0B protoco	3.3V
30 ※	CAN0_TX	GPIO0_C3_d	O		Support CAN 2.0B protoco	3.3V
31 ※	REF_CLK1_OUT	GPIO0_C2_d	I	UP	Interrupt input from RTC chip	
32 ※	UART1_TX	GPIO0_C1_d	O		UART1 serial data output	3.3V
33 ※	UART1_RX	GPIO0_C0_d	I		UART1 serial data input	3.3V
34 ※	UART3_RX	GPIO0_B7_d	I		UART3 serial data input	3.3V
35 ※	UART3_TX	GPIO0_B6_d	O		UART3 serial data output	3.3V
36 ※	9555IO_INT1	GPIO0_B5_d	I	UP	Interrupt input from NCA9555 chip	3.3V
37 ※	SAI1_SDO0	GPIO0_B4_d	O		I2S/PCM/TDM serial data output	3.3V
38 ※	SAI1_SDI	GPIO0_B3_d	I		I2S/PCM/TDM serial data input	3.3V
39 ※	SAI1_LRCK	GPIO0_B2_d	I/O		I2S/PCM/TDM channel indication signal	3.3V
40	GND	GND			GND	
41	NPOR_L	NPOR	I	UP	Chip hardware reset input	
42 ※	SAI1_SCLK	GPIO0_B1_d	I/O		I2S/PCM/TDM serial clock	3.3V
43 ※	SAI1_MCLK	GPIO0_B0_d	I/O		I2S/PCM/TDM master clock	3.3V
44 ※	I2C1_SDA	GPIO0_A7_d	I/O		I2C1 data	3.3V
45 ※	I2C1_SCL	GPIO0_A6_d	I/O		I2C1 clock	3.3V
46 ※	I2C2_SDA	GPIO0_A5_d	I/O	UP	I2C2 data	3.3V
47 ※	I2C2_SCL	GPIO0_A4_d	I/O	UP	I2C2 clock	3.3V
48 ※	PWM0_CH3_IR_RX	GPIO0_A3_d	I/O	UP	Pulse Width Modulation input and output	3.3V
49 ※	UART2_TX	GPIO0_A2_d	O		UART2 serial data output	3.3V
50 ※	PWM0_CH2_LCD_BL	GPIO0_A1_d	I/O	Down	Pulse Width Modulation input and output	3.3V
51 ※	UART2_RX	GPIO0_A0_u	I		UART2 serial data input	3.3V
52	VCC_1V8		O		Core board output power supply	
53	VCC_3V3		O		Core board output power supply	
54	VCC_3V3		O		Core board output power supply	
55	VCC5V0_SYS		I		Power up the core board	
56	VCC5V0_SYS		I		Power up the core board	
57	VCC5V0_SYS		I		Power up the core board	

58	GND	GND			GND	
59	GND	GND			GND	
60	GND	GND			GND	
61	GND	GND			GND	
62	GND	GND			GND	
63	RMII1_RXDV_CRS	GPIO3_B6_d	I		RMII RX indication signal	3.3V
64	RMII1_MDIO	GPIO3_B5_d	I/O		RMII management interface data	3.3V
65	RMII1_MDC	GPIO3_B4_d	O		RMII management interface clock	3.3V
66	RMII1_TXEN	GPIO3_B3_d	O		RMII TX data	3.3V
67	RMII1_TXD1	GPIO3_B2_d	O		RMII TX data	3.3V
68	RMII1_TXD0	GPIO3_B1_d	O		RMII TX data	3.3V
69	RMII1_CLK	GPIO3_B0_d	I/O		RMII REC_CLK output or external input	3.3V
70	RMII1_RXD1	GPIO3_A7_d	I		RMII RX data	3.3V
71	RMII1_RXD0	GPIO3_A6_d	I		RMII RX data	3.3V
72	SDMMC_D1	GPIO3_A3_d	I/O		SDMMC card data input and output	1.8V
73	SDMMC_D0	GPIO3_A2_d	I/O		SDMMC card data input and output	1.8V
74	SDMMC_CLK	GPIO3_A0_d	O		SDMMC card clock	1.8V
75	SDMMC_CMD	GPIO3_A1_d	I/O		SDMMC card command output and response input	1.8V
76	GND	GND			GND	
77	SDMMC_D3	GPIO3_A5_d	I/O		SDMMC card data input and output	1.8V
78	SDMMC_D2	GPIO3_A4_d	I/O		SDMMC card data input and output	1.8V
79	RMII0_RXDV_CRS	GPIO2_C0_d	I		RMII RX indication signal	3.3V
80	RMII0_MDIO	GPIO2_B7_d	I/O		RMII management interface data	3.3V
81	RMII0_MDC	GPIO2_B6_d	O		RMII management interface clock	3.3V
82	RMII0_TXEN	GPIO2_B5_d	O		RMII TX data enable	3.3V
83	RMII0_TXD1	GPIO2_B4_d	O		RMII TX data	3.3V
84	GND	GND			GND	
85	GND	GND			GND	
86	GND	GND			GND	
87	RMII0_TXD0	GPIO2_B3_d	O		RMII TX data	3.3V
88	RMII0_CLK	GPIO2_B2_d	I/O		RMII REC_CLK output or external input	3.3V
89	RMII0_RXD1	GPIO2_B1_d	I		RMII RX data	3.3V
90	RMII0_RXD0	GPIO2_B0_d	I		RMII RX data	3.3V
91	SARADC_IN3_GPIO4_B3_1V8	SARADC_IN3	I		SARADC 3 input signal,Hardware version identification	
92	SARADC_IN2_GPIO4_B2_1V8	SARADC_IN2	I		SARADC 2 input signal,Hardware version identification	
93	SARADC_IN1_RECOVER/KEY	SARADC_IN1	I		SARADC 1 input signal,recover system	
94	SARADC_IN0_BOOT	SARADC_IN0	I		SARADC 0 input signal, If SARADC_IN0_BOOT=0V after power-on reset, then system will enter into MASKROM mode.	
95	GND	GND			GND	
96	ACODEC_ADC_INN	ACODEC_ADC_INN	I		ADC input signal	
97	ACODEC_ADC_INP	ACODEC_ADC_INP	I		ADC input signal	

98	USB20_OTG0_DM	USB20_OTG0_DM	I/O		USB 2.0 Port0 Data signal DM	
99	USB20_OTG0_DP	USB20_OTG0_DP	I/O		USB 2.0 Port0 Data signal DP	
100	USB20_OTG1_DM	USB20_OTG1_DM	I/O		USB 2.0 Port1 Data signal DM	
101	USB20_OTG1_DP	USB20_OTG1_DP	I/O		USB 2.0 Port1 Data signal DP	
102	MIPI_DPHY_DSI_TX_CLKN	GPO4_A4_z	I/O		MIPI DSI negative differential clock transceiver output	1.8V
103	MIPI_DPHY_DSI_TX_CLKP	GPO4_A5_z	I/O		MIPI DSI positive differential clock transceiver output	1.8V
104	MIPI_DPHY_DSI_TX_D1N	GPO4_A2_z	I/O		MIPI DSI negative differential line transceiver output	1.8V
105	MIPI_DPHY_DSI_TX_D1P	GPO4_A3_z	I/O		MIPI DSI positive differential line transceiver output	1.8V
106	MIPI_DPHY_DSI_TX_D0N	GPO4_A0_z	I/O		MIPI DSI negative differential line transceiver output	1.8V
107	MIPI_DPHY_DSI_TX_D0P	GPO4_A1_z	I/O		MIPI DSI positive differential line transceiver output	1.8V
108	VO_LCDC_DEN	GPIO1_A0_d	0		LCDC RGB interface data enable,MCU interface REN signal	3.3V
109	VO_LCDC_VSYNC	GPIO1_A1_d	0		LCDC RGB interface vertical sync pulse,MCU interface CSN signal	3.3V
110	VO_LCDC_HSYNC	GPIO1_A2_d	0		LCDC RGB interface horizontal sync pulse,MCU interface WEN signal	3.3V
111	VO_LCDC_CLK	GPIO1_A3_d	0		LCDC RGB interface display clock out,MCU interface RS signal	3.3V
112	VO_LCDC_D23	GPIO1_A4_d	I/O		LCDC RGB interface data output, MCU interfacedata input/output	3.3V
113	VO_LCDC_D22	GPIO1_A5_d	I/O		LCDC RGB interface data output, MCU interfacedata input/output	3.3V
114	VO_LCDC_D21	GPIO1_A6_d	I/O		LCDC RGB interface data output, MCU interfacedata input/output	3.3V
115	VO_LCDC_D20	GPIO1_A7_d	I/O		LCDC RGB interface data output, MCU interfacedata input/output	3.3V
116	VO_LCDC_D19	GPIO1_B0_d	I/O		LCDC RGB interface data output, MCU interfacedata input/output	3.3V
117	VO_LCDC_D18	GPIO1_B1_d	I/O		LCDC RGB interface data output, MCU interfacedata input/output	3.3V
118	GND	GND			GND	

第五章 注意事项

- 接触主板时请佩戴静电手环等静电防护工具（要有良好接地）；
- 请勿带电组装、接线等操作；
- 请核对主板接口定义和外设接口定义，不能出现接错、接反；
- 请用 M3 平圆头螺丝固定主板，请勿使用沉头、规格较大的螺丝；扭螺丝时注意避免主板发生变形、弯曲；
- 注意 IO 口、串口、使能脚等电平匹配；
- 注意外接屏幕的功率，功率较大的请考虑外部供电；
- 注意产品的整体功率，选择功率足够的电源；
- 模块(核心板)的预烘烤处理：

  (1) 需要在 120±5℃条件下高温烘烤 8 小时；

  (2) 二次烘烤的模块须在烘烤后 24 小时内完成焊接，否则仍需在防潮柜内保存；