Technical Comparison

Traditional Analog Control vs BriPower EXDA Architecture

Introduction: The Evolution of Power Interface Engineering

In the sphere of high-power systems integration, the analog interface remains the critical high-fidelity bridge between digital control environments—ranging from industrial PLCs to real-time Hardware-in-the-Loop (HIL) simulators—and the physical power stage. These interfaces are responsible for the precise processing of external 0–5V, 0–10V, or 4–20mA signals to continuously modulate output parameters including voltage (VSET), current (ISET), and power (PSET). While traditional interfaces were designed for the steady-state requirements of industrial automation, the emergence of dynamic Power Hardware-in-the-Loop (PHIL) testing and the requirement for Four-Quadrant Operation (sourcing and sinking power) have necessitated a fundamental shift toward the BriPower EXDA architecture.



Figure 1 EXDA Front Panel



Figure 2 EXDA Rear Panel

Engineering an interface capable of high-fidelity closed-loop control requires navigating three primary technical challenges:

- **Galvanic Isolation:**

The imperative to break ground loops between high-power inverter stages and sensitive control hardware to prevent electrical breakdown and common-mode noise propagation.

- **EMC Immunity:**

The suppression of intense switching noise and electromagnetic interference (EMI) generated by high dV/dt and dI/dt transients during rapid semiconductor switching (SiC/IGBT).

- **Dynamic Fidelity:**

The minimization of end-to-end latency and the maximization of small-signal bandwidth to maintain phase margin and simulation stability in real-time environments.

This evolution begins with an analysis of the limitations inherent in integrated onboard designs.

Analysis of Traditional Onboard Analog Control Interfaces

The industry-standard approach for programmable power supplies typically involves integrating signal conditioning and circuit-level isolation directly onto the chassis, often terminating at the rear panel via DB25 connectors or terminal blocks. While cost-effective for static regulation, this architecture faces severe physical and electrical bottlenecks in high-speed applications.

Isolation Architectures and Mapping Logic

Traditional onboard interfaces generally utilize one of two isolation strategies:

- Digital Isolation Architecture:

This standard topology routes external signals through conditioning stages (employing inverting or differential operational amplifiers) into an ADC. Data is then passed across digital magnetic or optical isolators to the MCU/DSP. This requires an isolated DC-DC power supply and introduces significant conversion-related latency.

- Pure Analog Isolation Architecture:

This utilizes linear optocouplers or isolation amplifiers for direct transmission. While bypassing ADC/DAC delays, it is prone to linearity degradation over time due to optical aging and thermal drift.

Furthermore, these systems rely on percentage-based mapping (e.g., 0–10V representing 0–100% of the unit's rated output). This requires system integrators to perform constant model re-scaling in the external controller whenever the hardware power range is changed, increasing the risk of modeling errors.

Limitation Spotlight

- **End-to-End Latency:**

From around 100μs to several milliseconds, often causing mathematical instability in closed-loop PHIL.

- **Small-Signal Bandwidth:**

Typically restricted to < 5kHz.

- Filtering Constraints:

Use of standard RC low-pass filters with cutoff frequencies between 10Hz and 1kHz, limiting transient reproduction.

- Noise Vulnerability:

High susceptibility to switching noise (high dV/dt) due to the close physical proximity of signal conditioning to the high-power inverter stage.

The BriPower EXDA: Next-Generation FPGA-Fiber Optic Architecture

The BriPower EXDA (Analog & Digital IO Extension Box) decouples the "Signal Conditioning Layer" from the power cabinet. By utilizing a standalone hardware layer connected via a pure digital fiber-optic link, the EXDA isolates the sampling hardware from the switching transients of the inverter stage, providing a zero-noise environment for signal acquisition.

- Performance Specifications and Dynamic Fidelity

The EXDA utilizes a 500kHz sampling rate and an FPGA-driven core to reduce end-to-end latency to a maximum of 20µs. Combined with a 10kHz small-signal bandwidth, this architecture allows the ZGX host to emulate complex grid harmonics and high-frequency transients with industrial-grade fidelity.

- **Fixed-Gain Philosophy**

To eliminate the complexity of percentage-based mapping, the EXDA employs a "Fixed-Gain Philosophy." This hard-codes the physical conversion ratios, ensuring consistent control logic regardless of the power range.

Parameter	Conversion Ratio (Gain)	Application Note
Voltage Output (CV)	66.5 V/V	1V input command = 66.5V ZGX output
Current Output (CC)	10 A/V	1V input command = 10A ZGX output

The feedback signals are attenuated according to the following fixed ratios:

- Voltage Monitor: 0.0149 V/V (1V ZGX Output = 0.0149V AO signal)
- Current Monitor: 0.1 V/A (1A ZGX Output = 0.1V AO signal)

- **Physical Integrity and Customization Hub**

The EXDA is equipped with SMA female connectors featuring a locking mechanism (anti-detachment design) to ensure connectivity in high-vibration environments. The unit also serves as an Open Integration Hub, offering 4 Digital Inputs and 4 Digital Outputs (0-5V) for bespoke interlocking, synchronization pulses, and PLC handshaking.

CRITICAL SAFETY PROTOCOL: Hot Plugging Prohibited. To prevent permanent damage to the EXDA or the Device Under Test (DUT), SMA connectors must never be connected or disconnected while the system is energized.

Comparative Evaluation: Performance Differentiators and Impact

The transition to the EXDA architecture is the deciding factor in the feasibility of advanced testing scenarios like microgrid stability analysis or motor drive emulation.

Technical Comparison: Onboard vs EXDA Architecture

Comparison Dimension	Traditional Onboard Interface	BriPower EXDA (Optical)	Operational Impact
Target Application	PLC Automation; Steady-state testing	PHIL Simulation; Dynamic Emulation	Enables fourquadrant high-speed research.
End-to-End Latency	Around 100us	~20 us	Crucial for maintaining phase margin and loop stability.
Bandwidth	<5kHz	10kHz	Allows reproduction of high-order harmonics/transients.
EMI Performance	Vulnerable to high dV/dt noise	Pure digital fiber; Zero common mode noise	Prevents signal corruption from inverter switching.
Control Mapping	Percentage-based (0-10V =0-100%)	Fixed Physical Gain (e.g., 66.5V/V)	Simplifies control modeling; eliminates re-scaling.
Scalability	1-2Channels; standard I/O	8AI,4 AO, 4 IN/4 OUT DIO	Supports complex bespoke interlocking and safety logic.

The reduction in latency from around 100µs to 20µs is particularly transformative; in PHIL environments, this improvement prevents the mathematical oscillations that typically plague slower analog interfaces. Furthermore, by decoupling the sampling layer via fiber optics, the system achieves total galvanic isolation, shielding sensitive real-time simulators from the megawatt-scale transients of the power stage.

Selection Guide and Strategic Conclusion

Strategic interface selection must align with the dynamic requirements of the target application to ensure both system reliability and optimal ROI.

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- General Industrial Steady-State Testing

For standard voltage/current regulation, production-line PLC control, and response requirements in the millisecond range, the traditional onboard isolated analog interface remains a robust and cost-effective solution.

- High-Dynamic / PHIL Closed-Loop Simulation:

For applications requiring microgrid simulation (Opal-RT/RTDS), grid harmonic injection, motor drive emulation, or testing in high-noise environments, the BriPower EXDA architecture is required. Its FPGA-driven signal chain provides the necessary speed and noise immunity for stable, real-time execution..

- Engineering Summary

The shift from onboard isolation to the standalone EXDA fiber-optic architecture marks a significant advancement in power systems integration. By decoupling signal conditioning from the power stage and implementing a fixed-gain philosophy, the EXDA eliminates the bottlenecks of traditional analog control, enabling the next generation of high-precision power electronics research.